参考資料

TI Designs: TIDA-01372
シーケンシャル・ターン・アニメーション付き車載用LEDフロント・ランプのリファレンス・デザイン

概要

TIDA-01372デザインは、SEPICトポロジを使用した車載フロント・ランプ用のアナログ・ソリューションであり、シーケンシャル・ターン・アニメーションを実現します。このTI Designでは、フォルト・モード時に、低い静止電流で車両の完全な診断も行います。

リソース

TIDA-01372	デザイン・フォルダ
TPS92601-Q1	プロダクト・フォルダ
TPS7A6650-Q1	プロダクト・フォルダ
TCL555-Q1	プロダクト・フォルダ
CD71HC4017-Q1	プロダクト・フォルダ
SN74HC74-Q1	プロダクト・フォルダ
SN74AHCT1G32-Q1	プロダクト・フォルダ

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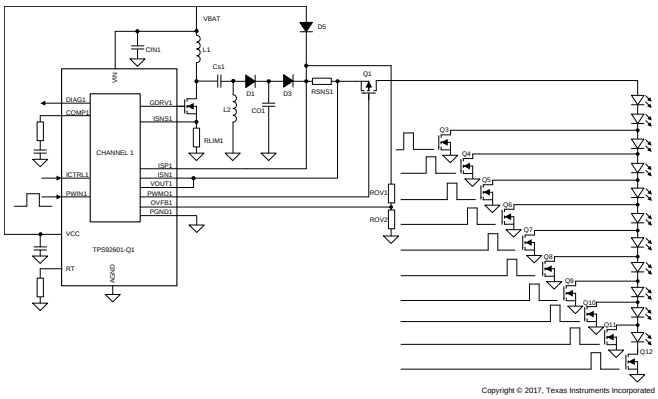
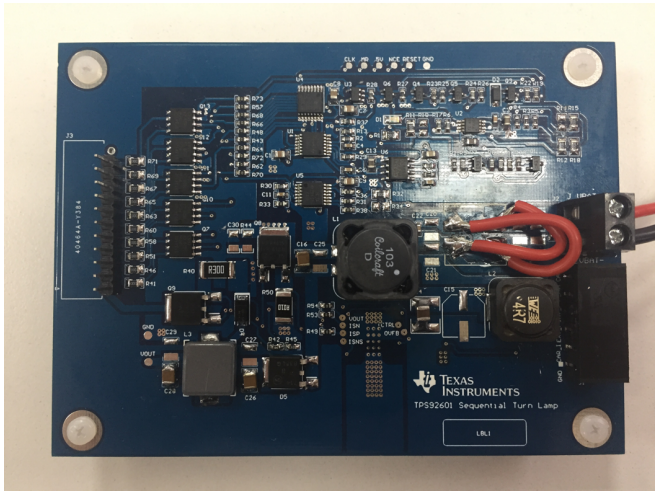
特長

- 車載バッテリに直接接続可能
- MCU不要のシーケンシャル・ターン・インジケータ
- SEPICトポロジにより広い出力電圧範囲と高い電力負荷をサポート
- 線形ソリューションよりも優れた熱特性
- 包括的な診断機能と保護機能
- フォルト・モードでの低い静止電流

アプリケーション

- 車両用フロント・ライト
- シーケンシャル・ターン・フロント・ランプ





1 System Description

The TIDA-01372 TI Design is for an automotive front light with a sequential turn indicator with full diagnostics. In this TI Design, linear light-emitting diode (LED) drivers (TPS92601-Q1) are used to drive the LEDs with constant current with SEPIC topology. The TPS7A6650-Q1 works as the power supply of the TLC555-Q1, CD74HC4017-Q1, SN74HC74-Q1, and CAHCT1G32-Q1. The EN pin is controlled by the carry in and fault signal, then the system fault will turn off the LDO and decrease system fault mode consumption current. The TPS7A6650-Q1 PG pin controls TLC555-Q1 and SN74HC74-Q1 reset pin to make sure these two devices reset out during every power down. In this TI Design, the TLC555-Q1 is used to generate a PWM as the clock of the CD74HC4017-Q1 and decide the delay time between the LED string turnon. The TLC555-Q1 also offers the clock for the SN74HC74 to generate the Carry out signal. In the design, the CD74HC4017-Q1 generates the 9 PWM on the signal to control the corresponding MOSFET turnon and turnoff in sequence. Then the SN74HC74 generates the turnon signal of the whole LED string.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage range	6 to 16 V
Output current	500 mA/Ch
Delay time for string on during sequential turn indicator	30 ms
LED number	11 s
LED type	LW-W5SG, OSRAM
Fault mode current	< 2 mA

2 System Overview

2.1 Block Diagram

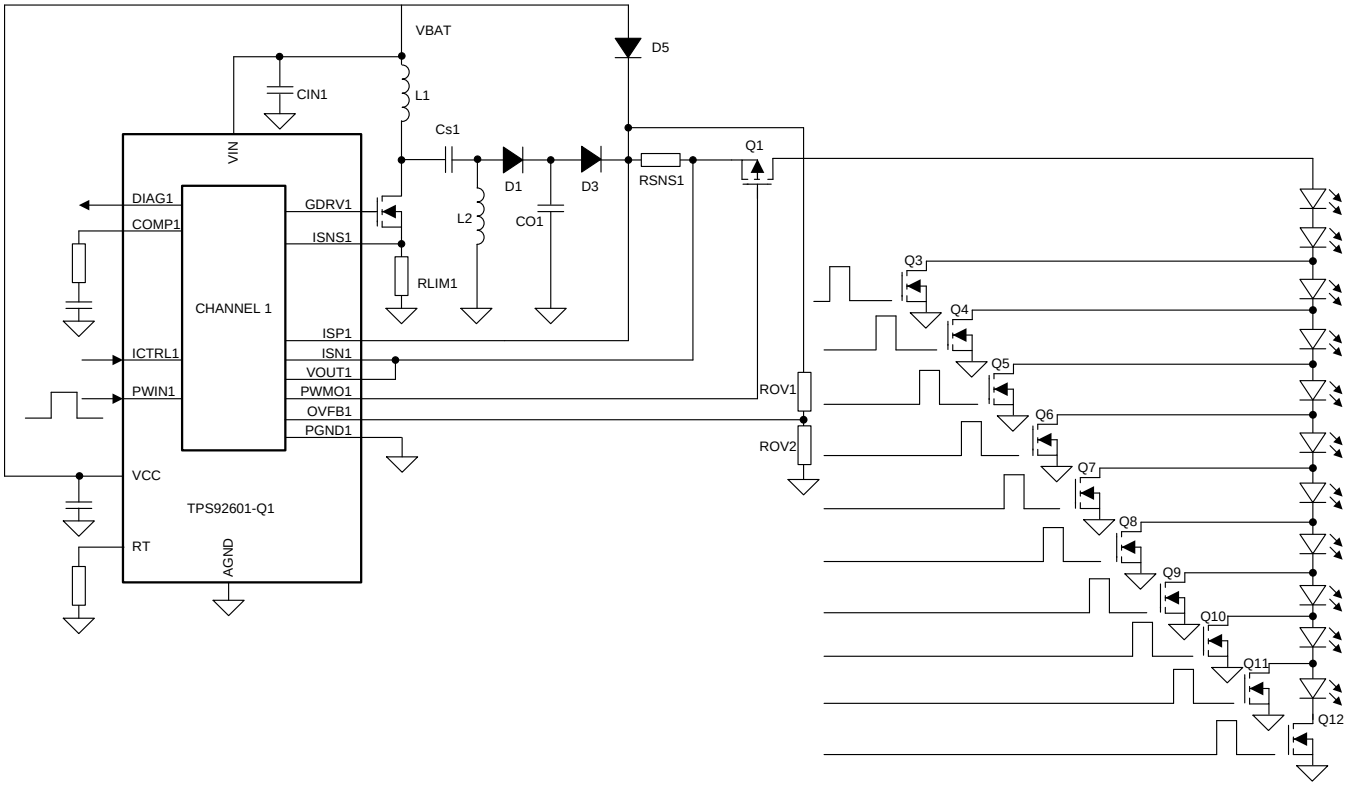


図 1. TIDA-01372 System Block Diagram

2.2 Highlighted Products

2.2.1 TPS92601-Q1—Single-Channel, High-Side Current LED Driver

The TPS92601-Q1 family of devices is a single-channel, high-side current LED driver. With full protection and diagnostics, this device is dedicated to and ideally suited for automotive front lighting. The base of this driver is a peak-current-mode boost controller. The controller has a feedback loop, a current-feedback loop with a high-side current-sensing shunt, and a voltage-feedback loop with an external resistor-divider network. The controller delivers a constant output voltage or a constant output current. The connected load determines whether the device regulates a constant output current (if the circuit reaches the current set point earlier than voltage set-point) or a constant output voltage (if the circuit reaches the voltage set point is reached first, for example, in an open-load condition). The controller supports all typical topologies such as boost, boost-to-battery, SEPIC, or flyback. Uses of the high-side PMOS FET driver are for PWM dimming of the LED string and for cutoff in case of an external short circuit to GND to protect the circuit.

2.2.2 TPS7A6650-Q1—High-Voltage, Low I_Q LDO

The TPS7A6650-Q1 is a low dropout linear regulator designed for up to 40-V V_{IN} operations. With only a 12-μA quiescent current at no load, this device is quite suitable for standby microprocessor control-unit systems, especially in automotive applications. The device features integrated short-circuit and overcurrent protection. The devices implement reset stable and in regulation. One can program the delay with an external capacitor. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

2.2.3 TLC555-Q1—Timer to Generate PWM Input for High Driver

The TLC555-Q1 is a monolithic timing circuit, which has been fabricated using the TI LinCMOS™ technology process. The timer is fully compatible with complementary metal-oxide semiconductor (CMOS), transistor-transistor logic (TTL), and MOS logic and operates at frequencies up to 2 MHz. This device uses smaller timing capacitors than those used by the NE555 because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

2.2.4 CD74HC4017-Q1—Automotive Decade Counter and Divider With 10 Decode Outputs

The CD74HC4017 is a high-speed silicon gate CMOS five-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low- to high-transition clock period of the 10 clock period cycle. The device can drive up to 10 low-power Schottky equivalent loads.

2.2.5 SN74HC74-Q1—Dual D-Type Positive-Edge-Triggered Flip-Flop With Clear and Preset

The SN74HC74 device contains two independent D-type positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK.

2.2.6 CAHCT1G32-Q1—Single Two-Input Positive-OR Gate

The SN74AHCT1G32 is a single two-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{A} \times \overline{B}$ in positive logic.

2.3 Design Considerations

The TIDA-01372 design uses a 1-pcs TPS92601-Q1 to drive one white LED string and the current string is set at 500 mA. When input V-BAT connects to battery, the LED strings will turn on by sequence with an adjustable delay time to implement sequential turn animation. The TLC555-Q1 is used to generate a PWM as a clock of the CD74HC4017-Q1 and decide the delay time between LED string turnon. The CD74HC4017 generates the nine PWM pluses to control corresponding LED turnon in sequence.

2.3.1 SEPIC LED Driver Design

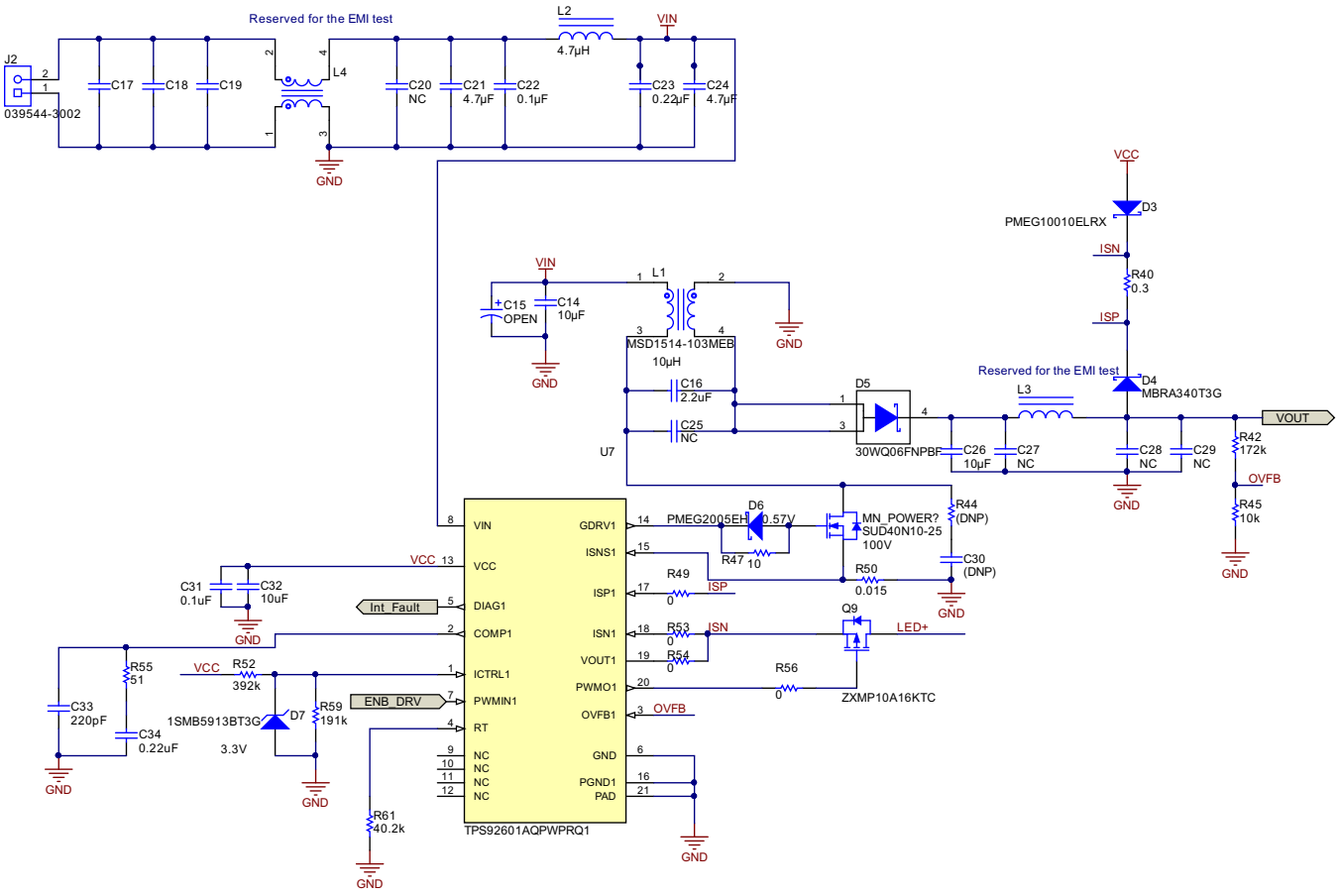


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図 2. TPS92601-Q1 SEPIC Main Power Schematic

表 2 outlines a design example.

表 2. SEPIC Design Performance Specifications

PARAMETER	TEST CONDITION	SPECIFICATIONS			UNIT
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input voltage range, V_{IN}	Connect to automotive battery	6	12	16	V
Input ripple voltage	—	—	120	—	mV
Switching frequency, f_{SW}	—	—	400	—	kHz
OUTPUT CHARACTERISTICS					
Output voltage, V_{OUT}	V_{IN} = 12 V, V_{OUT} = 33 V	6	—	33	V
Output current, I_{OUT}	—	—	0.5	—	A
Output current ripple, I_{RIPPLE}	—	–10	—	10	%
Conservative efficiency estimate, η_{EST}	V_{IN} = 12 V, V_{OUT} = 33 V	85	—	—	%

2.3.1.1 Detailed Design Procedure

To begin the design process, one must decide on the following:

- Input voltage range
- Output current
- Output voltage
- Input ripple voltage
- Output ripple current

2.3.1.2 Switching Frequency

In this TI Design, the frequency is 400 kHz. The RT pin resistor sets the switching frequency of the TPS92601-Q1 device. Use 式 1 to calculate the required value for R51. The calculated value is 31.25 kΩ. Use the nearest standard value of 31.2 kΩ.

$$R_{RT}\,(k\Omega) = \frac{12.5\ MHz \times 1\ k\Omega}{f_{OSC}\,(MHz)} \quad (1)$$

2.3.1.3 Max Output Current Set Point

The output constant of the TPS92601 is adjustable by using the external current shunt resistor. In the application circuit of 図 2, R40 is current shunt resistor, the max output current is given by 式 2.

$$R_{SENSE} = \frac{V_{SPSN\_DIFF}}{I_{SETTING}} \quad (2)$$

$$R6 = \frac{150\ mV}{0.5\ A} = 0.3\ \Omega$$

2.3.1.4 Output Overvoltage Protection Set Point

The output overvoltage protection threshold of the TPS92601 is externally adjustable using a resistor divider network. The relationship of the overvoltage protection threshold (V_{OVPT}) to the resistor divider is given by 式 3.

$$\frac{R42}{R45} = \frac{(V_{OVPT} - V_{VFB})}{V_{VFB}} \quad (3)$$

The load are 11 pcs white LED, then the LED forward voltage is about 33 V in max forward voltage. If one needs a 20% margin for the overvoltage protection, the V_{OVPT} will be: V_{OVPT} = 33 × 1.2 = 39.6 V.

So, $\frac{R42}{R45} = \frac{(39.6 - 2.2)}{2.2} = 17$. Select R45 = 10K, then R42 = 170 kΩ. Use the nearly standard value of 172 kΩ.

2.3.1.5 Duty Cycle Estimation

For further calculations, the minimum and maximum duty cycles are first estimated in continuous conduction mode (CCM). Estimate the duty cycle of the main switching MOSFET using 式 4 and 式 5.

$$D_{MIN} \approx \frac{V_{LED} + V_{FD}}{V_{LED} + V_{MAX} + V_{FD}} = \frac{33\ V + 0.5\ V}{33\ V + 16\ V + 0.5\ V} = 67.7\% \quad (4)$$

$$D_{MAX} \approx \frac{V_{LED} + V_{FD}}{V_{LED} + V_{MIN} + V_{FD}} = \frac{33\ V + 0.5\ V}{33\ V + 6\ V + 0.5\ V} = 84.8\% \quad (5)$$

where D is the duty cycle

Using and estimated forward drop of 0.5 V for a Schottky rectifier diode, the approximate duty cycle is 67.7% (minimum) to 84.8% (maximum) in max power out.

2.3.1.6 Inductor Selection

Inductors L1 and L2 could be uncoupled, but then they must be twice as large as if they are coupled. Another advantage is that if coupled inductors are used there is very small input current ripple.

The peak-to-peak ripple is limited to 30% of the maximum output current (see 式 6).

$$I_{Lrip\_max} = 0.3 \times \frac{I_{OUT} \times V_{OUT}}{V_{IN\_min}} = 0.3 \times \frac{0.5 \times 33}{6} = 0.825\ A \quad (6)$$

Because the two windings of a coupled inductor share the ripple current, the inductance value can be halved. The minimum inductor size can be estimated using 式 7.

$$L_{MIN} >> \frac{V_{IN\_min}}{2 \times I_{Lrip\_max}} \times D_{MAX} \times \frac{1}{f_{SW}} = \frac{6\ V}{2 \times 0.825\ A} \times 0.848 \times \frac{1}{400\ kHz} = 7.709\ \mu H \quad (7)$$

The near higher standard inductor value of 10 µH is selected.

式 8 and 式 9 calculate the RMS current in each winding. 式 15 and 式 16 take these currents and converts them to the ratings I_{RMS_one} and I_{RMS_both}, typically shown on the datasheets of coupled inductors. I_{RMS_one} represents only one winding conducting and I_{RMS_both} represents both windings conducting equally. The ratings are typically given for a 40°C temperature rise.

$$I_{La\_RMS} = \frac{V_{OUT} \times I_{OUT}}{V_{IN\_min} \times \eta} = \frac{33 \times 0.5}{6 \times 0.85} = 3.235\ A \quad (8)$$

$$I_{Lb\_RMS} \approx I_{OUT} = 0.5\ A \quad (9)$$

The ripple current is estimated by 式 10.

$$I_{RIPPLE} \approx \frac{V_{IN}}{2 \times L} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{16\ V}{20\ \mu H} \times 0.677 \times \frac{1}{400\ kHz} = 1.354\ A \quad (10)$$

$$I_{RIPPLE} \approx \frac{V_{IN}}{2 \times L} \times D_{MAX} \times \frac{1}{f_{SW}} = \frac{16\ V}{20\ \mu H} \times 0.848 \times \frac{1}{400\ kHz} = 1.636\ A \quad (11)$$

The worst-case peak-to-peak ripple current occurs at 84.8% duty cycle and is estimated as 0.636 A.

In a coupled inductor, the total peak current is the sum of the peak current in each winding. 式 14 calculates the peak current.

$$I_{La\_peak} = I_{IN\_min} + \frac{I_{RIPPLE}}{2} = 3.2354 + \frac{0.636}{2} = 3.5534\ A \quad (12)$$

$$I_{Lb\_peak} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 0.5 + \frac{0.636}{2} = 0.818\ A \quad (13)$$

$$I_{L\_peak} = I_{La\_peak} + I_{Lb\_peak} = \left(I_{IN\_min} + \frac{I_{RIPPLE}}{2}\right) + \left(I_{OUT} + \frac{I_{RIPPLE}}{2}\right) \quad (14)$$

$$I_{L\_peak} = 3.5534 + 0.818 = 4.3714\ A$$

For this TI Design, the peak current is estimated to be 4.3714 A. It is recommended that the saturation current of the inductor be 20% higher than the peak current or greater than the peak current limit of the IC. This leaves a margin for transient conditions when the peak inductor current may increase above the steady state value. Using the peak current limit of the IC is the most conservative criteria and ensures the inductor does not become saturated during an overcurrent fault condition. The TIDA-01372 design uses the 5.245-A typical current limit for the minimum saturation current rating.

$$I_{RMS\_one} = \sqrt{I_{La\_RMS}^2 + I_{Lb\_RMS}^2} \approx \sqrt{3.235^2 + 0.5^2} = 3.273\ A \quad (15)$$

$$I_{RMS\_both} = \sqrt{\frac{I_{RMS\_one}^2}{2}} \approx \sqrt{\frac{3.235^2 + 0.5^2}{2}} = 2.315\ A \quad (16)$$

In this TI Design, select the MSD1514-103MEB.

$$P_L = \left(I_{La\_RMS}^2 + I_{Lb\_RMS}^2\right) \times DCR = (3.273^2) \times 15 = 161\ mW \quad (17)$$

2.3.1.7 Rectifier Diode Selection

Similar to a boost converter, the average current through the diode is equal to the output current. The rectifying diode must be chosen to handle the output current and voltage at the switching node. At least a 25% margin is recommended for the diode's average current rating. A conservative design uses the maximum output current with V_{IN_max} with the typical current limit to choose the current rating. A low-forward voltage drop Schottky diode is used as a rectifier diode to reduce its power dissipation and improve efficiency. Using a 80% derating on V_{OUT} for ringing on the switch node, the rectifier diode minimum reverse breakdown voltage is given by 式 18.

$$V_{BR\_R\_min} \geq \frac{V_{VOPT} + V_{IN\_max} + V_{FD}}{0.8} = 1.25 \times 56.1\ V = 70\ V \quad (18)$$

The diode must have reverse breakdown voltage greater than 70 V. The rectifier diode peak and average currents are estimated by 式 19 and 式 20.

$$I_{D\_avg} \approx I_{OUT\_max} = 0.5\ A \quad (19)$$

$$I_{D\_peak} = I_{L\_peak} = 4.371\ A \quad (20)$$

For this TI Design, the peak current is 4.371 A.

The power dissipation in the diode is estimated by 式 21.

$$P_{D\_max} \approx V_F \times I_{OUT\_max} = 0.5 \times 0.5\ A = 0.25\ W \quad (21)$$

For this TI Design, the maximum power dissipation is estimated as 0.25 W. Reviewing the 70-V Schottky diodes, the 30WQ10FNPBF, Schottky, 100-V, 3.5-A D_{PAK} is selected. This diode has a forward voltage drop of 0.35 V at 1 A, so the conduction power dissipation is less than 170 mW and less than half its rated power dissipation.

2.3.1.8 Output Capacitor Selection

Assume a maximum LED current ripple of 0.1 × I_{LED}. Also, assume that the dynamic impedance of the chosen LED is 0.2 Ω (2.2 Ω in total for the 11-LED string). The total output voltage ripple is then calculated as follows:

$$V_{VOUT\_ripple} = 0.05\ A \times 2.2\ \Omega = 110\ mV \quad (22)$$

Assuming a ripple contribution of 95% from bulk capacitance, the output capacitor is calculated as follows:

$$C_{OUT} = \frac{I_{OUT} \times D}{V_{VOUT\_ripple} \times 0.95} \times \frac{1}{f_{SW}} = \left(\frac{0.5\ A \times 0.848}{110\ mV \times 0.95}\right) \times \frac{1}{400\ kHz} = 10.14\ \mu F \quad (23)$$

$$ESR = \frac{V_{OUT\_ripple} \times 0.05}{I_{L\_peak}} = \frac{5.5\ mV}{4.371\ A} = 1.26\ m\Omega \quad (24)$$

Select one 10-µF capacitors and ensure that the chosen capacitors meet the minimum bulk capacitance requirement at the operating voltage.

2.3.1.9 AC Capacitor (C16)

It is recommended to choose the AC capacitor (Cp) so the ripple voltage ΔV_{CP} is no more than 5% of the maximum V_{CP}DC equal to V_{IN_max}. 式 25 calculates the minimum capacitance.

$$Cp \geq \frac{I_{OUT} \times D_{MAX}}{0.05 \times V_{IN\_max} \times f_{SW}} = \frac{0.5\ A \times 0.848}{0.05 \times 16\ V \times 400\ kHz} = 1.325\ \mu F \quad (25)$$

The minimum capacitance is calculated to be 1.325 µF, and due to derating, the next highest standard value of 2.2 µF is used. This capacitor must be rated for the maximum input voltage and capacitance derating due to DC bias should be considered. The capacitor must also be rated for the RMS current (I_{CP_RMS}). This is calculated as 1.370 A using 式 26. The capacitor selected is a 2.2-µF, 63-V X7R 1206 ceramic capacitor.

$$I_{CP\_RMS} = I_{IN\_DC} \times \sqrt{\frac{\left(1 - D_{MAX}\right)}{D_{MAX}}} = 3.235 \times \sqrt{\frac{(1 - 0.848)}{0.848}} = 1.370\ A \quad (26)$$

2.3.1.10 Input Capacitor Selection

Assume that a maximum of 120 mV of the input ripple can be tolerated (2% of V_{INMIN}). Also assume that 50% of this input ripple comes from the bulk capacitance. Based on the stated design specifications, the input capacitor value is calculated using 式 27 and 式 28:

$$C_{IN} > \frac{I_{RIPPLE\_Vinmin}}{4 \times V_{IN\_RIPPLE} \times f_{SW}} = \frac{0.636\ A}{4 \times 60\ mV \times 400\ kHz} = 6.62\ \mu F \quad (27)$$

$$R_{ESR} < \frac{V_{IN\_RIPPLE}}{I_{IN\_DC}} = \frac{60\ mV}{3.235\ A} = 18.5\ m\Omega \quad (28)$$

For this TI Design, to meet a maximum input ripple of 120 mV, a minimum 10-µF input capacitor with an ESR of less than 18.5 mΩ is needed. A 2-pcs, 4.7-µF X7R ceramic capacitor is selected.

2.3.1.11 Current Sense and Current Limit

The maximum allowable current sense resistor value is limited by the inductor peak current. This limitation is given by 式 29.

$$R_{ISNS\chi} = \frac{V_{ISNS\chi}}{1.3 \times I_{L\_peak}} = \frac{100\ mV}{1.3 \times\ 4.371\ A} = 17.6\ m\Omega \quad (29)$$

A 15-mΩ resistor is selected.

2.3.1.12 Switching MOSFET Selection

The TPS92601-Q1 drives a ground referenced N-channel FET. The voltage at SW is the sum of V_{OUT} and V_{IN} plus 30% as a margin.

$$V_{BD\_MOS\_min} \geq \left(V_{VOPT} \times V_{IN\_max}\right) \times 1.3 = 1.3 \times 55.6\ V = 77.3\ V \quad (30)$$

An N-channel FET with a breakdown voltage of 100 V is selected.

The $R_{DS(on)}$ and gate charge are estimated based on the desired efficiency target.

$$P_{DISS\_total} \approx P_{OUT} \times \left(\frac{1}{\eta} - 1\right) = 33\ V \times 0.5\ A \times \left(\frac{1}{0.85} - 1\right) = 2.912\ W \quad (31)$$

For a target of 85% efficiency with a 16-V input voltage at 1 A, the maximum power dissipation is limited to 2.912 W. The main power dissipating devices are the MOSFET, inductor, diode, current sense resistor, and the integrated circuit, the TPS92601-Q1 device.

$$P_{FET} < P_{DISS\_total} - P_L - P_D - P_{RSNS\chi} - V_{IN\_max} \times I_{VDD} \quad (32)$$

$$I_{Q\_peak} = I_{La\_peak} + I_{Lb\_peak} = 4.371\ A \quad (33)$$

$$I_{Q\_RMS} = I_{OUT} \times \sqrt{\frac{\left(V_{OUT} + V_{IN\_min} + V_{FD}\right) \times \left(V_{OUT} + V_{FD}\right)}{V_{IN\_min}^2}} = 0.5 \times \sqrt{\frac{(33 + 6 + 0.5) \times (33 + 0.5)}{6^2}} = 3.031\ A \quad (34)$$

The SUD40N10-25 ($R_{DS(ON)}$ = 20 mΩ and Q_{GD} = 9 nC) is selected in this TI Design. The gate drive current I_G of the TPS92601-Q1 is 0.7 A. The estimated power loss is:

$$P_{FET} = I_{Q\_RMS}^2 \times R_{DS(on)} \times D_{MAX} + \frac{\left(V_{IN\_min} + V_{OUT}\right) \times I_{Q\_peak} \times Q_{GD} \times f_{OSC}}{I_G} \quad (35)$$

$$= 3.031\ A^2 \times 0.02\ \Omega \times 0.848 + \frac{(39\ V + 4.471\ A) \times 9 \times 10^{-9}\ nC \times 400\ kHz}{0.7\ A} = 0.1558 + 0.897 = 1.0528\ W$$

2.3.1.13 Loop Compensation

Select a large compensation capacitor (1 μF) and small compensation resistor (51 Ω) as the compensation network in the schematic. details in Section 2.12 of the application report *Using the TPS55340 as a SEPIC Converter* (SLVA516)[6].

2.3.1.14 SEPIC Startup Diode

Since the minimum common-mode voltage of ISP1 and ISN1 of TPS92601-Q1 and there is no current charge loop for ISP1 and ISN1 in SEPIC topology, it needs one startup diode D1 from VCC to ISP1 to charge ISP1 and ISN1 common-mode voltage higher than 4V. In normally application, there are serval uFs cap in the output, so it needs diode to block the ISN1 to VOUT path for charging ISP1 quickly in case of trigger latch fault. D3 is put in here for this function; it is suggested to select schottky with low forward voltage to improve total efficiency.

2.3.2 CLK and Turnon Delay Time Design

To implement 9 separated PWMs with adjustable shift delay time, CD74HC works for 8-bit parallel-out serial shift registers, in the design, connect pin A and pin B to VCC directly, so the Qx High shift time just depend on CLK. In this design, the TLC555-Q1 device is used to generate CLK input signal, as 図 3 shows. The following paragraphs describe how to set the CLK period and duty cycle.

- $t_H = 0.693\ (R_{35} + R_{39})C_{13}$
- $t_H = 0.693\ (R_{39})C_{13}$
- period = $t_H + t_L = 0.693\ (R_{35} + 2R_{39})\ C_{13}$

- CLK = 0.693 × (1 + 2 × 45.3) × 10^3 × 0.47 × 10^{-6} = 29.84 ms

So the LEDs will turn on with a 29.84-ms shift delay by sequence.

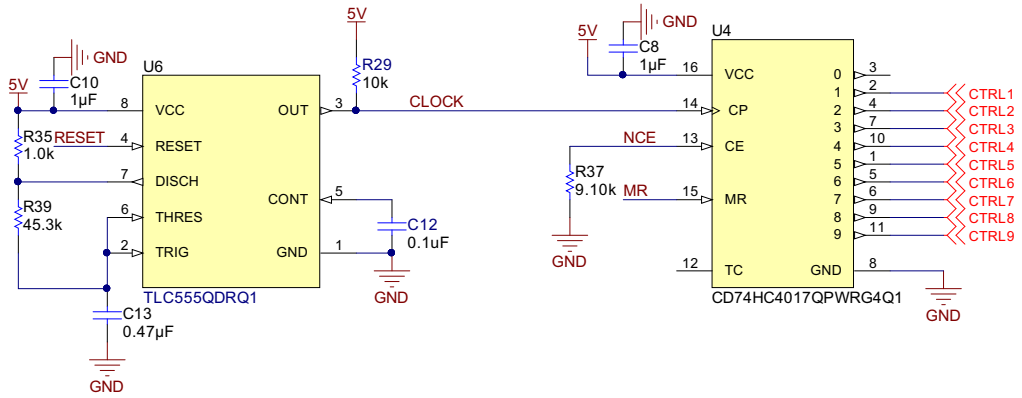

図 3. CLK and PWM Generator Schematic

2.3.3 LED Driver Enable Sequence Control

The first PWM output of the TLC555-Q1 is longer than the setting frequency due the device start up. In this TI Design, Q7A should be turned on before the SEPIC circuit starts working; the TPS92601-Q1 PWMIN needs around a 1-ms high to enable the device and latch the on status. Therefore, design the delay circuit to control the LED driver enable sequence, make sure the first turnon time is equal to the other turnon time, and keep the TPS92601-Q1 turnon until the SN74HC74-Q1(U5B) is clear.

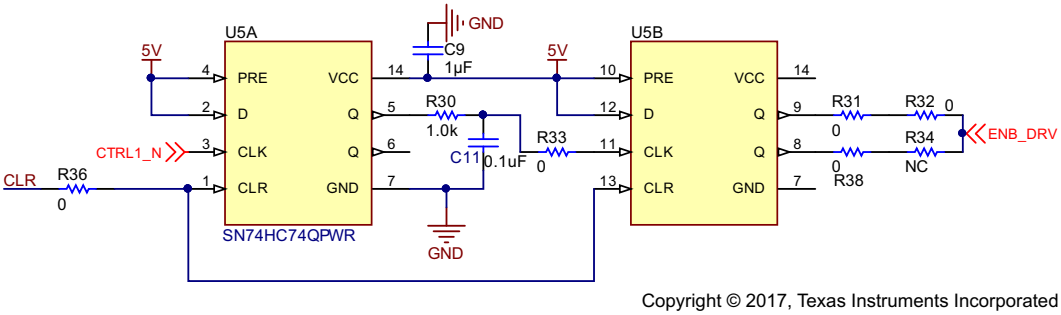

図 4. LED Driver Enable Control Schematic

For the All LED on control, when CTRL9 signal is rolled out, generate the NCE signal to keep the output state at no change until the MR status is changed in the next cycle.

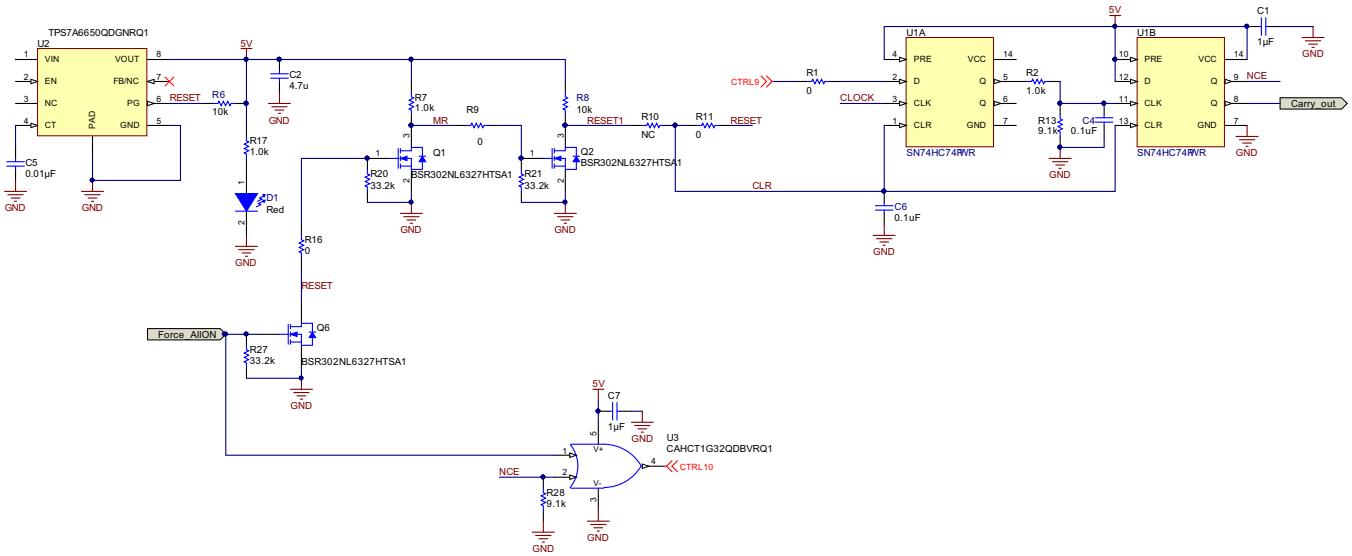

図 5. All LED ON Control Schematic

2.3.4 Low I_Q in Fault Mode

If any fault happens, the TPS7A6650-Q1 will also turn off the output. There is no current consumption of the TLC555-Q1, CD74HC4017-Q1, SN74HC74-Q1, CAHCT1G32-Q1 and TPS92601; this TI Design gets the low I_Q during the fault mode.

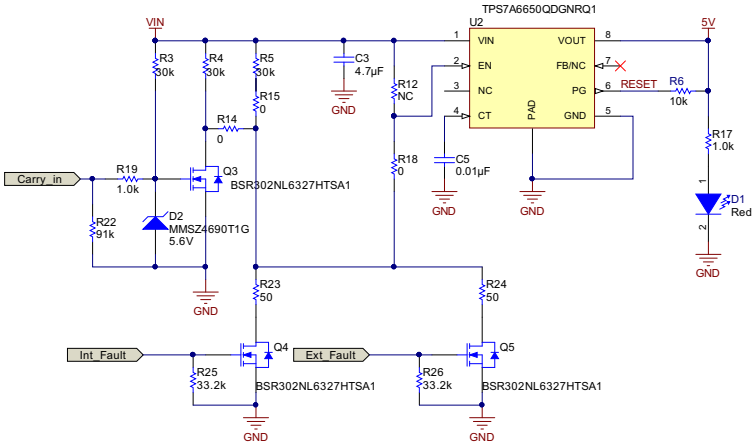

図 6. Low I_Q of Fault Mode Schematic

3 Getting Started Hardware

Connecting a 12-V DC supply through the PWM mode high-side driver with 0.5 s on and 0.5 s off to the onboard input connector (J2) lights up the LED in sequential turn indicator. Connect each LED of the LED string to J3 as shown in 図 8.

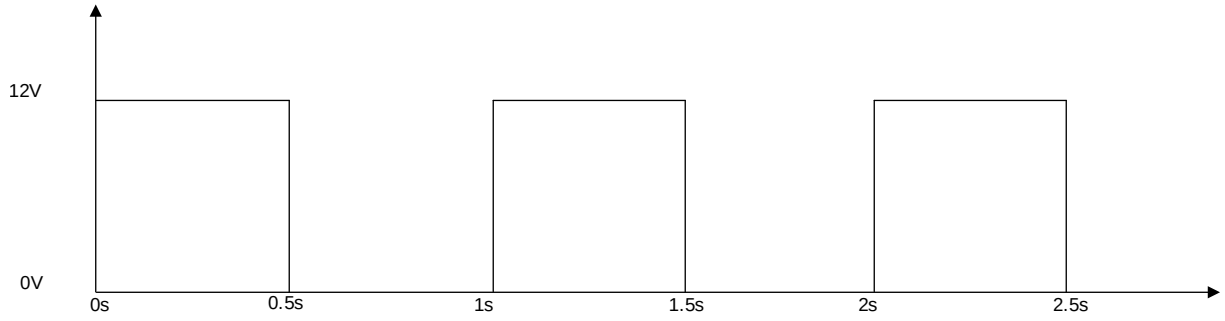

図 7. Input Voltage of Turn Mode

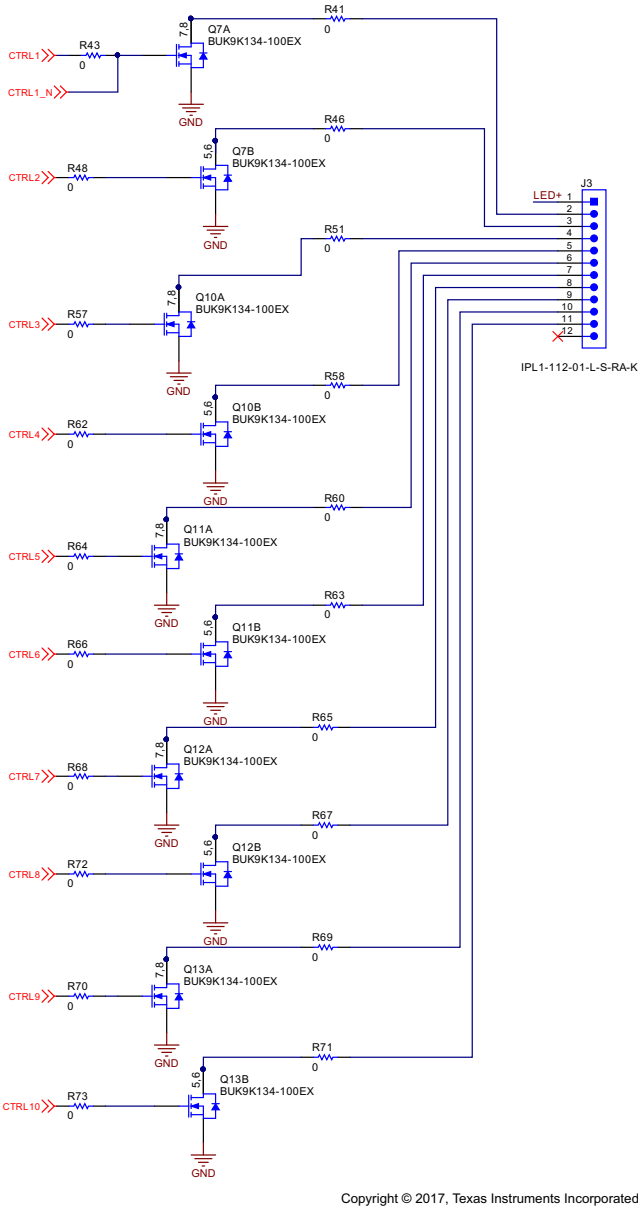

図 8. LED Connection Schematic

4 Testing and Results

4.1 Waveforms

注: For 図 9 and 図 10, CH1 is the clock generated by the TLC555-Q1; CH2 is the CTRL1 signal; CH3 is PWNIN1 of the TPS92601-Q1; and CH4 is CTRL2.

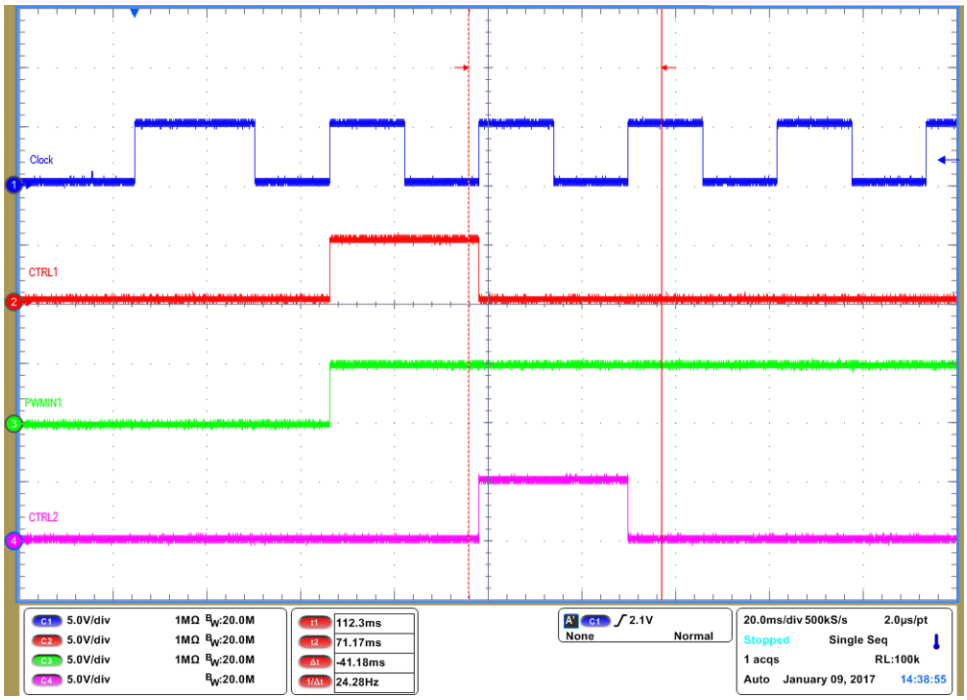

図 9. LED Turnon Control Sequence

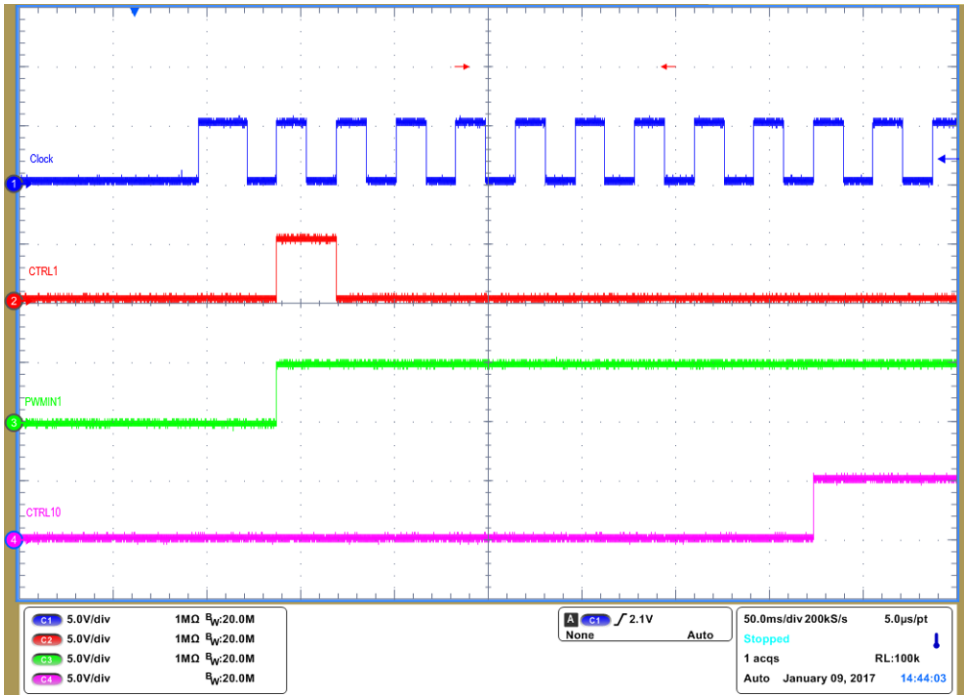

図 10. LED Turnon Control Sequence With Full On

注: For 図 11 and 図 12, CH1 is the clock generated by the TLC555-Q1; CH2 is the CTRL1 signal; CH3 is V_{OUT} of the SEPIC circuit; and CH4 is the LED string current.

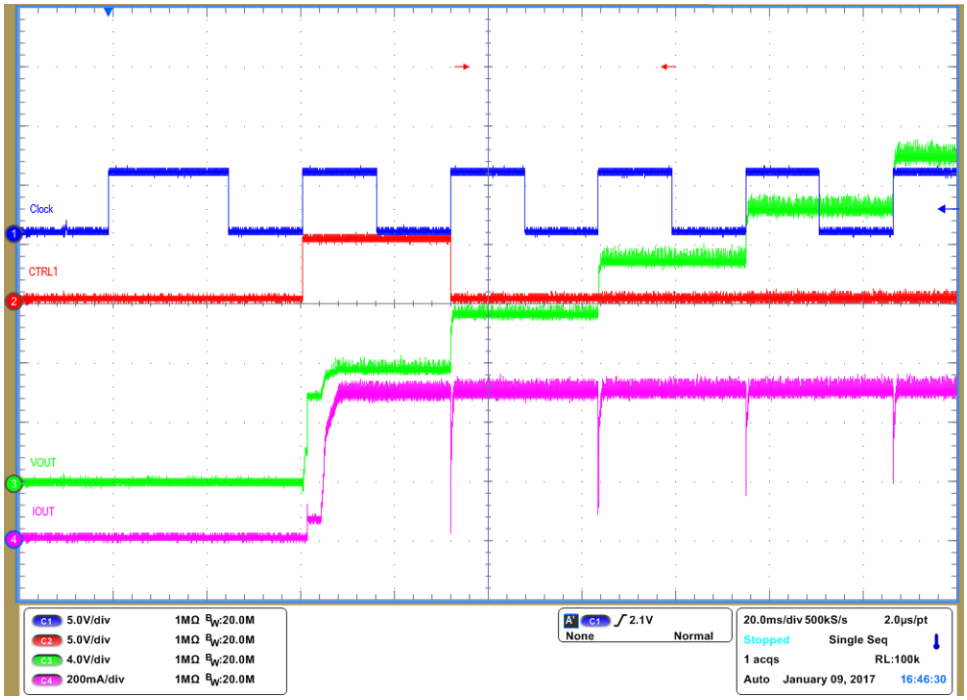

図 11. LED String Voltage and Current During Turnon

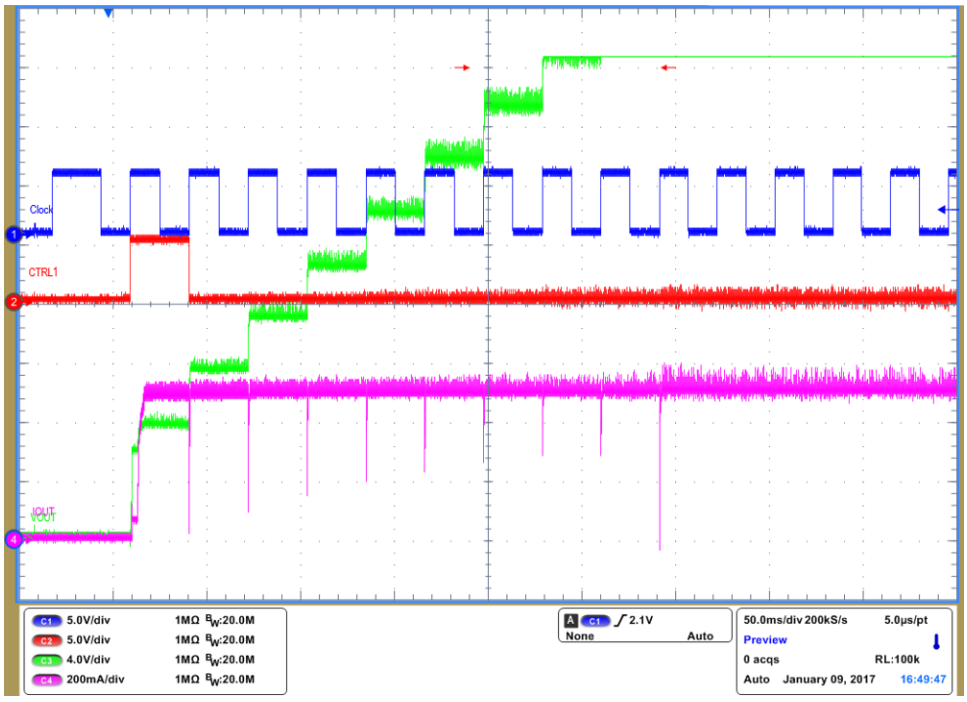

図 12. LED String Voltage and Current After Turnon

4.2 Fault Mode Consumption Current

Test condition: V_{IN} = 12 V, free-air temperature

表 3. Board Consumption Current of Fault Mode

FAULT	I_Q WITH SHUTDOWN LDO
Internal fault	1.179 mA
External fault	1.179 mA

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01372.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01372.

5.3 PCB Layout Recommendations

The performance of any switching regulator depends as much on the layout of the PCB as the component selection. Follow these simple guidelines to maximize noise rejection and minimize the generation of EMI within the circuit:

- Discontinuous currents are the most likely to generate EMI; therefore, take care when routing the following paths. The main paths for discontinuous current in the TPS92601-Q1 SEPIC regulator are discontinuous and require careful attention to layout. Keep these loops as small as possible and the connections between all the components short and thick to minimize parasitic inductance. In particular, make the switch node (where L1, D5, and MN_POWER1 connect) just large enough to connect the components. To minimize excessive heating, place large copper pours adjacent to the short current path of the switch node.
- The RT, COMP, ISNS, ICTRL, OVFB, ISP, and ISN pins are all high-impedance inputs, which couple external noise easily. Therefore, minimize the loops containing these nodes whenever possible. In some applications, the LED or LED array can be far away (several inches or more) from the TPS9260x-Q1 family of devices, or on a separate PCB connected by a wiring harness. When using an output capacitor where the LED array is large or separated from the rest of the regulator, place the output capacitor close to the LEDs to reduce the effects of parasitic inductance on the ac impedance of the capacitor.
- Separate and connect AGND and PGND at the input GND connector.
- Separate the control signal as low noise circuit with switching power loop.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01372.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01372.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01372.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01372.

6 Related Documentation

1. Texas Instruments, *TPS9260x-Q1 Single- and Dual-Channel Automotive Headlight LED*, TPS92601-Q1 Datasheet (SLUSBP5)
2. Texas Instruments, *TPS7A66xx-Q1 High-Voltage Ultra-Low IQ Low-Dropout Regulator*, TPS7A66xx-Q1 Datasheet (SLVSBL0)
3. Texas Instruments, *TLC555-Q1 LinCMOS™ TIMER*, TLC555-Q1 Datasheet (SLFS078)
4. Texas Instruments, *CD74HC4017-Q1 HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED*, CD74HC4017-Q1 Datasheet (SCLS546)
5. Texas Instruments, *SN74HC74-Q1 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET*, SN74HC74-Q1 Datasheet (SCLS577)
6. Texas Instruments, *Using the TPS55340 as a SEPIC Converter* , TPS554340 Application Report (SLVA516)

6.1 商標

7 About the Author

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