参考資料

TI Design: TIDA-01352
400W連続、スケーラブル、±2.5～±150V、プログラム可能な超音波電源のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDA-01352デザインは、超音波伝送回路を駆動するための、デジタル・プログラミング可能な電源により、モジュール化された高効率の電源スケーリング能力を実現します。このデザインはプッシュプル・トポロジを使用して、高電圧(HV)、低電圧(LV)、中電圧(MID)の電源を生成します。HVレールは±50～±150Vの範囲でプログラム可能、LVまたはMIDレールは±2.5～±50Vの範囲でプログラム可能です。電源は各レールで継続的に100Wの電力を供給できます。このプログラム能力は、オンボードの12ビット・デジタル/アナログ・コンバータ(DAC)を使用して実装されています。すべての電源レールは、マスタ・クロックと同期可能です。このデザインはスケーラブルでモジュール化されているため、チャネルの数やパルサーのレベル数に応じて、同じ電源を追加または除去できます。また、このデザインには、パルサーの動作に必要な他のLV電源も含まれています。このTI Designは、HV、DC/DCブースト段を、フローティング(ポスト)レギュレータ・デザインTIDA-01371と組み合わせて使用するために最適です。

リソース

TIDA-01352	デザイン・フォルダ
TIDA-01371	デザイン・フォルダ
LM5030	プロダクト・フォルダ
DAC60004	プロダクト・フォルダ
CSD19506KCS	プロダクト・フォルダ
CSD17381F4	プロダクト・フォルダ
TLV171	プロダクト・フォルダ
TLV2171	プロダクト・フォルダ
LMZ34202	プロダクト・フォルダ
LMZ34002	プロダクト・フォルダ
CDCE937	プロダクト・フォルダ
TPS7A49	プロダクト・フォルダ
REF5050	プロダクト・フォルダ

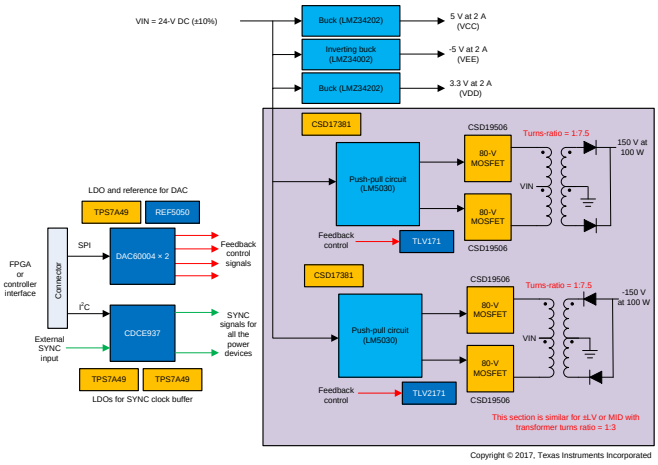
TI E2E™ Community　E2Eエキスパートに質問

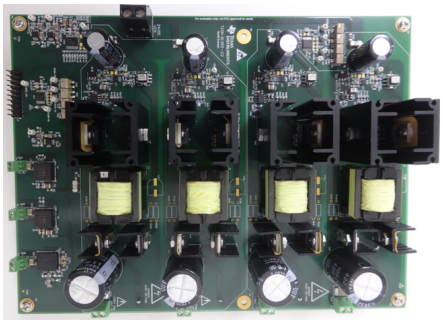
特長

- 高効率(24V入力、全負荷で89%)のプッシュプル・トポロジにより、より低いまたは高い電力(チャネル数)にスケーリング可能
- 正電圧と負電圧の電源が独立しているため、最大192のデジタル・パルサーおよびリニア・アンプ転送チャネル用のバイポーラ機能を実現可能
- モジュール化設計により、パルサーのレベル数に応じて同じ電源を追加または除去することが可能
- 超音波マスタまたはシステム・クロック周波数とのスイッチング周波数の同期が可能 - より優れた高調波の除去が可能
- オンボードのクワッド12ビットDACにより、±2.5V～±150Vの範囲で出力のデジタル・プログラミングが可能(各レールは100Wの連続電力と350Wのピーク電力をサポート)
- パルサー・ドライバ(Bモード、CWモード、エラストグラフィー・モードをサポート)、内蔵レベル・シフタ、およびロジック用の共通電源により、単一基板のデザインに統合

アプリケーション

- 医療用超音波スキャナ
- ソナー・イメージング機器
- 非破壊検査機器





1 System Description

The TIDA-01352 enables modular and efficient power scaling capabilities by providing a solution for digitally programmable power supplies to power ultrasound transmit circuits.

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. It uses high-voltage ultrasound signals to actuate the sensor, transmits those signals inside human body, and receives the echo on the same line. This needs a high-voltage power supply that is programmable, scalable, and able to drive more number of channels.

Sonar imaging equipments transmit sound pulses and convert the returning echoes into digital images, much like a medical ultrasound sonogram. The advantage is that they can "see" what is going on through dark or turbid (cloudy) water in zero visibility conditions. Because the principle of operation is the same as ultrasound scanners, the power supply requirements are also similar.

Nondestructive evaluation is a wide group of analysis techniques used in the science and technology industry to evaluate the properties of a material, component, or system without causing damage. Ultrasonic testing (UT) is part of the family of non-destructive testing techniques based on the propagation of ultrasonic waves in the object or material tested. In most common UT applications, very short ultrasonic pulse-waves with center frequencies ranging from 0.1 to 15 MHz, and occasionally up to 50 MHz, are transmitted into materials to detect internal flaws or to characterize materials. A common example is ultrasonic thickness measurement, which tests the thickness of the test object, for example, to monitor pipework corrosion.

1.1 Key System Specifications

表 1 shows different characteristics and their specifications of TIDA-01352 board.

表 1. Key System Specifications for TIDA-01352

CHARACTERISTICS	SPECIFICATIONS
Input voltage (V_{IN})	24 V ± 10%
VMAIN-Positive	50 to 150 V at 100 W nominal
VMAIN-Negative	–50 to –150 V at 100 W nominal
VMID-Positive	2.5 to 50 V at 100 W nominal
VMID-Negative	–2.5 to –50 V at 100 W nominal
3.3 V (logic supply for pulser)	3.3 V at 2 A
5 V (pulser level shifter)	5 V at 2 A
–5 V (pulser level shifter)	–5 V at 2 A
Programming capability	Digital
DAC resolution	12 bits
Control voltage range from DAC	0 to 5 V
External clock synchronization	Yes
External SYNC frequency range	100 to 500 kHz

2 System Overview

2.1 Block Diagram

図 1 shows the TIDA-01352 block diagram. The design has three main sections: push-pull section for ±HV power supply, push-pull section for ±LV or MID power supply, and point-of-load (PoL), low-voltage power supplies.

The HV and LV or MID power supply sections are identical with change in transformers. Both use PWM controller LM5030 and CSD19506KCS power MOSFETs to implement power supplies for generation of positive and negative rails to power the TX devices. ±HV rails are programmable in terms of voltage from ±50 to ±150 V, whereas the ±LV or MID rails are programmable in terms of voltage from ±2.5 to ±50 V. The programmability is implemented using two separate 12-bit, highly-linear DAC60004 devices. The outputs from DACs are compared and signal processed using op-amps TLVx171 to change the feedback of the LM5030 circuit. To power the DAC, TPS7A4901 is used to generate 5.3 V. REF5050 generates 5 V for REFIN of the DAC. The push-pull controller LM5030 requires an input circuit (for VCC generation), which is implemented using CSD17381 and 11-V Zener diodes.

Each TX device also requires low-voltage PoL power supplies for internal level-shifters and digital circuitry. The power module LMZ34202 generates a VDD of 3.3 V. The VCC and VEE supplies are generated using LMZ34202 and LMZ34002 respectively.

All the power supply rails should be synchronized to a master clock, which is implemented using CDCE937. CDCE937 generates seven SYNC outputs from a single external SYNC clock on the input. Two TPS7A4901 devices are used to power CDCE937. The entire board is sized in 165-mm × 220-mm size. The ±HV and ±LV or MID rails are scalable in terms of power and show modular approach for the designer to increase the power rails.

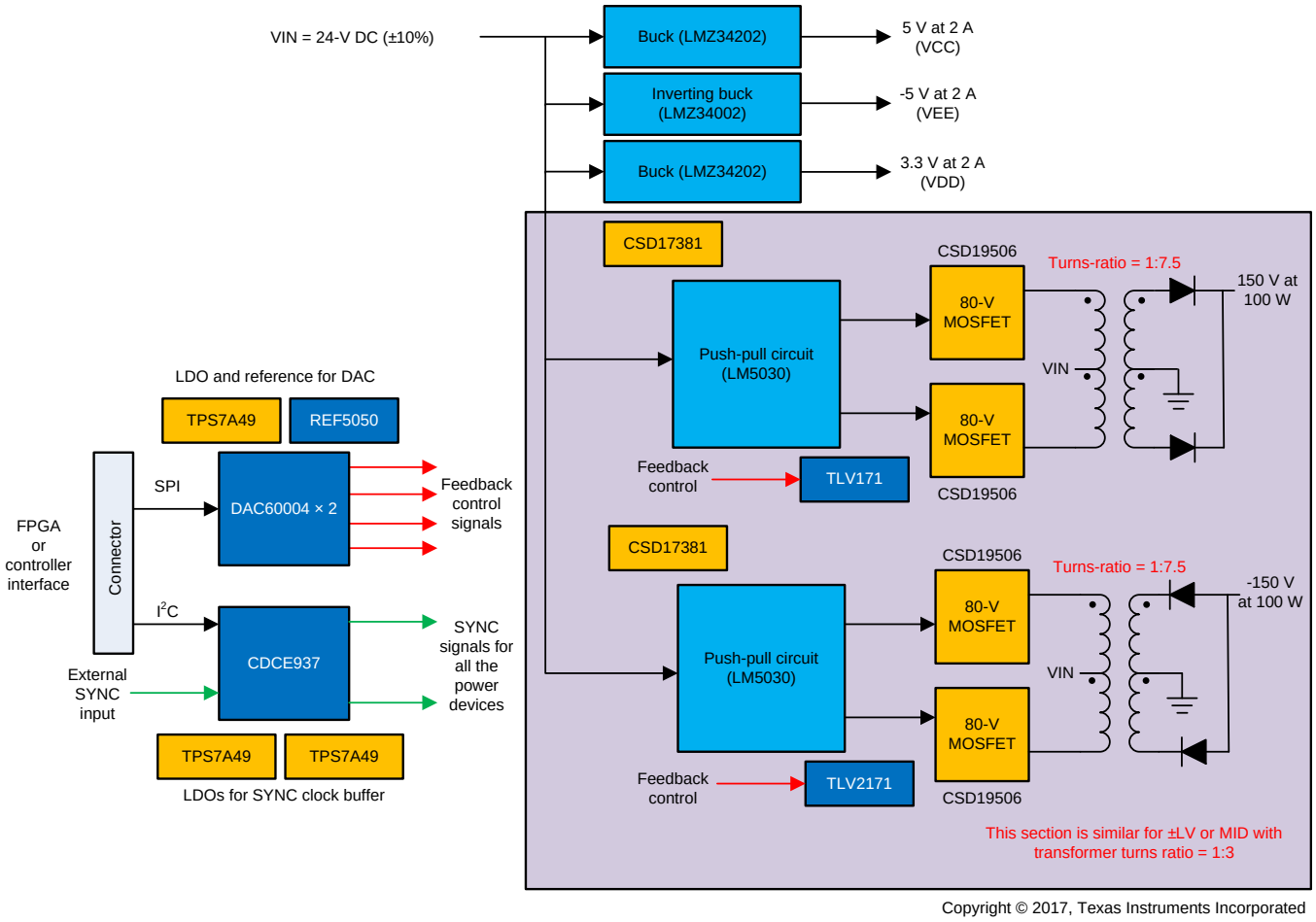


図 1. System Block Diagram for TIDA-01352

2.2 System Design Theory

2.2.1 Basic Ultrasound System

In an ultrasound system, the transmitter that generates HV signals to excite a transducer is one of the critical components in the entire ultrasonic diagnostic system. There are semiconductor devices available, which can generate HV signals to ensure the penetration depth of ultrasonic signals. A generic system level block diagram for cart-based ultrasound scanner is shown in 図 2.

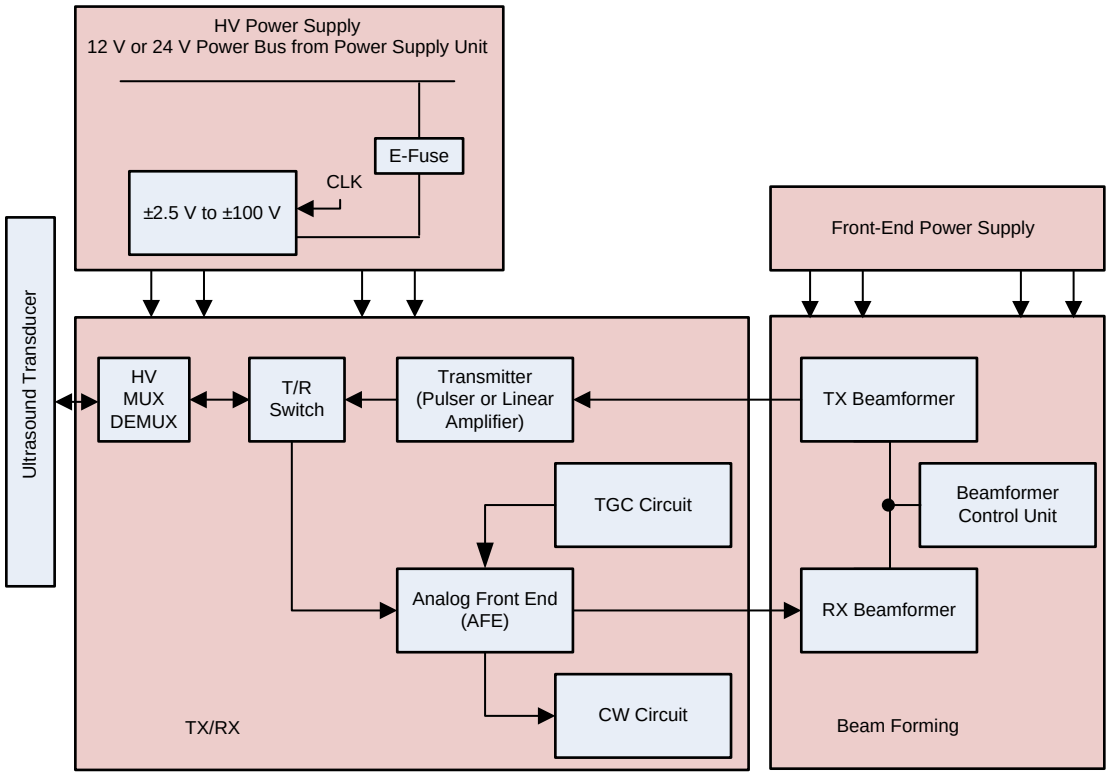


図 2. System Level Block Diagram for Cart-Based Ultrasound Scanners (Full Block Diagram Not Shown)

The high-voltage pulses are applied to the piezoelectric crystals in the transducer which generate ultrasound waves that traverse through the body and the reflected echo consists of information, such as blood flow, organs, tissues, and so on. These pulses applied are usually bipolar in nature and generated by transmit devices.

There are two modes in general:

1. Pulse mode (also known as B- or M-mode) where high-voltage pulses (up to –100 V and 100 V typically) are transmitted for short time only
2. Continuous (CW) mode where low-voltage (±2.5 to ±10 V typically) pulses are continuously transmitted by half the piezo elements in the transducer while the other half act as receive

It is important to note that same power supply is used for both the modes meaning the output of power supply is ranging from ±2.5 to ±100 V. This powering scheme is typically implemented using a switched mode power supply (SMPS) followed by regulators as shown in 図 3. Within pulse mode, there is a special mode called Elastography mode. The voltages in Elastography modes can go up to ±150 V. The current requirements is huge (sometimes more than >100 A) for a short period of time (may be tens of microseconds). Delivering such high currents at the high voltages without dropping the output voltage is a challenge. To cover for the droop in output voltage, a high value of capacitors is also used at the output of SMPS. The focus of this document is the SMPS only.

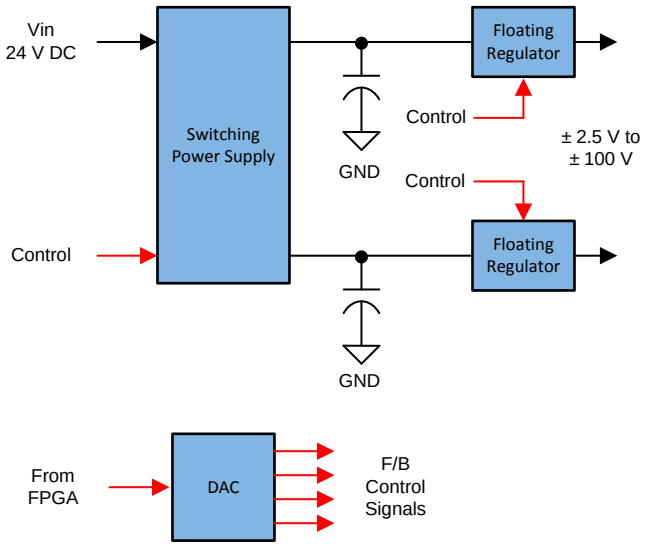


図 3. Typical Power Supply Scheme in Medical Ultrasound Application

In order to feed the ultrasound transmitter sections, the power supply board must generate, from a 24-V (or sometimes 12-V) DC input, one positive and one negative HV rail up to 100 V and −100 V, respectively. These rails should be digitally programmable. Sometimes the TX pulser is operated in different modes, which require four such rails (refer to 2.2.2.1 and 2.2.2.2). The TX devices also require low-voltage rails: VDD (typically 3.3 V) for internal logic supply, VCC, and VEE for internal level-shifters (typically ±5 V). The power supply should be capable of synchronizing to the ultrasound master or system clock frequency. Most ultrasound systems use frequency in the range of 100 to 500 kHz.

Before going into design and details of the power supply, it is important to understand some basic nomenclatures used in the ultrasound scanners.

2.2.2 Pulser and Linear Amplifier

There are two types of transmitter devices available—one is called pulser and other one known as linear amplifier. Both these devices generate HV signals to drive transducers, but they have specific requirement on the driving front as well as use case.

A pulser uses a combination of PMOS and NMOS switches and operates with square wave input signals. When FFT is taken for the output of a pulser, it has higher odd harmonics (because of square wave) and affects image quality. The advantage is that the pulser is extremely low power as the PMOS and NMOS switches only operate when there is input square wave (see 図 4).

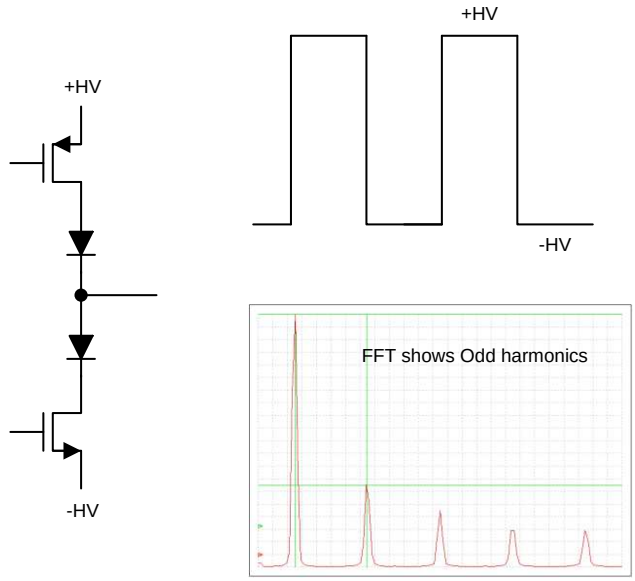


図 4. Pulser—Output Waveform and FFT of Output

Linear amplifier is a simple amplifier which takes approximately 2 Vp-p input signal and generates 180 Vp-p (or 200 Vp-p depending upon the requirement). The linear amplifier is a pure amplifier, which just amplifies sine wave and thus will not have harmonics when FFT is taken, which helps in improving the image quality. The drawback is that this amplifier has higher power consumption because of biasing of the amplifier while in operation and quiescent power consumption when not operating (see 図 5).

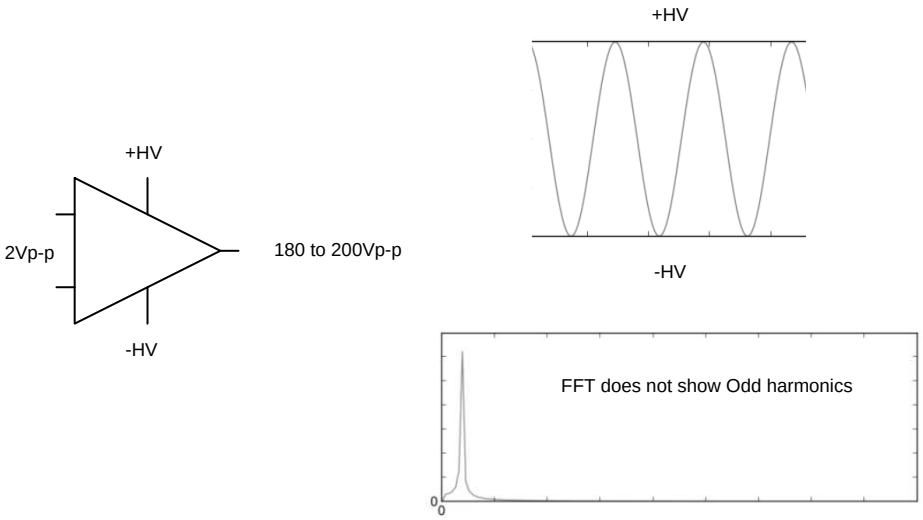


図 5. Linear Amplifier—Output Waveform and FFT of Output

In short, there is trade-off between the two approaches in terms of power consumption and image quality. In most cases, pulsers are used in low- and medium-end ultrasound systems, whereas linear amplifiers are used in high-end or premium ultrasound systems. One additional cost drawback with linear amplifiers is that a DAC is required for driving the input because FPGA beam-former only outputs digital. The DAC would also consume power, take up space, and require a reference, but there is a way to get rid of the harmonics even in low- and medium-end ultrasound systems. In case, a pulser is used for the transmit section, there are two mainly used nomenclatures: three-level and five-level.

2.2.2.1 Three-Level Pulser

A pulser, which can generate the output from +HV to 0 to –HV, is called a three-level pulser. The pulser has only three levels as shown in example 図 6.

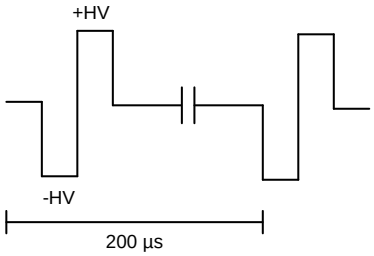


図 6. Three-Level Pulser Output Waveform

2.2.2.2 Five-Level Pulser

A pulser which can generate five levels to get the output waveform more closely to a sine wave is called a five-level pulser. The pulser has levels as +HV, +MID, 0, –MID, and –HV. An example waveform is shown in 図 7.

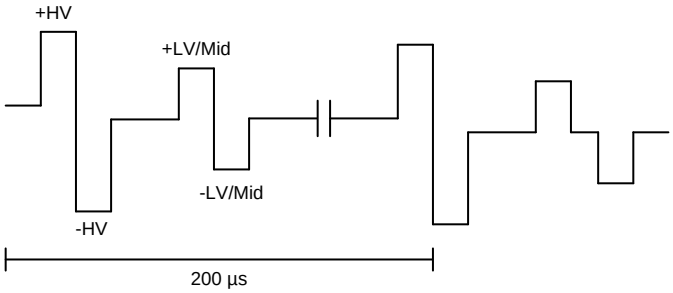


図 7. Five-Level Pulser Output Waveform

2.3 Design Considerations

This section explains the design theory for the topology and component selection for the design.

2.3.1 Selecting Devices

2.3.1.1 Selecting Topology for HV and LV or MID Power Supply Rails

The power supply for ultrasound pulsers must have variable or programmable outputs for both positive and negative rails. The power levels for both the rails also vary per the pulser level-types and modes used in the ultrasound scanners. This requirement needs a topology, which is scalable in terms of power. There are some modes where power levels can go up to 500 W. Push-pull topology is the most suitable topology as it is scalable in terms of power. Push-pull topology has both the switches (MOSFETs) referred to ground, which means there is no high-side switch requiring special treatment (like driver and isolation). Push-pull topology is a derivative of two forward converters operating 180° out of phase. This configuration allows operation in the first and third quadrant of the hysteresis loop with better usage of the

magnetic core of the transformer. The maximum voltage stress of the switching MOSFETs is twice the input voltage, which is the same as the forward topology. A current mode PWM converter avoids runaway of the flux core by monitoring the current of each of the push-pull transistors and forcing alternate current pulses to have equal amplitude. Also, synchronization to external clock is possible in push-pull topology and is a mandatory feature required for the power supplies.

2.3.1.2 Selecting Push-Pull Controller and MOSFETs

LM5030 is a high-voltage PWM controller that contains all of the features required to implement push-pull topology in current-mode control. The device provides two alternating gate driver outputs. The LM5030 includes a high-voltage start-up regulator that operates over a wide input range of 14 to 100 V. The device has total propagation delays less than 100 ns and a 1-MHz capable single-resistor adjustable oscillator. The output voltages range from ±2.5 to ±150 V for the ultrasound pulse power supply, which means the duty cycle of the controller should be able to take such big dynamic range. LM5030 can support this dynamic range also. The requirement to choose MOSFETs for push-pull topology is that they should be able to handle a stress of $2 \times V_{IN(max)} = 2 \times 26.4 = 52.8$ V. CSD19506KCS is 80-V MOSFET with very high current rating of 100-A peak. The package is able to handle heat using external heat-sink.

2.3.1.3 Selecting DAC, Reference, and Power for DAC

To cover the entire range of output voltages, a DAC is used to change the feedback of the push-pull controller. The requirements for the DAC are:

- Resolution: 12 bits at least
- Linearity: 1 LSB INL
- Channel count: quad
- Low temperature drift: few µV/C

DAC60004 is a suitable device for this application. The device accepts reference voltage from 2.2 V to VDD. The drift for reference is very important. REF5050 is suitable for the device, which can generate 5-V reference. The power supply for the DAC can be generated using TPS7A4901.

2.3.1.4 Selecting Buck Converters for LV Requirements

While powering a pulser, there are some requirements of 3.3-V, 5-V, and –5-V rails. Each of the rails should support the following needs:

1. V_{IN} = 24 V
2. V_{OUT} = programmable
3. I_{OUT} = up to 2 A. The ICs should be synchronizable to external clock frequency of 100 kHz to 1 MHz.

LMZ34202 and LMZ34002 devices are suitable for these requirements.

2.3.1.5 Selecting Clock Buffer

The clock buffer should meet the following requirements:

1. At least seven outputs (four outputs for four LM5030 devices, one output for 5-V generation, one output for –5-V generation, one output for 3.3-V generation)
2. Clock frequency range: 100 kHz to 1 MHz (表 2 shows the SYNC frequencies for the devices used in the design)
3. If possible, divide-by-2 options should be available

表 2. SYNC Frequency Range for the Devices Used in TIDA-01352

SYNC SIGNAL CONNECTION	DEVICE	SYNC CLOCK FREQUENCY RANGE	SYNC CLOCK SIGNAL THRESHOLD
U1 (positive supply for HV output)	LM5030	100 kHz to 1 MHz	3.2-V typical
U4 (negative supply for HV output)	LM5030	100 kHz to 1 MHz	3.2-V typical
U9 (–5-V generation)	LMZ34002	400 kHz to 900 kHz	1.9-V typical
U14 (positive supply for LV or MID output)	LM5030	100 kHz to 1 MHz	3.2-V typical
U17 (negative supply for LV or MID output)	LM5030	100 kHz to 1 MHz	3.2-V typical
U8 (5-V generation)	LMZ34202	200 kHz to 1 MHz	2-V minimum
U7 (3.3-V generation)	LMZ34202	200 kHz to 1 MHz	2-V minimum

The input clock for clock buffer is externally available *SYNC* signal, which is also the *master clock* signal in ultrasound systems. The signal synchronizes all the power supply ICs on the board.

表 3. Power Supply for CDCE937

RECOMMENDED OPERATING CONDITIONS						
			MINIMUM	NOMINAL	MAXIMUM	UNIT
V_{DD}	Device supply voltage		1.7	1.8	1.9	V
V_O	Output Yx supply voltage, V_{DDOUT}	CDCE937	2.3	—	3.6	V
		CDCEL937	1.7	—	1.9	V

The CDCE937 is a modular, PLL-based, low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. The device generates up to seven output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz using up to three independent configurable PLLs. The CDCE937 has separate output supply pins: VDD, which is 1.8 V, and V_{DDOUT}, which is 2.3 to 3.3 V for CDCE937 (see 表 3). The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable, which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

2.3.2 Push-Pull Circuit Design

There are four push-pull circuits used—two for generating positive and negative supplies in *HV* section and other two for generating positive and negative supplies for *LV or MID* power supply.

注: This section explains the LM5030 circuit for *Positive Supply for HV Circuit* only, but the circuit is similar for other three sections except the feedback circuits and transformers.

2.3.2.1 Input Section and Turnon Mechanism

As shown in 図 8, the input voltage for this design is 24-V DC (considering ±10%, the range is from 21.6-V to 26.4-V DC). The LM5030 contains an internal high-voltage startup regulator. The input pin (VIN) can be connected directly to line voltages as high as 100 V. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. In this TI Design, one 11-V Zener diode is used to power the VCC pin through a MOSFET CSD17381F4. This will keep the VCC voltage greater than 8 V, which effectively shuts off the internal startup regulator and saving power and reduces the controller

dissipation. The *LM5030 100-V Push-Pull Current Mode PWM Controller*[6] recommends a capacitor for the VCC regulator between 0.1 to 50 μF. This design uses 22 μF in parallel with 0.1 μF. When the voltage on the VCC pin reaches the regulation point of 7.7 V, the controller outputs are enabled. The outputs will remain enabled unless VCC falls below 6.1 V, the SS or SHUTDOWN pin is pulled to ground, or an overtemperature condition occurs.

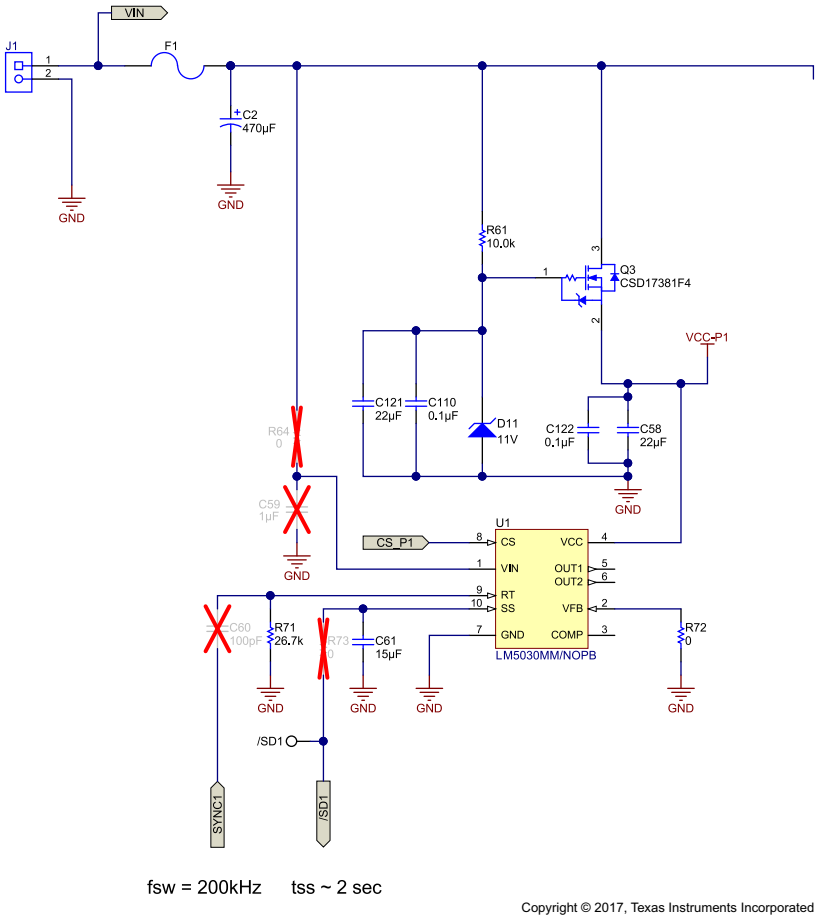


図 8. Input Section and Turnon Mechanism for LM5030

2.3.2.2 *Oscillator Frequency Setting*

The operating frequency of the power supply should be selected to obtain the best balance between switching losses, total transformer losses, and size and cost of magnetic components and output capacitors. High-switching frequency reduces the output capacitor value and the inductance of the primary and secondary windings and therefore, the total size of the transformer. In the same manner, higher-switching frequency increases the transformer losses and the switching losses of the switching transistor. These high losses reduce the overall efficiency of the power supply and increase the size of the heat-sink required to dissipate the heat.

Each output switches at half the oscillator frequency in a push-pull configuration. Assuming f_{SW} is 100 kHz: $f_{OSC} = 2 \times f_{SW} = 2 \times 100$ kHz = 200 kHz. The LM5030 oscillator is set by a single external resistor, which is connected between the RT pin and the return. To set a desired oscillator frequency, the RT resistor can be calculated as in 式 1.

$$RT = \frac{\left(\frac{1}{F}\right) - 172 \times 10^{-9}}{182 \times 10^{-12}} \quad (1)$$

Where:

- f = 200 kHz
- RT = 26.5 kΩ

The resistor value can also be approximated using the graph in 図 9, which is taken from the *LM5030 100-V Push-Pull Current Mode PWM Controller*[6].

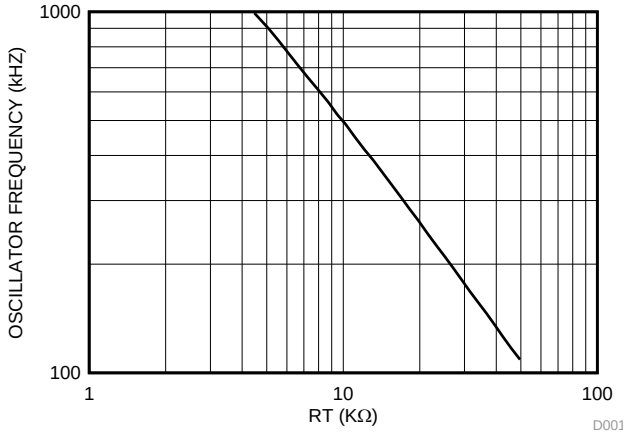


図 9. LM5030 Oscillator Frequency versus RT

2.3.2.3 Synchronizing External Clock

The LM5030 can also be synchronized to an external clock. The external clock must be of higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitive coupled into the RT pin with a 100-pF capacitor. A peak voltage level greater than 3 V with respect to ground is required for detection of the SYNC pulse. The SYNC pulse width should be set in the 15- to 150-ns range by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to a nominal 2 V. Locate the RT resistor close to the device and connected directly to the pins of the IC (RT and GND). The SYNC input pulse width must be between 15 and 150 ns and have amplitude of 1.5 to 3.0 V at the SYNC pad on the board. The pulses are coupled to the LM5030 through a 100-pF capacitor as specified in the *LM5030 100-V Push-Pull Current Mode PWM Controller*[6] datasheet. For TIDA-01352, SYNC option is available through a test-point as shown in 図 8. The capacitor C60 is 100 pF as per the recommendation in the *LM5030 100-V Push-Pull Current Mode PWM Controller*[6].

2.3.2.4 Soft Start and Shut Down

The soft-start feature allows the converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. An internal 10-µA current source and an external capacitor generate a ramping voltage signal that limits the error amplifier output during start-up. In the event of a second level current limit fault, the soft-start capacitor will be fully discharged which disables the output drivers. When the fault condition is no longer present, the soft-start capacitor is released to ramp and gradually restart the converter. The SS pin can also be used to disable the controller. If the SS pin voltage is pulled down below 0.45 V (nominal), the controller will disable the outputs and enter a low power state. Using the standard formula for current in a capacitor Using this equation, and assuming I is 10 µA, t is 1 second, and dV is 1.4 V (VCOMP for LM5030), the result is C_{SS} = 6.8 µF.

$$I = C \times \frac{dV}{dt} \tag{2}$$

2.3.2.5 OUT1, OUT2, and Time Delay

The LM5030 provides two alternating outputs, OUT1 and OUT2. The internal gate drivers can each sink 1.5-A peak each. The maximum duty cycle for each output is inherently limited to less than 50%. The minimum duty cycle is 0%. The typical dead-time between the falling edge of one gate driver output and the rising edge of the other gate driver output is 135 ns (see 図 10) .

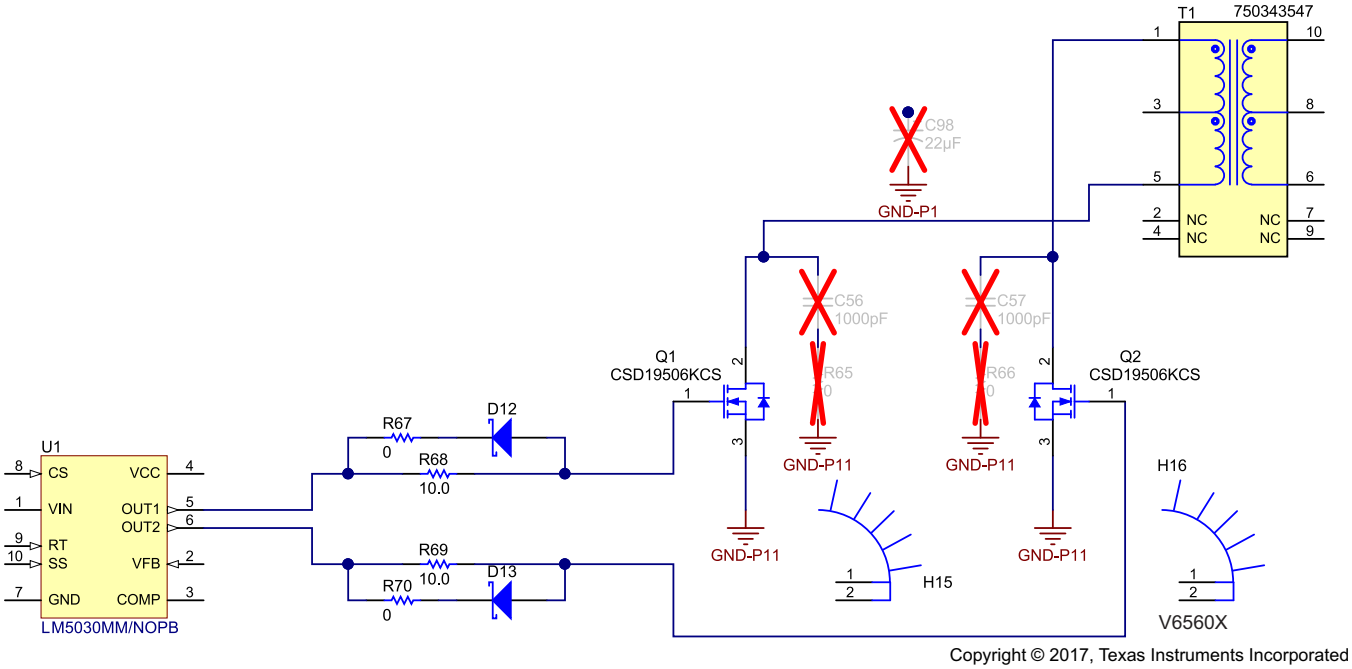


図 10. LM5030 Driving MOSFETs

2.3.2.6 Power MOSFETs

The voltage stress on MOSFETs for a push-pull power stage is twice the maximum input voltage (plus 15% margin for transformer leakage).

$$\text{Voltage Stress on MOSFETs} = 2 \times VIN_{(max)} + 15\% \text{ Margin} = (2 \times 26.4) + (0.15 \times 2 \times 26.4) = 60.72 \text{ V} \tag{3}$$

The power MOSFETs (CSD19506KCS) are chosen because they have a drain-to-source voltage rating of 80 V and a drain current rating of at least 10 A. There is a provision for snubber circuit to be connected across the MOSFET to avoid any excess ringing while switching the MOSFETs.

The maximum voltage drop across the switching MOSFET during the on time is calculated as 式 4.

$$V_{DS(on)} = \frac{\left(P_{o(max)} \times R_{DS(on)}\right)}{\left(\text{Transformer Efficiency} \times V_{IN(min)}\right)} = 8.7 \text{ mV} \quad (4)$$

2.3.2.7 Current Sensing Using Current Transformer

Monitoring the input current provides a good indication of the circuit's operation. If an overload condition should exist at the output (a partial overload or a short circuit), the input current would rise above the nominal value shown in 図 11. Current transformer, in conjunction with D9, R2, R62, R63, and C55, provides a voltage to pin 8 on the LM5030 (CS), which is representative of the input current flowing through its primary. If the voltage at the first current sense comparator exceeds 0.5 V, the LM5030 disables its outputs, and the circuit enters a cycle-by-cycle current limit mode. If the second level threshold (0.625 V) is exceeded due to a severe overload and transformer saturation, the LM5030 will disable its outputs and initiate a soft-start sequence.

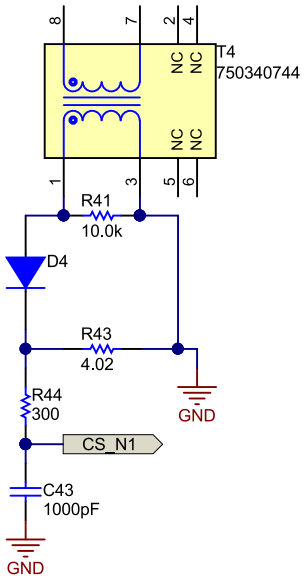


図 11. Current Sense Circuit

2.3.2.7.1 Selecting Turns Ratio for CT and Sense Resistor

The turns ratio for CT depends upon Ipk (primary) and bleeder resistor. The CS pin voltage should not be more than 0.5 V, or cycle-by-cycle protection will trigger. Assume CT turns ratio is 1:100, so with Ipk (primary) at 10 A, the result is 式 5.

$$R_{sense} = \frac{(0.5 \times 100)}{10} = 5\Omega \quad (5)$$

This TI Design uses CT from Wurth Elektronik™ (part number 750340744) with turns ratio of 1:100.

The current sensed through CT and bleeder resistor (R62) is filtered using a low-pass RC filter with cutoff frequency of 530 kHz. This helps in cleaning the current sense signal before feeding to CS pin of LM5030. R2 (10 kΩ) is used for resetting the core.

注: For the ±HV sections, the current sense resistor is selected to be 4.02 Ω to facilitate Elastography mode of testing. For ±LV or MID sections, the current sense resistor is the same as the calculated value of 5 Ω.

2.3.2.7.2 Calculating Turns Ratio for Push-Pull Transformer

The turn ratio for the ±HV output is as shown in 式 6.

$$n_{HV} = \frac{V_{O(max)}}{2 \times V_{IN} \times D_{max}} = \frac{155}{2 \times 24 \times 0.45} = 7.17 \quad (6)$$

The selected turns ratio is $n_{\pm HV}$ = 7.5.

The design uses push-pull transformer (part number 750343547) from Wurth Elektronik. The transformer can accept 24-V DC at the primary and switch between 100 to 400 kHz. The output is 110 V at 1 A with operating temperature range of –40°C to 125°C.

The turn ratio for the ±LV or MID output is as shown in 式 7.

$$n_{LV\,or\,MID} = \frac{V_{O(max)}}{2 \times V_{IN} \times D_{max}} = \frac{55}{2 \times 24 \times 0.45} = 2.5 \quad (7)$$

The selected turns ratio is $n_{\pm LV/Mid}$ = 3.1.

The design uses push-pull transformer (part number 750343548) from Wurth Elektronik. The transformer can accept 24-V DC at the primary and switch between 100 kHz to 400 kHz. The output is 55 V at 2 A with operating temperature range of –40°C to 125°C.

Both the transformers are designed to comply with the requirements (basic insulation for a primary circuit at a working voltage of 150 V_{PEAK}) as defined by IEC60601-1.

2.3.2.8 Output Rectifier and Filtering

For each of the HV and LV or MID outputs, the rectifier and output filter circuits are designed as per the following sections.

Diode stress = 2 × V_{IN} × n = 2 × 24 × 7.5 = 360 V.

The design uses diode with reverse voltage rating of 600 V and 10 A of forward current capacity. The forward voltage drop is 1.3 V at 2 A.

2.3.2.8.1 Calculating Output Inductor

L ≥ (n × V_{IN} – V_O) × D_{max} / (0.2 × I_O) × f_{SW} = 338 µH with current rating of 2-A minimum. The design uses 470-µH inductors with 4-A continuous current rating.

2.3.2.8.2 Calculating Output Capacitor

$C_{OUT(MIN)}$ = (0.2 × I_O) / (8 × f_{SW} × ΔV_{OUT}) = 40-µF minimum with voltage rating of 300 V at least. The design uses 100-µF capacitors at the output. For stability, it is good to have a smaller value ceramic capacitor (1 µF) in parallel with the bulk capacitor.

2.3.2.8.3 Output Rectifier and Filtering for Positive and Negative Rails

図 12 and 図 13 show the output rectifier diodes at the secondary of transformers. Note that for positive and negative outputs only direction of diode is reversed. The values of output inductor (470 µH), output capacitors (100 µF in parallel with 1-µF ceramic), and transformers remain the same.

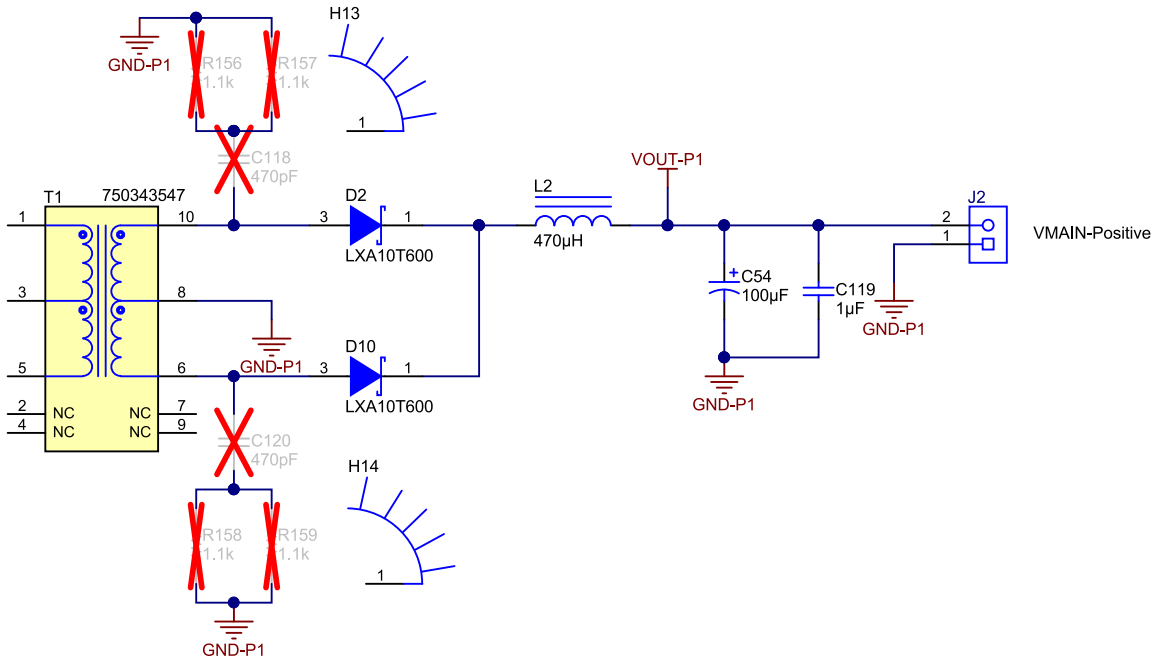


図 12. Output Rectifier and Filtering for Positive Output

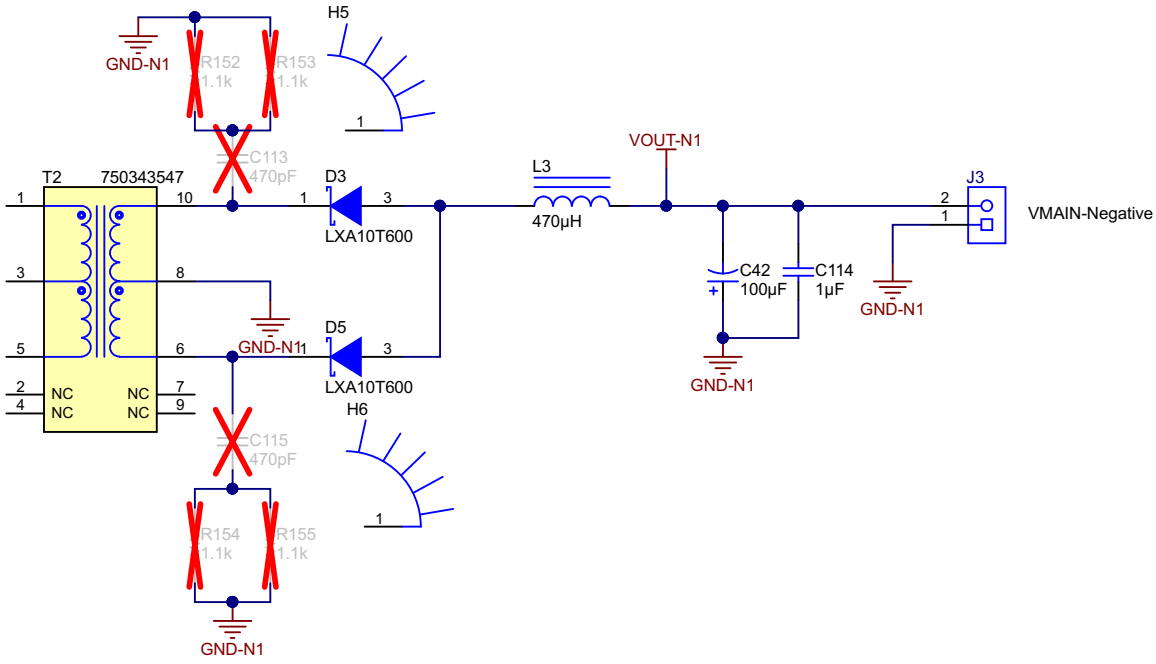


図 13. Output Rectifier and Filtering for Negative Output

2.3.2.9 Setting Output Using Feedback Circuit

The outputs are set using op-amp based circuits which compare a fraction of output voltage with control voltage from DAC.

2.3.2.9.1 Setting Output for Positive Rail for HV Section

The feedback circuit for positive rail uses a comparator based on TLV171 to compare the output voltage with control voltage set by DAC. The V_{OUT} for the +HV section varies from 50-V to 150-V DC. The gain is set to 0.03226 (= 10 k / 310 k). This gain gives the value of control voltage to be well within the maximum output from DAC, which is 5 V, at VOUT-P1 = 150 V (see 図 14). Once the fraction of output VOUT-P1 compared with control voltage VCON-A1, the output of U2 drives the transistor Q4. R76 (47 kΩ) and R78 (10 kΩ) are used for scaling the output of U2 to drive Q4. The collector of Q4 is used to pull down or pull up the voltage on COMP (pin 3) of LM5030 (U1) based on the result of comparison between output and control voltage. R75 (1 kΩ) and C62 (1 µF) form compensation network for COMP pin.

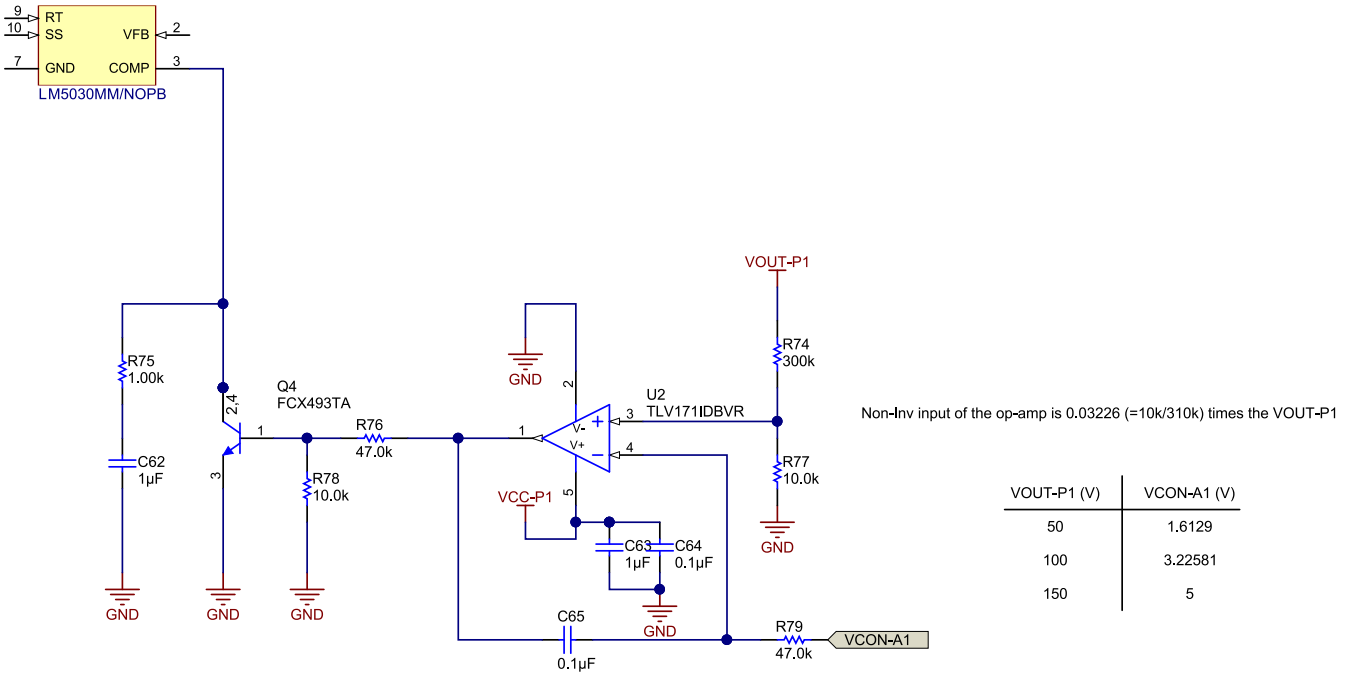


図 14. Feedback Circuit for Positive Rail for HV Section

図 15 shows the TINA™ simulation, and 図 16 shows the waveforms for VOUT-P1 = 50 to 150 V.

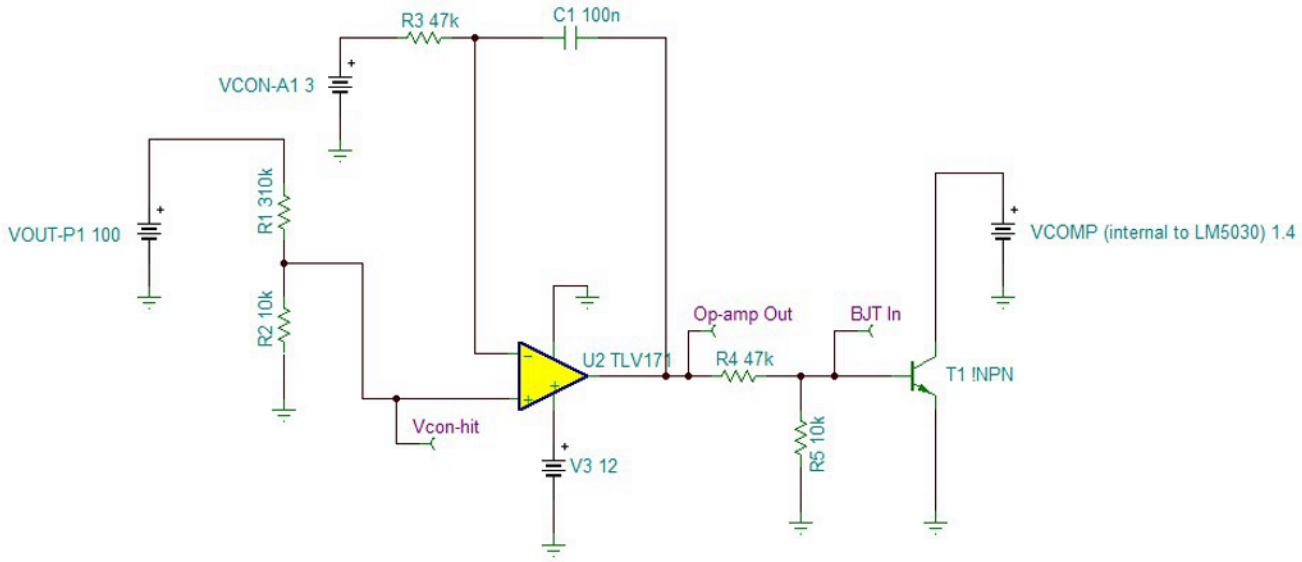


図 15. TINA Simulation for Feedback Circuit for Positive Rail for HV Section

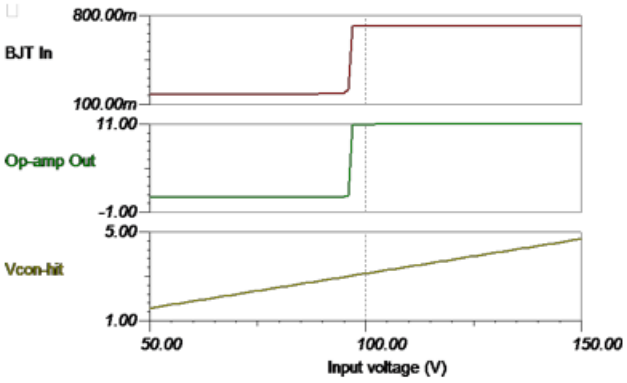


図 16. Simulation Waveform Showing Linearity (+HV Output)

2.3.2.9.2 Setting Output for Negative Rail for HV Section

The feedback circuit for negative rail uses an inverter and a comparator based on TLV2171 to invert and compare the output voltage with control voltage set by DAC. The V_{OUT} for the HV section varies from –50-V to –150-V DC. The gain is set to –0.03226 (= 10 k / 310 k). This gain gives the value of control voltage to be well within the maximum output from DAC, which is 5 V at VOUT-N1 = –150 V (refer to 図 17). Before comparing the fraction of output VOUT-N1 with control voltage, the fraction is inverted using an inverting amplifier U5B. Once the fraction is inverted, it is compared with control voltage VCON-B1, which is the output of U5A drives the transistor Q8. R57 (47 kΩ) and R58 (10 kΩ) are used for scaling the output of U5A to drive Q8. The collector of Q8 is used to pull down or pull up the voltage on COMP (pin 3) of LM5030 (U4) based on the result of comparison between output and control voltage. R55 (1 kΩ) and C50 (1 µF) form compensation network for COMP pin.

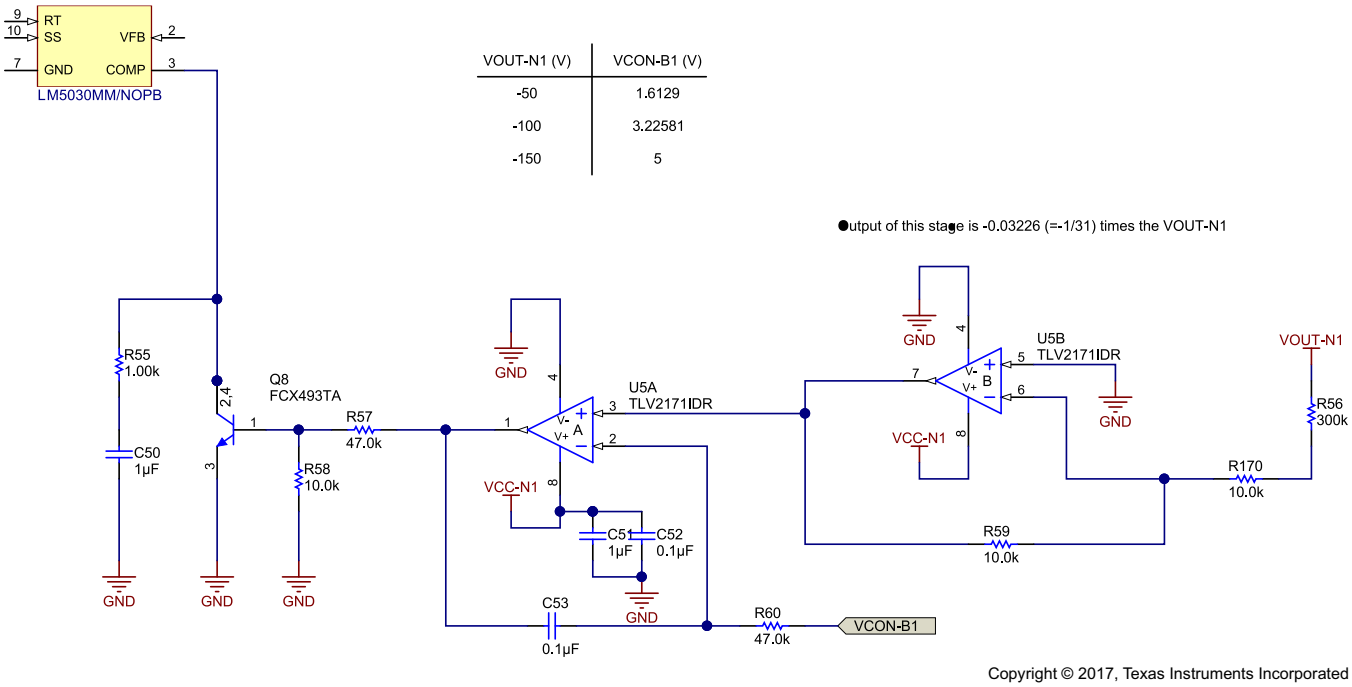


図 17. Feedback Circuit for Negative Rail for HV Section

図 18 shows the TINA simulation, and 図 19 shows the waveforms for VOUT-N1 = –50 to –150 V.

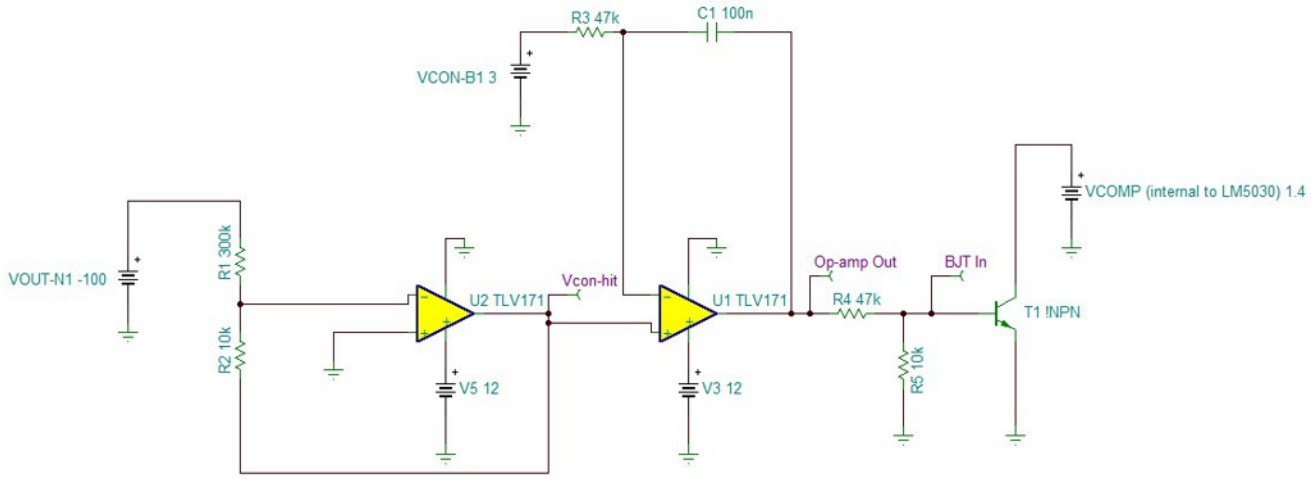


図 18. TINA Simulation for Feedback Circuit for Negative Rail for HV Section

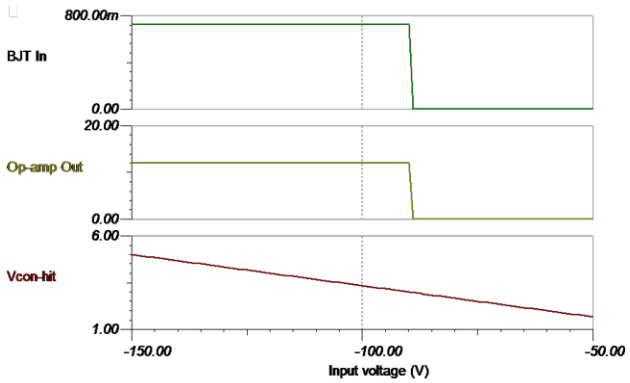


図 19. Simulation Waveform Showing Linearity (–HV Output)

2.3.2.9.3 Setting Output for Positive Rail for LV or MID Section

The feedback circuit is exactly same as for HV section except the gain. The V_{OUT} for LV- or MID-section varies from 2.5-V to 50-V DC. The gain is set to 0.09091 (= 1 k / 11 k). This gain gives the value of control voltage to be well within the maximum output from DAC, which is 5 V at VOUT-P2 = 50 V (refer to 図 20). Once the fraction of output VOUT-P2 is compared with control voltage VCON-A2, which is the output of U15 drives the transistor Q12. R118 (47 kΩ) and R120 (10 kΩ) are used for scaling the output of U15 to drive Q12. The collector of Q12 is used to pull down or pull up the voltage on COMP (pin 3) of LM5030 (U14) based on the result of comparison between output and control voltage. R117 (1 kΩ) and C88 (1 µF) form compensation network for COMP pin.

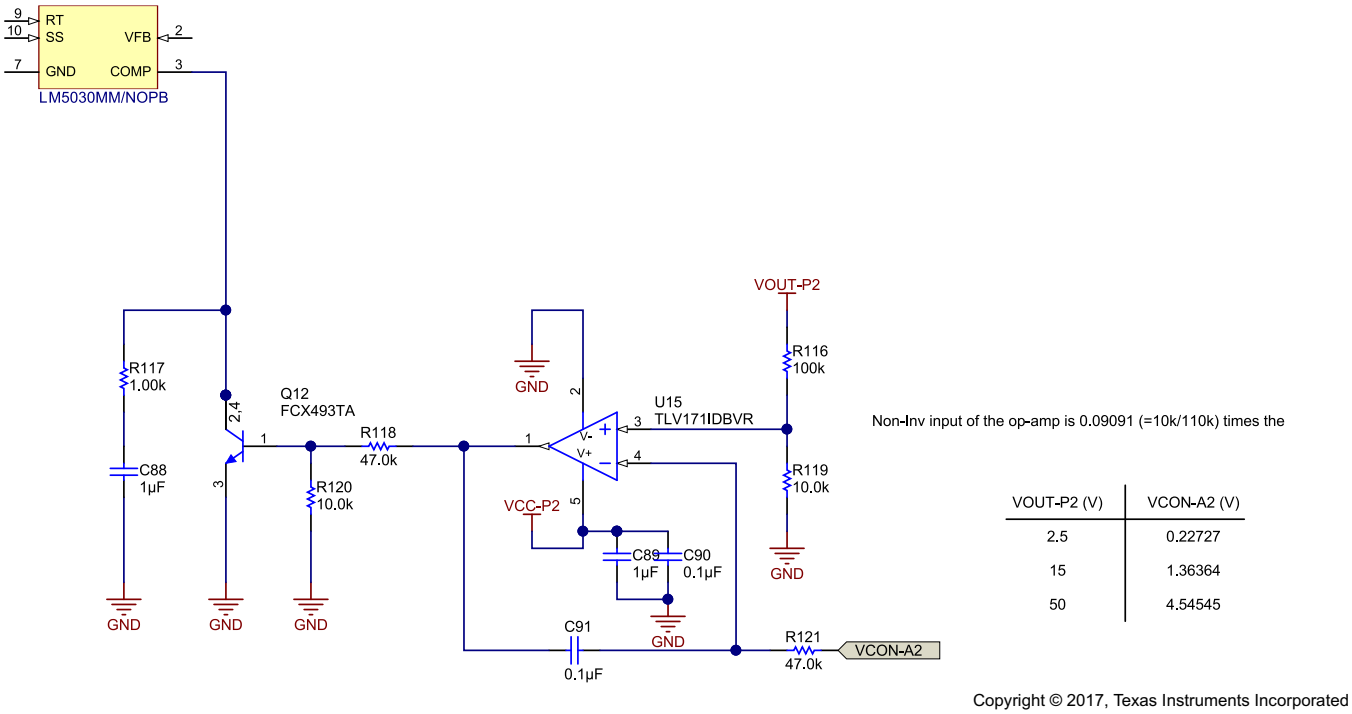


図 20. Feedback Circuit for Positive Rail for LV or MID Section

図 21 shows the TINA simulation, and 図 22 shows the waveforms for VOUT-P2 = 2.5 to 50 V.

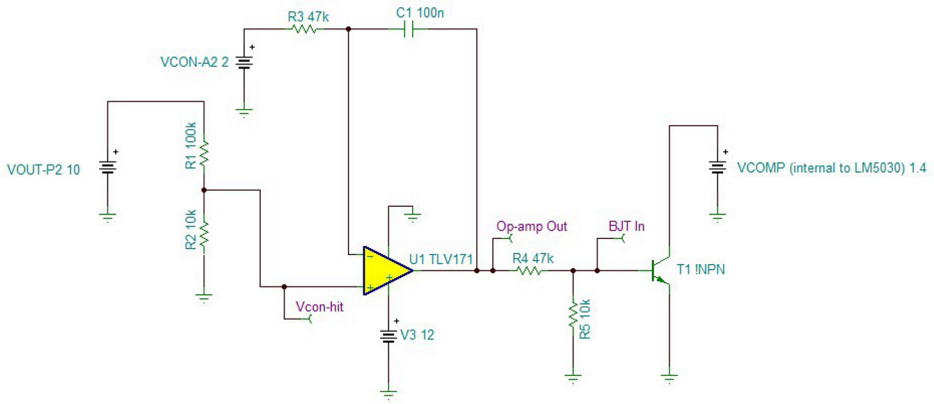


図 21. TINA Simulation for Feedback Circuit for Positive Rail for LV or MID Section

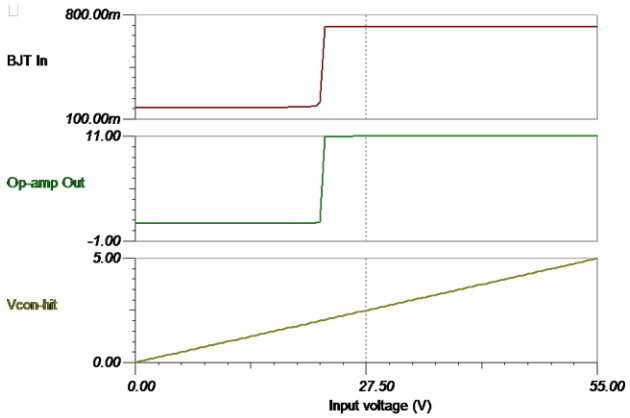


図 22. Simulation Waveform Showing Linearity (+LV or MID Output)

2.3.2.9.4 Setting Output for Negative Rail for LV or MID Section

The feedback circuit is exactly same as for HV section except the gain. The V_{OUT} for LV- or MID-section varies from –2.5-V to –50-V DC. The gain is set to –0.09091 (= 1 k / 11 k). This gain gives the value of control voltage to be well within the maximum output from DAC, which is 5 V at VOUT-N2 = –50 V (refer to 図 23). Before comparing the fraction of output VOUT-N2 with control voltage, the fraction is inverted using an inverting amplifier U18B. Once the fraction is inverted, it is compared with control voltage VCON-B2, which is the output of U18A drives the transistor Q16. R97 (47 kΩ) and R98 (10 kΩ) are used for scaling the output of U18A to drive Q16. The collector of Q16 is used to pull down or pull up the voltage on COMP (pin 3) of LM5030 (U17) based on the result of comparison between output and control voltage. R95 (1 kΩ) and C75 (1 µF) form compensation network for COMP pin.

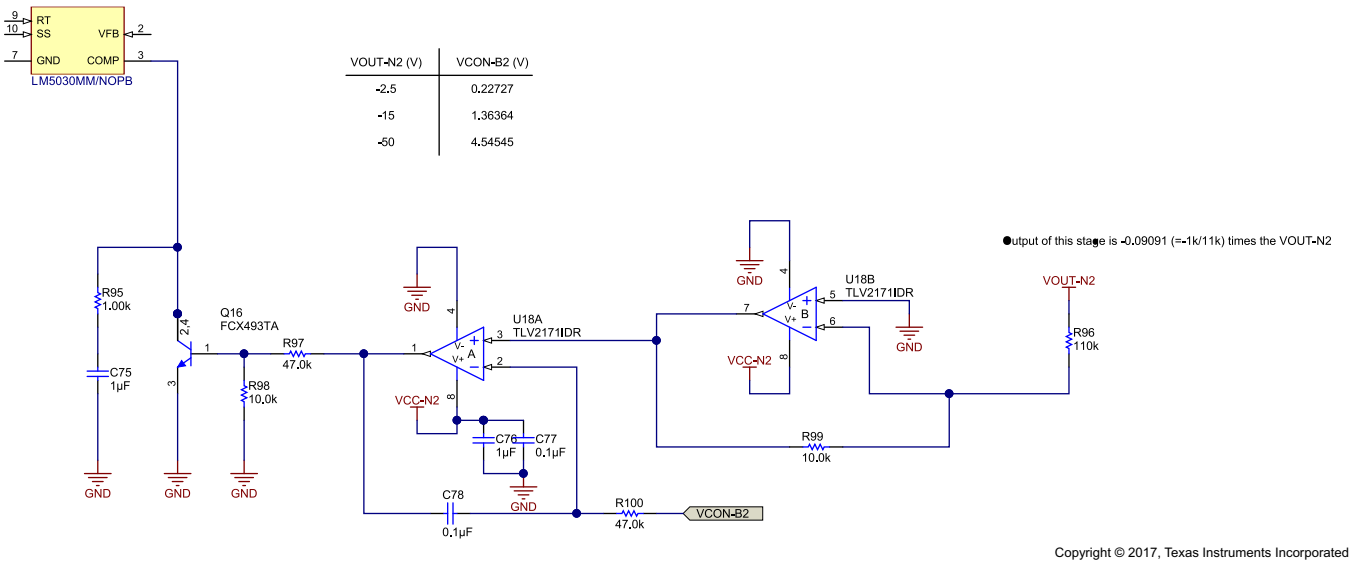


図 23. Feedback Circuit for Negative Rail for LV or MID Section

図 24 shows the TINA simulation, and 図 25 shows the waveforms for VOUT-P2 = 0 to –55 V.

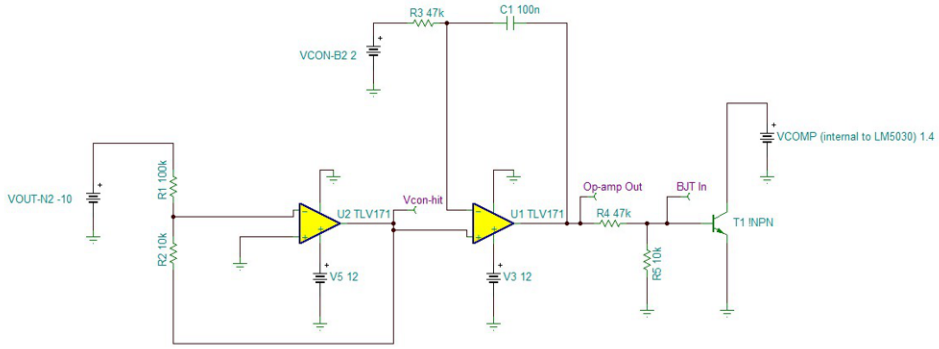


図 24. TINA Simulation for Feedback Circuit for Negative Rail for LV or MID Section

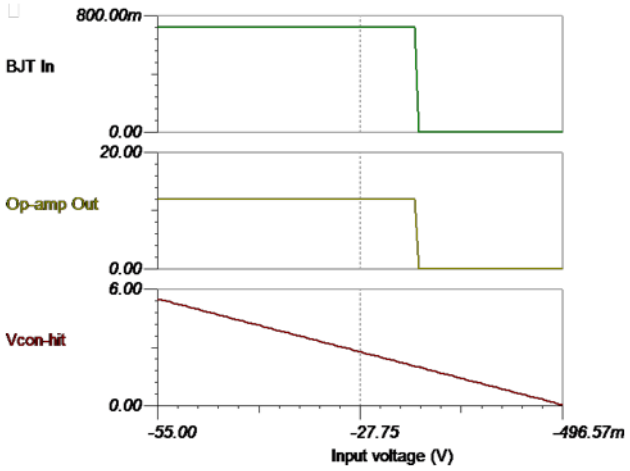


図 25. Simulation Waveform Showing Linearity (+LV or MID Output)

2.3.3 DAC60004 Circuit Design

There are two DACs used—one for programming the output voltage for *HV* power supply and other one for *LV or MID* power supply. This section explains the DAC60004 circuit and how it is similar for both the power supplies.

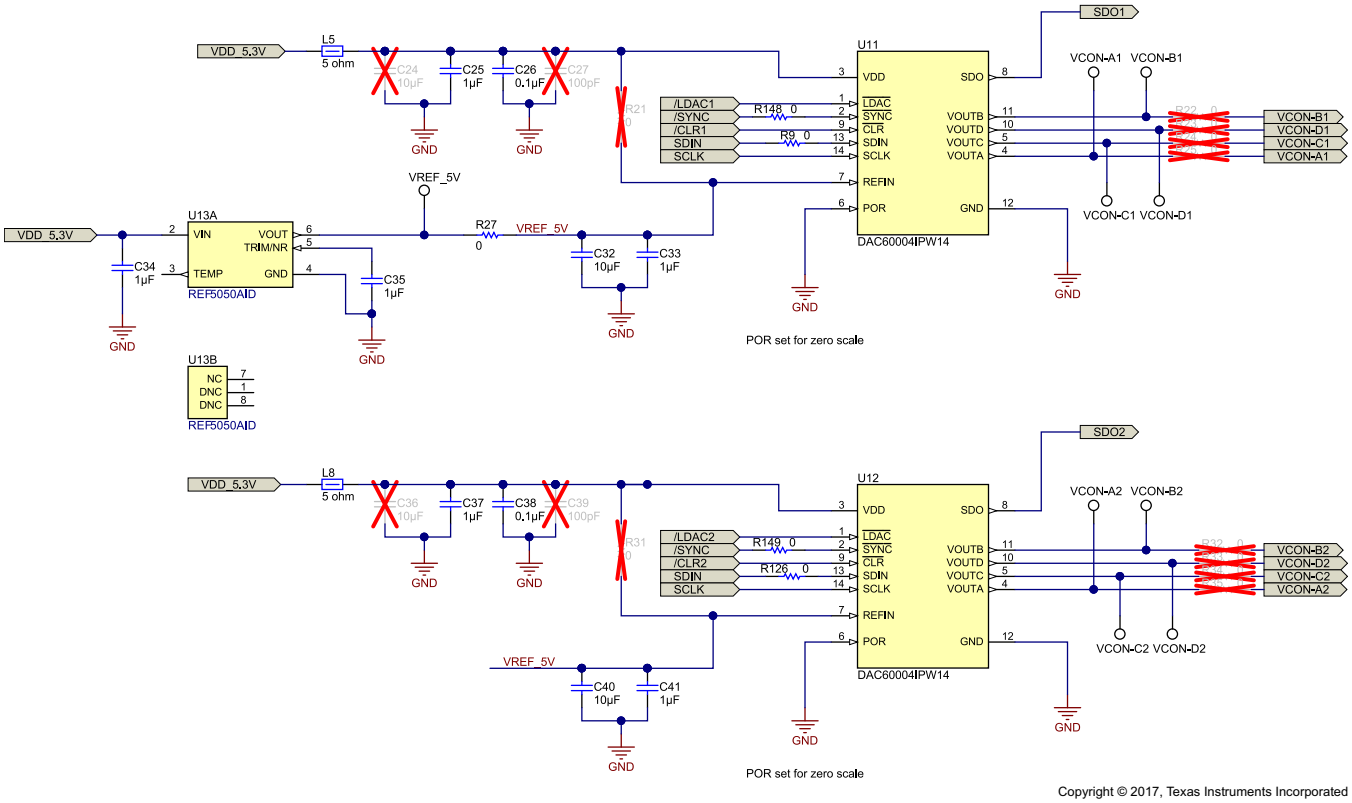


図 26. DAC60004 to set up Outputs for Power Supplies

2.3.3.1 Power Supply Requirements

The DAC60004 can operate within the specified supply voltage range of 2.7 to 5.5 V. The power applied to VDD should be well-regulated and have low-noise. A 1- to 10-µF capacitor and 0.1-µF bypass capacitor is recommended in order to further minimize noise from the power supply. Switching power supplies and DC-DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

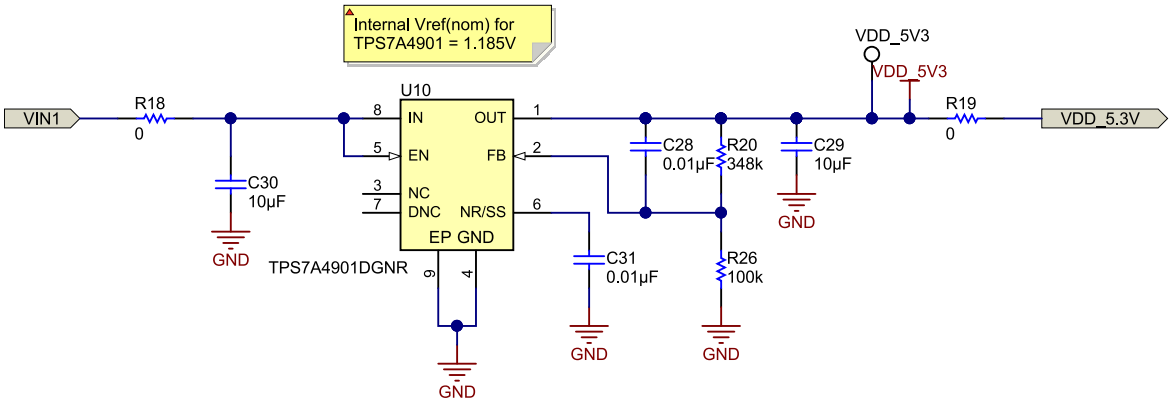


図 27. Power Supply for DAC60004

2.3.3.2 Reference Requirement for DAC60004

The reference input of DAC60004 is buffered internally using a dedicated reference buffer for each DAC channel, but it requires an external reference to operate. The REFIN pin drives the input of these buffers. The integrated reference buffers offer constant impedance of 30 kΩ (typical) at the REFIN pin. This simplifies the external reference drive circuit for the device. It is important to note that there should be some headroom between the VDD and VREF in order to achieve linearity at near-VDD codes. The reference input pin has the following input range:

- 2.2 V to (VDD – 0.2) for 2.7 V ≤ VDD ≤ 4.5 V
- 2.2 V to VDD for 4.5 V ≤ VDD ≤ 5.5 V

As shown in 図 26, REF5050 is used as reference for DAC60004. The REFIN pin of both the DACs, U11 and U12, is driven by 5-V reference voltage generated using REF5050.

2.3.3.2.1 REF5050 for REFIN of DAC60004

REF5050 (U13 in 図 27) is very low-noise, low-drift, high-precision, voltage reference. The input for U13 is connected to the 5.3-V output of U10. C34 (= 1 µF) is supply bypass capacitor for U13. C32 (= 10 µF) and C33 (= 1 µF) form output capacitance for U13. The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output. This pin is left open in this TI Design. Typical 0.1- to 10-Hz voltage noise for REF5050 is specified in *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* datasheet, but additional filtering can be used to improve output noise levels. C35 (= 1 µF) is used on pin TRIM-NR is for noise reduction purpose. Note that the capacitors at the REF5050 output should have ESR between 1 and 1.5 Ω or else an external resistor is recommended.

2.3.3.2.2 Using Supply as Reference for DAC60004

As highlighted in 2.3.3.2, if 4.5 V ≤ VDD ≤ 5.5 V, the value of reference voltage on REFIN pin can be 2.2 V to VDD. The VDD for U11 and U12 is 5.3 V. There is a bypass resistor for each of the DACs, R21 and R31, which can be used for this purpose. To isolate any noise coming from the VDD line, the designer can also use ferrite beads instead of resistors.

2.3.3.3 Power-on Reset

The DAC60004 contain a power-on-reset (POR) circuit that controls the output voltage during power up. The POR is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. At power up all DAC registers are filled with power-on reset code. For both the DACs used in this design, POR is set for zero scale by grounding the POR pin.

2.3.3.4 Programming DAC

The DAC60004 has a four-wire serial interface: SYNC, SCLK, SDIN, and SDO. The SPI shift register is 32 bits wide. The DAC accepts DAC code in straight binary format, and the DAC data is left aligned from MSB (D19) to LSB (D4: 16 bits, D6: 14 bits, D8: 12 bits). The channel address bits are shown in 表 4.

表 4. Channel Address Bits

CHANNEL ADDRESS BITS				DESCRIPTION
D23	D22	D21	D20	
0	0	0	0	Select channel A
0	0	0	1	Select channel B
0	0	1	0	Select channel C
0	0	1	1	Select channel D
1	1	1	1	Select all channels

2.3.3.4.1 CLR Pin Functionality and Software CLEAR Mode

The CLR pin is an asynchronous input pin to the DAC. When activated, this falling edge sensitive pin clears the DAC buffers and the DAC latches to zero, mid, full, or user-programmed code depending on the clear mode register. The default setting for clear operation is clear to 0 V.

2.3.3.4.2 LDAC Pin Functionality

The DAC60004 devices offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. Data updates can be performed either in synchronous or in asynchronous mode.

2.3.3.5 Potentiometers for Easy Evaluation

Potentiometers are provided for easy evaluation when the DAC is not use in the design. These are DNPs.

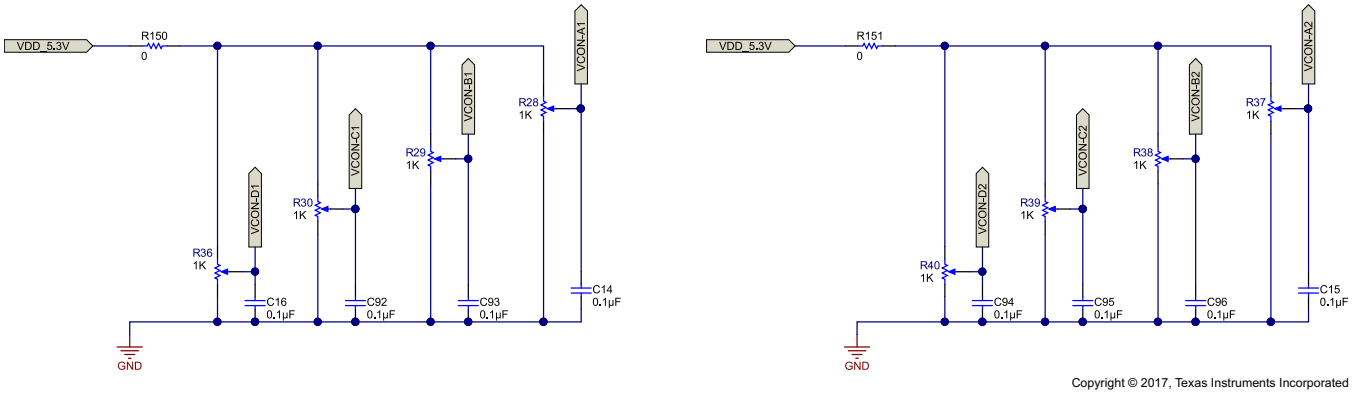


図 28. Potentiometers for Setting Feedback Outputs

2.3.4 Generation of 5-V (VCC) and 3.3-V (VDD) Rails Using LMZ34202

図 29 and 図 30 show schematic captures of the circuit using LMZ34202, which generates 5 V and 3.3 V, respectively.

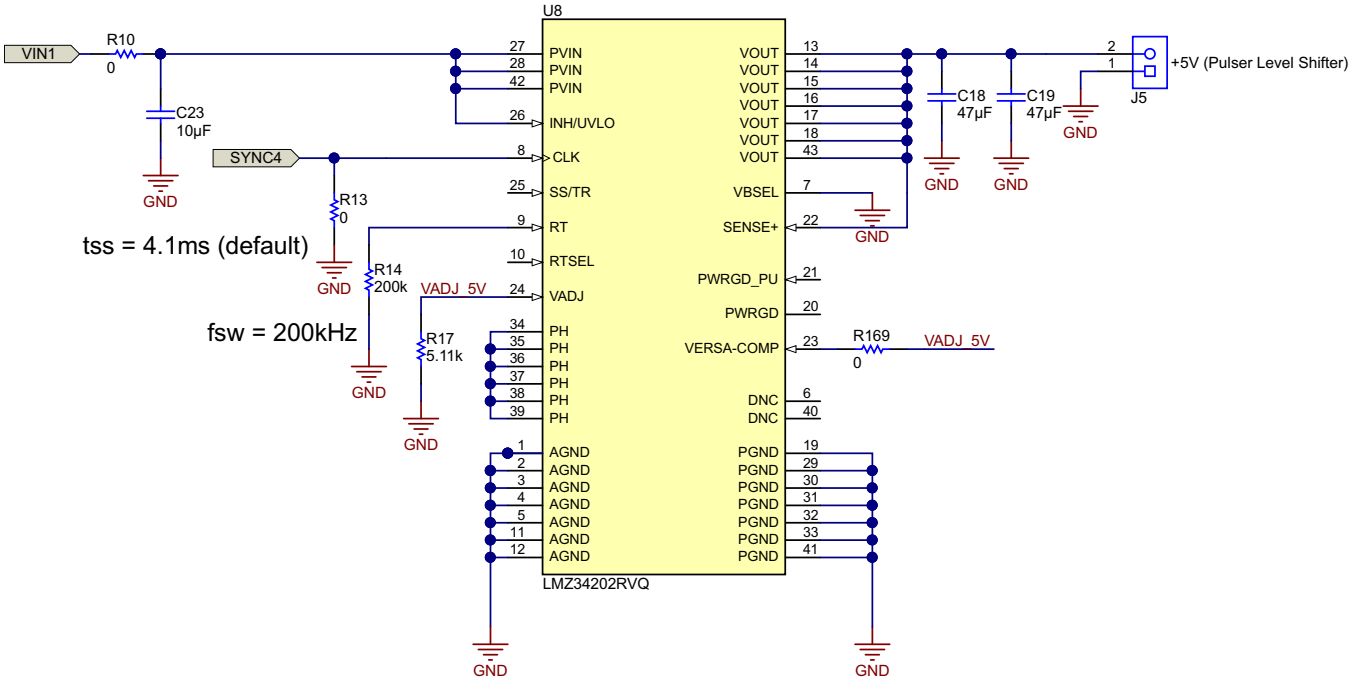


図 29. 5-V Generation Using LMZ34202

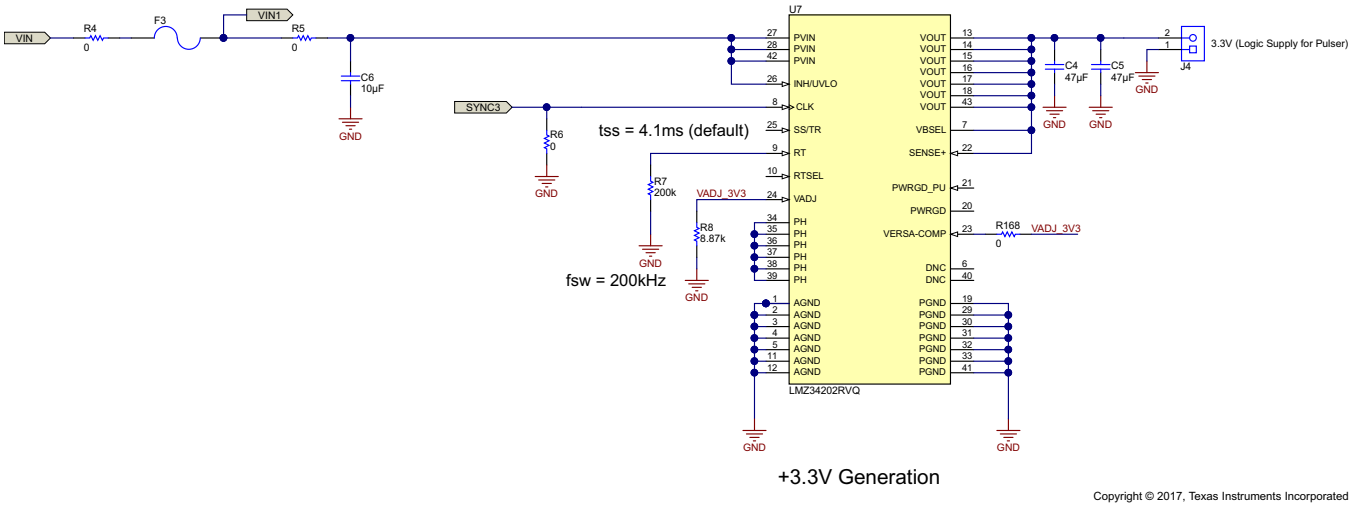


図 30. 3.3-V Generation Using LMZ34202

2.3.4.1 Input Capacitor Selection

The LMZ34202 requires a ceramic capacitor with a minimum effective input capacitance of 4.7 µF. Use only high quality ceramic type X5R or X7R capacitors with sufficient voltage rating. The voltage rating of input capacitors must be greater than the maximum input voltage. At worst case when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 1.0 Arms.

2.3.4.2 Switching Frequency (RT)

The switching frequency range of the LMZ34202 is 200 kHz to 1 MHz. Not all P_{VIN}, V_{OUT}, and I_{OUT} conditions can be set to all of the frequencies in this range. The switching frequency can easily be set one of three ways. First, leaving the RT pin (pin 9) and RTSEL pin (pin 10) floating (OPEN) allows operation at the default switching frequency of 500 kHz. Also, connecting the RTSEL pin to AGND while floating the RT pin sets the switching frequency to 1 MHz. The option is also available to set the switching frequency to any frequency in the range of 200 kHz to 1 MHz by connecting a resistor (RRT) between the RT pin and AGND while floating the RTSEL pin. The value of RRT can be calculated using 式 8. For f_{SW} = 200 kHz, R_{RT} = 200.4 kΩ.

$$R_{RT} = \frac{40200}{F_{SW}(kHz)} - 0.6\ (k\Omega) \tag{8}$$

2.3.4.3 Synchronization (CLK)

The LMZ34202 switching frequency can also be synchronized to an external clock from 200 kHz to 1 MHz. To implement the synchronization feature, connect a clock signal to the CLK pin with a duty cycle between 10% and 90%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the rising edge of CLK pin. Before the external clock is present the device operates in RT mode, and the switching frequency is set by R_{RT} resistor. Select R_{RT} to set the frequency close to the external synchronization frequency. When the external clock is present, the CLK mode overrides the RT mode. If the external clock is removed or fails at logic high or low, the LMZ34202 will switch at the frequency programmed by the R_{RT} resistor after a time-out period.

注: Not all P_{VIN}, V_{OUT}, and I_{OUT} conditions can be set to all of the frequencies from 200 kHz to 1 MHz (see 表 5).

表 5. Switching Frequency versus V_{OUT} (I_{OUT} > 1.75 A)

V_{OUT} RANGE (V)	SWITCHING FREQUENCY RANGE (kHz)					
	P_{VIN} = 12 V		P_{VIN} = 24 V		P_{VIN} = 36 V	
	MIN	MAX	MIN	MAX	MIN	MAX
2.5 to 3.5 V	200	450	200	500	200	400
> 3.5 to 4.5 V	200	500	200	600	200	550
> 4.5 to 5.5 V	200	500	200	650	200	700
> 5.5 to 6.5 V	300	500	250	700	250	800
> 6.5 to 7.5 V	300	400	300	750	300	800

2.3.4.4 Output Capacitor Selection

The minimum required and maximum output capacitance of the LMZ34202 is a function of the output voltage as shown in 表 6. Additionally, the output voltage will determine the VERSA-COMP configuration, which is also included in the same table. $C_{OUT(min)}$ must be comprised of ceramic type capacitors.

表 6. Required Output Capacitance for LMZ34202

V_{OUT} (V)	MINIMUM REQUIRED C_{OUT} (µF)	MAXIMUM C_{OUT} (µF)	VERSA-COMP CONNECTION
2.5	64	350	Leave open
3.3	64	350	Connect to VADJ
5.0	64	350	Connect to VADJ
6.0	64	200	Connect to VADJ
7.5	100	200	Connect to VADJ

2.3.4.5 VERSA-COMP Pin Configurations

The VERSA-COMP feature of the LMZ34202 allows a simple method to adjust the internal compensation network to provide the optimized phase and gain margin based on the output voltage. This easy-to-use feature requires no external components and is implemented by the simple configuration of two adjacent pins on the module. The VERSA-COMP feature must be configured in one of two ways: VERSA-COMP pin left OPEN or VERSA-COMP pin tied to VADJ. The output voltage determines the appropriate VERSA-COMP pin configuration.

2.3.4.6 Output On-Off Inhibit (INH/UVLO)

The INH/UVLO pin provides on and off control of the device. The INH input provides a precise 2.1-V rising threshold to allow direct logic drive or connection to a voltage divider from a higher voltage source such as P_{VIN}. The LMZ34202 device has an internal UVLO circuit which prevents the device from operating until the P_{VIN} voltage exceeds the UVLO threshold, [3.2 V (typ)]. The device will begin switching and the output voltage will begin to rise once P_{VIN} exceeds the threshold; however, P_{VIN} must be greater than (V_{OUT}/0.75) in order to for V_{OUT} to regulate at the set-point voltage.

2.3.4.7 Soft-Start (SS/TR)

Leaving the SS/TR pin open enables the internal slow start time interval of approximately 4.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Increasing the slow start time will reduce inrush current seen by the input source and reduce the current seen by the device when charging the output capacitors.

2.3.4.8 Other Pin Connections

The SENSE+ pin must be connected to VOUT at the load or at the device pins. Connecting the SENSE+ pin to VOUT at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV. The VBSEL pin allows the user to select the input source of the internal bias circuitry to improve efficiency. For output voltages ≥ 4.5V, connect this pin to VOUT. For output voltages

< 4.5 V, connect this pin to AGND. The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 95% and 105% of the set voltage, the PWRGD pin pulldown is released, and the pin floats. The recommended pullup resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 12 V or less. The LMZ34202 has an internal 100 kΩ between the PWRGD pin (pin 20) and the PWRGD_PU pin (pin 21).

2.3.5 Generation of –5-V VEE Rail Using LMZ34002

図 31 shows schematic capture of circuit using LMZ34002, which generates –5 V.

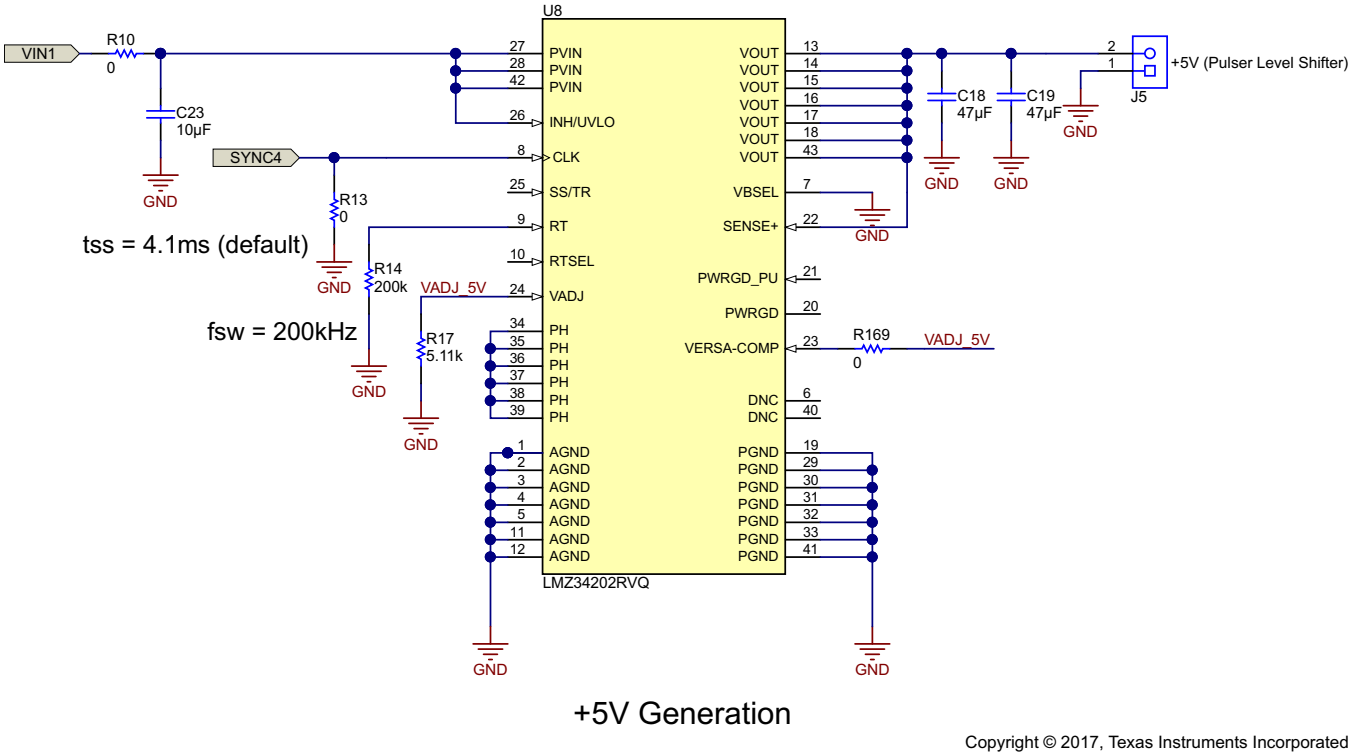


図 31. –5-V Generation Using LMZ34002

2.3.5.1 Input Capacitor

The LMZ34002 requires a minimum input capacitance of 4.7 µF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The ripple current rating of the capacitor must be at least 450 mA_{RMS}.

2.3.5.2 Output Capacitor

The required output capacitance of the LMZ34002 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 2 × 47 µF of ceramic type (or 4 × 22 µF). The voltage rating of output capacitors must be greater than the output voltage.

2.3.5.3 Adjusting Output Voltage

The LMZ34002 is designed to provide output voltages from –3 to –17 V. The output voltage is determined by the value of R_{SET}, which must be connected between the VADJ pin (pin 36) and GND. 式 9 gives R_{SET} = 52.65 kΩ for V_{out} = –5 V. The circuit uses standard resistor value of 52.3 kΩ.

$$R_{SET} = 10 \times \left(\frac{\text{Modulus of } V_{OUT}}{0.798} - 1 \right) (\text{k}\Omega) \tag{9}$$

2.3.5.4 UVLO and Output On-Off Inhibit (INH)

At turnon the V_{ON} UVLO threshold determines the input voltage level where the device begins power conversion. R_{UVLO1} (R146) and R_{UVLO2} (R147) set the turnon threshold as shown in 図 31. The following equations set the value of on voltage for the circuit.

$$R_{UVLO1} = \frac{0.5}{2.9 \times 10^{-3}} (\text{k}\Omega) \tag{10}$$

$$R_{ULVO2} = \frac{1.25}{\left(\frac{(V_{ON} - 1.25)}{R_{UVLO1}} \right) + 0.9 \times 10^{-3}} (\text{k}\Omega) \tag{11}$$

For V_{on} = 4.5 V, R146 = 174 kΩ, and R147 = 63.4 kΩ.

The INH pin provides electrical on-off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

2.3.5.5 Switching Frequency

The recommended switching frequency of the LMZ34002 is 800 kHz. To operate at the recommended switching frequency, connect the RT pin (pin 30) to A_VOUT (at pin 32). It is recommended to adjust the switching frequency in applications with both, higher input voltage (>18 V) and lower output voltage (<–8 V). For such applications, improved operating performance can be obtained by decreasing the operating frequency to 500 kHz by adding a resistor,. R_{RT} of 93.1 kΩ between the RT pin and A_VOUT as shown in 図 32.

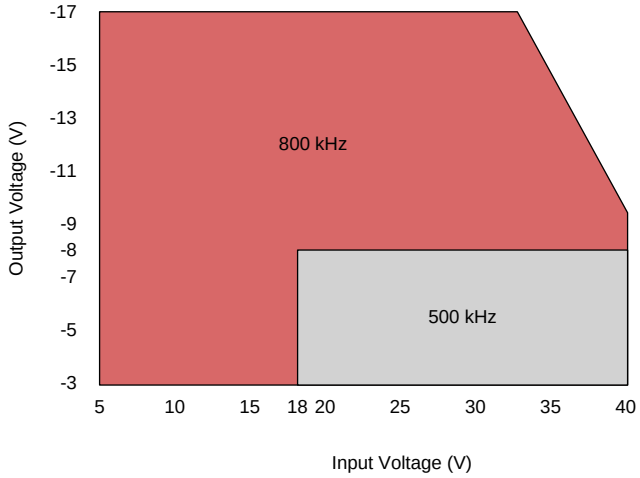


図 32. Recommended Switching Frequency for LMZ34002

2.3.5.6 Slow-Start Circuit (SS)

Connecting the STSEL pin (pin 29) to A_VOUT while leaving SS pin (pin 28) open enables the internal SS capacitor with a slow start interval of approximately 10 ms. Adding additional capacitance between the SS pin and A_VOUT increases the slow-start time.

2.3.5.7 Input to Output Coupling Capacitor

Adding an input-to-output coupling capacitor (CIO) across VIN to VOUT (as shown in 図 31) can help reduce output voltage ripple and improve transient response. A typical value for CIO is 2.2-μF ceramic with a voltage rating greater than the sum of V_{IN} + $|V_{OUT}|$.

2.3.5.8 Synchronization (CLK)

An internal phase locked loop (PLL) allows synchronization to external clock frequency. To implement the synchronization feature, connect a square wave clock signal to the RT-CLK pin with a duty cycle between 25% to 75%. The clock signal amplitude must transition lower than 0.5 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT-CLK pin. In applications requiring CLK mode, configure the device as shown in 図 33 (500 kHz).

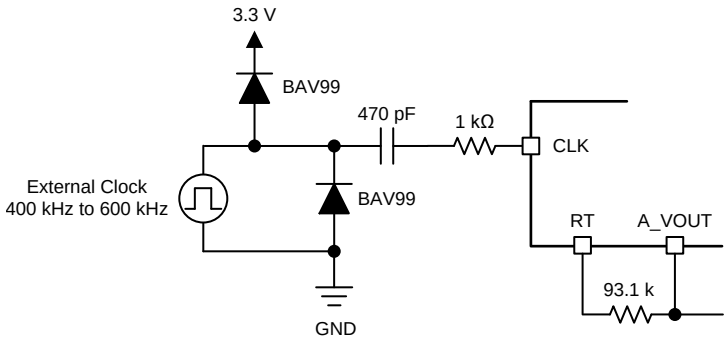


図 33. CLK Configuration (500-kHz Typ)

Before the external clock is present, the device works in RT mode where the switching frequency is set by the RRT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT-CLK high threshold (2.2 V), the device switches from RT mode to CLK mode, and the CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor.

2.3.6 Clock Synchronization

図 34 shows the schematic capture for CDCE937-based clock SYNC circuit. The circuit requires two different supply voltage values: 1.8 V for VDD and 3.3 V for V_{DDOUT}. The decoupling capacitors and filtering using ferrite beads is designed as per recommendations in *CDCEx937 Flexible Low Power LVCMOS Clock Generator With SSC Support For EMI Reduction*. There are seven outputs (Y1 to Y7), which are connected to SYNC signals as the mapping shown in 表 7. Note that mapping is done as per the routing convenience during the layout.

表 7. Mapping of SYNC Signals

CDCE937 PIN	SYNC SIGNAL	SYNC SIGNAL CONNECTION
Y1	SYNC1	U1 (positive supply for HV output)
Y2	SYNC2	U4 (negative supply for HV output)
Y3	SYNC5	U9 (–5-V generation)
Y4	SYNC6	U14 (positive supply for LV or MID output)
Y5	SYNC7	U17 (negative supply for LV or MID output)
Y6	SYNC4	U8 (5-V generation)
Y7	SYNC3	U7 (3.3-V generation)

As shown in 図 34, the input accepts an external crystal or LVCMOS clock signal. For TIDA-01352, the clock input signal (or SYNC signal) is always external hence the crystal (Y1) and load capacitors (C107 and C108) are not mounted.

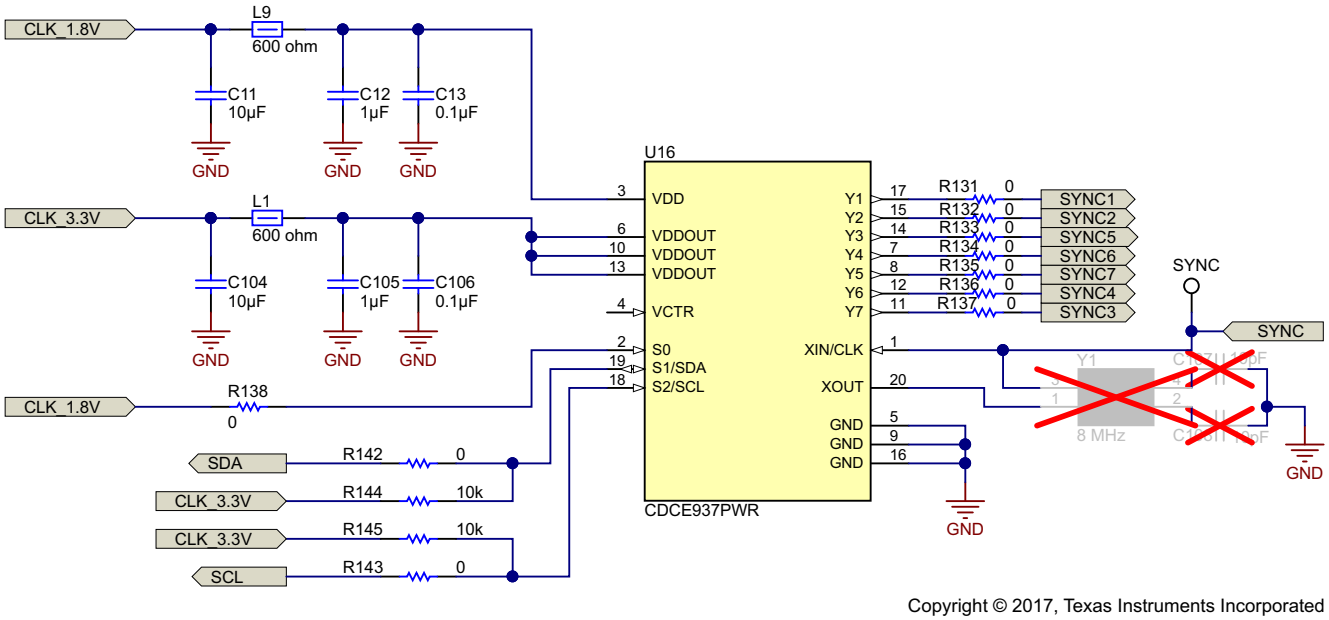


図 34. Schematic Capture for CDCE937—Clock SYNC Buffer

2.3.6.1 Power Supply Recommendations

CDCE937 has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components including the outputs. If there is a 3.3-V V_{DDOUT} available before the 1.8-V, the outputs remain disabled until the 1.8-V supply has reached a certain level. If VCXO pulling functionality is not required, VCTR pin should be left floating. All other unused inputs should be set to GND. Unused outputs should be left floating.

2.3.6.2 Frequency Planning

The required range for the SYNC signal is from 100 kHz to 1 MHz. To support this range, the PLL inside CDCE937 should be bypassed. This condition is highlighted in 表 8 (taken from the CDCE937 datasheet).

表 8. Input Frequency Range for CDCE937(1)

DESCRIPTION			MIN	NOM	MAX	UNIT
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0	—	160	MHz
		PLL mode	8	—	160	
t_r or t_f	Rise and fall time CLK signal (20% to 80%)		—	—	3	ns
$duty_{CLK}$	Duty cycle CLK at $V_{DD}/2$		40%	—	60%	—

(1) Over operating free-air temperature range (unless otherwise noted)

2.3.6.3 Programming Clock

CDCE937 supports non-volatile EEPROM programming for ease-customized application, which is preset to a factory default configuration. The internal EEPROM of CDCE937 is preconfigured so that the input frequency is passed through to the output as a default, which allows the device to operate in default mode without the extra production step of program it. The default setting appears after power is supplied or after power-down or power-up sequence until it is reprogrammed by the designer to a different application configuration. It can be reprogrammed to a different application configuration before PCB assembly or reprogrammed by in-system programming. All device settings are programmable through SDA or SCL bus, a two-wire serial interface.

2.3.6.4 VDD Supply for CDCE937

The 1.8-V VDD supply for CDCE937 is generated using TPS7A4901. It accepts 24-V input and sets output at 1.8 V using feedback resistors R129 and R130 as shown in 図 35.

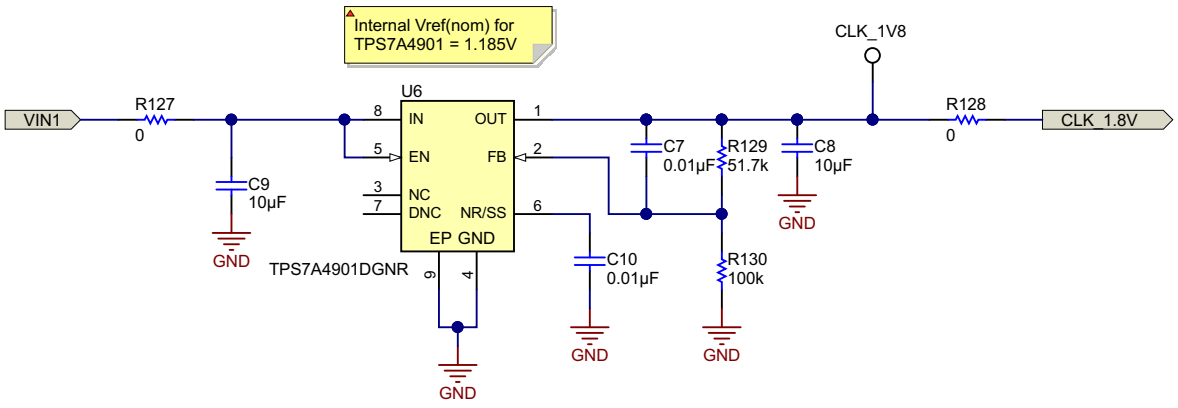


図 35. 1.8-V VDD Generation for CDCE937

2.3.6.5 V_{DDOUT} Supply for CDCE937

The 3.3-V V_{DDOUT} supply for CDCE937 is generated using TPS7A4901. The device accepts 24-V input and sets output at 3.3 V using feedback resistors R140 and R141 as shown in 図 36.

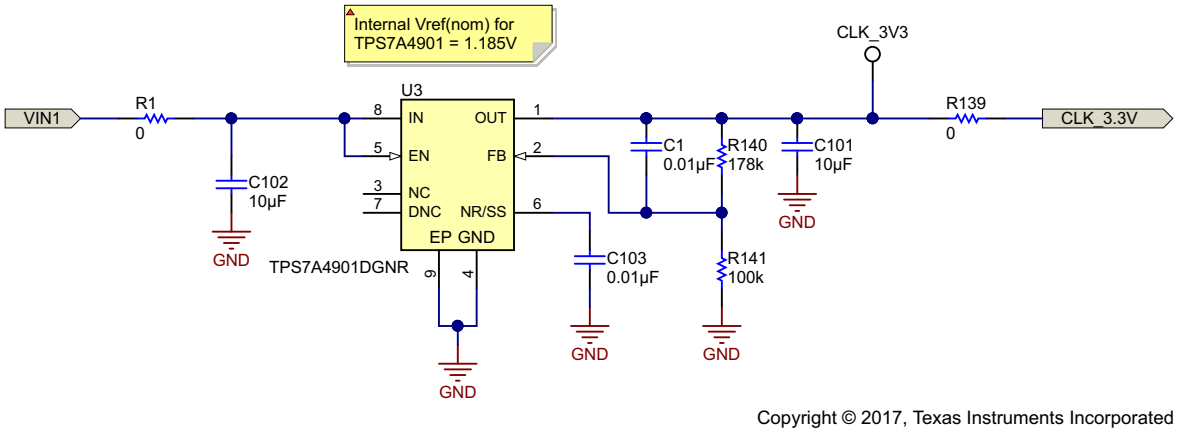


図 36. 3.3-V V_{DDOUT} Generation for CDCE937

2.3.7 Programming Connector

図 37 shows the programming connector for the DACs. The connector is a generic 20-pin connector, which can be used to connect to any controller or processor based on the requirement.

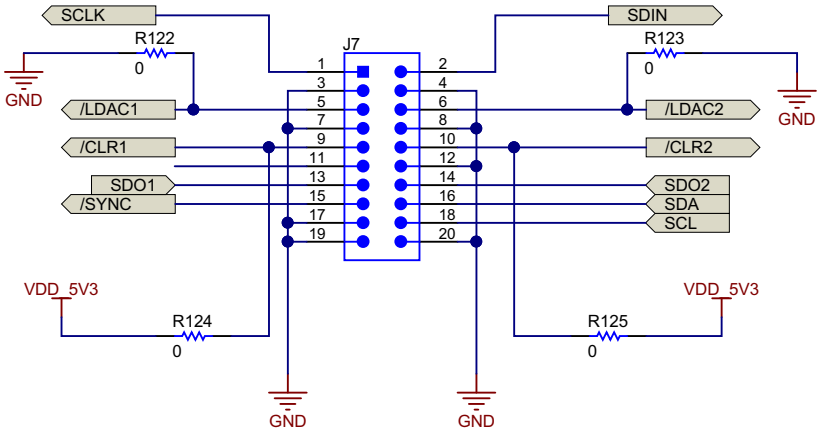


図 37. Programming Connector

2.3.7.1 Connectors, Fuses, and Test Points on Board

表 9 shows the connectors and test-points used on TIDA-01352. 表 9 also shows the ratings of each of the connectors.

表 9. Ratings for Onboard Connectors

RAIL	CONNECTOR OR TEST POINT	RATING
VIN	J1	300 V, 30 A, 6.35-mm pitch, two-position
VMAIN-Positive	J2	300 V, 13.5 A, 3.81-mm pitch, two-position
VMAIN-Negative	J3	300 V, 13.5 A, 3.81-mm pitch, two-position
3.3 V (logic supply for pulser)	J4	150 V, 10 A, 2.54-mm pitch, two-position
5 V (pulser level shifter)	J5	150 V, 10 A, 2.54-mm pitch, two-position
–5 V (pulser level shifter)	J6	150 V, 10 A, 2.54-mm pitch, two-position
VMID-Positive	J8	300 V, 13.5 A,3.81-mm pitch, two-position

表 9. Ratings for Onboard Connectors (continued)

RAIL	CONNECTOR OR TEST POINT	RATING
VMID-Negative	J9	300 V, 13.5 A, 3.81-mm pitch, two-position
Programming connector	J7	N/A
External clock SYNC signal	SYNC	N/A
Shutdown for push-pull circuits (HV section)	/SD1	N/A
Shutdown for push-pull circuits (LV or MID section)	/SD2	N/A
5.3-V rail	VDD_5V3	N/A
5-V reference for DAC	VREF_5V	N/A
Control voltages from DAC1	VCON-A1, VCON-B1, VCON-C1, VCON-D1	N/A
Control voltages from DAC2	VCON-A2, VCON-B2, VCON-C2, VCON-D2	N/A
VDD for CDCE937	CLK_1V8	N/A
V_{DDOUT} for CDCE937	CLK_3V3	N/A

2.4 Highlighted Products

2.4.1 LM5030

The LM5030 is a high-voltage PWM controller containing all of the features needed to implement push-pull topology in current-mode control. The device provides two alternating gate driver outputs. The LM5030 includes a high-voltage start-up regulator that operates over a wide input range of 14 to 100 V. The device has total propagation delays less than 100 ns and a 1-MHz, capable, single-resistor, adjustable oscillator.

2.4.2 CSD19506KCS

The CSD19506KCS is a 80-V N-Channel NexFET™ Power MOSFET available in a TO-220 package. The device has an $R_{DS(ON)}$ of 2 mΩ, which helps in minimizing losses in power conversion applications.

2.4.3 TLVx171

The 36-V TLVx171 family provides a low-power option for cost-conscious industrial systems requiring an electromagnetic interference (EMI)-hardened, low-noise, single-supply operational amplifier (op amp) that operates on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The single-channel TLV171, dual-channel TLV2171, and quad-channel TLV4171 provide low offset, drift, quiescent current balanced with high bandwidth for the power. This series of op amps are rail-to-rail input as well as output.

2.4.4 DAC60004

The DAC60004 is highly-accurate, low-power, voltage-output, quad-channel, 12-bit DAC. The device is ensured monotonic by design and offer excellent linearity of less than 1 LSB (maximum). The reference input of the DAC is buffered internally using a dedicated reference buffer. The DAC60004 incorporates a power-on-reset circuit that ensures the DAC output powers up at zero scale or mid scale depending on status of the POR pin and remains in this state until a valid code is written to the device. The device uses a versatile four- or three-wire serial interface that operates at clock rates up to 50 MHz.

2.4.5 LMZ34202

The LM34202 power module is an easy-to-use integrated power supply that combines a 2-A, DC-DC converter with a shielded inductor and passives into a low-profile, QFN package. This total power solution allows as few as three external components while maintaining an ability to adjust key parameters to meet specific design requirements.

2.4.6 LMZ34002

The LMZ34002 power module is an easy-to-use, negative output voltage power module that combines a 15-W, DC-DC converter with a shielded inductor and passives into a low-profile QFN package. This total power solution allows as few as five external components and eliminates the loop compensation and magnetics part selection process.

2.4.7 TPS7A4901

The TPS7A4901 is a positive, high-voltage (36 V), ultra-low-noise (15.4 μV_{RMS}, 72-dB PSRR) linear regulator that can source a 150-mA load. This regulator is ideal for high-accuracy, high-precision applications where clean voltage rails are critical to maximize system performance.

2.4.8 REF5050

The REF5050 is a low-noise, low-drift, very high-precision voltage reference. The device has excellent temperature drift (3 ppm/°C) and high accuracy (0.05%).

2.4.9 CDCE937

The CDCE937 is modular PLL-based, low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. The device can generate up to seven output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to three independent configurable PLLs. The CDCE937 has separate output supply pins, V_{DDOUT}, which is 1.8 V.

2.4.10 CSD17381F4

The CSD17381F4 is a 30-V N-Channel FemtoFET™ MOSFET available in a 1-mm × 0.6-mm package. The device has an $R_{DS(ON)}$ of 110 mΩ, which helps in minimizing losses in power conversion applications.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 TIDA-01352 Board Picture

図 38 and 図 39 show top and bottom views of TIDA-01352 PCB, respectively. The important sections are highlighted with red boxes and captions.

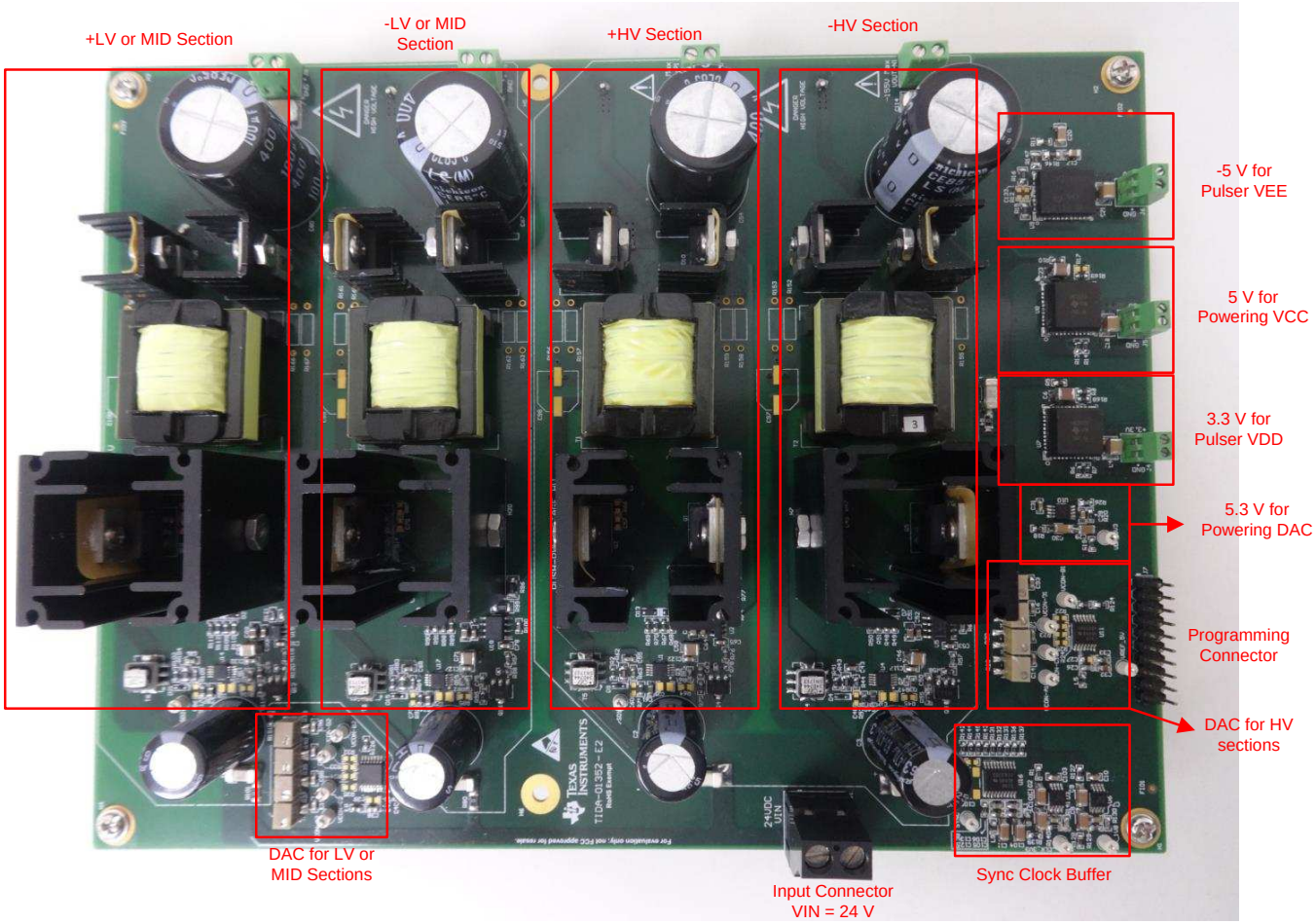


図 38. TIDA-01352 PCB—Top View

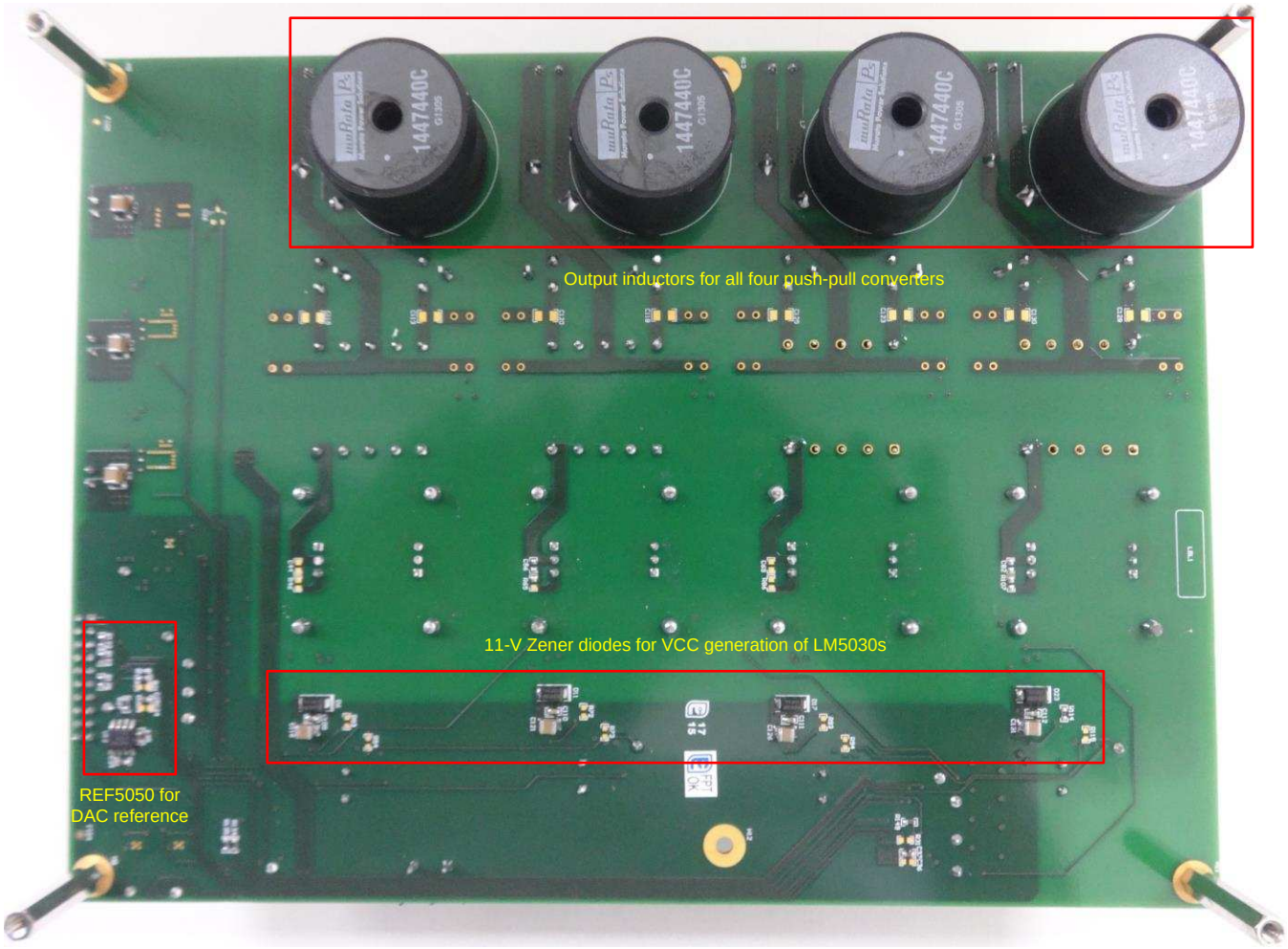


図 39. TIDA-01352 PCB—Bottom View

3.1.2 Software

This section shows the flow charts used for programming the DAC60004 and CDCE937 devices on TIDA-01352.

注: The connector J7 is generic connector and used for the programming. MSP430G2553 LaunchPad™ is used for programming the DAC60004 and CDCE937 devices on TIDA-01352. The designer can use any controller or processor or FPGA to program these devices.

3.1.2.1 DAC Programming

図 40 shows the flow chart for programming the DACs.

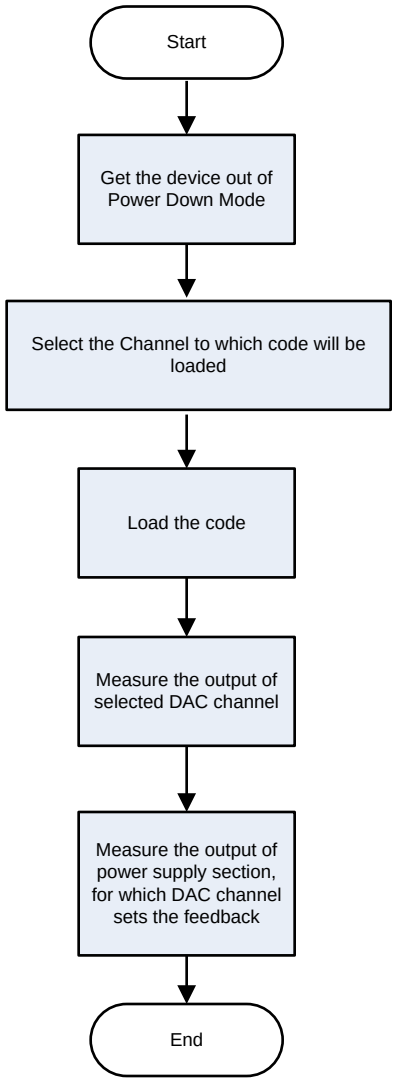


図 40. Flow Chart for Programming CDCE937

3.1.2.2 Clock Buffer Programming

図 41 shows the flow chart for programming the clock buffer CDCE937.

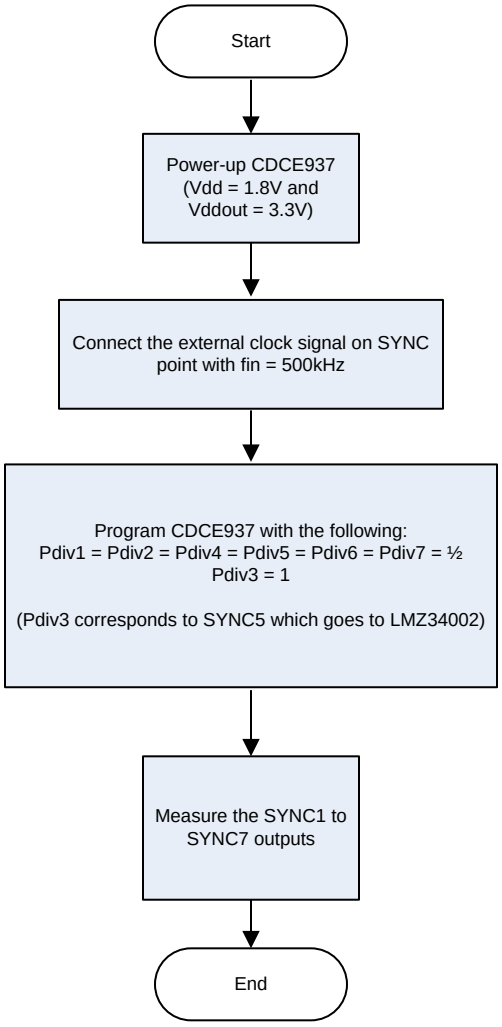


図 41. Flow Chart for Programming CDCE937

Based on this flow chart, 図 42 shows example programming for synchronization of all the other power devices to input clock frequency of 500 kHz.

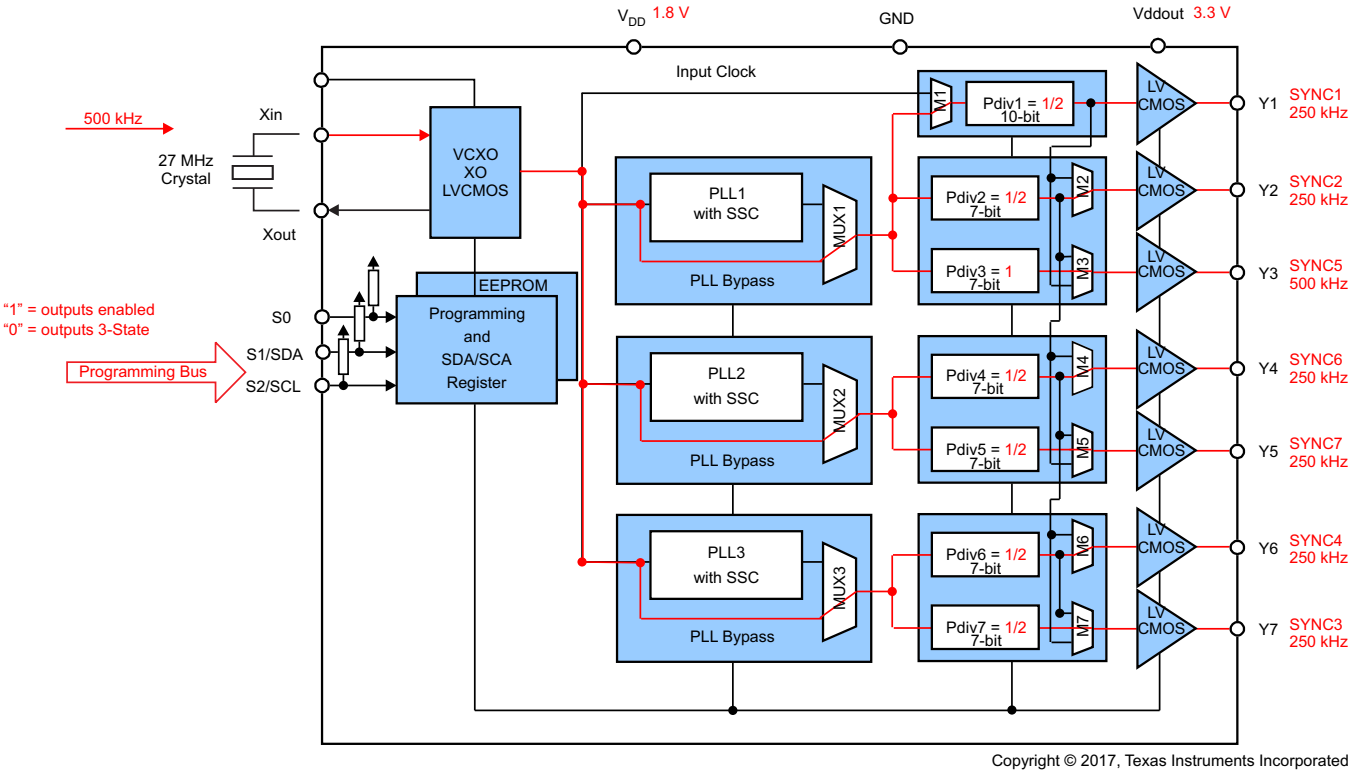


図 42. Clock Programming for Synchronization of All Devices to f_{IN} = 500 kHz

3.2 Testing and Results

3.2.1 Test Setup

The ±HV sections and ±LV or MID-sections are tested for different imaging modes. The load profile changes with the imaging mode (see 図 43 and 表 10).

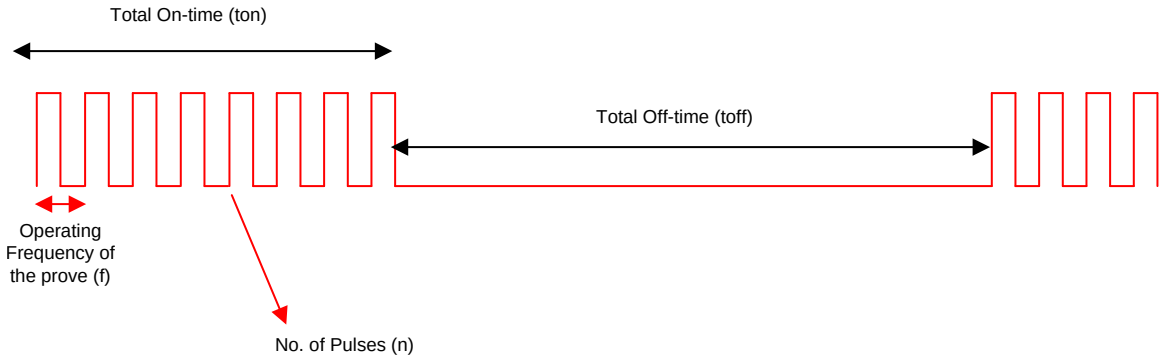


図 43. Load Profile for Testing TIDA-01352 in Different Imaging Modes

表 10. Conditions for Different Imaging Modes

MODE	t_{ON}	t_{OFF}	t_{TOTAL}
B-mode	20 µs	180 µs	200 µs
Elastography mode	0.75 ms	14.25 ms	15 ms

注: The design can support 350 W of peak output power by changing the current sense resistors for ±HV lines.

WARNING

High voltages that may cause injury exist on the TIDA-01352. Ensure all safety procedures are followed when working on the TIDA-01352 board. Never leave a powered board unattended.

3.2.2 Test Results

3.2.2.1 Functional Tests for +HV Section

図 44 and 図 45 show the efficiency graph and load regulation plot for +HV section in B-mode.

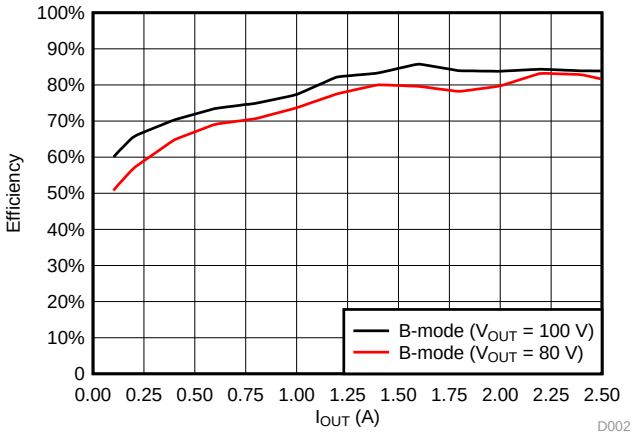


図 44. B-Mode Efficiency (+HV Output)

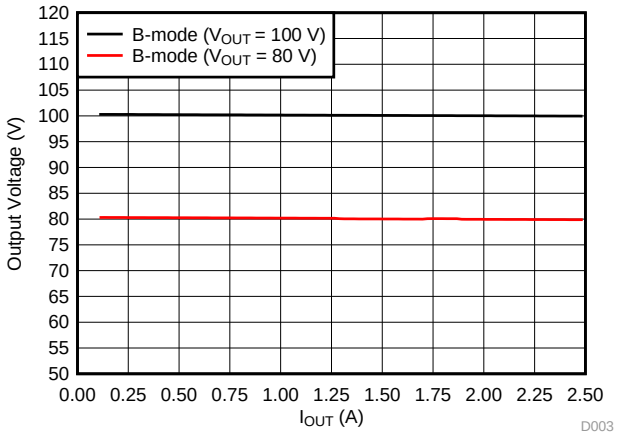


図 45. B-Mode Load Regulation (+HV Output)

図 46 and 図 47 show the efficiency graph and load regulation plot for +HV section in Elastography-mode.

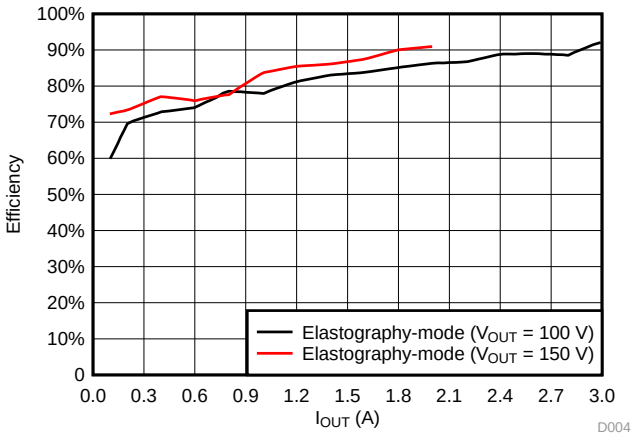


図 46. Elastography Mode Efficiency (+HV Output)

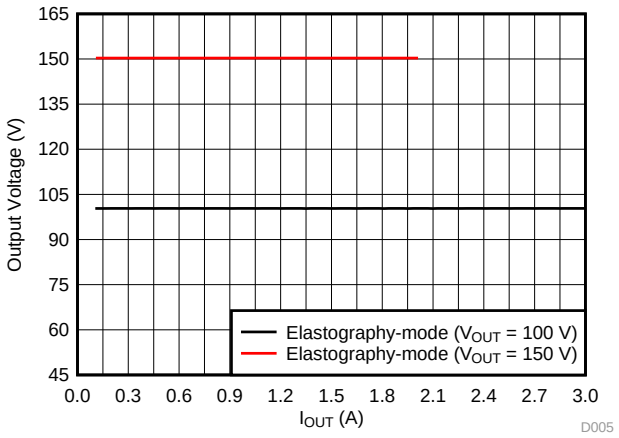


図 47. Elastography Mode Load Regulation (+HV Output)

図 48 and 図 49 show the efficiency graph and load regulation plot for +HV section in full load condition (V_{OUT} = 100 V, I_{OUT} = 1 A at V_{IN} = 24 V).

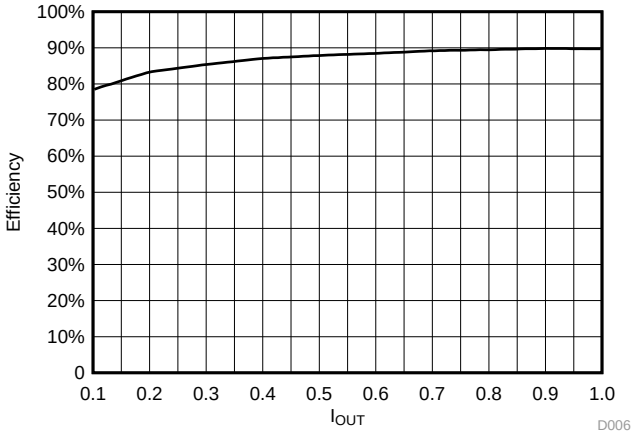


図 48. Full Load Efficiency at V_{IN} = 24 V, V_{OUT} = 100 V, I_{OUT} = 1 A

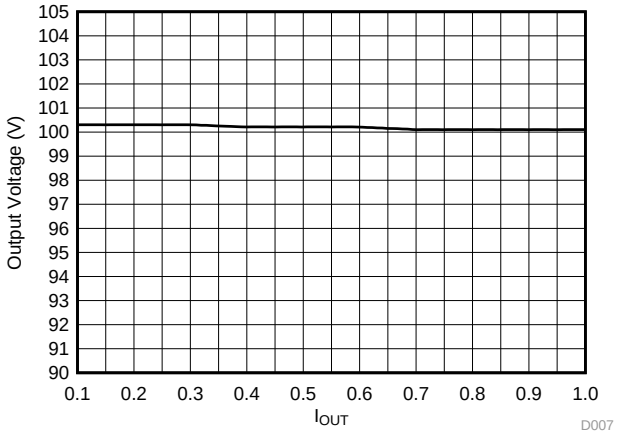


図 49. Load Regulation for V_{IN} = 24 V, V_{OUT} = 100 V

図 50 shows the start-up waveform at the power-up. The waveform shows a soft-start time of around 2 seconds as calculated in 2.3.2.4.

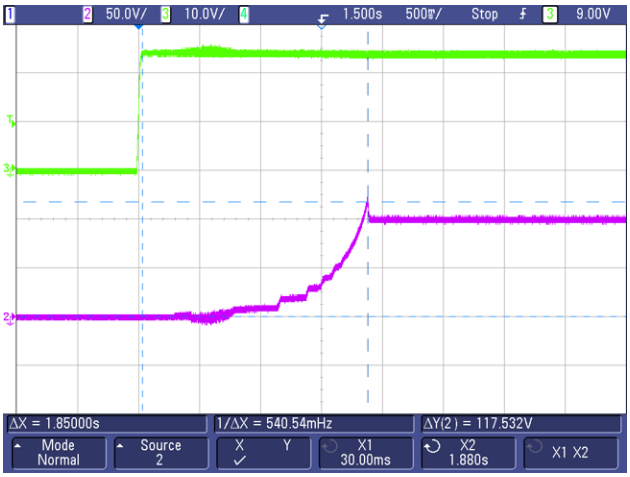


図 50. Start-up Waveform for +HV Output

図 51 shows the stress on the MOSFETs, such as drain-to-source voltages. For both the MOSFETs, stress is less than 80 V (the absolute maximum rating of the MOSFETs). It also shows the current sense waveform before the waveform is filtered and given to the CS pin of LM5030 (U1).

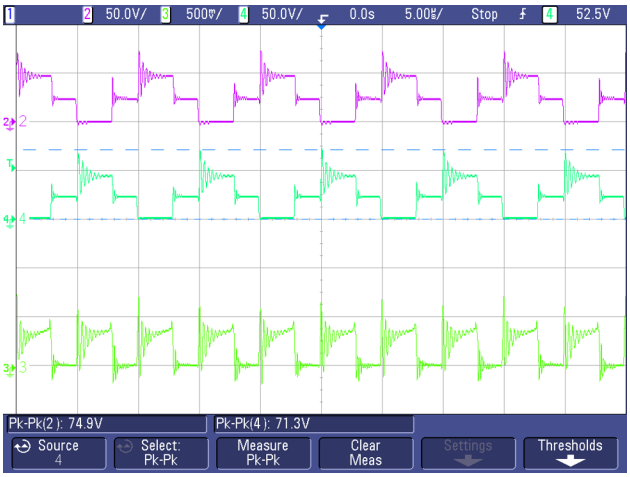


図 51. MOSFET Stress VDS for +HV Output

図 52 shows the output ripple voltage for +HV output. The measured value of peak-to-peak ripple is 110 mV.

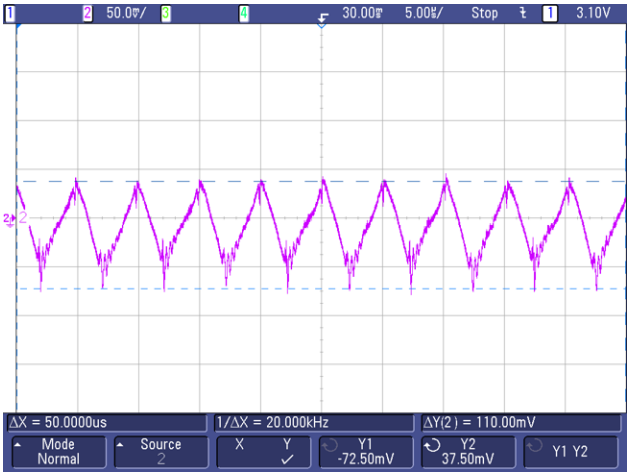


図 52. Output Voltage Ripple for +HV Output

3.2.2.2 Functional Tests for –HV Section

図 53 and 図 54 show the efficiency graph and load regulation plot for the –HV section in B-mode.

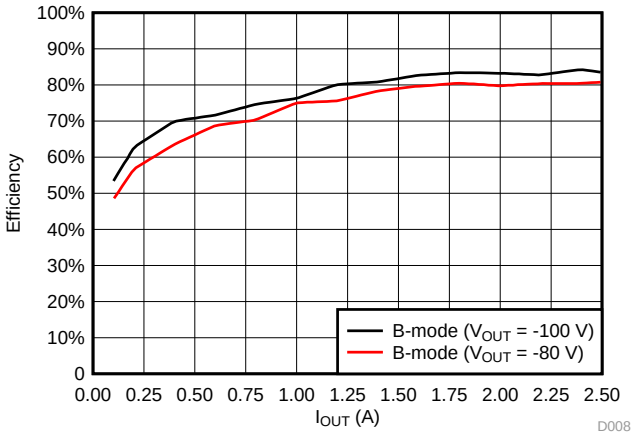


図 53. B-Mode Efficiency (–HV Output)

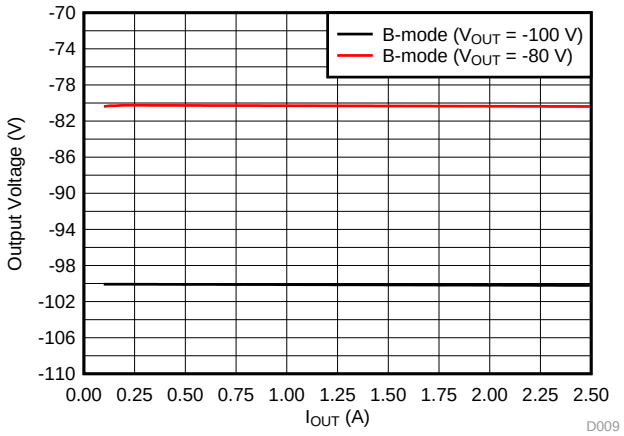


図 54. B-Mode Load Regulation (–HV Output)

図 55 and 図 56 show the efficiency graph and load regulation plot for the –HV section in Elastography-mode

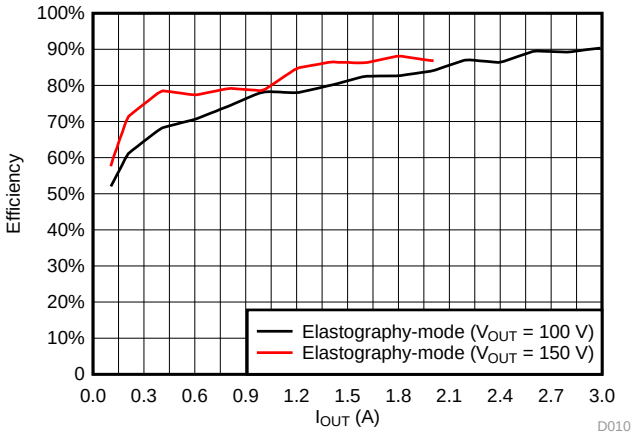


図 55. Elastography Mode Efficiency (–HV Output)

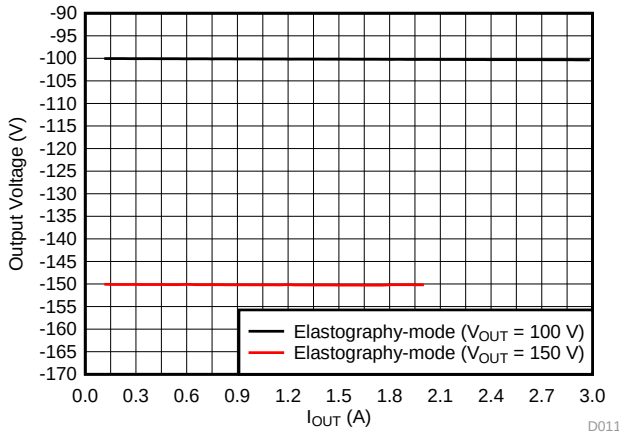


図 56. Elastography Mode Load Regulation (–HV Output)

図 57 and 図 58 show the efficiency graph and load regulation plot for the –HV section in full load condition (V_{OUT} = –100 V, I_{OUT} = –1 A at V_{IN} = 24 V).

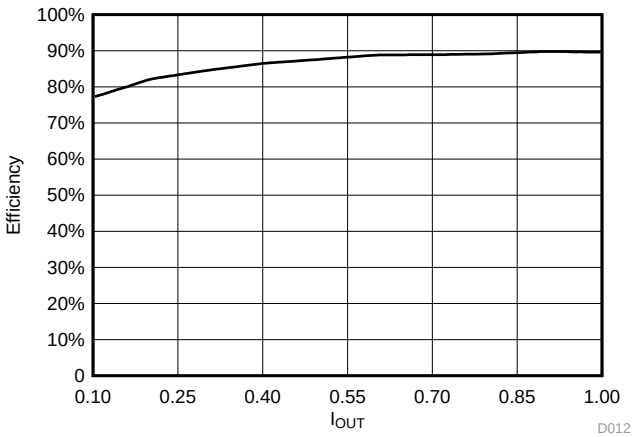


図 57. Full Load Efficiency at V_{IN} = 24 V, V_{OUT} = –100 V, I_{OUT} = –1 A

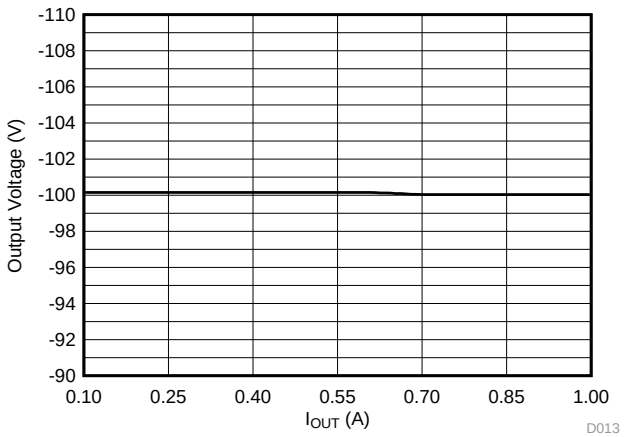


図 58. Load Regulation for V_{IN} = 24 V, V_{OUT} = –100 V

図 59 shows the start-up waveform at the power-up. The waveform shows a soft-start time of around 2 seconds as calculated in 2.3.2.4.

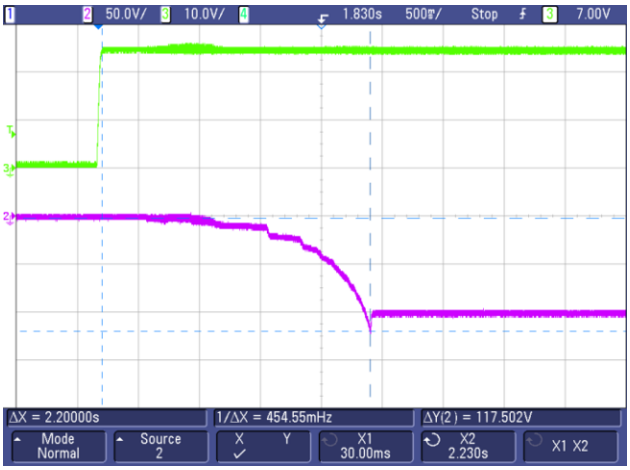


図 59. Start-up Waveform for –HV Output

図 60 shows the stress on the MOSFETs, such as drain-to-source voltages. For both the MOSFETs, stress is less than 80 V (the absolute maximum rating of the MOSFETs). It also shows the current sense waveform before the waveform is filtered and given to the CS pin of LM5030 (U4).

図 60. MOSFET Stress VDS for –HV Output

図 61 shows the output ripple voltage for the –HV output. The measured value of peak-to-peak ripple is 75 mV.

図 61. Output Voltage Ripple for –HV Output

3.2.2.3 *Functional Tests for +LV or Mid Section*

図 62 and 図 63 show the efficiency graph and load regulation plot for +LV or MID-section in CW-mode.

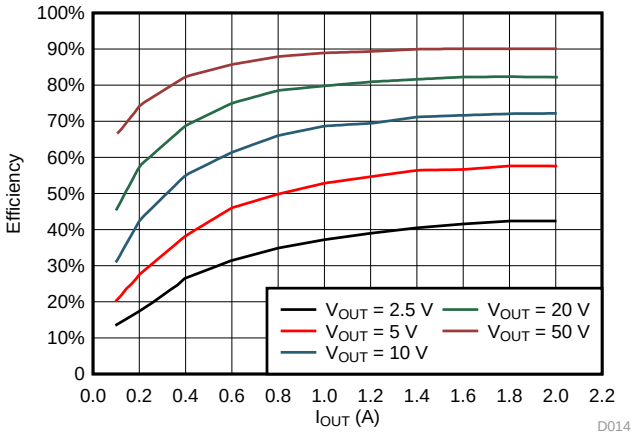


図 62. Efficiency for +LV or MID Section for CW Mode

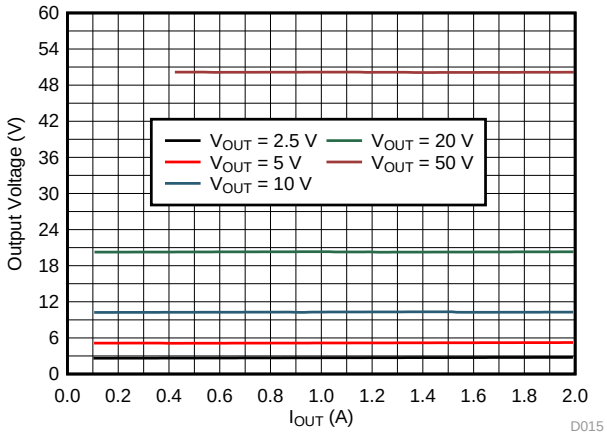


図 63. Load Regulation for +LV or MID Section for CW Mode

図 64 shows the output ripple voltage for +LV or MID output. The measured value of peak-to-peak ripple is 42.5 mV.

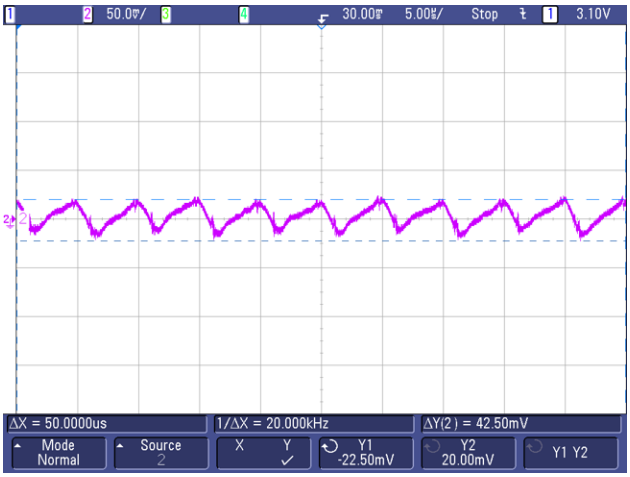


図 64. Output Voltage Ripple for +LV or MID Output at Full load

3.2.2.4 Functional Tests for –LV or Mid-Section

図 65 and 図 66 show the efficiency graph and load regulation plot for the –LV or MID-section in CW-mode.

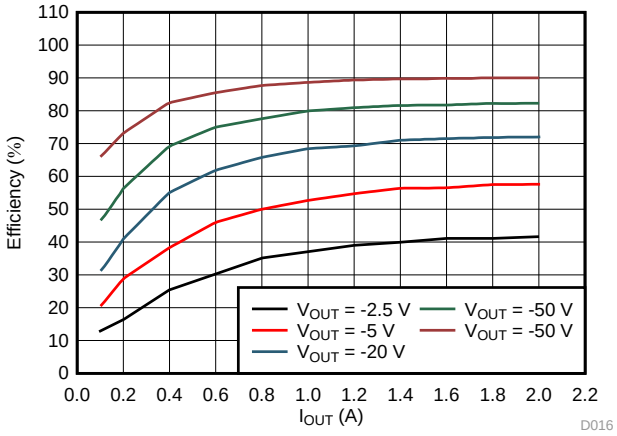


図 65. Efficiency for –LV or MID Section for CW Mode

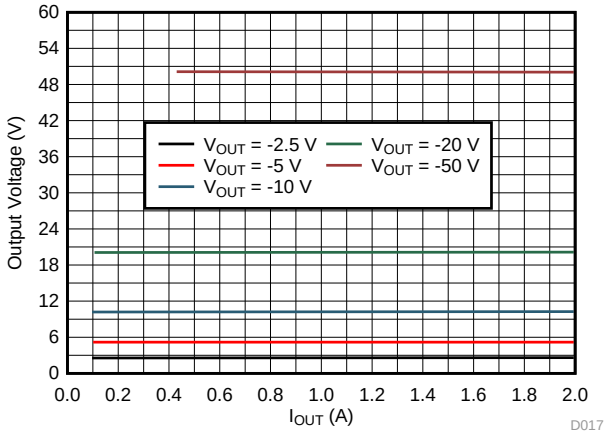


図 66. Load Regulation for –LV or MID Section for CW Mode

図 67 shows the output ripple voltage for the –LV or MID output. The measured value of peak-to-peak ripple is 40 mV.

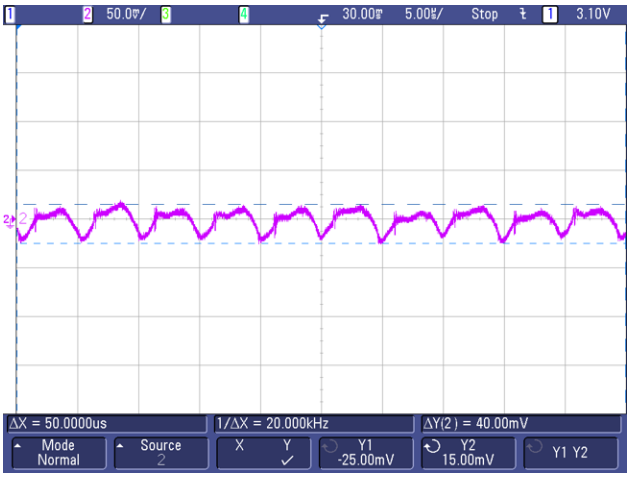


図 67. Output Voltage Ripple for –LV or MID Output at Full load

3.2.2.5 DAC Linearity Test

There are two DACs used in this TI Design. One is to program the output voltage for the ±HV section and other to program the output voltage for the ±LV or MID-section. The linearity of the DACs are tested.

For DAC60004 (U11), the linearity tested from V_{OUT} = ±50-V to ±150-V DC. 図 68 shows the linearity curves for the same.

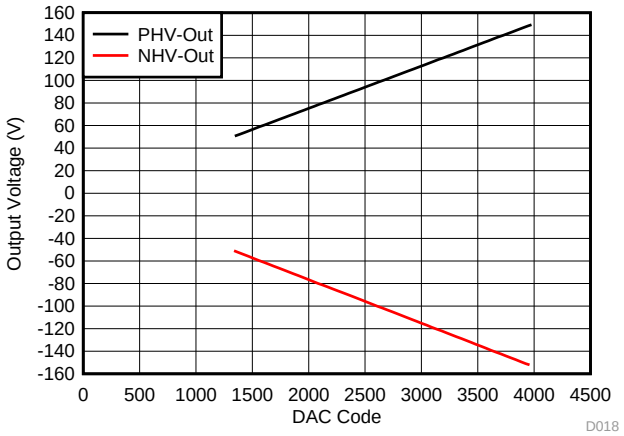


図 68. Output Voltage Linearity for U11 With Respect to Digital Input Code

For DAC60004 (U12), the linearity tested from V_{OUT} = ±2.5-V to ±50-V DC. 図 69 shows the linearity curves for the same.

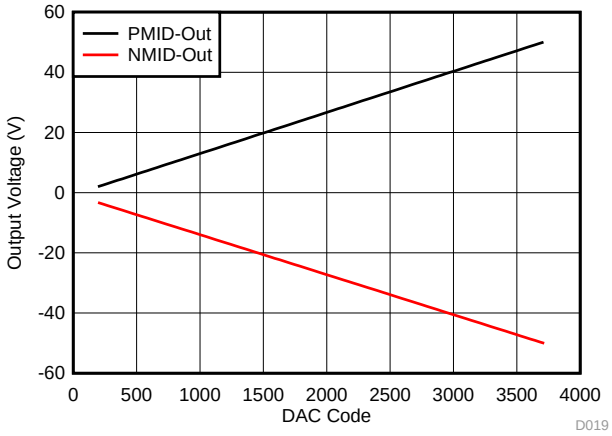


図 69. Output Voltage Linearity for U12 With Respect to Digital Input Code

3.2.2.6 Designed and Measured Voltage Values

表 11 shows the designed and measured voltage values for the TIDA-01352 board.

表 11. Designed and Measured Voltage Values

DESIGNED VALUES	MEASURED VALUES
3.3-V (logic supply for pulser)	3.3238
5-V (pulser level shifter)	5.0082
–5-V (pulser level shifter)	–4.9472
5.3-V rail for DAC	5.2895
5-V reference for DAC	5.0002
VDD for CDCE937 (3.3 V)	3.2858
V_{DDOUT} for CDCE937 (1.8 V)	1.7949
LM5030 V_{CC} for +HV (10.3 V)	10.2354
LM5030 V_{CC} for –HV (10.3 V)	10.3235
LM5030 V_{CC} for +LV or MID (10.3 V)	10.3503
LM5030 V_{CC} for –LV or MID (10.3 V)	10.2269

3.2.2.7 Thermal Image for ±HV Sections

図 70 shows the thermal image for ±HV sections at full load condition.

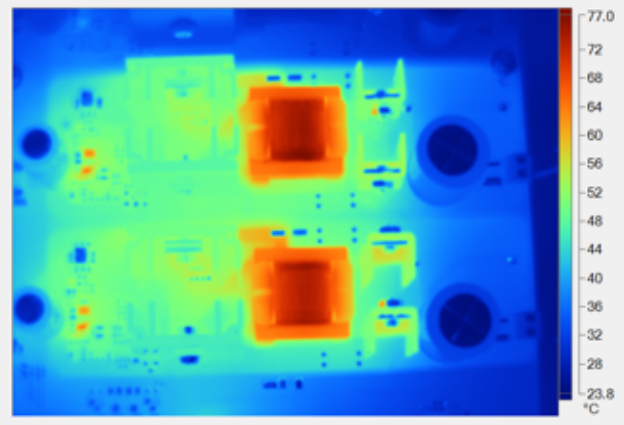


図 70. Thermal Image for ±HV Sections

3.2.2.8 Thermal Image for ±LV or Mid Sections

図 71 shows the thermal image for ±LV or MID-sections at full load condition.

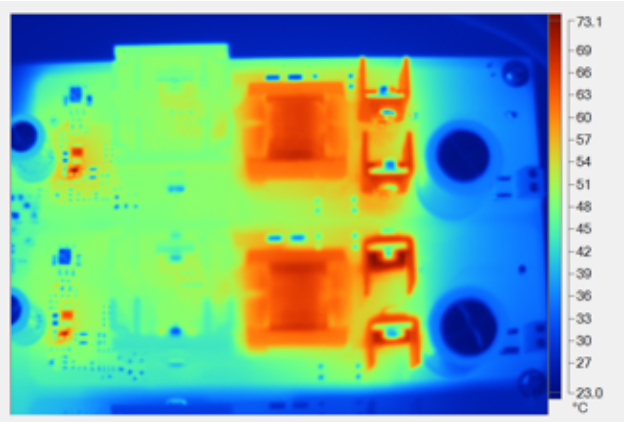


図 71. Thermal Image for ±LV or MID Sections

3.2.2.9 Checking Slew Rate for Outputs

While writing the code into the DAC to set the output, it is important to know what the slew rate is going from a low output to high output. 図 72 through 図 79 show different conditions in which the output slew rates are measured.

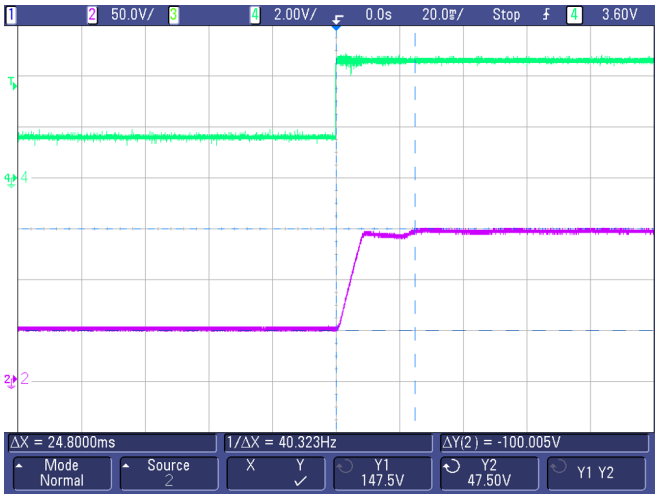


図 72. +HV-Out (Turnon) From 50 to 150 V at Full Load

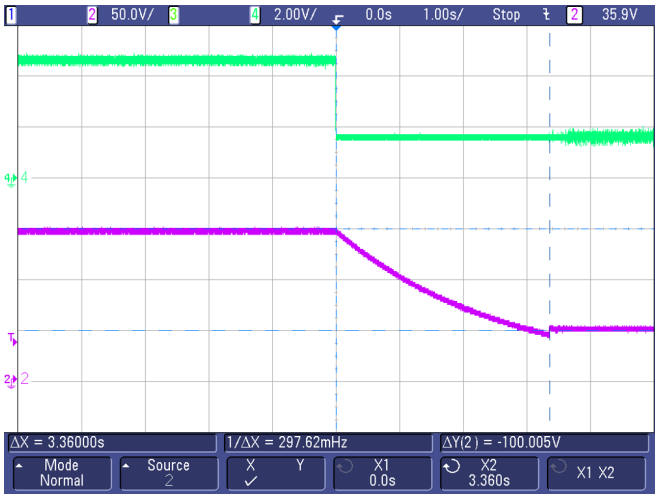


図 73. +HV-Out (Turnoff) From 150 to 50 V at Full Load

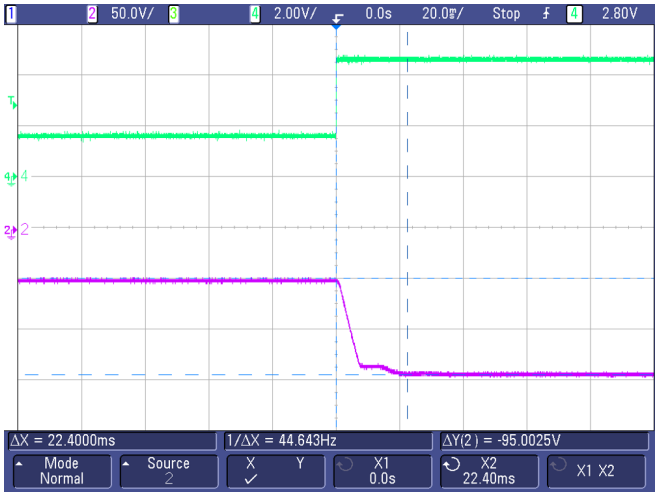


図 74. –HV-Out (Turnon) From –50 to –150 V at Full Load

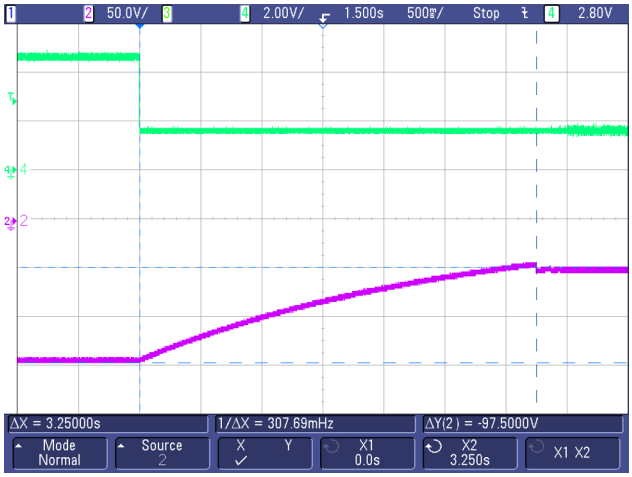


図 75. –HV-Out (Turnoff) From –150 to –50 V) at Full Load

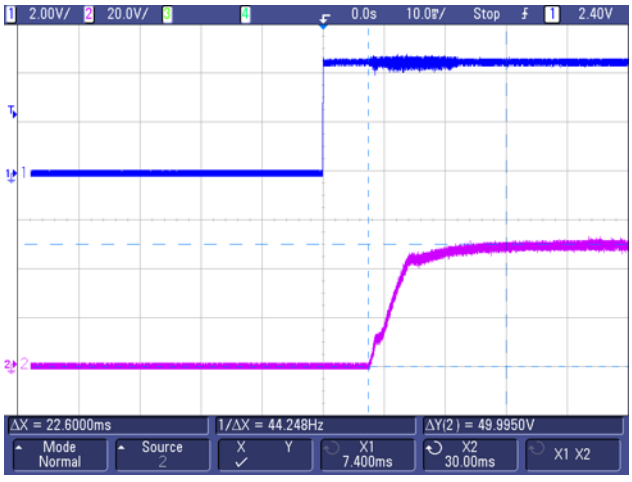


図 76. +LV/Mid-Out (Turnon) From 0 to 50 V at Full Load

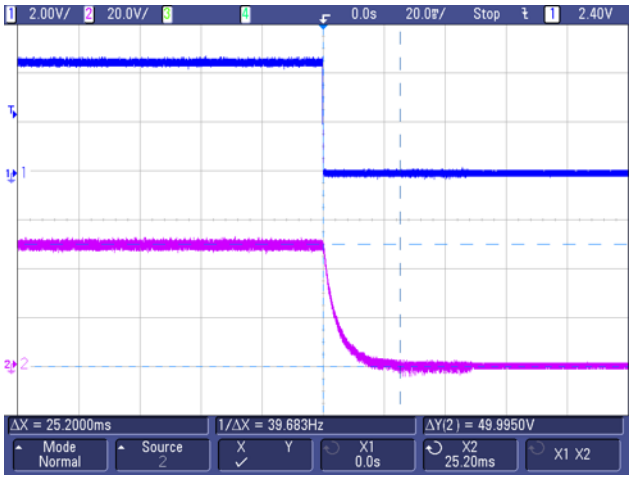


図 77. +LV/Mid-Out (Turnoff) From 50 to 0 V at Full Load

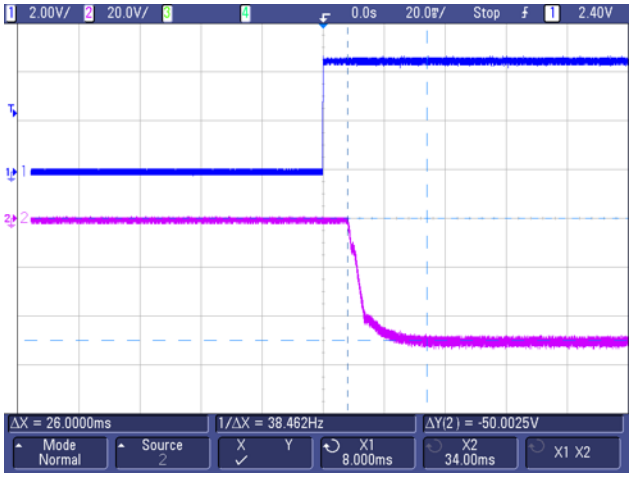


図 78. –LV/Mid-Out (Turnon) From 0 to –50 V at Full Load

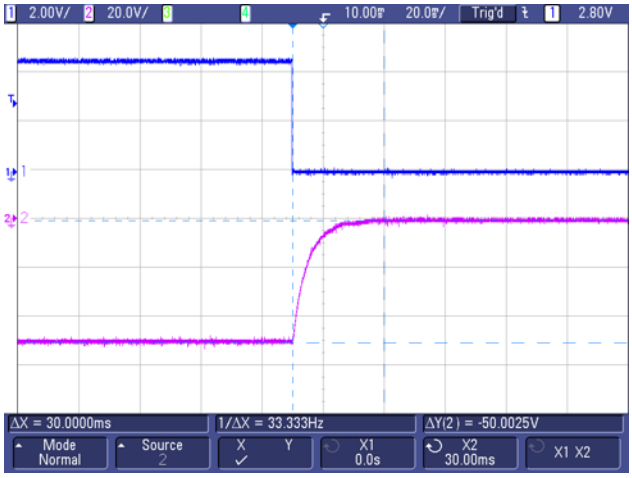


図 79. –LV/Mid-Out (Turnoff) from –50 to 0 V at Full Load

3.2.2.10 Functional Tests for 5-V Generator Circuit Using LMZ34202

This section shows test results for the 5-V generator circuit using LMZ34202. 図 80 shows peak efficiency of 88%. 図 81 shows load regulation of 1.39%.

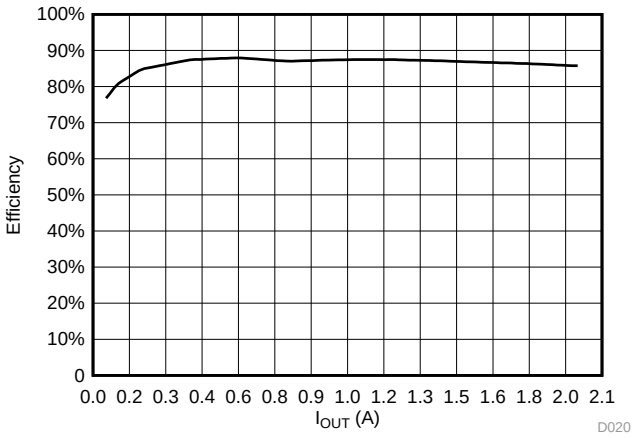


図 80. Efficiency at V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 2 A

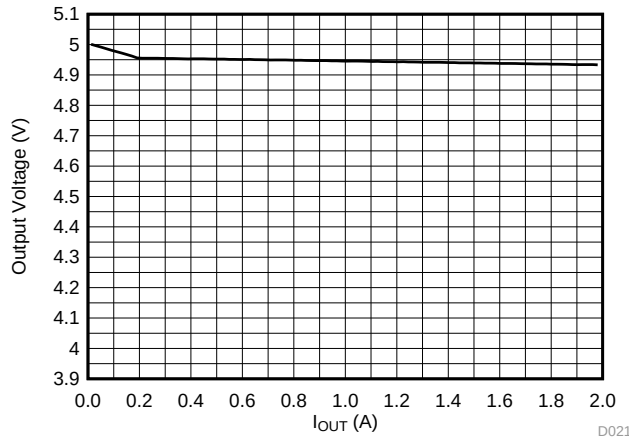


図 81. Load Regulation at V_{IN} = 24 V, V_{OUT} = 5 V

図 82 shows the voltage rail for V_{OUT} = 5 V. 図 83 shows start-up waveform with soft-start. The measured soft-start time is 4 ms, which is default soft-start time for LMZ34202. 図 84 shows the switching waveform and output ripple of 25.6 mV.

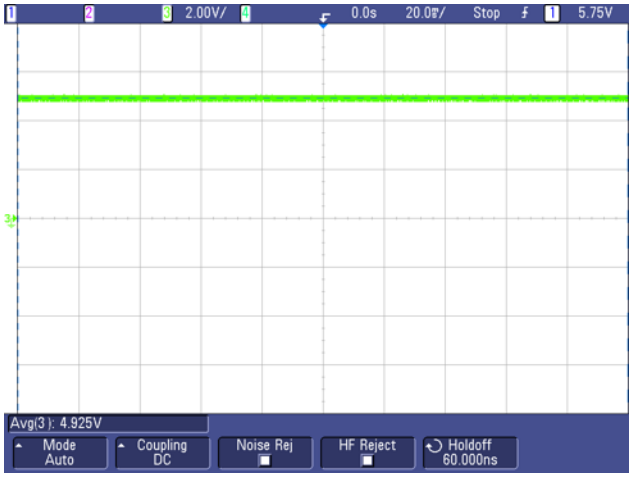


図 82. V_{OUT} = 5 V at V_{IN} = 24 V

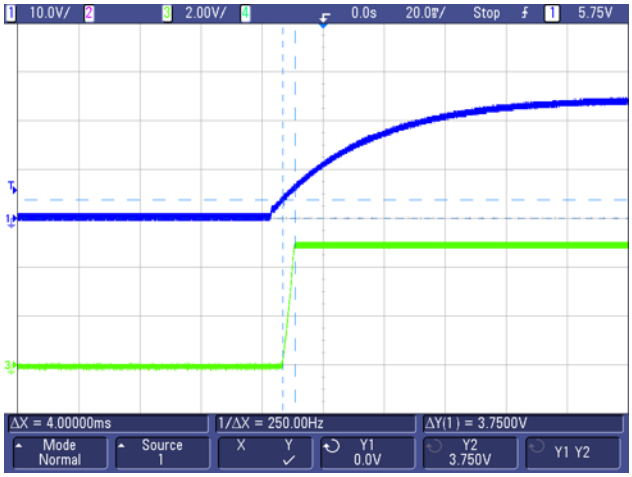


図 83. Start-up Waveform (for V_{OUT} = 5 V) Showing Soft-Start Time = 4 ms

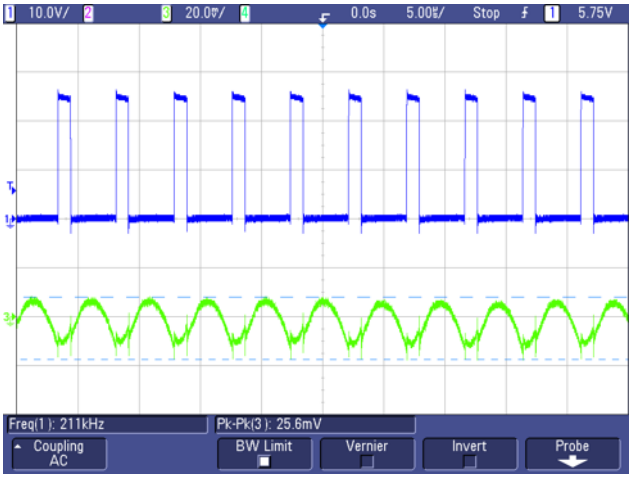


図 84. SW Node Waveform and Output Ripple for V_{OUT} = 5 V, I_{OUT} = 1 A

3.2.2.11 *Functional Tests for 3.3-V Generator Circuit Using LMZ34202*

This section shows test results for 3.3-V generator circuit using LMZ34202. 図 85 shows peak efficiency of 85%. 図 86 shows load regulation of 1.6%.

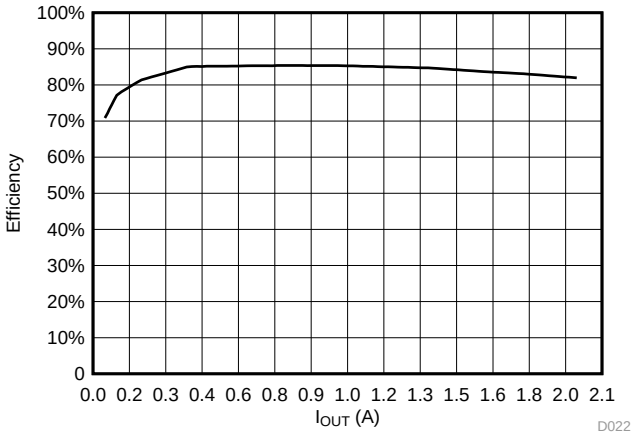


図 85. Efficiency at V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A

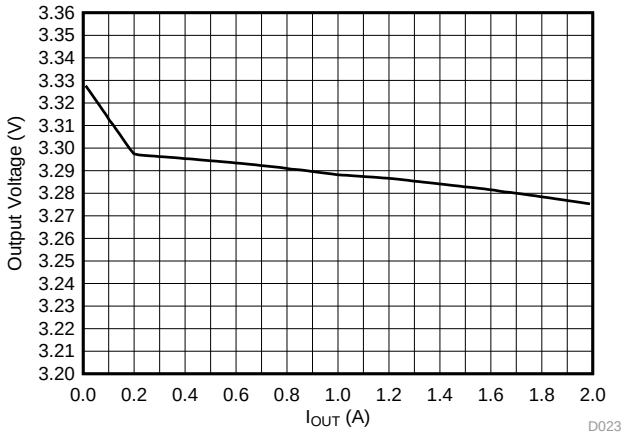


図 86. Load Regulation at V_{IN} = 24 V, V_{OUT} = 3.3 V

図 87 shows the voltage rail for V_{OUT} = 3.3 V. 図 88 shows start-up waveform with soft-start. The measured soft-start time is 4 ms, which is default soft-start time for LMZ34202. 図 89 shows the switching waveform and output ripple of 21.3 mV.

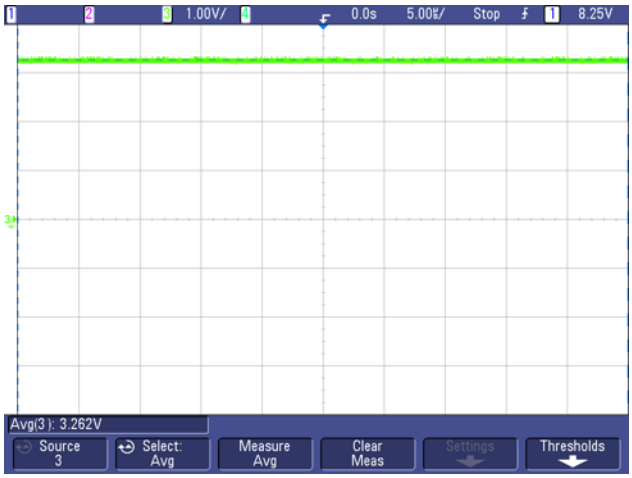


図 87. V_{OUT} = 3.3 V at V_{IN} = 24 V

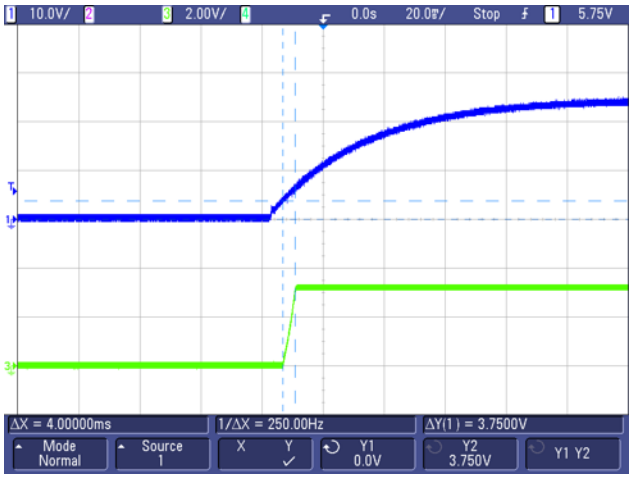


図 88. Start-up Waveform (for V_{OUT} = 3.3 V) Showing Soft-Start Time = 4 ms

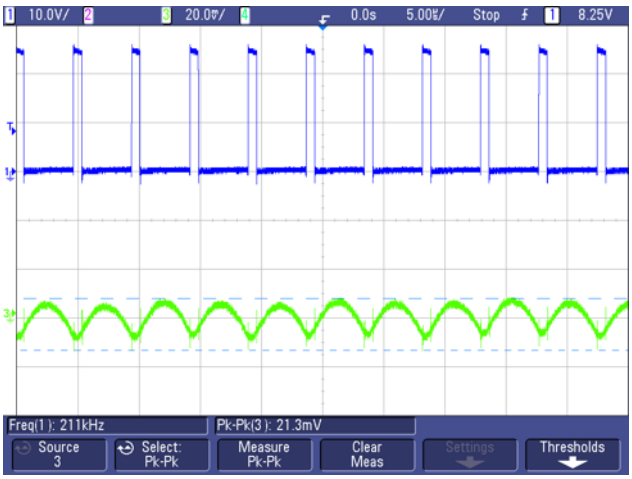


図 89. SW Node Waveform and Output Ripple for V_{OUT} = 3.3 V, I_{OUT} = 1 A

3.2.2.12 Functional Tests for –5-V Generator Circuit Using LMZ34002

This section shows test results for the –5-V generator circuit using LMZ34002. 図 90 shows peak efficiency of 79.7%. 図 91 shows load regulation of 0.55%.

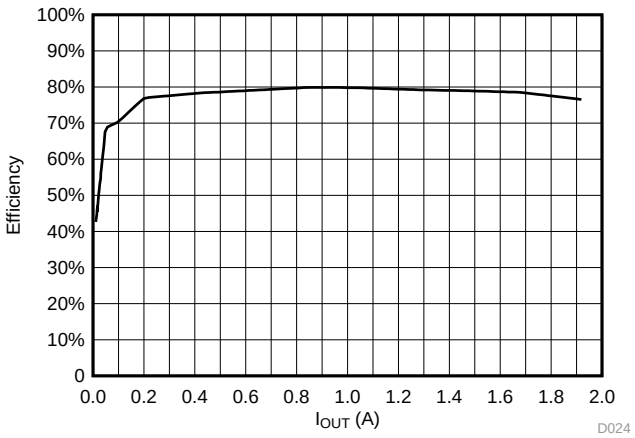


図 90. Efficiency at V_{IN} = 24 V, V_{OUT} = –5 V, I_{OUT} = –2 A

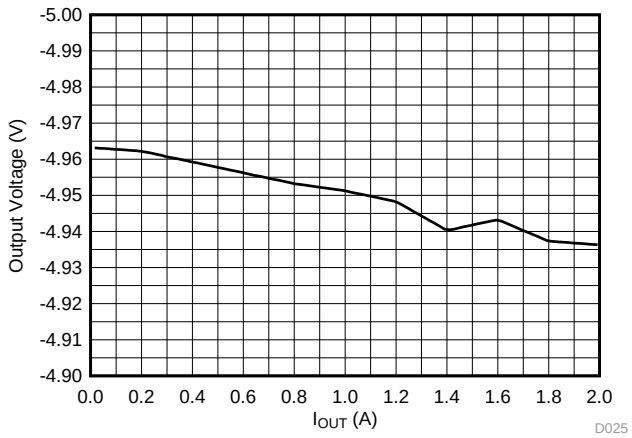


図 91. Load Regulation at V_{IN} = 24 V, V_{OUT} = –5 V

図 92 shows the voltage rail for V_{OUT} = –5 V. 図 93 shows start-up waveform with soft-start. The measured soft-start time is 10 ms, which is default soft-start time for LMZ34002. 図 94 shows the switching waveform and output ripple of 31.9 mV.

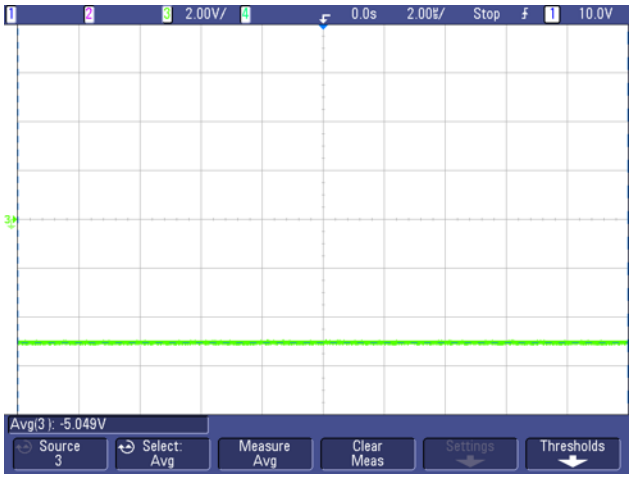


図 92. V_{OUT} = –5 V at V_{IN} = 24 V

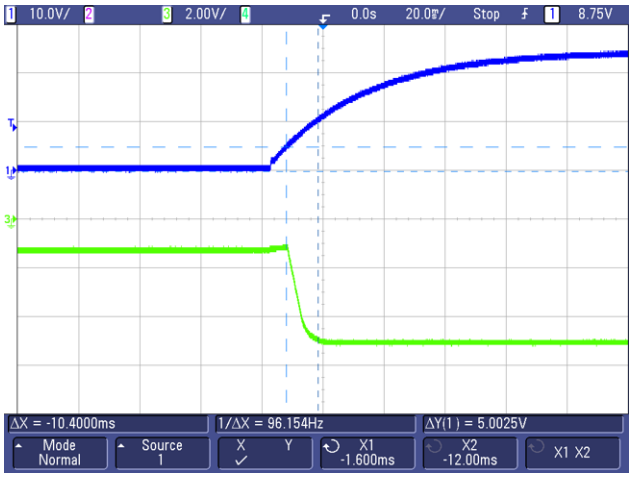


図 93. Start-up Waveform (for V_{OUT} = –5 V) Showing Soft-Start Time = 10.4 ms

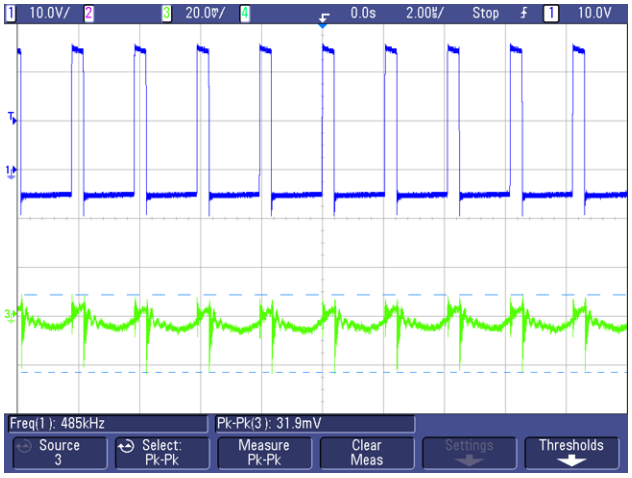


図 94. SW Node Waveform and Output Ripple for V_{OUT} = –5 V, I_{OUT} = –1 A

3.2.2.13 Thermal Image for LV Sections (LMZ34202 and LMZ34002)

図 95 shows the thermal image for LMZ modules at full load condition.

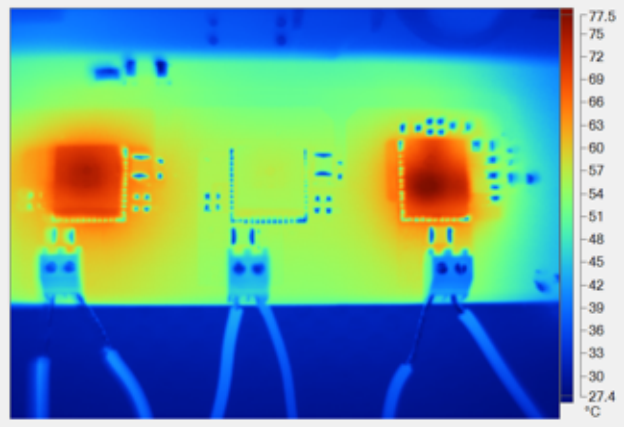


図 95. Thermal Image for LMZ Modules at Full Load

3.2.2.14 Synchronizing With External Clock Signal

One of the important features of this design is that all the power supplies on board are able to synchronize to an external clock signal. The design is tested for such clock synchronization and as an example LM5030 for the +HV section is tested for the same. 図 96, 図 97, and 図 98 show that the OUT+ and OUT– signals of LM5030 are synchronized to external clock frequency of 250 kHz, 300 kHz, and 350 kHz, respectively.

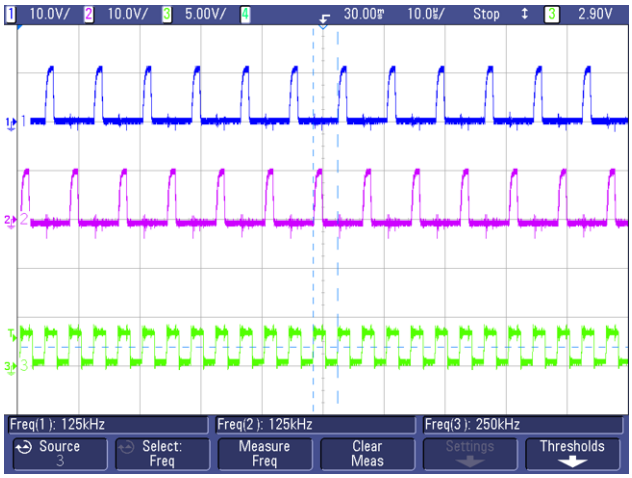


図 96. External SYNC Clock = 250 kHz (Channel 3 in Green)

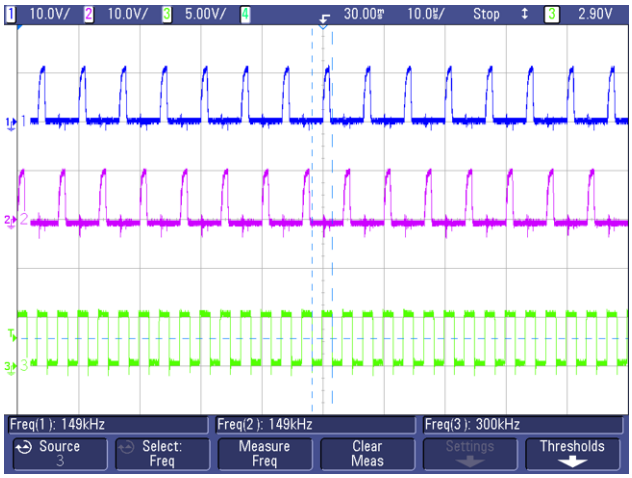


図 97. External SYNC Clock = 300 kHz (Channel 3 in Green)

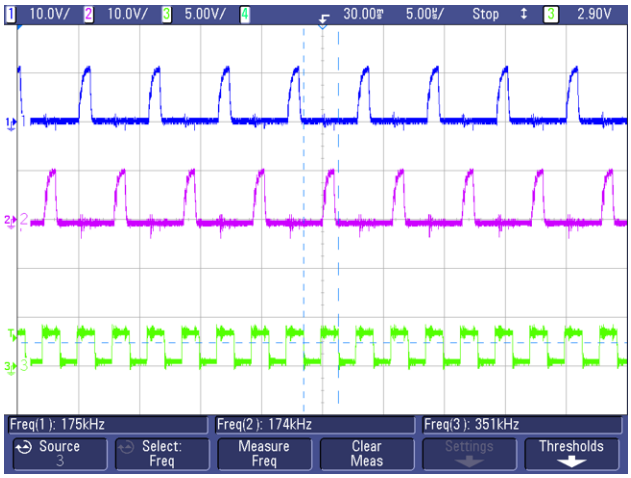


図 98. External SYNC Clock = 350 kHz (Channel 3 in Green)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01352.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01352.

4.3 PCB Layout Recommendations

Device specific layout guidelines for each individual TI part used in this TI Design can be found in the corresponding datasheets. 図 38 and 図 39 show top and bottom views of the TIDA-01352 PCB, respectively. The important sections are highlighted with arrows and captions.

4.3.1 Ground and Power Planes

図 99 shows the ground plane on the mid layer 1 (referred to as ground layer), and 図 100 shows the power plane on the mid layer 2 (referred to as power layer) on the TIDA-01352 board.

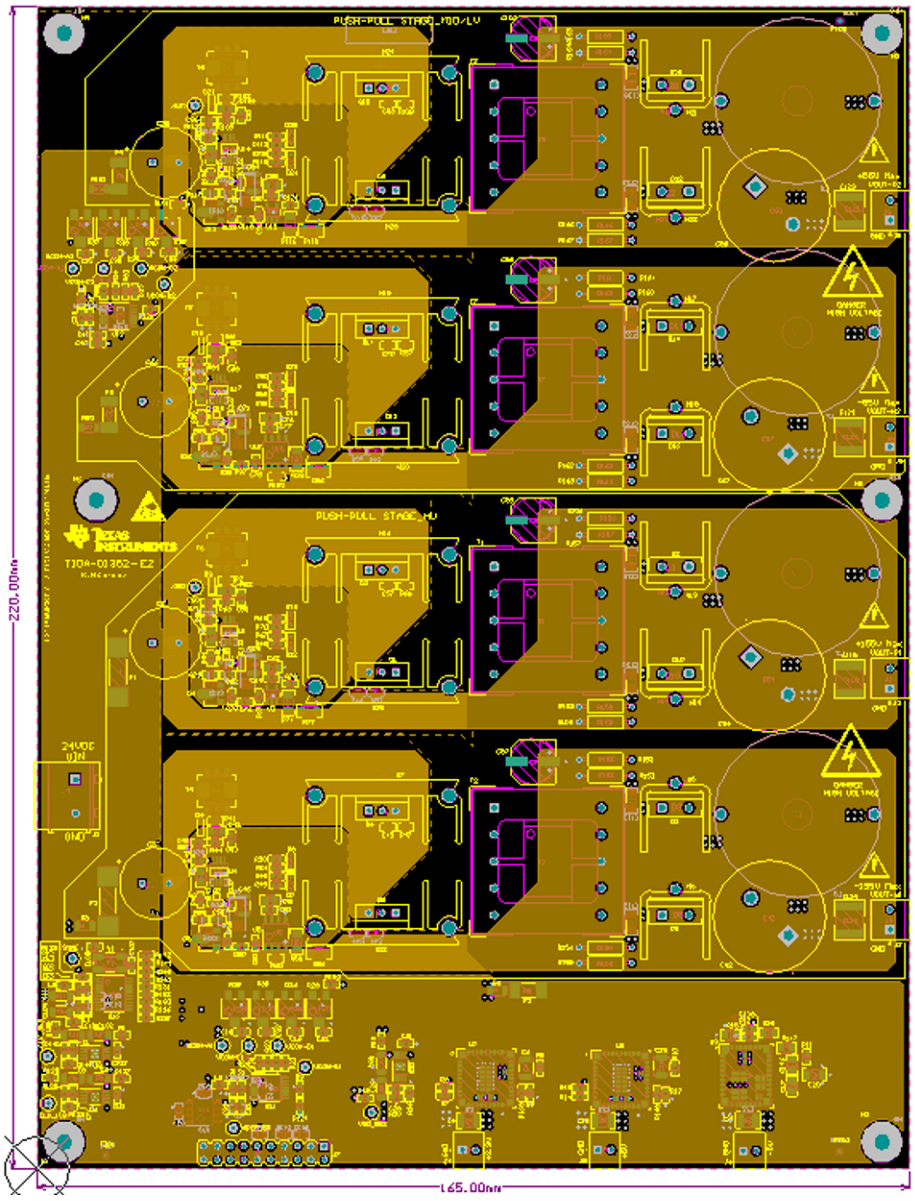


図 99. Ground Planes

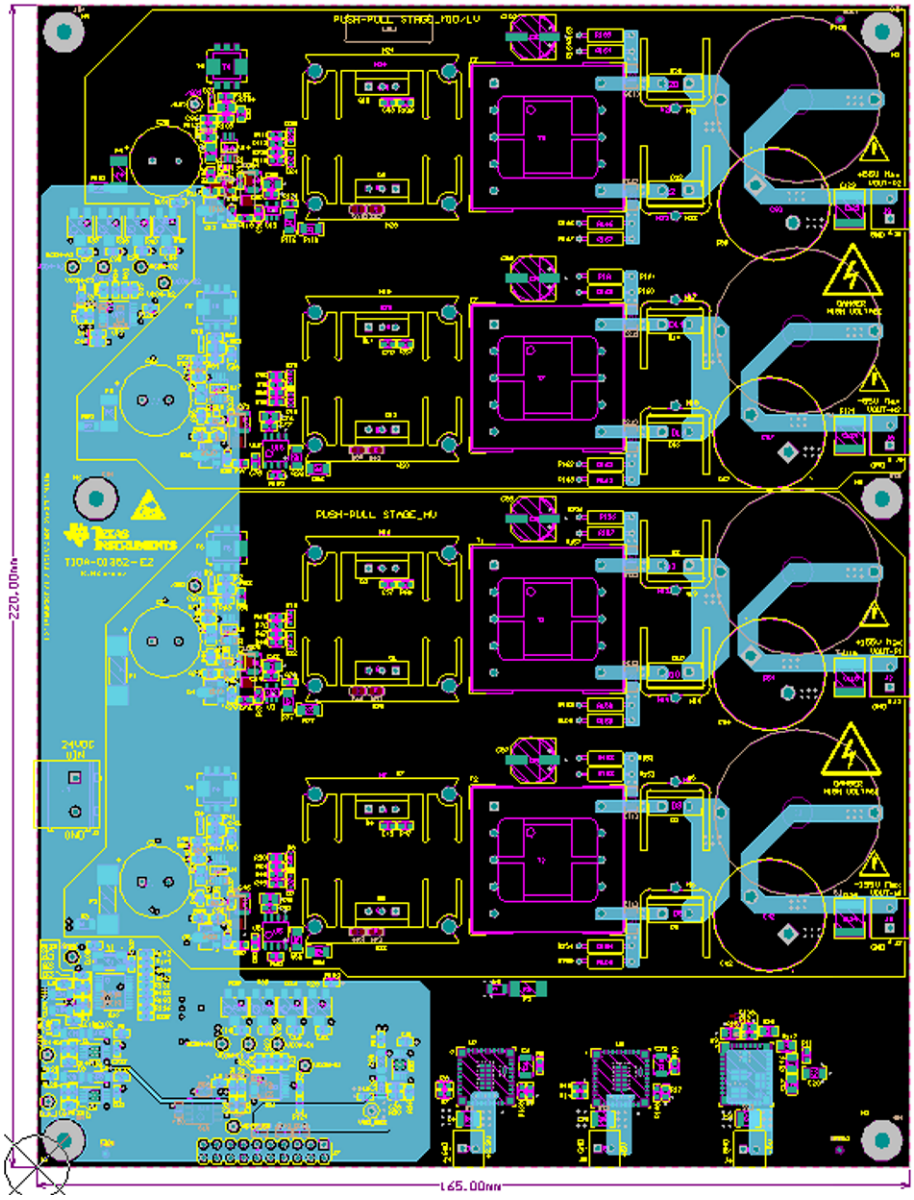


図 100. Power Planes

4.3.2 Star Ground Topology

Grounding is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. 図 101 shows the star ground topology where all the individual ground planes are terminating at negative of the input bulk capacitor.

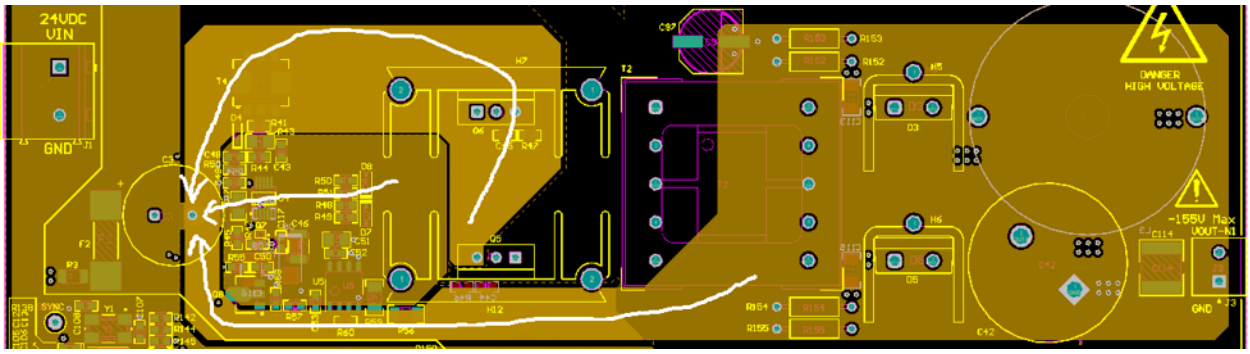


図 101. Star Ground Topology for Power Supply

4.3.3 Layout for CS Pin

Current sensing circuit is critical as it deals with the overcurrent and short-circuit protection of the power supply. The layout and routing for current sense circuit should not mix with the switching ground planes of MOSFETs. 図 102 shows the routing for CS pin of LM5030.

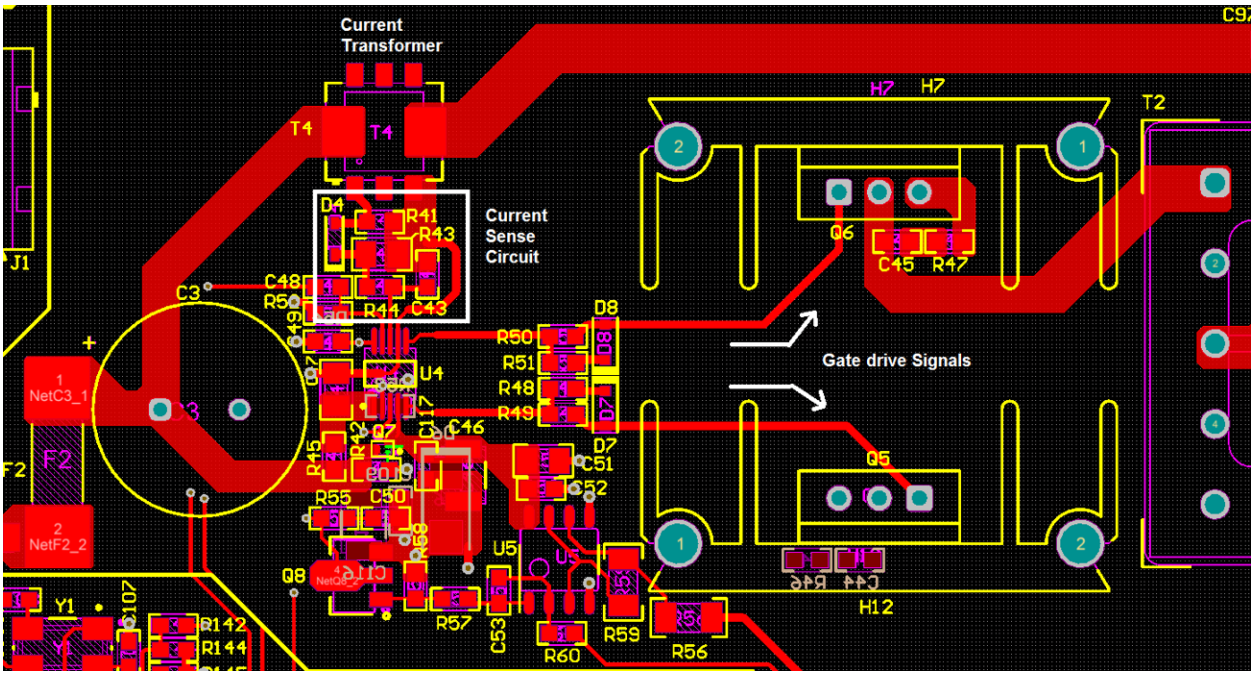


図 102. Routing for CS Pin for LM5030

4.3.4 Layout for LMZ Modules

図 103 shows the layout for LMZ modules.

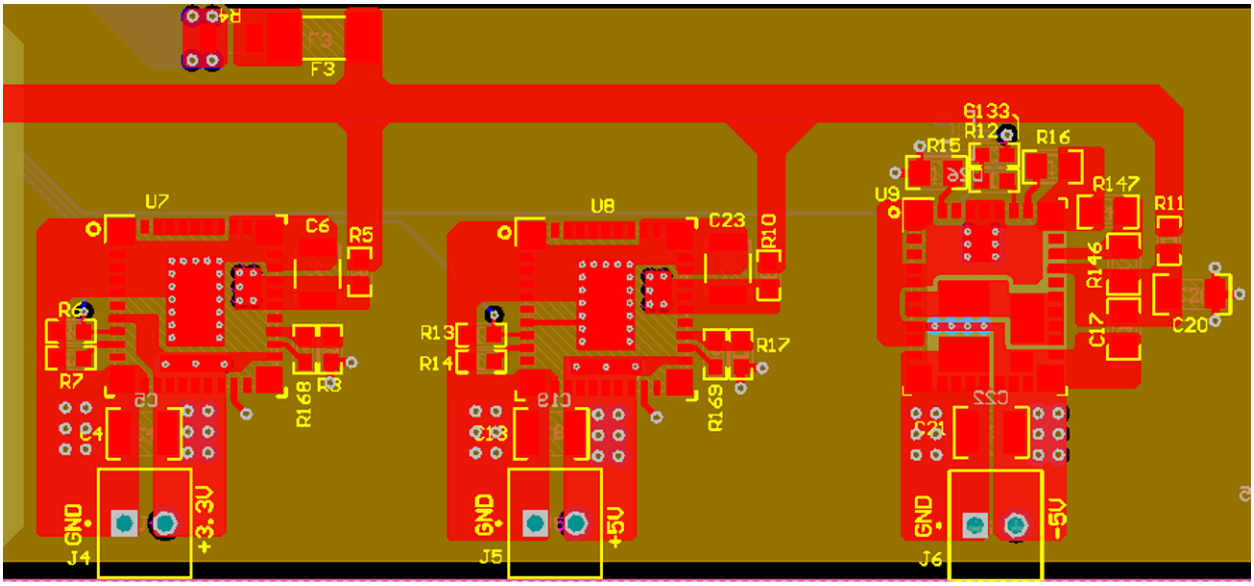


図 103. Layout for LMZ Modules

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-01352.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01352.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01352.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01352.

5 Related Documentation

1. Texas Instruments, *TX517 Dual Channel, 17-Level With RTZ, Integrated Ultrasound Transmitter*, User's Guide (SLOU317)
2. National Center for Biotechnology Information, *A 180-Vpp Integrated Linear Amplifier for Ultrasonic Imaging Applications in a High-Voltage CMOS SOI Technology*, Author Manuscript (https://www.ncbi.nlm.nih.gov/pmc/articles/PMC4406254/)
3. Texas Instruments, *Switching Power Supply Topology Voltage Mode vs. Current Mode*, Design Note (SLUA119)
4. Texas Instruments, *Power Topologies Handbook* (SLYU036)
5. Texas Instruments, TINA-TI Simulation Software
6. Texas Instruments, *LM5030 100-V Push-Pull Current Mode PWM Controller*, LM5030 Datasheet (SNVS215)

5.1 商標

6 About the Authors

SANJAY PITHADIA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Medical Healthcare and Fitness sector. Sanjay has been with TI since 2008 and has been involved in designing products related to energy, smart grid, industrial motor drives, and medical imaging. Sanjay brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Sanjay earned his bachelor of technology in electronics engineering at VJTI, Mumbai.

SANJAY DIXIT is a system architect in the Industrial Systems-Medical Healthcare and Fitness Sector at Texas Instruments, where he is responsible for specifying reference designs.

6.1 Acknowledgment

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