参考資料

TI Designsリファレンス・デザイン
グリッド・インフラストラクチャ・アプリケーション用の10/100Mbps産業用イーサネット・ブリック、IEEE 1588 PTPトランシーバ(ツイストペア/光ファイバ)搭載

TEXAS INSTRUMENTS

TI Designs リファレンス・デザイン

イーサネット・ベースの通信は、グリッド・アプリケーションで使用される多くのシステムに追加されています。イーサネット・インターフェイスは銅線または光ファイバを使用します。イーサネットにより、グリッドはよりスマートで効率的になります。電力グリッドの運用で、タイミングは常に重要な役割を果たしてきました。スマート・グリッドにおいては、時刻情報の役割が、事後の障害解析で履歴データを相互関連させるためのものから、リアルタイムの分析で迅速な是正動作と自動化運転を行うためのものに変化しています。

イーサネットを使用する場合、IEEE 1588規格のPrecision Time Protocol (PTP)により、ナノ秒精度で時刻を同期できます。IEEE 1588規格のPTPでは、分散システム内の既存のイーサネット・ネットワークで使用するNetwork Time Protocol (NTP)と同等の精度とコスト効果を実現できます。

このTI Designは、Precision PHYTER™の機能を実証するための小型イーサネット・ブリックです。PHYTERは、時刻情報をデコードするためTiva™ MCUに接続されています。このTI Designでは、10/100Mbpsの銅線インターフェイスまたは100Mbpsの光ファイバ・インターフェイスと、小型のLCコネクタ付きトランシーバを組み合わせて構成できます。

設計リソース

TIDA-00496	デザイン・フォルダ
DP83630	プロダクト・フォルダ
TPS75433	プロダクト・フォルダ
TM4C129XNCZAD	プロダクト・フォルダ
TPS62177	プロダクト・フォルダ
DP83849	プロダクト・フォルダ
INA196AIDBVR	プロダクト・フォルダ
TPD4E1U06DCK	プロダクト・フォルダ
CDCE913PW	プロダクト・フォルダ

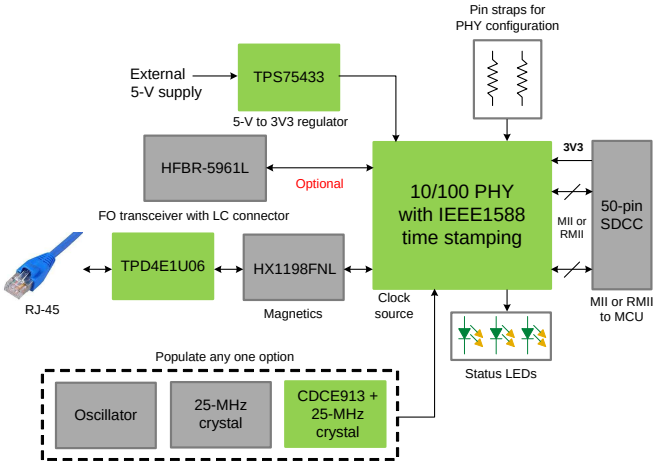
TI E2E™ Community　E2Eエキスパートに質問

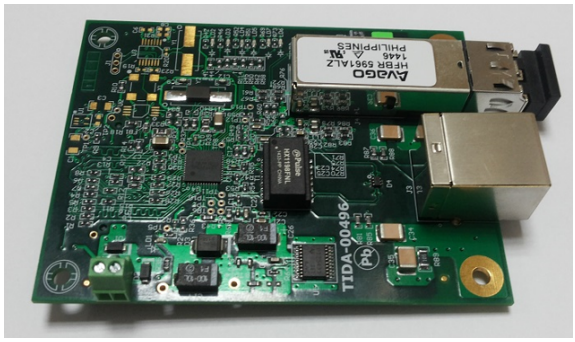
デザインの特長

- 10/100Mbpsのツイストペア(銅線)インターフェイスと100BASE-FX光ファイバ・インターフェイスでテスト済み
- DP83630 Precision PHYTERを基盤とし、IEEE 1588 PTPトランシーバはIEEE 1588 V1およびV2に対応
- 消費電力: 銅線、3.3Vにおいて350mW未満
- 通信およびIEEE 1588機能テストのため、Tiva MCU TI Design (TIDA-00226)と接続
- LCコネクタ付きのHFBR-5961L/ALトランシーバ: Fast Ethernet FOインターフェイスに使用した場合、3.3Vでトランスミッタ175mA未満、レシーバ120mA未満の消費電力
- 出力定格2Aのオンボードldoを搭載
- リンク、動作、速度を示す3つのプログラム可能LED
- ESD IEC61000-4-2準拠で6KVまでの接触放電テスト済み
- 産業用温度範囲: -40℃～85℃でPHYの動作を規定

主なアプリケーション

- マージング・ユニット
- IEC61850の機能に対応した保護リレー
- IEC61850に対応した電源品質アナライザ
- デジタル・フォルト・レコーダ
- 変電所自動化用のPTPサーバー
- PTPからPPSへのコンバータ
- IEC61850準拠のイーサネット・スイッチ





1 System Description of Electrical Substation

1.1 Time Synchronization in a Smart Substation

The generation and distribution of energy is a sophisticated, mature industry. Synchronizing generators, or keeping them in phase at 50 or 60 cycles per second across an electricity grid, is a common and accepted part of their safe and effective management around the world. Not doing so wastes energy and ultimately serious damages the system. Consequently, synchronization has been built into the core power system design for many years. Their growing importance is making time synchronization an integral part of the increasingly sophisticated control systems that are crucial to managing the modern power utility.

Time synchronization plays a pivotal role in two key areas:

1. Improving the accuracy of fault diagnosis and the subsequent quality of decision making, which helps reduce down time
2. Ensuring electricity networks are operating efficiently within system limits by helping increase the accuracy of control decisions by automatic control and protection equipment

As long as all processes and events in a facility like a substation are controlled from one singular central point, the absolute accuracy of the stations system time is not really important. However, as soon as time-synchronized switching events involving more than one substation have to be performed, the absolute accuracy of each station's time reference gains significant importance.

1.1.1 Challenges in Substation Timing

Currently, a lot of measurement and control data in the power grid must have an absolute accuracy of approximately 1 ms:

- SCADA data
- Data from event and disturbance recorders
- Time stamped data from protection relays (IEDs)
- Lightning strike correlation

A time accuracy of 1 ms is relatively easy to reach, but some current and emerging future measurement applications require a much higher accuracy. The applications mentioned in 表 1, for example, require an absolute accuracy of 1 μs or better:

- Sampled values
- Synchrophasor measurements
- Traveling wave fault location

表 1. Timing Accuracy for Different Time Sync Protocols

PROTOCOL	MEDIA	SYNC ACCURACY
NTP	Ethernet	1 to 10 ms
IRIG-B	Coaxial	1 to 10 ms
PTP	Ethernet	20 to 100 ns

1.1.2 Approaches for Time Synchronization

There are two main approaches for synchronizing protection relays and other control devices:

- Dedicated timing systems that use stand-alone cabling and repeaters
- Networked timing systems that use Ethernet networking cables and switches shared with other automation applications

Dedicated Timing Systems

Time synchronization systems in substations have historically used a separate distribution system with its own cabling (coaxial, twisted pair, or fiber optic). Two common methods in use are:

- IRIG-B time code, conveying time, and date information along with synchronization pulses
- One pulse per second (PPS), which is a very accurate synchronization pulse that has no time of day or date information

Networked Timing Systems

The Ethernet networks now widely used for substation automation systems can synchronize the internal clocks of devices throughout a substation. This has the advantage of not requiring additional cabling, but this does require support for suitable protocols by the various protection relays, power quality meters, and other such devices. Two network-based protocols are commonly used: NTP and PTP. Both protocols, when used in substations, work through the exchange of messages over Ethernet. NTP and PTP can compensate for propagation delay through bidirectional communication. NTP is a more established standard and is widely used, but PTP offers greater performance through the use of special networking hardware.

1.2 Power System Automation

Power system automation is one of the important aspects in an electrical power network. In power system automation, data acquisition system plays a major role as a base of the power system automation. From the recent trends and developments in power system automation, computerized system automation is most efficient compared to normal systems. A computerized power network for a data acquisition system helps the system and controller to meter and monitor the values for further manipulations for full-scale power system automation and system controlling.

The computerized data acquisition for metering and monitoring of power system automation can be divided into three general categories: data collection, metering, and monitoring. The data collection system collects data from the power system network using the digital power monitors through the current and potential transformers. The collected data will be metered by the digital power monitor consisting of a microcontroller (MCU) with peripherals like memory, an A/D converter, and sample and hold circuitry. According to the programming done in the MCU, the power monitor will store the parameters in the memory and will perform all the logical and arithmetic calculations to manipulate the parameters and to calculate the different power data like KWH, KVAR, KVA, PF, and so on. The collected parameters of the power system and the calculated power data can be monitored on the screen of the digital power monitor. The values are then sent to the computer system using the communication system like serial communication RS-485 and RS-232 for n number of power monitors using the data converter.

Structure of Power System Automation

The functional structure of power system automation will be as follows:

- Electrical protection
- Control
- Measurement
- Monitoring
- Data communications

Benefits of Power System Automation

Important benefits of automation are as follows:

- Improved quality of service and reduced manpower requirements
- Improved reliability with reduced system implementation costs
- Maintenance and expansion of customer base and reduced operating costs
- High value service provider and reduced maintenance costs
- Added value services with the ability to defer capacity addition projects
- Improved customer access to information and also improved information for engineering decisions
- Enterprise information accessibility along with improved information for planning decisions
- Flexible billing options and reduced customer outage minutes

1.3 Classification of Power System Automation

1.3.1 Substation Automation

For many years, substations have been equipped to perform automatic reclosing, bus sectionalizing, load transfers, capacitor switching, and so on. In the past, these and other functions were implemented using a combination of control panels, auxiliary relays, switches, lights, meters, transducers, and extensive wiring and cabling.

Modern protection relays are called intelligent electronic devices (IEDs), which typically consists of one or more protection systems and communications ports. IEDs can transmit data, execute control commands, and frequently provide a local user interface. Typical examples are relays, meters, and specialized sensors.

Only one panel is required when numerical relays are used. Interestingly, at the same time the space requirements are reduced by a factor of four, as is the installed cost. Advances in communications technology tie everything together into a useful network. Within the substation, a single high-speed Local Area Network (LAN) transmits data and control commands, replacing the extensive and costly cables that had been required. At the present time, a number of different LAN techniques and protocols are in use. The industry is actively working on development of a new standard LAN definition that will be based on the use of Ethernet and Manufacturing Messaging Specification (MMS) and will be compatible with the Utility Communications Architecture (UCA™). There are already many techniques for moving data out of the substation to a master station or to other substations. These include the use of leased or dedicated telephone lines, dial-up phone lines, cellular telemetry techniques, satellite transmissions, various flavors of radio techniques, and fiber-optic networks. This variety of communications methods results in the ability to transmit large amounts of information at a rapidly declining cost per bit.

Substation automation components are:

- Remote terminal unit
  - Telemetry and remote control device
- IEDs
  - Implements functions in a substation, such as a protection relay
- Bay controller
  - Controls all devices related to a single bay (transformer, feeder, and so on) and communicates with relays for functionality
- Human machine interface (HMI)
  - Typically an industrial PC with operator console for local control and system configuration
- Communication buses
  - Connection between devices
- Upwards communication interfaces
  - Implemented in the HMI, the bay controller, or an IED

1.3.2 Distribution Automation

Distribution automation systems enable an electric utility to monitor, coordinate, and operate system components in a real-time mode from remote locations. The distribution automation is modular and may be implemented in phases to include remote monitoring and control of substation, feeder, and consumer devices and loads.

The goals of distribution automation are:

- Reduced costs
- Improved service reliability
- Better consumer service
- Enhanced government relations

1.4 Communication in a Substation

1.4.1 Serial Communication

RS-232, RS-422, and RS-485 are serial communication methods for substation and protection applications. RS-232 is the best known and widely implemented interface. However, some of the other interfaces can be used in situations where RS-232 is not appropriate (for example, for long distances or when there is a need to network multiple devices).

RS-232 is an interface to connect one data terminal equipment (DTE) to one data communication equipment (DCE) at a maximum speed of 20 kbps with a maximum cable length of 50 ft. This was sufficient when almost all computer equipment were connected using modems, but soon after people started to look for interfaces capable of one or more of the following:

- Connect DTEs directly without modems
- Connect several DTEs in a network structure
- Ability to communicate over longer distances
- Ability to communicate at faster rates

RS-485 is the most versatile communication standard in the standard series defined by the EIA, as it performs well on all four points. That is why RS-485 is currently a widely used communication interface in data acquisition and control applications where multiple nodes communicate with each other.

1.4.2 Migration From Serial Communication to Ethernet

Serial communications were traditional in utilities installations; they were well understood and proven, available in robust packaging, and with adequate speed for their time. They required continuous point-to-point connections for operation. However, serial lines have been often associated with proprietary protocols and limited speed. Ethernet connectivity is becoming more popular because it offers standards-based interoperability and performance, along with the hardened characteristics required for many utilities installations. As older substations with serial communications are upgraded, serial interfaces are being replaced by Ethernet connections.

Ethernet's simple and effective design has made it the most popular networking solution at the physical and data link levels. With high speed options and a variety of media types from which to choose, Ethernet is efficient and flexible. These factors and the low cost of Ethernet hardware have made Ethernet an attractive option for industrial networking applications. Also, the opportunity to use open protocols such as TCP/IP over Ethernet networks offers the possibility of a level of standardization and interoperability. The result has been an ongoing shift toward the use of Ethernet for Grid Infrastructure applications. Ethernet is increasingly replacing proprietary communications.

1.4.2.1 Advantages With Ethernet

Because Ethernet is a standard, it is the least expensive way to have connectivity. Being a standard means more choices in products that can connect together and a greater potential for reasonably priced replacement components and long-term support. As a standard, Ethernet is the protocol of choice for new technologies that are being introduced in industrial facilities such as factories and substations. It is more profitable today for developers of technologies such as programmable controllers, dual-ported IEDs, and low-cost security cameras to introduce a product that will work with a large variety of installed

communications devices than to go to the expense of developing specific versions to meet proprietary communications requirements. Further, with Ethernet using fiber cabling, bandwidth is essentially free because it is practically unlimited for a one-time installation cost. An added benefit, of course, is that industrial Ethernet is compatible with IT facilities and eliminates a conversion bottleneck where factory and corporate networks meet.

1.4.3 Fiber versus Copper

While fiber cable is preferred for noise immunity, twisted pair cabling also has a role in substations. Within control room rack cabinets, copper cabling is safely used for short Ethernet interconnections. The same twisted pair cable and RJ45 port connectors can be used for both 10-Mbps and 100-Mbps speeds, simplifying installations. The assumption has been that copper cabling is less costly, so most RTU and IED manufacturers use RJ45 ports on their products for both lower cost and 10/100-Mbps compatibility. This makes some use of copper necessary even if only to connect to a nearby media converter.

However, the comparative cost of fiber and UTP copper needs to be re-examined. A recent analysis of the installation costs of copper versus fiber (typical for new substations and upgrades) shows surprisingly little difference.

1.4.3.1 Advantages of Fiber Optic

- Galvanic isolated and robust communication interface
- Cabling distance is greater than UTP cable to meet wide range demands and reduced communication failures
- Harsh environment capability: EMI immunity, high temperature, high pressure, high voltage
- No grounding required
- Intrinsically safe, small size, and lightweight
- Integrated telemetry: fiber itself is a data link
- Wide bandwidth and high sensitivity

1.4.4 Ethernet Speed

Initially, fiber with Ethernet was operated at a 10-Mbps speed, more than enough bandwidth to move data in the substation. As noted above, the trend now is to use fiber at a 100-Mbps speed because there is no longer a cost premium for 100 Mb. However, 100 Mb will soon be a necessity. Three major changes in substation operations are driving the need for a 100-Mbps full-duplex Ethernet speed: security, time synchronization per IEC61850, and redundancy.

Security: Substations are a vital part of essential public services. Pressures to secure facilities continue to grow. An example of an increasingly popular security tool is video surveillance. Video requires roughly 5 Mb of bandwidth to support one uncompressed picture-quality full-motion video image data stream. A 100-Mbps Ethernet environment can easily accommodate several security cameras without compromising other LAN traffic.

Time Synchronization per IEC61850: One of the areas the emerging IEC61850 standard addresses is the data movement associated with sampling and digitization of voltage and current measurements within a substation. Protection IEDs base their decisions on current and voltage samples, measured by other IEDs. The sample data must be moved and synchronized within a few milliseconds to assure proper decisions, and thus assure proper relay and power switching operations. Within a substation, typically 25 to 75 IEDs will be transmitting time-critical sample data. This high data rate can be handled reliably in a single common network by 100-Mbps full-duplex multi-casts Ethernet over fiber media, possibly with multiple VLAN segments in larger substations.

Redundancy: The mission-critical communications services for substations need a high level of availability. Within the Ethernet network serving a substation, redundancy is fairly easy to achieve. Networked devices may be sequentially connected by fiber cabling in a ring structure, with any two segments of a ring able to recover from any fault in the ring. With dual-ported IEDs and dual redundant rings, even multiple faults will typically not cause problems from loss of data connectivity. The ring topology—connecting multiple substation devices in series—drives up the bandwidth required in the ring and 100-Mbps full-duplex Ethernet can handle the load.

1.5 PTP

IEEE Standard 1588-2008 specifies the second generation of PTP, which is also known as "PTPv2" or "1588v2". This is capable of very accurate time synchronization by using special Ethernet hardware that records the exact time a PTP synchronization message is received at the Ethernet card. This information can compensate for the uncertainty introduced by real-time operating systems and other processing delays in both the synchronization master and the devices that are to be synchronized. The time-stamping hardware does not affect the operation of any other protocols running over Ethernet, so the same port can be used for IEC 61850, DNP3, IEC 60870-5-104, Modbus/IP, and other substation automation protocols. The PTP-specific hardware does marginally increase the cost of Ethernet switches. Native support for PTP is only available in the latest generation of protection relays and may be an option to be specified at the time of order (depending on the vendor). PTP supports multiple master-capable clocks, but these vote amongst themselves to choose a single clock to be the “grandmaster”. If the grandmaster fails or suffers degraded performance any other master-capable clock on the network will step up to be the grandmaster if it has better accuracy. The time required for this does vary; however, if PTP settings (known as a "profile") optimized for the power industry are used, this is usually less than 5 seconds.

1.5.1 PTP Clock Types

- Grandmaster: Synchronized with an external source as a GPS satellite (GPS clocks).
- Ordinary clock: Can act either a master or a slave (protection relay). In most network implementations, the clocks remain in the Slave state and only become master when the grandmaster fails.
- Transparent clock: Corrects the time information before forwarding it without synchronizing itself (managed Ethernet switch).
- Boundary clock: Acts as a slave to the upstream master clock, and master clock to downstream slave clocks (managed Ethernet switch).

The PTP clocks can be either one-step or two-step ones; their mixing should be avoided. Two-step clocks send sync messages (which contain the approximate time) and follow-up messages (which contain a more precise value of when the sync message left the clock). One-step clocks do not send follow-up messages. Instead, the sync message carries a precise time stamp. The one-step mode is preferable.

1.5.2 IEEE 1588 Standard

IEEE 1588 is a standard for a precision clock synchronization protocol for networked measurement and control systems. This defines a PTP designed to synchronize real-time clocks in a hierarchical distributed system. IEEE 1588 features include:

- Intended for LAN using multicast communications
- Targeted accuracy of microseconds or sub-microsecond
- IEEE 1588v1 originally was designed for time distribution for the measurement and control industry.
- IEEE 1588v2 is designed to distribute frequency and time to a higher accuracy and precision, to the scale of nanoseconds and fractional nanoseconds.
- The protocol operates over packet switched networks. The standard is currently defined to run over IEEE 802.3, UDP/IPv4, UDP/IPv6, DeviceNet, ControlNet, and PROFINET.
- Designed to operate automatically to establish master-slave hierarchy for time distribution. (not for the telecommunications industry)
- Introduces “transparent clocks” to overcome the network’s delay variation.

1.5.2.1 Applications

Version_1 of the protocol is used for applications in:

- Industries (for example, Automation)
- Test and measurement
- Power networks
- Military and Avionic

Version_2 (released June 2008) is made for applications in:

- Telecom
- Broadcasting
- Power and Utilities

1.6 Other Features of IEEE 1588 Ethernet PHY

表 2. DP83630 — Additional Features

FEATURES	DESCRIPTION
Internal loopback	The DP83630 includes a Loopback Test mode for facilitating system diagnostics. The Loopback mode is selected through bit 14 (Loopback) of the Basic Mode Control Register (BMCR). Writing 1 to this bit enables MII transmit data to be routed to the MII receive outputs. Loopback status may be checked in bit 3 of the PHY Status Register (PHYSTS). While in Loopback mode the data will not be transmitted onto the media. To ensure that the desired operating mode is maintained, autonegotiation should be disabled before selecting the Loopback mode.
Energy detect mode	When Energy Detect is enabled and there is no activity on the cable, the DP83630 will remain in a low power mode while monitoring the transmission line. Activity on the line will cause the DP83630 to go through a normal power up sequence. Regardless of cable activity, the DP83630 will occasionally wake up the transmitter to put ED pulses on the line, but will otherwise draw as little power as possible. Energy detect functionality is controlled via register Energy Detect Control (EDCR), address 1Dh.
Link diagnostic capabilities	The DP83630 contains several system diagnostic capabilities for evaluating link quality and detecting potential cabling faults in twisted pair cabling. These capabilities include: • Linked Cable Status • Link Quality Monitor • Time Domain Reflectometry (TDR) Cable Diagnostics
Polarity reversal	The DP83630 detects polarity reversal by detecting negative link pulses. Inverted polarity indicates the positive and negative conductors in the receive pair are swapped. Since polarity is corrected by the receiver, this does not necessarily indicate a functional problem in the cable. Since the polarity indication is dependent on link pulses from the link partner, polarity indication is only valid in 10-Mb modes of operation, or in 100-Mb autonegotiated mode. Polarity indication is not available in 100-Mb forced mode of operation or in a parallel detected 100-Mb mode.
Cable swap indication	As part of autonegotiation, the DP83630 has the ability (using Auto-MDIX) to automatically detect a cable with swapped MDI pairs and select the appropriate pairs for transmitting and receiving data. Normal operation is termed MDI, while crossed operation is MDIX.
100-Mb cable length estimation	The DP83630 provides a method of estimating cable length based on electrical characteristics of the 100-Mb link. This essentially provides an effective cable length rather than a measurement of the physical cable length. The cable length estimation is only available in 100-Mb mode of operation with a valid link status.

1.7 Selection of Ethernet PHY

表 3. TI Ethernet PHY

ETHERNET PHY PART NUMBER	APPLICATION
DP83848	10BASE-T and 100BASE-TX Copper Interface
DP83620	10BASE-T and 100BASE-TX and 100BASE-FX Fiber Interface
DP83630/DP83640	10BASE-T and 100BASE-TX and 100BASE-FX Fiber Interface with IEEE 1588 PTP capabilities
DP83849	Dual Port 10/100-Mbps Ethernet PHY Transceiver for use as Media Converter

1.8 TIDA-00496 Advantage

The TIDA-00496 demonstrates the following functionalities:

- 10/100-Mbps communication with copper interface using RJ45
- IEEE 802.3 100BASE-FX interface with LC-type transceiver
- DP83630 supports IEEE 1588 real-time Ethernet applications by providing hardware support for three time-critical elements.
  - IEEE 1588 synchronized clock generation
  - Packet timestamps for clock synchronization
  - Event triggering and timestamping through GPIO
  - IEEE 1588 V1 and V2 Supported
- Interface to Tiva ARM® MCU using TIDA-00226
- Onboard regulator
- Uses DP83649 for media conversion (copper to fiber) to test FO interface

This design demonstrates using TI Ethernet PHY with IEEE 1588 PTP capabilities for communication and time synchronization. This design demonstrates the communication with commonly used interfaces like copper or fiber. This design fits in a small form factor and can be further optimized based on the application configuration.

2 Key System Specifications

表 4. Key System Specifications

COMPONENT	ADDITIONAL INFORMATION
Ethernet PHY	DP83630 Ethernet PHY features: • DP83630 Precision PHYTER™ IEEE 1588 PTP Transceiver • MII or RMII: Resistor strapping options • Configurable PHY addresses: Resistor strapping options • Single register access for complete PHY status • Industrial temperature rating: –40°C to 85°C
Power supply	Single 3.3 V ± 0.3 V supply
Power supply input	Possible power input options are: • 5 V from external 2 terminal connector (not used) • 5-V DC input from MII connector and onboard regulator to generate 3.3 V (for fiber interface) • 3.3-V DC input from MII with no onboard regulator
Media interface	Copper: 10/100 Mbps Fiber: 100 Mbps
Power consumption	Ethernet PHY with copper interface: < 350 mW Ethernet PHY with fiber interface: < 350 mW Transceiver: < 1.1 W
Internal loop back	The loopback function enables MII transmit data to be routed to the MII receive data path.
MAC controller interface	50-terminal MII interface connector
Clock	The design has three options to provide clock to DP8630K: • 25-MHz crystal with internal oscillator • External oscillator to generate the clock (not populated) • Using TI's CDCE913PW and a 25-MHz crystal to generate the clock over I^2C lines (not populated)
Status LEDs	LED_ACT, LED_Link, LED_Speed
ESD	IEC61000-4-2 Level 2, Criterion B

3 Block Diagram

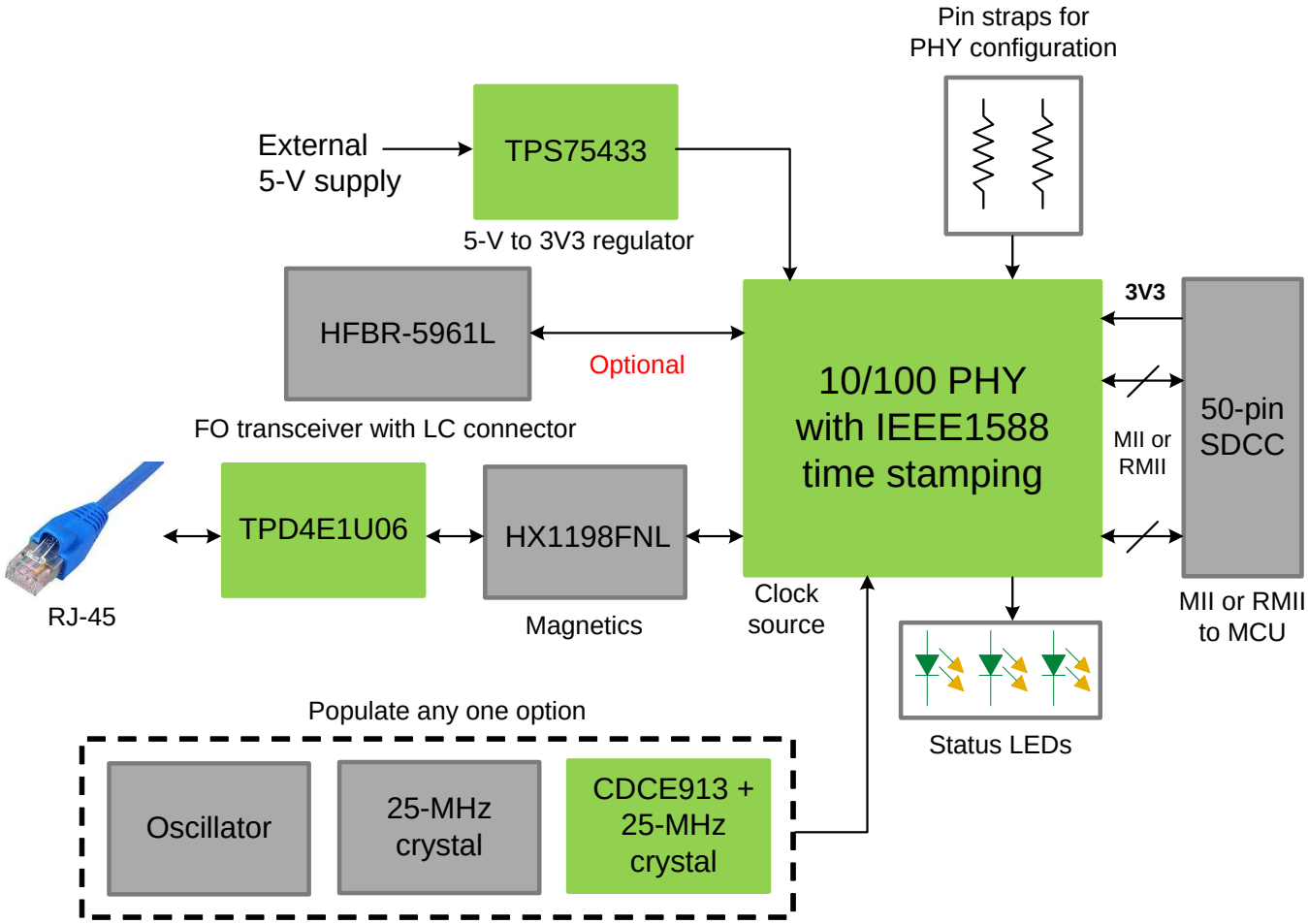


図 1. Ethernet Brick Block Diagram

3.1 Ethernet PHY — DP83630

The Ethernet PHY used in the design provides multiple functionalities:

1. Twisted Pair or FO communication Interface
2. Hardware assisted IEEE 1588 PTP

Having these functions integrated into one device enables easy migration for customers from a simple Ethernet interface to a PTP-enabled Ethernet interface.

The DP83630 Precision PHYTER™ device delivers the highest level of precision clock synchronization for real-time industrial connectivity based on the IEEE 1588 standard. The DP83630 has deterministic low latency and allows the choice of MCU with no hardware customization required. The integrated IEEE 1588 functionality allows system designers the flexibility and precision of a close to the wire timestamp. The three key IEEE 1588 features supported by the device are:

- Packet time stamps for clock synchronization
- Integrated IEEE 1588 synchronized low jitter clock generation
- Synchronized event triggering and time stamping through GPIO

The DP83630 offers innovative diagnostic features unique to Texas Instruments, including dynamic monitoring of link quality during standard operation for fault prediction. These advanced features allow the system designer to implement a fault prediction mechanism to detect and warn of deteriorating and changing link conditions. This single-port fast Ethernet transceiver can support both copper and fiber media.

表 5. Key Specifications for DP83630

PARAMETER	VALUE
Manufacturer part number	DP83630
Description	DP83630 Precision PHYTER IEEE 1588 PTP Transceiver
Type	Transceiver
Protocol	MII, RMII
Number of drivers/receivers	1/1
Supply voltage	3 to 3.6 V
Operating temperature	–40°C to 85°C

The DP83630 pins are classified into the following interface categories (each interface is described in the sections that follow):

- Serial management interface (SMI)
- MAC data interface
- Clock interface
- LED interface
- GPIO interface
- JTAG interface
- Reset and power down
- Strap options
- 10/100-Mbps PMD interface
- Power and ground pins

The major features of the Ethernet PHY are described as follows:

- MAC interface
  The DP83630 supports several modes of operation using the MII pins. The options are defined in the following sections and include:
  - MII Mode
  - RMII Mode
  - Single Clock MII Mode (SCMII)

  In addition, the DP83630 supports the standard 802.3u MII SMI.
  The modes of operation can be selected by strap options or register control. For RMII Slave mode, use the strap option because it requires a 50-MHz clock instead of the normal 25 MHz. In each of these modes, the IEEE 802.3 SMI is operational for device configuration and status. The SMI of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHYs. The current design uses MII.
- Architecture
  The Ethernet PHY supports the following communication architecture:
  - 100BASE-TX Transmitter
  - 100BASE-TX Receiver
  - 100BASE-FX Operation
  - 10BASE-T Transceiver Module
- LED interface
  The DP83630 supports three configurable LED pins:
  - LED_LINK
  - LED_SPEED/FX_SD
  - LED_ACT
- PHY address
  The five PHY address strapping pins are shared with the RXD[3:0] pins and COL pin.
  The DP83630 can be set to respond to any of 32 possible PHY addresses through strap pins. The information is latched into the PHYCR register (address 19h, bits [4:0]) at device power-up and hardware reset. Each DP83630 or port sharing an MDIO bus in a system must have a unique physical address.
  The DP83630 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined in 表 6. The functional pin name is indicated in parentheses. Use a 2.2-kΩ resistor for pulldown or pullup to change the default strap option. If the default option is required, then there is no need for external pullup or pulldown resistors. Because these pins may have alternate functions after reset is deasserted, do not directly connect them to VCC or GND.

表 6. Comparison of DP83630 and DP83640

PARAMETER	DP83630	DP83640
Function	PHY	PHY
Port count	Single	Single
Supply voltage (V)	3.3	3.3
Data rate (Mbps)	10/100	10/100

表 6. Comparison of DP83630 and DP83640 (continued)

PARAMETER	DP83630	DP83640
Special Features	IEEE 1588 PTP FX support Cable diagnostics	IEEE 1588 PTP FX support Cable diagnostics
Pin/Package	48WQFN	48LQFP

Choosing between the DP83630 and DP83640 is based on the application need as the difference is package only.

3.1.1 MII — MAC DATA INTERFACE

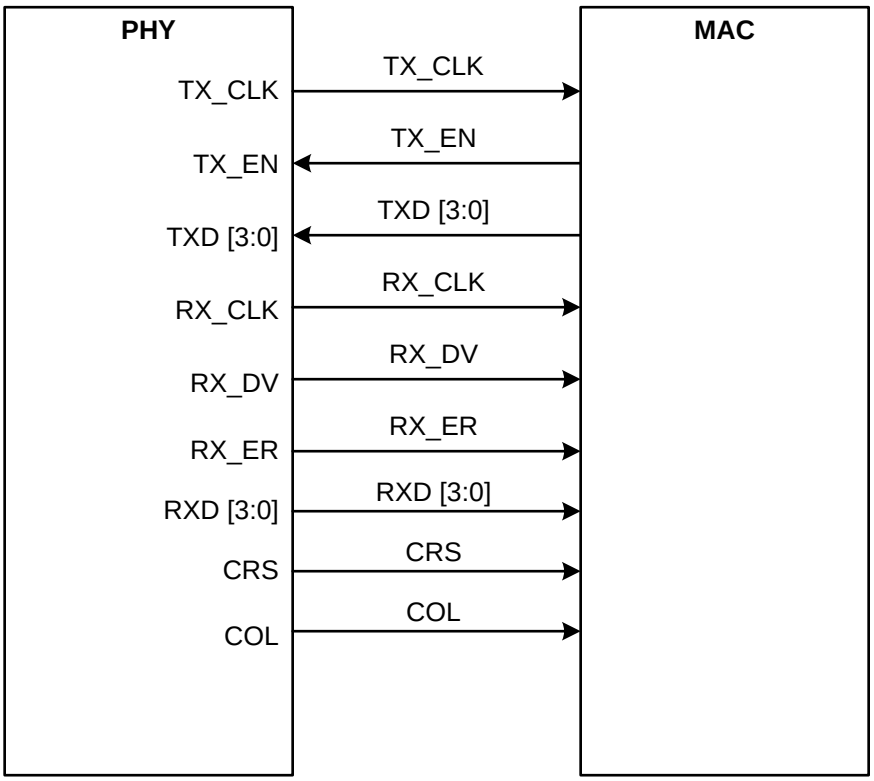


図 2. MII Signaling

The MII signals are as follows:

- MII transmit clock: 25-MHz transmit clock output in 100-Mbps mode or 2.5 MHz in 10-Mbps mode derived from the 25-MHz reference clock. The MAC should source TX_EN and TXD[3:0] using this clock
- MII transmit enable: Active high input indicates the presence of valid data inputs on TXD[3:0]
- MII transmit data: Transmit data MII input pins, TXD[3:0], that accept data synchronous to the TX_CLK (2.5 MHz in 10-Mbps mode or 25 MHz in 100-Mbps mode)
- MII receive clock: Provides the 25-MHz recovered receive clocks for 100-Mbps mode and 2.5 MHz for 10-Mbps mode
- MII receive data valid: Asserted high to indicate that valid data is present on the corresponding RXD[3:0]

- MII receive error: Asserted high synchronously to RX_CLK to indicate that an invalid symbol has been detected within a received packet in 100-Mbps mode
- MII receive data: Nibble wide receive data signals driven synchronously to the RX_CLK (25 MHz for 100-Mbps mode, 2.5 MHz for 10-Mbps mode). RXD[3:0] signals contain valid data when RX_DV is asserted
- MII carrier sense: Asserted high to indicate the receive medium is non-idle
- MII collision detect: Asserted high to indicate detection of a collision condition (simultaneous transmit and receive activity) in 10-Mbps and 100-Mbps half duplex modes

The interface to the controller is through a 50-pin high-speed connector. Male connector is mounted on the controller board and the female is on the Ethernet PHY Brick board. The connector has the MII signals and the power input (5-V or 3.3-V DC).

3.1.2 Fiber Network Interface for 100BASE-FX

The HFBR-5961L transceiver provides the system designer with a product to implement a range of solutions for multimode fiber Fast Ethernet and SONET OC-3 (SDH STM-1) physical layers for ATM and other services. This transceiver is supplied in the industry standard 2×5 DIP style with an LC fiber connector interface with an external connector shield (HFBR-5961L).

3.1.2.1 Transmitter Section

The transmitter section of the HFBR-5961L uses a 1300-nm InGaAsP LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by a custom silicon IC, which converts differential PECL logic signals, ECL referenced (shifted) to a 3.3-V supply, into an analog LED drive current.

3.1.2.2 Receiver Section

The receiver section of the HFBR-5961L uses an InGaAs PIN photodiode coupled to a custom silicon trans impedance preamplifier IC. It is packaged in the optical subassembly portion of the receiver. This pin and preamplifier combination is coupled to a custom quantizer IC, which provides the final pulse shaping for the logic output and the Signal Detect function. The Data output is differential. The Signal Detect output is single ended. Both Data and Signal Detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3-V power supply. The receiver outputs, Data Output and Data Out Bar, are squelched at the Signal Detect deassert. That is, when the light input power decreases to a typical –38 dBm or less, the Signal Detect deasserts, meaning the Signal Detect output goes to a PECL low state. This forces the receiver outputs, Data Out and Data Out Bar to go steady PECL levels high and low, respectively.

表 7. Fiber Transceiver Key Specifications

PARAMETER	VALUE
Manufacturer part number	HFBR-5961LZ
Description	TXRX MMF FE SONET OC-3 2X5
Data rate	155 MBd
Wavelength	1300 nm
Applications	Ethernet
Voltage supply	3.3 V
Connector type	LC duplex
Mounting type	Through hole

Alternative FO Transceiver modules include:

- Avago HFBR-5961ALZ
- Avago HFBR-57E5APZ
- Avago AFBR-59E4APZ

3.1.3 Twisted Pair Interface (Copper) With ESD Protection Using TPD4E1U06DCK

3.1.3.1 ESD Diodes

The ESD rating for DP83630 is 8 kV (at RZAP = 1.5 kΩ and CZAP = 120 pF). The network or Medium Dependent Interface (MDI) connection is through the transmit (TX+ and TX–) and receive (RX+ and RX–) differential pair terminals. The transmit and receive terminals connect to a termination network, then to a 1:1 magnetics (transformer), then to ESD protection devices and an RJ45 connector. This design uses the TPD4E1U06 as for ESD protection in between the RJ45 connector and the isolation transformer. The TPD4E1U06 is a quad-channel ultra-low capacitance TVS diode. It offers a ±15-KV IEC air-gap and ±15-KV contact discharge ESD protection compliant to IEC61000-4-2.

表 8. ESD Diode Key Specifications

PARAMETER	VALUE
Manufacturer part number	TPD4E1U06DCKR
Description	TVS DIODE 5.5VWM 15VC SC70-6
Unidirectional channels	4
Voltage—Reverse standoff (Typ)	5.5 V (Max)
Voltage—Breakdown (Min)	6.5 V
Voltage clamping (Max) at I_{PP}	15 V (Typ)
Current peak pulse (10/1000 µs)	3 A (8/20 µs)
Power peak pulse	45 W
Power line protection	Yes
Applications	Ethernet, HDMI
Operating temperature	–40°C to 125°C (T_A)
Mounting type	Surface mount

3.1.3.2 Isolation Transformer

This reference design uses a shielded RJ45 connector without internal isolation transformer. RJ45 is the standard cable used for all the Ethernet and LAN applications.

An external isolation transformer is interfaced. The design uses HX1198FNL (MODULE XFRMR SGL ETHR LAN 16SOIC) from Pulse Electronics. It is a 1:1 transformer with an isolation of 1.5 kV_{RMS} (for 60 seconds). Based on the application, it may be necessary to connect a common-mode choke along with the isolation transformer. HX1198FNL already has a common-mode transformer integrated into. 図 3 shows the internal schematic of HX1198FNL.

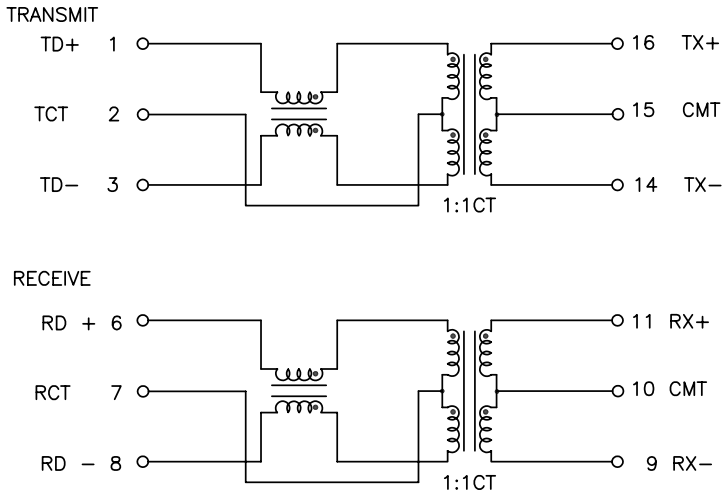


図 3. Internal Schematic of HX1198FNL

表 9. RJ45 Connector Key Specifications

PARAMETER	VALUE
Manufacturer part number	6116526-1
Description	CONN MOD JACK 8P8C R/A SHIELDED
Connector type	Jack
Number of positions/contacts	8p8c (RJ45, Ethernet)
Number of ports	1
Number of rows	1
Mounting type	Through hole
Orientation	90° angle (Right)
Termination	Solder
Shielding	Shielded
Ratings	Cat5
Features	Board guide
LED color	Does not contain LEDs
Tab direction	Down
Operating temperature	–40°C to 85°C

3.2 Host MCU With MII — TM4C129XNCZAD

The Tiva TM4C129XNCZAD is an ARM Cortex™-M4-based MCU with 1024KB flash memory, 256KB SRAM, 120-MHz operation, USB host/device/OTG, Ethernet controller, integrated Ethernet PHY, hibernation module, and a wide range of other peripherals. An internal multiplexer allows different peripheral functions to be assigned to each of these GPIO pads. When adding external circuitry, consider the additional load on the development board's power rails. The Tiva PinMux Utility can quickly develop pin assignments and the code required to configure them. The TM4C129XNCZAD MCU is factory programmed with a quick start weather display program. The quick start program resides in on-chip flash memory and runs each time power is applied, unless the application has been replaced with a user program.

- Performance
  - ARM Cortex-M4F processor core, 120-MHz operation
  - 150 DMIPS performance, 1024KB flash memory
  - 256KB single-cycle system SRAM, 6 KB of EEPROM
- Communication interfaces
  - Eight universal asynchronous receivers and transmitters (UARTs)
  - Four quad synchronous serial interface (QSSI) modules with bi-, quad-, and advanced SSI support
  - Ten I^2C modules with four transmission speeds, including a high-speed mode
  - Two controller area network (CAN) 2.0 A/B controllers
  - 10/100 Ethernet MAC
  - Ethernet PHY with IEEE 1588 PTP hardware support
  - USB 2.0 OTG/host/device with a ULPI-interface option and link power management (LPM) support
- Analog support
  - Two 12-bit analog-to-digital converter (ADC) modules, each with a maximum sample rate of one million samples per second
- Operating range (ambient)
  - Industrial (–40°C to 85°C) temperature range
  - Extended (–40°C to 105°C) temperature range
- One JTAG module with integrated ARM Serial Wire Debug (SWD)
- 212-ball BGA package

TM4C129XNCZAD supports the following Ethernet interfaces:

- 10/100-Mbps Ethernet interface with internal MAC and PHY
- 10/100-Mbps Ethernet interface with external MAC and internal PHY. The external MAC is interfaced with the MII/RMII

3.3 Fiber-to-Ethernet Media Converter — DP83489

The DP83849IF is a dual industrial temperature PHY with fiber support (FX), which does not need any software conflagration to function as a copper-to-fiber media converter.

The dual Ethernet PHY features:

- Low-power 3.3-V, 0.18-μm CMOS technology detection
- Low power consumption: < 600 mW typical
- 3.3-V MAC interface and filters
- Auto-MDIX for 10/100 Mbps
- IEEE 802.3u PCS, 100BASE-TX transceivers
- IEEE 802.3u 100BASE-FX fiber interface
- Dynamic link quality monitoring
- Flexible MII port assignment
- Integrated ANSI X3.263-compliant TP-PMD
- TDR-based cable diagnostic and cable length physical sub-layer with adaptive equalization detection and baseline wander compensation
- Optimized latency for real-time Ethernet
- Programmable LED support for link, 10/100-Mbps operation mode, activity, duplex, and collision
- Single register access for complete PHY
- SNI (configurable) status
- MII SMI (MDC and MDIO)
- 80-pin TQFP package (12×12 mm)

The DP83849IF pins are classified into the following interface (See the DP83849IF datasheet for details):

- SMI
- MAC data interface
- Clock interface
- LED interface
- JTAG interface
- Reset and power down
- Strap options
- 10/100-Mbps PMD interface
- Special connect pins
- Power and ground pins

3.4 Power Supply

The Ethernet PHY operates on a single supply. The Ethernet brick board can be powered by:

- External 5 V
- 5 V from the host board (TIDA-00226)
- 3.3 V from the host board (TIDA-00226)

The TPS75433, Single-Output LDO, 2.0-A, Fixed 3.3 V with Fast Transient Response is used when the board is configured for a fiber interface. The power supply from the host MCU board (TPS62177 28-V, 0.5-A Step-Down Converter) is used for copper interface.

3.4.1 Single-Output LDO — TPS75433

The TPS752xxQ and TPS754xxQ devices are low-dropout regulators with integrated power-on reset and power good (PG) functions respectively. These devices are capable of supplying 2 A of output current with a dropout of 210 mV (TPS75233Q, TPS75433Q). Quiescent current is 75 μA at full load and drops down to 1 μA when the device is disabled. These devices are designed to have fast transient response for larger load current changes.

The TPS754xxQ and TPS752xxQ are offered in 1.5 V, 1.8 V, 2.5 V, and 3.3 V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 to 5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS754xxQ and TPS752xxQ families are available in a 20-pin TSSOP (PWP) package.

Features:

- 2-A low-dropout voltage regulator
- Available in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed output and adjustable versions
- Open drain power-on reset with 100-ms delay (TPS752xxQ)
- Open drain PG status output (TPS754xxQ)
- Dropout voltage typically 210 mV at 2 A (TPS75233Q)
- Ultralow 75-μA typical quiescent current
- Fast transient response
- 2% tolerance over specified conditions for fixed-output versions
- 20-pin TSSOP PowerPAD™ (PWP) package
- Thermal shutdown protection

4 Ethernet Brick Design Theory

4.1 Ethernet PHY

4.1.1 PHY Interface

図 4 shows the DP83630 Brick configured for 10/100-Mbps communication using MII. A 25-MHz crystal (default) oscillator is connected. There are other clock options provided. The DP83630 package is WQFN. Alternatively, the DP83640, which is LQFP, can be used.

The PHY has general purpose I/Os (GPIOs) with the following functionality:

- GPIO 3,4,8,9: These pins may be used to signal or detect events.
- GPIO1: CLK_OUT OUTPUT ENABLE: When high, enables clock output on the CLK_OUT pin at power-up
- GPIO2 : PHY CONTROL FRAME ENABLE: When high, allows the DP83630 to respond to PHY Control Frames

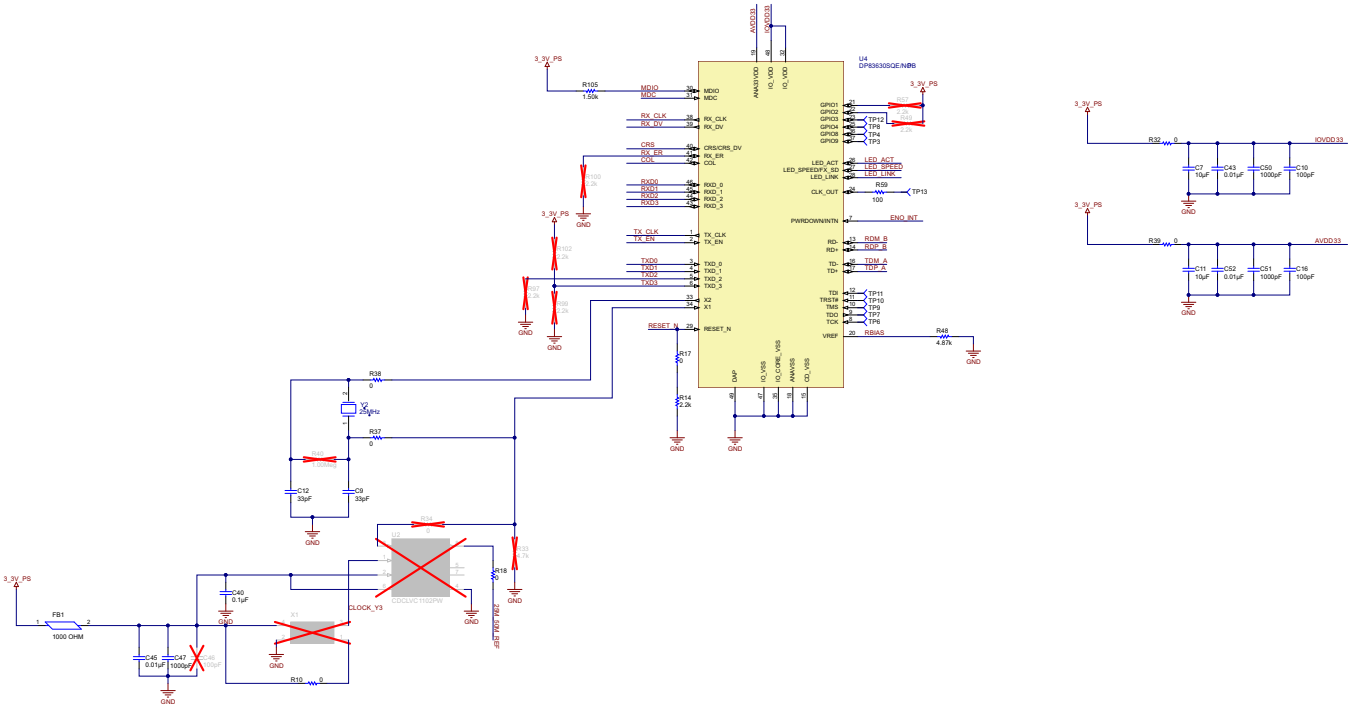


図 4. DP83630 PHY

注: 図 4 is configured for copper. When fiber interface is required, R100 is populated.

4.1.2 PHY Bootstrap Configuration

For a copper interface, the brick has been configured as shown in 表 10:

表 10. Interface Selection

PIN NAME	FUNCTIONALITY	CONFIGURATION
RX_DV	MII Mode	PD
RX_ER	FX ENABLE	PU—Copper PD—Fiber

The PHY ID programmed is 7 as shown in 表 11:

表 11. PHY ID Configuration

PIN NAME	FUNCTIONALITY	CONFIGURATION
PHYAD0	COL	PU
PHYAD1	RXD_3	PU
PHYAD2	RXD_2	PU
PHYAD3	RXD_1	PD
PHYAD4	RXD_0	PD

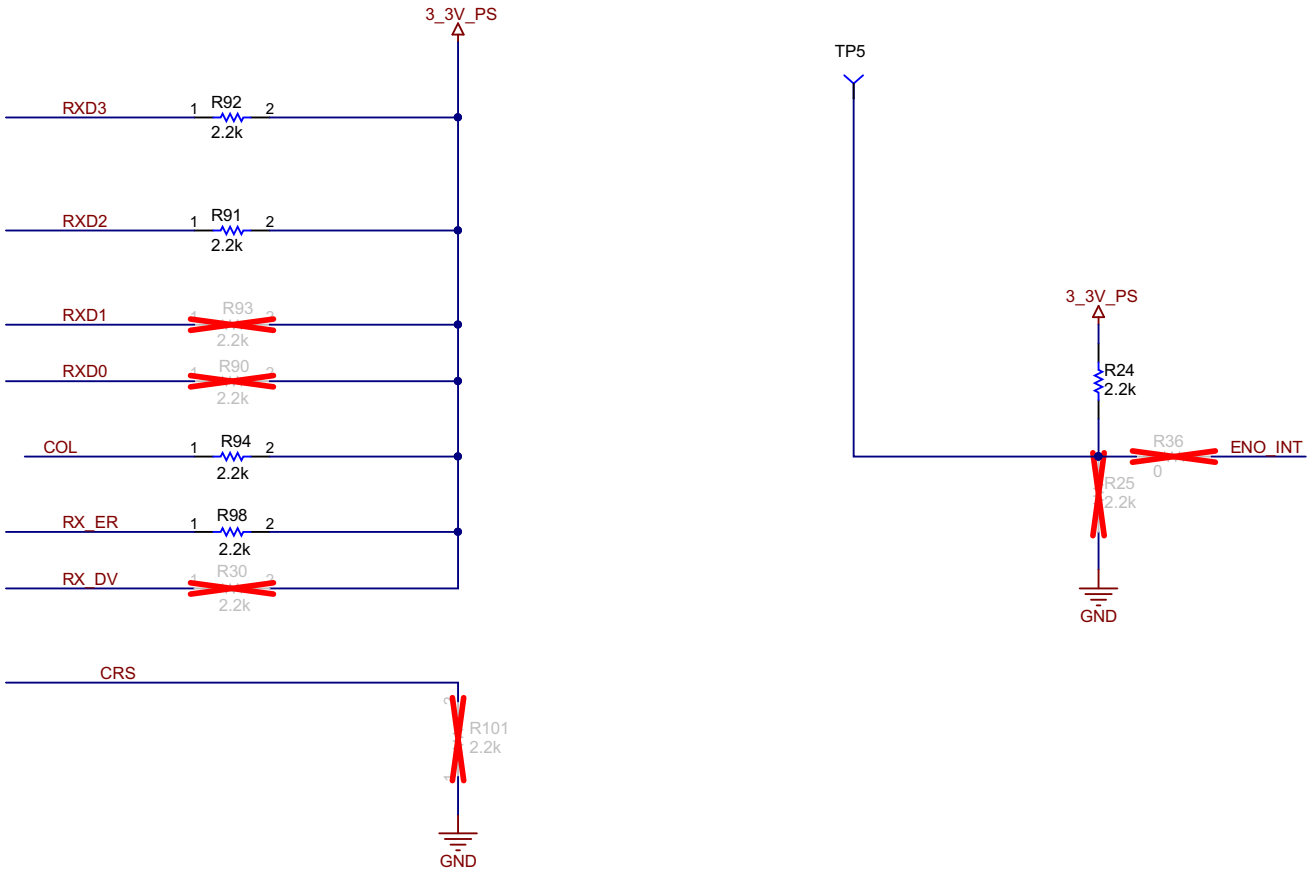


図 5. Pin Strap Options

注: R98 is not populated for a fiber configuration.

4.1.3 LEDs

The DP83630 supports three configurable LED pins: LED_LINK, LED_SPEED/FX_SD, and LED_ACT. The LEDs support two operational modes, which are selected by the LED mode strap. Because these LED pins are also used as strap options, the polarity of the LED is dependent on whether the pin is pulled up or down.

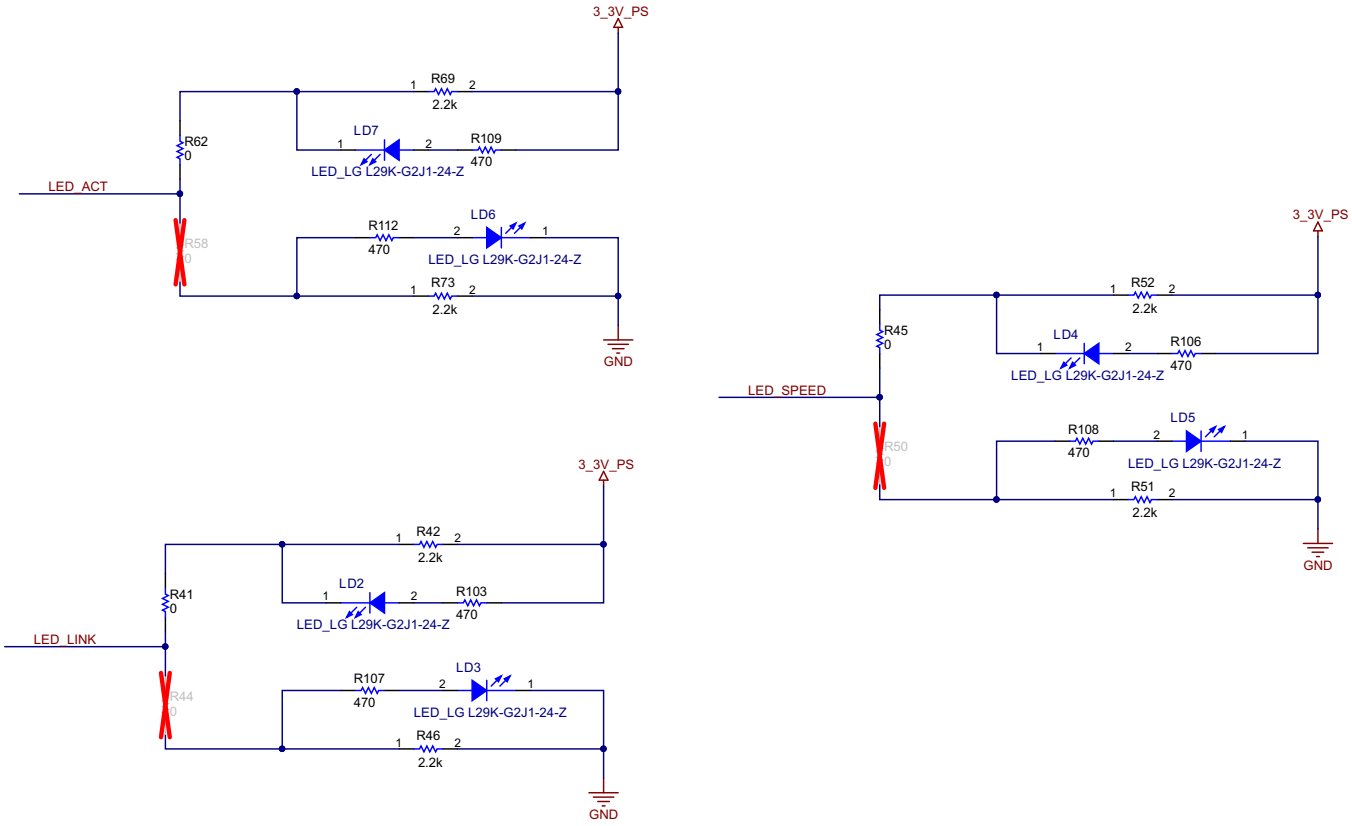


図 6. LED Configuration

注: R45 is not populated for a fiber option.

4.1.4 Cable Specifications

The specifications in 表 12 are for the FO cable that is used to test the communication with a media converter.

表 12. FO Cable Specifications

PARAMETER	VALUE
Manufacturer part number	DK-2632-02
Description	Cable fiber optic dual LC-SC 2M
First connector	LC duplex
Second connector	SC duplex
Cable diameter	0.12" (3.0 mm)
Cable type	Buffered fiber
Fiber type	62.5/125
Length (overall)	6.56' (2.0 m)
Type	Multimode, duplex
Color (cable)	Orange
Color (connectors)	Black, red

4.1.5 Twisted Pair Interface

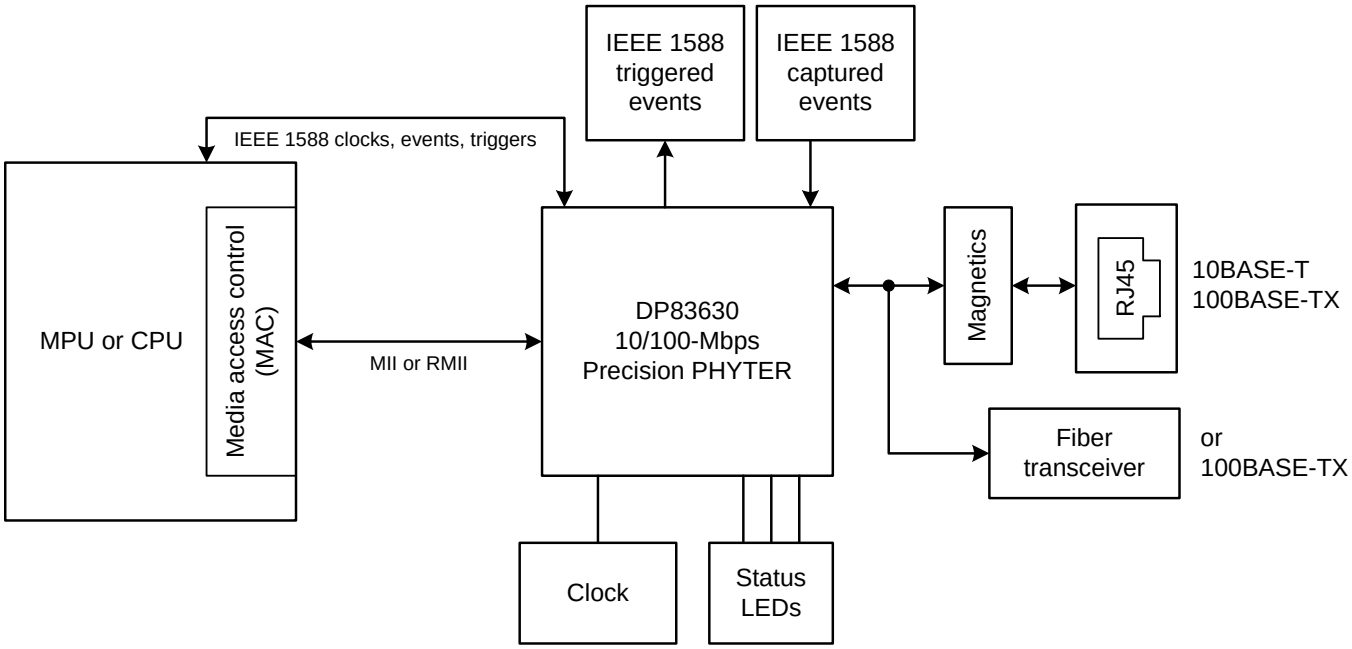


図 7. DP83630 Functional Diagram

The DP83630 supports both twister pair (100BASE-TX and 10BASE-T) and Fiber (100BASE-FX) media. The port may be configured for twisted pair (TP) or fiber (FX) operation by strap option or by register access. At power-up or reset, the state of the RX_ER pin will select the media for the port. The default selection is twisted pair mode, while an external pulldown will select FX mode of operation.

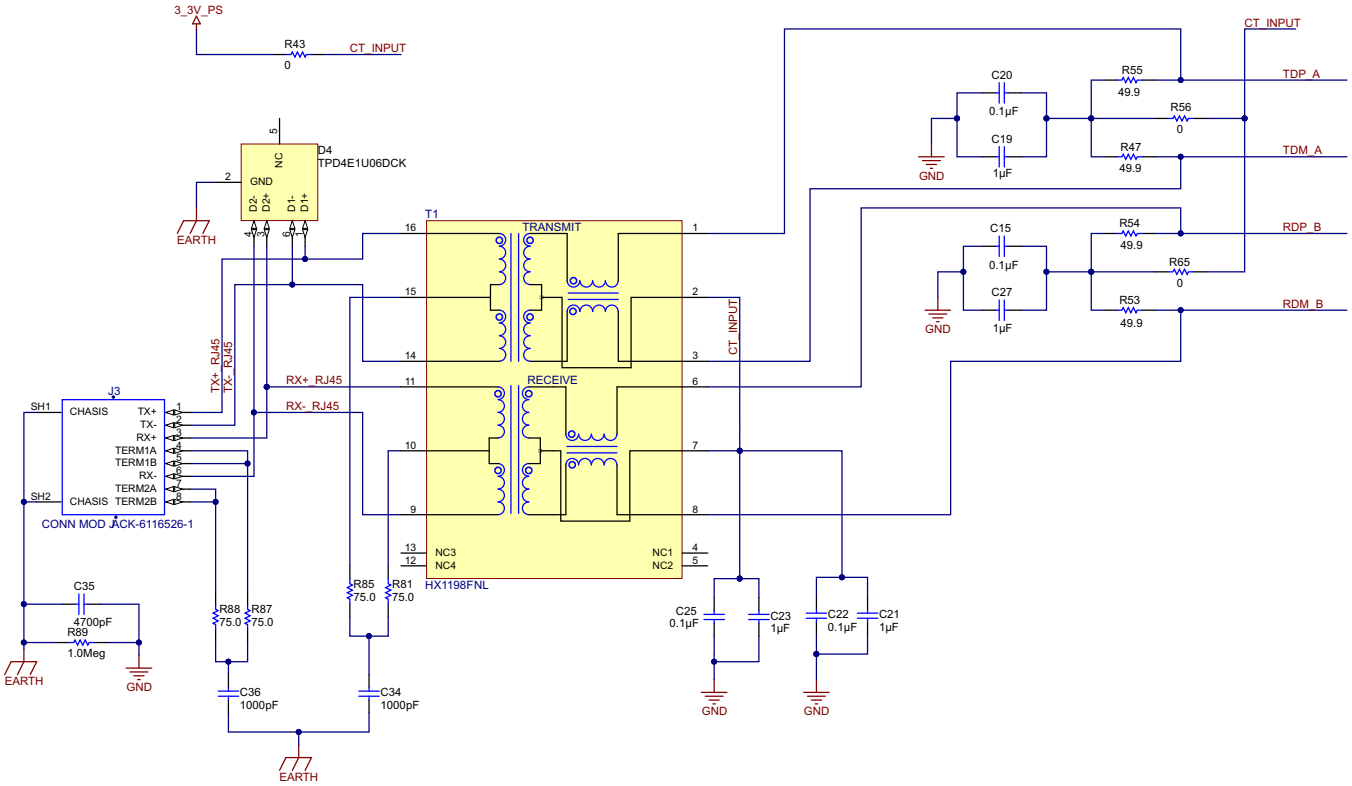


図 8. Twisted Pair (Copper) Interface for DP83630 PHY

注: The TVS diode array for ESD protection is provided across the RJ45 connector. In some of the applications based on testing, the TVS diode array is moved after the isolation transformer. This change needs to be verified for surge, ESD, and other EMC tests before implementing.

4.1.6 Fiber Interface

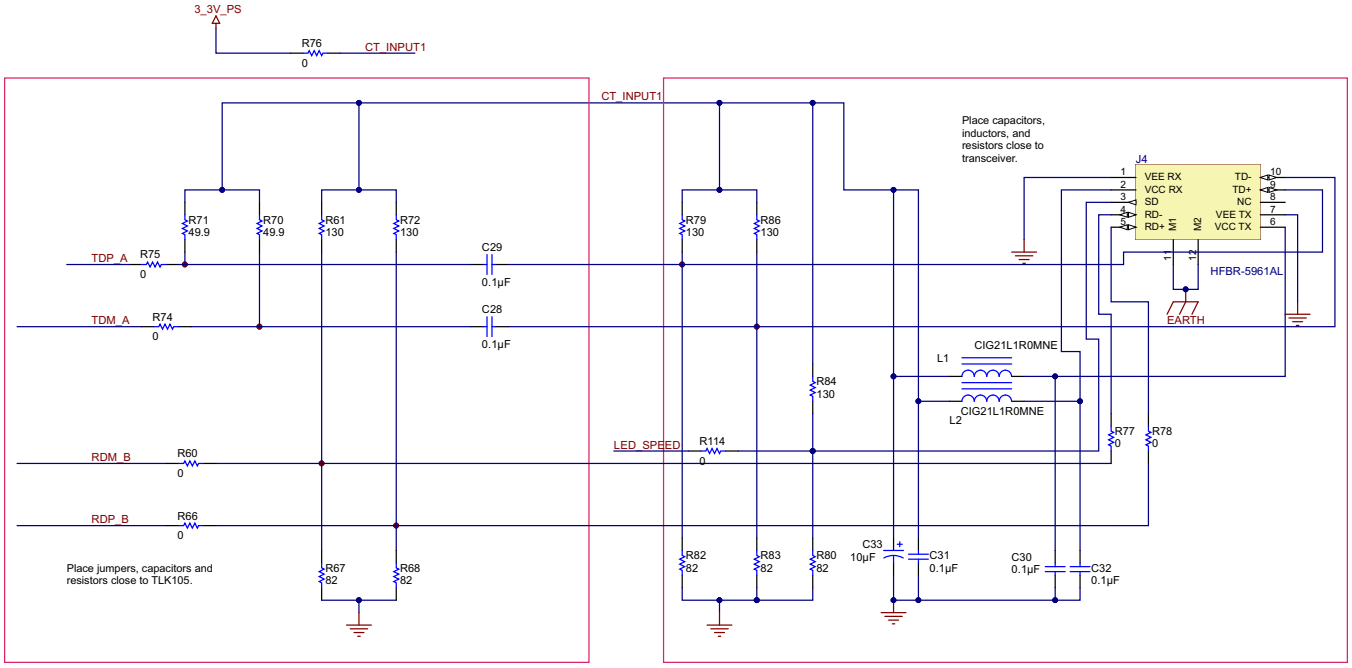


図 9. FO Interface for DP83630 PHY

The HFBR-5961L transceiver datasheet from Avago Technologies provides recommended decoupling and termination circuits and also alternative termination circuits. The design uses these recommended circuit and the TI EVM circuit. Any of these configuration can be populated.

4.1.7 MII to Host

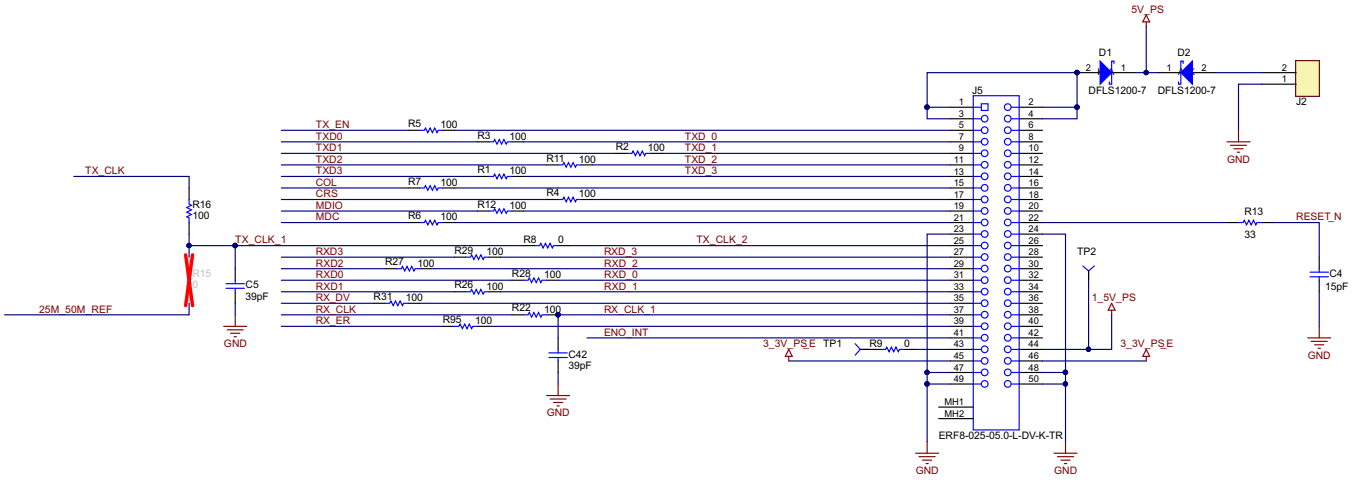


図 10. Interface Connector to Host MCU

The MII signals have been provided with 100R termination. Additionally, many of the MII signals have 50R internal termination. These terminations have been provided for improving EMI performance (radiated emission). The use of only internal termination or a combination of Internal and external termination can be optimized based on performance and EMI testing.

4.1.8 Host MCU Interface

The 32-bit ARM Cortex-M4F MCU-Based Small Form Factor Serial-to-Ethernet Converter TI Design has been used as the host to test Ethernet communication interface. Find more information is available at the TIDA-00226 product page.

IEEE 1588 Stack for Testing PTP Time Stamping Functionality

PTP daemon (PTPd) implements the PTP as defined by "IEEE Std 1588-2002" (also known as PTP version 1). PTPd can coordinate the clocks of a group of LAN connected computers with each other. Check with TI Industrial to get the updated files for PTP implementation and make the following changes:

1. Download and install latest TivaWare™. Example path at the default location:
   C:\ti\TivaWare_C_Series-2.1.0.12573\third_party
2. Add the *third_party* > *fatfs, third_party* > *lwip-1.4.1*, *third_party* > *ptpd-1.1.0*, and the sub-directories to project Include path.
3. Replace the following files in *third_party* > *lwip-1.4.1* with the ones from the downloaded TIDA-00496 project:
   lwip-1.4.1\ports\tiva-tm4c129\include\netif\tivaif.h
   lwip-1.4.1\ports\tiva-tm4c129\netif\tiva-tm4c129.c
   lwip-1.4.1\ports\tiva-tm4c129\sys_arch.c
   lwip-1.4.1\src\core\ipv4\ip.c
4. Replace the following files in *third_party* > *ptpd-1.1.0* with the ones from the downloaded TIDA-00496 project:
   ptpd-1.1.0\src\dep\datatypes_dep.h
   ptpd-1.1.0\src\dep\msg.c
   ptpd-1.1.0\src\dep\net.c
   ptpd-1.1.0\src\dep-tiva\ptpd_msg.c
   ptpd-1.1.0\src\dep-tiva\ptpd_net.c
   ptpd-1.1.0\src\dep-tiva\ptpd_servo.c
   ptpd-1.1.0\src\arith.c
   ptpd-1.1.0\src\datatypes.h
   ptpd-1.1.0\src\probe.c

ptpd-1.1.0\src\protocol.c

4.2 Power Supply

The Ethernet PHY operates on a single supply. The Ethernet PHY brick board can be powered by:

- External 5 V
- 5 V from the host board (TIDA-00226)
- 3.3 V from the host board (TIDA-00226)

The TPS75433, Single Output LDO, 2.0-A, Fixed 3.3 V with Fast Transient Response is used when the board is configured for fiber interface. The power supply from the host MCU board (TPS62177 28-V, 0.5-A Step-Down Converter) is used for the copper interface.

A 2-A LDO has been provided on the board. When the board is tested for copper interface the DC-DC converter on the serial-to-Ethernet converter can power the brick and so the onboard LDO output is disabled by depopulating R63. When the communication interface is tested with fiber, the current requirement is more; to source, the required current onboard LDO is used. Populate R63 to use the onboard LDO.

The output current capacity of the regulator is 2 A. This can be used to power any other application that has a 3.3-V power supply.

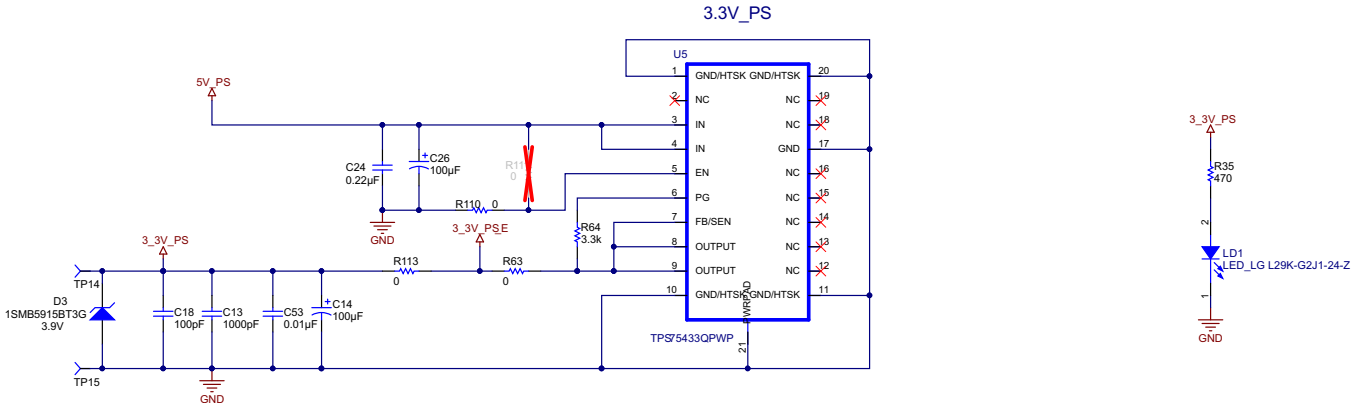


図 11. Regulator for PHY and FO Transceivers

4.3 Design Configuration for Twisted Pair (Copper) and Fiber Interface

The Ethernet brick provides board configurations for the following functionalities:

- Twisted pair (copper) interface
- Fiber interface

To make the design easy to use, two sets of design files have been provided: One for a copper interface and the other for a fiber interface. The design is the same except that the DNI components applicable for copper and fiber have been clearly identified. The functionality for copper or fiber can be tested with same PCB by assembling components as per respective BOM.

4.4 Design Guidelines

4.4.1 Reducing Radiated Emissions in 10/100-Mbps Ethernet LAN Applications

PHYTER products are designed to limit EMI in system implementations in three ways:

1. Analog and digital power distribution systems are intentionally partitioned, both externally and within the component, to reduce cross functional noise that can result in EMI.
2. Key analog blocks within the component are designed and tested to meet specific ground and power supply noise rejection targets, further reducing the effects of cross functional noise.
3. In some PHYTER products, including DP83849 and DP83630/DP83640 products, integrated series terminations are provided on digital signal drivers, reducing I/O related EMI.

In addition to these designed in advantages, key recommendations for designing reduced EMI applications include:

- Use high quality CAT5E or better cable in implementing network systems. If possible use shielded cable.
- Use shielded network connectors connected to a decoupled chassis ground plane.
- Use equal length differential MDI signal traces with a strip line impedance of 50 Ω.
- Carefully match the values and placement of MDI termination components.
- Use a common mode choke component in conjunction with the isolation transformer.
- Place local bypass components (including capacitors and optionally ferromagnetic beads) between device supply pins and power sourcing vias on PCBs.
- Reduce the energy of digital signal sources by including series termination resistors in signal paths (series resistors on all MII signals).

4.4.2 Clock IN (X1) Recommendations

The DP83630 supports an external CMOS level oscillator source or a crystal resonator device.

- Oscillator
  If an external clock source is used, X1 should be tied to the clock source and X2 should be left floating. For RMII Slave Mode, the 50-MHz oscillator is used.
- Crystal
  A 25-MHz, parallel, 20-pF load crystal resonator should be used if a crystal source is desired. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads. The oscillator circuit is designed to drive a parallel resonance AT cut crystal with a minimum drive level of 100 μW and a maximum of 500 μW. If a crystal is specified for a lower drive level, a current limiting resistor should be placed in series between X2 and the crystal.

5 Firmware

5.1 Ethernet Brick Configuration

表 13. PHY Functionality Configuration

FUNCTIONALITY	DESCRIPTION
Hardware reset	A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 μs, to RESET_N. This pulse resets the device such that all registers are reinitialized to default values, and the hardware configuration values are re-latched into the device (similar to the power-up/reset operation). The time from the point when the reset terminal is de-asserted to the point when the reset has concluded internally is approximately 200 μs.
External MII PHY rnitialization	Set the external PHY address. (All the read and write requests to the PHY shall use the configured external PHY address). To reset the MII PHY: • Set the BMCR (0x00) register bit 15 to one. • Set the BMCR (0x00) register to auto negotiation enable and auto negotiation restart by setting bit 12 and bit 8 to one. • Poll the BMSR (0x01) register bit 5 to check if autonegotiation is complete.
MII_MODE	The MII_MODE is selected by pin 32 (RX_DV). This terminal has internal weak pull down defaults to MII mode. An external pull-up makes the PHY to operate in RMII mode.
PHY ID	PHY ADDRESS [4:0]: The DP83630 provides five PHY address pins, the state of which is latched into the PHYCTRL register at system Hardware-Reset. The DP83630 supports PHY Address strapping values 0 (<00000>) through 31 (<11111>). Pin names are COL, RXD_3, RXD_2, RXD_1, RXD_0. A 2.2-kΩ resistor should be used for pull-down or pull-up to change the default strap option. If the default option is required, then there is no need for external pull-up or pull down resistors. Since these pins may have alternate functions after reset is deasserted, they should not be connected directly to VCC or GND.
LED configuration	The DP83630 supports three configurable LED pins. LED_LINK, LED_SPEED, LED_ACT are the supported LED functionalities. The LEDs support two operational modes, which are selected by the LED mode strap, and a third operational mode that is register configurable.
TPI/fiber interface	FX ENABLE: This strapping option enables 100BASE-FX (fiber) mode. This mode is disabled by default. An external pulldown will enable 100BASE-FX mode.

注: When fiber mode is enabled through strap, the other configuration (auto-negotiation disabled, SD option, LED configuration) occurs automatically. Note that the external strap resistors are only sampled upon power up or upon a reset via the RESET_N pin.

If the fiber is configured via register access, write PHYCR2[9], SOFT_RESET, after enabling or disabling fiber mode through register access to ensure correct configuration.

5.2 DP83630 Precision PHYTER Control Registers

表 14. PHY Control Registers Including PTP Registers Configuration

COMMANDS (FUNCTIONALITY)	DESCRIPTION		
	FIELD	BIT LOCATION	DESCRIPTION
Command format of MDIO	Command type	31:30	Set to 01 for write Set to 10 for read
	PHY address	29:25	Set to PHY address or to 0x1F (broadcast)
	Page select	24:21	Register page select
	Register address	20:16	Register address
	Write data	15:0	Write data
Reset PHY	Select PTP 1588 CONFIGURATION REGISTERS page4 by writing the value 0x0000 to PAGESEL (Page Select Register). To reset PHY write the value 0x8000 to the BMCR register.		

表 14. PHY Control Registers Including PTP Registers Configuration (continued)

COMMANDS (FUNCTIONALITY)	DESCRIPTION
Enable PTP	Select PTP 1588 CONFIGURATION REGISTERS page4 by writing the value 0x0004 to PAGESEL (Page Select Register) Enable the PTP_ENABLE (bit2) in the PTP_CTL register.
Disable PTP	Select PTP 1588 CONFIGURATION REGISTERS page4 by writing the value 0x0004 to PAGESEL (Page Select Register). Enable PTP_DISABLE (bit1) in PTP_CTL register.
Reset PTP	Select PTP 1588 CONFIGURATION REGISTERS page4 by writing the value 0x0004 to PAGESEL (Page Select Register). Set bit0 in PTP_CTL register. Clear bit0 in PTP_CTL register.
Set time	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Write clock time NS [15:0] to PTP_TDR. Write clock time NS [29:16] to PTP_TDR (30 bit of ns). Write clock time Seconds [15:0] to PTP_TDR. Write clock time Seconds [31:16] to PTP_TDR. Write to PTP_CTL register with PTP_Load_Clk (bit4) set.
Read time	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Write to PTP_CTL register with PTP_Rd_Clk (bit5) set. Read clock time NS [15:0] from PTP_TDR. Read clock time NS [29:16] from PTP_TDR (30 bit of ns). Read clock time Seconds [15:0] from PTP_TDR. Read clock time Seconds [31:16] from PTP_TDR.
Configure transmit timestamp	Select PTP 1588 CONFIGURATION REGISTERS page 5 by writing to PAGESEL (Page Select Register). Enable TX_L2_EN, TX_IPV4_EN (bits 5, 7) in the PTP_TXCFG0 register to enable layer2 timestamp and IPv4 timestamp, respectively. Set TX_PTP_VER ie bits [4:1] to 1 in PTP_TXCFG0 register to select PTP version1 (or) 2 for PTP version 2. Enable TX_TS_EN (bit0) to enable transmit timestamp.
Check transmit timestamp available	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Check TXTS_RDY (bit11) is set in PTP_STS register.
Read transmit timestamp for configured PTP packets	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Read clock time NS [15:0] from PTP_TXTS. Read clock time NS [29:16] from PTP_ TXTS, bits [31:30] represent overflow. Read clock time Seconds [15:0] from PTP_TXTS. Read clock time Seconds [31:16] from PTP_TXT.
Configure receive timestamp	Select PTP 1588 CONFIGURATION REGISTERS page 5 by writing to PAGESEL (Page Select Register). Enable RX_L2_EN, RX_IPV4_EN (bits 5,7) in RXCFG0 register to enable layer2 and IPv4 packets, respectively. Set PTP version in [4:1] bits in RXCFG0 register to 1 for PTP v1 and 2 for PTP v2. Enable RX_TS_EN (bit 0) for receive timestamp enable. Select PTP domain to zero using [7:0] bits in RXCFG3 register.
Check receive timestamp available	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Check RXTS_RDY (bit 10) is set in PTP_STS register.
Read receive timestamp for configured PTP packets	Select PTP 1588 CONFIGURATION REGISTERS page 4 by writing to PAGESEL (Page Select Register). Read clock time NS [15:0] from PTP_RXTS. Read clock time NS [29:16] from PTP_ RXTS, bits [31:30] represent overflow. Read clock time Seconds [15:0] from PTP_RXTS. Read clock time Seconds [31:16] from PTP_RXTS.
Step correction using add or subtract time	Write Clock_time_ns[15:0] to PTP_TDR. Write Clock_time_ns[31:16] to PTP_TDR. Write Clock_time_sec[15:0] to PTP_TDR. Write Clock_time_sec[31:16] to PTP_TDR. Write to PTP_CTL with the PTP_Step_Clk (bit3) set.

表 14. PHY Control Registers Including PTP Registers Configuration (continued)

COMMANDS (FUNCTIONALITY)	DESCRIPTION
Rate correction (frequency scaling)	Write Temp_Rate[25:16] to PTP Rate High Register (PTP_RATEH) with PTP_TMP_RATE (bit14) set to 0. The clock rate direction can be increased or decreased. Set bit 15 to decrease the clock frequency and clear bit 15 to increase the clock frequency. Write Temp_Rate[15:0] to PTP Rate Low Register (PTP_RATEL). For example: When PTP_RATEH = 0 and PTP_RATEL = 1, the adjustment is 8 ns. When PTP_RATEH = 0x0400 and PTP_RATEL = 0x0000, the adjustment is 0.536 seconds over configured time period SYNC interval (typically one second).
Temporary oscillator speed correction	Write Temp_Rate_duration[25:16] to PTP Temporary Rate Duration High Register(PTP_TRDH). Write Temp_Rate_duration[15:0] to PTP Temporary Rate Duration Low Register (PTP_TRDL). Write Temp_Rate[25:16] to PTP Rate High Register (PTP_RATEH) with PTP_TMP_RATE bit set to 1. Write Temp_Rate[15:0] to PTP Rate Low Register (PTP_RATEL). Once the preconfigured temporary time period elapses, the clock rate will revert to normal.
Enable clock output	Select PTP 1588 CONFIGURATION REGISTERS page 0 by writing to PAGESEL register. Set PHYCR2[1] to 1. Select PTP 1588 CONFIGURATION REGISTERS page 6 by writing to PAGESEL register. Write the desired configuration to EPHY_PTP_COC.
Disable clock output	Select PTP 1588 CONFIGURATION REGISTERS page 0 by writing to PAGESEL (Page Select Register). Make PHYCR2 [1] to 0.
Enable fiber mode	Select PTP 1588 CONFIGURATION REGISTERS page 0 by writing to PAGESEL (Page Select Register). Set EPHY_PTP_PCSR [6] to 1.

6 Test Setup

6.1 Test Setup Block Diagram

6.1.1 Twisted Pair (Copper) Interface

The RJ45 interface is the most common interface on ethernet enabled systems. The copper interface can be directly tested using a computer or IEEE 1588 master. No media converters are required.

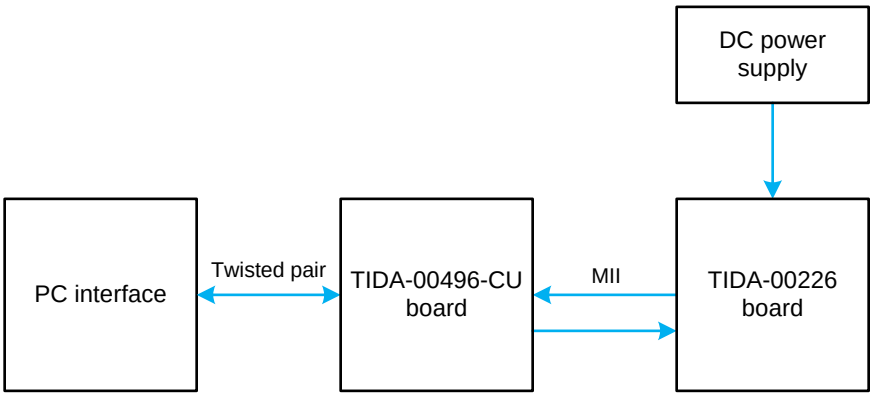


図 12. Ethernet Interface Testing With Twisted Pair Interface

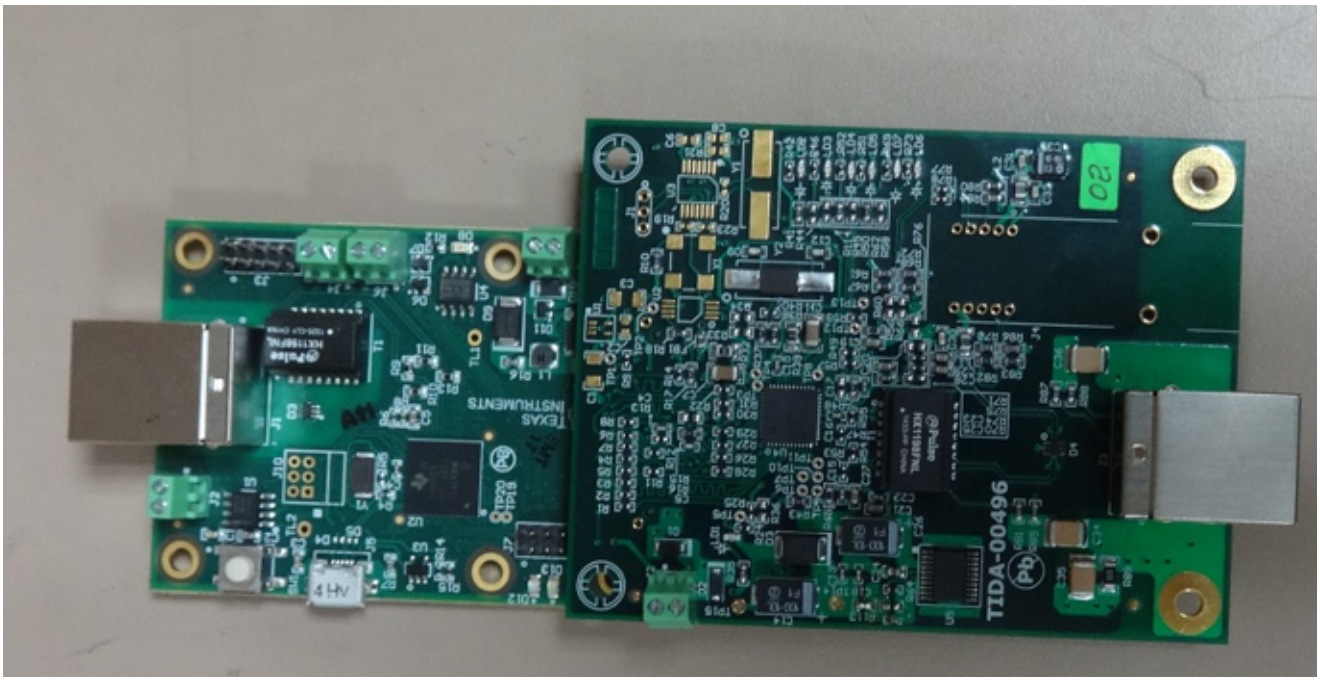


図 13. Twisted Pair Board Connection for Testing

6.1.2 Fiber Interface

The simplest way to test the FO interface is to use a media converter (TIDA-00306).

The media converter has an SC-type FO transceiver and the TIDA-00496 has an LC-type FO transceiver. The design uses an FO cable with an LC-type connector on one side and an SC type connector on the other side to connect the two boards.

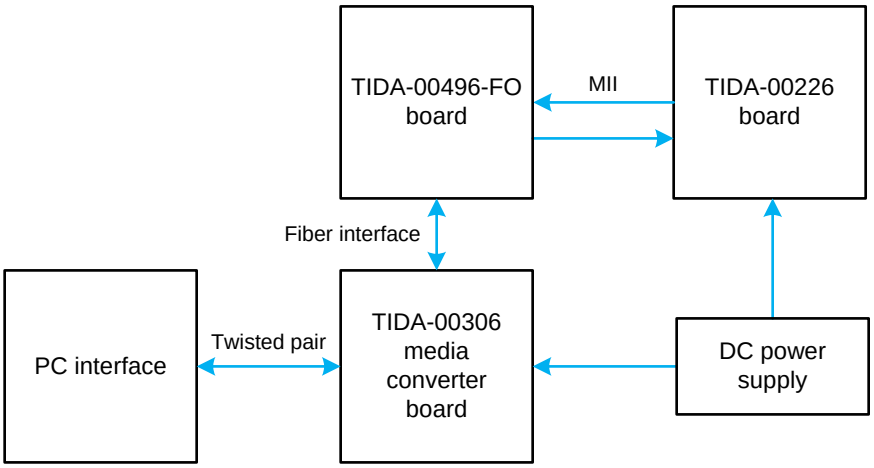


図 14. Ethernet Interface Testing With Fiber Interface

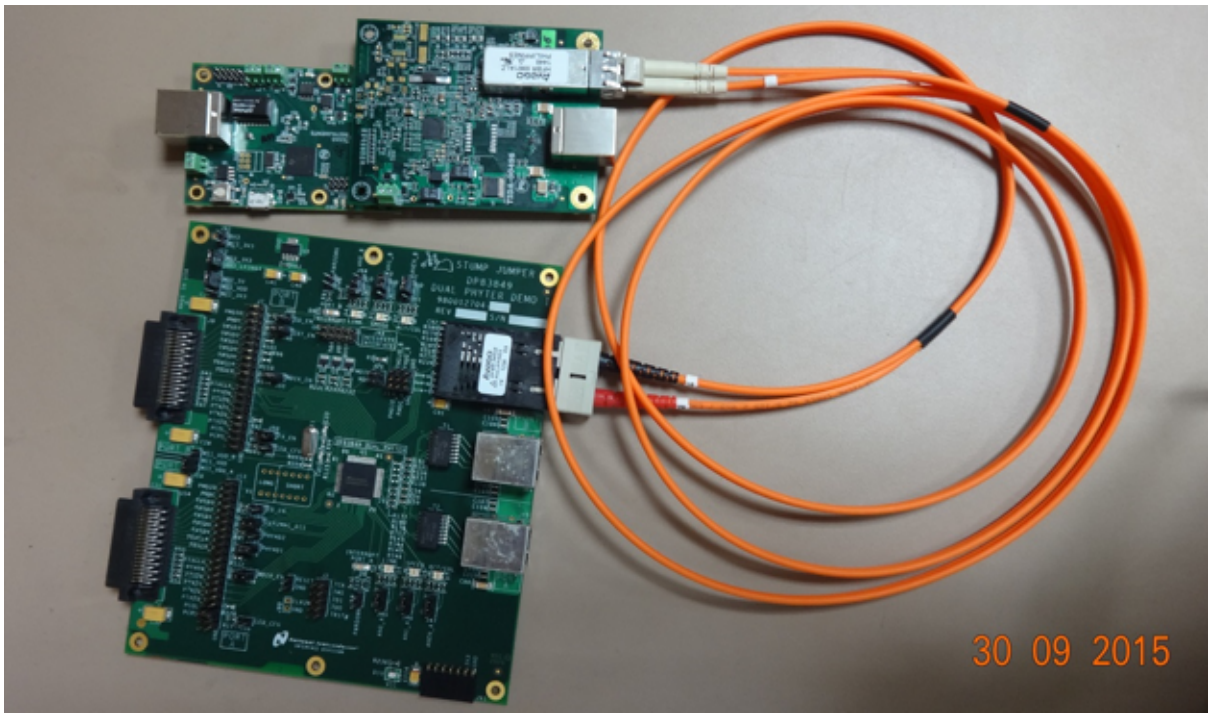


図 15. FO Board Connection for Testing

6.1.3 IEEE 1588 PTP Time Synchronization Performance Setup

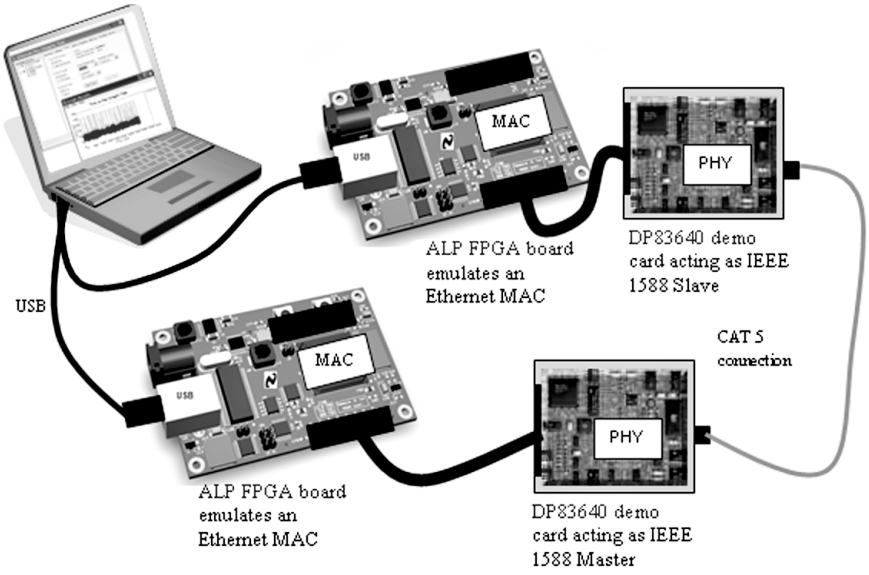


図 16. Software Synchronization Test Setup

6.1.4 PPS Output and Clock Output Synchronization Test Setup

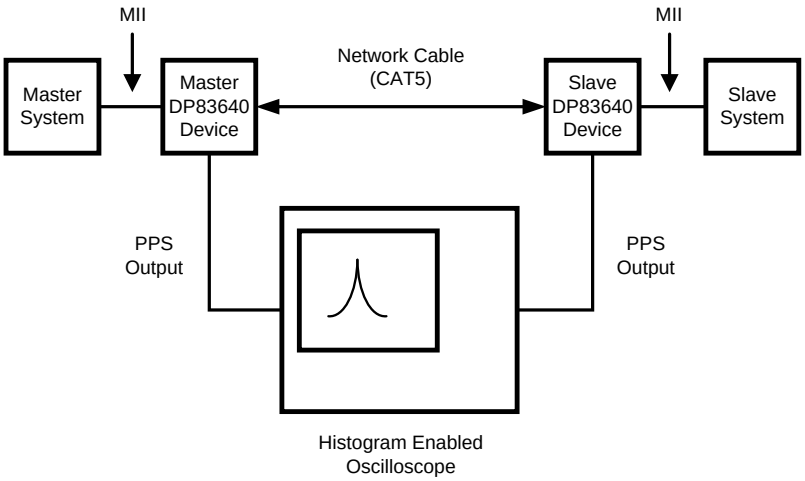


図 17. Output Synch Test Setup

7 Test Data

7.1 Functional Testing

表 15. 7.1 Design Parameters Test Summary

PARAMETERS	OBSERVATION
Clock	25 MHz
Analog supply voltage (V_{CC}) and I/O supply voltage ($V_{I/O}$): 1. (3 to 3.6 V) with external LDO for copper mode 2. VCC (3 to 3.6 V) with onboard LDO for fiber mode	3.31-V DC 3.29-V DC
MII with the PHY connected to Host MCU using 50-pin connector	OK
Status LEDs (copper) LED_LINK LED_SPEED LED_ACT	OK
Status LEDs (FO) LED_LINK LED_ACT (LED_Speed is configured as FX_SD)	OK
Power consumption board including PHY	~350 mW
FO receiver	~0.225 W
FO transmitter	~0.44 W

7.2 Ethernet 10/100-Mbps Communication Testing

表 16. Communication Testing

TEST	OBSERVATION
10/100-Mbps communication with twisted pair RJ45	The following functions were tested: 1. Ping test for communication errors 2. LED functionality for • LED_LINK • LED_SPEED • LED_ACT
100-Mbps fiber pair interface	The following functions were tested: 1. Ping test for communication errors 2. LED functionality for • LED_LINK • LED_ACT

7.2.1 Testing Multiple Boards

表 17. Communication Test With Copper

BOARD NUMBER	COMMUNICATION
Board 1	No failures observed
Board 2	No failures observed
Board 3	No failures observed
Board 4	No failures observed

表 18. Communication Test With Fiber

BOARD NUMBER	COMMUNICATION
Board 1	No failures observed
Board 2	No failures observed

7.2.2 Communication Interface Testing (Computer to Device [Brick]) — Ping Test

The setup for copper and fiber connection is made as per 6.

Network connection settings for ping test are:

1. Go to *Network Connections.*
2. Go to *Local Area Connection.*
3. Right click for *Properties.*
4. Select "Internet Protocol Version 4 (TCP/IPv4)".
5. Go to *Properties.*
6. Select "Use the following IP Address".
7. Enter the IP Address = 192.16.0.100 and click on Subnet Mask (It should show 255.255.255.0).
8. Click *OK.*
9. Click *Close.*

Go to *Start* → *Run* → Type "cmd" → Type "ping 192.16.0.1" and press *Enter*. It will show the following window and show four replies (図 18).

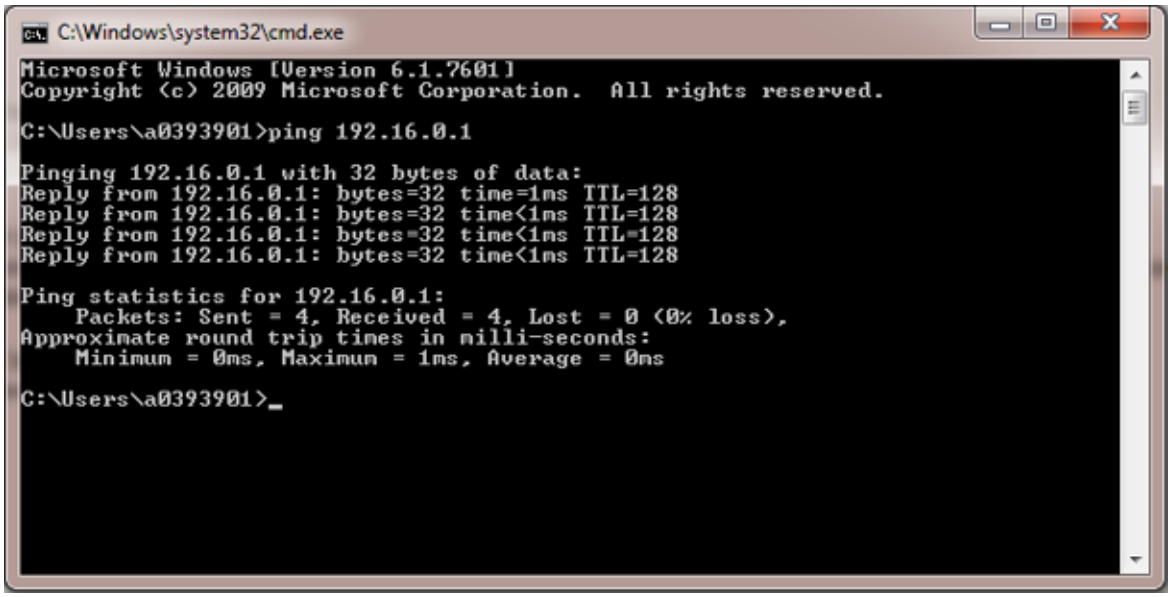


図 18. Ping Test

For continued replies, type "ping 192.16.0.1 –t" and press *Enter*. It will show the following window and show continuous replies for the ping (図 19).

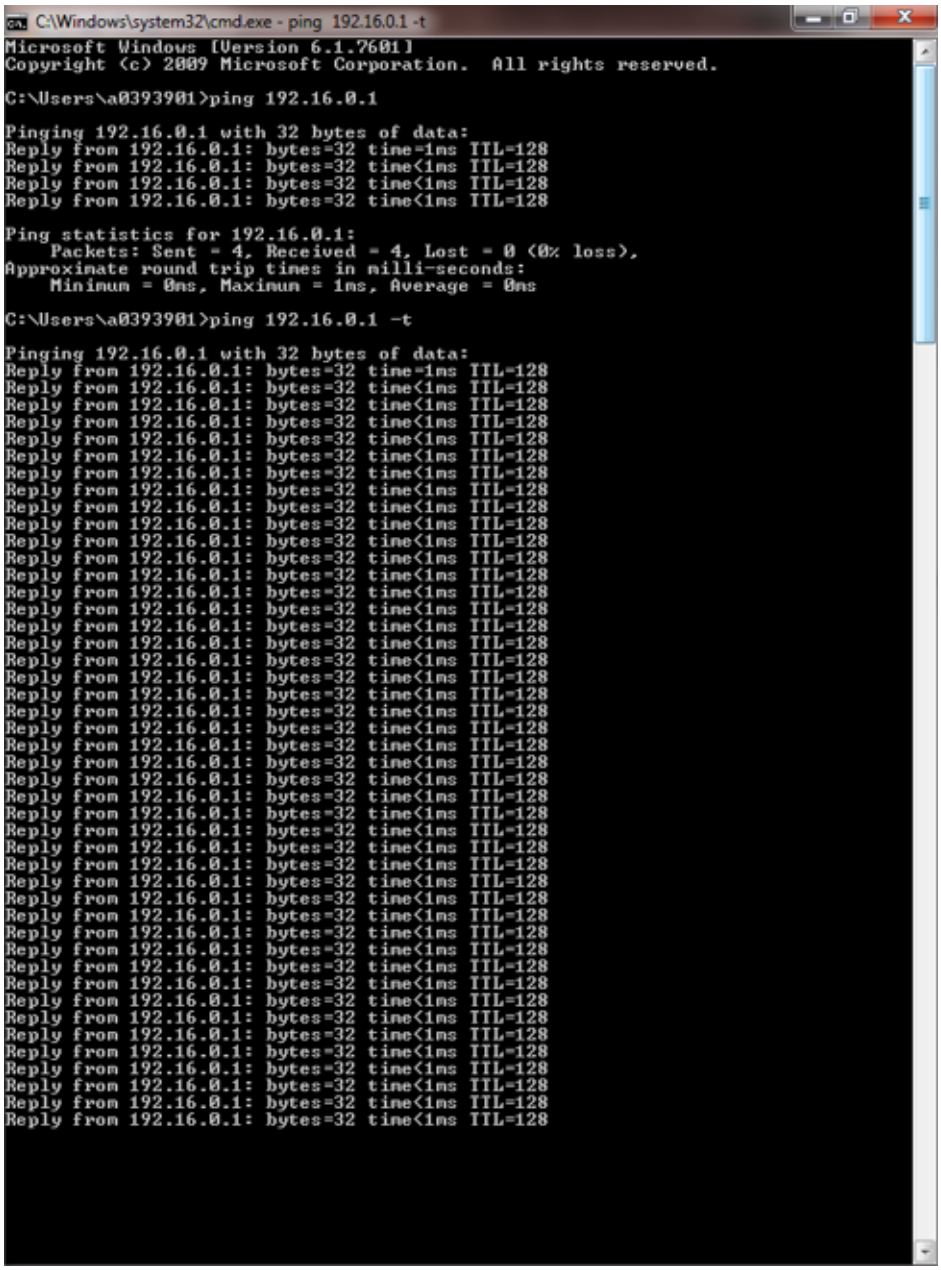


図 19. Ping Test (for Continuous Replies)

To stop the replies, press *CTRL+C* or close the command prompt window. It will show the following window and stop the replies (図 20).

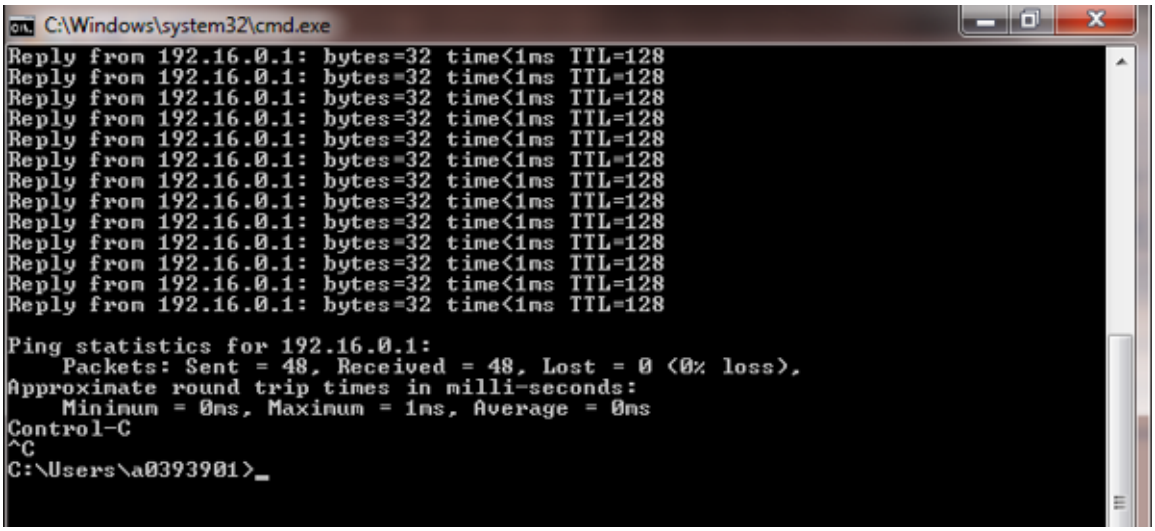


図 20. Ping Test Stopped

The data traffic can also be monitored using the Wireshark tool. First, open Wireshark software. Select the network "Local Area Connection", go to the *Capture* menu and click *Start*. The window will show the requests and replies as shown in 図 21.

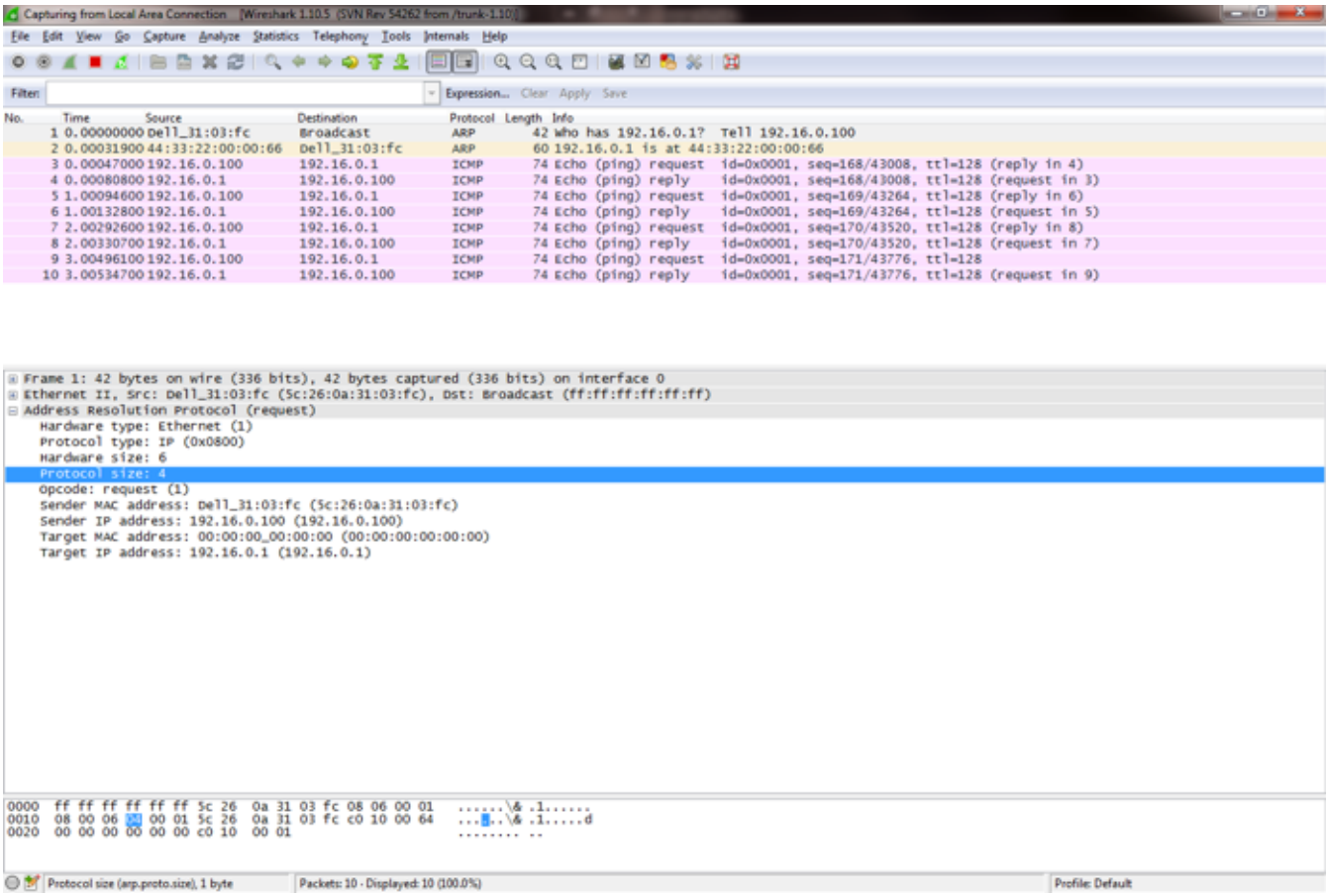


図 21. Wireshark Showing Data Traffic

7.3 IEEE 1588 Features Testing — IEEE 1588 PTP Synchronized Clock Output

These tests were been performed on an EVM board. See the application reports AN-1728[3] and AN-1729[4] for more details.

Many industrial, test and measurement, and telecommunications applications require highly accurate and precise clock signals to synchronize control signals, capture data, and so forth. The IEEE 1588 PTP used in standard Ethernet provides a method for propagating a master clock time to many nodes in a system. Current implementations rely purely on software or on a mix of software and FPGA or ASIC hardware. While nodes based on these implementations may be able to generate a clock output signal based on the master clock time, the precision of such a signal may not be sufficient for systems requiring extremely low clock jitter. In addition, there may be stringent requirements for clock phase alignment across the system. The DP83630/DP83640 precision PHYTER provides solutions to both of these issues.

The DP83640 includes a highly configurable clock output signal that is syntonized to its internal IEEE 1588 clock. Note that synchronization implies equal frequency but not necessarily equal phase. The nominal frequency of this clock is an integer division of 250 MHz (250 MHz/N, where N is an integer from 2 to 255). Therefore, the possible nominal frequencies are discrete values between 980.4 kHz and 125 MHz. The DP83630/DP83640 uses software assisted rate correction to eliminate the frequency offset between the local and master reference clocks. The final output frequency incorporates the same rate correction parameter (ppm offset) as the internal IEEE 1588 clock time. Since the rate correction is in units of sub-nanoseconds (one sub-nanosecond = 2_{-32} nanoseconds), the clock output frequency can be finely tuned (to the order of one part per billion). In addition to fixed values, the rate correction can be programmed to operate at one value for a short duration of up to ½ second (a "temporary rate"). After the temporary rate duration expires, the rate correction returns to the fixed rate correction value. By correcting additional frequency offset over a short time interval, the clock output signal will not exhibit discrete jumps in frequency or phase.

The DP83630/DP83640 also offers a method for aligning the phase of the clock output signal with that of the master clock. Unlike the trigger outputs of the device, which are generated with a discrete resolution of 8 ns, the clock output is generated from a highly tunable analog source, either a frequency-controlled oscillator (FCO) or phase generation module (PGM). The clock output is enabled at power-up by default, running at 25 MHz; however, the 1588 logic, including the 1588 clock, must be initialized prior to operation. Therefore, the initial phase relationship between the clock output and the 1588 master clock is not known. However, clever use of the DP83630/DP83640 features allows alignment of the clock output phase to the phase of the 1588 clock. There are advantages to both sources of the 1588 clock output. The FCO offers better jitter performance but has a smaller correction range and some usage restrictions in order to preserve the clock phase on a link loss event. The PGM does not have these restrictions and has a larger correction range, but its long term jitter performance is not as good as that of the FCO.

To test the PTP performance, the design is set up as shown in 6.1.3.

7.3.1 Jitter Testing

表 19. Jitter Test Results

SOURCE	CYCLE-TO-CYCLE		10-µs DELAY	
	PEAK TO PEAK (ps)	STANDARD DEVIATION (ps)	PEAK TO PEAK (ps)	STANDARD DEVIATION (ps)
FCO	320	53.1	340	58.5
PGM	340	53.2	1160	267.5

7.3.2 Clock Phase Error Testing

The synchronization error to the master is measured by determining the delay from the master clock output pin to the slave clock output pin. The devices were connected directly using a 1-m CAT5 cable. IEEE 1588 v1 was used with a 1-second sync period, 100-ms temporary rate duration, timestamp insertion enabled, and one-step operation enabled.

表 20. Clock Phase Error Test Results

SOURCE	CYCLE-TO-CYCLE	
	MEAN (ns)	STANDARD DEVIATION (ns)
FCO	4.647	5.905
PGM	5.134	6.381

7.4 IEEE 1588 Features Testing Time Synchronization

These tests were been performed on an EVM board. See the application reports AN-1728[3] and AN-1729[4] for more details.

There are three approaches to testing time synchronization: software testing, pulse per second signal comparison, and output clock comparison. Software testing relies on the results reported by the PTP stack to show the quality of the time synchronization. This means that the software results are subject to the same limitations as the PTP algorithm itself. The primary limitation of the PTP algorithm is that it cannot correct for differences in the length of the transmit path and the receive path. Another consideration when analyzing software results is that the reported error is always taken just before the time synchronization. Since the process is reporting an error that is essentially due to the drift between two clocks, the software error represents a worst case picture of the average time synchronization. The most common way to analyze time synchronization comes from looking at the PPS signal. Sending out a pulse at every second transition produces a PPS signal. For many older systems, the PPS signal is the only way to measure the success of time synchronization. The primary disadvantage to this measurement is that this effectively samples the error every second. Because there is not necessarily a correlation between the second transition and the clock synch update, it is difficult to achieve dependable results. Another issue with the PPS measurement is that the PPS signal is typically generated from a digital output that will add additional error to the synchronization results. That additional error will only impact digital inputs and outputs, but not the synchronized clock itself and, thus, should not be included in the synchronization measurement.

The most accurate method to measure clock synchronization is set both the master and slave to generate a clock output at a known frequency and then compare those two clock signals. This provides the error at many more times a second, providing a more accurate view of the time synchronization. As an additional benefit, the clock output can be handled through an analog output that will not add additional synchronization error.

To test the PTP performance, the design is set up as shown in 6.1.3.

7.4.1 Software Reported Synchronization Test Results

The software test setup relies on an FPGA card that emulates an Ethernet MAC to allow the control software to interface with the Ethernet PHY hardware. The software connects to the MAC emulator through a USB connection. The PTP packets and PHY controls are created by the MACs and sent to the Ethernet PHYs. The software portion of the PTP protocol is handled by the computer while the hardware portion of the PTP protocol remains in the DP83630/DP83640 on the PHY board.

表 21. Software Reported Synchronization Test Results(1)

MEAN	STANDARD DEVIATION	NO OF SAMPLES
1.59 ns	6.5 ns	500

(1) Synchronized to master using IEEE 1588 PTP

7.4.2 PPS Synchronization Test Results

Testing the PPS signal time synchronization was achieved by analyzing the PPS signals from both the master and slave devices with a Tektronix TDS784C oscilloscope.

表 22. PPS Synchronization Test Results(1)

MEAN	STANDARD DEVIATION	NO OF SAMPLES
–869 ps	7.87 ns	1000

(1) Synchronized to master using IEEE 1588 PTP

7.4.3 Clock Synchronization Test Results

Testing the PPS signal time synchronization was achieved by analyzing the clock output signals from both the master and slave devices with a Tektronix TDS784C oscilloscope. Both devices were set to output a 10-MHz clock signal for testing purposes.

表 23. Clock Synchronization Test Results(1)

MEAN	1-σ STANDARD DEVIATION	NO OF SAMPLES
–226 ps	2.655 ns	1100

(1) Synchronized to master using IEEE 1588 PTP

7.5 IEEE 1588 Functionality Testing (With PTP Master Simulator)

Test Setup IEEE 1588 Simulation

The time master is a Linux PC-based simulator. The PTP master is a service that could be invoked as necessary. The time master could generate the PTP messages that could verify the PTP slave functionality.

The TIDA-00496 board is connected to the TIDA-00226 Tiva MCU-based board using MII. The time master is connected using the copper Ethernet cable. The time master sends sync and follow up messages periodically every one second.

Pinging the slave board successfully confirms that the time master and the slave are in the same subnet. Ensure that IGMP is enabled in the master and slave and the IGMP packets are captured on Wireshark Ethernet packet sniffer. This confirms the packets are in the same multicast group.

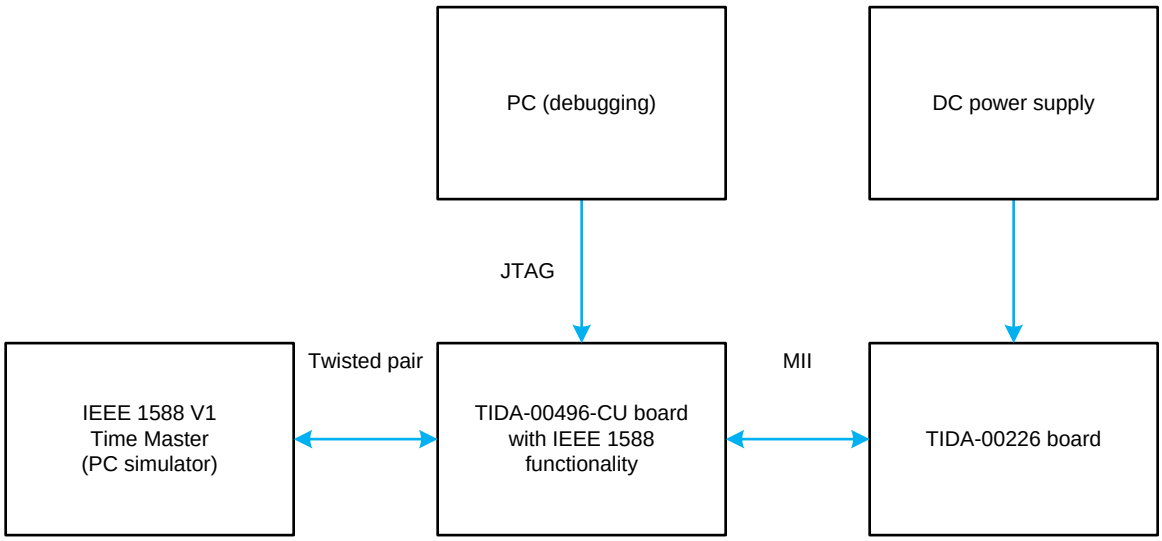


図 22. Setup for IEEE 1588 Testing With PTP Simulator

Timestamping Overview

Synchronization accuracy directly depends on time stamp accuracy. There are different options to take time stamps.

The most accurate method is to detect PTP frames with hardware assistance. Ethernet frame Ingress and egress can be timestamped at the PHY or at the MAC. PHY level timestamping provides better timestamping accuracy compared to MAC level timestamping.

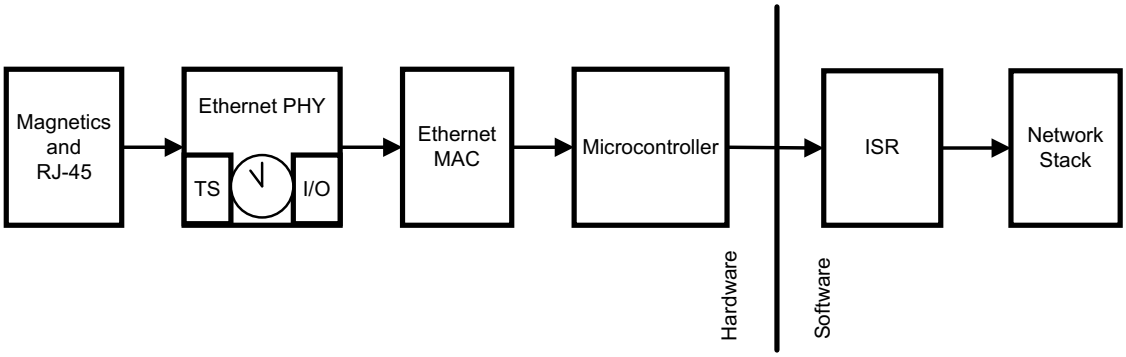


図 23. Timestamping Overview

7.5.1 Summary of PTP Tests Performed

Testing Overview

Time master sends sync and follow up messages periodically every one second (configured sync interval) using two-step clock. The slave sends a delay request to the time master and receives a delay response message.

Time offset from the master and the delay is computed and corrected periodically. For the first time, the clock time is set and read back to verify that the time has indeed been set. From the next time onwards, if the offset is above one second, add/subtract time is used. Once the offset is below one second, the frequency control kicks in and tries to catch up without causing rapid adjustments, but enables uniform and smooth transitions spread over one configured sync interval.

Time Master Configuration

The IP address is set to a static IP address (that is, 192.168.1.10 and subnet is set to 255.255.255.0). The sub-domain is set as _DFLT (default domain) IGMP messaging is enabled so that time master can join the IPV4 multicast address group 224.0.1.129.

Time master is started as a service. Ensure that the time master status is active and has started to send the PTP messages. (Firewall or antivirus software may prevent PTP messages.)

Time Synchronization Process

The PTP time master periodically broadcasts the current time as a message to the other clocks. Under IEEE 1588 broadcasts are up to once per second. Each Sync message broadcast is sent by the master to all the clocks in the domain. A clock receiving this message takes note of the local time (RX timestamp) when this message is received. The master may subsequently send a multicast Follow_Up with accurate timestamp at which SYNC message was sent.

To accurately synchronize to their master, clocks must individually determine the network transit time of the sync messages. The transit time is determined indirectly by measuring round-trip time from each slave clock to its master. The clocks initiate an exchange with their master designed to measure the transit time delay. The exchange begins with a clock sending a Delay_Req message at time (TX timestamp) to the master. The master receives and timestamps the Delay_Req at time (RX timestamp-Master) and responds with a Delay_Resp message. The master includes the timestamp (RX timestamp-Master) in the Delay_Resp message.

Testing the Transmit and Receive Timestamps

The PTP time master sends the IEEE 1588 packets and are received by the PTP slave. Timestamps are captured when sync or follow up messages are received. Timestamps are captured when Delay request message is transmitted. The captured timestamps are compared with the clock time for verification.

Set Time and Get Time

Once sync and follow up messages are received, the time difference (offset) between the master and slave time is computed. Clock time is updated by calling function setTime(). Alternatively, AddSubClockTime() can also be called. The offset time is highlighted on the right side while the updated time, which is read back from the clock using getTime(), is highlighted on the left side.

7.5.1.1 Rate Correction (Frequency Scaling)

The offset values are collected for a defined period of time (10 sync cycles with each sync cycle being one second) and clock variation is to be computed. If the correction value is greater than one second, the clock time is adjusted by using AddSubClockTime(). If the correction value is less than one second, rate correction (frequency scaling) is used to uniformly adjust the clock over one sync interval.

The PTP rate is controlled using the PTP rate control registers (PTP_RATEH and PTP_RATEL) and PTP temporary rate duration control registers (PTP_TRDH and PTP_TRDL). A fixed rate correction may be programmed as follows:

1. Write the rate direction (0x8000 for higher, 0x0000 for lower) and the upper 10 bits of the value to the PTP_RATEH register.
2. Write the lower 16 bits of the value to the PTP_RATEL register. The rate takes effect upon writing PTP_RATEL.

Example: Set fixed rate correction to –100 ppm relative to the master.

1. Since the nominal reference clock period is 8 ns, 100 ppm is 0.0008 ns. This is 0.0008 × 232 sub-nanoseconds, which equals approximately 3435974 sub-nanoseconds (0x346DC6).
2. Write 0x8034 to PTP_RATEH.
3. Write 0x6DC6 to PTP_RATEL.

A temporary rate correction is programmed in a manner similar to that of the fixed rate correction, except that bit 14 (0x4000) of PTP_RATEH must also be set. Because the temporary rate takes effect upon writing the PTP_RATEL register, the PTP temporary rate Duration registers must be programmed before setting the temporary rate. The rate correction value switches back to the fixed rate value after the temporary rate duration expires. The temporary rate duration is configured as follows:

1. The temporary rate duration is a 26-bit number in units of clock cycles. At the default 8-ns reference clock period, the maximum duration is about 537 ms.
2. Write the upper 10 bits of the temporary rate duration to PTP_TRDH.
3. Write the lower 16 bits of the temporary rate duration to PTP_TRDL.

The temporary rate duration setting takes effect upon writing this register, and remains constant until modified via register write. Often there will not be a need to change the temporary rate duration.

Example: Set a temporary rate correction of 3 ns over 10 ms:

1. For a temporary rate duration of 1 ms at the default reference clock period, the designer needs 10 ms / 8 ns = 1250000 clock cycles (0x1312D0). For 3 ns of correction over 1250000 clock cycles, the designer needs 3 ns / 1250000 = 0.0000024 ns = 10308 sub-nanoseconds per clock cycle (0x2844).
2. Write 0x0013 to PTP_TRDH.
3. Write 0x12D0 to PTP_TRDL.
4. Write 0xC000 to PTP_RATEH.
5. Write 0x2844 to PTP_RATEL.

7.6 PTP Register Functionality Testing

The PTP registers have been tested by executing various test cases. 表 24 lists the test results.

表 24. PTP Registers

PTP TESTS	OBSERVATION
PTP control register (PTP_CTL)	OK
PTP time data register (PTP_TDR)	OK
PTP status register (PTP_STS)	OK
PTP transmit timestamp register (PTP_TXTS)	OK
PTP receive timestamp register (PTP_RXTS)	OK
PTP event data register (PTP_EDATA)	OK
PTP transmit configuration register (PTP_TXCFG1)	OK
PTP receive configuration register (PTP_RXCFG0)	OK
PTP clock output control register (PTP_COC)	OK
PTP interrupt control register (PTP_INTCTL)	OK
PTP clock source register (PTP_CLKSRC)	OK
PTP GPIO monitor register (PTP_GPIOMON)	OK

7.7 Summary of PTP Functionality Tests Performed

There are many applications for time synchronized Ethernet that require closer synchronization than what can be achieved with software only implementations of time synchronization protocols. TI's DP83630/DP83640 precision PHYTER provides an easy to implement method for adding high precision time synchronization to Ethernet applications. The provided test results clearly show that the precision PHYTER solution provides very precise and accurate time synchronization of less than 10 ns standard deviation over a single link. This precision allows a hardware developer to develop a very capable, Ethernet-based solution for any application with strict time synchronization requirements. The results from software analysis, PPS signal analysis, and synchronized clock output analysis provide an accurate representation of the capabilities of the DP83630/DP83640 device to support application development and system design.

7.8 IEC Pre-Compliance Testing

This design is tested with the ESD IEC61000-4-2 standard EMC test. 表 25 details the performance criteria.

表 25. Performance Criteria

PERFORMANCE (PASS) CRITERIA	DESCRIPTION
A	The module must continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart or power off/power on.

7.8.1 IEC61000-4-2 ESD Test

This standard specifies a system's ability to withstand ESD events. Conditions are described under which direct or air discharge testing should be performed. In this application, metallic chassis grounded network connectors were used, so the direct coupling method was required. Applications utilizing all plastic chassis and connectors require air discharge testing.

Specifications are provided for rise time, current, and impedance control of the voltage applied in the testing. Texas Instrument's serial communications devices are designed and tested to withstand ESD energy on a component level as specified in individual device datasheets. IEC testing is defined for system level testing, which complements Texas Instrument's component testing.

To simulate a discharge event, an ESD generator applies ESD pulses to the equipment under test (EUT), which can happen through direct contact with the EUT (contact discharge). This was applied across RJ45 connector. A series of 10 negative and positive pulses were applied during the test (contact discharge). After the test, communication test was performed. The test results show the EUT was able to withstand the required discharge. The EUT was not permanently damaged.

表 26. ESD Test Steps

TEST NO	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 6 kV	Pass
6	Contact –6 kV	Pass

表 27. ESD Testing Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	RJ45 input	±4 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

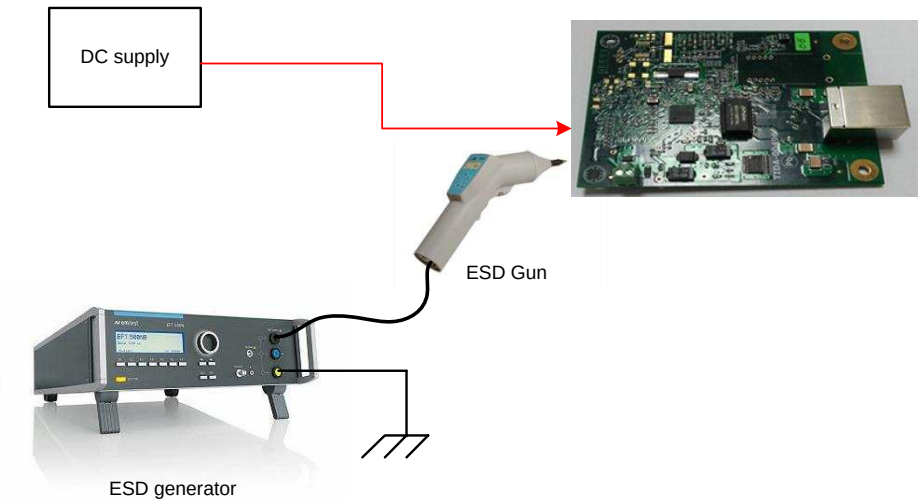


図 24. ESD Setup for Ethernet Brick

7.9 Summary of Test Results

表 28. Test Results

SERIAL NUMBER	PARAMETERS	RESULT
1	Power supply—LDO (onboard)	OK
2	Ethernet PHY—25-MHz oscillator and PTP clock output (25 MHz)	OK
3	Interface with MCU (host)	OK
4	Communication with twisted pair (copper) interface	OK
5	Communication with fiber interface	OK
6	Communication testing on multiple boards	OK
7	Loop back test	OK

8 Design Files

For simplicity, The design files are in two sets because there are a number of components that have to be mounted and unmounted to configure the board for copper or fiber interface.

8.1 Schematics

To download the schematics, see the design files at TIDA-00496.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00496.

8.3 Layer Plots

To download the layer plots, see the design files at TIDA-00496.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00496.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00496.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00496.

9 References

1. Texas Instruments, *Copper-to-Fiber Ethernet Media Converter*, TIDA-00306 Design Guide (TIDU510).
2. Texas Instruments, *32-Bit ARM® Cortex®-M4F MCU-Based Small Form Factor Serial-to-Ethernet Converter*, TIDA-00226 Design Guide (TIDU348).
3. Texas Instruments, *AN-1728 IEEE 1588 Precision Time Protocol Time Synchronization Performance*, Application Report (SNLA098).
4. Texas Instruments, *AN-1729 DP83640 IEEE 1588 PTP Synchronized Clock Output*, DP83640 Application Report (SNLA099).

10 Terminology

PTP— Precision time protocol

PPS— Pulse per second

FCO— Frequency-controlled oscillator

PGM— Phase generation module

PD— Pulled down

PU— Pulled up

PMD— Physical medium dependent

11 About the Author

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2015年10月発行のものから更新 **Page**

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