参考資料

TI Designs
磁気耐性トランスレス絶縁シャント電流測定用電源

概要

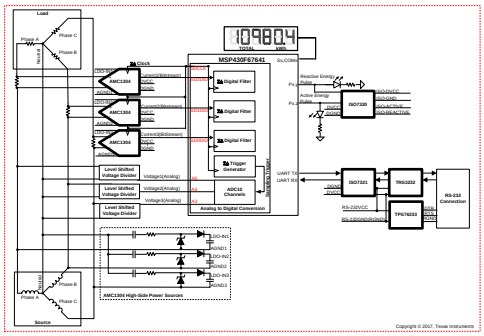
このTI Designは、絶縁デルタ-シグマ変調器を使用して、絶縁型シャント・センサを持ち変圧器を使用しないクラス0.5三相エネルギー測定システムを実装します。このデルタ-シグマ変調器は、出力回路が容量的に入力回路と絶縁されているため、変圧器なしでデータ絶縁が可能です。各変調器のハイサイドは、変圧器を使用しないキャップドロップ電源により駆動されます。変圧器を使用しないため、このTI Designは本質的に磁気耐性があります。さらに、ハイサイドに配置したキャップドロップ電源は、システム全体のコスト低減に寄与し、本質的に伝導性および放射性エミッションが低いことに加えて、ハイサイドはローサイド電源からではなく商用電源から独立に電力供給されるため、ローサイド電源からの消費電流を低減します。

リソース

TIDA-01094	デザイン・フォルダ
AMC1304M05	プロダクト・フォルダ
AMC1305M05	プロダクト・フォルダ
TLV70450	プロダクト・フォルダ
MSP430F67641A	プロダクト・フォルダ
TRS3232	プロダクト・フォルダ
ISO7321	プロダクト・フォルダ
TPS70933	プロダクト・フォルダ
ISO7320	プロダクト・フォルダ

TI E2E™ Community

E2Eエキスパートに質問

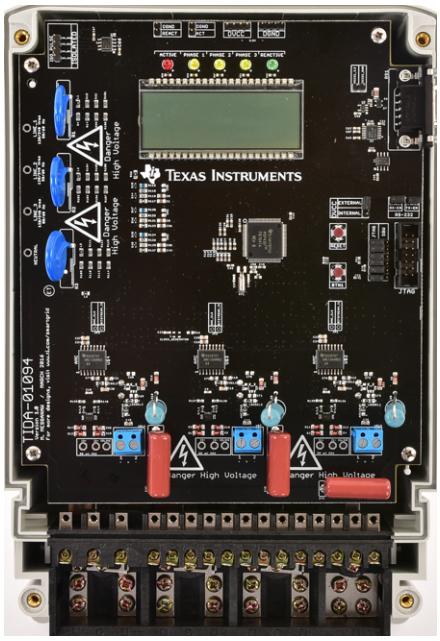


特長

- クラス0.5%三相測定、ガルバニック絶縁されたシャント電流センサ使用
- 変調器のハイサイド用のキャップドロップ電源
- 最高で1kV AC (動作電圧)および7kV (ピーク)の絶縁性能
- AMC1304M05とAMC1305M04+TLV70450の両方の構成をサポート
- TIのエネルギー・ライブラリ・ファームウェアにより、アクティブ/リアクティブな電力とエネルギー、実効値(RMS)電流と電圧、力率、ライン周波数など、各種のエネルギー測定パラメータを計算
- PCのグラフィカル・ユーザー・インターフェイス(GUI)との通信用に3kV$_{RMS}$動作絶縁境界の特性を持つ絶縁型RS-232

アプリケーション

- 電気メーター
- 電力品質測定器
- 電力品質分析器



1 System Overview

1.1 System Description

Three-phase electricity meters are used to measure the energy consumption at a business or industrial site. In order to properly sense energy consumption, voltage and current sensors are used to translate mains voltage and current to a voltage range that an analog-to-digital converter (ADC) can sense. For three-phase electricity meters, it is necessary for the current sensors to be isolated in order to be able to properly sense the energy consumption of multiple phases without damaging the ADC. As a result, current transformers, which inherently have isolation, have historically been used for the current sensors for three-phase electricity meters. One disadvantage of current transformers (and many transformers in general) is that they can be paralyzed by applying a strong enough magnetic field so that the sensed energy consumption would be less than the actual energy consumption. Due to this weakness of current transformers against magnetic fields, it is common for people to try to tamper with a meter by placing a strong magnet outside the electricity meter to try paralyze the current transformers in order to steal electricity. This TI Design prevents magnet tampering by using isolated shunts as current sensors instead of current transformers.

In this TI Design, a class 0.5 three-phase transformerless energy measurement system is implemented with isolated shunt sensors by using isolated delta-sigma modulators. The delta-sigma modulators have their output circuitry capacitively isolated from input circuitry, thereby providing transformerless data isolation. The high-side of each modulator is powered by a cap-drop supply that is also transformerless. Because a transformer is not used in this design (whether a power supply transformer or current transformer), the TIDA-01094 is inherently magnetically immune, thereby preventing electricity theft due to magnetic tampering. In addition, the high-side cap-drop power supply reduces the entire system cost, has inherent low conducted and radiated emissions, and reduces the current consumption drawn from the low-side power supply since the high-side is separately powered from mains instead of being derived from the low-side power supply.

An energy measurement system on chip (SoC) takes the different bit-streams from the isolated modulators and uses the onboard digital filters of the SoC to produce ADC sample readings. The energy measurement SoC is also used for sensing voltages, calculating metrology parameter values, driving the board's liquid crystal display (LCD), and communicating to a PC GUI through the board's isolated RS-232 circuitry. In regard to metrology, the software energy library supports calculation of various parameters for up to three-phase energy measurement. The key parameters calculated during energy measurements are: RMS current and voltage; active power, reactive power, and energies; power factor; and frequency. These parameters can be viewed either from the calibration GUI or LCD.

Another advantage of using shunts is that it does not share the same degradation in metrology results that current transformers show when harmonics are present in a system. As a result, these isolated shunt current sensors may also be used for equipment that perform harmonic analysis, such as power quality meters or power quality analyzers.

1.1.1 AMC1304M05

The AMC1304 is used to provide isolated current measurement for the design's shunt current sensors. This isolated current measurement is accomplished by the AMC1304 providing a modulation bit-stream output that is capacitively isolated from the analog signal fed from the shunts to the AMC1304, as 図 1 shows.

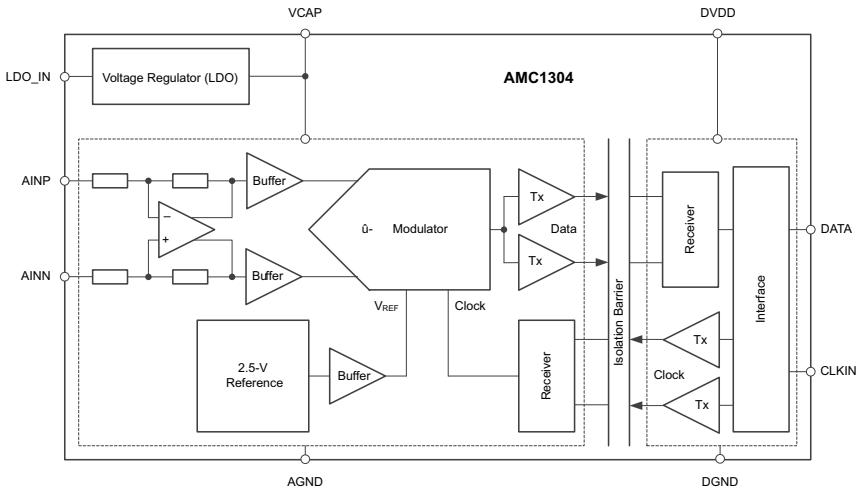


図 1. AMC1304 Simplified Block Diagram

In 図 1, the shunt current measurement is made across terminals AINP and AINN of the AMC1304. The third terminal of the shunt is then connected to AGND of the AMC1304. To perform measurements, 4 to 18 V must be fed between LDO_IN and AGND. The AMC1304 then uses its integrated low dropout voltage (LDO) regulator to power the high-side of the chip, which includes the modulator.

To properly power the controller side, pins DVDD and DGND on the AMC1304 must be connected to DVCC and DGND of the MSP430F67641A. In addition, the modulation clock used by the MSP430F67641's SD24_B digital filters must be connected to CLKIN. This modulation clock must be between 5 to 20 MHz for the AMC1304 to properly work and can either be generated from the clock output of the MSP430 SD24_B module or from an external clock generator that is fed to both the MSP430F67641A SD24_B and the AMC1304s. With a proper clock fed into CLKIN, the bit-stream is output from the AMC1304s DATA pin. This DATA pin must be connected to the MSP430F67641A digital bit-stream input.

For selecting an AMC1304 chip, there are four device variations. Two of these variations correspond to a CMOS digital interface option (denoted with an "M" in the part name) and the other two correspond to a low-voltage differential signaling (LVDS) digital interface option (denoted with an "L" in the part name). To properly interface to the MSP430F67641A, select the CMOS options. From the CMOS options, there is an option to choose from having a ±50-mV input range (denoted with a "05" in the part name) or a ±250-mV input range (denoted with a "25" in the part name). For e-meter applications, typically shunts with small resistances are used to reduce the power dissipation of the shunt; therefore, to use the full input range of the AMC1304, the ±50-mV input range must be used instead of the ±250-mV input range. As a result, the AMC1304M05 is the AMC1304 device variation that is best suited for this design.

For the AMC1304M05 device variant, if the input voltage value exceeds ±50 mV, there is degradation in the accuracy of readings. Also, to find out the density of ones that result from applying a certain differential input voltage (assuming it is not at the full-scale voltage or beyond this), use the following formula in 式 1:

$$\%_{HIGH} = 100 \times \left(\frac{V_{input} + 0.625}{1.25} \right) \quad (1)$$

From this formula, a differential input voltage of 0 V corresponds to the associated bit-stream that has a stream of ones and zeros that are high 50% of the time, a differential input voltage of 50 mV has ones and zeros that are high 90% of the time, and a differential input of –50 mV produces a stream of ones and zeros that are high 10% of the time.

1.1.2 AMC1305M05

As an alternative option to using the AMC1304M05 with its internal LDO, the AMC1305M05 could be used with an external TLV70450 LDO. 図 2 shows a block diagram of the AMC1305.

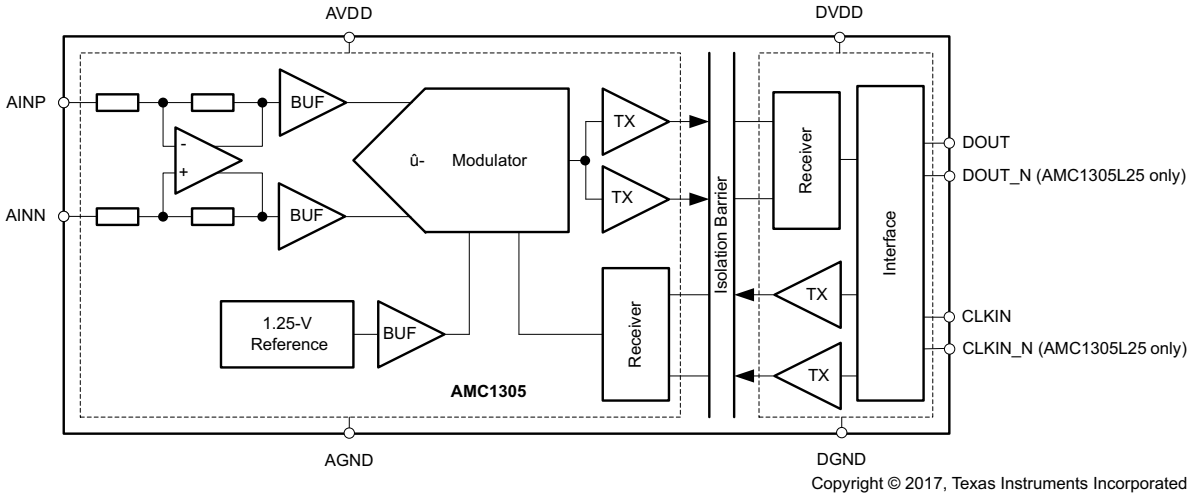


図 2. AMC1305 Simplified Block Diagram

The AMC1305M05 is similar to the AMC1304M05 except it does not have an internal LDO on the high-side of the modulator. As a result, 5 V must be fed between AVDD and AGND.

1.1.3 TLV70450

When the AMC1305 device is used instead of the AMC1304, an external LDO is needed to regulate the voltage to the AMC1305's high-side power because the AMC1305 does not have an internal LDO. The TLV70450 LDO can be used as this external LDO. In this configuration, the input of the TLV70450 would be connected to the output of the unregulated cap-drop power supply and the output of the LDO would be connected directly to AVCC of the AMC1305.

1.1.4 MSP430F67641A

For sensing and calculating the metrology parameters, the MSP430F67641A energy measurement SoC is used. This device is the latest metering SoC that belongs to the MSP430F67xxA family of devices. This family of devices belongs to the powerful 16-bit MSP430F6xx platform, which brings in many new features and provides flexibility to support robust poly-phase metrology solutions. These chips are intended for energy measurement applications and have the necessary architecture to support this application.

The MSP430F67xxA devices have a delta-sigma ADC module (SD24_B) with ADCs that have the capability to use their own internal modulator or an external modulator. In this TI Design, the external modulator option is used so that the digital filter of the MSP430F67641 can be used with the isolated delta-sigma modulators that measure the current. 図 3 shows the block diagram of one of these SD24_B converters. In 図 3, the items shaded red are used when the external modulation option is selected and the items that are unshaded are bypassed when using an external modulator.

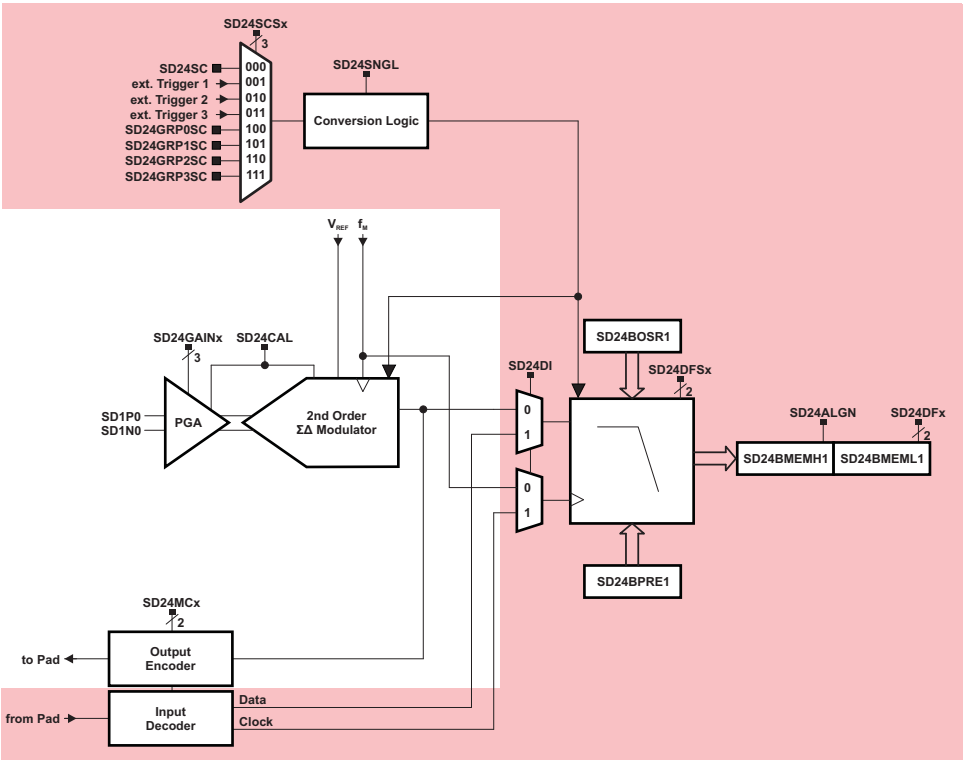


図 3. SD24_B Converter Block Diagram

To minimize the number of isolated delta-sigma modulators in the design, the modulators are only used for measuring current. As a result of using these modulators, the modulation clock frequency used in the SD24_B module is too high to be able to use the internal modulator of any extra SD24_B ADCs that are not already connected to the external modulators. Because of this constraint, the integrated 10-bit SAR ADCs of the MSP430F67641A are used for sensing phase voltages as is done in the following design: TIDM-THREEPHASEMETER-F67641.

To synchronize the SAR ADCs and the SD24_B, all of the MSP430F67xxA poly-phase devices have a trigger generator that triggers the ADC10 to ensure that the timing between the ADC10 and SD24_B modules are grouped and synchronized. 図 4 shows the block diagram of this trigger generator.

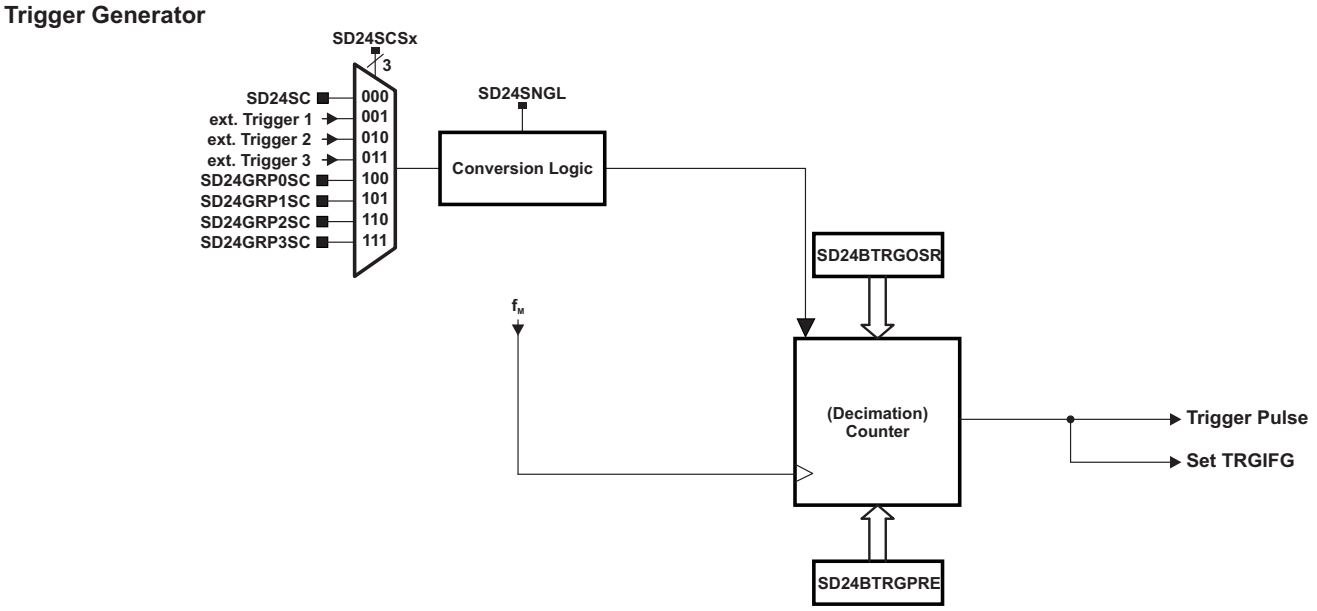


図 4. SD24_B Trigger Generator Block Diagram

1.1.5 TRS3232

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232 device. The TRS3232 device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

1.1.6 ISO7321

To add isolation to the RS-232 connection to a PC, the isolated RS-232 portion of this design uses capacitive galvanic isolation, which has an inherent lifespan advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The TI ISO7321 device is a simple dual-channel isolator that is capable of operating at 3.3 V or 5 V, enabling a wide range of devices that can connect to the data circuit-terminating equipment (DCE) side of the interface. The ISO7321 device can simply be inserted into a universal asynchoronous receiver/transmitter (UART) signal path, with the appropriate power supplies on each side to enable operation. The ISO7321 device also maintains 3 kV of isolation in order to meet the Underwriters Laboratories (UL) certification levels.

The ISO7321 device is available as the ISO7321C and ISO7321FC variants, where the difference of these variants is in whether the default output is high or low. Although both variants can be used in the design, this TI Design specifically uses the ISO7321C device. In addition, as an alternative, other isolators such as the ISO7421 can also be used because they are pin-to-pin compatible with the ISO7321.

1.1.7 TPS70933

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this design utilizes the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 to 12 V, depending on the driver implementation. The 5 to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

1.1.8 ISO7320

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of a meter by calculating the error based on these pulses and how much energy is provided to the meter. In this TI Design, pulses are output through headers for the cumulative active and reactive energy consumption. Using the ISO7320 provides an isolated version of these headers for connection to non-isolated equipment. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the isolated sides VCC (ISO_VCC) and the isolated sides GND (ISO_GND).

The ISO7320 device is available as the ISO7320C and ISO7320FC variants, where the difference of these variants is in whether the default output is high or low. Although both variants can be used in the design, this design specifically uses the ISO7320C device. In addition, as an alternative, other isolators such as the ISO7420 can also be used because they are pin-to-pin compatible with the ISO7320.

1.2 Key System Specifications

表 1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	3
Accuracy class	Class 0.5
Current sensor	Shunt
Voltage ADC type	SAR (MSP430F67641A)
Current ADC type	• Option 1: Delta-sigma modulator (AMC1304M05) + sinc3 filter(MSP430F67641A) • Option 2: Delta-sigma modulator (AMC1305M05) + TLV70450 + sinc3 filter(MSP430F67641A)
Delta-sigma (for current channels) modulation clock frequency	5,033,164.8 Hz
Delta-sigma (for current channels) OSR	1024
Delta-sigma (for current channels) output sample rate	4,915.2 samples per second
Ratio of skipped samples to total samples	0/5
Effective sample rate (for both current and voltage)	4,915.2 samples per second
Phase compensation implementation	Hardware (Delta-sigma module feature)
Phase compensation resolution	198.68 ns = 0.00358° at 50 Hz or 0.00429° at 60 Hz
Selected CPU clock frequency	25,165,824 Hz
System nominal frequency	50 or 60 Hz
Measured parameters	• Active power, reactive power, apparent power, and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Utilized LEDs	Total Active Energy and Total Reactive Energy
Communication	LCD; PC GUI via Isolated RS-232
Isolated modulator high-side power	Option 1: Power derived from mains using cap-drop supply; Option 2: External power
Key devices	AMC1304M05 or AMC1305M05 + TLV70450, MSP430F67641A, TRS3232, ISO7321C, TPS70933, and ISO7320C

1.3 Block Diagram

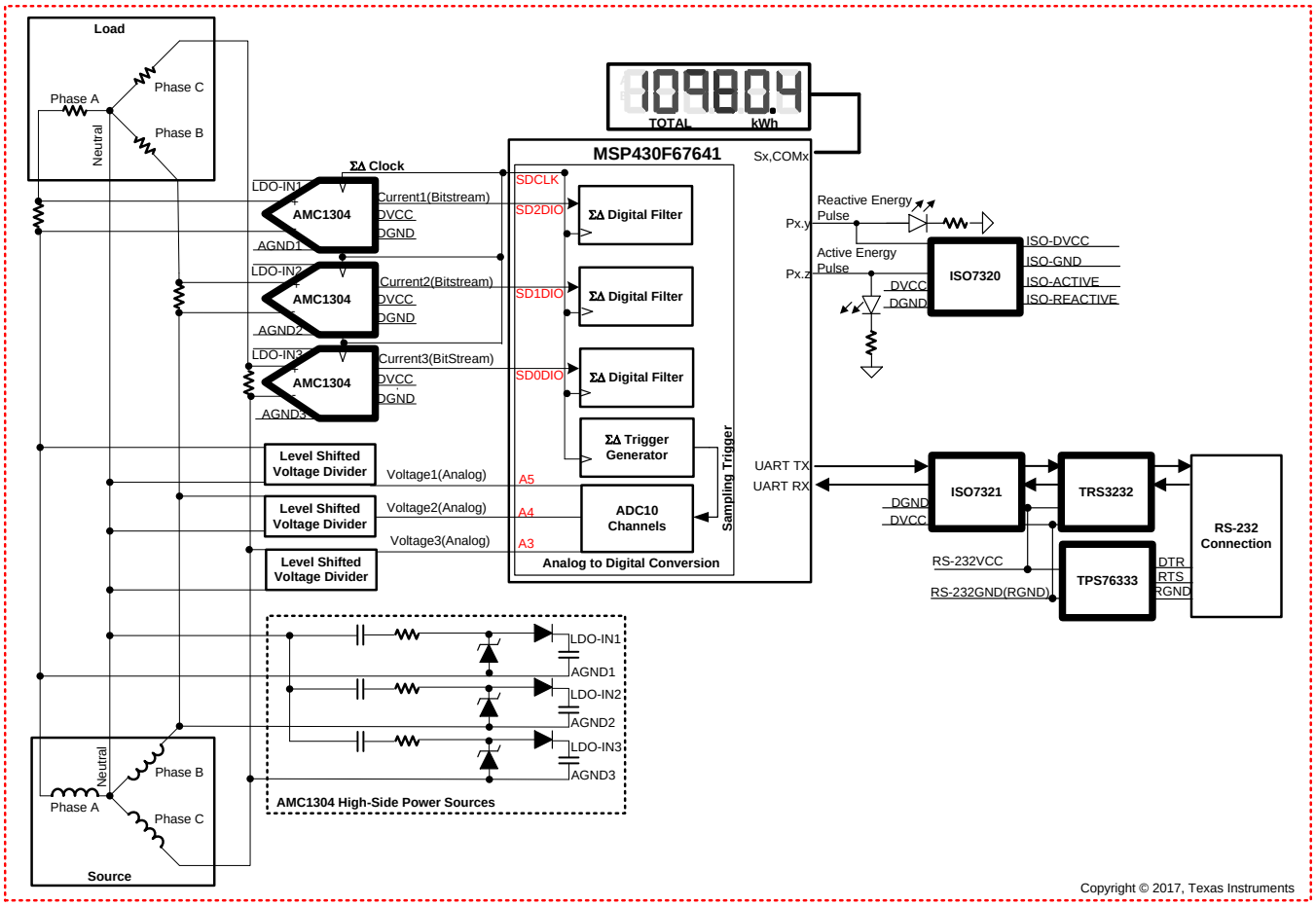


図 5. System Block Diagram for AMC1304 Configuration

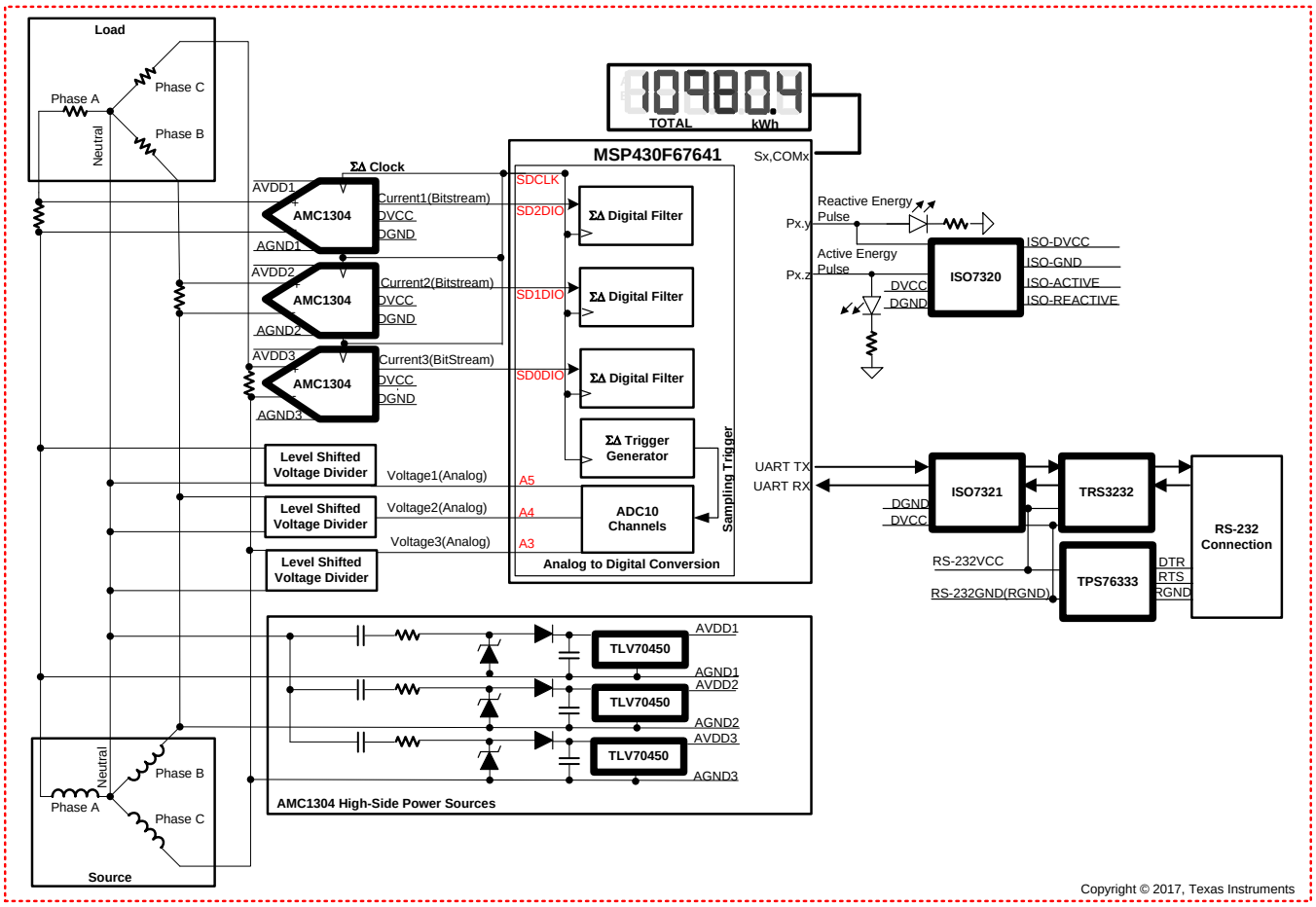


図 6. System Block Diagram for AMC1305 Configuration

図 5 depicts a block diagram that shows the high-level interface used for an MSP430F67641A-based three-phase energy measurement application with isolated shunts using AMC1304 devices. If the AMC1305 configuration is used instead of the AMC1304 configuration, 図 6 shows the corresponding block diagram. 図 5 and 図 6 show a three-phase, four-wire star connection to the AC mains in this case. In this TI Design, each phase has a shunt current sensor and an AMC device for measuring the voltage across the shunt current sensor. The resistance of the shunt is selected based on the current range required for energy measurements and also the minimization of the maximum power dissipation of the shunt.

For powering the high-side of the AMC, each AMC has an external power supply. Because the AMC1304 has an internal LDO, this circuitry does not require an external LDO; however, if an AMC1305 configuration is selected for the board instead of the AMC1304 configuration, the TLV70450 is used for the external LDO. Note that because each high side of the AMCs must be referenced from a different line voltage, three different cap drop supplies are used. Each implemented power supply provides power to the associated AMC device by using a half-bridge cap-drop power supply from the line of that phase and neutral. In contrast, for powering the controller-side of the AMC chips, all AMCs should be powered from the same source that powers the MSP430F67641A device.

To perform conversions, all AMC chips must have the same external clock fed into them. In this TI Design, the SD24_B module outputs its modulation clock, which is generated internally within the MSP430F67641A, and feeds the modulation clock to all of the AMC chips. The AMC chips then output their corresponding bit-streams, which are isolated from the high-side part of the chips. Each of these bit-streams is fed into a different MSP430F67641A converter's bit-stream input.

For the voltage sensor, a combination of a voltage divider and level shifter are used to ensure that the input voltage to the ADC fits within the single-ended voltage range of operation. The range of operation is determined by the chosen reference voltage source of the SAR ADCs. The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to the normal input ranges that are valid for the SAR ADC, based on the selected reference voltage. To synchronize the SAR ADCs with the SD24_B module, the trigger generator within the SD24_B triggers the ADC10 to ensure that the timing between the ADC10 and SD24_B modules are grouped and synchronized.

Other signals of interest in 図 5 and 図 6 are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO7320 provides an isolated connection for these pulses for connecting to non-isolated equipment. In addition to isolated pulses, the design supports isolated RS-232 communication through the use of the TPS70933, ISO7321, and TRS3232 devices. For more information on the isolated RS-232 portion of the design, see the TIDA-00163 design.

1.4 Highlighted Products

1.4.1 AMC1304M05/AMC1304M05

The AMC1304 and AMC1305 devices are precision, delta-sigma (ΔΣ) modulators with the output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the UL 1577 standard, VDE V-0884-10 standards, and also a working insulation voltage over the life of the part of up to 1.0-$kV_{AC,RMS}$. On the high-side of the AMC1304, the modulator is additionally supplied with an integrated LDO regulator that allows an unregulated voltage between 4 and 18 V to power the high side of the chip.

1.4.2 TLV70450

The TLV704 series of low-dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power microcontrollers, such as the MSP430. The TLV704 operates over a wide operating input voltage of 2.5 to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients.

1.4.3 MSP430F67641A

The MSP430F67641A poly-phase metering SoC is a powerful, highly-integrated energy measurement solution that offers accuracy and low system cost with few external components. The F67641A uses the low-power MSP430 CPU with a 32-bit multiplier to perform all energy calculations, metering applications such as tariff rate management, and communications with automatic meter reading (AMR) or advanced metering infrastructure (AMI) modules. The chip has an LCD controller with support for up to 320 segments, a real-time clock (RTC) module with integrated offset and temperature calibration, and a separate auxiliary supply to power the RTC independently from the rest of the chip. 図 7 shows these features as well as additional ones for the MSP430F67641A SoC.

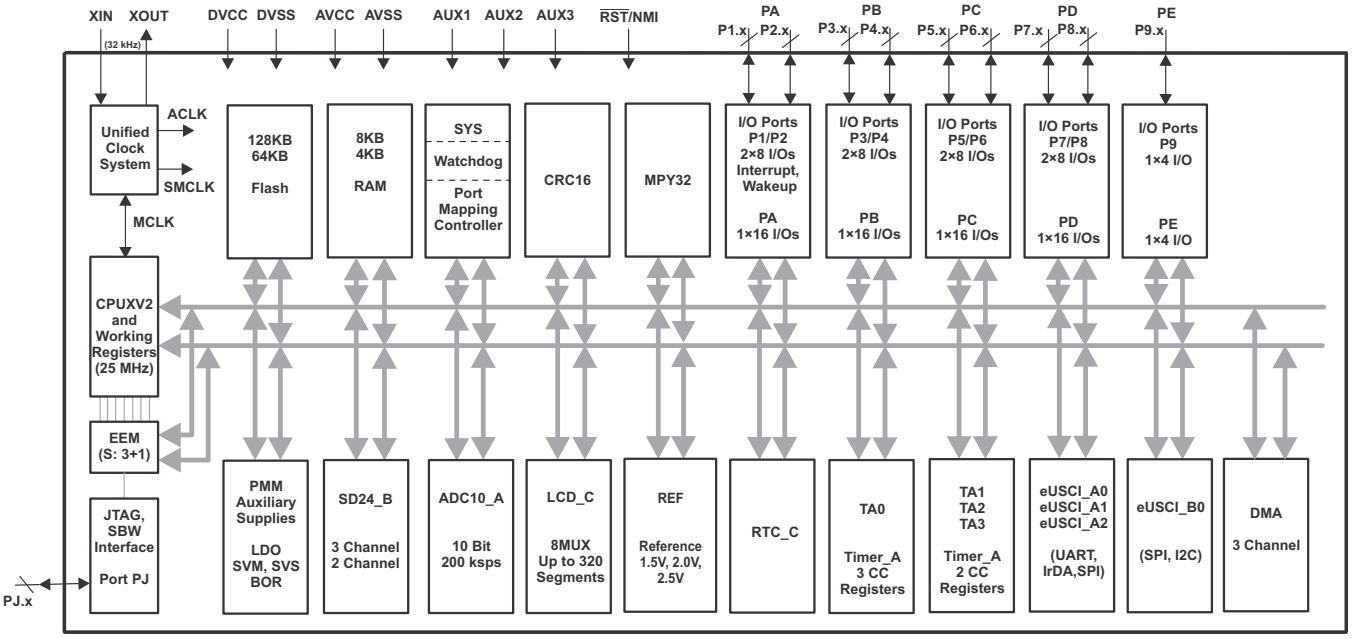


図 7. MSP430F67641A Block Diagram

1.4.4 TRS3232

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3- to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

1.4.5 ISO7321

The ISO7321 provides galvanic isolation up to 3 kV_{RMS} for one minute per UL. This digital isolator has two isolated channels where one is a forward channel and the other is a reverse channel. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. This chip supports a signaling rate of 25 Mbps. The chips can operate from 3.3- and 5-V supply and logic levels. At the rated voltage, the ISO7321 has over a 25-year isolation integrity.

1.4.6 TPS70933

The TPS709xx series of linear regulators are ultra-low quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical.

1.4.7 ISO7320

The ISO7320 provides galvanic isolation up to 3 kV_{RMS} for 1 minute per UL. This digital isolator has two isolated forward channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. This chip supports a signaling rate of 25 Mbps. The chips can operate from 3.3- and 5-V supply and logic levels. At the rated voltage, the ISO7320 device has over a 25-year isolation integrity.

2 System Design Theory

2.1 Design Hardware Implementation

2.1.1 Analog Inputs

The design of the front end consists of the three AMC chips used for measuring current: the MSP430F67641A's three digital filters that are connected to each AMC, a 10-bit SAR ADC (ADC10_A), and a mechanism to synchronize the digital filters with the SAR ADC.

For maximum accuracy, the AMC requires that the input analog signal voltage does not exceed ±50 mV. In addition, the AMC has differential inputs; therefore, the AC current signal from mains can be directly interfaced without the requirement for level shifters.

In contrast, the ADC10_A module has single-ended inputs. Therefore, the ADC10_A requires that the sensed voltage is between 0-V_{REF} volts, with the option to select the V_{REF} source and voltage in the software. As a result, after the mains voltage is divided down for sensing, the voltage front-end circuitry requires a level shifter to properly interface to the ADC10_A module.

2.1.1.1 Voltage Analog Front-End

The voltage from the mains is usually 230 V or 120 V and must be brought down to within V_{REF} volts. The analog front-end for voltage consists of spike protection varistors followed by a voltage divider and shifter network, and a RC low-pass filter that functions like an anti-alias filter.

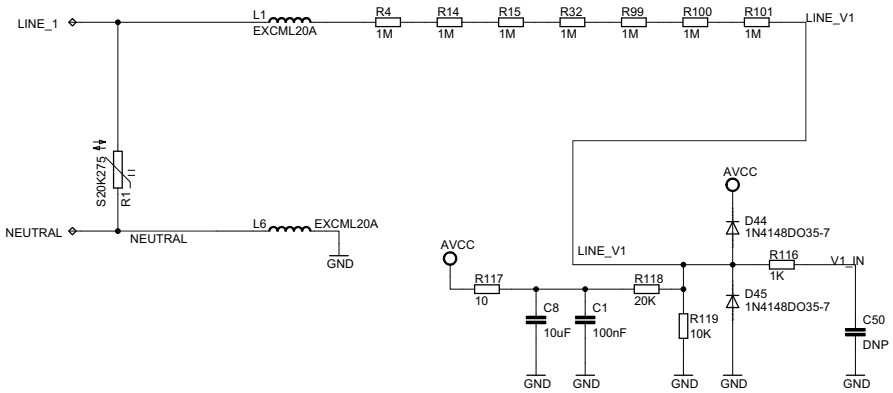


図 8. Analog Front-End for Voltage Inputs

図 8 shows the analog front-end for the voltage inputs for a mains voltage of 230 V. The voltage is brought down to a range within V_{REF} volts, where V_{REF} is selected to be the 2.0-V reference produced by the chips reference module. The maximum voltage that is fed to the ADC is usually a certain margin below the maximum V_{REF} voltage. As an example, when the 2.0-V reference is selected, the front end may be built to produce a maximum voltage of 1.4 to 1.6 V when the maximum mains voltage is applied. This margin helps prevent ADC clipping when the system is exposed to harmonics or an overvoltage condition.

2.1.1.2 Current Front-End

2.1.1.2.1 AMC High-Side Power Supply

To sense the voltage across the shunt, the high-side of each AMC device must be powered. Because each AMC should be referenced from a different line voltage, a different power supply is required for each AMC. In this design, there are two options for powering the high-side of the AMC devices: an onboard half-bridge cap-drop power supply or an off-board, custom power supply.

There are multiple advantages to using the onboard cap-drop high-side power supply. First, this cap-drop power supply does not have any magnetic components, so the power supply should be magnetically immune to magnetic fields instead of only being magnetically tolerant to a certain limit. Additionally, cap-drop supplies are relatively inexpensive compared to alternative power supply options. Also, LDO-based cap-drop power supplies inherently have low conducted and radiated emissions compared to SMPS power supplies. Finally, because the power to each AMC high side would be derived directly from mains instead of from the controller-side power supply, less current (<20 mA for the entire controller side of the board, which includes the F67641A, AMC high-side, and isolators) is drawn from the controller-side power supply allowing the specifications on the controller-side power supply maximum current drive to be relaxed.

図 9 shows the design's implementation of the high-side power supply. In this implementation, VIN3 is fed directly into the AMC to provide power to it. For the AMC1304 configuration, VIN3 is the unregulated output from the half-bridge cap-drop supply and is fed to the LDO_IN pin of the AMC1304. Because the AMC1304 has an integrated LDO, VIN3 can be unregulated as long as the voltage fed into LDO_IN of the AMC1304 is within the 4- to 18-V operating range. As an alternative to using the onboard cap-drop power supply for the AMC1304 configuration, the design has the option to instead power the AMC1304 by providing the necessary 4- to 18-V from an external isolated voltage supply to the associated terminal block (U$14 in 図 9).

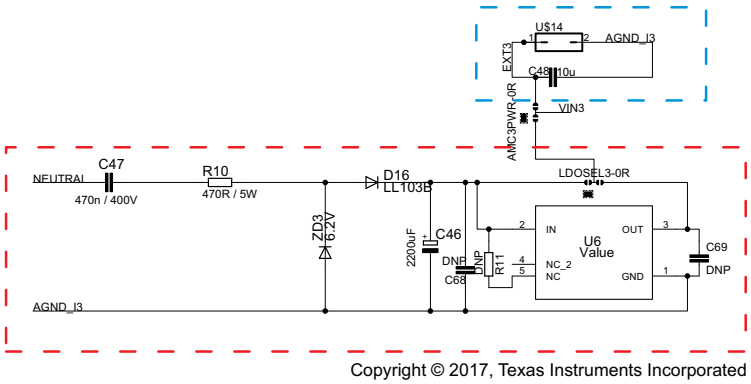


図 9. AMC High-Side Power Options

For the AMC1305 configuration, the unregulated output from the half-bridge cap-drop power supply is fed into a TLV70450 LDO. The regulated output of the TLV70450 is then fed into the AVDD pin of the AMC1305. As an alternative to using the onboard cap-drop power supply for the AMC1305 configuration, the design has the option to instead power the AMC1305 by providing the necessary 5 V from an external isolated voltage supply to the associated terminal block(U$14 in 図 9).

For both AMC1304 and AMC1305 configurations, the modulation clock frequency is selected to be a relatively minimum value to minimize the current consumption of the AMC high-side, thereby allowing the relaxation of the maximum current drive specification on the cap-drop supply. In this TI Design, the onboard cap-drop power supplies are able to power the high-side of the AMC devices for voltages as low as 75 $V_{AC,RMS}$ at 50 and 60 Hz .

2.1.1.2.2 Current Sensing

The analog front-end for current inputs is different from the analog front-end for the voltage inputs. 図 10 shows the analog front-end used for a current channel.

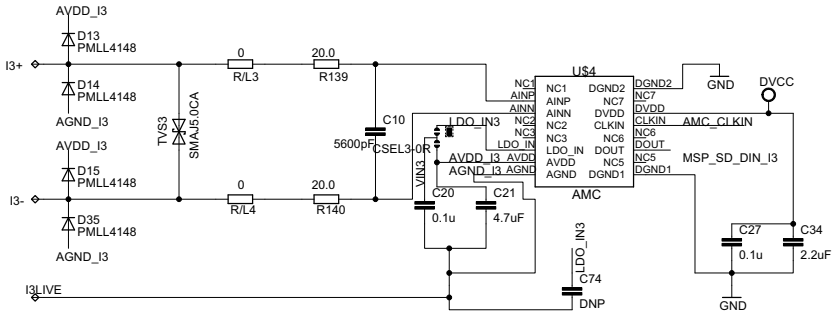


図 10. Analog Front-End for Current Inputs

The analog front-end for current consists of diodes and transorbs for any additional transient voltage suppression, footprints (R/L3 and R/L4) that could be replaced with inductors for EMI suppression (these footprints are populated with 0-Ω resistors by default), an anti-alias filter (R139, R140, and C10), and the AMC isolated delta-sigma modulator.

In 図 10, the three-terminal shunt used for current measurement is to be connected at I3+, I3−, and I3Live. The value of this shunt is selected based on balancing maximizing the peak analog voltage input into the AMC with minimizing the power dissipation of the shunt. In particular, for optimal accuracy, the peak DC voltage fed into the AMC must be as close as possible to 50 mV without surpassing this voltage. This peak voltage is dependent on the rated maximum current of the system and the resistance of the selected shunt. For example, this design uses 400-µΩ shunts (utilized shunts are shown here: http://www.vishay.com/docs/30173/wsms3124.pdf). With these 400-µΩ shunts and a maximum RMS current of 90 A, the maximum DC voltage fed into the AMC is $90 \times \sqrt{2} \times (400 \times 10^{-6}) \approx 50$ mV. To minimize the power dissipation in the shunt, a smaller value shunt can also be used. In this design, 220-µΩ shunts are also used. However, by using smaller value shunts, the voltage fed into the AMC is also reduced. As a result, there is a tradeoff in accuracy. Based on the requirements of the system, the tradeoff in accuracy from using a shunt with a small resistance and the reduced power dissipation from choosing the smaller shunt must be taken into account when selecting the proper shunt value.

2.2 Metrology Software Implementation

This section discusses the software for the implementation of three-phase metrology. The first subsection discusses the setup of various peripherals of the metrology and application processors. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.2.1 Peripherals Setup

2.2.1.1 SD24_B Setup

The MSP430F67641A has three delta-sigma data converters, with each of them having the ability to bypass its internal modulator and accept an external bit-stream to be used with its associated digital filters. This feature is used to obtain ADC samples using the bit-stream input that is output from the AMC.

In addition, the SD24_B has a trigger generator module that is used to trigger the ADC10, which in turn is used to sense the corresponding three voltages of the three-phase system. In this application, all of the digital filters for the SD24_B ADCs and the trigger generator are grouped together for synchronization.

In this TI Design, the modulation clock used in the SD24_B is derived internally and output from the SD24_B module to the AMC device. The modulation clock (f_M) to the trigger generator and the digital filters of the SD24_B ADCs is derived from the F67641A's system clock, which is configured to run at 25,165,824 Hz. The AMC could only support a modulation clock frequency of 5 to 20 MHz, so the clock modulation frequency is divided down by using the clock dividers on the F67641A's SD24_B module. As the modulation clock frequency decreases, the current consumption of the AMC1304 decreases as shown in 図 11.

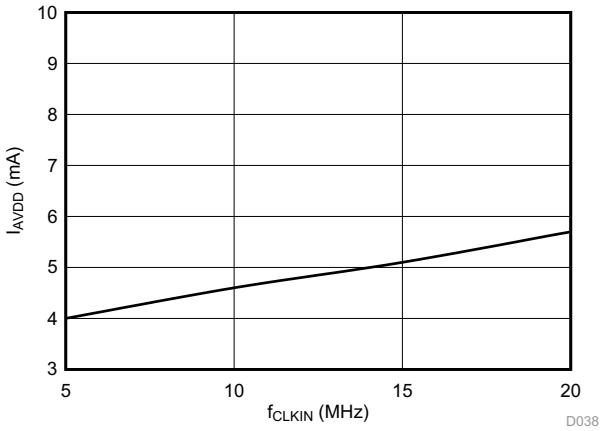


図 11. AMC1304 High-Side Current Consumption versus Clock Frequency

As a result, a modulation clock frequency of 5,033,165 Hz is used because it is the minimum frequency that can be supported by the AMC1304 while still being able to be derived by divided down the system clock using the SD24_B's clock divider. Because the digital filters of the MSP430F67641A's SD24_B ADC can also operate at this 5-MHz modulation clock frequency (unlike the internal modulators of the SD24_B ADC, which are bypassed in this application), there are no issues in using this modulation frequency in the system.

To reduce the central processing unit (CPU) utilization, the effective sample rate is divided down to 4915.2 samples per second for the digital filters. This reduction is accomplished by choosing the highest oversampling ratio (OSR) setting for the digital filters and trigger generator, which is 1024. Because the sampling frequency is defined as $F_s = f_M$ / OSR, this results in a sampling frequency of 4915.2.

In the application, the following SD24_B channels associations are used:

- SD0DIO (Converter 0 digital filter) → Current I1 (Current I_A)
- SD1DIO (Converter 1 digital filter) → Current I2 (Current I_B)
- SD2DIO (Converter 2 digital filter) → Current I3 (Current I_C)

2.2.1.2 ADC10_A Setup

The ADC10 is used to sample the three mains voltages and is triggered by the SD24_Bs trigger generator. When triggered by the ΣΔ, the ADC10 enters autoscan mode and samples 16 of its channels once. In the software, the clock to the ADC10 is set to 4 MHz. The sample and hold time for each converter is 8 cycles and the conversion time is 12 cycles, which results in an approximate 20-cycle (approximately 5 µs) delay between conversion results of adjacent converters. In addition, the ADC10_A uses the 2.0-V reference from the REF module and is configured to output 10-bit results that are scaled to 16-bit twos complement numbers (ADC10DF = 1). This configuration allows the ADC results from the ADC10 to be treated as a 16-bit signed number when performing mathematical operations.

In this application, the following are the relevant ADC10 channel associations:

- A10 (internal channel) → Temperature sensor
- A5 → Voltage V1
- A4 → Voltage V2
- A3 → Voltage V3

2.2.1.3 Real Time Clock (RTC_C)

The RTC_C is a real-time clock module that is configured to give precise one second interrupts. Based off of these one second interrupts, the time and date are updated in software, as necessary.

2.2.1.4 LCD Controller (LCD_C)

The LCD controller on the MSP430F67641A can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to ACLK/64, which is 512 Hz.

2.2.1.5 Port Map

The MSP430F67641A has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP430F67641A device in particular, the digital bit-stream inputs for the three SD24_B converters and the delta-sigma modulation clock output are all available options to port to ports P1, P2, and P3. In this TI Design, this port mapping feature is used for providing flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

- SDCLK (SD24_B modulation clock output) → Port P2.6
- SD0DIO (SD24_B Converter 0 digital filter input) → Port P3.1
- SD1DIO (SD24_B Converter 1 digital filter input) → Port P3.0
- SD2DIO (SD24_B Converter 2 digital filter input) → Port P2.7

2.2.2 Foreground Process

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. 図 12 shows the flowchart for this process.

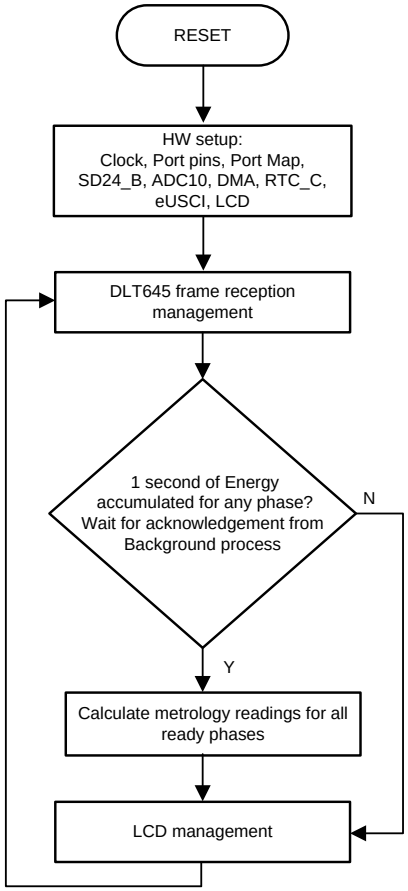


図 12. Foreground Process

The initialization routines involve the setup of the SD24_B module; ADC10_A module; DMA; clock system; general purpose input/output (GPIO) port pins and associated port map controller; RTC module for clock functionality; LCD; and the USCI_A0 for UART functionality.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the foreground's calculated values of active and reactive power, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in 2.2.2.1.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See 4.2.1 for more information about the different items displayed on the LCD.

2.2.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, energy, and temperature calculations.

As previous sections describe, voltage and current samples are obtained at a sampling rate of 4915.2 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (2)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph} \quad (3)$$

where:

- ph = Phase parameters that are being calculated [that is, Phase A(=1), B(=2), or C(=3)]
- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$= Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for each current

Power and energy are calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ph}(n)}{\text{Sample count}} \quad (4)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ph}(n)}{\text{Sample count}} \quad (5)$$

$$P_{APP,ph}^{2} = \sqrt{P_{ACT,ph}^{2} + P_{REACT,ph}^{2}} \quad (6)$$

where:

- $V_{90}(n)$ = Voltage sample at a sample instant 'n' shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the following 式 7, 式 8, and 式 9:

$$P_{ACT,Cumulative} = \sum_{ph=1}^{3} P_{ACT,ph} \quad (7)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^{3} P_{REACT,ph} \quad (8)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^{3} P_{APP,ph} \quad (9)$$

Using the calculated powers, energies are calculated by the following formulas in 式 10:

$$E_{ACT,ph} = P_{ACT,ph} \times \text{Samplecount}$$
$$E_{REACT,ph} = P_{REACT,ph} \times \text{Samplecount}$$
$$E_{APP,ph} = P_{APP,ph} \times \text{Samplecount} \quad (10)$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following 式 11, 式 12, and 式 13:

$$E_{ACT,Cumulative} = \sum_{ph=1}^{3} E_{ACT,ph} \quad (11)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^{3} E_{REACT,ph} \quad (12)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^{3} E_{APP,ph} \quad (13)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by the following formula:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \tag{14}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated by the following formula:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \tag{15}$$

In addition, temperature is also calculated in the software. Temperature is calculated using the TLV entries on the MSP430F67641A and is calculated in units of Celsius. The measured values for 30°C ±3°C and 85°C ±3°C for the 2.0-V reference are used for calculating temperature. The following 式 16 shows the exact formula that is used to calculate temperature:

$$\text{Temp} = \left(\text{ADC(raw)} - \text{CAL\_ADC\_20T30}\right) \times \left(\frac{85 - 30}{\text{CAL\_ADC\_20T85} - \text{CAL\_ADC\_20T30}}\right) \tag{16}$$

2.2.3 Background Process

図 13 shows the background process, which mainly deals with timing critical events in software. The background process uses the SD24_B trigger generation to collect voltage and current samples. The SD24_B interrupt occurs either when a new current sample is ready or when the trigger generator of the SD24_B triggers the ADC10. As soon as the trigger to the ADC is generated, sample processing is done on the previously obtained voltage and current samples. This sample processing is done by the "per_sample_dsp()" function. After sample processing, the background process uses the "per_sample_energy_pulse_processing()" for the calculation and output of energy-proportional pulses. 図 13 shows the flowchart for this process.

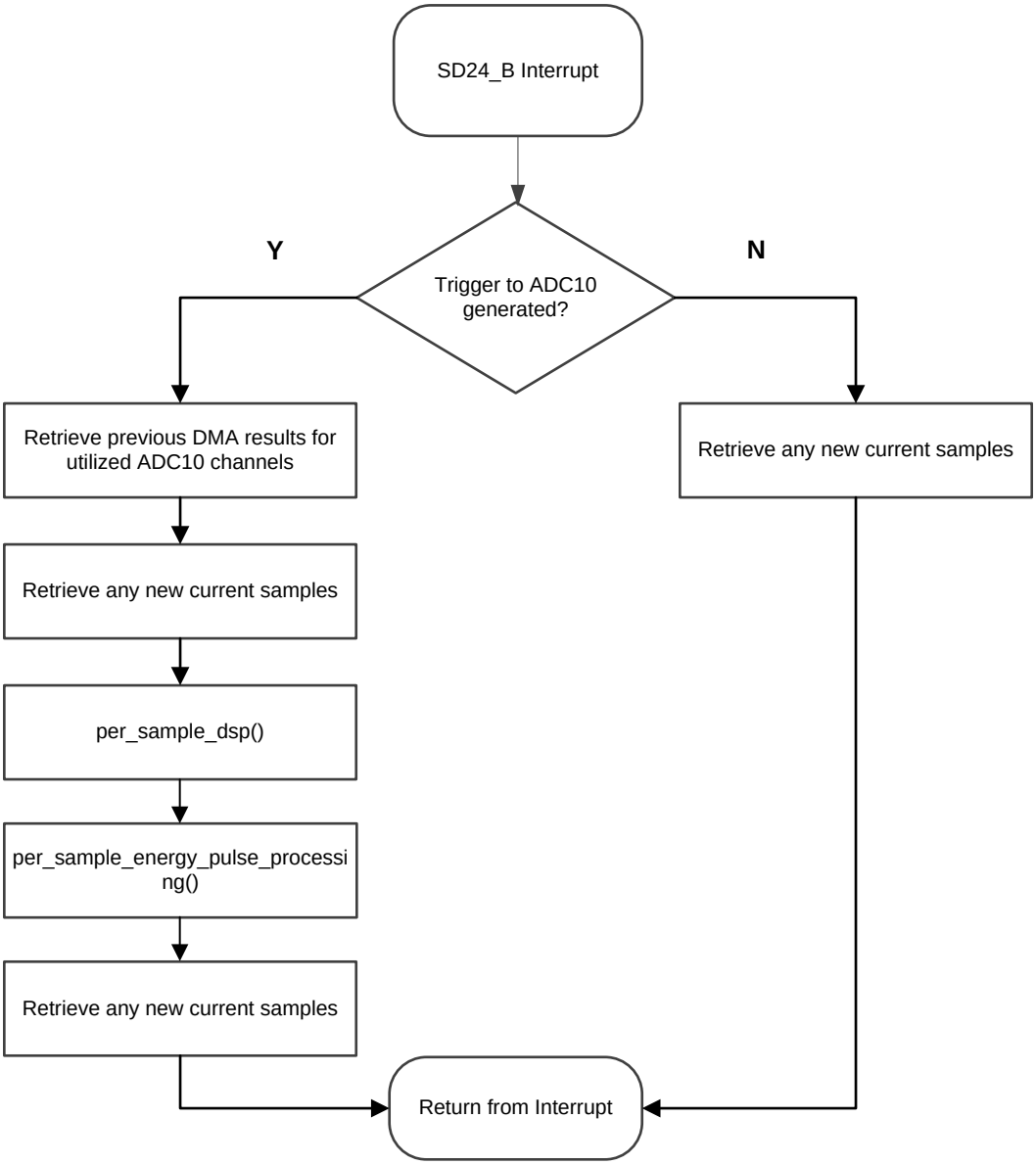


図 13. Background Process

When a trigger is generated, the next set of ADC10 conversions occur in parallel to the activity in the background process. 図 14 shows this parallel activity. In 図 14 the gray containers represent items that are done automatically by the configuration of the ADC10, DMA, and SD24_B modules. For these gray items, CPU intervention is not required.

As 図 14 represents, whenever the ADC10 is triggered, the ADC10 enters autoscan mode and samples all of its 16 ADC channels once. After each channel has a conversion result, the DMA automatically places these results in memory and the next channel's conversion is automatically started. For each converter, there is a memory location that stores the conversion results for that particular converter. The procedure of sampling a converter and storing the results in memory is repeated until the last converter (ADC10INCH = 0) is sampled. Because the clock to the ADC10 is set to 4 MHz, the sample and hold time for each converter is 8 cycles, and the conversion time is 12 cycles, there is an approximate 20-cycle (approximately 5-µs) delay between the conversion results of adjacent converters.

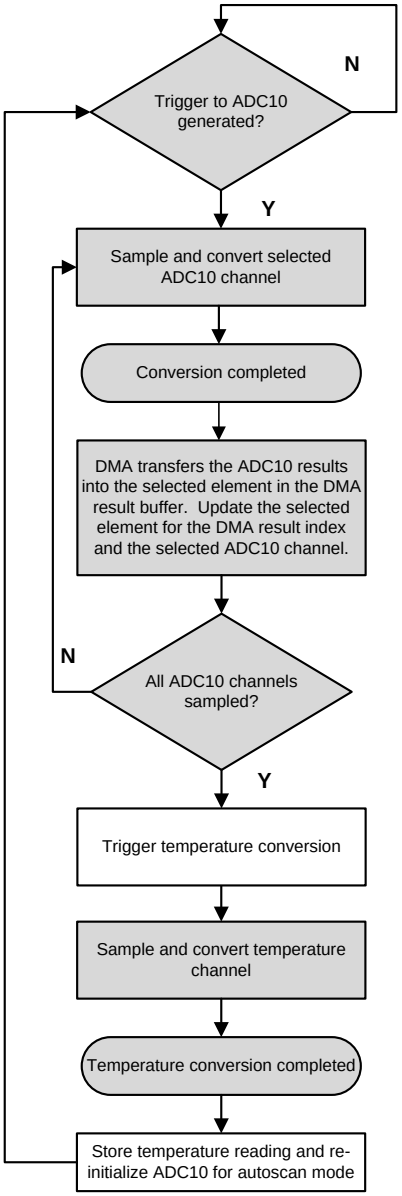


図 14. ADC10 Triggering Process

To sense the internal temperature sensor using the ADC10, a recommended sample period of at least 30 µs must be used. As a result, the temperature reading measured in the autoscan mode may be invalid because the sample time used is not sufficient. To mitigate this, a single conversion of the ADC10 temperature channel is triggered. This is triggered in the DMA ISR when all of the autoscan ADC results have been placed in the proper memory locations. After a temperature reading has been received, the ADC10 ISR is triggered. In this ISR, the temperature reading is stored and the ADC10 settings are then reset to support autoscan mode. The ADC10 enters autoscan mode again at the next trigger from the ΣΔ's trigger generator.

2.2.3.1 per_sample_dsp()

図 15 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. The ADC10 is configured to represent the 10-bit voltage results as a 16-bit signed result. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, as a result of using an OSR of 1024, current samples have more bits. Because many of these bits are unnecessary, they are shifted out so that 24-bit current samples are used. As a result, current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

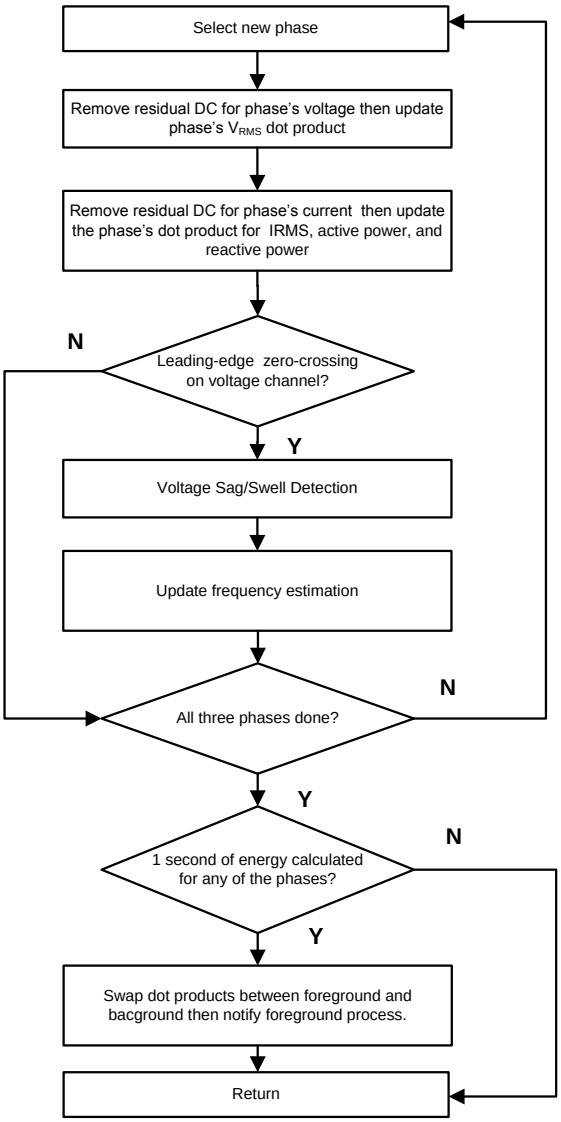


図 15. per_sample_dsp()

After sufficient samples (approximately one second's worth) have been accumulated, the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; and frequency, temperature, and power factor. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products.

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding phase's frequency (in samples per cycle) and voltage sag and swell conditions. For the sag conditions, whenever the RMS voltage is below a certain user-defined threshold percentage, the number of mains cycles where this condition persists is logged as the sag duration. The number of periods in time where there was a sag condition is logged as the sag events count. Note that the sag duration corresponds to the total number of cycles in a sag condition since being reset, and is therefore not cleared for every sag event. Also, when the RMS voltage is above a certain threshold percentage, swell events and duration are logged in a similar way.

The following sections describe the various elements of electricity measurement in the per_sample_dsp() function.

2.2.3.1.1 Voltage and Current Signals

The output of each SD24_B digital filter and ADC10 converter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

2.2.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages are accumulated in a 48-bit register. In contrast, the instantaneous currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one second's worth of samples have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. 図 16 shows the samples near a zero cross and the process of linear interpolation.

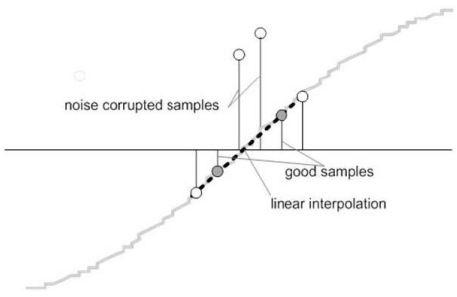


図 16. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

2.2.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP430 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates at every ΣΔ interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The tick is usually defined in pulses per kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh/6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the EVM, the LED is labeled "Active" correspond to the active energy consumption for the cumulative three-phase sum. "Reactive" corresponds to the cumulative three-phase reactive energy sum. The number of pulses per kWh and each pulse duration can be configured in software. 図 17 shows the flow diagram for pulse generation.

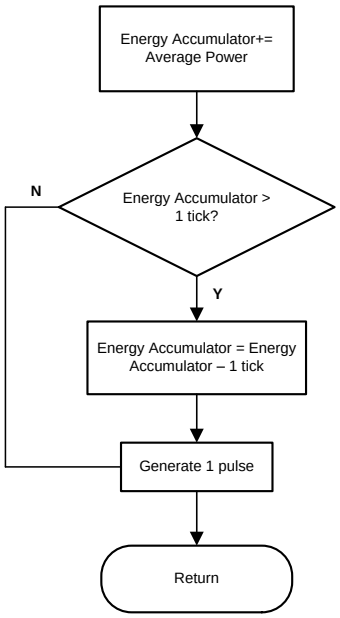


図 17. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

1-kWh threshold = 1 / 0.001 × 1 kW × (Number of interrupts per sec) × (Number of seconds in one hour) = 1000000 × 4915.2 × 3600 = 0x1017DF800000

2.2.3.3 Phase Compensation

In order to ensure accurate measurements, the relative phase shift between voltage and current samples must be compensated. This phase shift may be caused by the passive components of the voltage and current input circuit or even the sequential sampling on the voltage channels. The SD24_B converters have programmable delay registers (SD24PREx) that can be applied to a particular channel.

The fractional delay resolution is a function of input frequency (f_{IN}), OSR, and the sampling frequency (f_s).

$$\text{Delay resolution}_{\text{Deg}} = \frac{360^\circ \times f_{IN}}{OSR \times f_s} = \frac{360^\circ \times f_{IN}}{f_M} \quad (17)$$

In the current application, for an input frequency of 60 Hz, OSR of 1024, and sampling frequency of 4915.2, the resolution for every bit in the pre-load register is about 0.0043° with a maximum of 4.39° (maximum of 1023 steps).

3 Getting Started Hardware and Software

3.1 Hardware

The following figures of the EVM best describe the hardware: 図 18 is the top view of the energy measurement system, and 図 19 shows the location of various pieces of the EVM based on functionality.

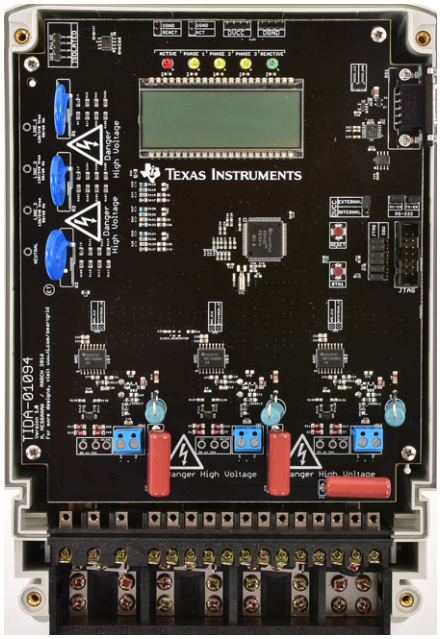


図 18. Top View of TIDA-01094 Design

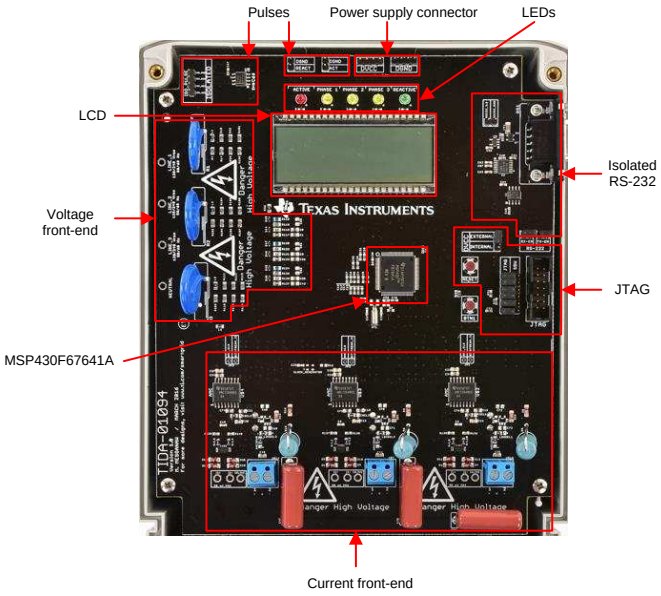


図 19. Top View of TIDA-01094 Design With Components Highlighted

3.1.1 Connections to the Test Setup for AC Voltages

AC voltages can be applied to the board for testing purposes at these points:

- Pad "LINE1" corresponds to the line connection for phase A.
- Pad "LINE2" corresponds to the line connection for phase B.
- Pad "LINE3" corresponds to the line connection for phase C.
- Pad "Neutral" corresponds to the neutral voltage. The voltage between any of the three line connections to the neutral connection must not exceed 230-V AC at 50 and 60 Hz.
- I1+, I1−, and I1Live are connected to the output terminals of the shunt that is used for measuring the current for Phase A. When a shunt is selected, the differential voltage that is output across I1+ and I1− must not exceed 50 mV.
- I2+, I2−, and I2Live are connected to the output terminals of the shunt that is used for measuring the current for Phase B. When a shunt is selected, the differential voltage that is output across I2+ and I2− must not exceed 50 mV.
- I3+, I3−, and I3Live are connected to the output terminals of the shunt that is used for measuring the current for Phase C. When a shunt is selected, the differential voltage that is output across I3+ and I3− must not exceed 50 mV.

図 20 shows a mapping between shunt terminals and I1 (Phase A) current pads. A similar mapping is done between the other shunts and corresponding phases.

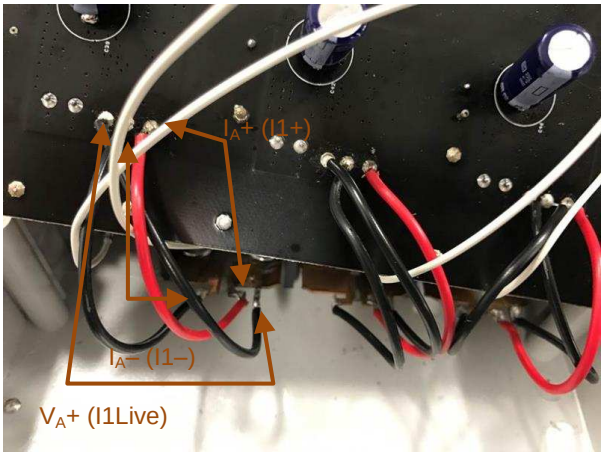


図 20. Mapping Between Shunt Terminals and Ix Current Pads

図 21 through 図 24 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. 図 21 and 図 22 show the connections from the top view if the voltage and current are directly connected and disconnected, respectively, from each other. V_A+, V_B+, and V_C+ correspond to the line voltages for phases A, B, and C, respectively. V_N corresponds to the neutral voltage from the test AC source.

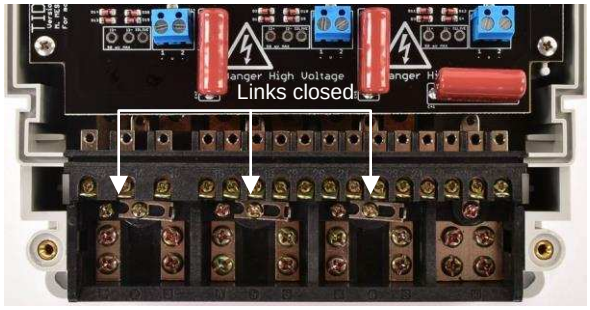


図 21. Top View of EVM With Test Setup Connections With Current and Voltage Connected

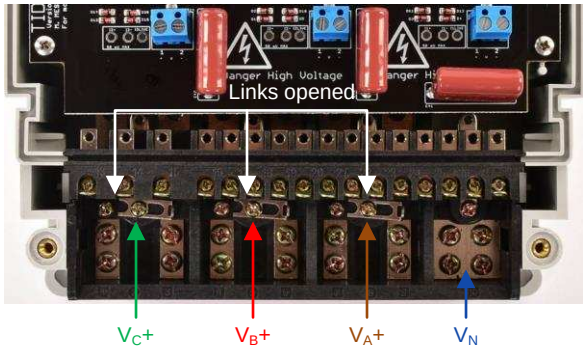


図 22. Top View of EVM With Test Setup Connections With Current and Voltage Disconnected

図 23 and 図 24 shows the connections from the front view if the voltage and current are directly connected and disconnected, respectively, from each other. I_A+ and I_A− correspond to the current inputs for phase A, I_B+, and I_B− correspond to the current inputs for phase B; I_C+ and I_C− correspond to the current inputs for phase C. V_N corresponds to the neutral voltage from the test setup. If the voltage and current are disconnected from each other, note that the IxLive pads must also be externally connected to the corresponding line voltage (this connection must be made in addition to the connection to the line voltage shown already made in 図 22).

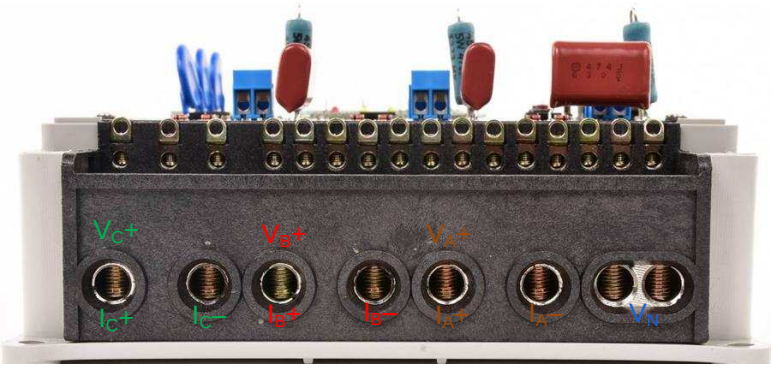


図 23. Front View of EVM With Test Setup Connections With Current and Voltage Connected

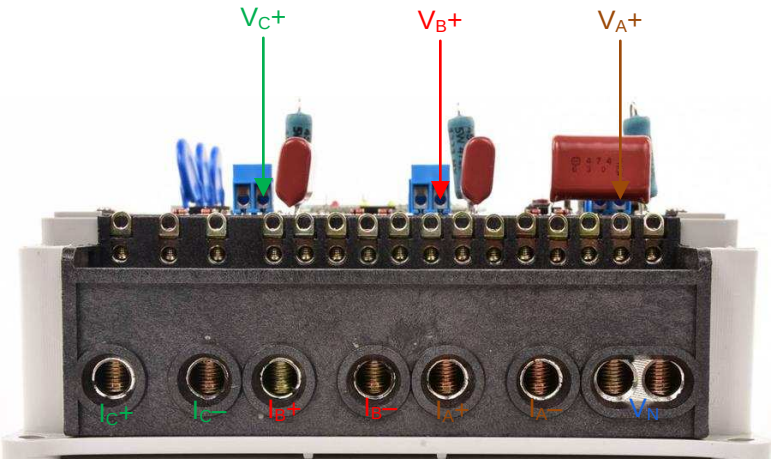


図 24. Front View of EVM With Test Setup Connections With Current and Voltage Disconnected

3.1.2 Power Supply Options and Jumper Settings

The high-side of each AMC is powered from mains. The controller side of the board is powered by a single DC voltage rail (DVCC), which can be derived either by JTAG or external power. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. 表 2 indicates the functionality of each jumper on the board.

表 2. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACT (Not isolated, do not probe)	1-pin header	Active energy pulses (WARNING)	Probe between here and ground for cumulative three-phase active energy pulses.	This header is not isolated from AC voltage, so do not connect measuring equipment unless isolators external to the EVM are available. See Isolated ACT instead.
AMC1PWR	3-pad jumper resistor footprint	Selection for the AMC high-side power supply for Phase A	This header is used to select the power source for the AMC associated with Phase A.	To enable powering the high-side using the onboard cap-drop supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as 図 18 shows). To enable powering the high side by external power, apply voltage directly to the U$16-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as 図 18 shows). For the AMC1304 configuration, the applied voltage should be between 4 to 18 V. In contrast, for the AMC1305 configuration, the applied voltage should be 5 V.
AMC2PWR	3-pad jumper resistor footprint	Selection for the AMC high-side power supply for Phase B	This header is used to select the power source for the AMC associated with Phase B.	To enable powering the high side using the onboard cap-drop power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as 図 18 shows). To enable powering the high side by external power, apply voltage directly to the U$8-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as 図 18 shows). For the AMC1304 configuration, the applied voltage should be between 4 to 18 V. In contrast, for the AMC1305 configuration, the applied voltage should be 5 V.
AMC3PWR	3-pad jumper resistor footprint	Selection for the AMC high-side power supply for Phase C	This header is used to select the power source for the AMC associated with Phase C.	To enable powering the high side using the onboard cap-drop supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as 図 18 shows). To enable powering the high side by external power, apply voltage directly to the U$15-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as 図 18 shows). For the AMC1304 configuration, the applied voltage should be between 4 to 18 V. In contrast, for the AMC1305 configuration, the applied voltage should be 5 V.

表 2. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
AMC_CLK (Not isolated, do not probe)	1-pin header	Modulation clock fed into the AMC	Probe between here and ground for the clock fed into the AMC chips. An external clock can also be fed into this header to be used as the modulation clock; however, the software must be changed to accept a modulation clock input instead of providing one from the SD24_B.	Each AMC has its own associated AMC_CLK header. However, all AMC_CLK headers are connected to each other.
BIT-STREAM_I1 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase A.	Probe between here and ground for the bit-stream output from the AMC chip associated with Phase A.	—
BIT-STREAM_I2 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase B.	Probe between here and ground for the bit-stream output from the AMC chip associated with Phase B.	—
BIT-STREAM_I3 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase C.	Probe between here and ground for the bit-stream output from the AMC chip associated with Phase C.	—
CSEL1	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC for Phase A	This jumper is used to determine whether the power supply should be connected to the AVCC pin(for the AMC1305 configuration) or the LDOIN pin(for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
CSEL2	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC for Phase B	This jumper is used to determine whether the power supply should be connected to the AVCC pin(for the AMC1305 configuration) or the LDOIN pin(for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
CSEL3	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC for Phase C	This jumper is used to determine whether the power supply should be connected to the AVCC pin(for the AMC1305 configuration) or the LDOIN pin(for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
DGND (Not isolated, do not probe)	Header	Ground voltage header (WARNING)	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.

表 2. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
DVCC (Not isolated, do not probe)	Header	VCC voltage header (WARNING)	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.
DVCC EXTERNAL (Do not connect JTAG if AC mains is not isolated)	Jumper header option	JTAG external power selection option (WARNING)	Place a jumper at this header option to select external voltage for JTAG programming.	This jumper option and the DVCC INTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
DVCC INTERNAL (Do not connect JTAG if AC mains is not isolated; isolated JTAG is fine)	Jumper header option	JTAG internal power selection option (WARNING)	Place a jumper at this header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.	This jumper option and the DVCC EXTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
ISO_ACT	1-pin header	Isolated active energy pulses	Probe between here and ground for cumulative three-phase active energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_GND	1-pin header	Isolated ground For energy pulses	Ground connection for the isolated active and reactive energy pulses.	—
ISO_REACT	1-pin header	Isolate reactive energy pulses	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_VCC	1-pin header	Isolated VCC for energy pulses	VCC connection for the isolated active and reactive energy pulses.	Either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce isolated active and reactive pulses on the respective isolated ISO_ACT and ISO_REACT pins. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.

表 2. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
JTAG (Do not connect JTAG if AC mains is not isolated)	Jumper header option	4-wire JTAG programming option (WARNING)	Place jumpers at the JTAG header options of all of the six JTAG communication headers to select 4-wire JTAG.	There are six headers that jumpers must be placed at to select a JTAG communication option. Each of these six headers has a JTAG option and an SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.
LDOSEL1	3-pad jumper resistor footprint	Internal LDO or External LDO Selection for Phase A	This jumper is used to determine whether the external TLV70450 should be enabled(this is needed for the AMC1305 configuration) or if the internal LDO of the AMC1304 is used(this is needed for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
LDOSEL2	3-pad jumper resistor footprint	Internal LDO or External LDO Selection for Phase B	This jumper is used to determine whether the external TLV70450 should be enabled(this is needed for the AMC1305 configuration) or if the internal LDO of the AMC1304 is used(this is needed for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
LDOSEL3	3-pad jumper resistor footprint	Internal LDO or External LDO Selection for Phase C	This jumper is used to determine whether the external TLV70450 should be enabled(this is needed for the AMC1305 configuration) or if the internal LDO of the AMC1304 is used(this is needed for the AMC1304 configuration).	For the AMC1304 configuration, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as 図 18 shows). For the AMC1305 configuration, place a 0-Ω resistor on the two right-most terminals instead.
R16 Resistor	2-pad jumper resistor footprint	External clock generation selection	This design has a footprint that allows placing a clock generator (footprint is labeled CLOCK_GENERATOR on PCB) on the board so that it can be used for the modulation clock. When using this option, populating the clock generator footprint (not populated by default) and placing a 0-Ω resistor at R16 (also not populated by default) connects the clock generator to the AMC and MSP430F67641A.	If the external clock generator is used as the modulation clock of the AMC and MSP430F67641A, the software must be changed for the SD24_B to use an external clock and to prevent outputting the SD24_B clock.

表 2. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
REACT (Not isolated, do not probe)	1-pin header	Reactive energy pulses (WARNING)	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is not isolated from AC voltage so do not connect measuring equipment unless isolators external to the EVM are available. See isolated REACT instead.
RS232_3.3	1-pin header	Voltage source harvested from RS-232 line	Voltage source that is used to power the TRS3232 and ISO7321 for isolated RS-232 communication. This voltage source is harvested from the RS-232 line.	—
RS232_GND	1-pin header	Ground connection for the isolated RS-232	Ground connection for the isolated RS-232 circuitry.	—
RX_EN	Jumper header	RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232.	—
SBW (Do not connect JTAG if AC mains is not isolated)	Jumper header option	SBW JTAG programming option (WARNING)	Place jumpers at the SBW header options of all of the six JTAG communication headers to select SBW.	There are six headers that jumpers must be placed at to select a JTAG communication. Each of these six headers that have a JTAG option and a SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.
TX_EN	Jumper header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	—

3.2 Software

The source code is developed in the IAR™ environment using IAR compiler version 6.x. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the integrated development environment (IDE) prompts the user to create a backup. Click "YES" to proceed. There are four main parts to the energy metrology software:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for the host-processor functionality of the system (that is, communication, LCD display, RTC setup, and so forth)
- The GUI that is used for calibration

図 25 shows the contents of the source folder.

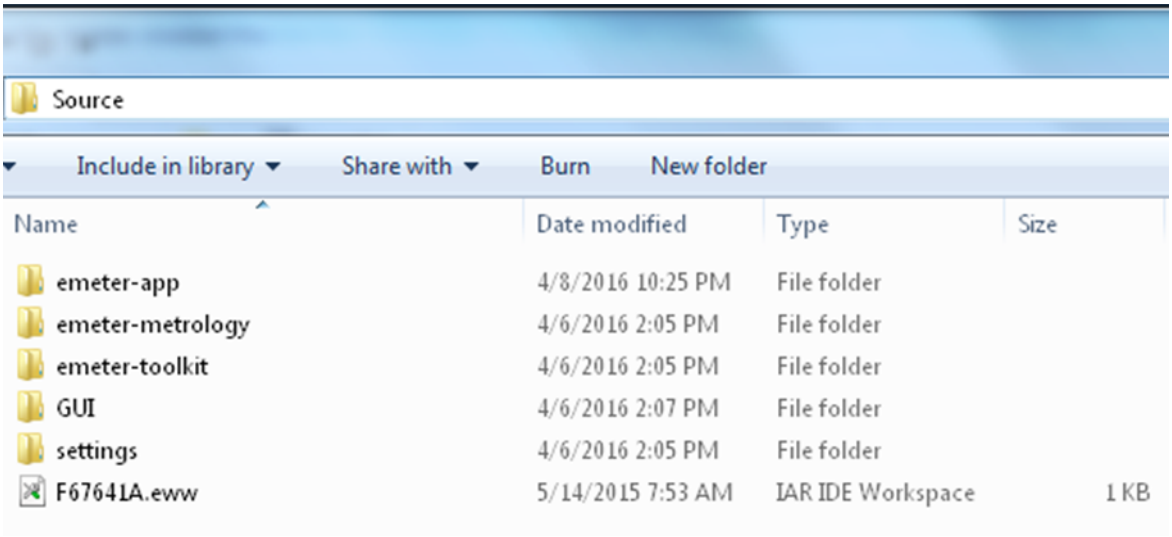


図 25. Source Folder Structure

Within the *emeter-app-67641A* folder in the *emeter-app* folder, the *emeter-app-67641A.ewp* project corresponds to the application code. Similarly, within the *emeter-metrology-67641A* folder in the *emeter-metrology* folder, the *emeter-metrology-67641A.ewp* project corresponds to the portion of the code for metrology. Additionally, the folder *emeter-toolkit-67641A* within the *emeter-toolkit* has the corresponding toolkit project file *emeter-toolkit-67641A.ewp*. For first-time use, TI recommends that all three projects be completely rebuild by performing the following steps:

1. Open the IAR IDE.
2. Open the F67641A workspace, which is located in the *Source* folder.
3. Within IARs workspace window, click the *Overview* tab to have a list view of all the projects.
4. Right-click the *emeter-toolkit-67641A* option in the workspace window and select *Rebuild All*, as 図 26 shows.
5. Right-click the *emeter-metrology-67641A* option in the workspace window and select *Rebuild All*, as 図 27 shows.
6. Within IARs workspace window, click the *emeter-app-67641A* tab.
7. Within the workspace window, select *emeter-app-67641A*, click *Rebuild All* as 図 28 shows, and then download this project onto the MSP430F67641A device.

Note that if any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

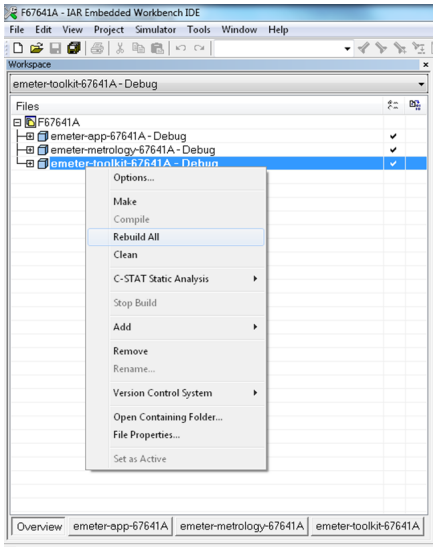


図 26. Toolkit Project Compilation

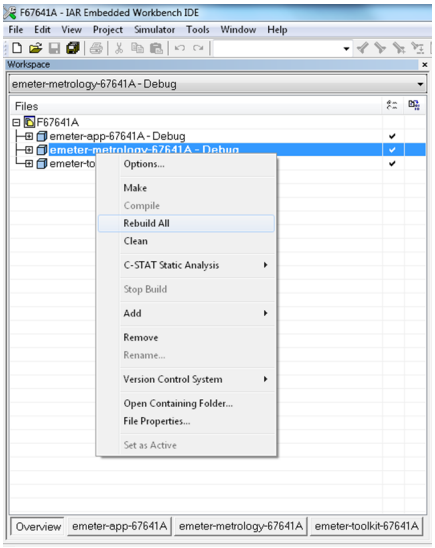


図 27. Metrology Project Compilation

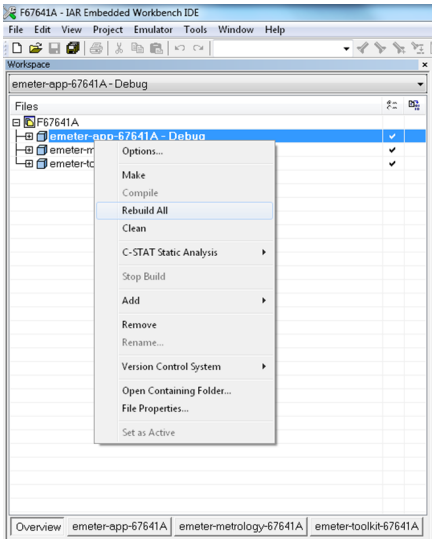


図 28. Application Project Compilation

4 Testing and Results

4.1 Test Setup

For performing metrology testing, a source generator was used to provide the voltages and currents to the system at the proper locations mentioned in 3.1.1. Additionally, a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz were used for each phase.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this TI Design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active and reactive energy output pulse. In the TIDA-01094, cumulative active energy error testing, cumulative reactive energy error testing, voltage variation testing, and frequency variation testing were performed.

For cumulative active energy error and cumulative reactive energy error testing, current was varied from 100 mA to 90 A simultaneously at each phase. For cumulative active energy error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current channels. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used and cumulative reactive energy error is plotted instead of cumulative active energy error.

In performing metrology tests, two sets of voltage tests were also performed. In the first test, the 230-V nominal voltage was varied by ±10% at different currents and power factors. The resulting active energy error at each test point was then logged. For the second test, the active energy error was plotted when voltage was varied over a larger voltage range at unity power factor. Specifically, voltage was varied from 75 to 270 V. Testing beyond 270 V can also be done; however, this requires the 275-V varistors to be removed from the design and replaced with varistors that are rated for a higher voltage.

Another set of tests that were performed were frequency variation tests. For this test, the frequency is varied by ±2 Hertz from its 50-Hz nominal frequency. This test was conducted at 1.5 A and 15 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error was logged.

4.2 Viewing Metrology Readings and Calibration

4.2.1 Viewing Results from LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. 図 29, 図 30, and 図 31 show the mapping between the different orientations of the triangle and the phase descriptor:

図 29. Symbol for Phase A

図 30. Symbol for Phase B

図 31. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. 表 3 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

表 3. Displayed Parameters

PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power	AcPo	Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power	rEPo	Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power	APPo	Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor	PF	Constant between 0 and 1	This parameter is displayed for each phase.
Voltage	Vrms	Volts (V)	This parameter is displayed for each phase.
Current	Irms	Amps (A)	This parameter is displayed for each phase.
Frequency	Fr89	Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy	AcEn	kWh	This parameter is displayed for each phase.
Total consumed reactive energy	rEEn	kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time	t inE	Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date	dAtE	Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

図 32 shows an example of phase Bs measured frequency of 49.99 Hz displayed on the LCD.

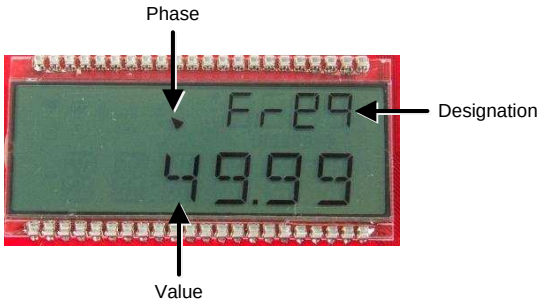


図 32. LCD Display

4.2.2 Calibrating and Viewing Results From PC

4.2.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As 図 33 shows, this field is changed to *COM7*.

```
260      </correction>
261    </phase>
262    <temperature/>
263    <rtc/>
264  </cal-defaults>
265  <meter position="1">
266    <port name="com7" speed="9600"/>
267  </meter>
268  <reference-meter>
269    <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270    <type id="chroma-66202"/>
271    <log requests="on" responses="on"/>
272    <scaling voltage="1.0" current="1.0"/>
273  </reference-meter>
```

図 33. GUI Configuration File Changed to Communicate With Energy Measurement System

4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the EVM, the GUI opens (see 図 34). If the GUI connects properly to the EVM, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

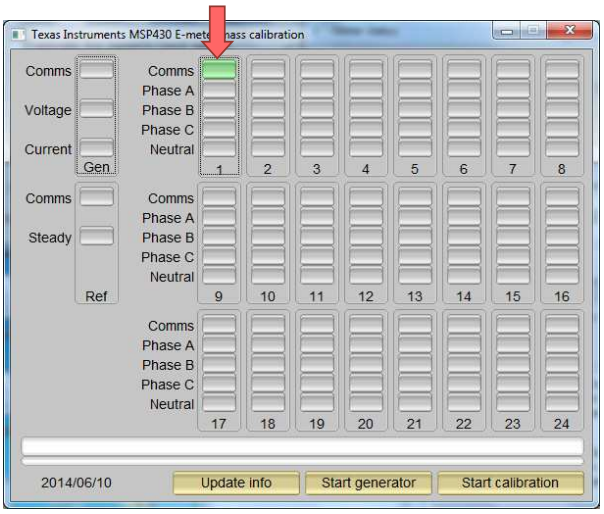


図 34. GUI Startup Window

Upon clicking on the green button, the results window opens (see 図 35). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

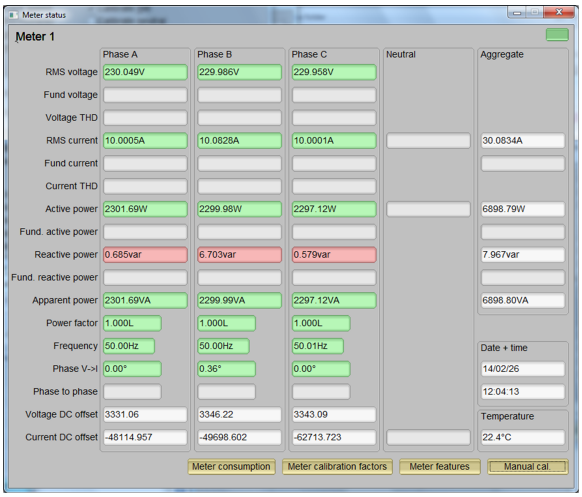


図 35. GUI Results Window

From the results window, the total-energy consumption readings and sag/swell logs can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as 図 36 shows.

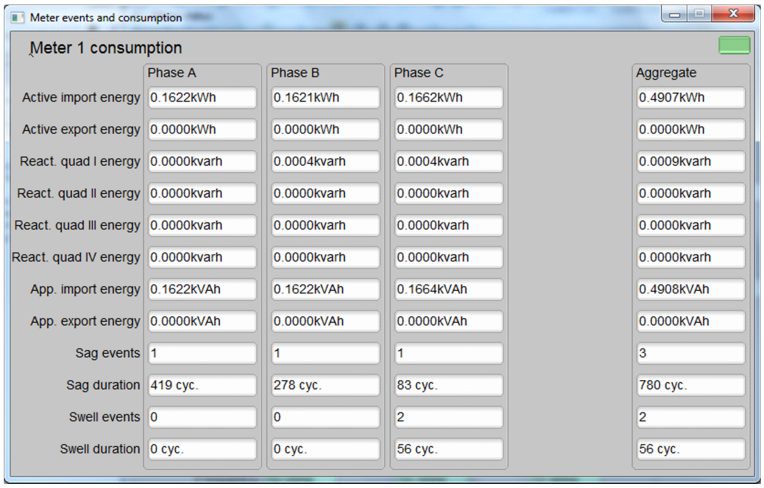


図 36. Meter Events and Consumption Window

From this *Meter events and consumption* window, the user can view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

4.2.2.2 Calibration

Calibration is key to any meter performance and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, voltage AC offset, current scaling factor, current AC offset, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Please note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed with the code (available in the *.*zip* file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted. However, if the code is re-flashed during debugging, the calibration factors are replaced and the meter has to be recalibrated. One way to save the calibration values is by clicking on the *Meter calibration factors* button (see 図 35). The *Meter calibration factors* window (see 図 37) displays the latest values, which can be used to restore calibration values.

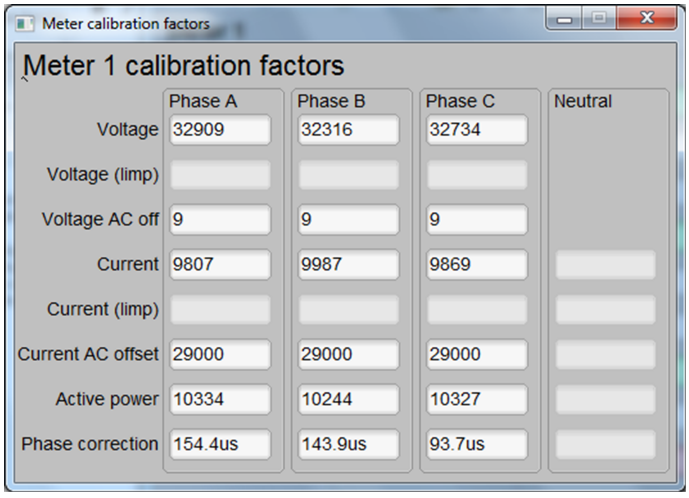


図 37. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with 3.1.1, and the energy pulses connected to the reference meter.

4.2.2.2.1 Gain Calibration

Usually gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other two phases must be turned OFF. Typically, switching only the currents OFF is good enough for disabling a phase.

4.2.2.2.1.1 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 230 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that 図 35 shows. The following screen pops up from 図 38:

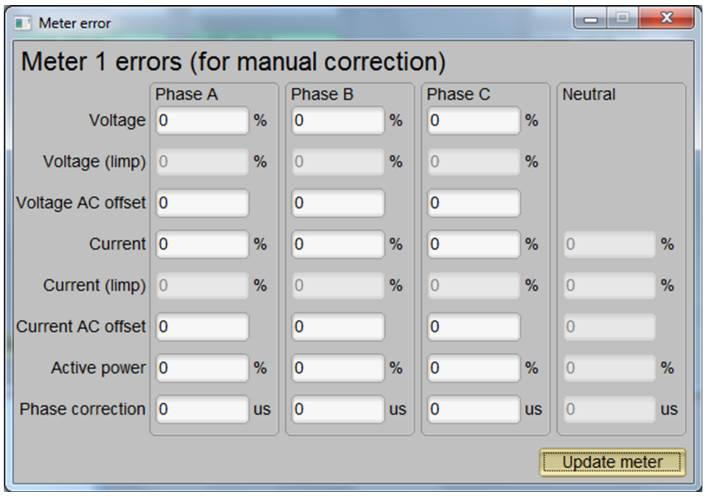


図 38. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (18)$$

where:

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

4.2.2.2.1.2 Active Power Gain Calibration

Note that this an example is for one phase. Repeat these steps for other phases.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating using Step 4 with active power readings (displayed on the AC test source) can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, perform the following steps.

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source
3. Repeat Step 1 to Step 3 from 4.2.2.2.1.1 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

4.2.2.2.2 Phase Correction

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 1 through Step 3 from 4.2.2.2.1.1 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If the error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   (a) Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error would require a positive (negative) number as correction.
   (b) Click on the *Update meter* button and monitor the error values on the reference meter.
   (c) If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Please note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   (d) Change the phase now to −60° and check if this error is still acceptable. Ideally, errors should be symmetric for same phase shift on lag and lead conditions.

After performing phase correction, calibration is complete for one phase. Note that the gain calibration and phase calibration are completed in sequence for each phase before moving on to other phases. These two procedures must be repeated for each phase, unlike voltage and current calibration.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see 図 39) by clicking the *Meter calibration factors* button of the GUI metering results window in 図 35.

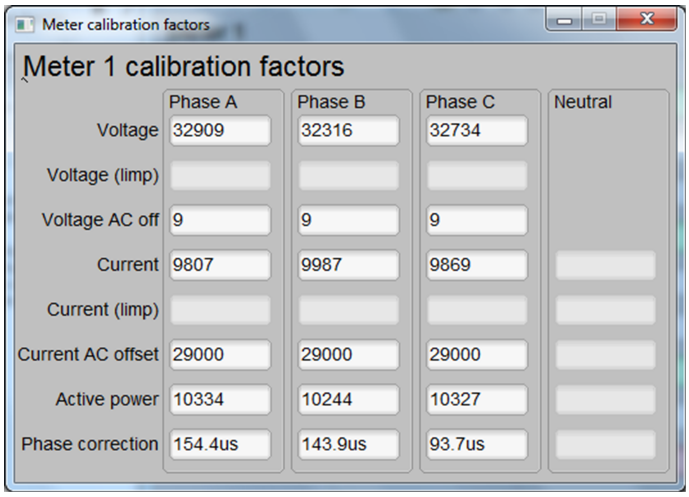


図 39. Calibration Factors Window

Also view the configuration of the system by clicking on the *Meter features* button in 図 35 to get to the window that 図 40 shows.

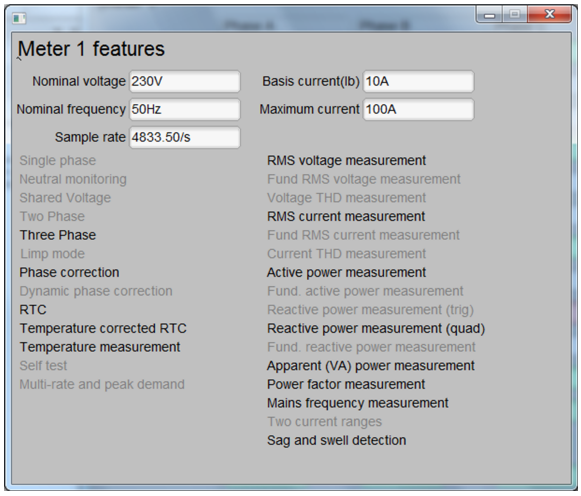


図 40. Meter Features Window

4.3 Test Data

表 4. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.10	0.0130	0.1580	0.1200
0.25	–0.0020	0.0580	0.0320
0.50	–0.0230	0.0200	–0.0085
1.00	–0.0223	0.0010	–0.0260
2.00	–0.0380	–0.0110	–0.0520
5.00	–0.0300	–0.0180	–0.0360
10.00	–0.0270	–0.0195	–0.0350
20.00	–0.0250	–0.0085	–0.0383
30.00	–0.0307	–0.0190	–0.0500
40.00	–0.0410	–0.0380	–0.0840
50.00	–0.0790	–0.0810	–0.1100
60.00	–0.0960	–0.1130	–0.1430
70.00	–0.1320	–0.1530	–0.1810
80.00.	–0.1700	–0.1900	–0.2220
90.00	–0.2100	–0.2340	–0.2730

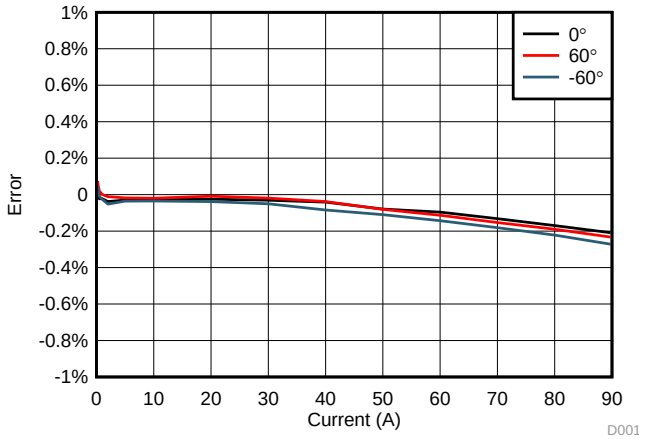


図 41. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

表 5. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.10	0.1230	0.3540	0.4917
0.25	0.0720	0.1500	0.2570
0.50	0.0347	0.0780	0.1357
1.00	0.0190	0.0250	0.0820
2.00	–0.0067	–0.0017	0.0320
5.00	–0.0030	–0.0250	0.0340
10.00	0.0025	–0.0193	0.0290
20.00	–0.0020	–0.0220	0.0100
30.00	0.0027	–0.0170	0.0140
40.00	–0.0037	–0.0260	–0.0037
50.00	–0.0247	–0.0670	–0.0140
60.00	–0.0410	–0.0800	–0.0390
70.00	–0.0510	–0.1060	–0.0690
80.00	–0.0933	–0.1560	–0.1220
90.00	–0.1490	–0.2000	–0.1830

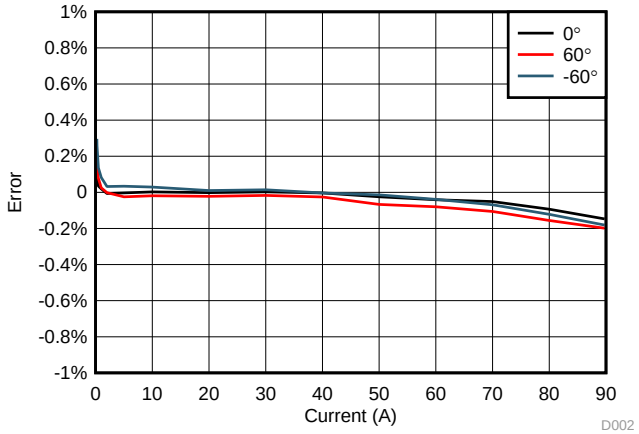


図 42. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

表 6. Cumulative Reactive Energy % Error Versus Current

CURRENT (A)	30°	60°	–30°	–60°
0.10	0.3010	0.1330	–0.5440	–0.3380
0.25	–0.0887	–0.0630	–0.0487	–0.0580
1.00	–0.0545	–0.0457	–0.0393	–0.0470
5.00	–0.0487	–0.0370	–0.0260	–0.0410
10.00	–0.0380	–0.0267	–0.0133	–0.0177
30.00	–0.0520	–0.0390	–0.0030	–0.0185
50.00	–0.0597	–0.0667	–0.0650	–0.0700
70.00	–0.1130	–0.1270	–0.1150	–0.1390
90.00	–0.1730	–0.2000	–0.2080	–0.2240

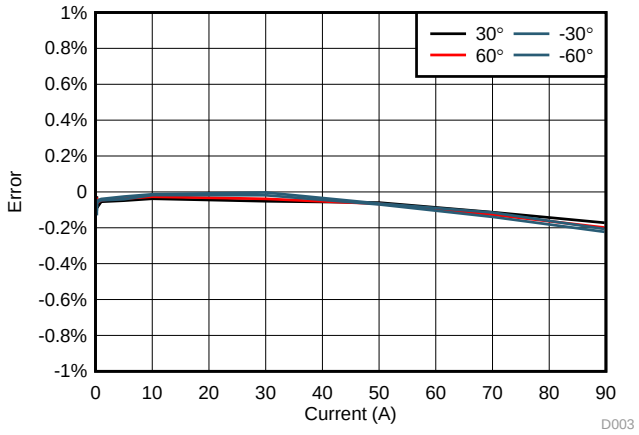


図 43. Cumulative Reactive Energy % Error Versus Current

表 7. Cumulative Active Energy Measurement Error Versus Voltage, 75 to 270 V

VOLTAGE (V)	%ERROR
75	0.0750
100	–0.0620
110	–0.0610
120	–0.1130
150	–0.1000
180	–0.0540
210	–0.0517
220	–0.0400
230	–0.0310
240	–0.0113
250	–0.0210
260	–0.0257
265	–0.0300
270	–0.0340

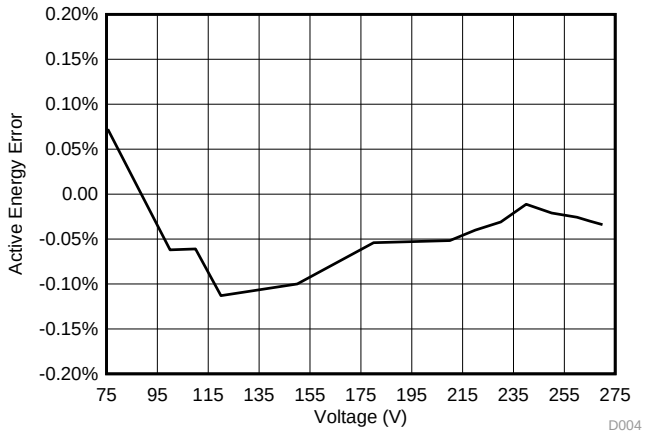


図 44. Cumulative Active Energy Measurement Error Versus Voltage, 57.5 to 270 V

表 8. Cumulative Active Energy Measurement Error Versus Voltage, ±10% Nominal Voltage

VOLTAGE (V)	0°, 15 A	60°, 15 A	300°, 15 A	0°, 1.5 A	60°, 1.5 A	300°, 1.5 A
207	–0.062	–0.0370	–0.0705	–0.0637	–0.039	–0.081
230	–0.031	–0.0203	–0.0560	–0.0367	–0.006	–0.053
253	–0.133	0.0157	–0.0410	–0.0177	0.013	–0.031

表 9. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	48 Hz	50 Hz	52 Hz
1.5 A, 0	–0.0425	–0.0367	–0.0477
1.5 A, 60	–0.0120	–0.0060	–0.0137
1.5 A, 300	–0.0373	–0.0530	–0.0617
15 A, 0	–0.0340	–0.0310	–0.0380
15 A, 60	–0.0070	–0.0203	–0.0063
15 A, 300	–0.0500	–0.0560	–0.0600

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01094.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01094.

5.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially for the ground planes of the high side of each AMC. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Give each AMC its own set of ground planes that are used for the high side of each AMC. Each of these ground planes is actually referenced from a different line voltage because each AMC must be connected to a different line voltage.
- Use a different ground plane for the isolated RS-232. This other ground plane is at the potential of the RS-232 ground and not DGND.
- Be careful to avoid crosstalk from the delta-sigma modulation clock traces or the AMC bit-stream traces.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high frequency signals away from the crystal.
- Use wide traces for power supply connections.
- Maintain at least an 8.1-mm spacing between the ground planes of the high side of each AMC device and the ground plane on the controller side. This spacing maintains the recommended clearance for the AMC isolation rating. In addition, ensure that the recommended clearance and creepage spacing for other isolation devices (such as the ISO7320 and ISO7321) is also followed.
- Keep the traces of the analog input pin symmetrical and as close as possible to each other.

5.4 CAD Project

To download the Altium project files, see the design files at TIDA-01094.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01094.

6 Software Files

To download the software files, see the design files at TIDA-01094.

7 Related Documentation

1. Texas Instruments, *Isolated, Shunt-Based Current Sensing Reference Design*, TIPD165 Design Guide (TIDU384)
2. Texas Instruments, *Self-Powered Isolated RS-232 to UART Interface*, TIDA-00163 Design Guide (TIDU298)
3. Texas Instruments, *Implementation of a Low-Cost Three-Phase Electronic Watt-Hour Meter Using the MSP430F67641*, MSP430F67641 Application Report (SLAA621)

7.1 商標

8 About the Author

MEKRE MESGANAW is a systems engineer in the Grid Infrastructure group at Texas Instruments, where he primarily works on grid monitoring and electricity metering customer support and reference design development. Mekre received his bachelor of science and master of science in computer engineering from the Georgia Institute of Technology.

リビジョンAの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年12月発行のものから更新 **Page**

- 現行のスタイルガイドに合わせて文章と画像を 変更 1

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。