参考資料

TI Designsリファレンス・デザイン
PLC用デュアル構成チャネル相互間絶縁型ユニバーサル・アナログ入力モジュールのリファレンス・デザイン

TEXAS INSTRUMENTS

TI Designsリファレンス・デザイン

このプログラマブル・ロジック・コントローラ (PLC)に適したデュアル構成のチャネル相互間絶縁型ユニバーサル・アナログ入力モジュールのリファレンス・デザインは、高い精度とフレキシビリティを両立しています。電圧と電流の両方を測定でき、熱電対、RTD、4～20mAのループをサポートしています。高密度のユニバーサル・マルチチャネル・モジュールで、チャネルごとに4つの入力端子しか必要としません。

設計リソース

TIDA-00550	デザイン・フォルダ
TIDA-00549	ツール・フォルダ
ADS1262	プロダクト・フォルダ
LMT01	プロダクト・フォルダ
LM5017	プロダクト・フォルダ
LM2903	プロダクト・フォルダ
TPS7A4901	プロダクト・フォルダ
TPS7A3001	プロダクト・フォルダ
TPS7A4101	プロダクト・フォルダ
TLV70433	プロダクト・フォルダ
TPS61093	プロダクト・フォルダ

TI E2E™ Community

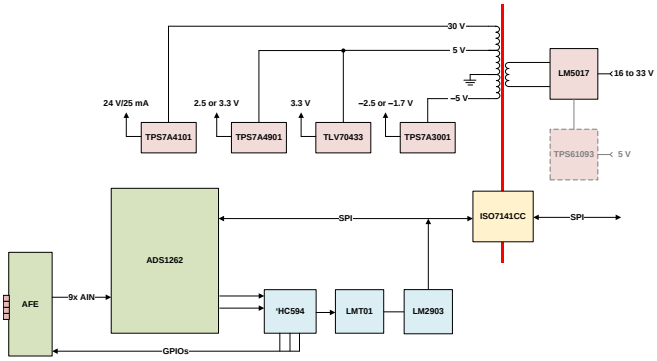
E2Eエキスパートに質問

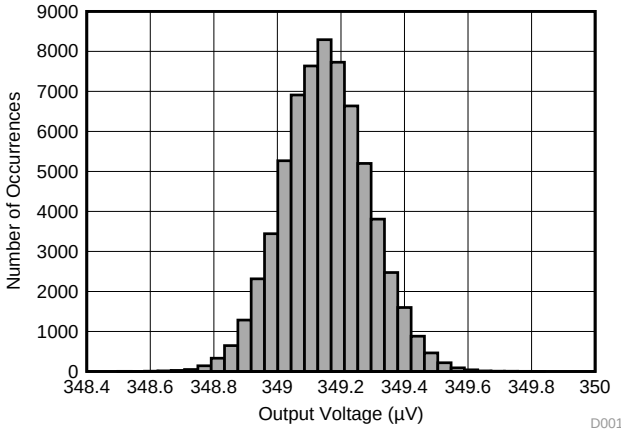
デザインの特長

- 最高±12Vの測定
- 最大±55mAの電流測定
- 熱電対と2、3、4線式RTDのサポート
- 4～20mAのループ電源
- パッシブ・アナログ・フロントエンド
- 最大1kHzのアナログ帯域幅
- 27.4Ωの小さな負荷抵抗
- 精度:
  - < 0.002% (25℃)
  - < 0.05% (-35℃～85℃)
- 50Hzと60Hzを同時に除去
- IEC61000-4-5 class II (±1kV、42Ω時)
- HART対応(TIDA-00549プラグイン基板が必要)

主なアプリケーション

- PLC用のマルチチャネル絶縁型アナログ入力モジュール





1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATION				DETAILS
Number isolated of channels	2				—
Operating voltage	Primary input (J2)		Secondary input (BeagleBone)		3.7
Ranges	16 to 33 V		5 V		3.7
Power consumption per channel	400 mW				3.7
Operating modes	High-voltage measurement				3.1, 4.1
	Low-voltage measurement				3.1, 4.2
	Current measurement				3.1, 4.3
	4- to 20-mA loop				3.1, 3.7.4, 4.4, 4.7
	Thermocouple with cold-junction compensation				3.3, 4.5
	2-, 3-, and 4-wire RTD Measurement				3.9, 4.6
Analog inputs	Voltage, HV	Voltage, SE	Voltage, DIFF	Current	—
Ranges	±12.39 V	±2.20 V	±1.25 V	±55 mA	3.1, 3.10
		±1.25 V	±0.62 V	±45 mA	
		±0.62 V	±0.31 V	±22 mA	
		±0.31 V	±0.15 V	±11 mA	
		±0.15 V	±0.07 V	±5.5 mA	
		±0.07 V	±0.03 V	±2.7 mA	
Input impedance	100 kΩ	~1 GΩ	~1 GΩ	43 Ω	3.1
Input accuracy					—
25°C	±0.001%	±0.0006%	±0.0006%	±0.002%	3.10
–35°C to 85°C	±0.035%	±0.05%	±0.05%	±0.05%	3.10
Loop power supply	Min. 24-V DC (0 to 25 mA)				3.7.4, 4.7
Thermocouple accuracy (25°C)	±0.7°C				4.5
RTD (3-wire) accuracy (25°C)	±0.07°C				4.6
Signaling	Four LEDs at terminal inputs				3.4
Surge transient immunity	EN 61000-4-5 class 2 (±1 kV, 24 A)				3.8
Operating temperature	–40°C to 85°C				2
Storage temperature	–40°C to 125°C				—
Form factor					—
Each channel	93 × 27 mm (3.66 × 1.06 in)				—
Entire board	159 × 55 mm (6.26 × 2.17 in)				—
HART communication	Supported by TIDA-00549				3.10

2 System Description

The TIDA-00550 universal analog input module is a versatile dual channel-to-channel isolated low-input terminal count, high-performance design. It includes a high-voltage, low-voltage, and current measurement signal path. The high-voltage path can be used in parallel with the low-voltage or current path. Temperature sensors such as resistance temperature detectors (RTDs) and thermocouples (TC), including cold-junction compensation (CJC), can be directly connected to the terminal pins. In addition, the 4- to 20-mA loop supports remote sensor transmitters without an additional power supply. The TI Design TIDA-00549 can be used to add HART communication to the 4- to 20-mA loop.

The passive analog front-end (AFE) avoids distortion of the measurement signal. Noise from active components such as op amps, which are used in comparable designs, is therefore eliminated. This BeagleBone Cape (1) compatible design can be powered either from an external PLC power supply (16 to 33 V) or directly from the BeagleBone Black (5 V).

Each channel uses only four isolated channels, all dedicated to the digital interface (SPI). The general output pins (GPO) required for the mode switching are provided by the analog-to-digital converter (ADC) itself. The data stream of the local temperature sensor for the cold junction compensation shares the same SPI isolator as the ADC.

The four terminal input pins can withstand 33 V continuously (important in the event of wrong wiring of the PLC supply voltage) and are immune to EN61000-4-5 class 2 (±1 kV at 24 A). The four blue signaling LED visible at the terminal inputs allows fast discovery of the selected mode of the particular channel.

The isolated switches and the TPS61093 support a temperature range of –40°C to 85°C. All other devices can operate in the extended temperature range of -40°C to 125°C. The TPS61093 has only a supporting function here (transforming the BeagleBone voltage to 16.5 V) and is not an integral part of the design.

The board includes two exact same channels. The AM3359 (2) Sitara processor on the BeagleBone board distinguishes the two channels by two separate chip select signals, CS0 and CS1. The block diagram in 図 1 shows one channel only. The functionality of the devices is described in the following sections.

(1) See the System Reference Manual at https://github.com/CircuitCo/BeagleBone-Black/blob/master/BBB_SRM.pdf?raw=true
(2) See the product folder at http://www.ti.com/product/AM3359

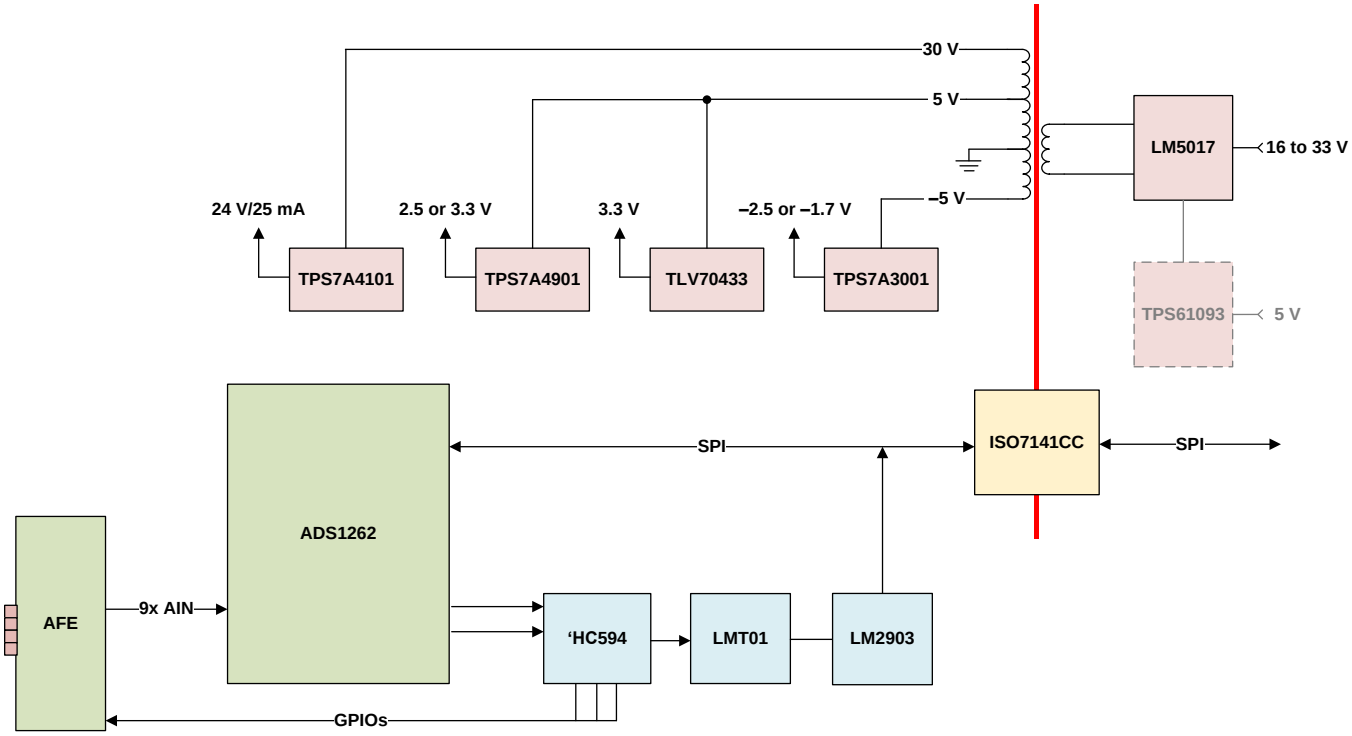


図 1. Block Diagram (One Channel)

To get familiar with the physical board, 図 2 describes the interfacing components of the design.

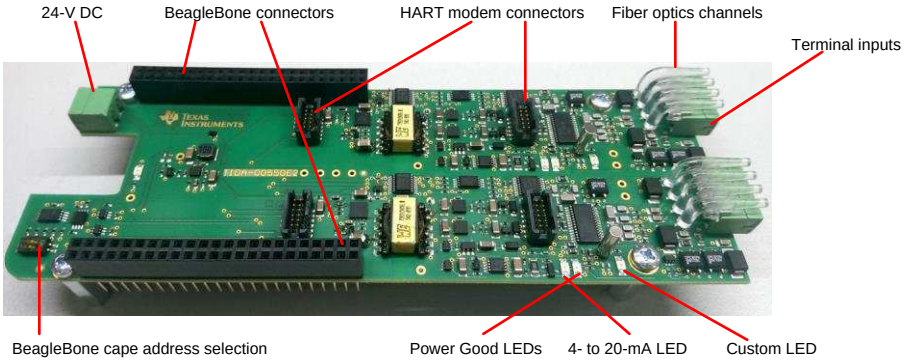


図 2. Physical Board

2.1 Highlighted Products

2.1.1 ADS1262

The ADS1262 is a low-noise, low-drift, 38.4-kSPS, delta-sigma (ΔΣ) ADC with an integrated PGA, reference, and internal fault monitors. The sensor-ready ADC provides complete, high-accuracy, one-chip measurement solutions for the most demanding sensor applications, including weigh scales, strain-gauge sensors, TCs, and RTDs.

The ADCs are comprised of a low-noise, CMOS PGA (gains 1 to 32), a ΔΣ modulator, followed by a programmable digital filter. The flexible AFE incorporates two sensor-excitation current sources suitable for direct RTD measurement. A single-cycle settling digital filter maximizes multiple-input conversion throughput, while providing 130-dB rejection of 50- and 60-Hz line cycle interference.

The ADS1262 is available in a 28-pin TSSOP package and fully specified over the –40°C to 125°C temperature range.

2.1.2 ISO7141CC

The ISO7141CC provides galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. The ISO7141CC is a quad-channel isolator with three forward and one reverse-direction channels. This device is capable of 50-Mbps maximum data rate with a 5-V supply and 40-Mbps maximum data rate with a 2.7- or 3.3-V supply, with integrated filters on the inputs for noise-prone applications. The suffix CC states the default output state is high.

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7-, 3.3-, and 5-V supplies. All inputs are 5-V tolerant when supplied from a 2.7- or 3.3-V supply.

2.1.3 LMT01

The LMT01 is a high-accuracy, 2-pin temperature sensor with an easy-to-use pulse count interface, which makes it an ideal digital replacement for PTC or NTC thermistors both on and off board in automotive, industrial, and consumer markets. The LMT01 digital pulse count output and high accuracy over a wide temperature range allow pairing with any MCU without concern for integrated ADC quality or availability while minimizing software overhead. TI's LMT01 achieves a flat ±0.5°C accuracy with very fine resolution (0.0625°C) over a wide temperature range of –20°C to 90°C without system calibration or hardware or software compensation.

Unlike other digital IC temperature sensors, the LMT01's single-wire interface is designed to directly interface with a GPIO or comparator input, thereby simplifying hardware implementation. Similarly, the LMT01's integrated EMI suppression and simple 2-pin architecture make it ideal for onboard and off-board temperature sensing. The LMT01 offers all the simplicity of analog NTC or PTC thermistors with the added benefits of a digital interface, wide specified performance, EMI immunity, and minimum processor resources.

2.1.4 LM5017

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

2.1.5 LM2903

The LM2903 consists of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 V to 36 V, and VCC is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

2.1.6 TPS7A4901

The TPS7A49 series of devices are positive, high-voltage (36 V), ultralow-noise (15.4-μV_{RMS}, 72-dB PSRR) linear regulators that can source a 150-mA load.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other available features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49 family is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, ADCs, digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

2.1.7 TPS7A3001

The TPS7A30 series of devices are negative, high-voltage (–35 V), ultralow-noise (15.1-μV_{RMS}, 72-dB PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

2.1.8 TPS7A4101

The TPS7A41 is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8) and is able to withstand continuous DC or transient input voltages of up to 50 V.

The TPS7A41 is stable with any output capacitance greater than 4.7 μF and any input capacitance greater than 1 μF (over temperature and tolerance). Thus, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A41 offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

The TPS7A41 has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 packages has an operating temperature range of T_J = –40°C to 125°C. In addition, the TPS7A41 is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only can it supply a well-regulated voltage rail, but it can also withstand and maintain regulation during very high and fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications.

2.1.9 TLV70433

The TLV704 series of low-dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range.

The TLV704 operates over a wide operating input voltage of 2.5 to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients.

2.1.10 TPS61093

The TPS61093 is a 1.2-MHz, fixed-frequency boost converter designed for high integration and high reliability. The IC integrates a 20-V power switch, I/O isolation switch, and power diode. When the output current exceeds the overload limit, the isolation switch of the IC opens up to disconnect the output from the input, thus protecting the IC and the input supply. The isolation switch also disconnects the output from the input during shutdown to minimize leakage current. When the IC is shut down, the output capacitor is discharged to a low voltage level by internal diodes. Other protection features include 1.1-A peak overcurrent protection (OCP) at each cycle, output overvoltage protection (OVP), thermal shutdown, and UVLO. The output can be boosted up to 17 V.

3 System Design Theory

3.1 AFE

The ADS1262 is a high-performance 32-bit ΔΣ ADC. This keeps the attached AFE simple and cost-effective. The built-in PGA is able to scale the analog input signal 1×, 2×, 4×, 8×, 16×, or 32× to use the entire ADC measurement range. The AFE (see 図 3) has three independent input paths:

- High-voltage input
- Low-voltage input
- Current input

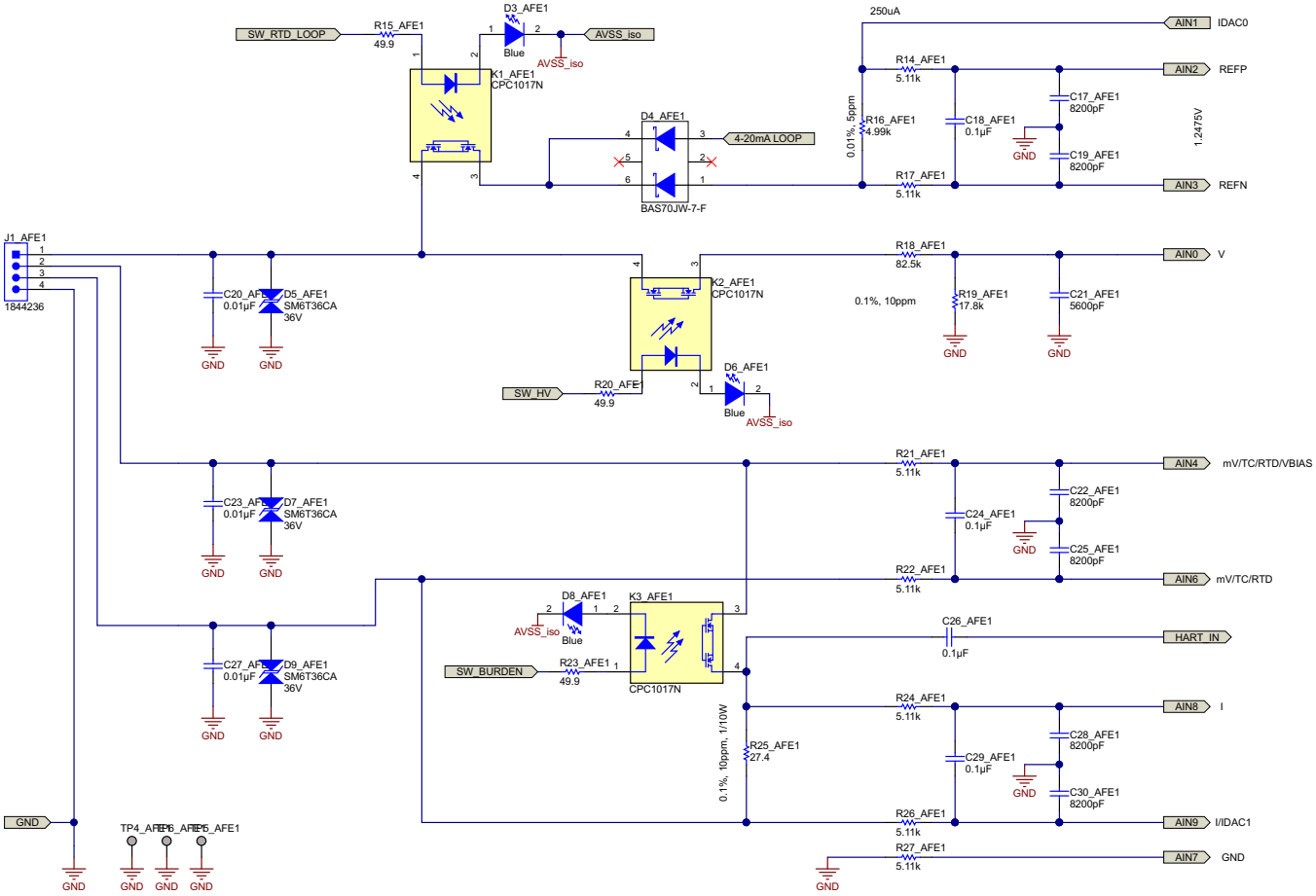


図 3. AFE Schematic

A basic requirement of such a universal design is a low terminal input count per channel to relax the real estate at the terminals of an analog input module. By supporting the RTD 4-wire connection mode, a minimum input count of four is given.

On the other hand, the ADC must have multiple input channels to separate the inputs path as much as possible to maintain the highest performance. The ADS1262 has 10 analog input channels, which are sufficient for this design.

Nevertheless, some signal switching is required to condense all supported measurement modes to the four terminal inputs. Three isolated switches (K1, K2, and K3 of type CPC1017Ni from IXYS) are used to route the I/O signals according to the selected mode. The function for each terminal is documented in 表 2, and 図 4 shows the assignments of the terminal pin number on the hardware. For more information about the mode control, see 3.4.

表 2. Terminal Functionality Overview

TERMINAL INPUT	V	mV (SE)	mV (DIFF)	CURRENT	TC	RTD (2-WIRE)	RTD (3-WIRE)	RTD (4-WIRE)	4- to 20-mA LOOP
T1	V	—	—	—	—	tie to T2	tie to T2	RTD++	Loop+
T2	—	mV	mV+	mA+	TC+	RTD+	RTD+	RTD+	Loop–
T3	—	GND	mV–	mA–	TC–	RTD–	RTD–	RTD–	Tie to T4
T4	GND	Tie to T3	GND	GND	—	Tie to T3	RTD– –	RTD– –	Tie to T3

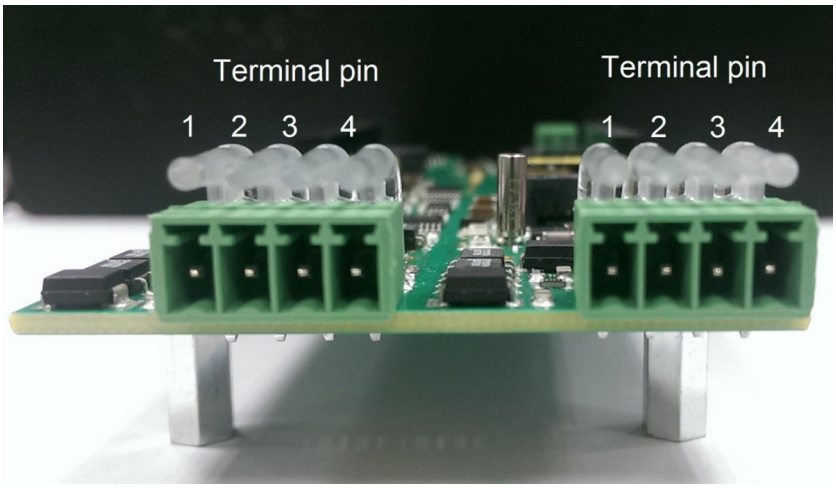


図 4. Terminal Pin Assignments

The connection for each mode is shown in 図 5.

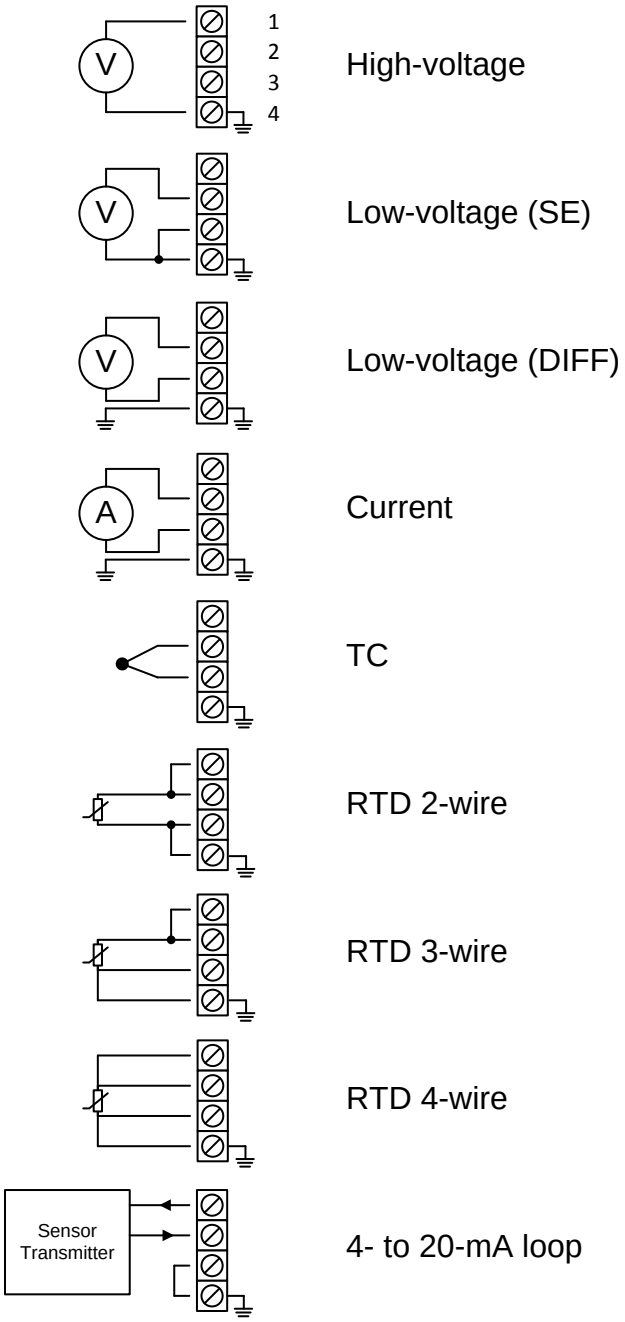


図 5. Connection Diagram

Due to the independent input paths, the high-voltage mode can run in parallel with the low-voltage or current inputs, making this design even more flexible and expanding the number of channels available by two.

From a protection point-of-view, this AFE is designed per IEC61000-4-5 class 2. It can tolerate ±1-kV (24-A) surge pulses. See 3.8 for more information about protection.

The following subsections examine the purpose of each terminal pin individually.

3.1.1 Terminal Input T1

Terminal pin T1 is used for

- Voltage input in high-voltage mode
- 24-V output in 4- to 20-mA loop mode
- Excitation current output in RTD modes

In the high-voltage mode, the isolated switch K1 is open and K2 closed. The ±12 V is attenuated by the R18:19 resistor divider bringing the input voltage to the input range of the ADS1262. The input resistance is around 100 kΩ, but can be increased if required. See 4.1 for more information and test results.

In the 4- to 20-mA loop mode, the isolated switch K1 is closed and K2 is open. The nominal loop voltage of 24 V is passed through D4 (pins 3-4) and K1 is finally available at T1.

In the RTD mode, the switch constellation is the same as in the loop mode. The ADC current source IDAC0 is internally connected to AIN1. The RTD measurement is performed in a ratiometric manner, meaning the current flowing through the RTD also flows through the precision reference resistor R16. The voltage drop of R16 is used as a reference voltage for the ADC. The minimum accepted reference voltage the ADS1262 is 0.9 V. With R16 = 4.99 kΩ and the excitation current of 250 μA, the reference voltage is U = R × I = 4.99 kΩ × 250 μA = 1.2475 V.

Unfortunately, the current through R_{REF} and R_{RTD} will not be 100% the same. The leakage current of K2 is around 4 nA at 85°C at the load pins (switched signal) with a load voltage, V_L, of 60 V. The second component where current is lost is the TVS diode D5. The leakage at the breakdown voltage, V_{BR}, of 30.8 V is typical 1 nA at 85°C. However, the maximum voltage during RTD measurement at both K2 and D5 is about 950 mV, which is much smaller than V_L and V_{BR}. This means that a much smaller leakage current can be expected. Nevertheless, the error I_{RTD} to I_{REF} at the maximum voltages would be 0.0002% and, therefore, is already at high voltages neglectable.

The 4- to 20-mA loop leakage is not an issue since the current leaks before it reaches the sensor transmitter.

3.1.2 Terminal Input T2 and T3

T2 and T3 are the inputs for almost all measurement modes (except high-voltage mode). Internally, this input is split in the voltage path and in the current path.

The voltage path measures the low-voltage (single-ended or differential), TC voltage and RTD voltage. No additional semiconductor is attached, meaning only the differential anti-aliasing filter with a cut-off frequency of 142 Hz separates the input of the system from the input of the ADC. Error sources, such as noise, offset or distortion as introduced by amplifiers are avoided this way. The input range of the signal is ±2.2 V (±2.5 V with PGA disabled). The PGA can gain the input signal by factor 1, 2, 4, 8, 16, and 32 introducing multiple input ranges programmable by software.

Since the components of the anti-aliasing filter are in the signal path, high-performance part should be used. C22, C24, and C25 are C0G/NP0 type capacitors with a 5% tolerance. The resistors are 1% metal film.

The current path anti-aliasing filter uses the same parameter as the voltage path. The burden resistor, R25, converts the current to measure into a proportional voltage accepted by the ADC input. When the isolated switch K3 is closed, the particular channel is in current mode; otherwise the channel is in voltage mode.

Using different ADC1262 input pairs for the voltage and current path has the advantage that the voltage drop over K3 is not being measured in current mode — at the cost of more analog input channels being used. The switch-on resistance, R_{DSON}, of K3 varies between 3 and 16 Ω over temperature and would make a high-precision measurement impossible. Here, only the voltage drop over R25 is measured, meaning the precision of the measurement is only dependent on this component. This design uses a 0.1%, 10ppm part. The parameter of R25 is dependent on the system requirements. See 4.3 for test results with the components used in this design.

The current mode is also used to measure the 4- to 20-mA loop. In addition, it provides the HART voltage signal to the HART modem plug-in board (TIDA-00549) through C26.

3.1.3 Terminal Input T4

T4 is the ground of the system. All ground-based signals must refer to T4. Floating signals, for example from TCs, will leave this pin unconnected. Because the nominal analog supply voltage of the ADS1262 is ±2.5 V, it is also the mid-point of the analog input range.

3.2 Data Converter

The heart of the system is the ADS1262, a high-performance 32-bit ΔΣ ADC. It offers a high integration of essential components required in an ADC signal chain, such as a PGA, a MUX, or a high-precision low-noise voltage reference. This fact can drive down cost, complexity, and real estate of an analog input module. Due to the high-dynamics range and the bipolar input of the ADC, a passive AFE is possible, which avoids additional noise sources.

Although the ADS1262 already includes a high-precision internal clock (7.3728 MHz ±2%) and a precision crystal in the system with ±50 ppm (equals ±0.005%), it depends on the application whether this external crystal with a higher accuracy is required.

3.3 CJC

CJC is required for proper TC measurement [(1)]. The local temperature measured at the terminal screws is added to the temperature measured by the TC to obtain the correct temperature at the TC. The local temperature is measured with the LMT01. The 2TO-92 package comes handy to measure the cold-junction temperature where it is actually generated, at the terminal block (see 図 6). The two large pads (without solder masks) are thermally connected to T2 and T3 to mirror the temperature at the terminal screws as accurate as possible. The LMT01 is glued to the pads in a way that the temperatures of T2 and T3 influence the LMT01 equally.

(1) For more information on the theory, please see TIDA-00189 Design Guide *Isolated Loop Powered Thermocouple Transmitter* Section 5 (TIDU449)

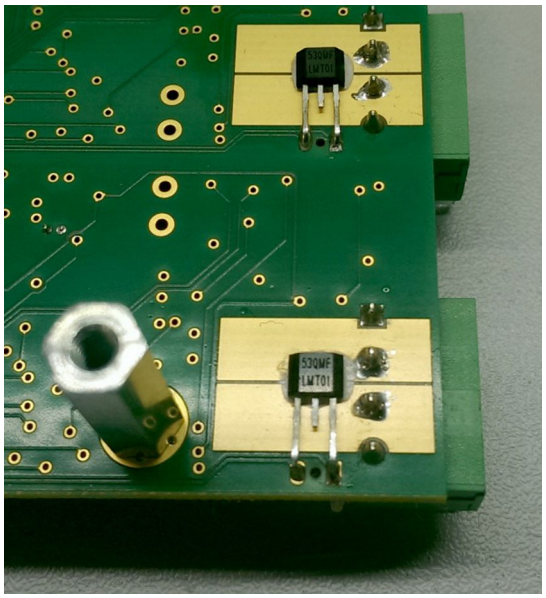


図 6. LMT01 Mounting

The digital pulse-train output provides its (digital) information by two different currents (34 μA indicating a logical '0', 125 μA indicating a logical '1'). By measuring the voltage drop, V_{DROP}, of the connected burden resistor R7 at the output of the LMT01, the information can be extracted. With the value of 1.65 kΩ, the voltage is U= R × I = 1.65 kΩ × 34 μA = 56 mV ('0') and 206 mV ('1') (see 図 7).

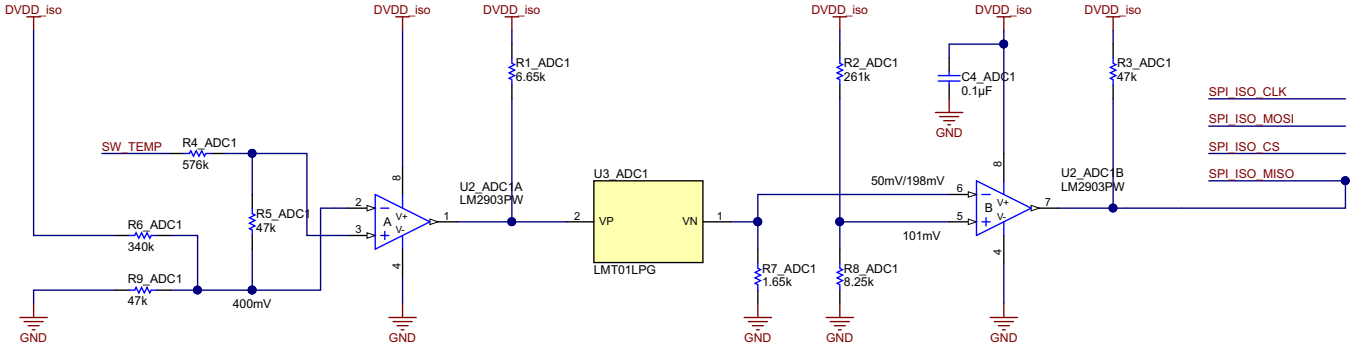


図 7. LMT01 Schematics

This information is modulated onto the SPI MISO line, saving an isolated channel. Software ensures the ADS1262 MISO line and the LMT01 output do not interfere. Once the LMT01 is enabled, every ~100 ms it pushes a new pulse-train with the temperature information. The length (pulse count) of the pulse train is dependent on the temperature value and is between 1 (corresponds to –49.9375°C) and 4096 (205.9375°C) pulses. With a nominal pulse frequency of 88 kHz and a maximum design operating temperature of 125°C (2812 pulses) one pulse train has a maximum length of 88 kHz^{-1} × 2812 = 32 ms (図 8 shows a screenshot at 25°C (1204 pulses = 13.6 ms)).

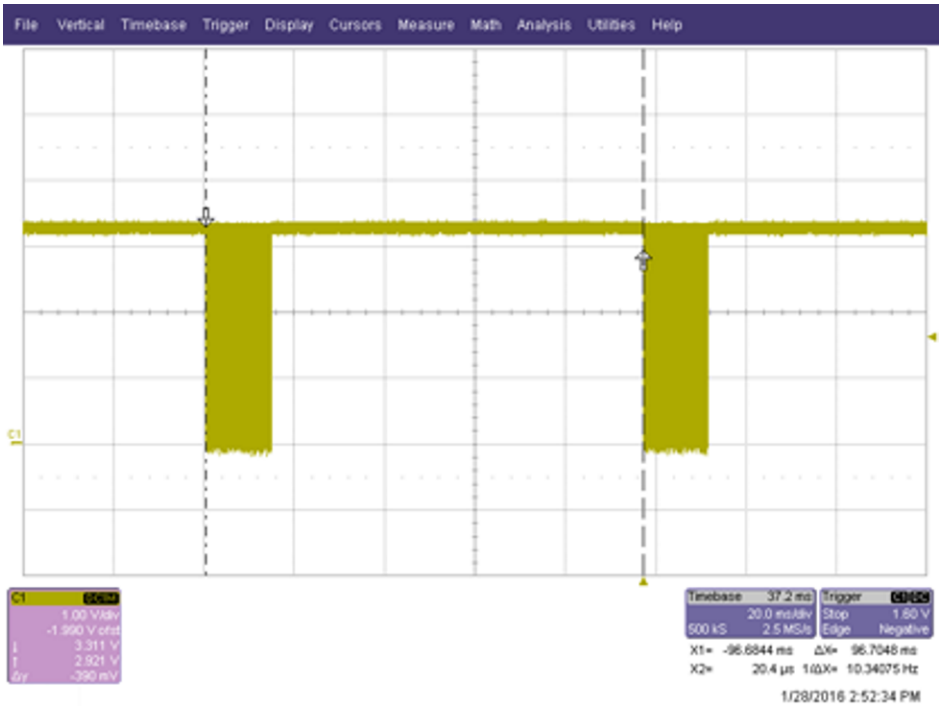


図 8. LMT01 Pulse Train at 25°C

The minimum time of inactivity between two pulse trains at 125°C is > 68 ms. This is enough time to turn off the LMT01 after the measurement (see 3.5 on how to control the LMT01). 図 9 shows the enabling of the LMT01, one pulse train, and the disabling of the LMT01. The disable time is time critical and needs to be shorter than 68 ms. Otherwise the start of a second pulse train interferes with SPI communication. The scope shows a time of 65 ms without optimization of the GPO switching.

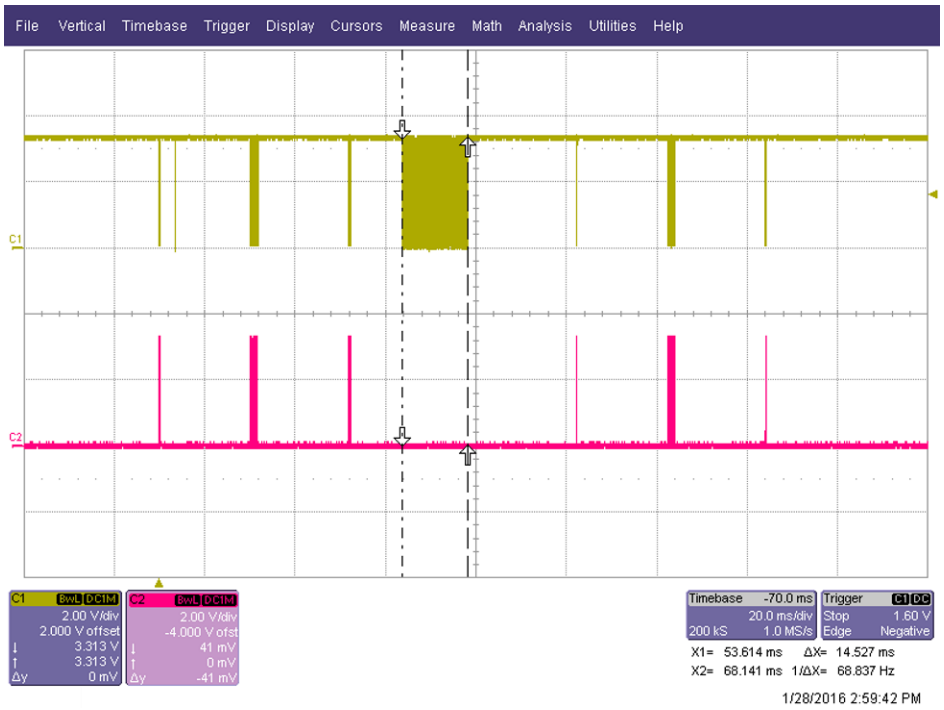


図 9. Controlling the LMT01

The dual-comparator LM2903 in 図 7 injects the pulse-train signal to the MISO line and turns on and off the LMT01. Its open-drain output is high-Z when the voltage at the comparator's negative input is smaller than the voltage on the positive input.

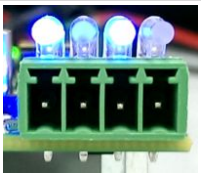
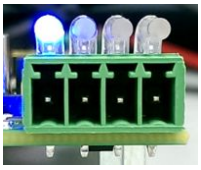
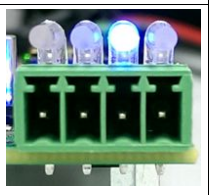
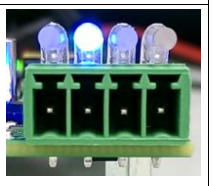
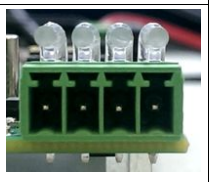
For comparator U2B, this is the case when the LMT01 is not powered because the pulse-train burden resistor R7 is connected to GND. Because the voltage at the positive input is fixed at around 100 mV and higher than the negative input, the output is high-Z. When the LMT01 is enabled, the comparator just copies the incoming pulse train to the output, but with CMOS compatible voltage 0 V (low) and 3.3 V (high-Z).

The second comparator of the LM2903 is used to translate the signal SW_TEMP from range ±2.5 V to 0 or 3.3 V to turn on and off the LMT01. When the GPO is low, the comparator output is enabled and pulls pin VP of the LMT01 low (disabled); otherwise, the output is high-Z, powering the LMT01 over R1.

3.4 Signaling

Each universal input channel is equipped with four blue-colored mode LEDs (D1, D3, D6, and D8) visibly outside the case by transferring the LED light using fiber optic channels. Three of the four LEDs (D3, D6, and D8) are in series with the three optical switches K1, K2, and K3. This saves control signals and provides direct feedback when current is flowing through the switches (switch on). The fourth LED (D1) is software-programmable by the GPIO expander. As shown in 表 3, all modes can be clearly decoded by D3, D6, and D8. One enhancement could be to turn on diode D1 in low-voltage or TC mode manually to provide feedback in every mode (also switches are off in this mode).

表 3. Mode LED Assignment

MODE	D3	D6	D8	D1	LEDs
4- to 20-mA loop mode enabled	On	Off	On	On/Off	
RTD mode enabled	On	Off	On	On/Off	
Current mode enabled	Off	On/Off	On	On/Off	
High-voltage mode enabled	Off	On	On/Off	On/Off	
Low-voltage or TC mode enabled	Off	On/Off	Off	On/Off	

Note that the high-voltage mode can work in parallel with the current mode and low-voltage or TC mode; therefore, D6 can be either on or off here.

Additional three status LEDs (D2, D12, and D14) for each input channel and one global status LED (D11) are available on board to provide feedback on supply voltages and enabled features. The status LEDs will not be visible from the outside when the board is mounted in a case. 表 4 shows the function of each status LED.

表 4. Status LED Assignment

LED	COLOR	FUNCTION
D2	Red	Software programmable
D11	Green	24-V DC available
D12	Green	4- to 20-mA loop enabled
D14	Green	DVDD available (3.3 V)

D11 is used to indicate feedback for the primary voltage (24-V DC from the PLC back-end power supply) while D14 can be used to verify availability of proper isolated voltage (isolated power supply working correctly). There is no separate indication of the analog supply rails (±2.5 V).

3.5 Isolated General Purpose Output

The TIDA-00550 requires at least six control signals to switch between the different modes. This design uses programmable GPIOs of the ADS1262 to save the cost of additional isolator channels. The two available GPIOs control an SN74HC594 shift register to provide the six required outputs. This shift register has the advantage to support the extended temperature range of –40°C to 125°C at low cost. Both GPOs from the ADS1262 (AIN5 and AIN7) are used to provide a simple synchronous serial bus to drive the SN74HC594. AIN5 (or GPIO2) acts as clock and AIN7 (or GPIO4) as data line. Both pins are controlled by writing to the ADS1262 GPIO data register (GPIODAT). Each level change of any of the GPO requires a separate SPI transfer from the main controller, which is acceptable since the mode of the TIDA-00550 changes rather seldom. 図 10 shows the connections to the serial bus of the expander.

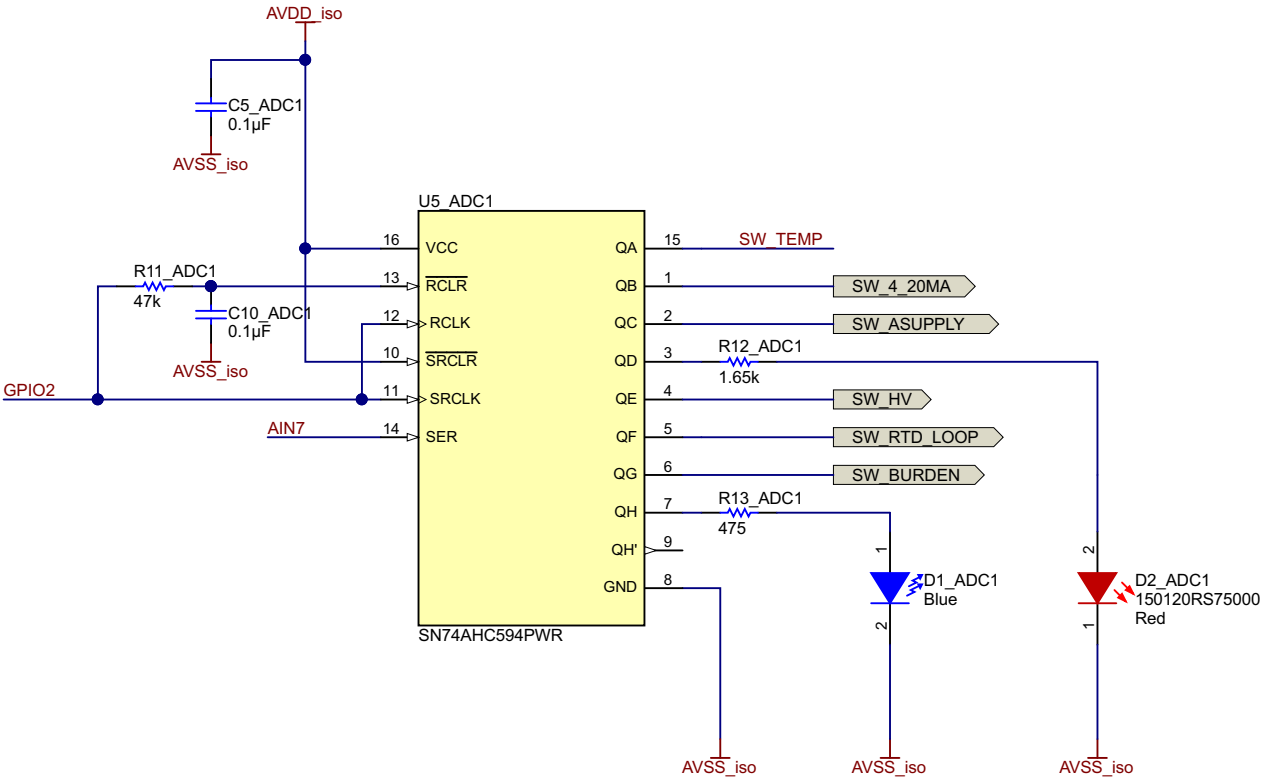


図 10. Driving the GPIO Expander

図 11 shows a waveform screenshot. Signal C1 is measured at pin 11 (SRCLK) of the expander, C2 is measured at pin 13 (#RCLR), and C3 is measured at pin 14 (SER).

Note that the SN74HC594 is connected to the AVDD/AVSS of the ADS1262, driving the GPO level to low (AVSS) and high (AVDD), as displayed in 図 11.

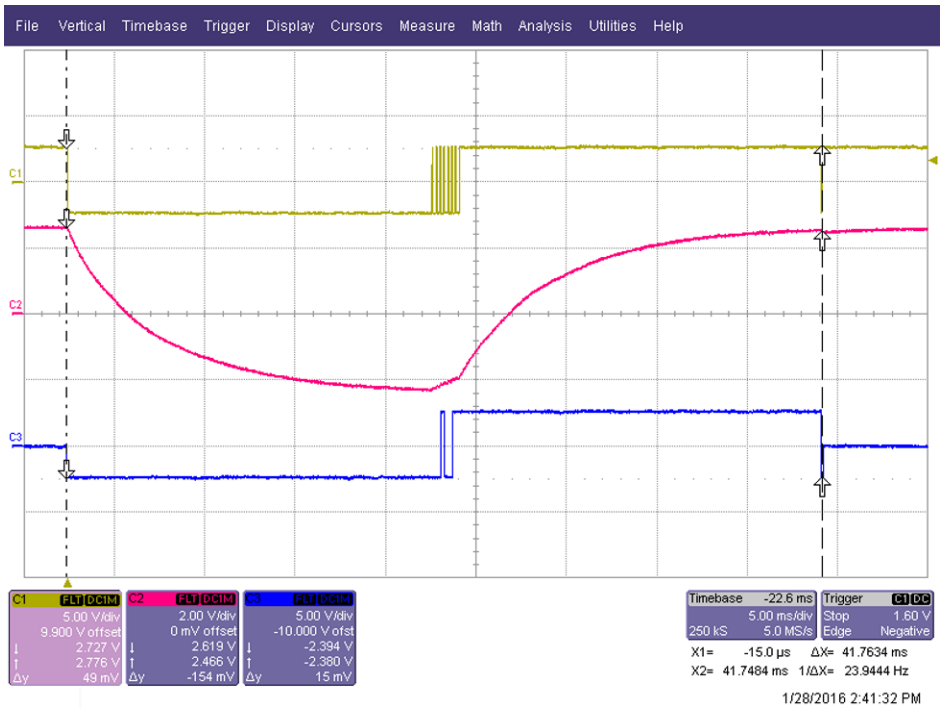


図 11. GPIO Access Waveforms

To provide a safe behavior of the design during operation mode changes, all output registers are cleared first, new data is shifted in, and finally the new data are passed to the outputs.

1. Set C1 (SRCLK) low → RC (R11, C10) network gets discharged.
2. Wait until C2 (#RCLR) is low (outputs buffer cleared).
3. Clock in new data byte; make sure the high pulses of the clock signal are short to avoid energizing of the RC network (In this example, the clock frequency is about 5 kHz).
4. Set C1 high (RC network energizes).
5. Wait until C2 (#RCLR) is high.
6. Apply an additional clock pulse to clock in the new data to output register.
7. Keep C1 high until next communication with the GPIO expander.

The entire procedure takes about 42 ms, but can be adjusted by changing τ of the RC network. 図 12 shows an example communication. In this case, the high-voltage mode will be enabled. By sending value 0x10 (most-significant bit first), the output QE (high-voltage mode enabled) of the SN74AHC594 is driven high.

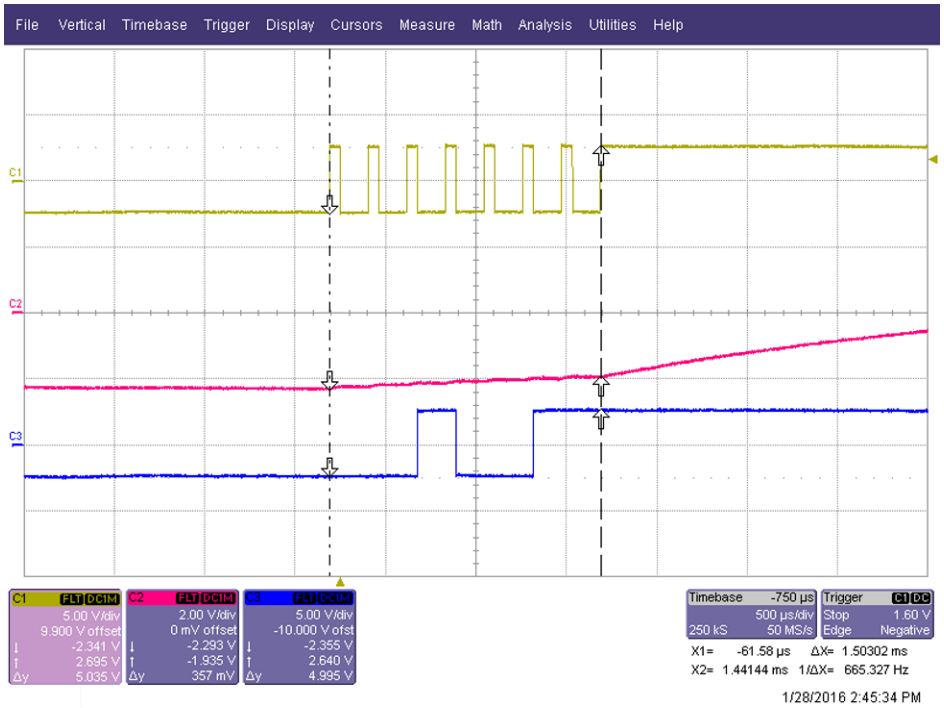


図 12. GPIO Expander Data Shift

The different modes are selected by the GPIO expander output. 表 5 provides information about the GPO patterns to set a certain mode.

表 5. GPO Signal to Mode Mapping

GPO SIGNALS	V	mV	TC	4- to 20-mA LOOP	RTD
SW_TEMP	0	0	0/1(1)	0	0
SW_4_20MA	0	0	0	1	0
SW_ASUPPLY	0	0	0	0	1
SW_HV	1	0	0	0	0
SW_RTD_LOOP	0	0	0	1	1
SW_BURDEN	0	0	0	1	0

(1) Signal SW_TEMP enables the LMT01 and is enabled occasionally only. No TC measurement can be performed when the local temperature measurement is on progress. See 3.3.

3.6 Data Isolation

The ISO7141CC isolates the data between the field and the PLC side. It supports the minimum required number of four channels to support a 4-wire SPI. Although equipped with enable capability the ISO7141CC is always on. The reason is the pulse train from the local temperature sensor LMT01, which is delivered independently of the SPI bus, but sharing the SPI_MISO line. However, there is still the option to enable or disable the isolator by an additional GPO from the host processor to save power.

The SPI_MISO line must still be gated by the SPI_CS signal because multiple universal input channels may share a SPI. Component U4, a single-gate buffer SN74LVC1G125, passes the SPI_MISO signal if SPI_CS is low. The pulse train signal is asynchronous to the SPI_CS signal, and thus must be monitored independently when a pulse train from the LMT01 is expected (LMT enabled).

3.7 Power

The power section is split in the PLC-side part and in the field-side part. To power the board a nominal voltage of 24-V DC (operating range: 16-V to 33-V DC) is provided from the PLC side. Due to the low power consumption of the board (< 400 mW), a power connection from the field side is not provided to avoid additional protection.

3.7.1 Input Stage

This TI Design can be powered in two ways. The primary option is to connect the nominal 24-V DC to J2. When the board is used in conjunction with a BeagleBone Black, it can be powered from the provided 5-V DC by header P9. The TPS61093, a 17-V DC step-up converter, boosts the 5-V DC to around 16.5-V DC, which is still in the accepted supply voltage range. The step-up converter is disabled if a valid voltage is detected on connector J2. Status LED D11 is turned on if the board has a proper input voltage from either input.

3.7.2 Isolated Power Supply

The provided input voltage passes a PI-filter for bidirectional filtering and then connects straight to the LM5017, a constant on-time synchronous buck regulator. It will buck the input voltage to 10 V. This is just enough to operate the LM5017 internal LDO from the secondary voltage instead of the higher input voltage, thus decreasing power dissipation of the LM5017. The switching frequency of the converter is around 264 kHz to keep the efficiency high and the harmonics away from the sensitive ADS1262 modulator frequency, f_{MOD}, of 921.6 kHz. With nearest harmonics at 793 kHz (third harmonic) and 1.057 MHz (fourth harmonic), f_{MOD} is located about in the middle.

The converted voltage is connected to the primary winding of a customized transformer from company Würth Electronics (see 5.2 for an orderable part number). It provides the following voltages at the secondary side:

- 30-V DC for a 24-V DC loop power supply
- 5.6-V DC for a 3.3-V DC digital power (DVDD) and a 2.5-V DC analog positive rail (AVDD)
- –5.6-V DC for a –2.5-V DC analog negative rail (AVSS)

3.7.3 Point-of-Load (POL) Power Supplies

The three voltages from the transformer are rectified by standard diodes before they are passed to the LDOs.

The LDO TLV70433 (U13) provides 3.3-V DC to supply the digital part of the ADS1262, the ISO7141CC, and the LM2903.

The TPS7A4901 (U14) and TPS7A3001 (U16) are high-performance LDOs supplying the analog section of the ADS1262 with a positive voltage, AVDD, and a negative voltage, AVSS. This power supply allows direct measurement of bipolar signals without additional signal.

AVSS can be in range of –2.5-V DC to 0 V while AVDD must always be AVSS + 5-V DC. This way, unipolar and bipolar power supplies are supported. The default analog supply of the ADS1262 in this design is ±2.5-V DC, but the TIDA-00550 has the capability to shift this supply to –1.7-V DC and 3.3-V DC. The main reason for this feature is to support the RTD measurement (see 3.7.4 for more information), but is not limited to it. The GPO signal SW-ASUPPLY is responsible for the voltage selection (low = ±2.5-V DC, high = –1.7-V DC and 3.3-V DC). It drives a MOSFET on each rail changing the ratio of each LDO feedback resistors and setting the target voltage this way. It is unlikely that both voltages switch at the same time causing lower and higher voltages in range 4.2-V to 5.8-V DC. This voltage range can be safely handled by the ADS1262.

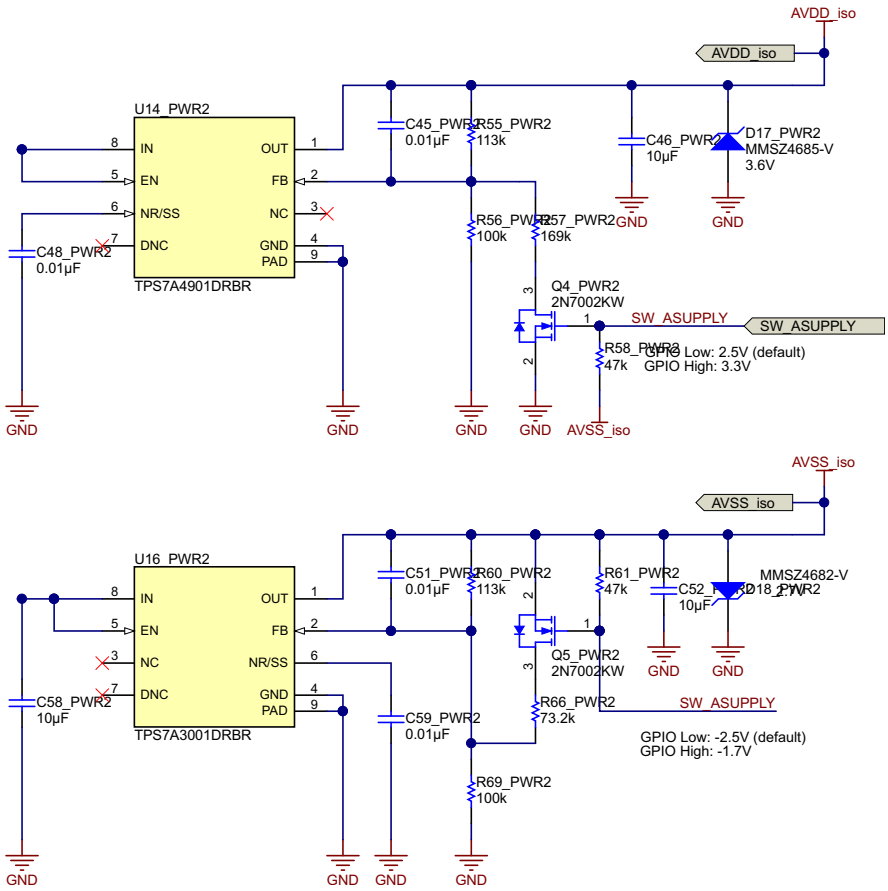


図 13. Bipolar Power Supply

The DVDD, AVDD, and AVSS supply rails integrate Zener diodes (D15, D16, and D18) to ensure the voltage never lifts up above absolute maximum voltages harming the integrated circuits by providing low impedance to ground. Such voltages may be generated by a surge at the terminal pins. For more details, see 3.8.

3.7.4 Current-Limiting 24-V DC Power Supply

The current-limiting 24-V DC power supply is designed to drive remote devices (for example, sensor transmitters) with a 4- to 20-mA loop interface (see 図 14). As long as the loop stays in its normal operating conditions, up to 25-V DC are delivered at terminal pin 1. If more than about 22 mA are drawn the power supply will slowly enter the current-limiting state by decreasing the output voltage. The current limiting circuit is located at high-side, meaning the current set by the remote device will be flowing through the burden resistor for most accurate results because no additional current monitor between the loop-powered device and the burden resistor is required. The supply can be enabled and disabled by the signal SW_4_20MA.

The isolated power supply transformer provides a separate secondary winding for the power supply. The wide input range LDO TPS7A4101 (U12) regulates the 30 V from the transformer to 25 V. The current drawn is constantly monitored by the R46/Q2. The voltage drop across R46 generates the basis-emitter voltage, V_{BE}, of the PNP transistor Q2. If the current increases, V_{BE} also increases, causing Q2 to start conducting. The upper feedback resistor R48 of the LDO is connected to the collector and emitter of Q2, which will lower the resistance and increase the feedback voltage of the LDO, V_{FB}. This will decrease the output voltage.

Another reason to use this topology is the simple injecting of the HART transmitter signal. The HART signal provided by the TIDA-00549 is directly fed into the feedback node of the LDO (signal HART_OUT).

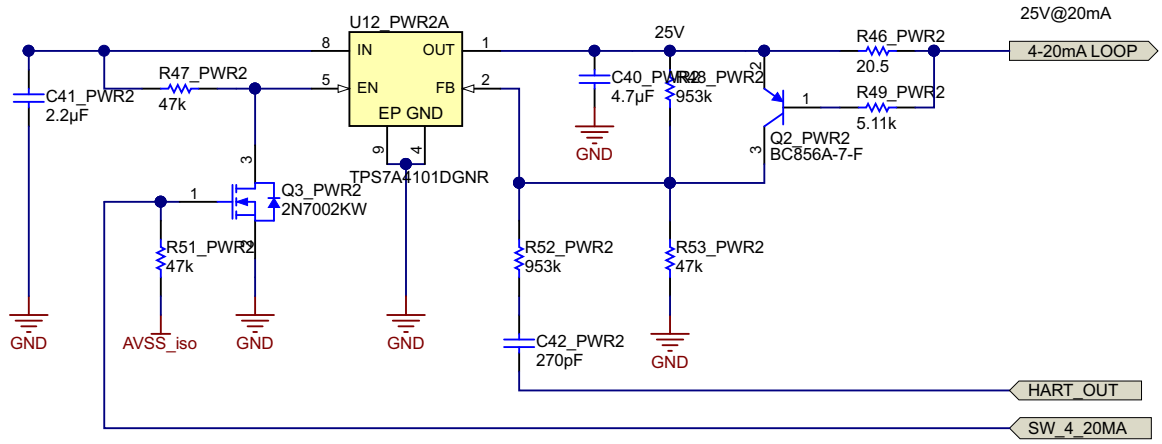


図 14. 4- to 20-mA Loop Supply

3.8 Protection

Protection against surges is an important property of every component used in factory automation and control. Take care with any interface to the outside world. In this design, the terminal pins are protected because these pins are the only connection to the outside. Having protection at analog signals is always a tradeoff because the leakage of the protection will have influence to the sensitive signal to measure. For instance, inappropriate protection may decrease the input impedance of an analog signal due to leakage, unnecessarily loading the signal source. Protection of the power supply is not implemented here. It is assumed that the power supply embedded in the PLC uses already sufficient protection. For more information on power supply protection (and much more), see the TI Design TIDA-00233 (1).

To protect the signal lines, the TIDA-00550 uses primarily TVS diodes to clamp excessive high and low voltages to ground. As an additional requirement, all terminal pins must be tolerant to steady PLC power supply voltages. Unlike in a surge event, a PLC power supply up to 33 V can be connected for a longer period of time because of incorrect wiring during installation. For this event, no significant current should flow into the board. With this requirement, the breakdown voltage, V_{BR}, is given directly. The bidirectional TVS diode SM6T36CA has a nominal V_{BR} of 36 V, where 1 mA will flow through the TVS diode. This means at PLC power supply level (up to 33 V) the TVS diode will have no effect and the voltage will be seen by the AFE. The sensitive part of the front-end are the analog inputs of the ADS1262. The internal ESD diode will start conducting 0.3 V beyond the analog supply rail, which is ±2.8 V. The design has to ensure that the current does not exceed 10 mA through the ESD diodes. Therefore, each analog input is protected by a 5.11-kΩ resistor. At 33 V, the current through an ESD diode will be IESD = (33 V – 2.8 V) / 5.11 kΩ = ~6 mA. See 図 15 for the schematics.

(1) See the product folder at http://www.ti.com/tool/TIDA-00233

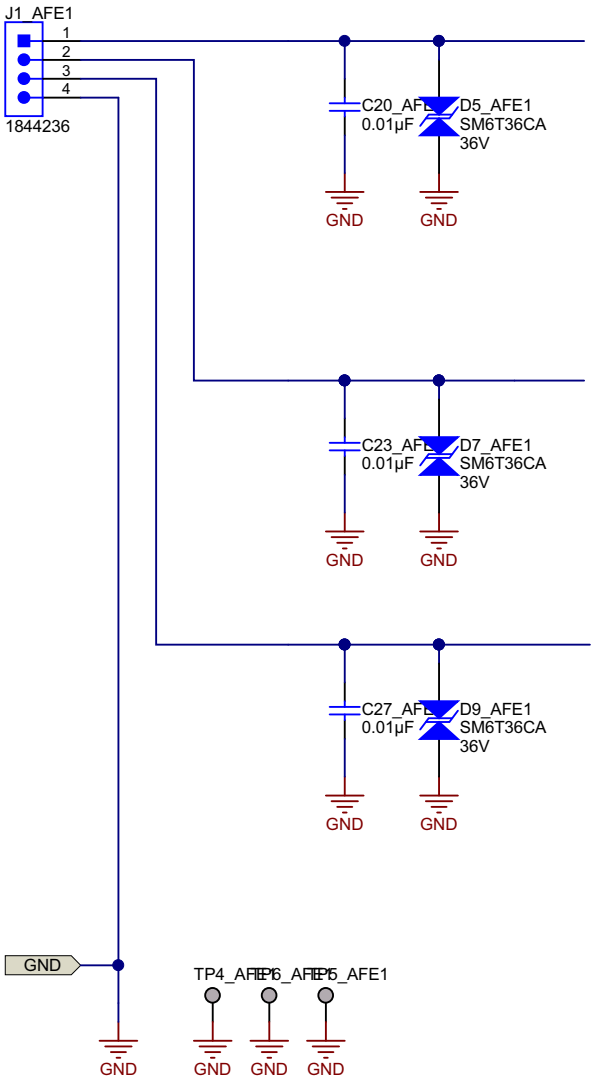


図 15. Input Protection

The protection circuit gets more challenged if a surge happened at the terminal pins. The target is that a class 2 (±1-kV) surge with a current of 24 A (42-Ω resistance requirement for non-power lines) can be handled without damaging the board, according to EN61000-4-5.

On such an event the TVS diode will still try to clamp the ±1 kV to its nominal V_{BR} of 36 V, but the dynamic resistance of the TVS diode, R_D, will now come into play. The resulting clamping voltage, V_{CL}, which is seen by the circuitry, will be higher than V_{BR}. With a peak pulse current, I_{PP}, of 24 A and RD = 0.427 Ω, the value of the V_{CL} increases to $R_D \times I_{PP} + V_{BR}$ = 48.05 V at 25°C ambient temperature. In a worst case scenario with an ambient temperature of 125°C, V_{CL} even rises to 50.04 V. This voltage can still be handled by the ADS1262 input pin. The maximum current over the internal ESD diode is now ~9.3 mA. The capacitors C20, C23, and C27 in front of the TVS diodes are supposed to help the diodes to catch the steep surge pulse.

The protection circuit will have some impact on the analog input signal under normal conditions. The TVS diode will drain a leakage current, I_{RM}, of maximal 1000 nA at the stand-off voltage, V_{RM}, of 30.8 V and 85°C ambient temperature. For the high-voltage input the input impedance is 100 kΩ due to the resistor divider. The impedance change through the TVS diode leakage is negligible. For the low-voltage input, the maximum input voltage over the diode is ±2.5 V, which is less than 10% of V_{RM}. With a typical I_{RM} of 100 nA at V_{RM}, a typical leakage current of < 10 nA can be expected decreasing the input impedance from 1 GΩ to about 250 MΩ. For the current measurement with its worst-case 18 bits (noise-free) resolution the leakage current is lower than ½ LSB and therefore also not relevant.

3.9 RTD Measurement

RTDs measure the temperature at a remote location. The resistance of the element changes with temperature, thus providing information by a voltage drop when a constant current is applied. In Factory Automation, two approaches are used.

The first option is the use of a so-called sensor transmitter [(2)]. The sensor transmitter measures and processes the temperature and sends the information over a 4- to 20-mA loop to the current input of an analog input module. This option is supported by TIDA-00550 in the 4- to 20-mA loop mode. The second option is the direct connection of an RTD. No additional hardware is required between the RTD and the input of the analog input mode. This option is also supported and is discussed in this chapter.

The ADS1262 integrates all required features for a direct RTD measurement, such as two matched current sources, support of an external differential reference for ratiometric measurement, as well as enhanced features like rotating current sources to eliminate variances in the two current sources. A temperature using RTD can be measured in three ways: the 2-wire, 3-wire and 4-wire connection scheme. This design supports all three measurements methods.

RTD elements are available in different accuracy classes. To achieve this accuracy, the wire resistance must be compensated. An AWG24 wire with a diameter of 0.511 mm (0.0201 in) has a resistance of 84.2 mΩ/m (25.67 mΩ/ft). Assuming the RTD sensor is 50 m (164 ft) away from the PLC, the resistance of a 2-wire connection sums up to 2 × 50 × 84.2 mΩ = 8.45 Ω. With the RTD resistance of 100 Ω at 0°C (Pt100), the error would be more than 8% at this temperature point and even more at lower temperatures. The 3-wire and 4-wire connection schemes address this issue.

The supported Pt100 covers the temperature range from –200°C to 850°C. Within this area, the resistance of the RTD element changes from 18.52 to 390.48 Ω. The °C/R curve is nonlinear. Typically, the microprocessor unit compensates using a look-up table and interpolation.

The selected components in this design work with a constant RTD current, I_{RTD}, of 250 μA. Other currents are also possible, but need a change of the reference resistor, R_{REF}. See 表 6 for a comparison of different I_{RTD}. While the first three columns use the minimum reference resistor value for a certain I_{RTD} (resulting in the minimum required reference voltage, V_{REF}, of 0.9 V), the last column shows the actual configuration in the design. The nominal AVDD voltage of 2.5-V DC is not sufficient for 250- and 500-μA operation. Also for 100 μA, the margin is very small. For this reason, the analog power supply of the ADS1262 is shifted up by 800 mV with AVSS = –1.7-V DC and AVDD = 3.3-V DC for all RTD measurements. This provides enough of a margin also for higher I_{RTD} currents. This feature is not limited to the RTD mode. It can be also used to adjust the analog input range in other modes. The TIDA-00550 uses a reference resistor of 4.99 kΩ to protect AIN1 from surges at the same time. See 3.8 for more details on protection.

(2) See TI Design TIDA-00851 for an example (http://www.ti.com/tool/TIDA-00851)

表 6. RTD Current Comparison

CASE	LOWER CURRENT	USED CURRENT	HIGHER CURRENT	USED CONFIGURATION
Excitation current (μA)	100	250	500	250
Reference resistor (kΩ)	9000	3600	1800	4990
Reference voltage (V)	0.9	0.9	0.9	1.2
Min IDAC voltage (V)	1.1	1.1	1.1	1.1
Max RTD V-drop (V)	0.039	0.098	0.195	0.098
Diode V-drop (V)	0.4	0.4	0.4	0.4
50-m wire V-drop (V)	0.001	0.002	0.004	0.002
Min AVDD (V)	2.44	2.5	2.599	2.847

表 6. RTD Current Comparison (continued)

CASE	LOWER CURRENT	USED CURRENT	HIGHER CURRENT	USED CONFIGURATION
PGA gain (V/V)	16	8	4	8

I_{RTD} takes a certain path for RTD measurements (see also 図 16 for component names). First, it flows through R_{REF} (R16) used to generate V_{REF} for the ratiometric measurement. With R_{REF} = 4.99 kΩ and I_{RTD} = 250 µA, V_{REF} is about 1.25 V. Next, I_{RTD} passes diode D4. This diode protects inputs AIN1, AIN2, and AIN3 from the 24-V 4- to 20-mA loop power (Mode IV). The next component, the isolated switch K1, is required to disconnect the RTD reference from the high-voltage input in Mode I (this mode accepts ±12.39 V at the input). Finally, I_{RTD} appears at the terminal pin 1 where the RTD is connected.

3.9.1 2-Wire RTD Measurement

The 2-wire mode is the simplest and cheapest, but also the most imprecise measurement method. The RTD connects to the PLC input module with only two wires. The constant current I_{RTD} (from IDAC0) is carried over the connection wires and, thus, the measurement of the RTD also includes these wires. The resistance of the wires, R_{LEAD}, causes a voltage drop, which is measured along the actual RTD resistance R_{RTD}. This method should only be used for short, low-impedance wires to minimize this error. The temperature-dependent resistance of the wires does not allow a simple subtraction of the wire resistance from the measurement. 図 16 shows the current flow (red lines) and the measurement path (green lines) for the 2-wire connection.

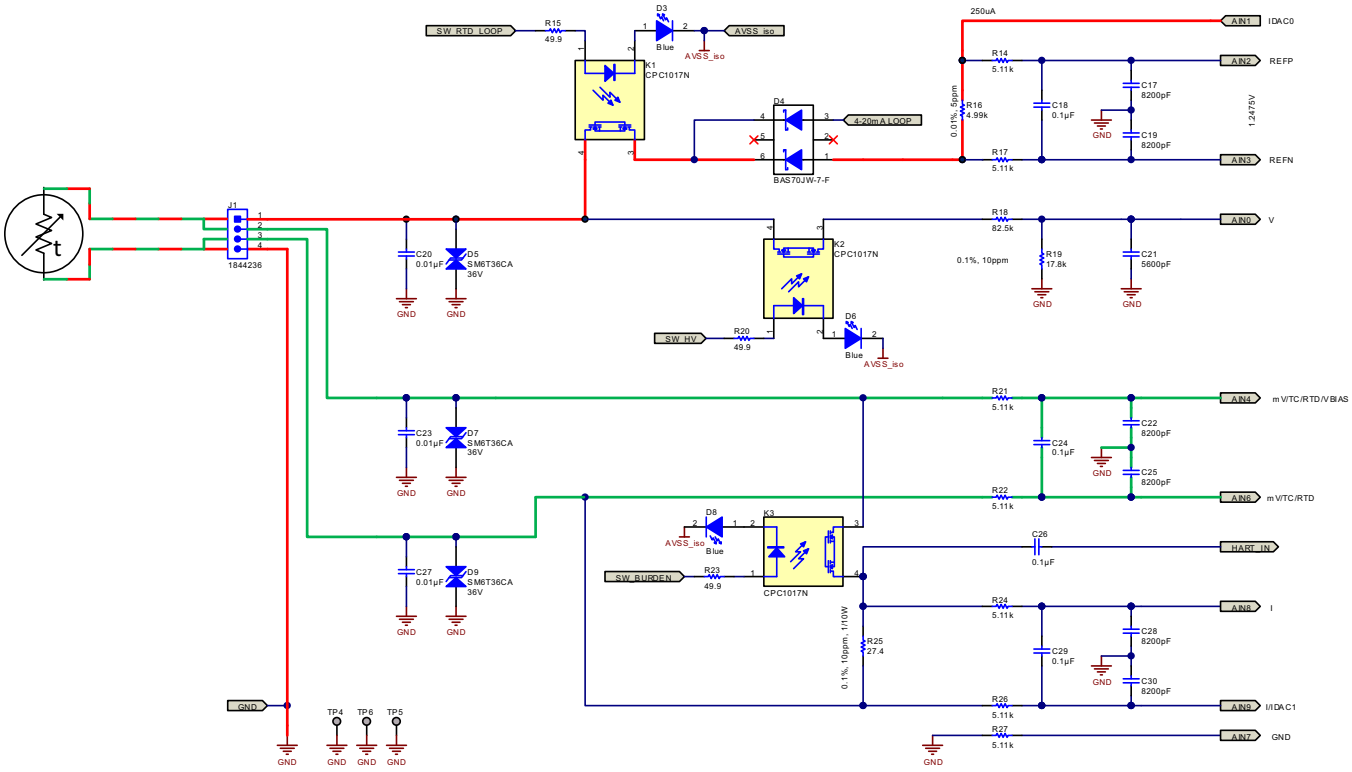


図 16. RTD 2-Wire Connection

3.9.2 3-Wire RTD Measurement

The 3-wire method is most common. It is a good trade-off between accuracy and cost of wire. In this connection scheme, two current sources, IDAC0 and IDAC1 of the ADS1262, are used. Both currents are injected on the measurement wires, like in the 2-wire connection. Assuming the wires have the same R_{LEAD} and the current from the sources match, both voltage drops across R_{LEAD} are subtracted from the equation. Both currents will flow towards ground with the third wire.

To compensate for current mismatches of the sources, the IDAC rotation feature has been implemented in the ADS1262. Two consecutive measurements are averaged, the first with IDAC0 at AIN1 and IDAC1 at AIN9 and the second with IDAC0 at AIN9 and IDAC1 at AIN1, thus removing the mismatch of both current sources.

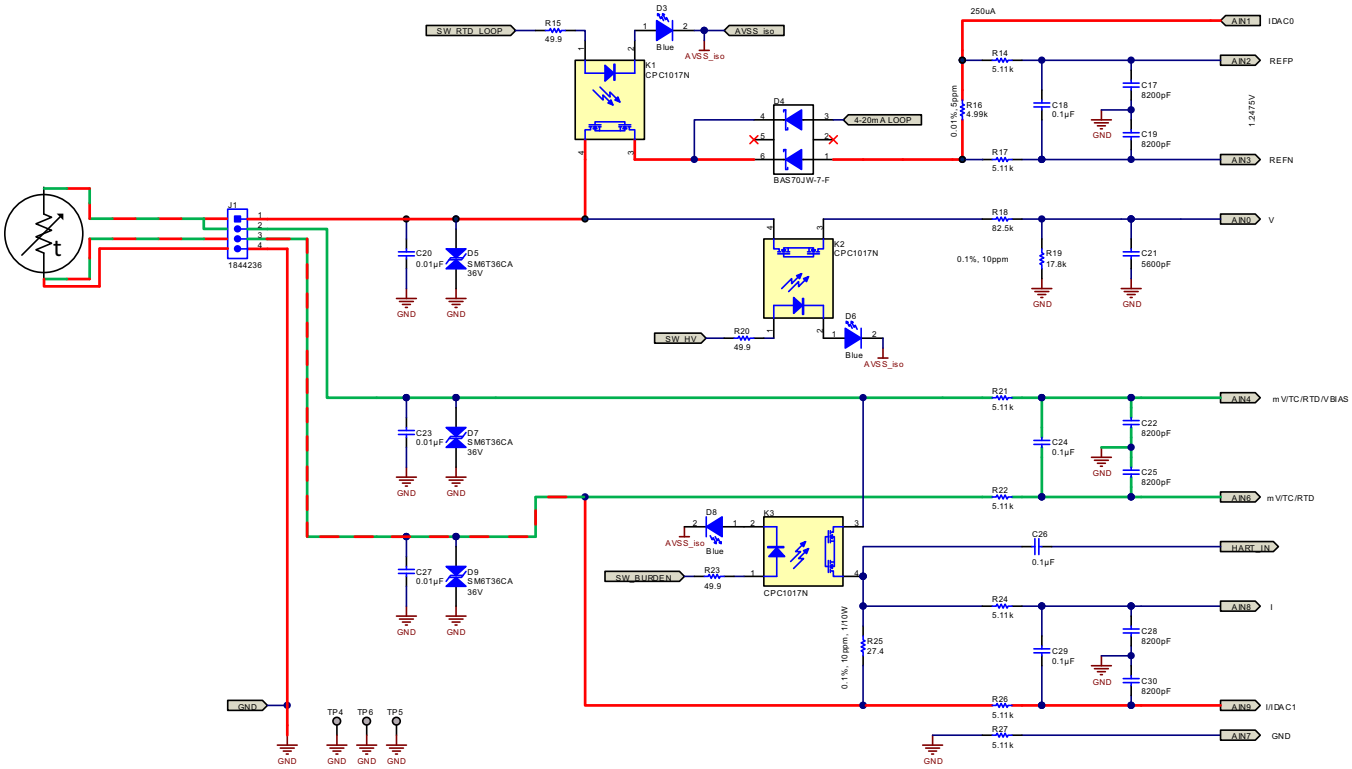


図 17. RTD 3-Wire Connection

3.9.3 4-Wire RTD Measurement

The 4-wire connection is more costly due to the required four wires. Nevertheless, it is quite straight forward due to its symmetry and delivers the most accurate results. Two wires are connected to each of the RTD leads. One pair supplies the current; the other pair measures the voltage. There is no overlapping of supply lines and measurement lines at all. The measurement input of the ADS1262 has an impedance of > 250 MΩ. Therefore, the error from the voltage drop over the measuring wires is less than 1 ppm.

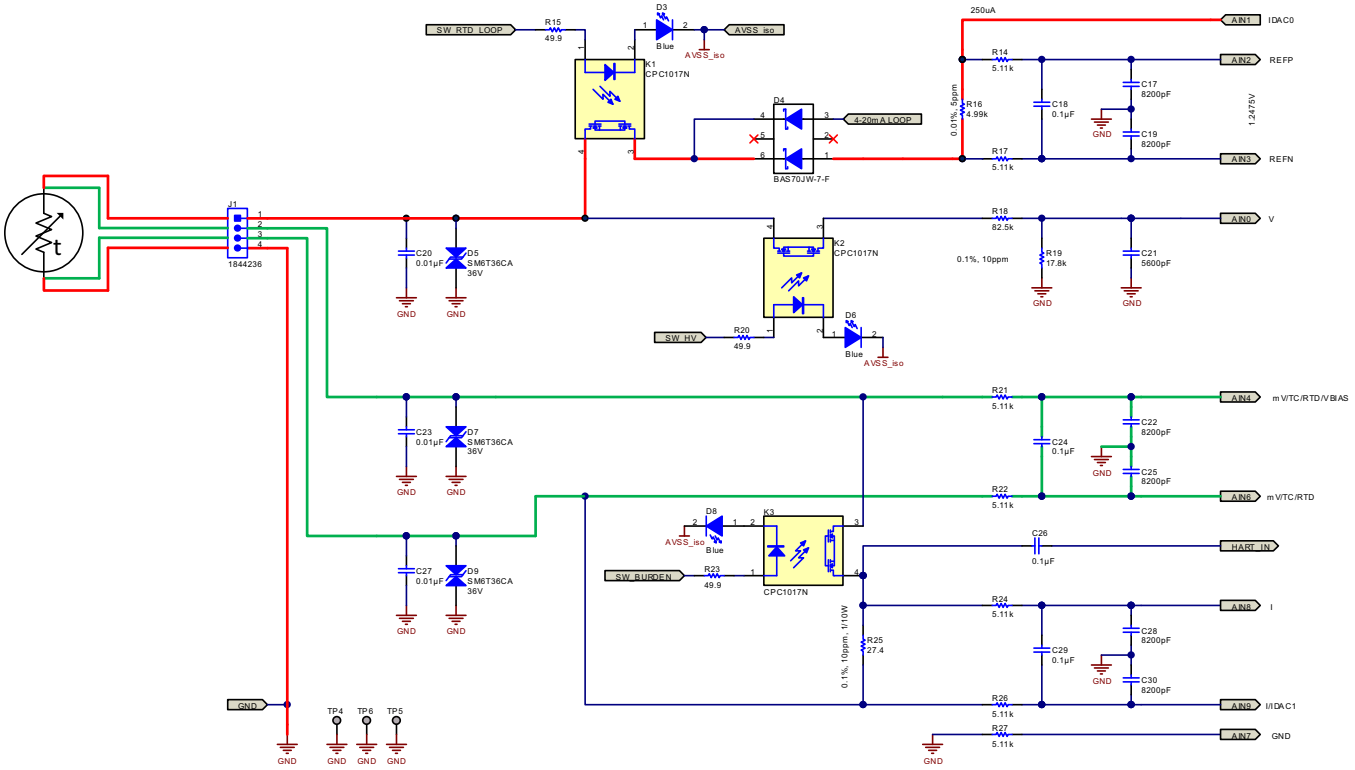


図 18. RTD 4-Wire Connection

3.10 Optional Hart Communication

The TIDA-00549 is a plug-in board for the TIDA-00550, extending its functionality with HART. The TIDA-00550 includes two sockets per channel to connect the HART modem hardware. The TIDA-00549 has its own isolation and connects through UART to the back end.

The received HART signal is decoupled from the 4- to 20-mA current by C26. Signal conditioning is done on the HART board. The HART signal to be send to sensor transmitters is connected to the feedback loop of the 4- to 20-mA loop LDO (U12). This provides a very power efficient method to modulate the HART signal on top of the 4- to 20-mA current. 図 19 shows the HART modem board.

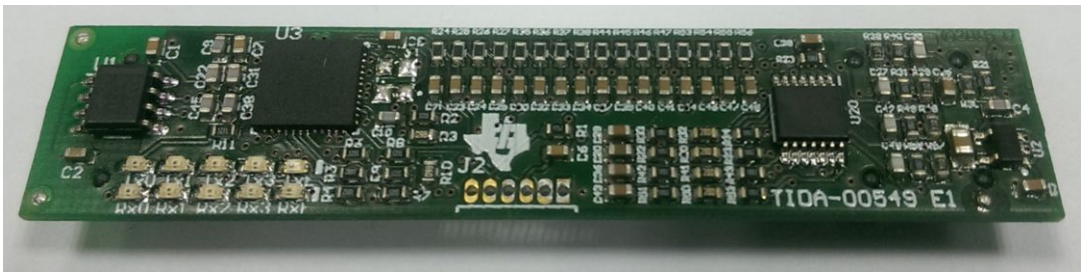


図 19. Picture of the HART Modem Board (TIDA-00549)

4 Test Setup and Results

This section shows the test results of the TIDA-00550. Test software (not provided) has been written on the MSP430FR5969 LaunchPad (図 20) handling the SPI of the TIDA-00550. A separate capture input of the MSP430 counts the pulses from the LMT01. The user interface is a simple command line terminal allowing user input settings, which is basically the mode selection and read/write capability of the ADS1262 register bank (see 図 21). The register access is important to get and set the gain and offset register values of the ADS1262.

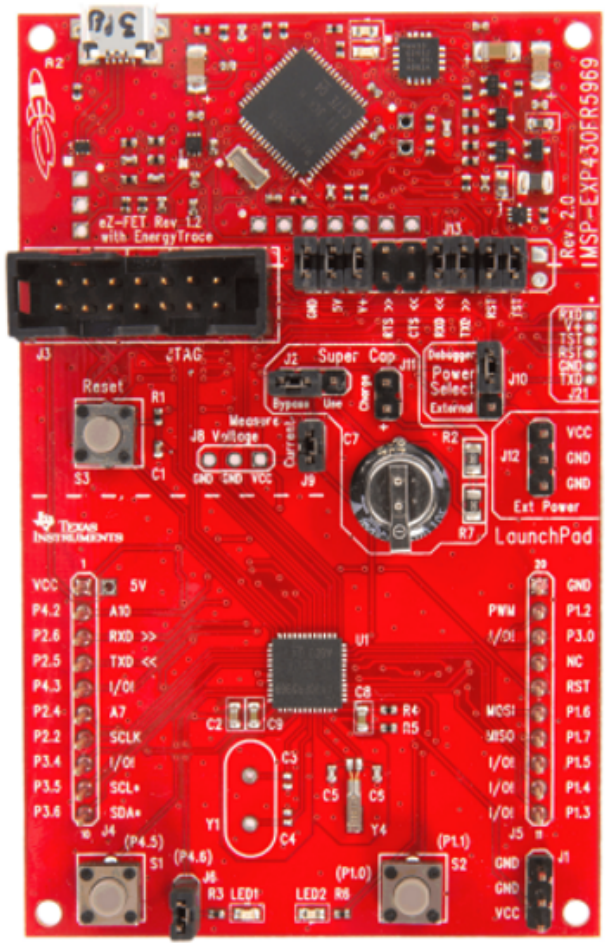


図 20. MSP430FR5969 LaunchPad

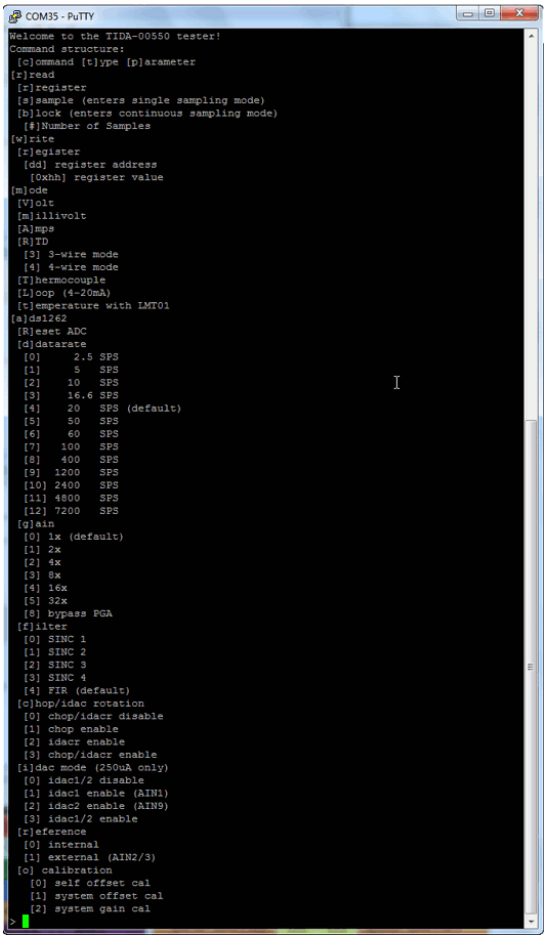


図 21. Test Program Options

The user interface can also be set to quiet mode with very limited feedback. This mode is used by an automated test environment (ATE). The test script is written in python and connects the TIDA-00550 with the ATE including

- Climate chamber T40/25 from CTS
- 8.5-digit digital multimeter (DMM) 3458A from HP
- Source Measurement Unit Agilent B2912A from KeySight
- Power Supply E3631A from Agilent
- MSP430FR5959 LaunchPad from Texas Instruments
- RTD simulator Type 1049 from Time Electronics

- Resistor Ladder R1-3000 from CMT
- Standard PC

The raw test results are written to a .csv file for further data processing.

4.1 Mode I (High-Voltage) Measurements

With the bipolar power supply set to ±2.5-V DC and the internal PGA enabled (gain = 1 V/V), the ADS1262 samples a terminal single-ended input voltage value up to ±12.39 V at terminal pins 1 and 4. The resistor divider R18:R19 provides a fixed attenuation of about 15 dB, converting the input signal to ±2.2 V suitable for the ADS1262 input. The absolute resistor tolerance of 0.1% provides a stable attenuation and can be relaxed if gain calibration is performed during production. More important is the temperature stability to maintain optimum results over temperature. The selected value of 10 ppm is a good trade-off between cost and stability.

The maximum voltage drop over the on-resistance of the isolated switch, R_{DSON}, can be neglected because the 0.1% tolerance of R18 is about 10 times higher than R_{DSON} and therefore the dominating factor in the equation of the signal attenuation.

The external antialiasing filter together with the circuitry inside the ADS1262 has its –3-dB corner frequency at around 1000 Hz and –100-dB attenuation at around 921 kHz; providing effective signal suppressing around the delta-sigma modulator frequency (see 図 22).

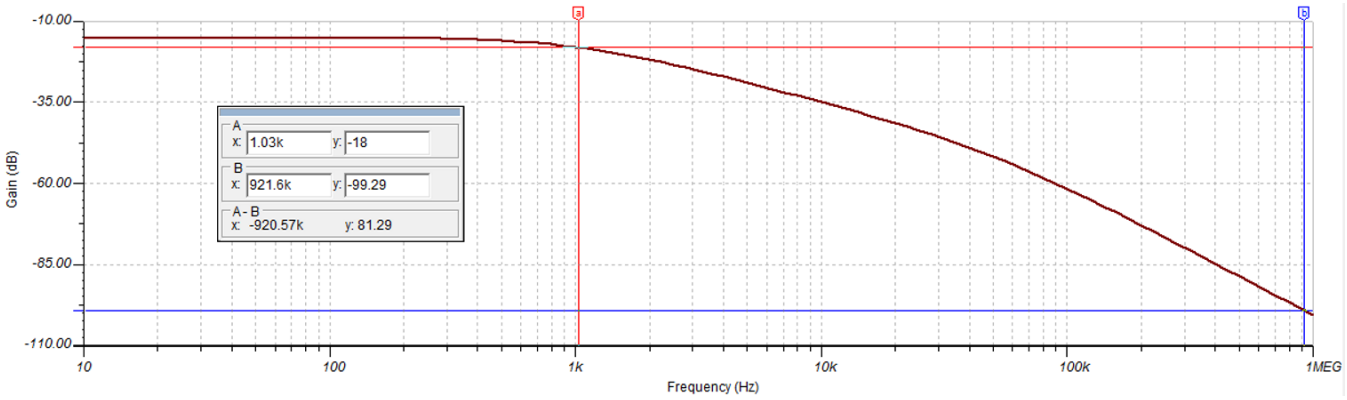


図 22. High-Voltage Anti-Aliasing Filter Curve

To measure DC performance of an ADC, the input must be set to a heavily decoupled constant input voltage while a series of samples are taken. Due to the symmetrical bipolar ADC input range, the input is shorted to GND to perform DC measurements. The analog input is shorted to ground at the terminal pins of the board to include the AFE to the measurement (図 23).

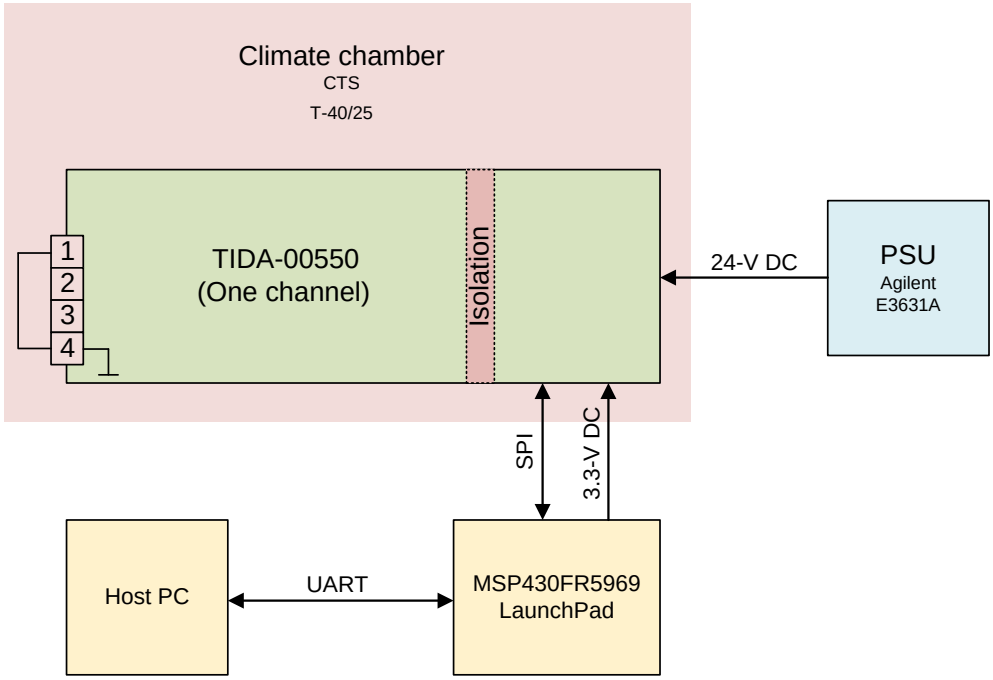


図 23. Test Setup for High-Voltage Noise Measurement

図 24 to 図 26 show the histograms for signals samples with 20 SPS at temperatures 25°C, 85°C, and –35°C. 図 27 to 図 29 are taken at the same temperature points, but with 2400 SPS to use the entire bandwidth of the high-voltage input path. No calibration has been performed to show the overall system offset, which is at about 340 µV and nearly constant over temperature.

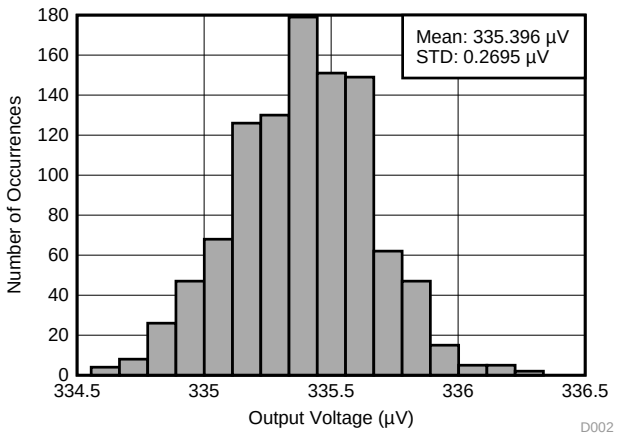


図 24. Distribution at 25°C and 20 SPS

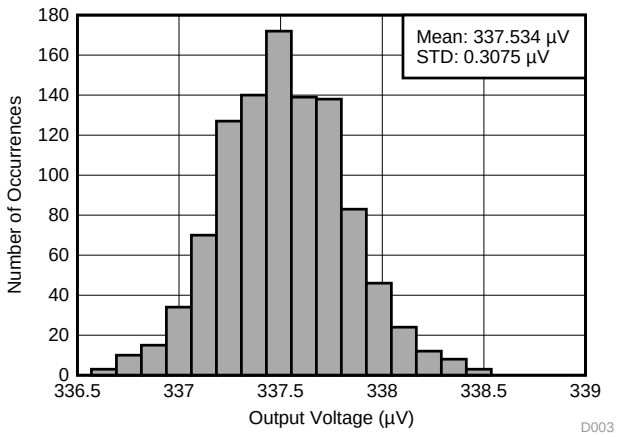


図 25. Distribution at 85°C and 20 SPS

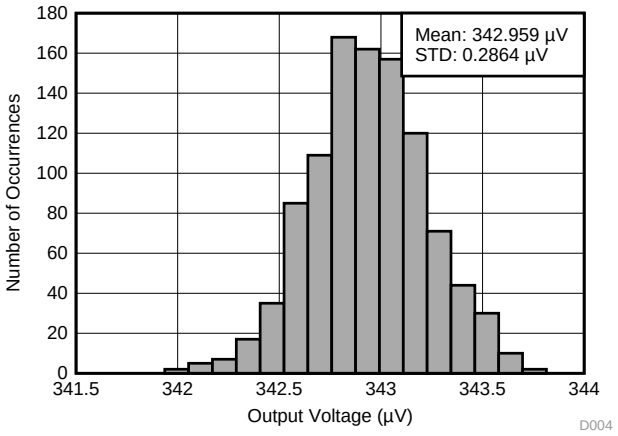


図 26. Distribution at –35°C and 20 SPS

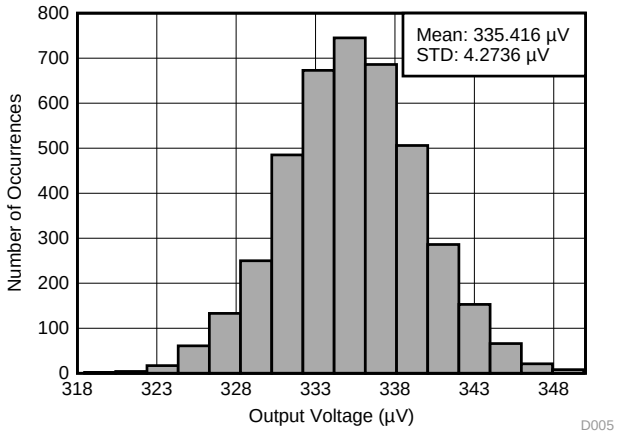


図 27. Distribution at 25°C and 2400 SPS

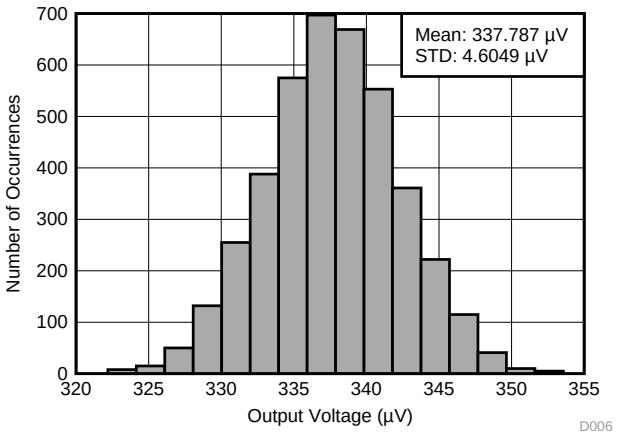


図 28. Distribution at 85°C and 2400 SPS

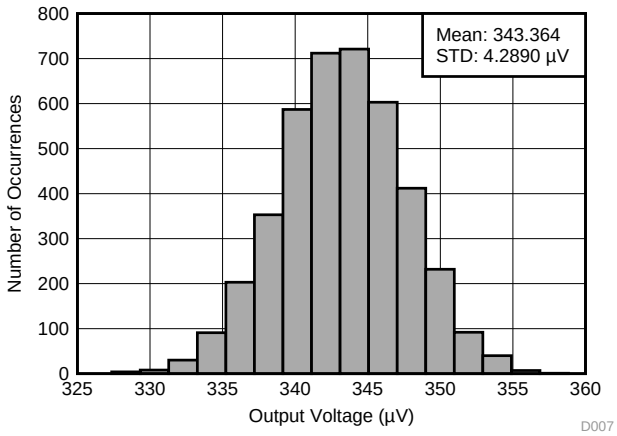


図 29. Distribution at –35°C and 2400 SPS

As expected, the distribution follows a Gaussian curve. Based on the standard deviation of the Gaussian curve, important DC parameters can be calculated. The effective number of bits (式 1) and noise free bits (式 2) can be directly calculated:

$$\text{Effective bits} = \log_2\left(\frac{2^N}{\text{stddev}(\text{histogram})}\right) \quad [N = 32] \tag{1}$$

The number of noise-free bits is 6.6× the standard deviation, or 2.7 bits less than the effective bits, making sure 99.9% of all samples are included.

$$\text{Noise-free bits} = \log_2\left(\frac{2^N}{\text{stddev}(\text{histogram}) \times 6.6}\right) = \text{Effective bits} - 2.7\,\text{bits} \tag{2}$$

With the obtained effective bits and noise-free bits, the input referred noise can be calculated by taking the range of the input range (dependent on gain) into account (式 3 and 式 4). The full-scale range is –2.5 V to 2.5 V = 5 V.

$$\text{RMS noise}\left(\mu V_{RMS}\right) = \frac{\left(\frac{\text{Full-scale range}}{\text{Gain}}\right)}{2^{\text{effective bits}}} \tag{3}$$

$$\text{Peak noise}\left(\mu V_{PP}\right) = \frac{\left(\frac{\text{Full-scale range}}{\text{Gain}}\right)}{2^{\text{noise-free bits}}} \quad (4)$$

表 7 shows the performance for various temperatures and two data rates.

表 7. High-Voltage Mode DC Performance at Various Data Rates and Temperatures

DATA RATE (SPS)	TEMP (°C)	EFFECTIVE BITS	NOISE-FREE BITS	NOISE (μV_{RMS})	NOISE (μV_{PP})	FILTER
20	–35	24.0	21.3	0.287	1.890	SINC4
20	–20	23.9	21.2	0.301	1.984	SINC4
20	0	24.0	21.3	0.285	1.881	SINC4
20	25	24.1	21.4	0.270	1.779	SINC4
20	55	24.0	21.3	0.289	1.907	SINC4
20	85	23.9	21.2	0.308	2.029	SINC4
2400	–35	20.1	17.4	4.289	28.305	SINC1
2400	–20	20.1	17.4	4.224	27.875	SINC1
2400	0	20.1	17.4	4.166	27.494	SINC1
2400	25	20.1	17.4	4.274	28.203	SINC1
2400	55	20.1	17.3	4.396	29.010	SINC1
2400	85	20.0	17.3	4.605	30.389	SINC1

The nominal data rate of 20 SPS was selected for slowly changing (DC-like) signals. For example, if AC signals with a bandwidth up to 1 kHz (anti-aliasing filter limit), a data rate of 2400 SPS with SINC1 filter can be used. This combination provides a –3-dB corner frequency of 1015 Hz.

Another key parameter is the error of the signal chain across the full input range. The test setup uses the SMU B2912A to generate the analog input voltage. The 8.5-digit DMM 3458A measures the voltage and will be used as a reference voltage to measure the error. The setup is drawn in 図 30.

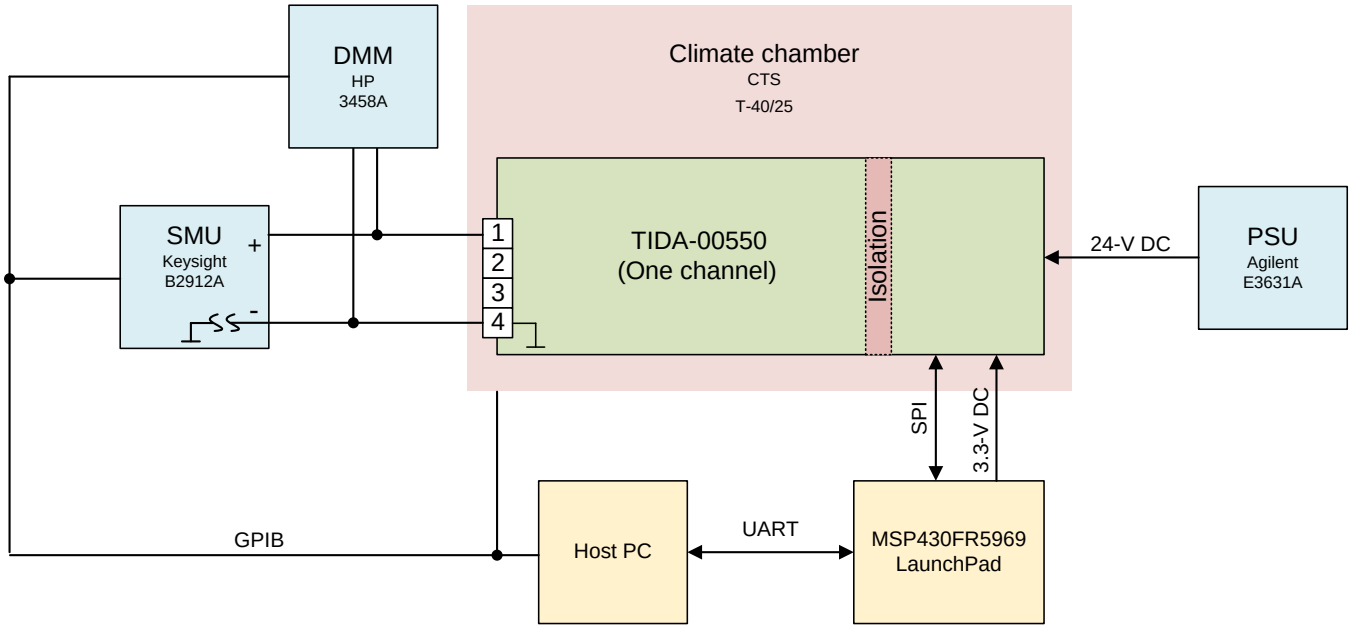


図 30. Test Setup for High-Voltage Full Input Range

The result is plotted in 図 31 and 図 32. Gain calibration was performed at 25°C only. Calibration at other extreme temperature points like –35°C and 85°C might not be feasible during production, but would lead to a smaller error over the entire temperature range, especially since the error is quite linear over the entire input range.

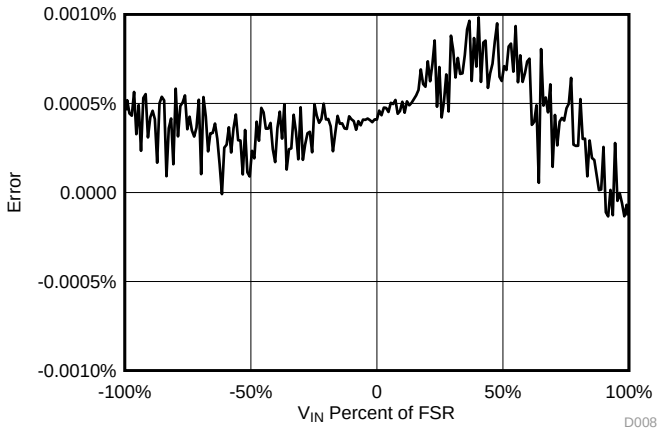


図 31. Input Error at Room Temperature

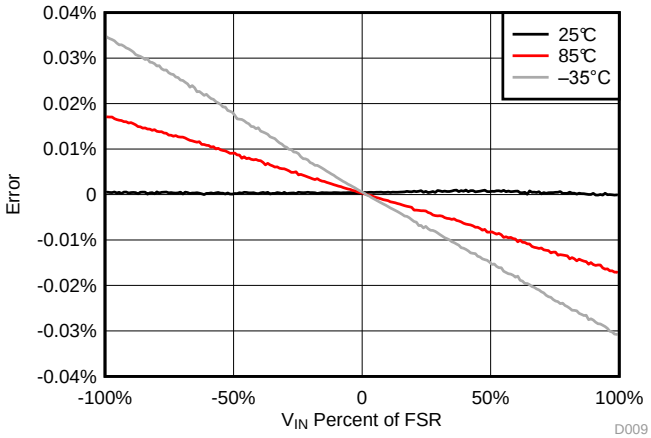


図 32. Input Error at 25°C, 85°C, and –35°C

At calibration temperature, the error is maximal 0.001% (~124 µV). Over temperature range, especially at cold temperatures, the error increases up to 0.035% (~4.3 mV).

All measurements use a gain of 1 V/V in this mode, using the entire voltage range of ±12.39 V. Input signals up to ±6.195 V can use a gain of 2 V/V and input signals up to ±3.0975 V can use a gain of 4 V/V. Signals below ±2.2 V should be measured with the low-voltage mode because the signal is already within the ADS1262 native input range.

4.2 Mode II (Low-Voltage) Measurements

The low-voltage path passes the signal straight to the input of the ADS1262 to avoid additional noise sources, offset, and gain error.

The maximum absolute voltages to terminal pins T2/T3 are ±2.2 V (PGA enabled) and ±2.6 V (1) (PGA disabled). This is not to be confused with the differential input voltage, V_{IN}, which is the difference of the positive and the negative voltage — the actual measured information. The maximum V_{IN} for each PGA gain setting is shown in 表 8.

(1) Note the ADS1262 can measure beyond the supply rails if PGA is disabled.

表 8. Full-Scale Voltage Input Ranges

PGA GAIN (V/V)	FULL SCALE RANGE
1	±2.2 V
2	±1.25 V
4	±0.625 V
8	±0.3125 V
16	±0.15625 V
32	±0.078125 V
Bypass	±2.6 V

The minimum and maximum absolute voltages on the positive input, V_{INP}, and on the negative input, V_{INN}, are dependent on the PGA gain, the differential input voltage, and the tolerance of the power supply voltages AVDD and AVSS:

$$V_{INP} > AVSS + 0.3\ V + \left|V_{IN}\right| \times \frac{(Gain - 1)}{2}$$

$$V_{INN} < AVDD - 0.3\ V - \left|V_{IN}\right| \times \frac{(Gain - 1)}{2}$$

The anti-aliasing filter has a cut-off frequency of 142 Hz, making it suitable for DC signals. If more bandwidth is required, the cut-off frequency can be adapted.

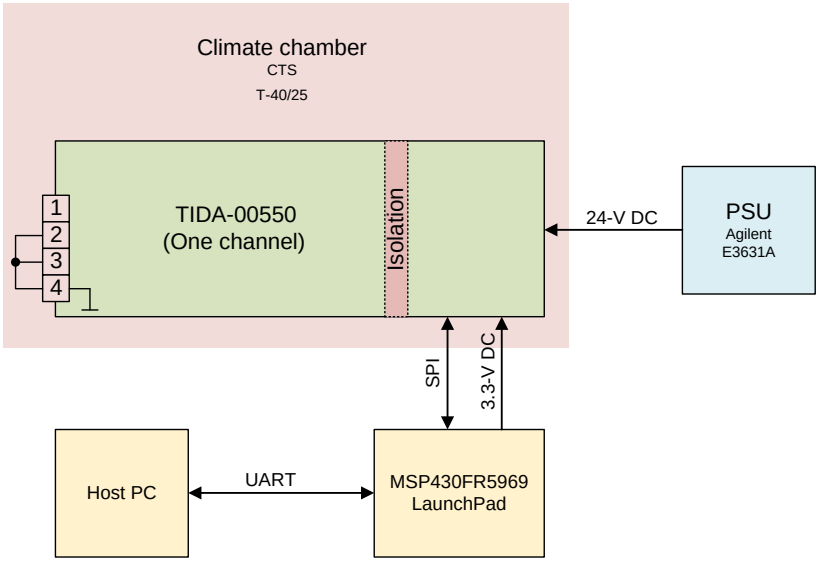


図 33. Test Setup for Low-Voltage Noise Measurement

Performance measurements of DC-like signals are important to understand how many effective and noise-free bits can be expected from slowly changing signals like temperature sensors deliver. 図 34 to 図 36 show the histogram for a gain of 1 V/V for various temperatures while 図 37 to 図 39 show measurements with a gain of 32 V/V. As expected, the mean and standard deviation at a gain of 32 V/V is about 32 times lower than a gain of 1 V/V due to the reduced analog input range. All histograms are uncalibrated, meaning no offset calibration or chopping, to show the system offset.

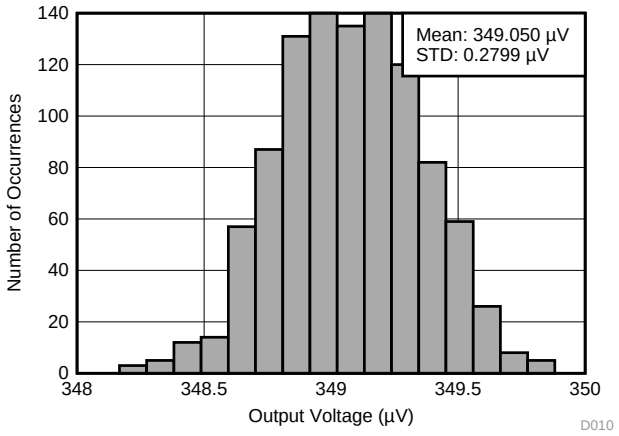


図 34. Distribution at 25°C and Gain 1 V/V

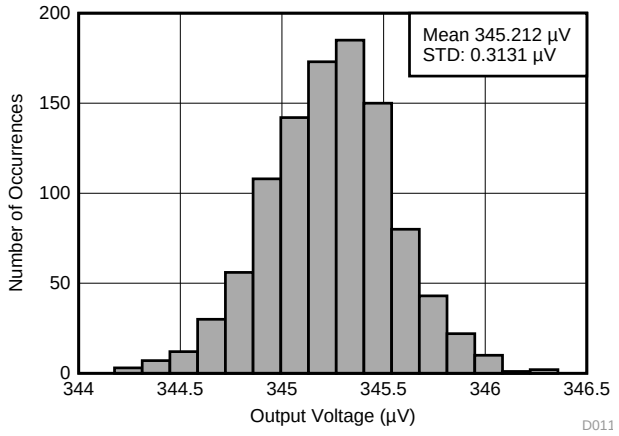


図 35. Distribution at 85°C and Gain 1 V/V

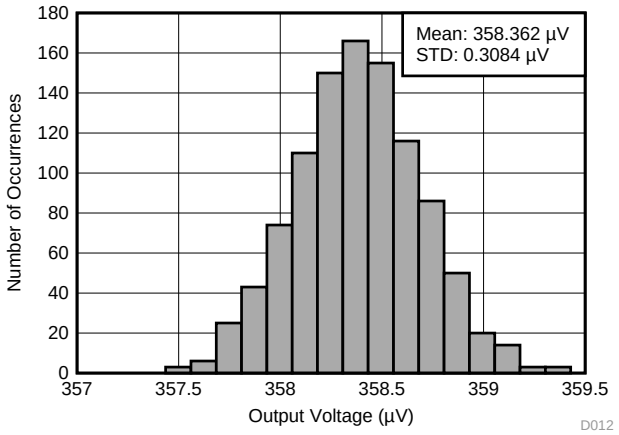


図 36. Distribution at –35°C and Gain 1 V/V

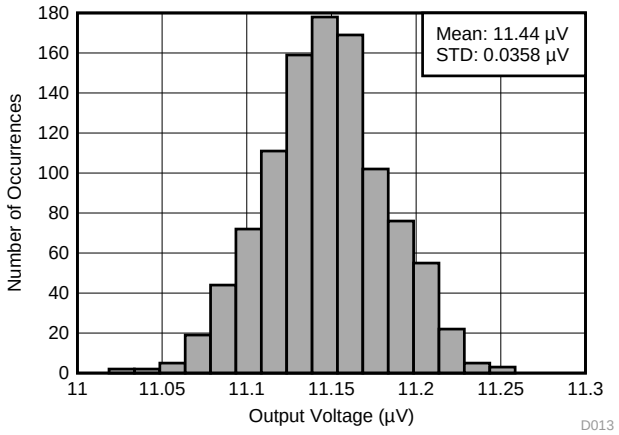


図 37. Distribution at 25°C and Gain 32 V/V

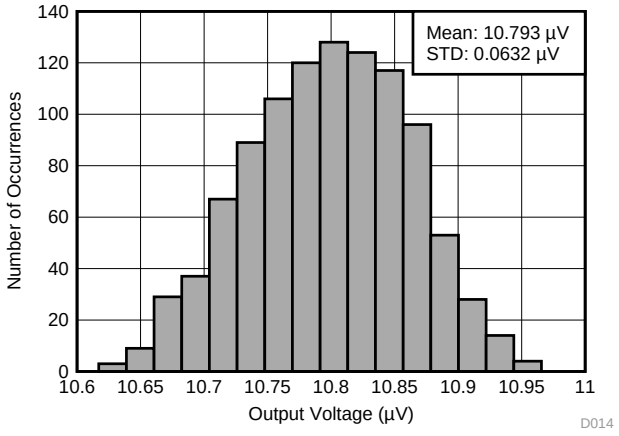


図 38. Distribution at 85°C and Gain 32 V/V

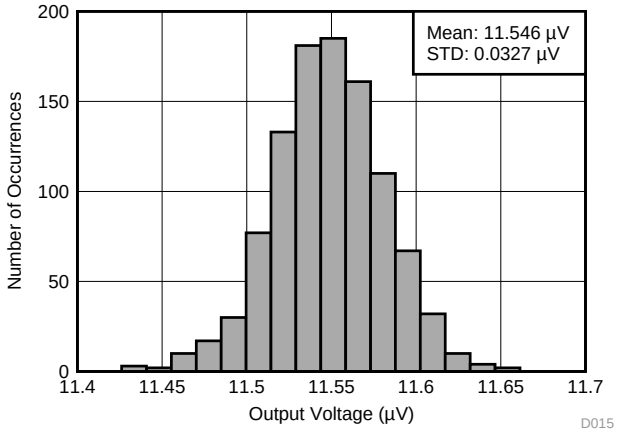


図 39. Distribution at –35°C and Gain 32 V/V

表 9 shows the effective bits, noise-free bits, and noise resulting from the standard deviation for several temperature-gain combinations. For all measurements, a data rate of 20 SPS and SINC4 filter was selected.

表 9. DC Performance Low-Voltage Mode

TEMP (°C)	GAIN (V/V)	EFFECTIVE BITS	NOISE-FREE BITS	NOISE (μV_{RMS})	NOISE (μV_{PP})
–35	1	24.0	21.2	0.308	2.028
	2	24.0	21.3	0.145	0.951
	4	23.9	21.2	0.080	0.525
	8	23.7	21.0	0.047	0.308
	16	23.1	20.4	0.035	0.226
	32	22.3	19.6	0.031	0.200
	Bypass	23.4	20.7	0.458	3.020
–20	1	24.0	21.3	0.292	1.924
	2	24.0	21.3	0.149	0.977
	4	24.0	21.2	0.077	0.503
	8	23.6	20.9	0.049	0.322
	16	23.1	20.3	0.036	0.237
	32	22.2	19.5	0.033	0.214
	Bypass	23.7	21.0	0.370	2.437
0	1	24.1	21.4	0.279	1.838
	2	24.1	21.4	0.137	0.898
	4	24.0	21.2	0.078	0.509
	8	23.6	20.9	0.049	0.318
	16	22.9	20.2	0.041	0.268
	32	22.1	19.3	0.036	0.235
	Bypass	23.8	21.1	0.339	2.236
25	1	24.1	21.4	0.277	1.828
	2	24.1	21.4	0.140	0.923
	4	23.9	21.2	0.078	0.515
	8	23.6	20.9	0.050	0.326
	16	23.0	20.3	0.038	0.249
	32	22.1	19.4	0.035	0.231
	Bypass	24.0	21.3	0.294	1.935
55	1	24.0	21.3	0.293	1.933
	2	24.0	21.3	0.150	0.984
	4	23.9	21.1	0.083	0.544
	8	23.5	20.8	0.052	0.341
	16	22.9	20.2	0.041	0.269
	32	22.0	19.3	0.038	0.250
	Bypass	24.0	21.3	0.292	1.927
85	1	23.9	21.2	0.312	2.059
	2	24.0	21.2	0.155	1.018
	4	23.6	20.9	0.096	0.633
	8	23.1	20.4	0.070	0.460
	16	22.3	19.6	0.060	0.396
	32	21.4	18.6	0.058	0.383
	Bypass	23.8	21.1	0.332	2.189

The test setup is shown in 図 40 and the measurements results are shown in 図 41 to 図 44.

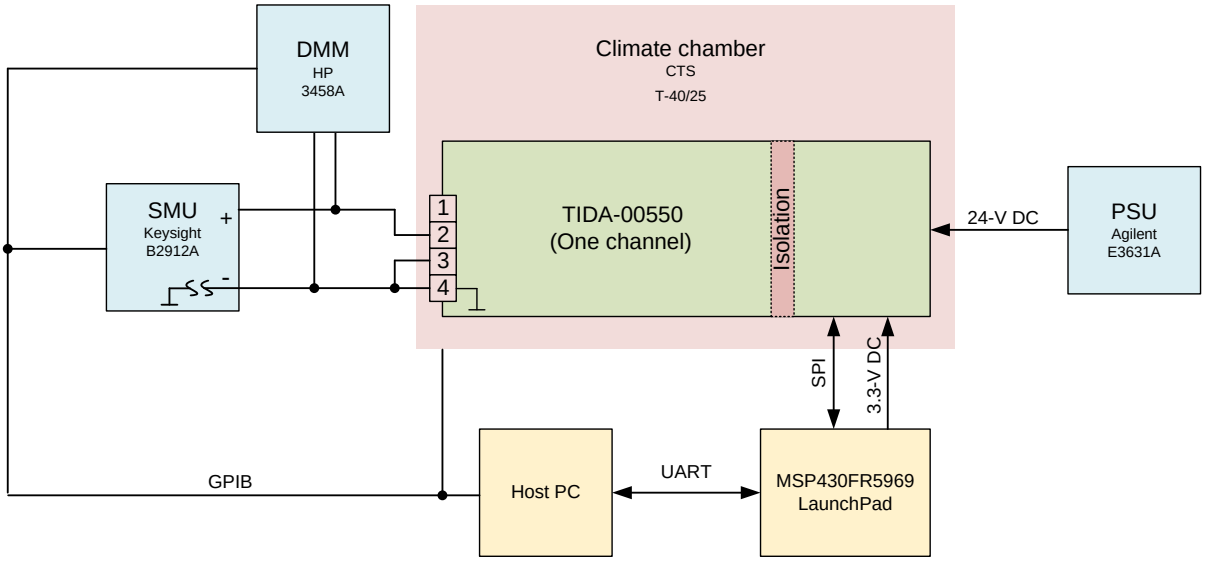


図 40. Test Setup for Low-Voltage Full Input Range

To get highest data rate using the FIR filter a data rate of 20 SPS was chosen. This way one can get a fairly high (for example, temperature) update rate while proper 50- or 60-Hz rejection is performed. Thus, this system can be used across continents without the need of main frequency adaption. On top of that, the usage of the FIR filter provides a better bandwidth-to-data rate ratio compared to SINC filter. While the best –3-dB bandwidth is 8.85 Hz (SINC1), the FIR reaches 13 Hz (which depends on the type of analog input signal whether this is an advantage or disadvantage, of course). Last but not least, the FIR is the single-cycle fully settled conversion. For SINC filters, the required number for fully settled samples is dependent on the order (SINC1 = 1, SINC5 = 5, and so on).

The input error for the measurements at room temperature stays below 0.001% for a gain of 1 V/V and does not change significantly for gains up to 32 V/V. The error towards higher temperature stays about the same while it increases for temperatures colder ambient temperatures.

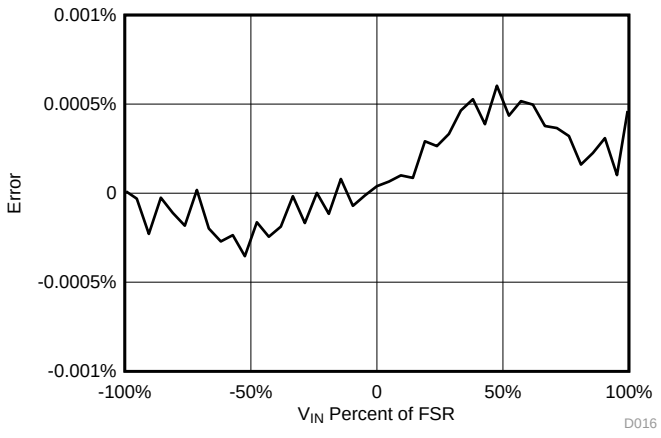


図 41. Input Error at 25°C

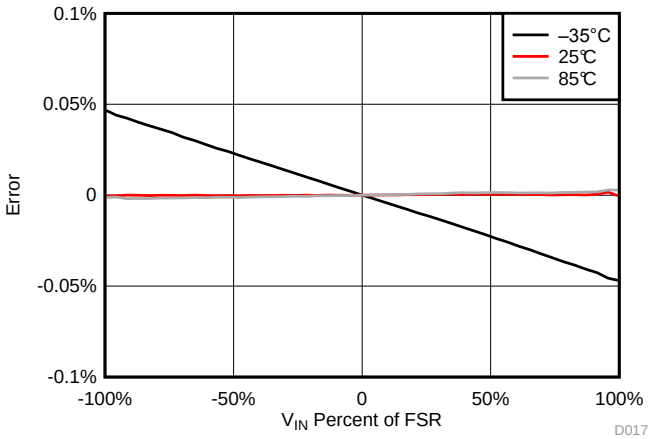


図 42. Input Error at Border Temperatures

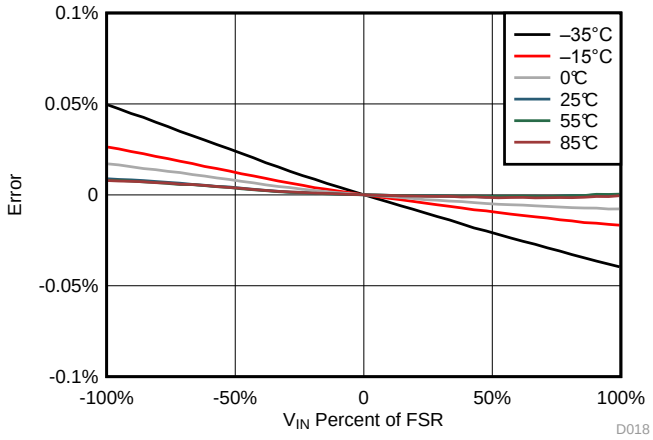


図 43. Input Error 25°C, All Gain

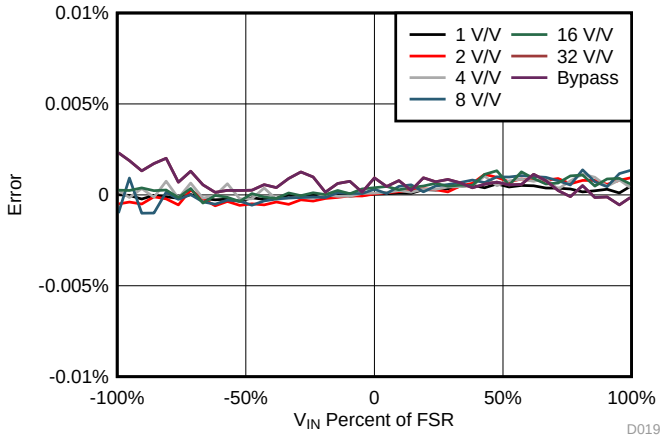


図 44. Input Error at Gain 32, All Temps

4.3 Mode III (Current-Mode) Measurements

The current measurement mode uses terminal input 2 and 3, the same as for low-voltage measurements, but internally a different pair of AD1262 input pins. This enables the measurement of the voltage drop across the burden resistor R25 only — leaving R_{DSON} of K3 out of the equation. In this configuration the accuracy and temperature stability is dominated by R25 (0.1%, 10 ppm).

The voltage drop over the resistor should be as small as possible; as a result, the resistor value should be low. Benefits are the lower power dissipation (less self-heating) of the burden resistor and the measurement of higher currents. On the other side, the burden resistor has to provide a certain voltage to maintain precise measurements of smaller currents. It is a trade-off in terms of dynamic range and power dissipation. The TIDA-00550 uses a 27.4-Ω resistor and accepts the current input ranges shown in 表 10 with this value. The minimum voltage is the voltage required for a reliable current measurement.

表 10. Full-Scale Current Input Ranges

PGA GAIN (V/V)	FULL SCALE RANGE	MINIMUM VOLTAGE
1	±55.0 mA	±2.4 V
2	±45.6 mA	±2.00 V
4	±22.8 mA	±1.00 V
8	±11.4 mA	±0.50 V
16	±5.7 mA	±0.25 V
32	±2.85 mA	±0.13 V

The entire input voltage range at PGA gain 1 V/V is not used. The reason is the max power dissipation of R25 rated 0.1 W up to 70°C (0.08 W at 85°C). With a voltage drop of ±2.2 V (full input range), the power dissipation would be 0.18 W. The maximum current of 55 mA is still state of the art. If one requires the full input of 80 mA, a resistor with higher power dissipation rating is recommended. The test setup diagram given in 図 45 is the same for low-voltage noise measurement.

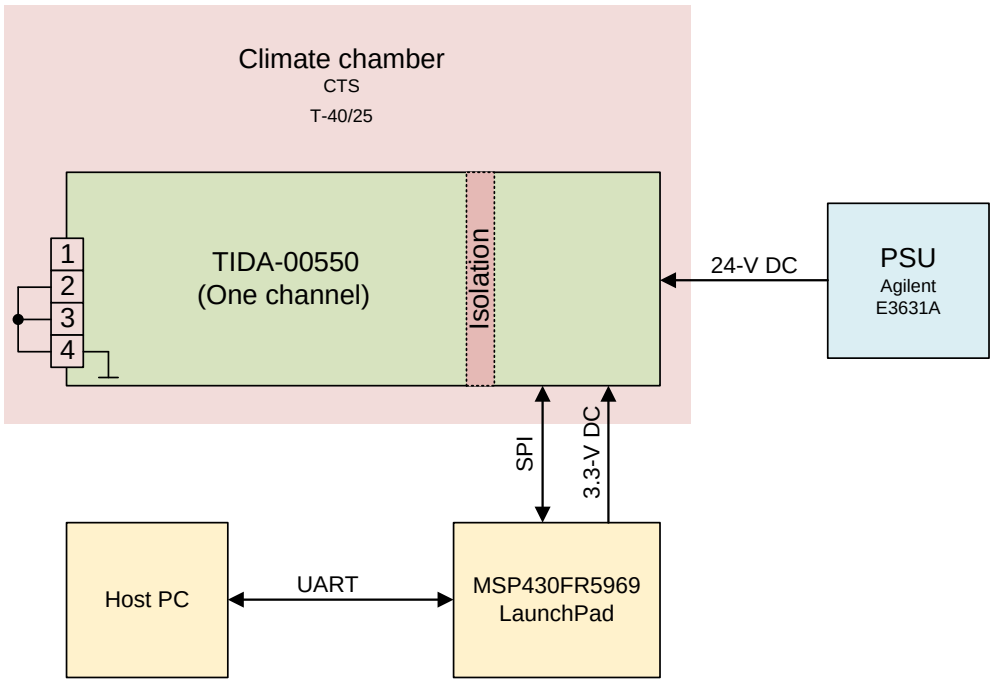


図 45. Test Setup for Current Noise Measurement

図 46 to 図 51 show the histograms of the current input with gain of 1 V/V and 32 V/V at different temperatures.

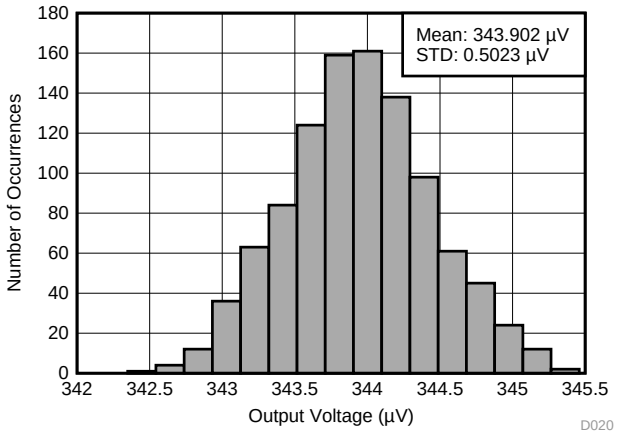


図 46. 20 SPS, Gain: 1 V/V, Temp: 25°C

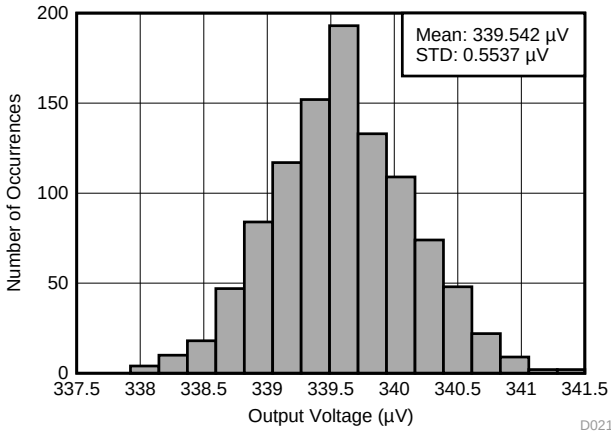


図 47. 20 SPS, Gain: 1 V/V, Temp: 85°C

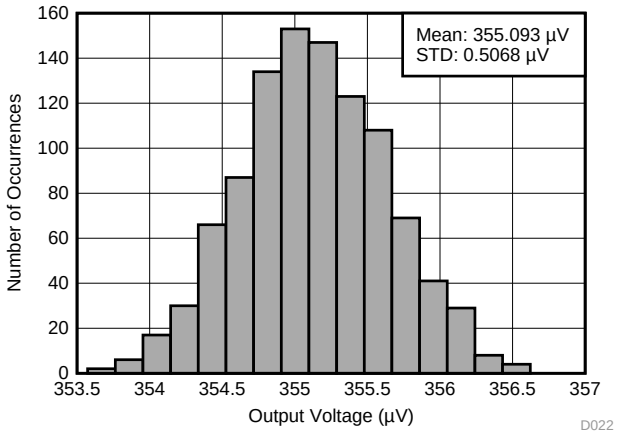


図 48. 20 SPS, Gain: 1 V/V, Temp: –35°C

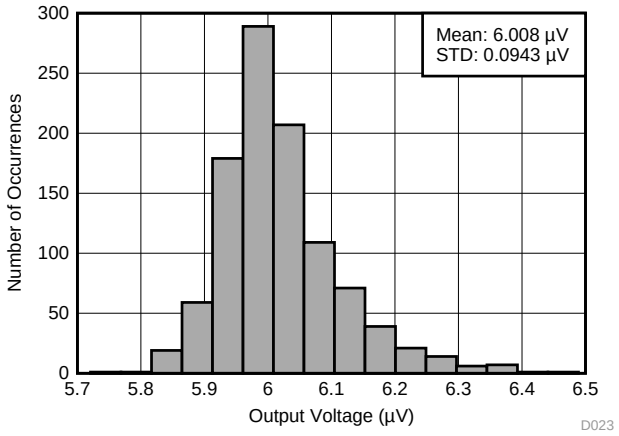


図 49. 20 SPS, Gain: 32 V/V, Temp: 25°C

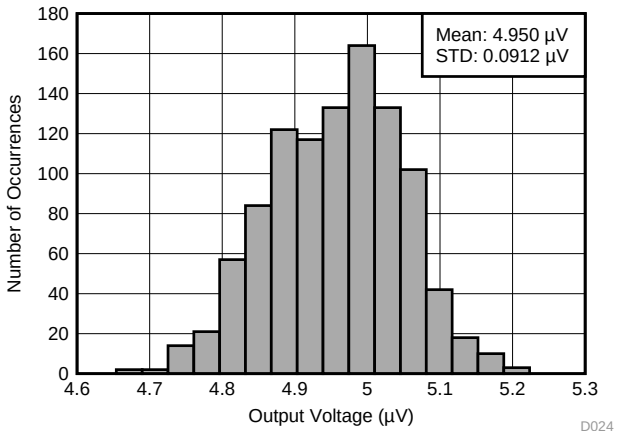


図 50. 20 SPS, Gain: 32 V/V, Temp: 85°C

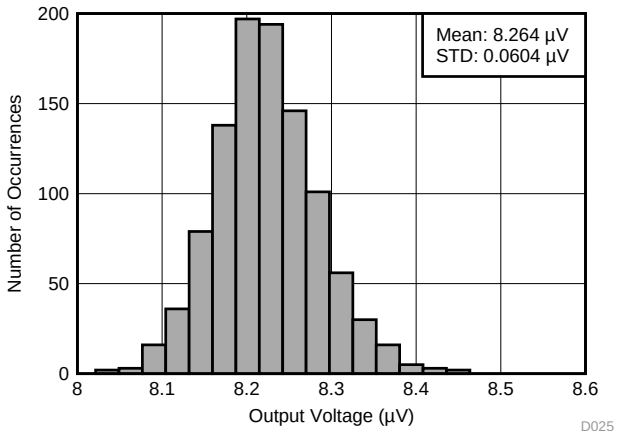


図 51. 20 SPS, Gain: 32 V/V, Temp: –35°C

The noise measurement is shown in 表 11. Compared to the voltage input paths, the current input path effective and noise-free bits are about 0.8 bits less. The main reason for this performance drop is the layout, which is not optimal due to space constrains. While the signals traces from terminal pin 2 and 3 for the voltage path are symmetrical, this is not the case for the current path.

表 11. DC Performance Current Mode

TEMP (°C)	GAIN (V/V)	EFFECTIVE BITS	NOISE-FREE BITS	NOISE (μV_{RMS})	NOISE (μV_{PP})
–35	1	23.2	20.5	0.507	3.344
	2	23.2	20.5	0.262	1.728
	4	23.1	20.4	0.139	0.914
	8	22.8	20.1	0.084	0.551
	16	22.3	19.5	0.063	0.413
	32	21.4	18.7	0.058	0.379
	Bypass	22.8	20.1	0.687	4.530
–20	1	23.2	20.5	0.512	3.379
	2	23.2	20.5	0.258	1.699
	4	23.1	20.4	0.141	0.927
	8	22.7	20.0	0.090	0.591
	16	22.1	19.4	0.069	0.452
	32	21.3	18.6	0.059	0.390
	Bypass	23.1	20.3	0.572	3.772
0	1	23.3	20.6	0.485	3.196
	2	23.2	20.5	0.260	1.711
	4	23.1	20.3	0.144	0.949
	8	22.7	20.0	0.091	0.598
	16	22.1	19.4	0.070	0.459
	32	21.2	18.5	0.064	0.422
	Bypass	23.1	20.4	0.565	3.729
25	1	23.2	20.5	0.503	3.314
	2	23.2	20.5	0.264	1.737
	4	22.9	20.2	0.155	1.019
	8	22.4	19.7	0.115	0.755
	16	21.5	18.8	0.106	0.697
	32	20.7	17.9	0.095	0.622
	Bypass	23.2	20.5	0.506	3.337
55	1	23.2	20.5	0.517	3.409
	2	23.2	20.4	0.265	1.747
	4	23.0	20.3	0.147	0.969
	8	22.7	19.9	0.095	0.623
	16	22.0	19.3	0.074	0.488
	32	21.1	18.4	0.069	0.454
	Bypass	23.2	20.5	0.504	3.327
85	1	23.2	20.5	0.520	3.432
	2	23.1	20.4	0.271	1.788
	4	22.9	20.2	0.156	1.024
	8	22.4	19.7	0.113	0.743
	16	21.6	18.9	0.096	0.629
	32	20.7	18.0	0.092	0.602
	Bypass	23.2	20.5	0.524	3.453

The error over the analog input range is about 0.002% at room temperature. Like the voltage results, the error is dependent on the temperature, not on the gain setting. The test setup is shown in , and the results with different gains and ambient temperatures in 図 53 to 図 56.

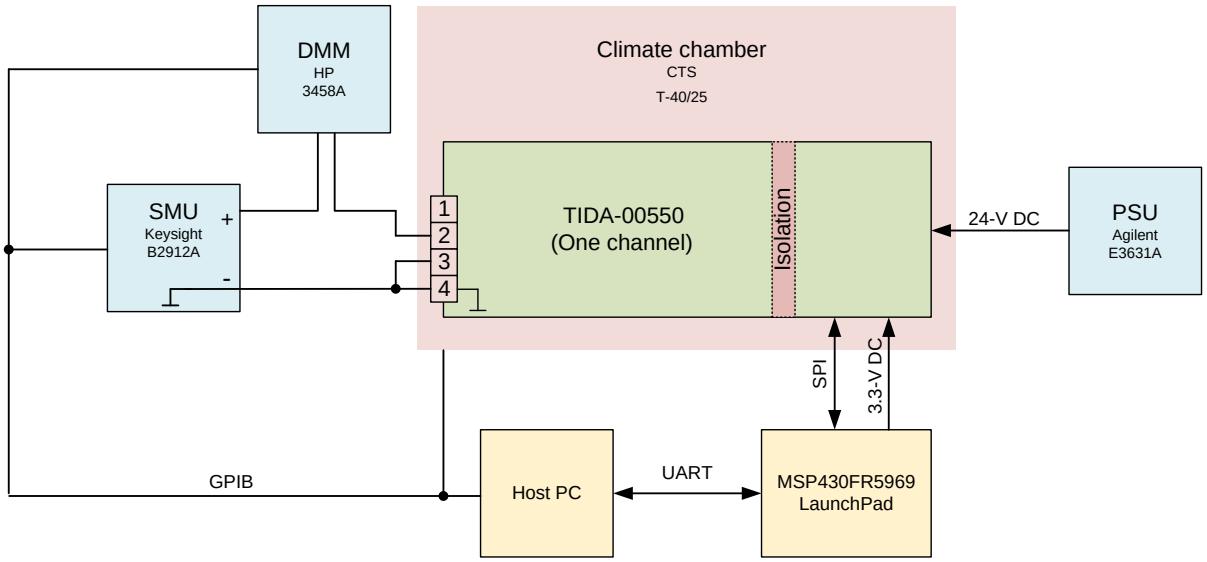


図 52. Test Setup for Current Input Range

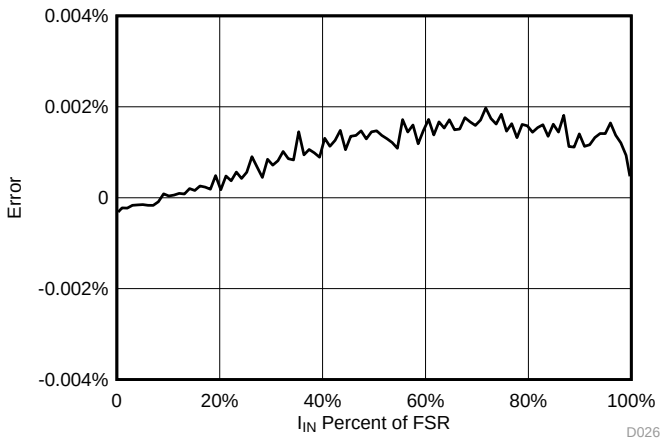


図 53. Input Error at 25°C

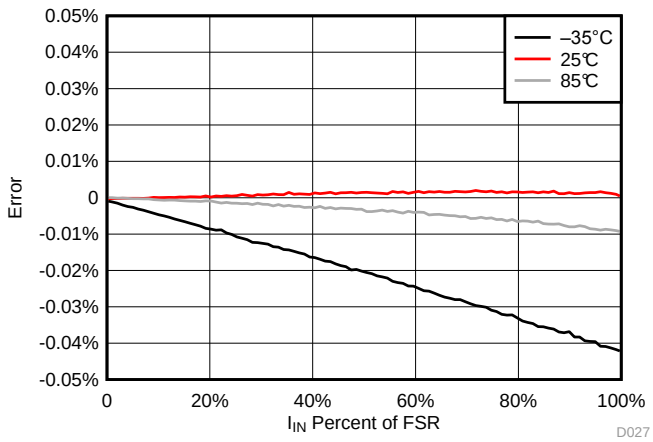


図 54. Input Error Over Temperature

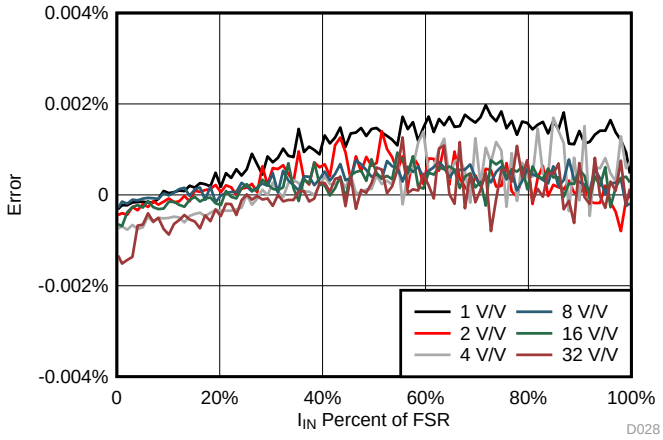


図 55. Input Error at Various Gains

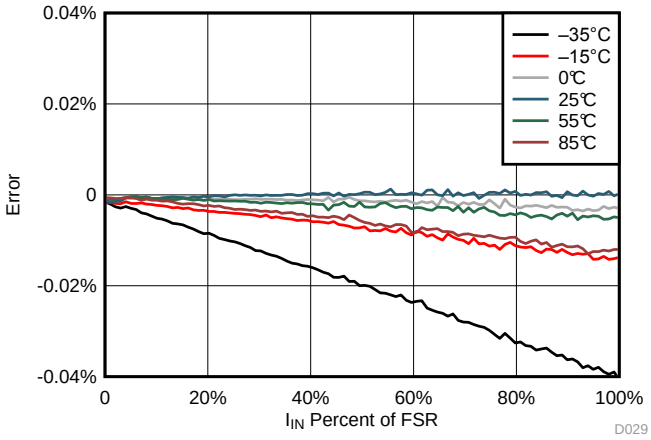


図 56. Input Error Gain of 32 V/V and Various Temperatures

4.4 Mode IV (4- to 20-mA Loop Mode) Measurements

The 4- to 20-mA loop mode is designed for connecting sensor transmitters with the 4- to 20-mA interface to the TIDA-00550. It uses Mode III (current) with a fixed PGA gain setting of 4 V/V for best modulation of the ADS1262 analog input range. As shown in 表 10, up to 22.8 mA can be measured with this gain stage. The analog bandwidth of a 4- to 20-mA is specified to 25 Hz. The analog bandwidth of the FIR filter at 20 SPS is 13 Hz. It depends on the application whether this bandwidth is enough or a SINC filter with higher data rate should be used. 図 57 shows the error at gain of 4 V/V and FIR filter.

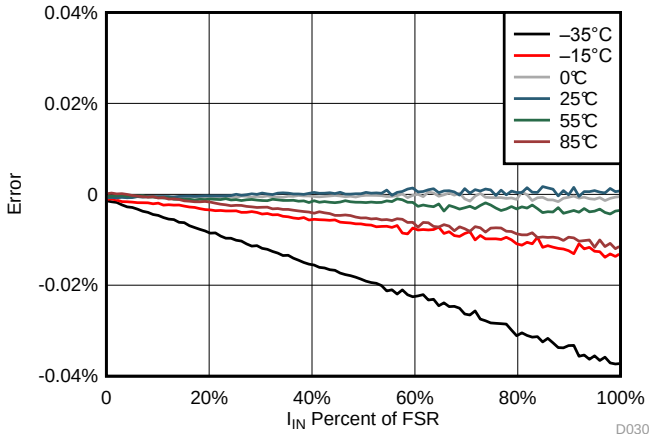


図 57. 4- to 20-mA Loop Error Over Temperature

The effective bits of 23 (noise-free bits of 20.3) are more than sufficient since common sensor transmitters output not more than 16 bits.

表 12. 4- to 20-mA System Noise

TEMP (°C)	GAIN (V/V)	EFFECTIVE BITS	NOISE-FREE BITS	NOISE (μV_{RMS})	NOISE (μV_{PP})
–35	4	23.1	20.4	0.139	0.914
–15	4	23.1	20.4	0.141	0.927
0	4	23.1	20.3	0.144	0.949
25	4	22.9	20.2	0.155	1.019
55	4	23.0	20.3	0.147	0.969
85	4	22.9	20.2	0.156	1.024

4.5 Mode V (Thermocouple) Measurements

The thermocouple mode uses the low-voltage mode path. By nature, thermocouples provide a floating voltage. To reference this voltage to the system, the ADS1262 built-in V_{BIAS} feature is used, which provides a reference input voltage for isolated sensors on pin AINCOM. The generated voltage is $V_{BIAS} = (V_{AVDD} + V_{AVSS}) / 2 = 0$ V (for a ±2.5-V analog supply). Here, this pin is connected to terminal pin 2, which is the positive input of the thermocouple signal. The thermocouple voltage range is very small relative to the ADC input range of ±2.2 V. For type K thermocouples, for instance, the expected voltage is –6.5 to 54.9 mV for the full temperature range of –270°C to 1372°C. This fits well in PGA gain setting 32 V/V with an input voltage range of ±78 mV. 図 58 shows the test setup.

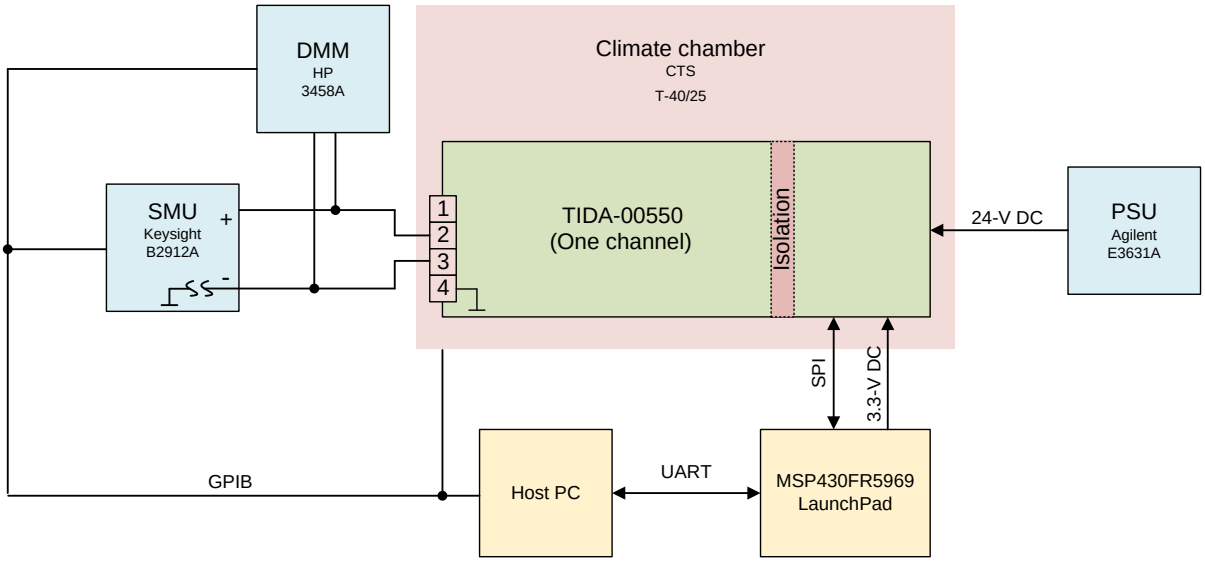


図 58. Test Setup for Thermocouple Measurement

The higher error at negative temperatures at the thermocouple (see 図 59) results from a smaller ΔV/ΔC in this region. For example, ΔV/ΔC from 100°C to 200°C is 4.042 mV/100°C while from –100°C to –200°C is only 2.337 mV/100°C. As seen in the low voltage measurements (see 4.2), the error at this small voltage range is symmetrical, thus resulting in the higher error of the TC at negative temperatures.

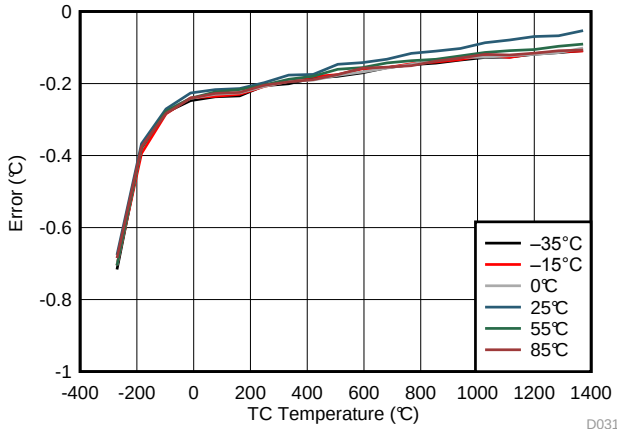


図 59. TC Error (°C) at Various Ambient Temperatures

4.6 Mode VI (RTD) Measurements

During the tests, the 3-wire connection method was measured because it is the most complex connection using both current sources. 図 60 shows the test setup.

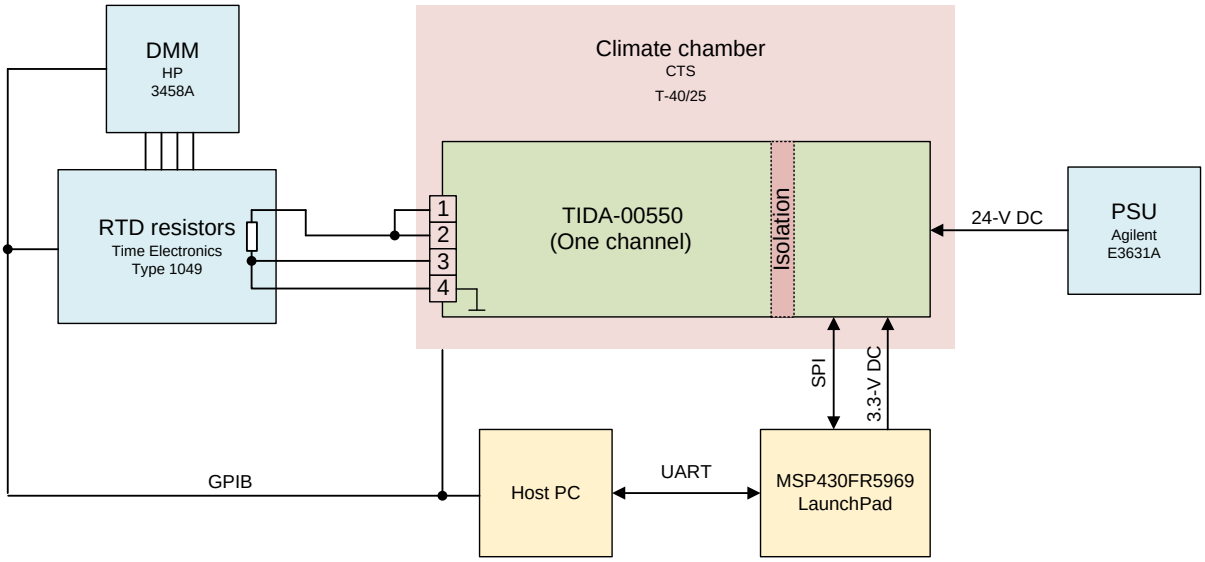


図 60. Test Setup for 3-Wire RTD Measurement

A resistor network from Time electronics for RTD resistor emulation comes into play here. It provides 13 resistors to generate the temperature points between –200°C and 800°C. The accuracy of the resistors is ±0.65°C for higher temperatures. Since much better results are expected from the TIDA-00550, the exact resistor values must be determined first. To get most precise results, the following steps were performed for each temperature point:

1. Set the desired temperature point on the resistor network.
2. Measure the resistance with the 8.5-digit DMM using the 4-wire measurement method.
3. The resistance measured leads to an updated provided temperature point by the RTD network.
4. Connect the resistor network to the terminal inputs using the 3-wire connection and perform the actual measurement. The updated temperature point was taken into account to obtain the error shown in 図 61.

This way, the resistance of the mechanical selector of the temperature point in the RTD emulator should stay the same, but the contact resistance due to rewiring from the DMM to the TIDA-00550 may vary.

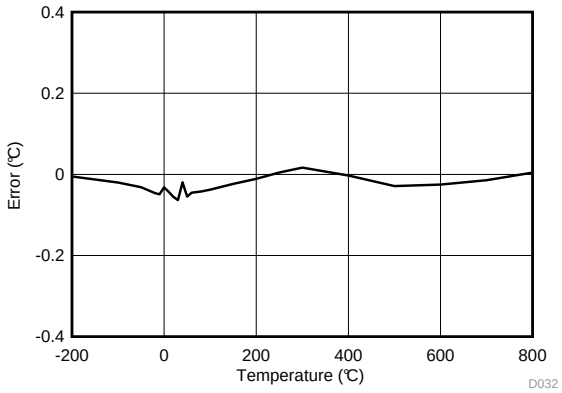


図 61. RTD Error Measurement

The max temperature error measured is 0.065°C over the entire RTD temperature range. For proper measurement, the ADS1262 analog supply voltage is set to –1.7-V/3.3-V mode.

4.7 4- to 20-mA Loop Power Supply Measurements

The loop power supply provides the energy for the remote 4- to 20-mA transmitter at terminal pin 1. The curve was created by connecting a standard resistor network from terminal 1 to ground (図 62).

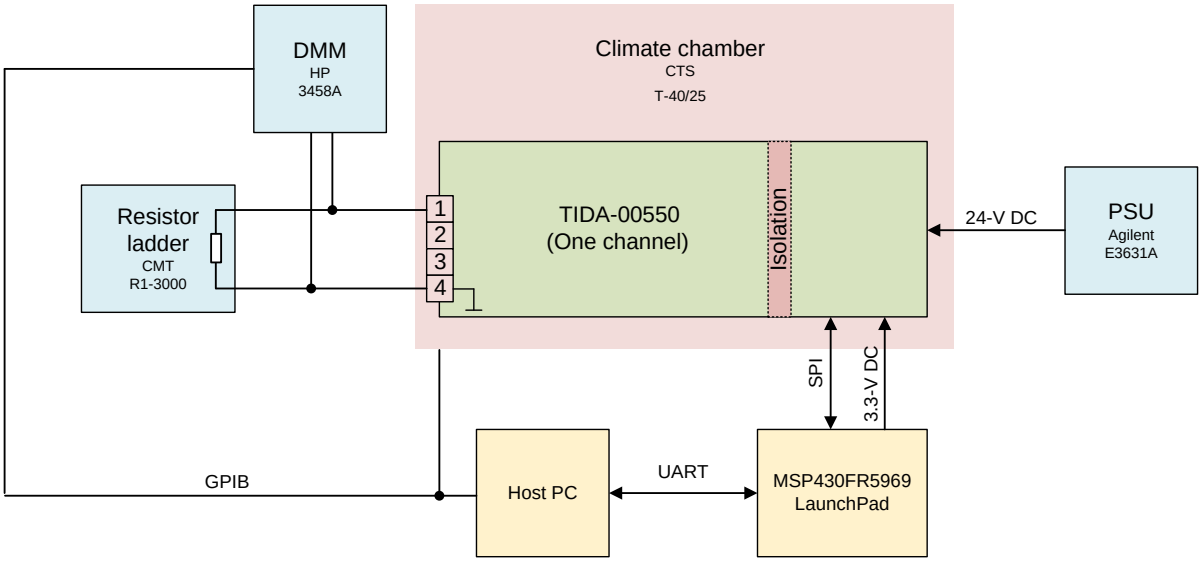


図 62. Test Setup for 4- to 20-mA Loop PSU

Since the resistor value is known and the voltage over the resistor is measured, the current can easily be calculated using R = U × I. 図 63 shows the output voltage based on the current drawn by the transmitter.

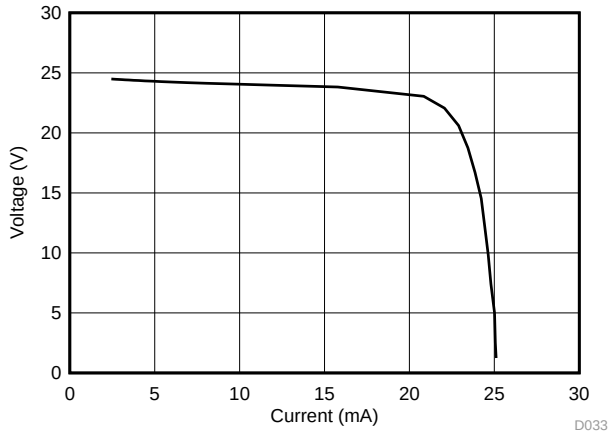


図 63. Dependency of Output Voltage on Drawn Current

The output voltage has a good stability in the target range of 4 to 20 mA while it decreases rapidly beyond 22 mA. The curve is strongly dependent on resistor R46 (20.5 Ω). Changing the value of resistor to a smaller value will push the knee of the curve towards higher current values and vice versa.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00550.

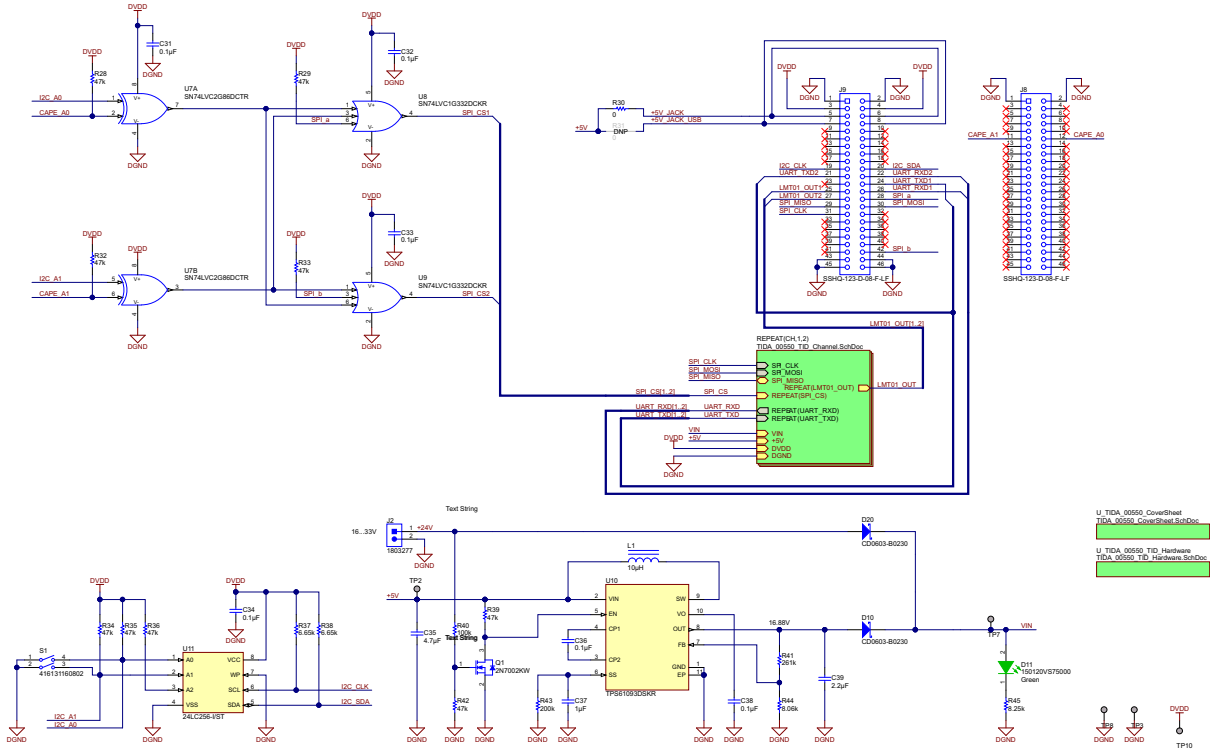


図 64. BeagleBone Cape Functionality (Main Top Level Sheet)

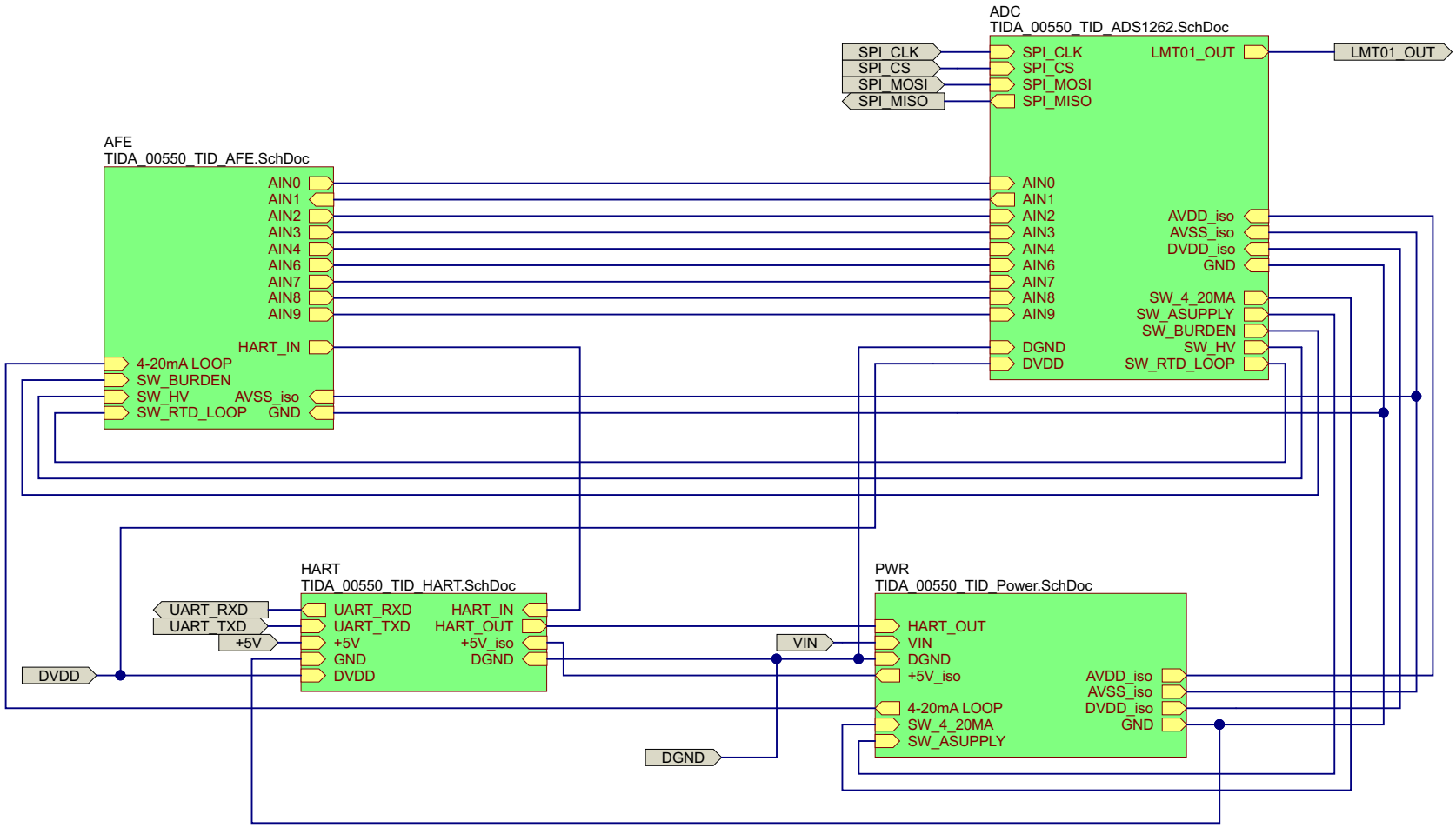
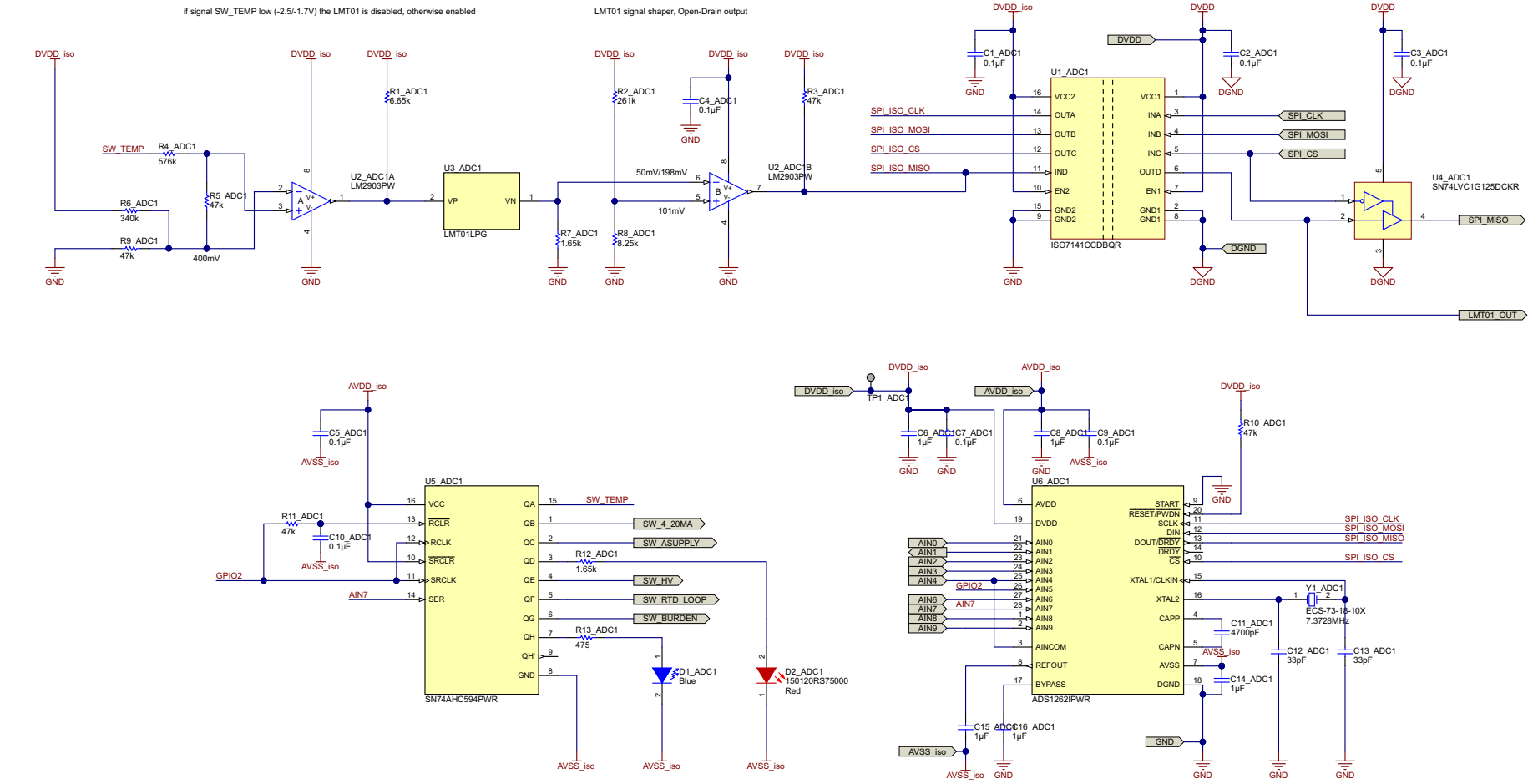


図 65. Per Channel Top Level Sheet



AIN9 is normally connected to GND over 5kOhm -> can be used as temporary Data line
OE (594: RCLR) controlled over longer periods of high and low of GPIO0

図 66. ADC, LMT01, GPO, and Isolation Schematics

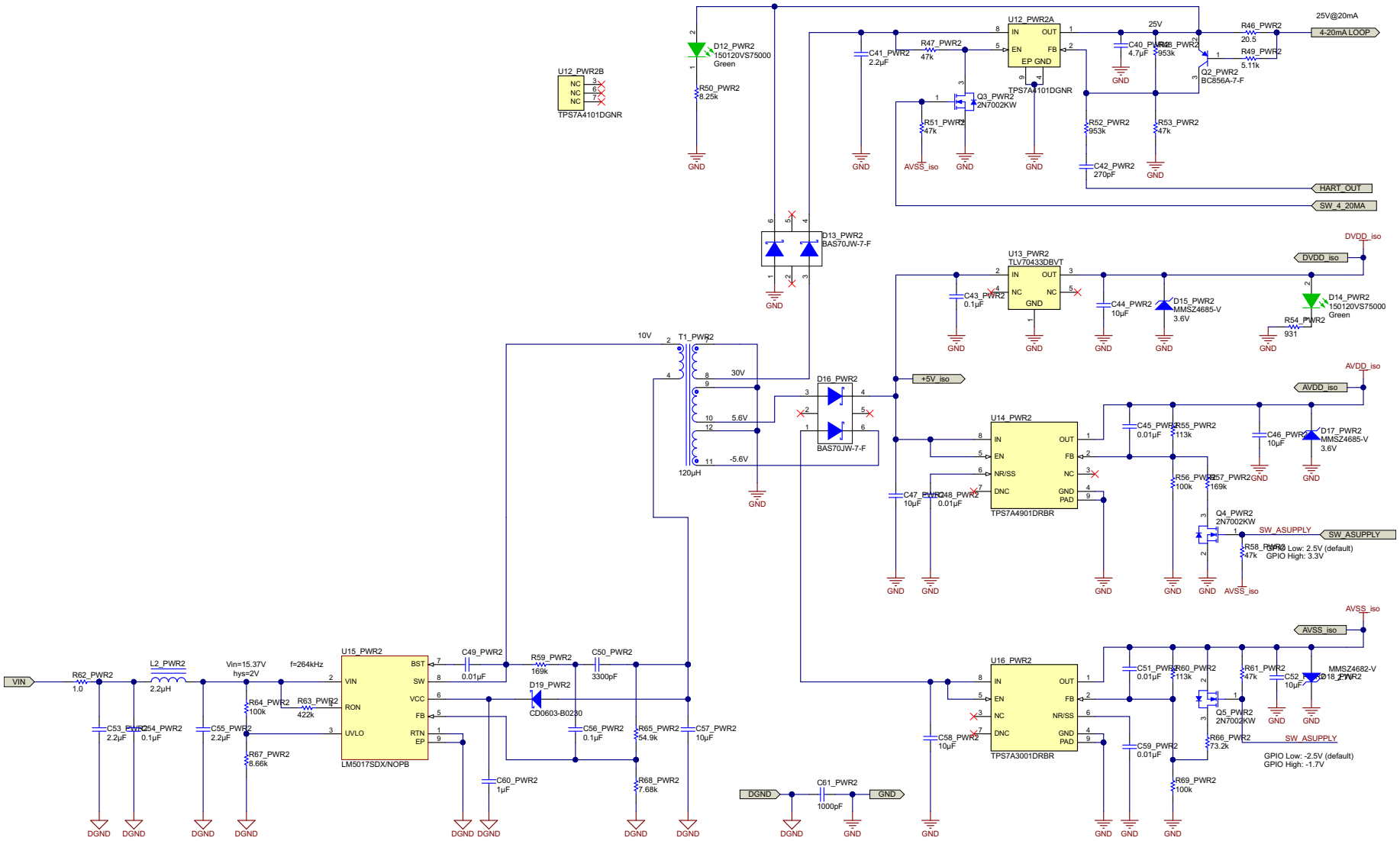


図 67. Power Schematics

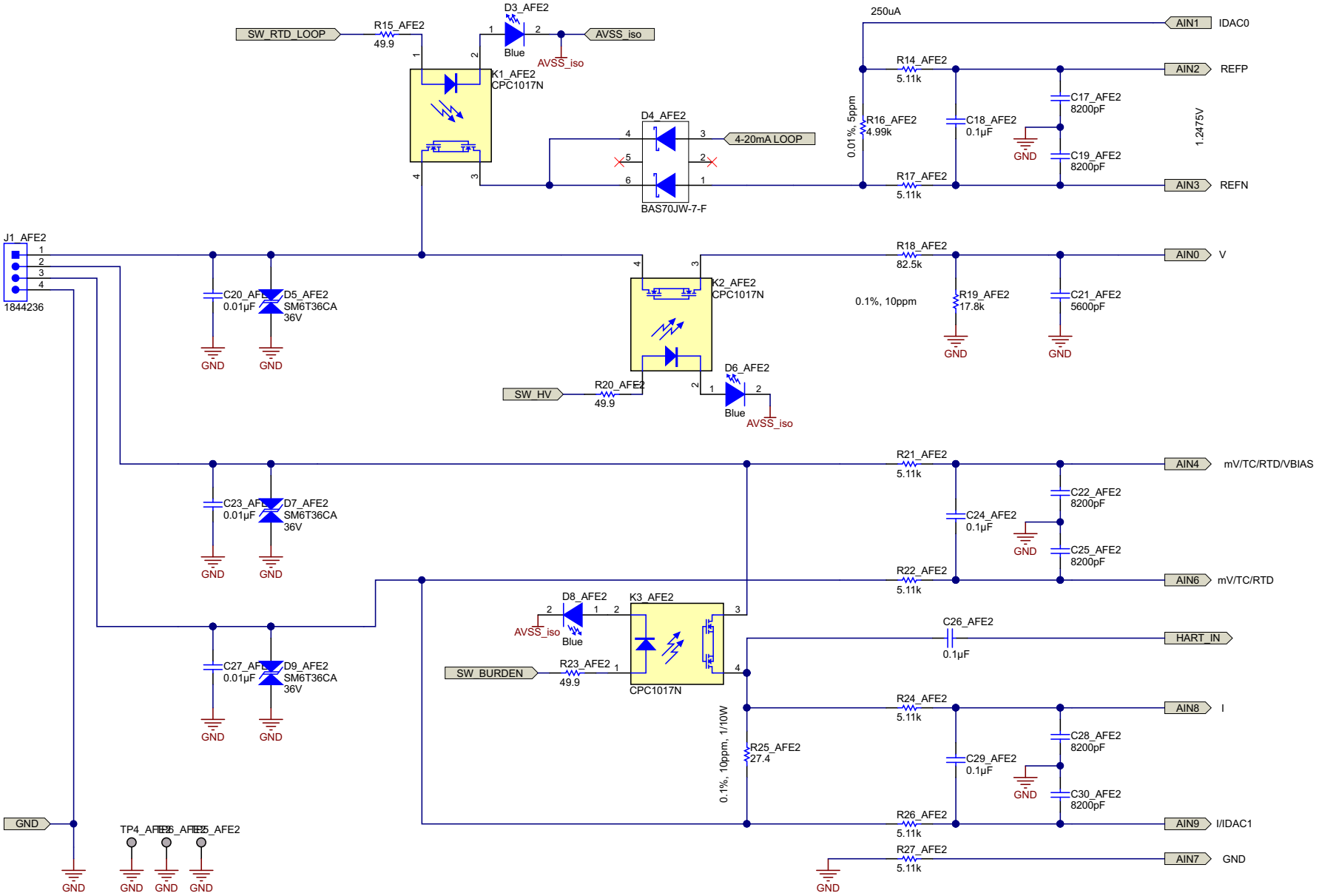


図 68. AFE Schematics

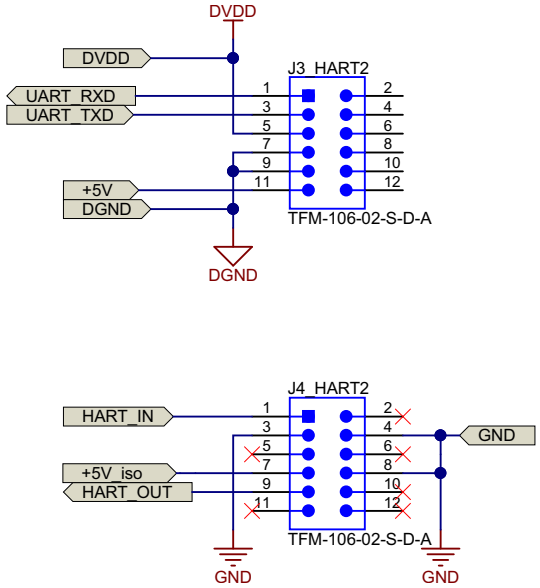


図 69. HART Connection Schematics

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00550.

表 13. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-00550	Any	Printed Circuit Board	
2	C1_ADC1, C1_ADC2, C2_ADC1, C2_ADC2, C3_ADC1, C3_ADC2, C4_ADC1, C4_ADC2, C5_ADC1, C5_ADC2, C7_ADC1, C7_ADC2, C9_ADC1, C9_ADC2, C10_ADC1, C10_ADC2, C26_AFE1, C26_AFE2, C31, C32, C33, C34, C36, C38, C43_PWR1, C43_PWR2, C54_PWR1, C54_PWR2, C56_PWR1, C56_PWR2	30	0.1uF	C1005X7R1H104K	TDK	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402	0402
3	C6_ADC1, C6_ADC2, C8_ADC1, C8_ADC2, C14_ADC1, C14_ADC2, C15_ADC1, C15_ADC2, C16_ADC1, C16_ADC2, C37	11	1uF	C1608X7R1C105K	TDK	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	0603
4	C11_ADC1, C11_ADC2	2	4700pF	C1608C0G1E472J	TDK	CAP, CERM, 4700 pF, 25 V, +/- 5%, C0G/NP0, 0603	0603
5	C12_ADC1, C12_ADC2, C13_ADC1, C13_ADC2	4	33pF	GRM1555C1E330JA01D	MuRata	CAP, CERM, 33 pF, 25 V, +/- 5%, C0G/NP0, 0402	0402
6	C17_AFE1, C17_AFE2, C19_AFE1, C19_AFE2, C22_AFE1, C22_AFE2, C25_AFE1, C25_AFE2, C28_AFE1, C28_AFE2, C30_AFE1, C30_AFE2	12	8200pF	GRM2195C1H822JA01D	MuRata	CAP, CERM, 8200 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805
7	C18_AFE1, C18_AFE2, C24_AFE1, C24_AFE2, C29_AFE1, C29_AFE2	6	0.1uF	C3216NP01H104J160AA	TDK	CAP, CERM, 0.1 µF, 50 V, +/- 5%, C0G/NP0, 1206_190	1206_190
8	C20_AFE1, C20_AFE2, C23_AFE1, C23_AFE2, C27_AFE1, C27_AFE2	6	0.01uF	08051C103KAT2A	AVX	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0805	0805
9	C21_AFE1, C21_AFE2	2	5600pF	GRM2195C1H562JA01D	MuRata	CAP, CERM, 5600 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805
10	C35, C40_PWR1, C40_PWR2	3	4.7uF	C3216X7R1H475M160AC	TDK	CAP, CERM, 4.7 µF, 50 V, +/- 20%, X7R, 1206_190	1206_190

表 13. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
11	C39, C41_PWR1, C41_PWR2, C53_PWR1, C53_PWR2, C55_PWR1, C55_PWR2	7	2.2uF	UMK316B7225KL-T	Taiyo Yuden	CAP, CERM, 2.2 µF, 50 V, +/- 10%, X7R, 1206	1206
12	C42_PWR1, C42_PWR2	2	270pF	GRM155R71H271KA01D	MuRata	CAP, CERM, 270 pF, 50 V, +/- 10%, X7R, 0402	0402
13	C44_PWR1, C44_PWR2, C46_PWR1, C46_PWR2, C47_PWR1, C47_PWR2, C52_PWR1, C52_PWR2, C58_PWR1, C58_PWR2	10	10uF	C3216X7R1C106M	TDK	CAP, CERM, 10 µF, 16 V, +/- 20%, X7R, 1206	1206
14	C45_PWR1, C45_PWR2, C48_PWR1, C48_PWR2, C49_PWR1, C49_PWR2, C51_PWR1, C51_PWR2, C59_PWR1, C59_PWR2	10	0.01uF	GRM155R71E103KA01D	MuRata	CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0402	0402
15	C50_PWR1, C50_PWR2	2	3300pF	GRM155R71H332KA01D	MuRata	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0402	0402
16	C57_PWR1, C57_PWR2	2	10uF	GRM31CR71E106KA12L	MuRata	CAP, CERM, 10 µF, 25 V, +/- 10%, X7R, 1206	1206
17	C60_PWR1, C60_PWR2	2	1uF	GRM188R71E105KA12D	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603
18	C61_PWR1, C61_PWR2	2	1000pF	202R18W102KV4E	Johanson Technology	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1206_190	1206_190
19	D1_ADC1, D1_ADC2, D3_AFE1, D3_AFE2, D6_AFE1, D6_AFE2, D8_AFE1, D8_AFE2	8	Blue	LB Q39G-L2N2-35-1	OSRAM	LED, Blue, SMD	BLUE 0603 LED
20	D2_ADC1, D2_ADC2	2	Red	150120RS75000	Wurth Elektronik	LED, Red, SMD	3.2x1.6mm
21	D4_AFE1, D4_AFE2, D13_PWR1, D13_PWR2, D16_PWR1, D16_PWR2	6	70V	BAS70JW-7-F	Diodes Inc.	Diode, Schottky, 70 V, 0.07 A, SOT-363	SOT-363
22	D5_AFE1, D5_AFE2, D7_AFE1, D7_AFE2, D9_AFE1, D9_AFE2	6	36V	SM6T36CA	STMicroelectronics	Diode, TVS, Bi, 36 V, 600 W, SMB	SMB
23	D10, D19_PWR1, D19_PWR2, D20	4	35V	CD0603-B0230	Bourns	Diode, Schottky, 35 V, 0.2 A, 0603 Diode	0603 Diode
24	D11, D12_PWR1, D12_PWR2, D14_PWR1, D14_PWR2	5	Green	150120VS75000	Wurth Elektronik	LED, Green, SMD	3.2x1.6mm
25	D15_PWR1, D15_PWR2, D17_PWR1, D17_PWR2	4	3.6V	MMSZ4685-V	Vishay-Semiconductor	Diode, Zener, 3.6 V, 500 mW, SOD-123	SOD-123
26	D18_PWR1, D18_PWR2	2	2.7V	MMSZ4682-V	Vishay-Semiconductor	Diode, Zener, 2.7 V, 500 mW, SOD-123	SOD-123

表 13. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
27	H1, H3	2		1840382	Phoenix Contact	Terminal Block Plug, 3.5mm, 4x1, Green	
28	H2	1		1841161	Phoenix Contact	Fiber optics - MC 1,5/10-LWL 1,5-3,5 for Phoenix connectors	
29	H4	1		1803578	Phoenix Contact	Terminal Block Plug, 3.81mm, 2x1, Green	
30	J1_AFE1, J1_AFE2	2		1844236	Phoenix Contact	Terminal Block, 4x1, 3.5mm, Green, R/A, TH	Terminal Block, 4x1, 3.5mm, R/A, TH
31	J2	1		1803277	Phoenix Contact	Terminal Block, 2x1, 3.81mm, R/A, TH	Connector, 2 pos. 3.8mm RA
32	J3_HART1, J3_HART2, J4_HART1, J4_HART2	4		TFM-106-02-S-D-A	Samtec	Header(Shrouded), 1.27mm, 6x2, Tin, SMT	Header(Shrouded), 1.27mm, 6x2, SMT
33	J8, J9	2		SSHQ-123-D-08-F-LF	Major League Electronics	Female Connector, 2.54mm, 23x2, TH	Female Connector, 2.54mm, 23x2, TH
34	K1_AFE1, K1_AFE2, K2_AFE1, K2_AFE2, K3_AFE1, K3_AFE2	6		CPC1017N	IXYS	Relay, SPST-NO (1 Form A), 0.1 A, 1.2 VDC, SMD	4.089x3.81mm
35	L1	1	10uH	74404042100	Wurth Elektronik	Inductor, Wirewound, Ferrite, 10 µH, 1.2 A, 0.15 ohm, SMD	4x4mm
36	L2_PWR1, L2_PWR2	2	2.2uH	LQM18PN2R2MFH	MuRata	Inductor, Ferrite, 2.2 µH, 0.35 A, 0.38 ohm, SMD	0603
37	Q1, Q3_PWR1, Q3_PWR2, Q4_PWR1, Q4_PWR2, Q5_PWR1, Q5_PWR2	7	60V	2N7002KW	Fairchild Semiconductor	MOSFET, N-CH, 60 V, 0.31 A, SOT-323	SOT-323
38	Q2_PWR1, Q2_PWR2	2	65 V	BC856A-7-F	Diodes Inc.	Transistor, PNP, 65 V, 0.01 A, SOT-23	SOT-23
39	R1_ADC1, R1_ADC2, R37, R38	4	6.65k	CRCW04026K65FKED	Vishay-Dale	RES, 6.65 k, 1%, 0.063 W, 0402	0402
40	R2_ADC1, R2_ADC2, R41	3	261k	CRCW0402261KFKED	Vishay-Dale	RES, 261 k, 1%, 0.063 W, 0402	0402
41	R3_ADC1, R3_ADC2, R5_ADC1, R5_ADC2, R9_ADC1, R9_ADC2, R10_ADC1, R10_ADC2, R11_ADC1, R11_ADC2, R28, R29, R32, R33, R34, R35, R36, R39, R42, R47_PWR1, R47_PWR2, R51_PWR1, R51_PWR2, R53_PWR1, R53_PWR2, R58_PWR1, R58_PWR2, R61_PWR1, R61_PWR2	29	47k	CRCW040247K0JNED	Vishay-Dale	RES, 47 k, 5%, 0.063 W, 0402	0402

表 13. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
42	R4_ADC1, R4_ADC2	2	576k	CRCW0402576KFKED	Vishay-Dale	RES, 576 k, 1%, 0.063 W, 0402	0402
43	R6_ADC1, R6_ADC2	2	340k	CRCW0402340KFKED	Vishay-Dale	RES, 340 k, 1%, 0.063 W, 0402	0402
44	R7_ADC1, R7_ADC2, R12_ADC1, R12_ADC2	4	1.65k	CRCW04021K65FKED	Vishay-Dale	RES, 1.65 k, 1%, 0.063 W, 0402	0402
45	R8_ADC1, R8_ADC2, R45, R50_PWR1, R50_PWR2	5	8.25k	CRCW04028K25FKED	Vishay-Dale	RES, 8.25 k, 1%, 0.063 W, 0402	0402
46	R13_ADC1, R13_ADC2	2	475	CRCW0402475RFKED	Vishay-Dale	RES, 475, 1%, 0.063 W, 0402	0402
47	R14_AFE1, R14_AFE2, R17_AFE1, R17_AFE2, R21_AFE1, R21_AFE2, R22_AFE1, R22_AFE2, R24_AFE1, R24_AFE2, R26_AFE1, R26_AFE2, R27_AFE1, R27_AFE2, R49_PWR1, R49_PWR2	16	5.11k	CRCW04025K11FKED	Vishay-Dale	RES, 5.11 k, 1%, 0.063 W, 0402	0402
48	R15_AFE1, R15_AFE2, R20_AFE1, R20_AFE2, R23_AFE1, R23_AFE2	6	49.9	CRCW040249R9FKED	Vishay-Dale	RES, 49.9, 1%, 0.063 W, 0402	0402
49	R16_AFE1, R16_AFE2	2	4.99k	RNCF0603TKY4K99	Stackpole Electronics Inc	RES, 4.99 k, 0.01%, 0.1 W, 0603	0603
50	R18_AFE1, R18_AFE2	2	82.5k	RN73C2A82K5BTDF	TE Connectivity	RES, 82.5 k, 0.1%, 0.1 W, 0805	0805
51	R19_AFE1, R19_AFE2	2	17.8k	RN73C2A17K8BTDF	TE Connectivity	RES, 17.8 k, 0.1%, 0.1 W, 0805	0805
52	R25_AFE1, R25_AFE2	2	27.4	RN73C2A27R4BTDF	TE Connectivity	RES, 27.4, 0.1%, 0.1 W, 0805	0805
53	R30	1	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
54	R40, R56_PWR1, R56_PWR2, R64_PWR1, R64_PWR2, R69_PWR1, R69_PWR2	7	100k	CRCW0402100KFKED	Vishay-Dale	RES, 100 k, 1%, 0.063 W, 0402	0402
55	R43	1	200k	CRCW0402200KFKED	Vishay-Dale	RES, 200 k, 1%, 0.063 W, 0402	0402
56	R44	1	8.06k	CRCW04028K06FKED	Vishay-Dale	RES, 8.06 k, 1%, 0.063 W, 0402	0402
57	R46_PWR1, R46_PWR2	2	20.5	CRCW120620R5FKEA	Vishay-Dale	RES, 20.5, 1%, 0.25 W, 1206	1206
58	R48_PWR1, R48_PWR2, R52_PWR1, R52_PWR2	4	953k	CRCW0402953KFKED	Vishay-Dale	RES, 953 k, 1%, 0.063 W, 0402	0402

表 13. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
59	R54_PWR1, R54_PWR2	2	931	CRCW0402931RFKED	Vishay-Dale	RES, 931, 1%, 0.063 W, 0402	0402
60	R55_PWR1, R55_PWR2, R60_PWR1, R60_PWR2	4	113k	CRCW0402113KFKED	Vishay-Dale	RES, 113 k, 1%, 0.063 W, 0402	0402
61	R57_PWR1, R57_PWR2, R59_PWR1, R59_PWR2	4	169k	CRCW0402169KFKED	Vishay-Dale	RES, 169 k, 1%, 0.063 W, 0402	0402
62	R62_PWR1, R62_PWR2	2	1.0	CRCW04021R00JNED	Vishay-Dale	RES, 1.0, 5%, 0.063 W, 0402	0402
63	R63_PWR1, R63_PWR2	2	422k	CRCW0402422KFKED	Vishay-Dale	RES, 422 k, 1%, 0.063 W, 0402	0402
64	R65_PWR1, R65_PWR2	2	54.9k	CRCW040254K9FKED	Vishay-Dale	RES, 54.9 k, 1%, 0.063 W, 0402	0402
65	R66_PWR1, R66_PWR2	2	73.2k	CRCW040273K2FKED	Vishay-Dale	RES, 73.2 k, 1%, 0.063 W, 0402	0402
66	R67_PWR1, R67_PWR2	2	8.66k	CRCW04028K66FKED	Vishay-Dale	RES, 8.66 k, 1%, 0.063 W, 0402	0402
67	R68_PWR1, R68_PWR2	2	7.68k	CRCW04027K68FKED	Vishay-Dale	RES, 7.68 k, 1%, 0.063 W, 0402	0402
68	S1	1		416131160802	Wurth Elektronik	Switch, SPST, Off-On, 2 Pos, SMD	5.6x3.58mm
69	T1_PWR1, T1_PWR2	2	120uH	750315856	Wurth Elektronik	Transformer, 120 uH, SMT	12.85x12.95mm
70	U1_ADC1, U1_ADC2	2		ISO7141CCDBQR	Texas Instruments	4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A
71	U2_ADC1, U2_ADC2	2		LM2903PW	Texas Instruments	Dual Comparator, PW0008A	PW0008A
72	U3_ADC1, U3_ADC2	2		LMT01LPG	Texas Instruments	0.5°C Accurate 2-Pin Digital NTC or PTC Thermistor Replacement, LPG0002A	LPG0002A
73	U4_ADC1, U4_ADC2	2		SN74LVC1G125DCKR	Texas Instruments	Single Bus Buffer Gate With 3-State Output, DCK0005A	DCK0005A
74	U5_ADC1, U5_ADC2	2		SN74AHC594PWR	Texas Instruments	8-Bit Shift Register With Output Registers, PW0016A	PW0016A
75	U6_ADC1, U6_ADC2	2		ADS1262IPWR	Texas Instruments	32-Bit, Precision, 38-kSPS, Analog-to-Digital Converter (ADC) with Programmable Gain Amplifier (PGA) and Voltage Reference, PW0028A	PW0028A

表 13. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
76	U7	1		SN74LVC2G86DCTR	Texas Instruments	Dual 2-Input Exclusive-OR Gate, DCT0008A	DCT0008A
77	U8, U9	2		SN74LVC1G332DCKR	Texas Instruments	Single 3-Input Positive-OR Gate, DCK0006A	DCK0006A
78	U10	1		TPS61093DSKR	Texas Instruments	LOW INPUT BOOST CONVERTER WITH INTEGRATED POWER DIODE AND INPUT/OUTPUT ISOLATION, DSK0010A	DSK0010A
79	U11	1		24LC256-I/ST	Microchip	256K I2C CMOS Serial EEPROM, TSSOP-8	TSSOP-8
80	U12_PWR1, U12_PWR2	2		TPS7A4101DGNR	Texas Instruments	Single Output LDO, 50 mA, Adjustable 1.175 to 48 V Output, 7 to 50 V Input, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	DGN0008B
81	U13_PWR1, U13_PWR2	2		TLV70433DBVT	Texas Instruments	Single Output LDO, 150 mA, Fixed 3.3 V Output, 2.5 to 24 V Input, with Ultra-Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	DBV0005A
82	U14_PWR1, U14_PWR2	2		TPS7A4901DRBR	Texas Instruments	+36V, +150mA, Ultralow-Noise, Positive LINEAR REGULATOR, DRB0008A	DRB0008A
83	U15_PWR1, U15_PWR2	2		LM5017SDX/NOPB	Texas Instruments	100V, 600mA Constant On-Time Synchronous Buck Regulator, NGU0008B	NGU0008B
84	U16_PWR1, U16_PWR2	2		TPS7A3001DRBR	Texas Instruments	-35-V, -200-mA, Ultralow-Noise, Negative Linear Regulator, DRB0008A	DRB0008A
85	Y1_ADC1, Y1_ADC2	2		ECS-73-18-10X	ECS Inc.	Crystal, 7.3728MHz, 18pF, SMD	D3.2xL10.5mm
86	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
87	R31	0	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603

5.3 Layout Prints

To download the layout prints, see the design files at TIDA-00550.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00550.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00550.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00550.

6 Software Files

To download the software files, see the design files at TIDA-00550.

7 References

1. IXYS Integrated Circuits Division, *60V Normally-Open Single-Pole 4-Pin SOP OptoMOS® Relay*, CPC1017N Datasheet (PDF)
2. Texas Instruments, LaunchPad Product Folder (http://www.ti.com/tool/msp-exp430fr5969)

7.1 商標

8 About the Authors

LARS LOTZENBURGER is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Lars brings to this role his extensive experience in analog and digital circuit development, PCB design, and embedded programming. Lars earned his diploma in electrical engineering from the University of Applied Science in Mittweida, Saxony, Germany.

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