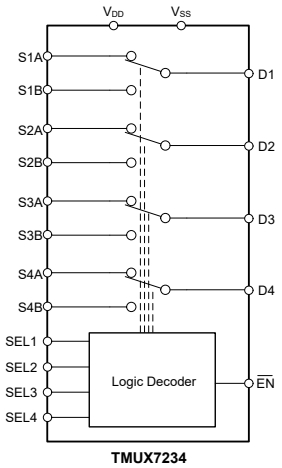
TMUX7234 44V、低 Ron、2:1、4 チャネル高精度スイッチ、ラッチアップ・フリー、1.8V ロジック

1 特長

- ラッチアップ・フリー
- デュアル電源電圧範囲:±4.5V～±22V
- 単一電源電圧範囲:4.5V～44V
- 低いオン抵抗:3Ω
- 少ない電荷注入:3pC
- 大電流に対応:400mA (最大値)
- –40℃～+125℃の動作温度範囲
- 1.8V ロジック互換入力
- フェイルセーフ・ロジック
- レール・ツー・レール動作
- 双方向の信号パス
- ブレイク・ビフォー・メイクのスイッチング動作

2 アプリケーション

- ファクトリ・オートメーション / 制御
- 流量トランスミッタ
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- データ・アクイジション・システム (DAQ)
- 半導体試験用機器
- バッテリ・テスト機器
- 超音波スキャナ
- メディカル・モニタと診断
- 光学ネットワーク機器
- 光学テスト機器
- 有線ネットワーク
- リモート無線ユニット (RRU)
- アクティブ・アンテナ・システム (AAS) の mMIMO



簡略ブロック図

3 概要

TMUX7234 は、ラッチアップ フリーの CMOS マルチプレクサです。TMUX7234 は、 個別に制御できる 4 つの SPDT スイッチを内蔵し、$\overline{EN}$ ピンで 4 つのチャネルをイネーブルまたはディセーブルにします。このデバイスは、単一電源 (4.5V～44 V)、デュアル電源 (±4.5V～±22V)、または非対称電源 (V_{DD} = 12V、V_{SS} = –5V など) をサポートしています。TMUX7234 は、ソース (Sx) およびドレイン (D) ピンで、V_{SS} から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。

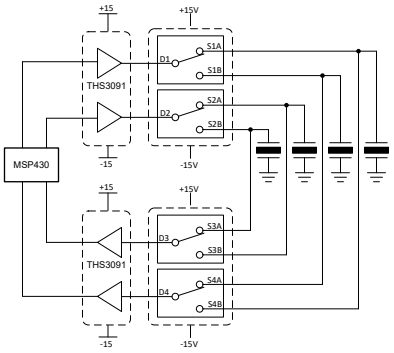
すべてのロジック制御入力は、1.8V～V_{DD} のロジック レベルをサポートしており、有効な電源電圧範囲で動作している場合、TTL ロジックと CMOS ロジックの両方の互換性を確保できます。フェイルセーフ ロジック回路により、電源ピンよりも先に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。

TMUX72xx ファミリはラッチアップ フリーであるため、一般的に過電圧イベントによって発生するデバイス内の寄生構造間の好ましくない大電流イベントを防止できます。ラッチアップ状態は通常、電源レールがオフにされるまで継続するため、デバイスの障害の原因となる場合があります。このラッチアップ フリーという特長により、TMUX72xx スイッチおよびマルチプレクサ ファミリは過酷な環境でも使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TMUX7234	PW (TSSOP、20)	6.5 mm × 6.4 mm
	RRQ (WQFN、20)	4 mm × 4 mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

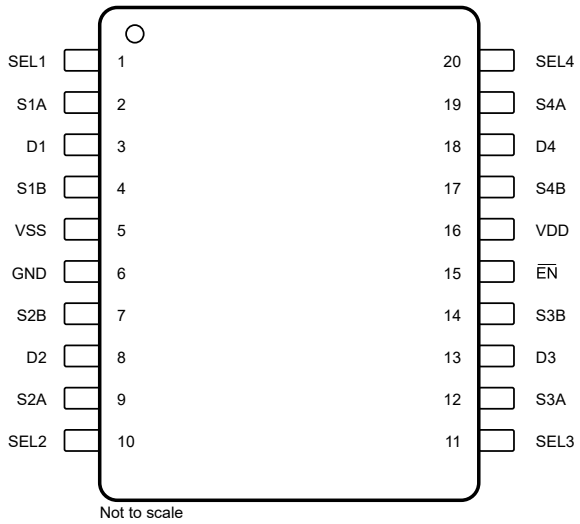

図 4-1. TMUX7234 PW Package, 20-Pin TSSOP (Top View)

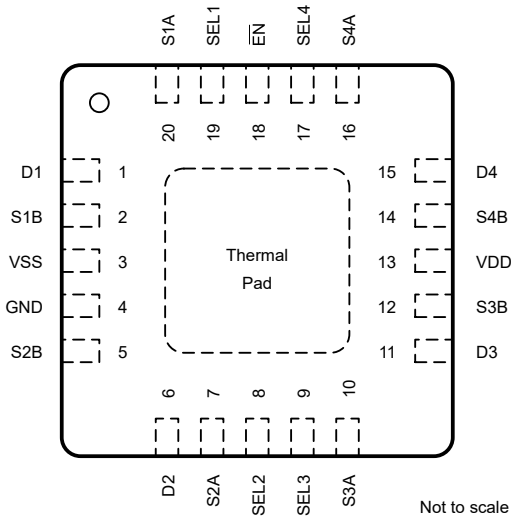

図 4-2. TMUX7234 RRQ Package, 20-Pin WQFN (Top View)

表 4-1. Pin Functions TMUX7234

PIN			TYPE(1)	DESCRIPTION(2)
NAME	PW NO.	RRQ NO.		
SEL1	1	19	I	Logic control input 1; has internal pull-down resistor. Controls switch 1 (see セクション 7.5).
S1A	2	20	I/O	Source pin 1A. Can be an input or output.
D1	3	1	I/O	Drain pin 1. Can be an input or output.
S1B	4	2	I/O	Source pin 1B. Can be an input or output.
VSS	5	3	P	Negative power supply. This pin has the most negative power-supply potential. This pin can be connected to ground in single supply applications. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND for reliable operation.
GND	6	4	P	Ground (0 V) reference.
S2B	7	5	I/O	Source pin 2B. Can be an input or output.
D2	8	6	I/O	Drain pin 2. Can be an input or output.
S2A	9	7	I/O	Source pin 2A. Can be an input or output.
SEL2	10	8	I	Logic control input 2; has internal pull-down resistor. Controls switch 2 (see セクション 7.5).
SEL3	11	9	I	Logic control input 3; has internal pull-down resistor. Controls switch 3 (see セクション 7.5).
S3A	12	10	I/O	Source pin 3A. Can be an input or output.
D3	13	11	I/O	Drain pin 3. Can be an input or output.
S3B	14	12	I/O	Source pin 3B. Can be an input or output.
$\overline{EN}$	15	18	I	Active low logic enable; has internal pull-down resistor. The SELx logic inputs determine switch connections when this pin is low (see セクション 7.5).
VDD	16	13	P	Positive power supply. This pin has the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
S4B	17	14	I/O	Source pin 4B. Can be an input or output.
D4	18	15	I/O	Drain pin 4. Can be input or output
S4A	19	16	I/O	Source pin 4A. Can be an input or output.
SEL4	20	17	I	Logic control input 4, has internal pull-down resistor. Controls switch 4 (see セクション 7.5).
Thermal Pad			—	The thermal pad is not connected internally. There is no requirement to solder this pad. If connected, it is recommended to leave the pad floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to セクション 7.4 for what to do with unused pins.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}–V_{SS}	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx, $\overline{EN}$)	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx, $\overline{EN}$)	–30	30	mA
V_S or V_D	Source or drain voltage (SxA, SxB, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)		I_{DC} ± 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN package)(5)		1680	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.8mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		TMUX7234		UNIT
		PW (TSSOP)	RRQ (WQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	40.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.9	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.3	16.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.7	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (SxA, SxB, Dx)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)			I_{DC} (2)	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	+44 V Single Supply(1)	350	230	129	mA
	±15 V Dual Supply	360	235	130	mA
	+12 V Single Supply	260	177	108	mA
	±5 V Dual Supply	255	175	105	mA
	+5 V Single Supply	170	129	80	mA
RRQ (WQFN)	+44 V Single Supply(1)	400	230	120	mA
	±15 V Dual Supply	400	230	120	mA
	+12 V Single Supply	300	180	100	mA
	±5 V Dual Supply	300	180	100	mA
	+5 V Single Supply	240	150	85	mA

(1) Specified for nominal supply voltage only.

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5.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		3.6	5.5	Ω
			–40°C to +85°C			7.1	Ω
			–40°C to +125°C			8.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–40°C to +125°C			1.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to セクション 6.2	25°C	–0.4	0.01	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to セクション 6.2	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–12		12	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to セクション 6.3	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–8		8	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		45	70	µA
			–40°C to +85°C			80	µA
			–40°C to +125°C			95	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		8	25	µA
			–40°C to +85°C			30	µA
			–40°C to +125°C			40	µA

(1) When V_S is positive, V_D is negative. Or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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5.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		90	180	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			200	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		110	180	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			210	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		80	140	ns
			–40°C to +85°C			150	ns
			–40°C to +125°C			160	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to セクション 6.8	25°C		450		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 100 pF Refer to セクション 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		100		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to セクション 6.14	25°C		–48		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to セクション 6.13	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		16		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		28		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		77		pF

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5.8 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		3.2	5.4	Ω
			–40°C to +85°C			6.7	Ω
			–40°C to +125°C			7.9	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10 mA Refer to On-Resistance	25°C		0.6	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–40°C to +125°C			1.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.014		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to セクション 6.2	25°C	–1	0.02	1	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–12		12	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to セクション 6.2	25°C	–1	0.04	1	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V Refer to セクション 6.3	25°C	–1	0.04	1	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–30		30	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		50	80	µA
			–40°C to +85°C			95	µA
			–40°C to +125°C			110	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		10	30	µA
			–40°C to +85°C			35	µA
			–40°C to +125°C			45	µA

(1) When V_S is positive, V_D is negative. Or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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5.9 ±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		90	190	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			210	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		110	190	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			210	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		75	140	ns
			–40°C to +85°C			150	ns
			–40°C to +125°C			160	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to セクション 6.8	25°C		470		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 100 pF Refer to セクション 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		95		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.25		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to セクション 6.14	25°C		–48		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to セクション 6.13	25°C		0.002		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		16		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		26		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		77		pF

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5.10 44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		3	5.8	Ω
			–40°C to +85°C			7.2	Ω
			–40°C to +125°C			8.9	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		1.5	2	Ω
			–40°C to +85°C			2.5	Ω
			–40°C to +125°C			3.3	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.012		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to セクション 6.2	25°C	–1	0.02	1	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–20		20	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to セクション 6.2	25°C	–1	0.04	1	nA
			–40°C to +85°C	–8		8	nA
			–40°C to +125°C	–40		40	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V Refer to セクション 6.3	25°C	–1	0.04	1	nA
			–40°C to +85°C	–8		8	nA
			–40°C to +125°C	–40		40	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		70	110	µA
			–40°C to +85°C			118	µA
			–40°C to +125°C			140	µA

(1) When V_S is 40 V, V_D is 1 V. Or when V_S is 1 V, V_D is 40 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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5.11 44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		90	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		100	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		90	180	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			220	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		45		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.13		ms
			–40°C to +85°C		0.13		ms
			–40°C to +125°C		0.13		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to セクション 6.8	25°C		570		ps
Q_{INJ}	Charge injection	V_D = 22 V, C_L = 100 pF Refer to セクション 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		92		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to セクション 6.14	25°C		–45		dB
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1 MHz	25°C		16		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1 MHz	25°C		28		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1 MHz	25°C		77		pF

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5.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		6.2	12	Ω
			–40°C to +85°C			15	Ω
			–40°C to +125°C			18	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		2.4	3.6	Ω
			–40°C to +85°C			3.9	Ω
			–40°C to +125°C			4.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.025		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to セクション 6.2	25°C	–0.4	0.01	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to セクション 6.2	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–12		12	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to セクション 6.3	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–8		8	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		36	55	µA
			–40°C to +85°C			65	µA
			–40°C to +125°C			75	µA

(1) When V_S is 10 V, V_D is 1 V. Or when V_S is 1 V, V_D is 10 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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5.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		105	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			250	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		110	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			250	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to セクション 6.5	25°C		105	190	ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			240	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		60		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to セクション 6.8	25°C		490		ps
Q_{INJ}	Charge injection	V_D = 6 V, C_L = 100 pF Refer to セクション 6.9	25°C		1		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		130		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.5		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to セクション 6.14	25°C		–50		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to セクション 6.13	25°C		0.0016		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		19		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		33		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		78		pF

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5.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

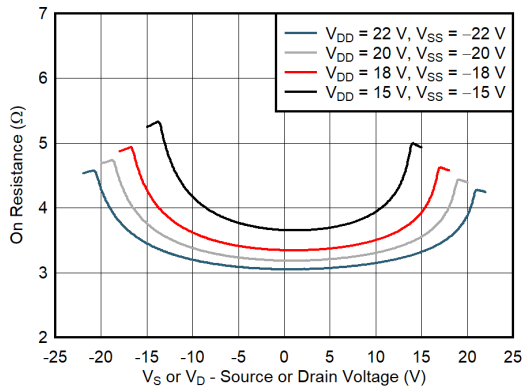


図 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

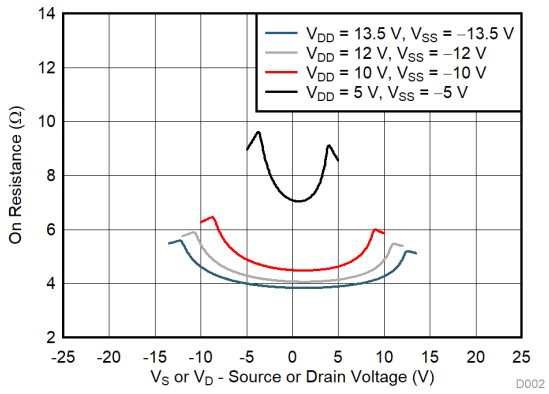


図 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply

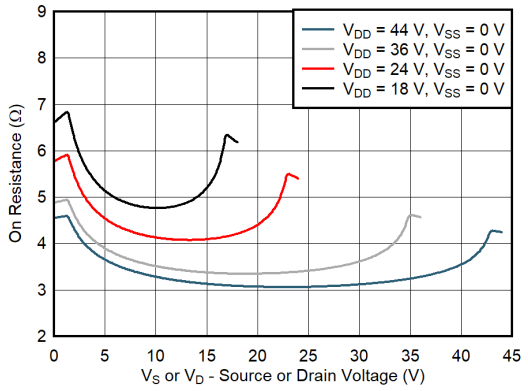


図 5-3. On-Resistance vs Source or Drain Voltage – Single Supply

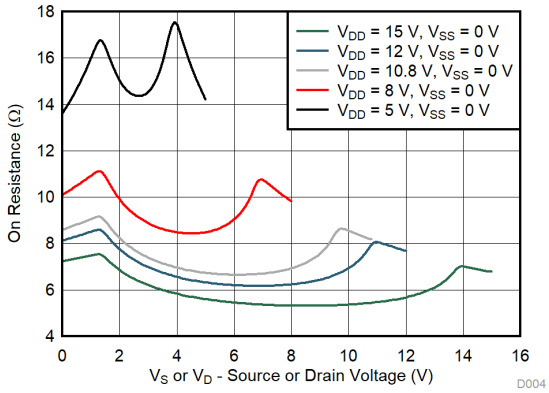
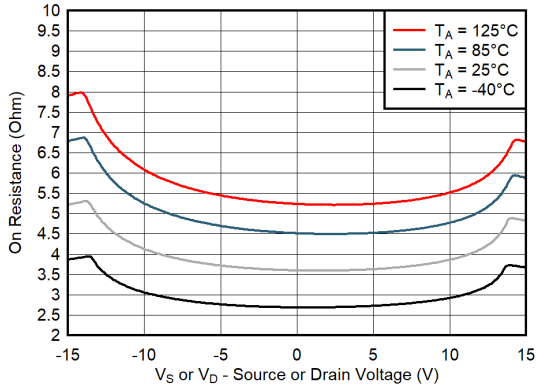
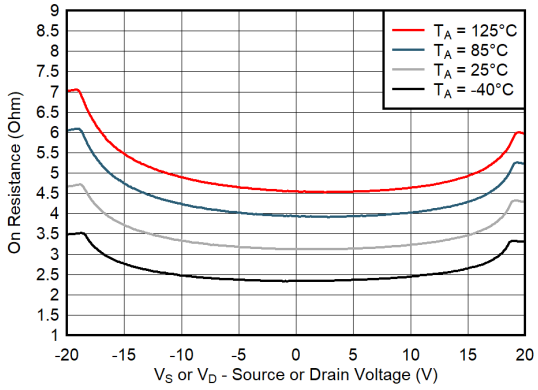


図 5-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

図 5-5. On-Resistance vs Temperature



V_{DD} = 20 V, V_{SS} = -20 V

図 5-6. On-Resistance vs Temperature

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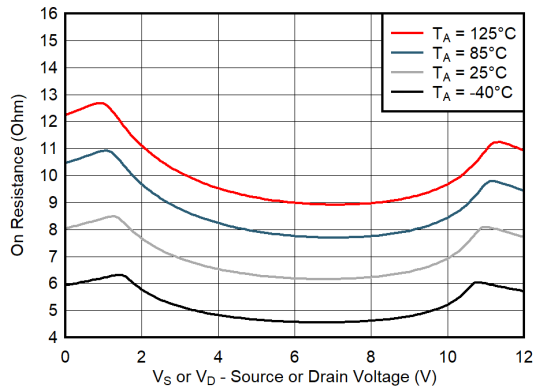
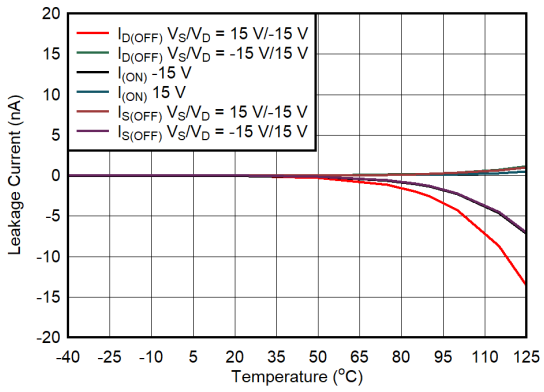
5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



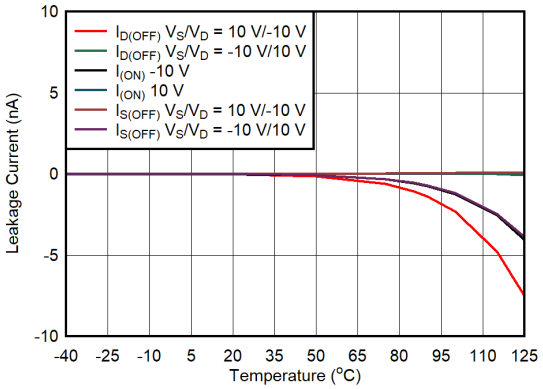
V_{DD} = 12 V, V_{SS} = 0 V

図 5-7. On-Resistance vs Temperature



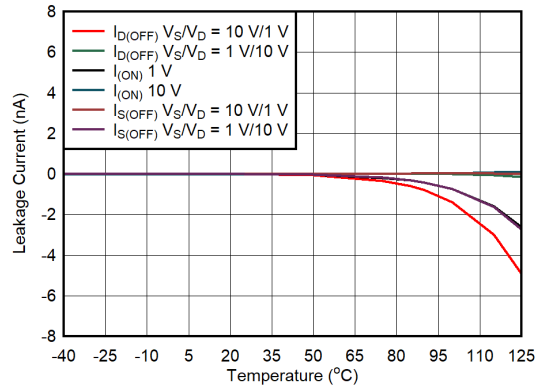
V_{DD} = 20 V, V_{SS} = -20 V

図 5-8. Leakage Current vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V

図 5-9. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

図 5-10. Leakage Current vs Temperature

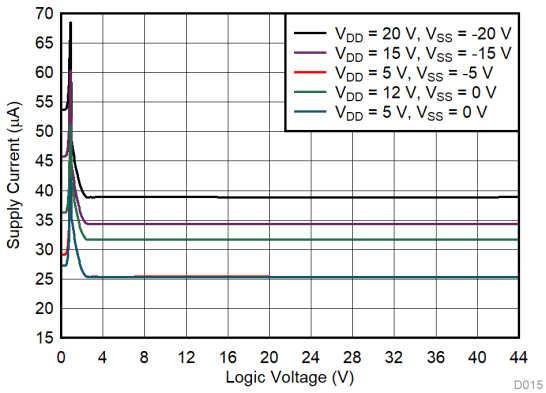


図 5-11. Supply Current vs Logic Voltage

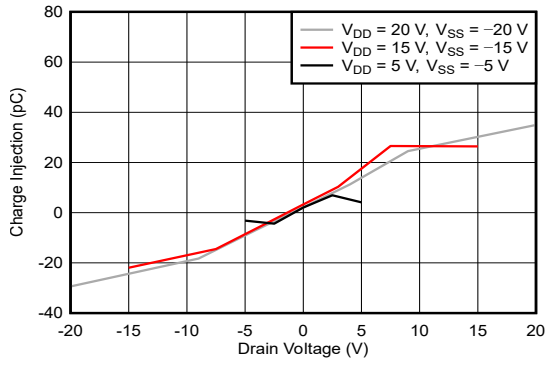


図 5-12. Charge Injection vs Drain Voltage – Dual Supply

5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

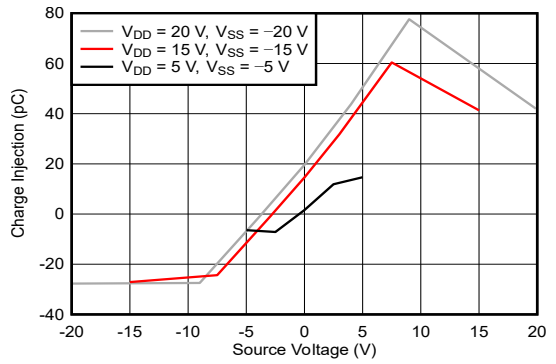


図 5-13. Charge Injection vs Source Voltage – Dual Supply

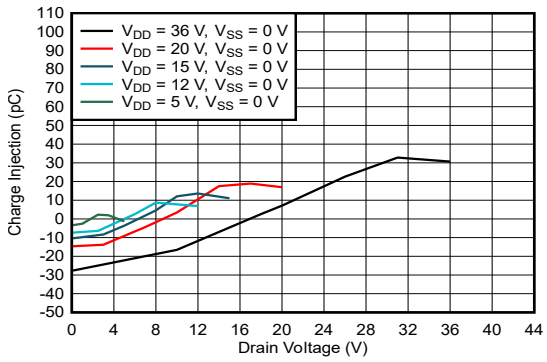


図 5-14. Charge Injection vs Drain Voltage – Single Supply

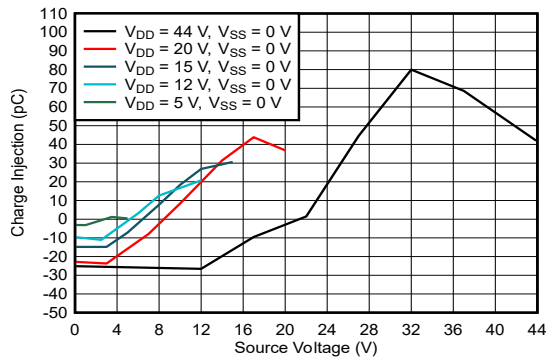


図 5-15. Charge Injection vs Source Voltage – Single Supply

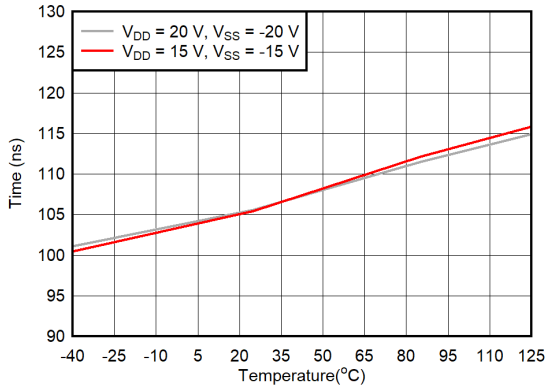


図 5-16. $T_{TRANSITION}$ vs Temperature

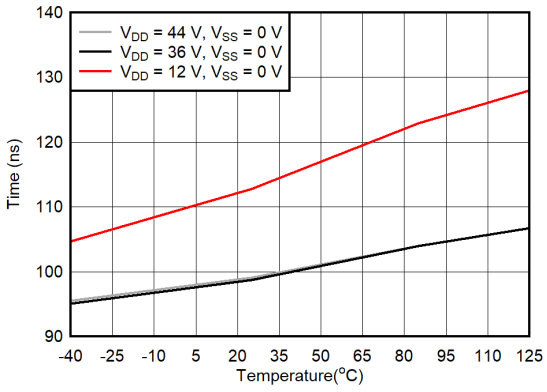
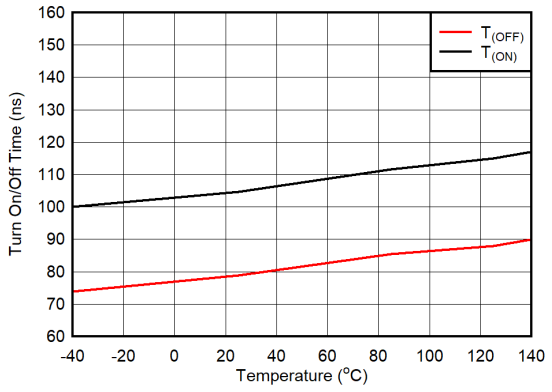


図 5-17. $T_{TRANSITION}$ vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V

図 5-18. T_{ON} and T_{OFF} vs Temperature

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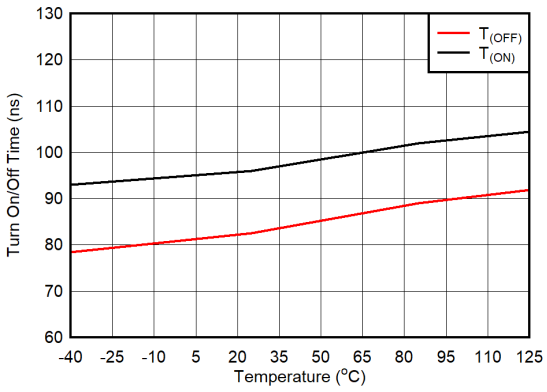
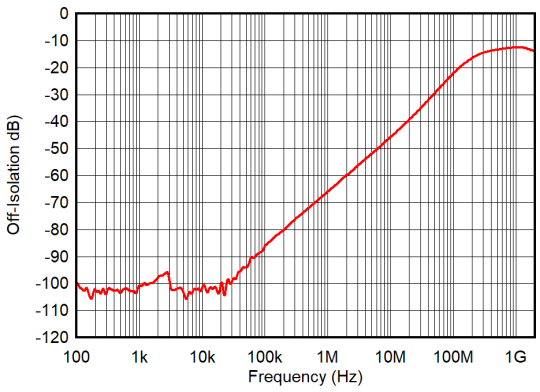
5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



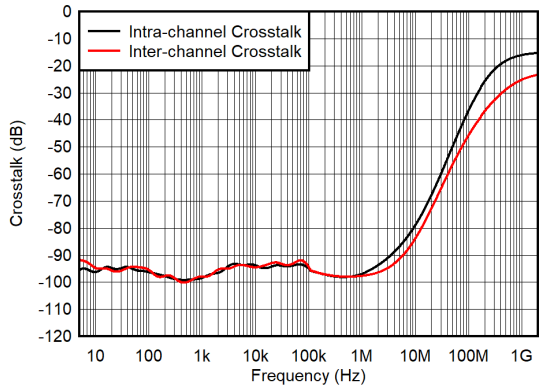
V_{DD} = 44 V, V_{SS} = 0 V

図 5-19. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V, T_A = 25°C

図 5-20. Off-Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = -15 V

図 5-21. Crosstalk vs Frequency

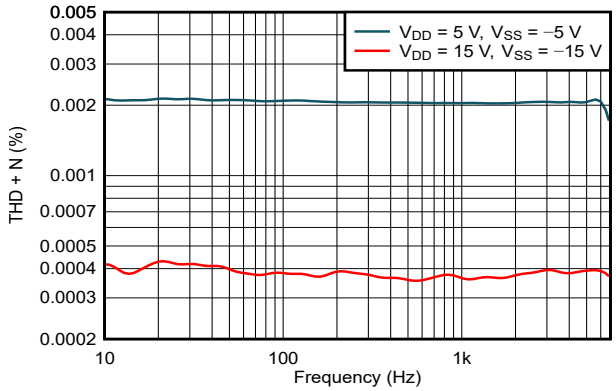


図 5-22. THD+N vs Frequency (Dual Supply)

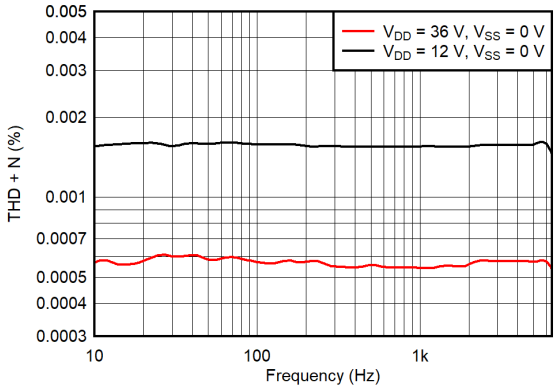
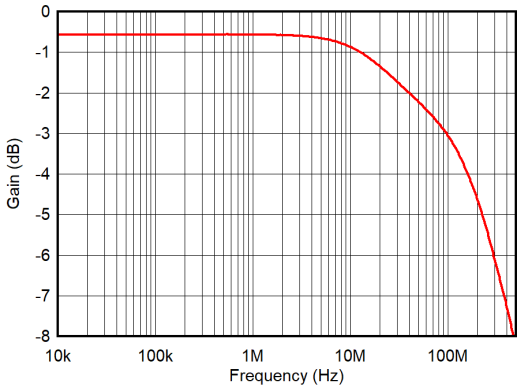


図 5-23. THD+N vs Frequency (Single Supply)

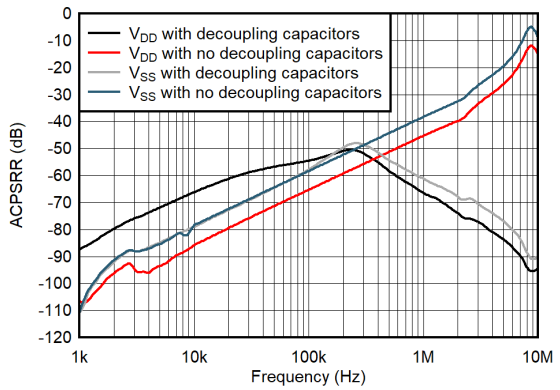


V_{DD} = 15 V, V_{SS} = -15 V

図 5-24. On Response vs Frequency

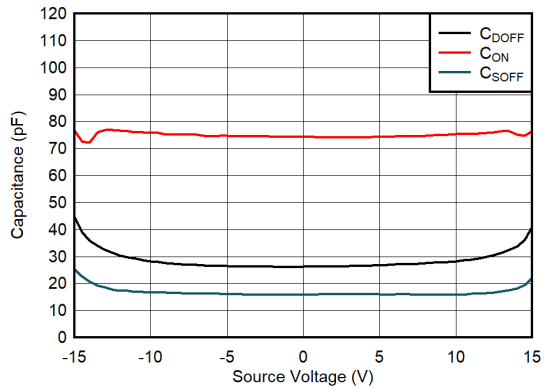
5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



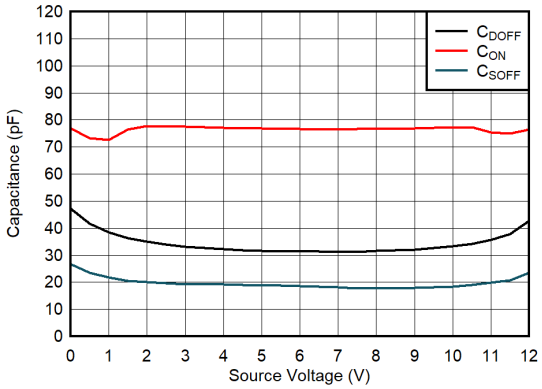
V_{DD} = +15 V, V_{SS} = -15 V

図 5-25. ACPSRR vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

図 5-26. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

図 5-27. Capacitance vs Source Voltage or Drain Voltage

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6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. 図 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

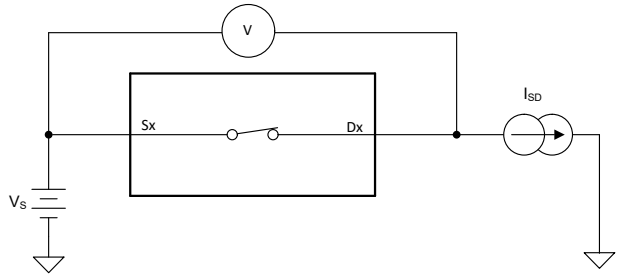

図 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

図 6-2 shows the setup used to measure both off-leakage currents.

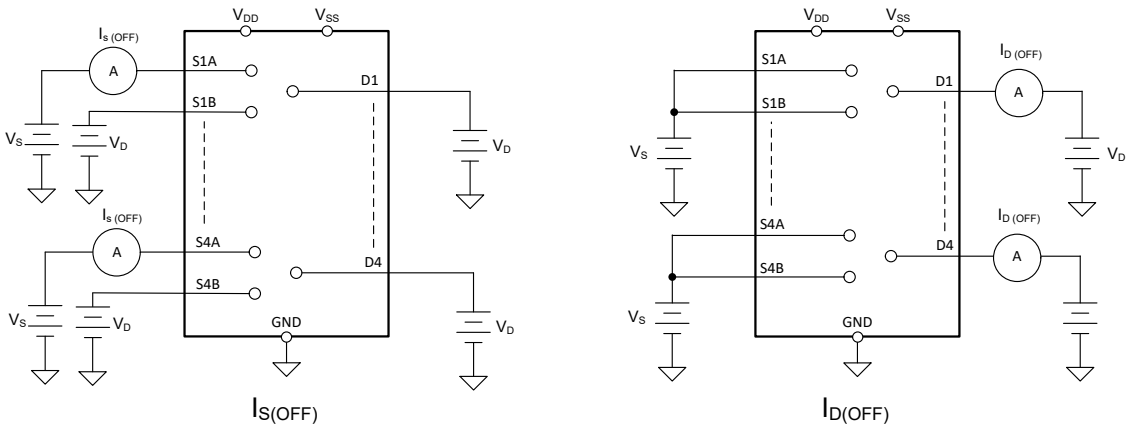

図 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 図 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

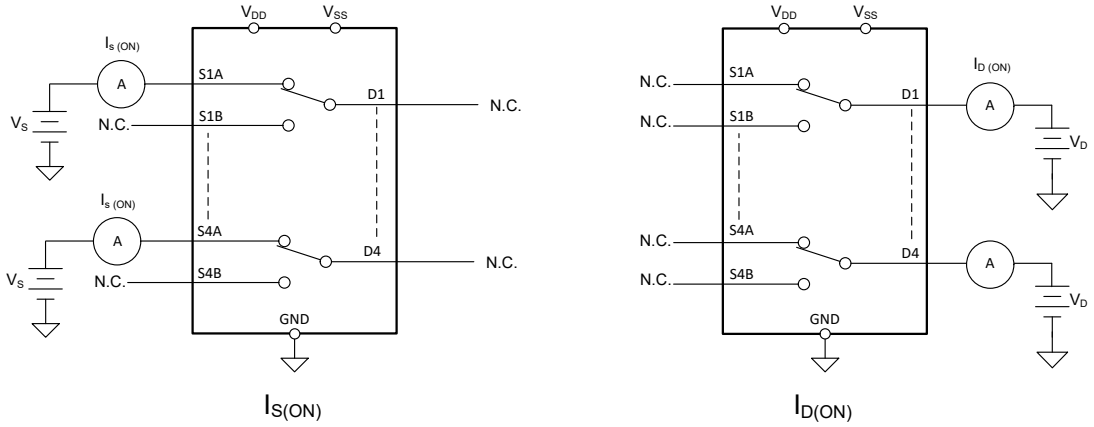

図 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

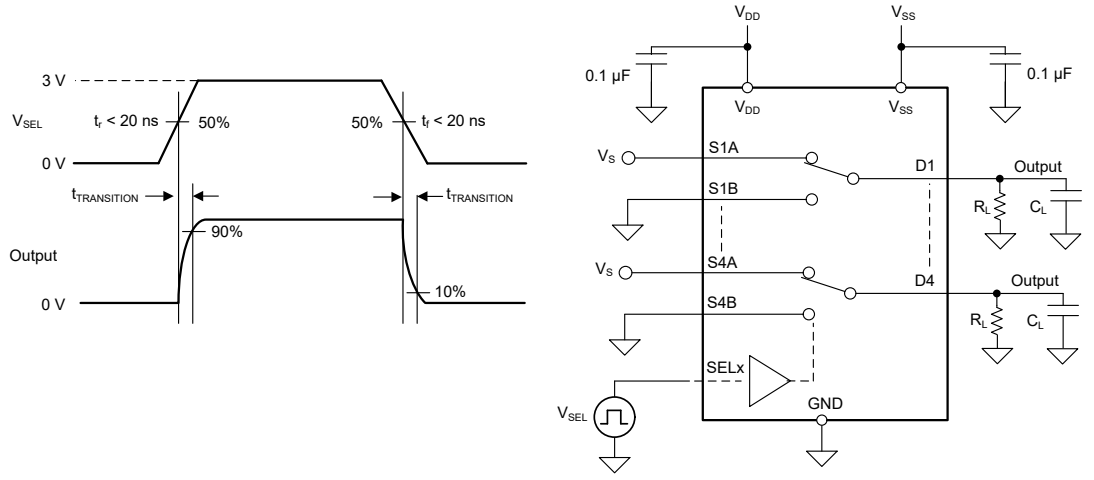

図 6-4. Transition-Time Measurement Setup

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6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 6-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 6-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

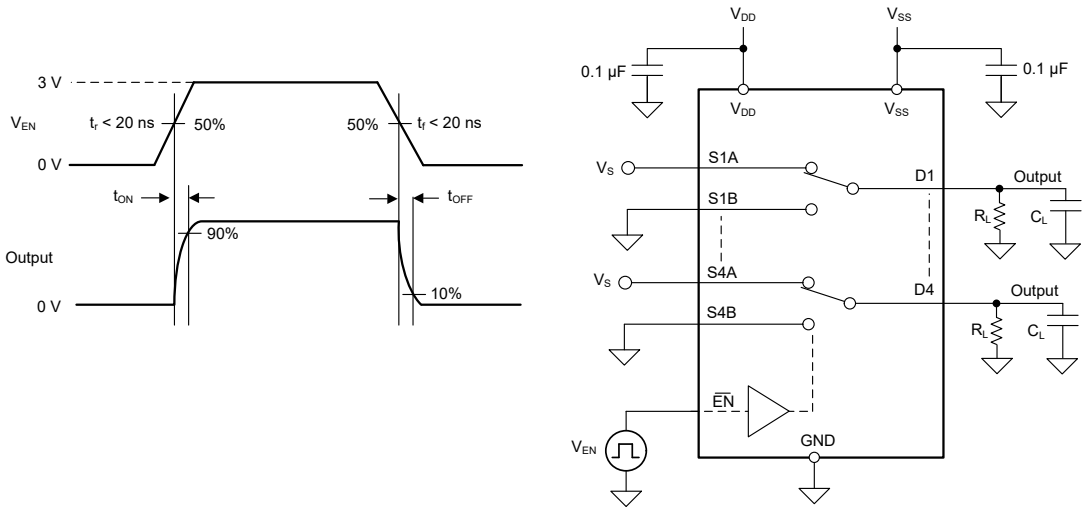

図 6-5. Turn-On and Turn-Off Time Measurement Setup

6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

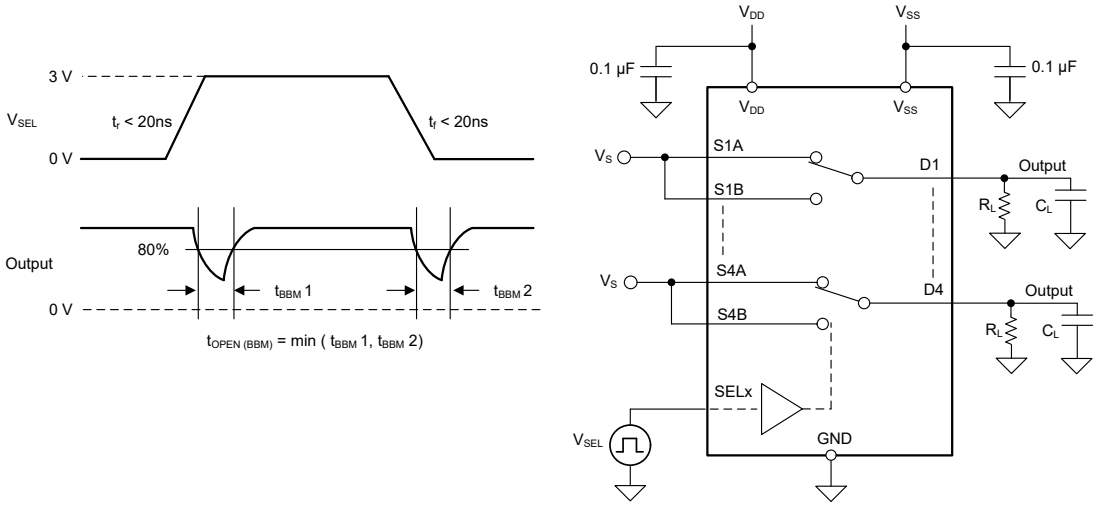

図 6-6. Break-Before-Make Delay Measurement Setup

6.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 図 6-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

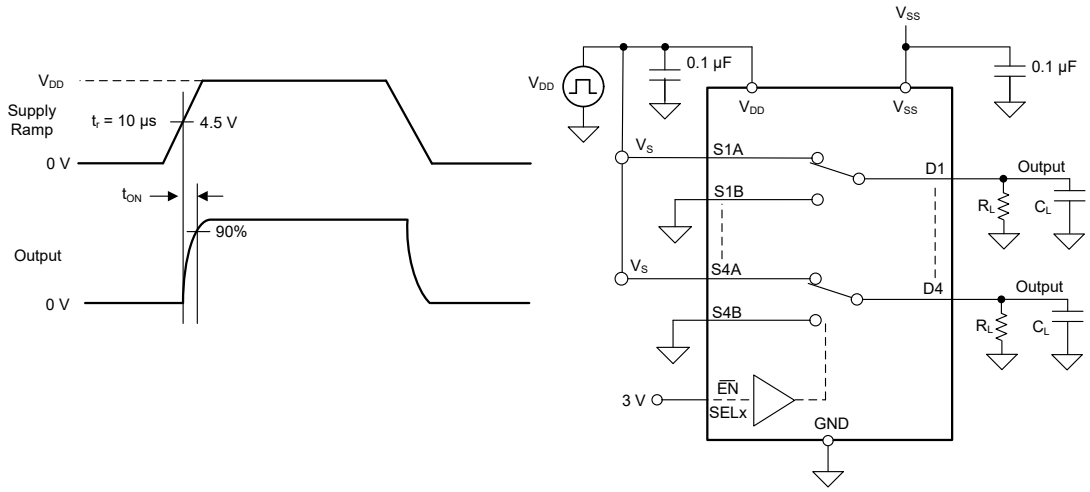

図 6-7. $t_{ON\ (VDD)}$ Time Measurement Setup

6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 図 6-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

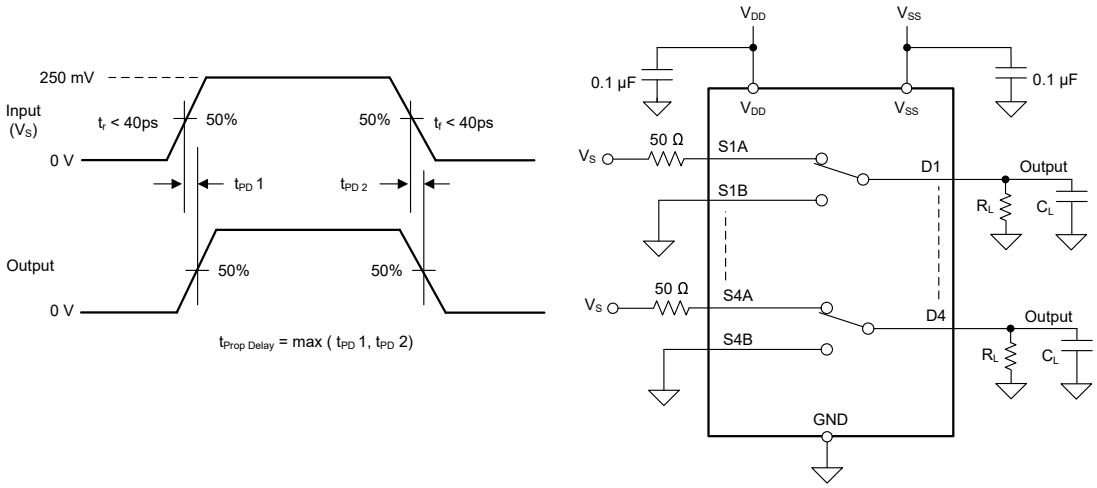

図 6-8. Propagation Delay Measurement Setup

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6.9 Charge Injection

The TMUX7234 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 6-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

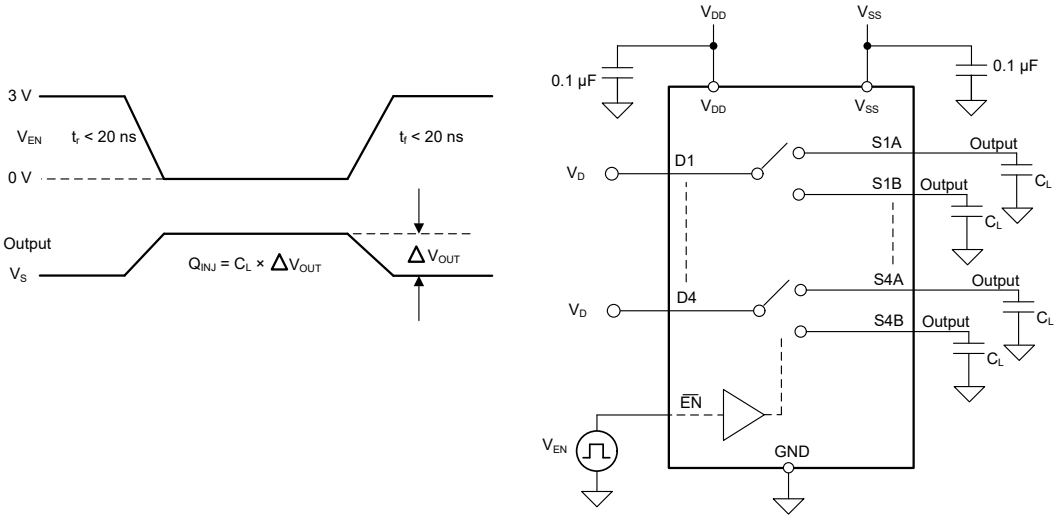

図 6-9. Charge-Injection Measurement Setup

6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 6-10 shows the setup used to measure, and the equation used to calculate off isolation.

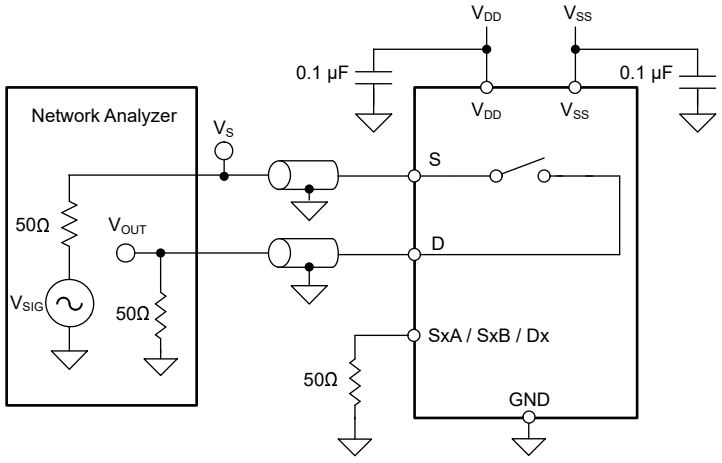

図 6-10. Off Isolation Measurement Setup

6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 図 6-11 shows the setup used to measure and the equation used to calculate crosstalk.

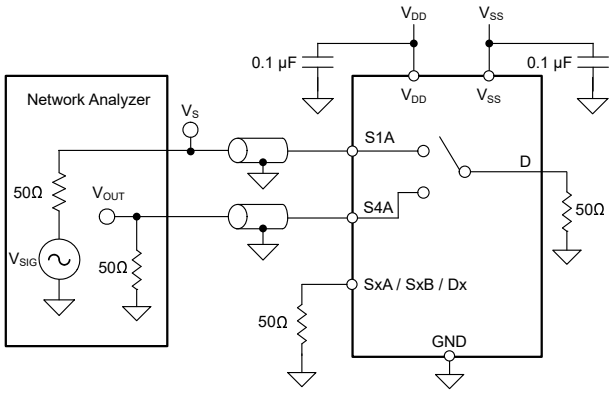

図 6-11. Crosstalk Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 図 6-12 shows the setup used to measure bandwidth.

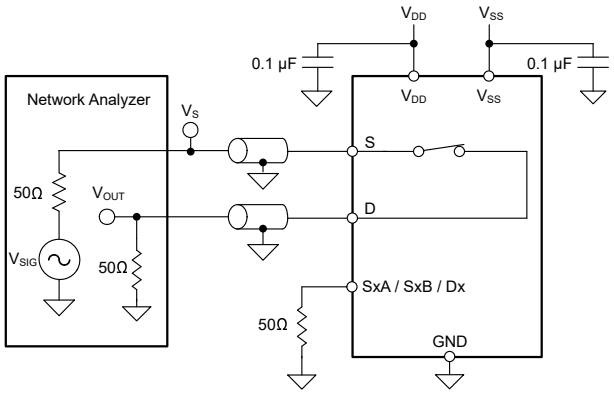

図 6-12. Bandwidth Measurement Setup

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6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

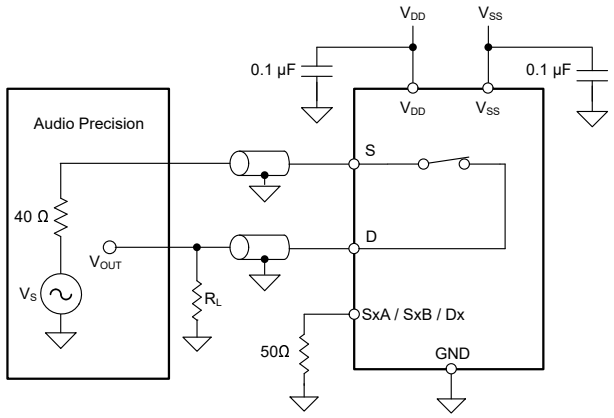


図 6-13. THD Measurement Setup

6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

The below shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.

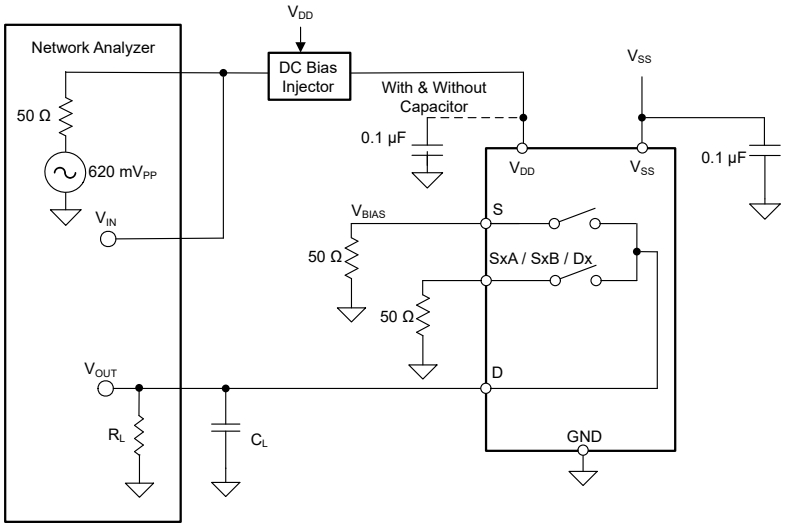


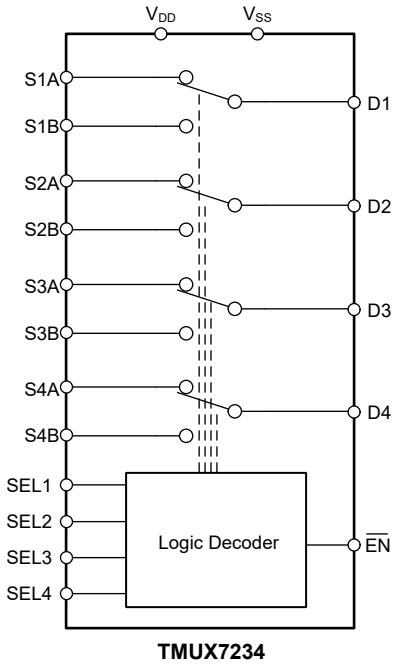
図 6-14. ACPSRR Measurement Setup

7 Detailed Description

7.1 Overview

The TMUX7234 contains four independently controlled SPDT switches with an $\overline{EN}$ pin to enable or disable all four switches.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX7234 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for the TMUX7234 ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX7234 has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the switch to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches* .

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7.3.4 Fail-Safe Logic

TMUX7234 supports Fail-Safe Logic on the control input pins ($\overline{EN}$ and SELx) allowing it to operate up to 44 V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the TMUX7234 logic input pins to ramp up to +44 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.5 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX72xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability* .

7.3.6 Ultra-Low Charge Injection

The TMUX7234 has a transmission gate topology, as shown in 図 7-1. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

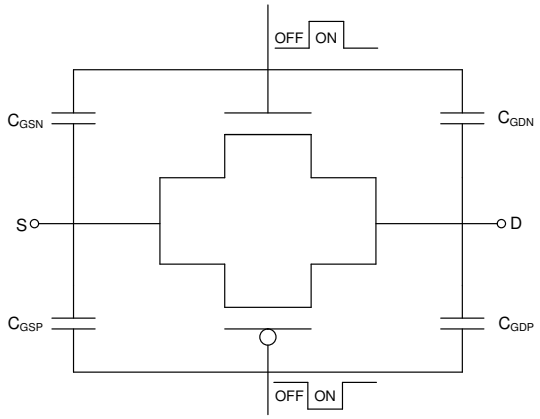

図 7-1. Transmission Gate Topology

The TMUX7234 contains specialized architecture to reduce charge injection on the source (Sx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the drain (D). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the drain (D) instead of the source (Sx). As a general rule of thumb, Cp should be 20x larger than the equivalent load capacitance on the source (Sx). 図 7-2 shows charge injection variation with different compensation capacitors on the drain side. This plot was captured on the TMUX7219 as part of the TMUX72xx family with a 100pF load capacitance.

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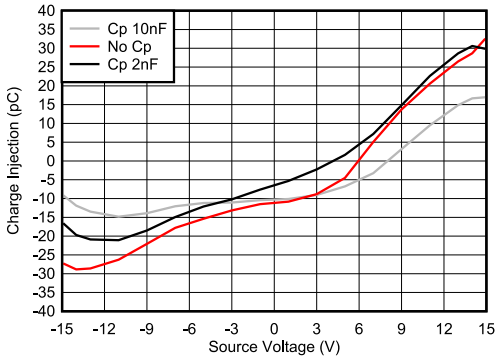

図 7-2. Charge Injection Compensation

7.4 Device Functional Modes

The enable $\overline{EN}$ pin is an active-low logic pin that controls the connection between the source (SxA and SxB) and drain (Dx) pins of the device. The TMUX7234 SELx logic control inputs determine which source pin is connected to the drain pin for each channel. When the $\overline{EN}$ pin of the TMUX7234 is pulled low, the SELx logic control inputs determine which source input is selected. When the $\overline{EN}$ pin is pulled high, all of the switches are in an open state regardless of the state of the SELx logic control inputs. The control pins can be as high as 44 V.

The TMUX7234 can be operated without any external components except for the supply decoupling capacitors. The $\overline{EN}$ and SELx pins have internal pull-down resistors of 4 MΩ. If unused, $\overline{EN}$ and SELx pins should be tied to GND in order to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx or Dx) should be connected to GND.

7.5 Truth Tables

表 7-1 shows the truth tables for the TMUX7234.

表 7-1. TMUX7234 Truth Table

$\overline{EN}$	SEL1	SEL2	SEL3	SEL4	Selected Source Pins Connected to Drain Pins
0	0	X(1)	X	X	S1B to D1
0	1	X	X	X	S1A to D1
0	X	0	X	X	S2B to D2
0	X	1	X	X	S2A to D2
0	X	X	0	X	S3B to D3
0	X	X	1	X	S3A to D3
0	X	X	X	0	S4B to D4
0	X	X	X	1	S4A to D4
1	X	X	X	X	Hi-Z (OFF)

(1) *X* means *do not care*.

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8 Application and Implementation

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8.1 Application Information

The TMUX7234 is part of the precision switches and multiplexers family of devices. This device operates with dual supplies (±4.5 V to ±22 V), a single supply (4.5 V and 44 V), or asymmetric supplies (such as, V_{DD} = 12 V and V_{SS} = −5 V), and offers rail-to-rail input and output. The TMUX7234 offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX7234 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

One key application of the TMUX7234 is in the ultrasonic water flow measurement system. Ultrasonic flow meters use time of flight (ToF) of an ultrasonic wave and its dependency and behavior in the medium using two transducer pairs for upstream and downstream paths. The signal waveforms are transmitted between two adjacent transducers. One transducer transmits an upstream path signal and the other transducer receives a downstream signal path. The flight time for the signal can be calculated using the known velocity of sound and length between the transducers. The upstream and downstream waveforms are processed on the main MCU to obtain the volume. 図 8-1 shows a circuit example utilizing the MSP430FR66047 MCU, high voltage low distortion operational amplifiers (THS3091), along with TMUX7234, 2:1, 4 channel precision switches. The TMUX7234 is used to select the Rx and Tx path of the transducer. The TMUX7234 offers low on-state resistance, flat capacitance performance, and low propagation delay which leads to very low signal distortion. The break-before-make feature allows transferring of a signal from one port to another, without shorting the inputs together. This device also offers low charge injection which makes this device suitable for high precision data acquisition systems.

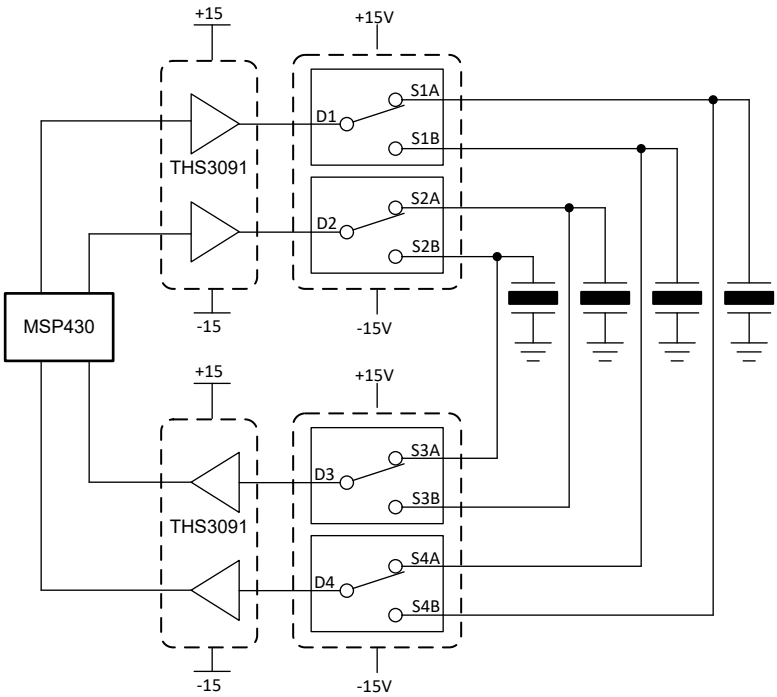

図 8-1. Ultrasonic Water Flow Measurement System

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15 V
Supply (V_{SS})	-15 V
MUX I/O signal range	-15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatiable (up to V_{DD})
$\overline{EN}$	$\overline{EN}$ pulled low to enable the switch

8.2.2 Detailed Design Procedure

The TMUX7234 can operate without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommended operating conditions of the TMUX7234, including signal range and continuous current. セクション 5.4 shows how the signal range for this design can be -15 V to +15 V and the maximum continuous current can be up to 400 mA for wide-range current measurement with a positive supply of 15 V on V_{DD} and negative supply of -15 V on V_{SS}. The TMUX7234 device are bidirectional, single-pole double-throw (SPDT) switches that offer low on-resistance, low leakage, and low power. These features make these devices suitable for portable and power sensitive applications such as ultrasonic water metering systems. For a more detailed analysis of the ultrasonic water flow measurement system refer to the reference design.

8.2.3 Application Curve

The low on and off leakage currents of TMUX7234 and ultra-low charge injection performance make this device ideal for implementing high precision industrial systems. The TMUX7234 contains specialized architecture to reduce charge injection on the Source side (Sx) (For more details, see セクション 7.3.6). 図 8-2 shows the plot for the charge injection versus drain voltage for the TMUX7234.

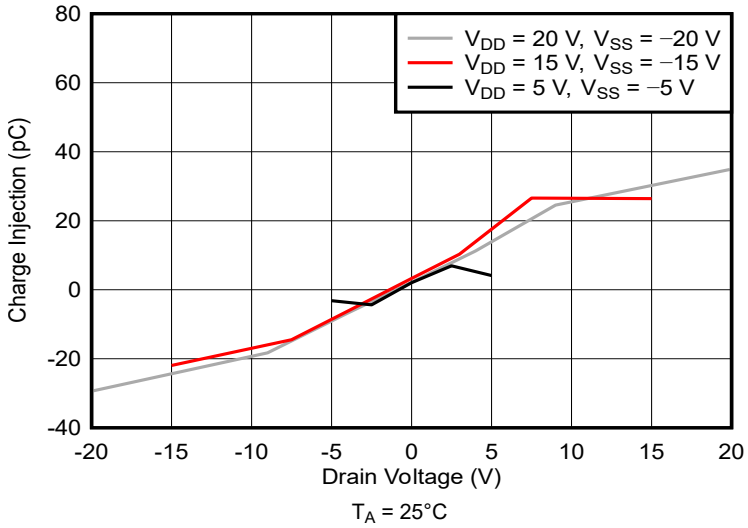

図 8-2. Charge Injection vs Drain Voltage

9 Power Supply Recommendations

TMUX7234 operates across a wide supply range of ±4.5 V to ±22 V (4.5 V to 44 V in single-supply mode). TMUX7234 also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

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Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. Use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground for an improved supply noise immunity. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

10 Layout

10.1 Layout Guidelines

A reflection can occur when a PCB trace turns a corner at a 90° angle. A reflection occurs primarily because of the change of width of the trace. The trace width increases to 1.414 times the width at the apex of the turn. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

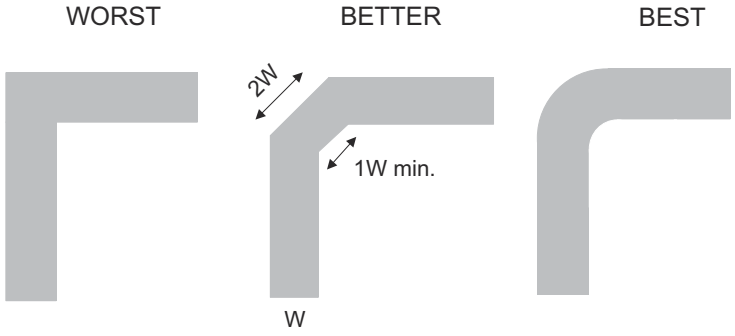

図 10-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

図 10-2 and 図 10-3 illustrate an example of a PCB layout with the TMUX7234. Some key considerations are:

- Decouple the supply pins with a 0.1 µF and 1 µF capacitor, placed lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

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10.2 Layout Example

図 10-2 shows an example board layout for the TMUX7234.

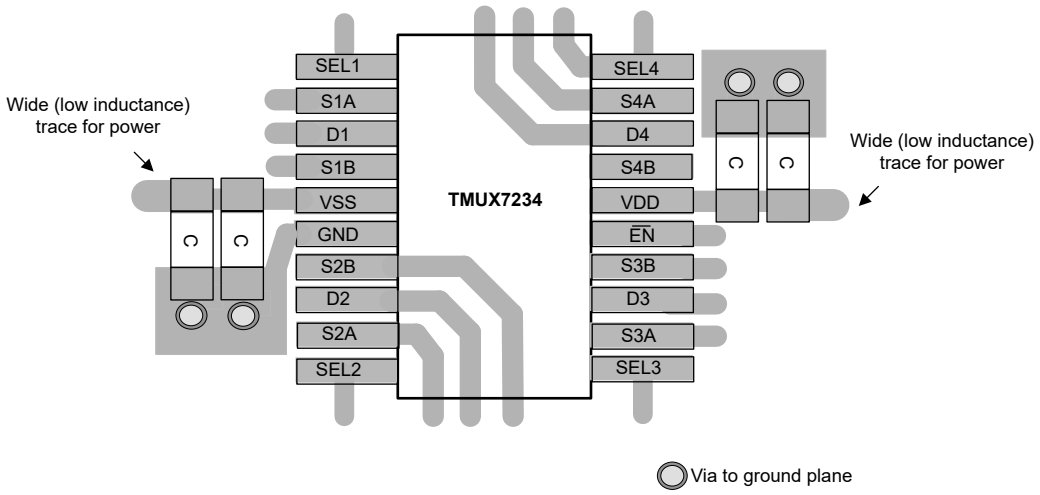

図 10-2. TMUX7234PW Layout Example

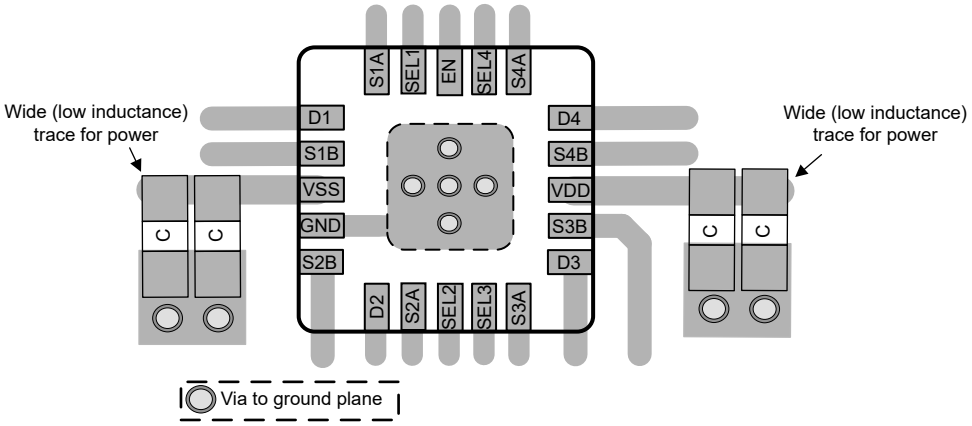

図 10-3. TMUX7234RRQ Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application report
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application report
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

11.2 Receiving Notification of Documentation Updates

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12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (November 2022) to Revision G (July 2024)	Page
• Updated ESD HBM value	4
• Updated IIH max specification	6

Changes from Revision E (August 2021) to Revision F (November 2022)	Page
• PW パッケージのステータスをプレビューからアクティブに変更	1

Changes from Revision D (August 2021) to Revision E (August 2021)	Page
• Updated ESD HBM spec	4

Changes from Revision C (June 2021) to Revision D (August 2021)	Page
• *ステータスを事前情報から量産データに変更*	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7234PWR	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T234
TMUX7234PWR.B	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T234
TMUX7234RRQR	Active	Production	WQFN (RRQ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX X234
TMUX7234RRQR.B	Active	Production	WQFN (RRQ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX X234

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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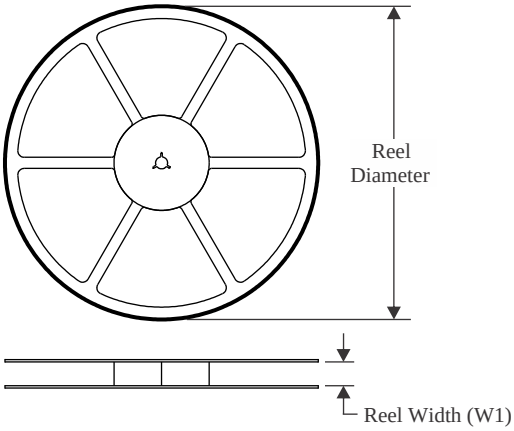
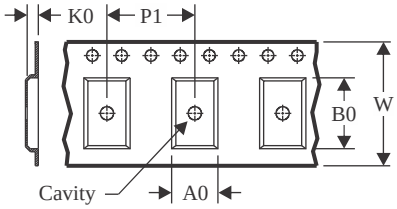
TAPE AND REEL INFORMATION

REEL DIMENSIONS

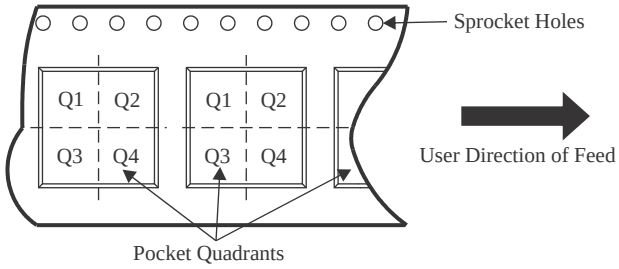


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

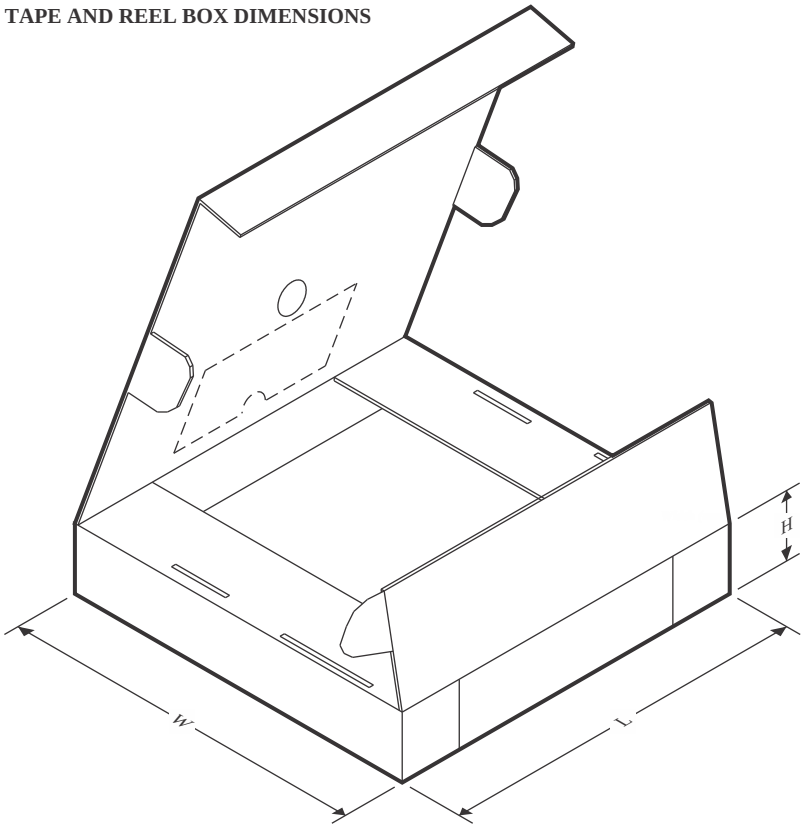
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7234PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TMUX7234RRQR	WQFN	RRQ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

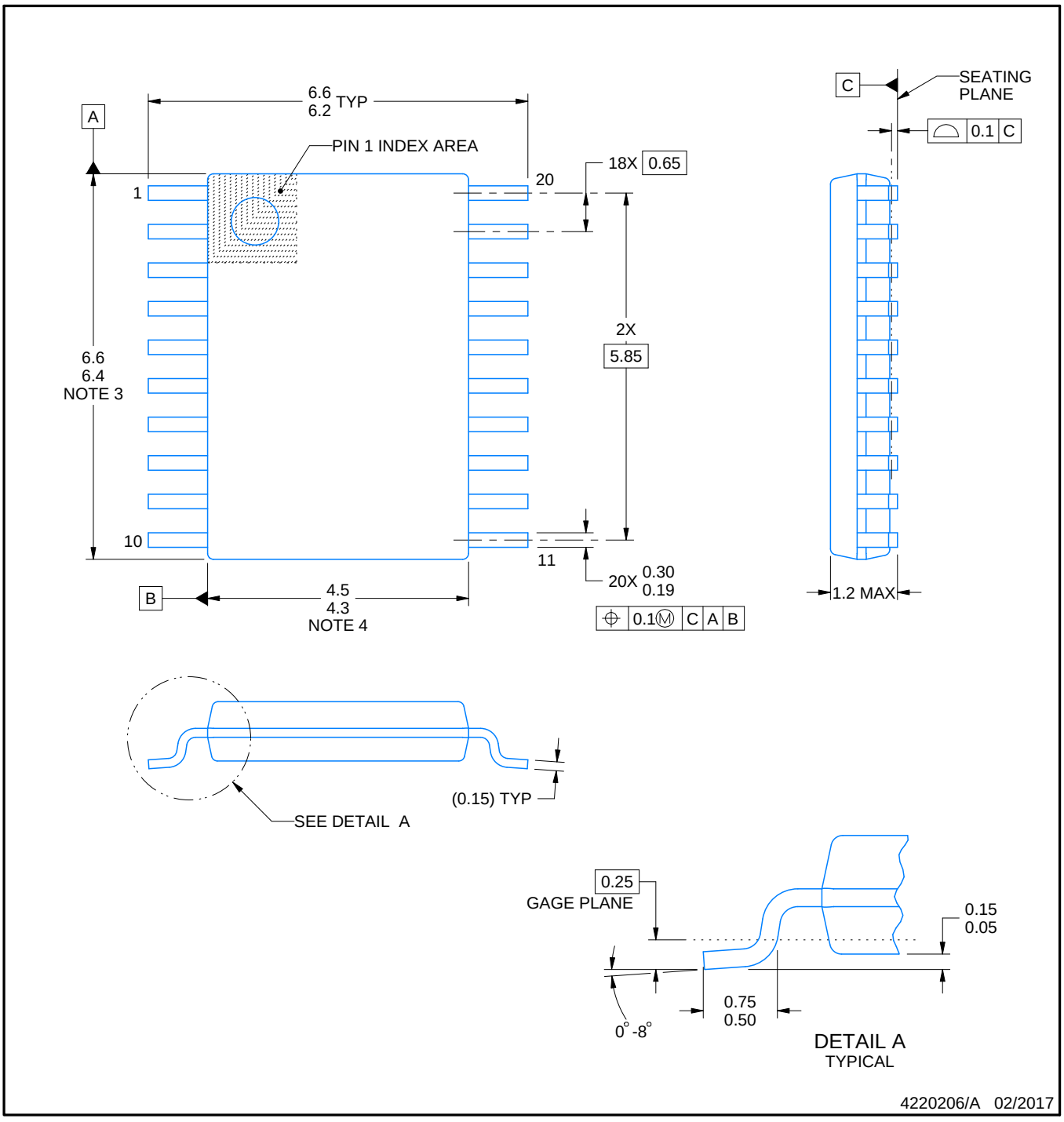
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7234PWR	TSSOP	PW	20	3000	356.0	356.0	35.0
TMUX7234RRQR	WQFN	RRQ	20	3000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0020A

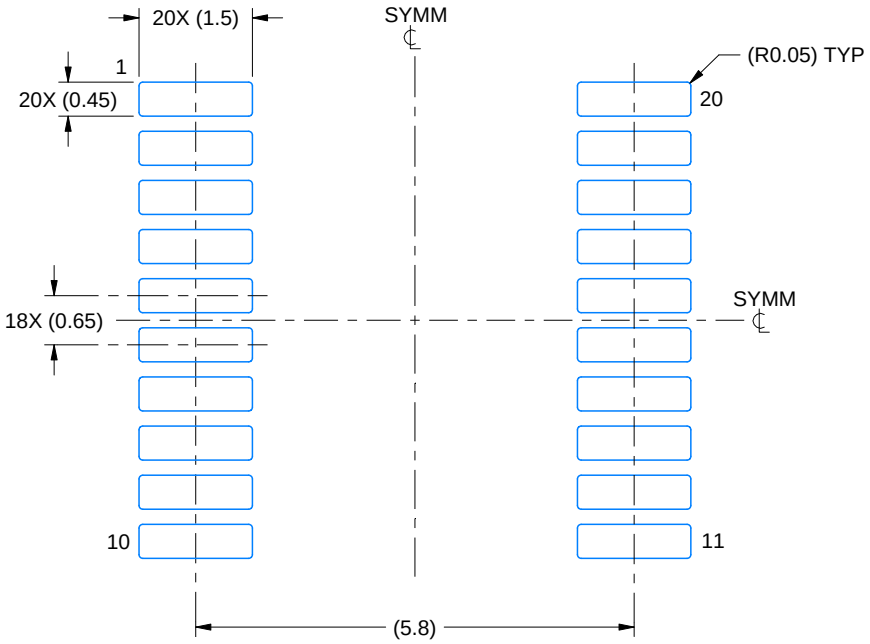
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

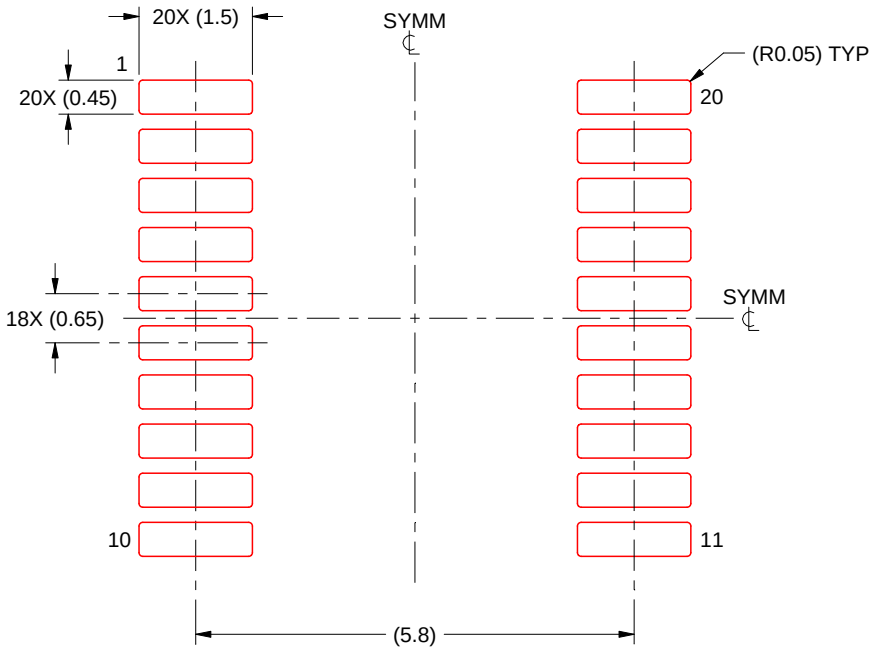
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

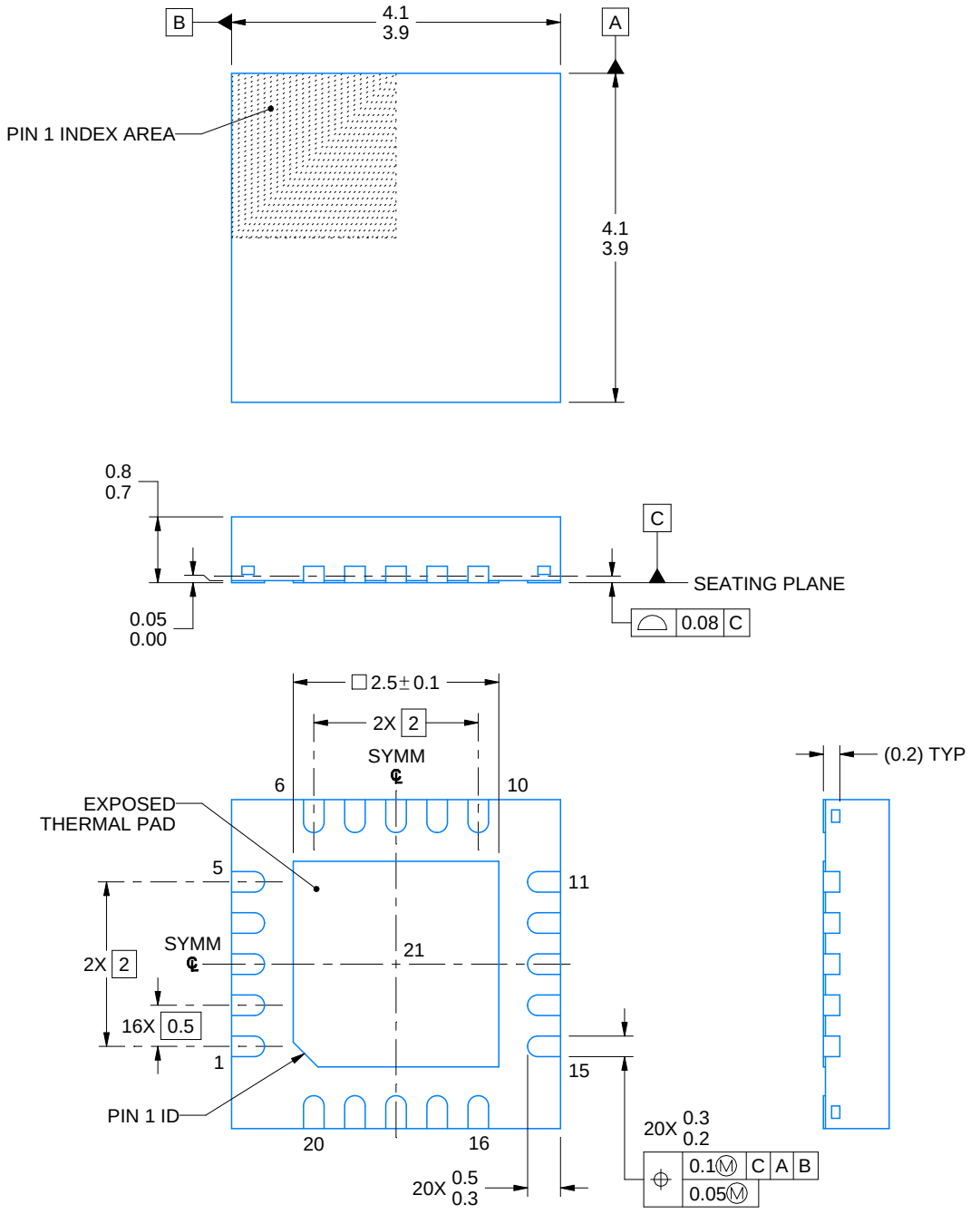
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RRQ0020A

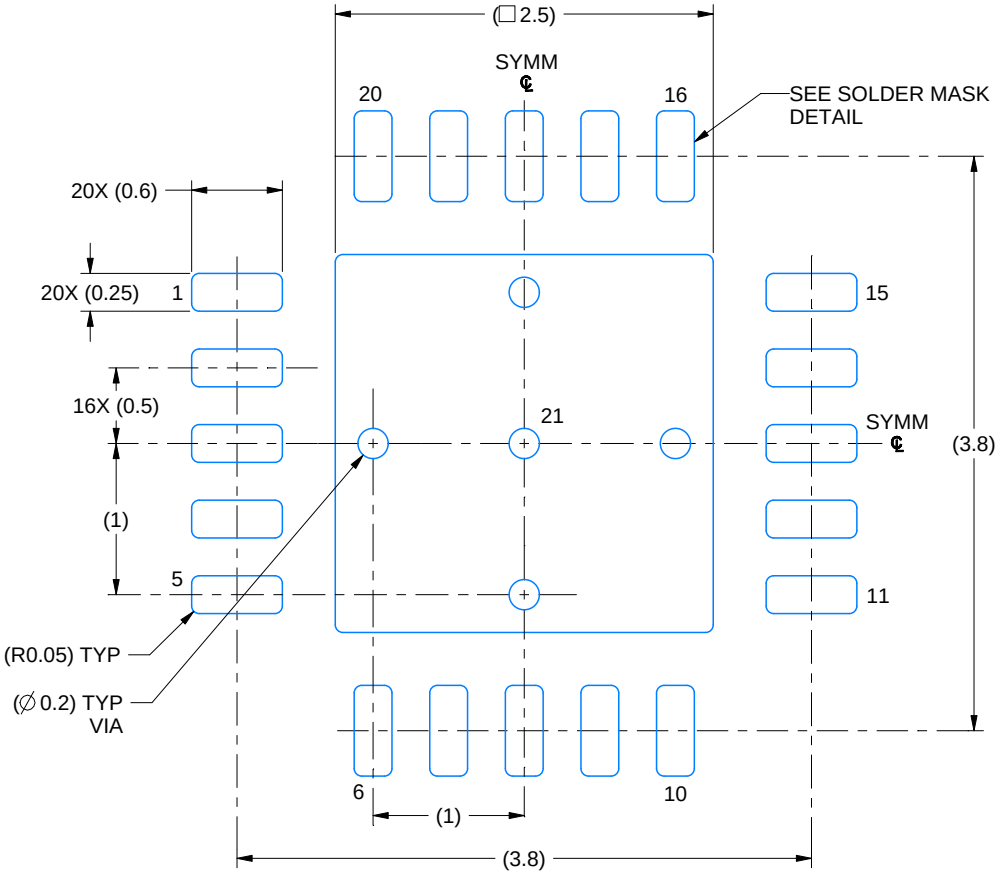
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

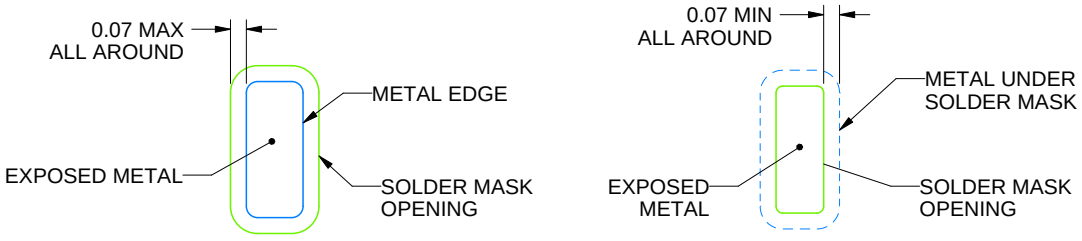


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224817/A 03/2019

NOTES: (continued)

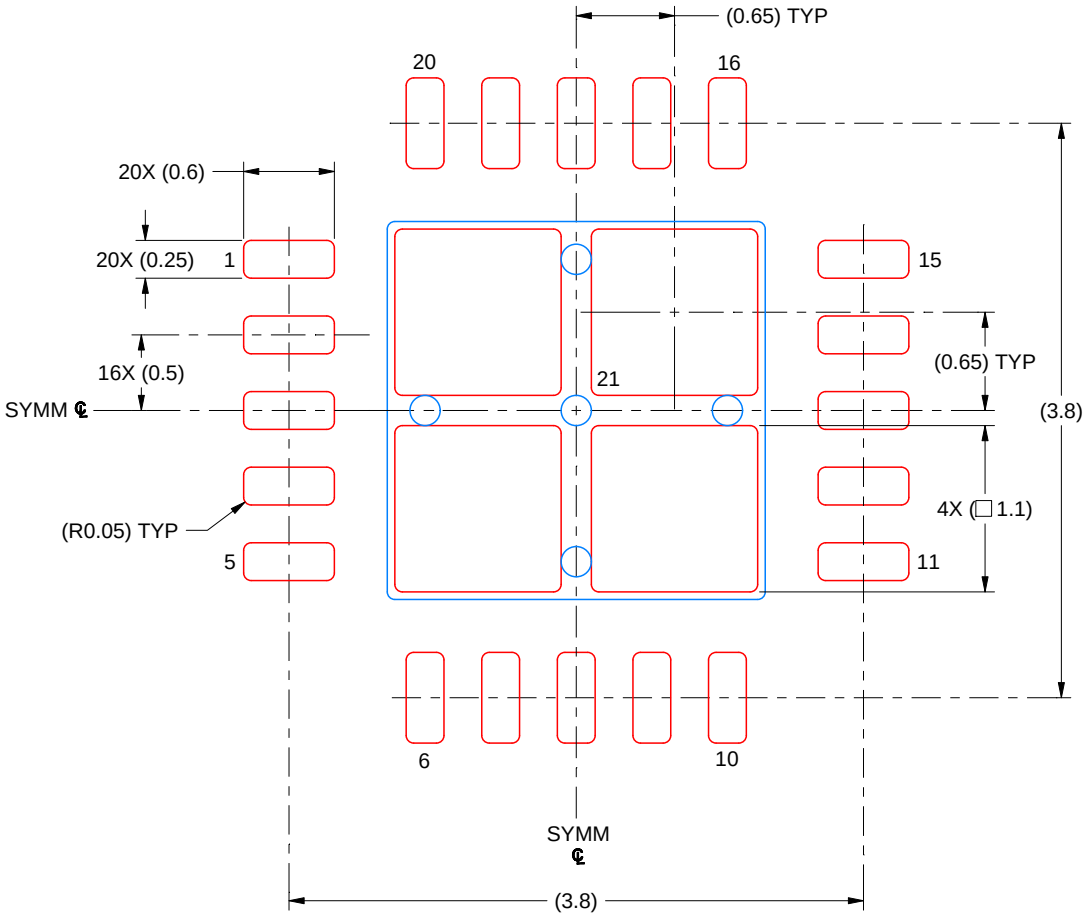
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RRQ0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224817/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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