

TIOL112 および TIOL112x IO-Link デバイス・トランシーバ、低残留電圧、および小型パッケージのサージ保護機能内蔵

1 特長

- 電源電圧: 7V~36V
- PNP、NPN、または IO-Link を構成可能な出力
 - IEC 61131-9 COM1、COM2、COM3 のデータ・レートをサポート
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- TIOL111(x) とピン互換でさらに性能向上
 - 低い残留電圧: 200mA で 0.5V (標準値)
 - アクティブ・ドライバの電流制限機能
 - パッケージの放熱性能向上
 - ドライバのスルーレートを下げてオーバーシュートを低減: 750ns (最大値)
- 堅牢なシステムのための保護機能を内蔵
 - ドライバの過電流制限を設定可能: 50mA~350mA
 - L+、CQ、L- で最大 65V のアクティブな逆極性保護
 - 過電流、過熱、UVLO フォルトのフォルト・インジケータ
 - 誘導性負荷に対する安全で高速な消磁
 - 拡張周囲温度動作範囲: -40°C~125°C
- L+ および CQ に EMC 保護を搭載
 - ±8kV IEC 61000-4-2 ESD 接触放電
 - ±4kV IEC 61000-4-4 電気的高速過渡
 - ±1.2kV/500Ω の IEC 61000-4-5 サージ
- 大容量負荷駆動能力
- 2μA 未満の CQ リーク電流
- 1.5mA 未満の無信号時電流
- 最大電流 20mA 対応の LDO オプションを搭載
 - TIOL1123: 3.3V LDO
 - TIOL1125: 5V LDO
 - TIOL1123L (YAH): 3.3V/5V の出力を選択可能
- リモート・ウェイクアップ通知およびウェイクアップ発生
- スペースを節約する小型のパッケージ・オプション
 - 3mm × 3mm の 10 ピン VSON パッケージ: TIOL111 とピン互換
 - 2.45mm x 1.7mm の DSBGA パッケージ

2 アプリケーション

- フィールド・トランスミッタおよびアクチュエータ
- ファクトリ・オートメーション
- プロセス・オートメーション
- リモート IO の IO-link PHY

3 概要

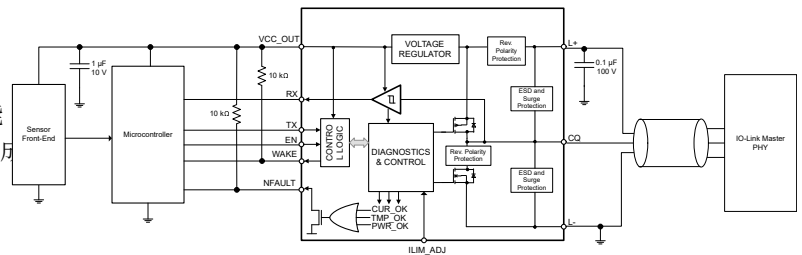
TIOL112(x) ファミリのトランシーバには、産業用の双方向ポイント・ツー・ポイント通信向けに IO-Link インターフェイスが実装されています。このデバイスが 3 線式のインターフェイス経由で IO-Link マスタに接続されているとき、マスタは通信を開始してリモート・ノードとデータを交換でき、TIOL112(x) はこの通信の完全な物理層として機能します。

これらのデバイスは、最大 1.2kV (500Ω) の IEC 61000-4-5 サージに耐えることができ、また、逆極性保護を内蔵しています。ピンによりプログラム可能なインターフェイスを使って、コントローラ回路と容易に接続できます。出力電流制限は、外付けの抵抗を使用して構成できます。TIOL112(x) はウェイクアップ・パルスを生成するように構成することができ、IO-Link のマスター・アプリケーションで使用できます。低電圧、過電流、過熱状態に対するフォルト通知および内部保護機能を備えています。

デバイス情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TIOL112	VSON (10)	3.00mm × 3.00mm
TIOL1123		
TIOL1125		
TIOL112	DSBGA (12)	2.45mm × 1.70mm
TIOL1123		

(1) 利用可能なデバイスについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーションの図



Table of Contents

1 特長.....	1	8.2 Functional Block Diagrams.....	13
2 アプリケーション.....	1	8.3 Feature Description.....	14
3 概要.....	1	8.4 Device Functional Modes.....	21
4 Revision History.....	2	9 Application and Implementation.....	22
5 Pin Configuration and Functions.....	3	9.1 Application Information.....	22
6 Specifications.....	5	9.2 Typical Application.....	22
6.1 Absolute Maximum Ratings.....	5	9.3 Power Supply Recommendations.....	26
6.2 ESD Ratings.....	5	9.4 Layout.....	26
6.3 ESD Ratings - IEC Specifications.....	5	10 Device and Documentation Support.....	27
6.4 Recommended Operating Conditions.....	5	10.1 Receiving Notification of Documentation Updates.....	27
6.5 Thermal Information.....	6	10.2 サポート・リソース.....	27
6.6 Electrical Characteristics.....	6	10.3 Trademarks.....	27
6.7 Switching Characteristics.....	8	10.4 静電気放電に関する注意事項.....	27
6.8 Typical Characteristics.....	9	10.5 用語集.....	27
7 Parameter Measurement Information.....	10	11 Mechanical, Packaging, and Orderable Information.....	27
8 Detailed Description.....	13		
8.1 Overview.....	13		

4 Revision History

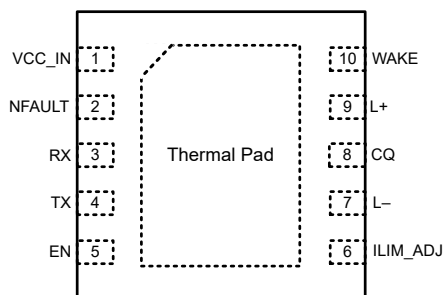
Changes from Revision C (January 2023) to Revision D (March 2023)	Page
• Added the package outline and land pattern images for the YAH (DSBGA) 12-pin package.....	27

Changes from Revision B (December 2022) to Revision C (January 2023)	Page
• 「製品情報」表で DSBGA パッケージの事前情報の注記を削除.....	1

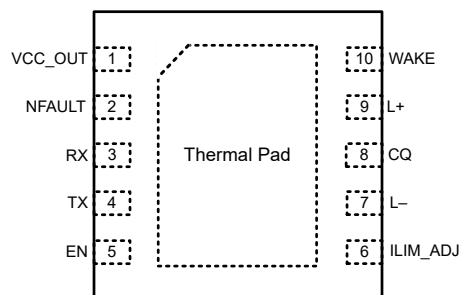
Changes from Revision A (April 2022) to Revision B (December 2022)	Page
• Removed the conditional note 2 from the <i>IEC Ratings - ESD Specifications</i> table that specified 4.5kV when EN=TX=HIGH	5
• Changed the description of $I_{(VCC_OUT)}$ from: (TIOL112L only) to: TIOL1123(L), TIOL1125 only in the <i>Recommended Operating Conditions</i> table.....	5
• Changed 図 6-4 and 図 6-6	9
• Added application curves Figure 9-6 and Figure 9-7 showing inductive load demagnetization.....	25

Changes from Revision * (February 2022) to Revision A (April 2022)	Page
• 「デバイス情報」表で VSON パッケージの TIOL112 および TIOL1125 から事前情報の注記を削除.....	1

5 Pin Configuration and Functions



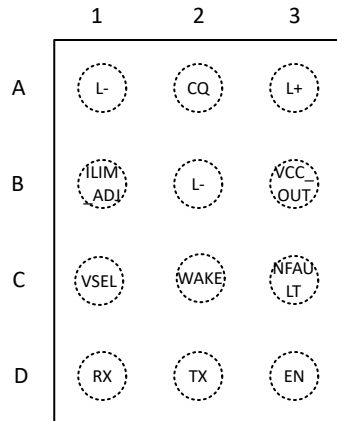
**5-1. TIOL112
DRC (VSON), 10-Pin
(Top View)**



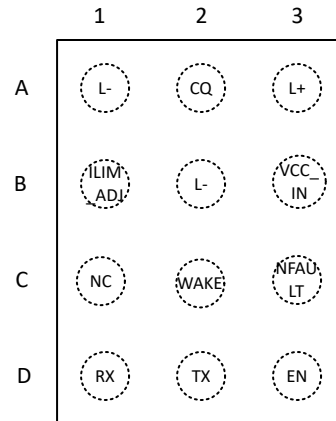
**5-2. TIOL1123, TIOL1125
DRC (VSON), 10-Pin
(Top View)**

表 5-1. Pin Functions (VSON Package)

PIN NO	PIN NAME		TYPE	DESCRIPTION
	TIOL112	TIOL1123 TIOL1125		
1	VCC_IN	VCC_OUT	P	VCC_IN (TIOL112): External 3.3-V or 5-V logic supply input pin. VCC_OUT (TIOL1123, TIOL1125): 3.3-V or 5-V linear regulator output
2	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. A low level indicates either an over- current, an undervoltage supply or an overtemperature condition.
3	RX	RX	O	Receive data output to the local microcontroller
4	TX	TX	I	Transmit data input from the local microcontroller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
5	EN	EN	I	Driver enable input signal from the local microcontroller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
6	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and L-.
7	L-	L-	GND	IO-Link ground potential
8	CQ	CQ	I/O	IO-Link data signal (bidirectional)
9	L+	L+	P	IO-Link supply voltage (24 V nominal)
10	WAKE	WAKE	O	Wake-up indicator to the local microcontroller. Open-drain output, connect this pin via pull-up resistor to VCC_IN/OUT.
	Thermal Pad	Thermal Pad	—	Connect to L- for optimal thermal and electrical performance



**图 5-3. TIOL1123L
YAH (DSBGA), 12-Pin
(Top View)**



**图 5-4. TIOL112
YAH (DSBGA), 12-Pin
(Top View)**

表 5-2. Pin Functions (DSBGA)

PIN NO	PIN NAME		TYPE	DESCRIPTION
	TIOL112	TIOL1123L		
B3	VCC_IN	VCC_OUT	P	VCC_IN (TIOL112): External 3.3-V or 5-V logic supply input pin. VCC_OUT (TIOL1123): 3.3-V or 5-V linear regulator output
C3	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. A low level indicates either an over-current, an undervoltage supply or an overtemperature condition.
D1	RX	RX	O	Receive data output to the local controller
D2	TX	TX	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
D3	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
B1	ILIM_ADJ	ILIM_ADJ	O	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and L-.
A1, B2	L-	L-	GND	IO-Link ground potential
A2	CQ	CQ	I/O	IO-Link data signal (bidirectional)
A3	L+	L+	P	IO-Link supply voltage (24 V nominal)
C1	NC	VSEL	I	TIOL112 (NC): Leave floating. Do not connect. TIOL1123 (VSEL): Connect to GND for 5V LDO output. Please leave this pin floating for 3.3V LDO output. VSEL has an internal pull-up of 1 MΩ
C2	WAKE	WAKE	O	Wake-up indicator to the local controller. Open-drain output, connect this pin via pull-up resistor to VCC_IN/OUT.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for L+ and CQ	–65	65	V
	Transient pulse width < 100 µs for L+ and CQ	–70	70	V
Voltage difference	$ V_{(L+)} - V_{(CQ)} $		65	V
Logic supply voltage (TIOL112)	VCC_IN	–0.3	6	V
Input logic voltage	TX, EN, VSEL	–0.3	$\min(V_{CC_IN} + 0.3, 6)$	V
Output current	RX, WAKE, NFAULT	–5	5	mA
Storage temperature, T _{stg}		–55	170	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the L- pin, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins	±4000	V
V _(ESD)	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	All pins	±750	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), L+, CQ and L- ⁽¹⁾	±8,000	V
	Electrostatic discharge	IEC 61000-4-5, 1.2 µs/50 µs Surge with 500 Ω in series, L+, CQ and L- ⁽¹⁾	±1,200	
	Electrostatic discharge	IEC 61000-4-4 EFT (Fast transient or burst), L+, CQ and L- ⁽¹⁾	±4,000	

- (1) Minimum 100-nF capacitor is required between L+ and L-. Minimum 1-µF capacitor is required between VCC_IN/VCC_OUT and L-.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _(L+)	Supply voltage		7	24	36	V
V _(VCC_IN)	Logic level input voltage (TIOL112 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R _{SET}	External resistor for CQ current limit		0		110	kΩ
1/t _{BIT}	Data rate (Communication mode)				250	kbps
I _(VCC_OUT)	LDO output current (TIOL1123(L), TIOL1125 only)				20	mA
T _A	Operating ambient temperature		–40		125	°C
T _J	Junction temperature				150	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TIOL112, TIOL1123, TIOL1125	TIOL112, TIOL1123L	UNIT
		DRC (10 Pins)	YAH (12 Pins)	
R _{θJA}	Junction-to-ambient thermal resistance	45.9	79.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	45.9	0.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.9	19.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.7	0.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	17.8	19.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at L₊ = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (L+)						
I _(L+)	Quiescent supply current	EN = LOW, no load		1	1.5	mA
		EN = HIGH, no load		2	2.95	mA
LOGIC-LEVEL INPUTS (EN, TX, VSEL)						
V _{IL}	Input logic low voltage				0.8	V
V _{IH}	Input logic high voltage		2			V
R _{PD}	Pull-down (EN) resistance			100		kΩ
R _{PU}	Pull-up (TX) resistance			200		kΩ
R _{PU}	Pull-up (VSEL) resistance			1000		kΩ
CONTROL OUTPUTS (WAKE, NFAULT)						
V _{OL}	Output logic low voltage	I _O = 4 mA			0.5	V
I _{OZ}	Output high impedance leakage	Output in Hi-Z, V _O = 0 V or VCC_IN/OUT	−1		1	μA
DRIVER OUTPUT (CQ)						
R _{DS(ON)}	High-side driver on-resistance			2.5	4.5	Ω
V _{DS(ON)}	High-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
R _{DS(ON)}	Low-side driver on-resistance			2.5	4.5	Ω
V _{DS(ON)}	Low-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
I _{OZ(CQ)}	CQ leakage	EN = LOW, 0 ≤ V _(CQ) ≤ (V _(L+) - 0.1 V)	−2		2	μA
I _{LLM}	CQ load discharge current	EN = LOW, R _{SET} = 0 to 5 kΩ ⁽²⁾ , V _(CQ) ≥ 5 V	5		15	mA
I _{O(LIM)}	Driver output current limit	R _{SET} = 110 kΩ; V _(CQ) = (V _(L+) - 3) V or 3 V	35	50	70	mA
		R _{SET} = 10 kΩ	300	350	400	mA
		R _{SET} = 0 to 5 kΩ ⁽²⁾ V _(CQ) = (V _(L+) - 3) V or 3 V T _J < T _(SDN) or t < 200 μs ⁽⁷⁾	500			mA
		(Fast-detect mode) R _{SET} = OPEN ⁽¹⁾ V _(CQ) = (V _(L+) - 3) V or 3 V	260	330	400	mA
RECEIVER INPUT (CQ)						
V _(THH)	Input threshold “H”	V _(L+) > 18 V, EN= LOW	10.5		13	V
V _(THL)	Input threshold “L”		8		11.5	V
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))		0.75			V
V _(THH)	Input threshold “H”	V _(L+) < 18 V, EN= LOW	See Note ⁽⁴⁾		See Note ⁽⁵⁾	V

6.6 Electrical Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at $V_{L+} = 24\text{ V}$, $V_{VCC_IN} = 3.3\text{ V}$, $V_{VCC_OUT} = 3.3\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _(THL)	Input threshold "L"	V _(L+) < 18 V, EN= LOW		See Note ⁽⁶⁾		See Note ⁽⁷⁾	V
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))			0.75		V	
V _{OL}	RX output low voltage	I _{OL} = 4 mA				0.4	V
V _{OH}	RX output high voltage	I _{OL} = −4 mA		VCC_IN/ OUT−0.5			V
PROTECTION CIRCUITS							
V _(UVLO)	L+ under voltage lockout	L+ falling; NFAULT = Hi-Z		6	6.3		V
		L+ rising; NFAULT = LOW			6.5	6.8	V
V _(UVLO,HYS)	L+ under voltage hysteresis	Rising to falling threshold		200			mV
V _(UVLO_IN)	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z		2.3			V
		VCC_IN rising; NFAULT = LOW		2.5			V
V _(UVLO,HYS)	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold		190			mV
T _(WRN)	Thermal warning	Die temperature T _J		125			°C
T _(SDN)	Thermal shutdown			150	160		°C
T _(HYS)	Thermal hysteresis for shutdown			14			°C
T _(WRN)	Thermal hysteresis for warning	Die temperature T _J		14			°C
I _{REV}	Leakage current in reverse polarity	EN=LOW, TX=x; V _(CQ) < V _(L-) or V _(CQ) > V _(L+) , up to 36 V		60			μA
		EN=LOW, TX=x; V _(CQ) < V _(L-) or V _(CQ) > V _(L+) , up to 65 V		110			μA
		EN = HIGH, TX = LOW; V _(CQ to L+) = 3 V		640			μA
		EN = HIGH, TX = HIGH; V _(CQ to L-) = -3 V		10			μA
LINEAR REGULATOR (LDO)							
V _(VCC_OUT)	Voltage regulator output	TIOL1125, TIOL1123L (5V)		4.75	5	5.25	V
		TIOL1123, TIOL1123L (3.3V)		3.13	3.3	3.46	V
V _(DROP)	Voltage regulator drop-out voltage (V _(L+) − V _(VCC_OUT))	I _{CC} = 20 mA load current	TIOL1125, TIOL1123L (5V)	0.75		1.9	V
			TIOL1123, TIOL1123L (3.3V)	0.75		2.3	V
REG	Line regulation (dV _(VCC_OUT) /dV _(L+))	I _(VCC_OUT) = 1 mA				1.7	mV/V
L _{REG}	Load regulation (dV _(VCC_OUT) /V _(VCC_OUT))	V _(L+) = 24 V, I _(VCC_OUT) = 100 μA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, I _(VCC_OUT) = 20 mA		40			dB

- (1) Current fault indication will be active. Current fault auto recovery will be de-activated.
- (2) Current fault indication and current fault auto recovery will be de-activated.
- (3) If operating continuously with this current limit, ensure that the current through the device does not cause the T_J to be greater than $T_{(SDN)}$ for a given ambient temperature and thermal property of the system. For pulse durations $t < 200\text{ }\mu\text{s}$, the device can source or sink current of at least 500 mA across the recommended operating conditions. For YAH (DSBGA) package, this parameter is specified by design and characterization.
- (4) $V_{THH}(\text{min}) = 5\text{ V} + (11/18) [V_{(L+)} - 8\text{ V}]$
- (5) $V_{THH}(\text{max}) = 6.5\text{ V} + (13/18) [V_{(L+)} - 8\text{ V}]$
- (6) $V_{THL}(\text{min}) = 4\text{ V} + (8/18) [V_{(L+)} - 8\text{ V}]$
- (7) $V_{THL}(\text{max}) = 6\text{ V} + (11/18) [V_{(L+)} - 8\text{ V}]$

6.7 Switching Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at $L_+ = 24\text{ V}$, $V_{VCC_IN} = 3.3\text{ V}$, $V_{VCC_OUT} = 3.3\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{PLH}, t_{PHL}	Driver propagation delay	See 7-1 See 7-2 See 7-3 $R_L = 2\text{ k}\Omega$ $C_L = 5\text{ nF}$ $R_{(SET)} = 10\text{ k}\Omega$		600	1200	ns
$t_{P(skew)}$	Driver propagation delay skew. $ t_{PLH} - t_{PHL} $			75		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	μs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	μs
t_r, t_f	Driver output rise, fall time		200		700	ns
$ t_r - t_f $	Difference in rise and fall time			50		ns
t_{WU1}	Wake-up recognition begin	See 7-5	45	60	75	μs
t_{WU2}	Wake-up recognition end		85	100	145	μs
t_{PWAKE}	Wake-up output delay				150	μs
t_{SC}	Current fault blanking time		175	200		μs
t_{pSC}	Current fault indication delay				280	μs
t_{WUL}	Wake output pulse duration on wake detection in EN=L mode	See 7-6	175	225	285	μs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	CQ re-enable delay after UVLO ⁽¹⁾	$V_{(UVLO)}$ rising threshold crossing time to CQ enable time	10	30	50	ms
RECEIVER						
t_{ND}	Noise suppression time ⁽²⁾				250	ns
t_{PLH}, t_{PHL}	Receiver propagation delay	See 7-4 15-pF load on RX,		150	300	ns

(1) CQ output remains Hi-Z for this time

(2) Noise suppression time is defined as the permissible duration of a receive signal above/below the detection threshold without detection taking place.

6.8 Typical Characteristics

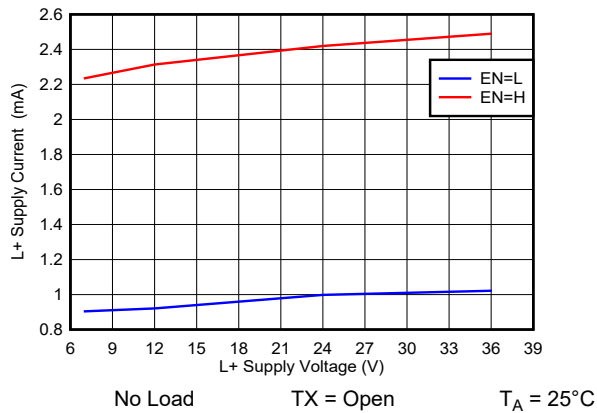


Figure 6-1. Supply Current vs Supply Voltage

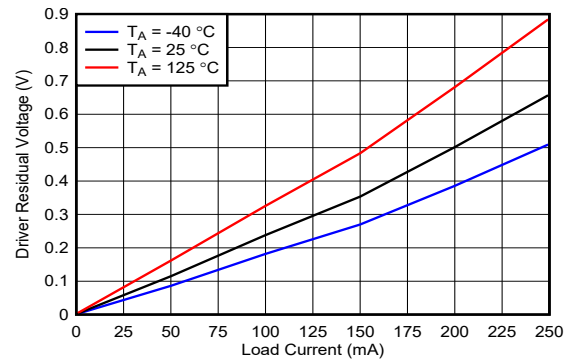


Figure 6-2. Residual Voltage vs Load Current: High Side

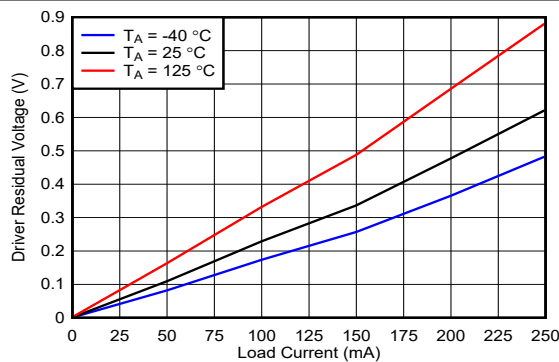
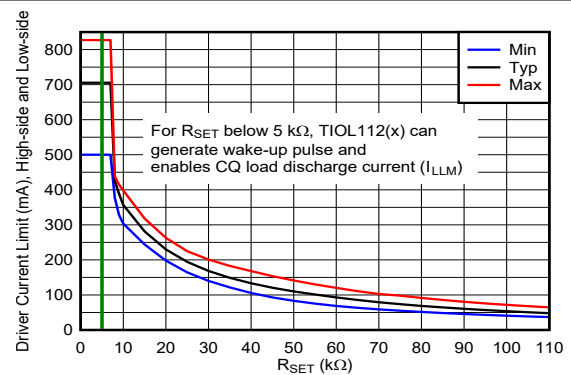


Figure 6-3. Residual Voltage vs Load Current: Low Side



For R_{SET} in the 0-5 kΩ range, TIOL112(x) can source/sink 500 mA required for wake-up pulse generation in IO-link applications. For R_{SET} in the 0-5 kΩ range, TIOL112(x) also activates a pull-down current source (I_{LLM}) when the driver is disabled. Min and max curves specified by design and characterization across temperature and process variation.
 $T_A = 25^\circ\text{C}$ (typ curve)

Figure 6-4. Current Limit vs R_{SET}

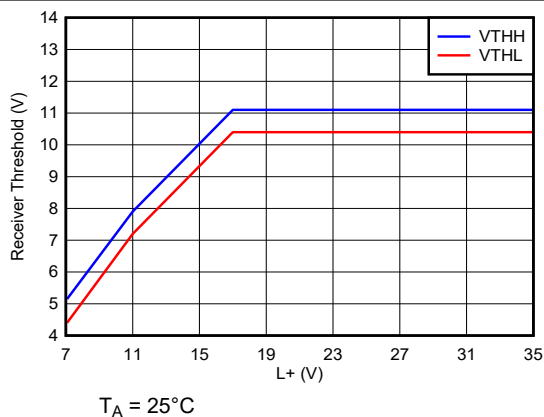


Figure 6-5. Receiver Threshold Boundaries

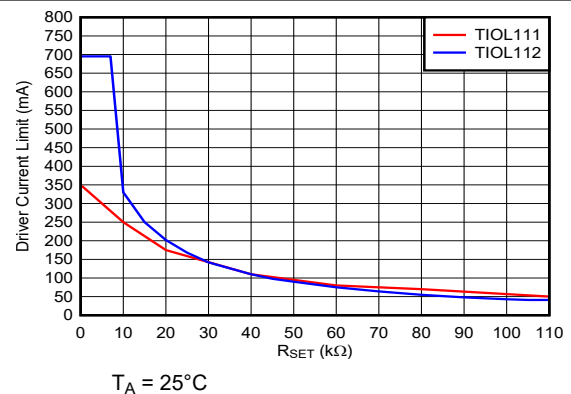
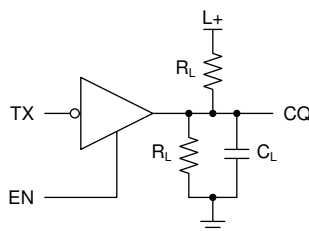


Figure 6-6. Current limit vs R_{SET} : TIOL112(x) vs TIOL111(x)

7 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated

FIG 7-1. Test Circuit for Driver Switching

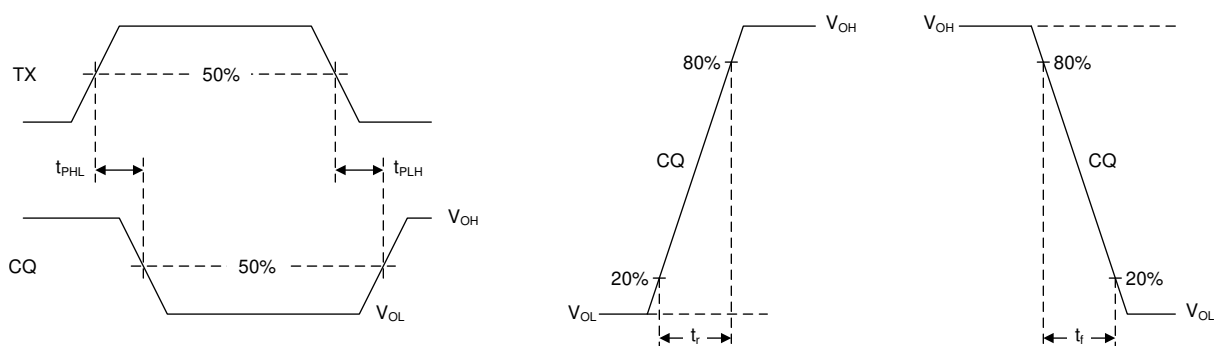


FIG 7-2. Waveforms for Driver Output Switching Measurements

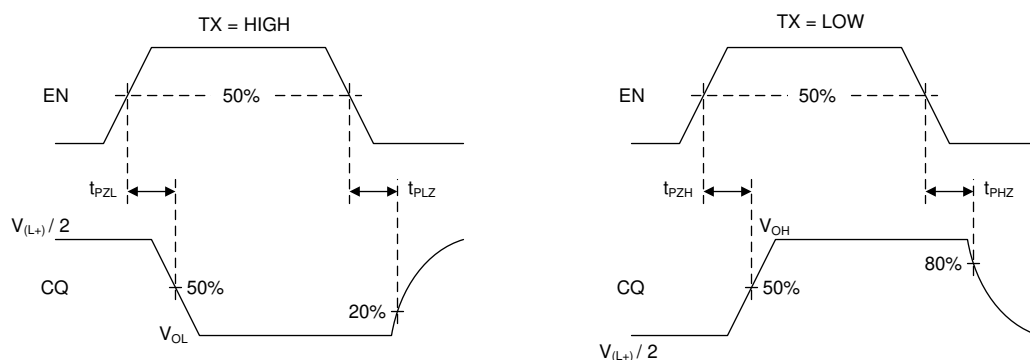


FIG 7-3. Waveforms for Driver Enable or Disable Time Measurements

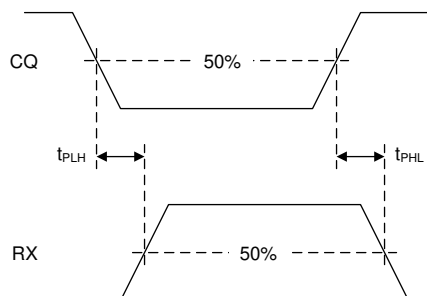
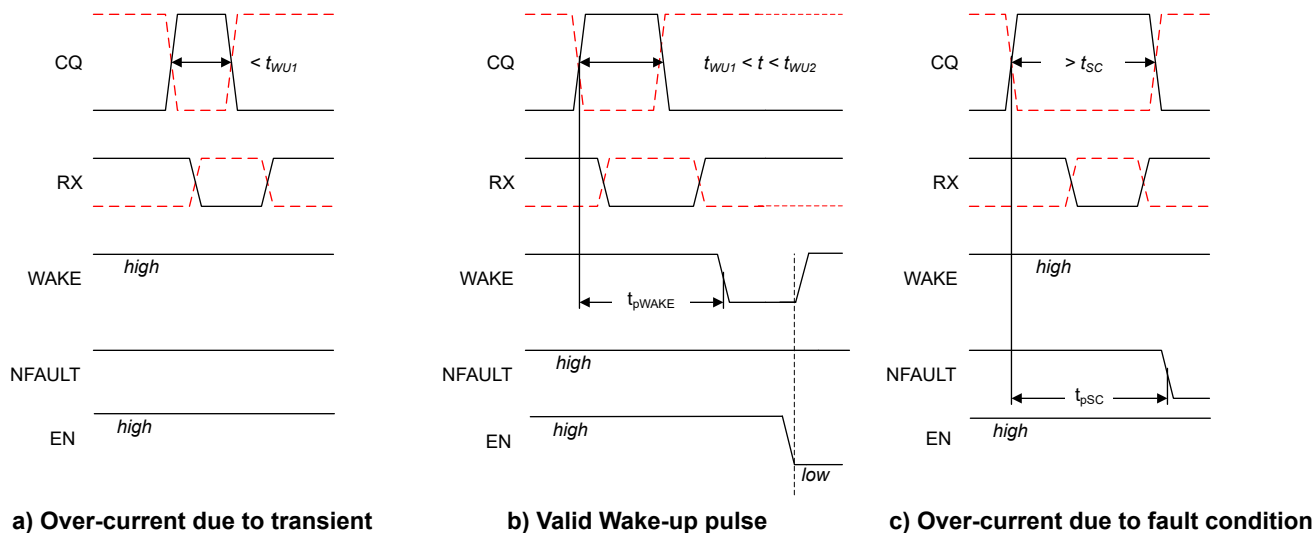
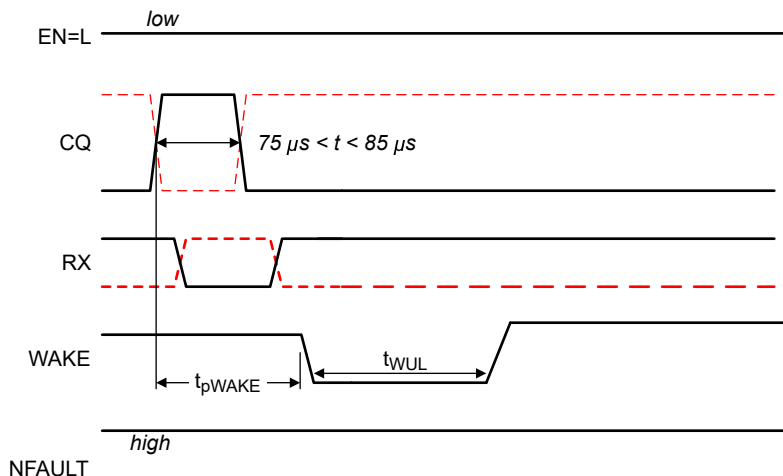


FIG 7-4. Receiver Switching Measurements



7-5. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ = 10 kΩ to 110 kΩ, TX = H (Full Lines); and TX = L (Red Dotted Lines)



7-6. Wake Conditions for EN = L, RX = H (Full Lines); and RX = L (Red Dotted Lines)

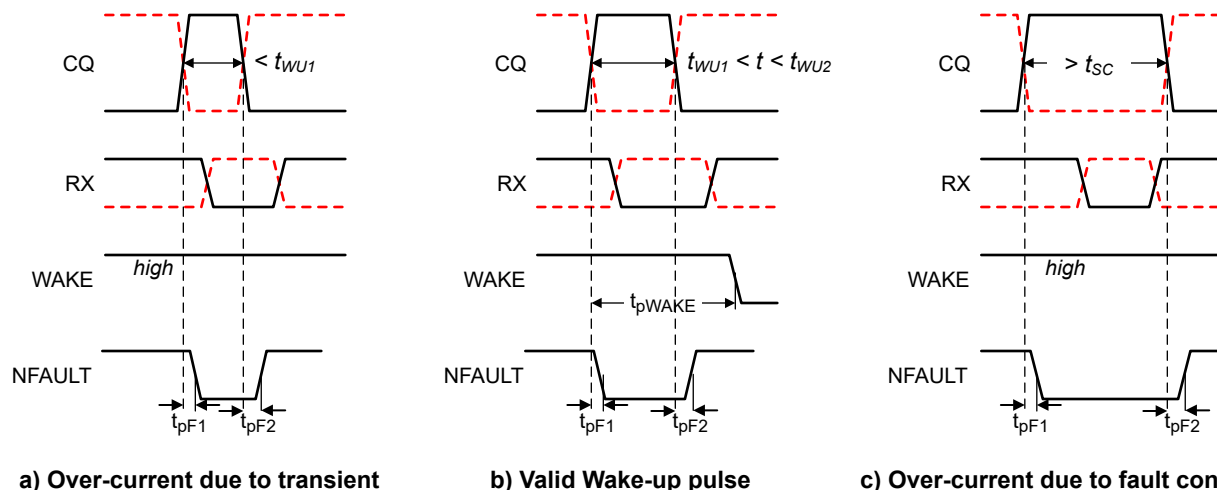


图 7-7. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ is floating, TX = H (Full Lines); and TX = L (Red Dotted Lines)

8 Detailed Description

8.1 Overview

Figure 8-1 shows that the TIOL112 or TIOL112x driver output (CQ) can be used in either push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (TX) input pins. The internal receiver converts the 24-V signal on the CQ line to standard logic levels on the receive data (RX) pin. A simple parallel interface is used to receive/transmit data and status information between the device and the local controller.

These devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ± 70 -V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system level design by reducing external protection circuitry.

TIOL112 or TIOL112x transceivers implement protection features for overcurrent, overvoltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The devices derive the low-voltage supply from the IO-Link L+ voltage (24 V nominal) via an internal linear regulator to provide power to the local controller and sensor circuitry.

8.2 Functional Block Diagrams

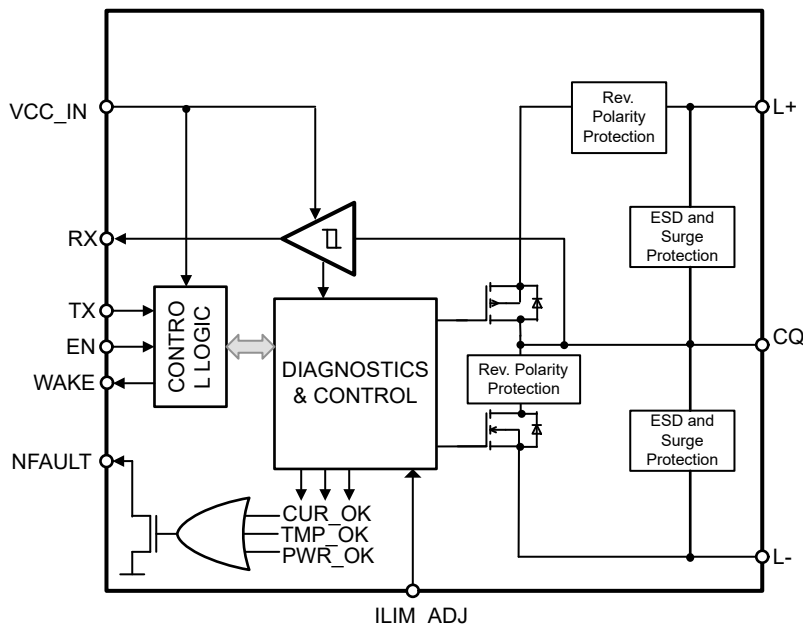
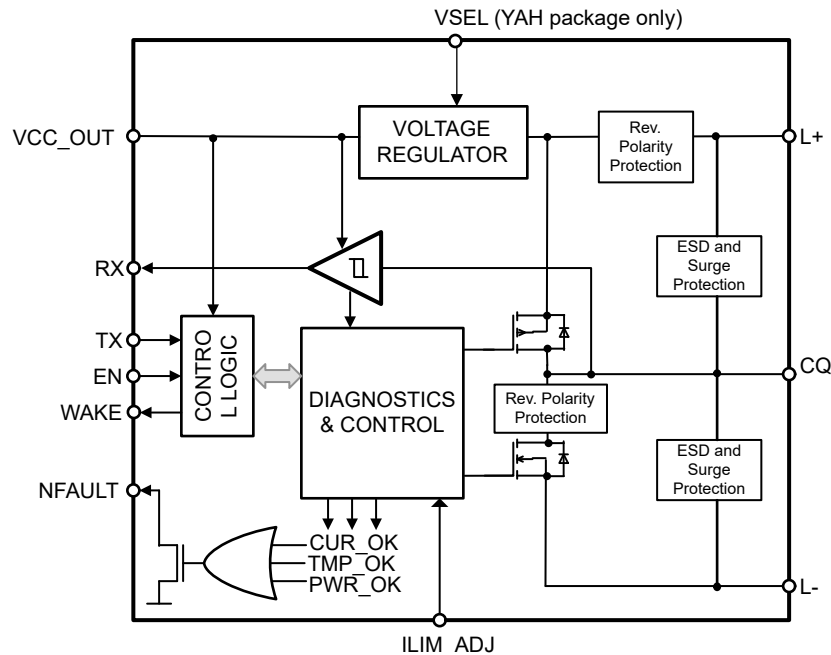


Figure 8-1. Block Diagram TIOL112



8-2. Block Diagram TIOL1123(L), TIOL1125

8.3 Feature Description

8.3.1 Wake-Up Detection

The TIOL112(x) may be operated in IO-Link mode or Standard Input / Output (SIO) mode. If the device is in SIO mode and the IO-link master node wants to initiate communication with the device node, the master drives the CQ line to the opposite of its present state, and will either sink or source the current (≥ 500 mA) for the wake-up duration (typically 80 μ s) depending on the CQ logic level as per the IO-Link specification. The TIOL112(x) detects this as a wake-up condition and communicates to the local microcontroller via the WAKE pin. The IO-Link communication specification requires the device node to switch to receive mode within 500 μ s after receiving the wake-up signal.

For overcurrent conditions shorter or longer than a valid wake-up pulse, the WAKE pin remains in a high-impedance (inactive) state. This is illustrated in 7-5.

If the driver of TIOL112(x) is disabled ($EN = L$), any change in CQ logic level for duration $t_{WU1} < t < t_{WU2}$ is detected as a wake-up event and WAKE asserts low for the duration of t_{WUL} . This is illustrated in 7-6. Please refer to 表 8-4 for the summary of the conditions for Wake-Up detection.

8.3.2 Current Limit Configuration

The output current can be configured with an external resistor on ILIM_ADJ pin. The highest current limit setting with an external resistor of 10 k Ω provides a minimum of 300 mA over the operating temperature and voltage range.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

When ILIM_ADJ pin is shorted to ground, the TIOL112(x) is configured to be in the IO-link master mode. In this mode, the TIOL112(x) can source or sink minimum of 500 mA to generate a wake-up request. In addition, the TIOL112(x) enables a small current sink of 5 mA (minimum). The current fault indication, output disable, and auto recovery features are disabled in this mode.

表 8-1. Current Limit Configuration

ILIM_ADJ Pin Condition	CQ Current Limit (Min.)	NFAULT Indication During Current Fault	Output Disable and Auto Recovery
R _{SET} resistor to L- (10 kΩ to 110 kΩ)	Variable (35 mA to 300 mA)	Yes	Yes
Connected to L- (R _{SET} 0 to 5 kΩ)	500 mA	No	No
OPEN	260 mA	Yes	No

8.3.3 Current Fault Detection, Indication and Auto Recovery

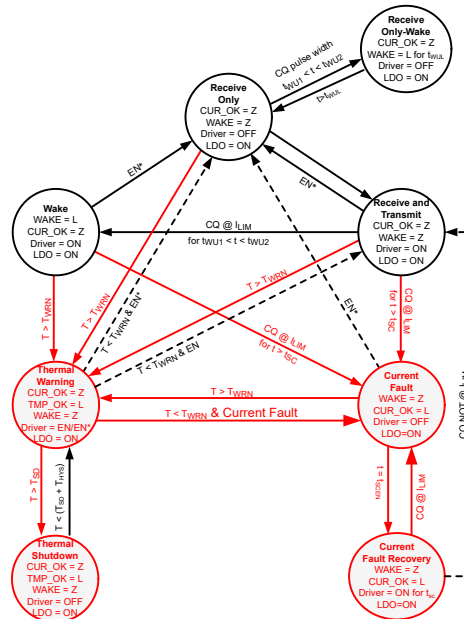
If the output current at CQ exceeds the internally-set current limit $I_{O(LIM)}$ for a duration longer than t_{SC} , the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN. See 表 8-5. Toggling EN will clear NFAULT.

8.3.4 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and TX pins.

8.3.5 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



Note: NFAULT = [CUR_OK && PWR_OK && TMP_OK]

図 8-3. Device State Diagram

8.3.6 Transceiver Function Tables

表 8-2. Driver Function

EN	TX	CQ	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	CQ is sourcing current (high-side drive)
H	H / Open	L	CQ is sinking current (low-side drive)

表 8-3. Receiver Function

CQ VOLTAGE	RX	COMMENT
$V_{(CQ)} < V_{(THL)}$	H	Normal receive mode, input low
$V_{(THL)} < V_{(CQ)} < V_{(THH)}$	?	Indeterminate output, may be either high or low
$V_{(THH)} < V_{(CQ)}$	L	Normal receive mode, input high
Open	?	Indeterminate output, may be either high or low

表 8-4. Wake-Up Function ($t_{WU1} < t < t_{WU2}$)

EN	TX	CQ CURRENT	WAKE	COMMENT
L / Open	X	X	Asserts low for t_{WUL}	Device asserts low for t_{WUL} if RX output changes high-to-low or low-to-high for $t_{WU1} < t < t_{WU2}$
H	H / Open	$ I_{(CQ)} \geq 500 \text{ mA}$	L	Device receives high-level wake-up request over the IO-Link bus
H	L	$ I_{(CQ)} \geq 500 \text{ mA}$	L	Device receives low-level wake-up request over the IO-Link bus

表 8-5. Current Limit Indicator Function ($t > t_{SC}$)

EN	TX	CQ CURRENT	NFAULT	COMMENT
H	H / Open	$ I_{(CQ)} > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$ I_{(CQ)} < I_{O(LIM)}$	Z	Normal operation
H	L	$ I_{(CQ)} > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$ I_{(CQ)} < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, Current limit indicator is inactive

注

Current limit indicator function is disabled when ILIM_ADJ is connected to GND (or $R_{SET} < 5 \text{ k}\Omega$)

8.3.7 The Integrated Voltage Regulator (LDO)

The TIOL1123 and TIOL1125 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for L+ voltages in the range of 7 V to 36 V with respect to L-. The LDO is capable of delivering up to 20 mA.

In the DSBGA (YAH) package, TIOL1123L offers pin-configurable LDO output via VSEL pin. When VSEL is connected to GND, VCC_OUT is configured to provide a 5-V output. When VSEL is left floating, VCC_OUT provides a 3.3-V output.

表 8-6. LDO Output Configuration via VSEL pin (YAH Package)

VSEL pin connection	VCC_OUT
Connected to L-	5 V
Floating	3.3 V

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μ F or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω . With tolerance and dc bias effects, the minimum capacitance for stability is 1 μ F.

The voltage regulator has an internal 35-mA current limit to protect against initial start-up inrush current due to large decoupling capacitors and accidental short circuit conditions.

8.3.8 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the L+, CQ and L- pins. The maximum voltage between any of the pins may not exceed 65 V DC at any time.

Figure 8-4 and Figure 8-5 shows all the possible connection combinations.

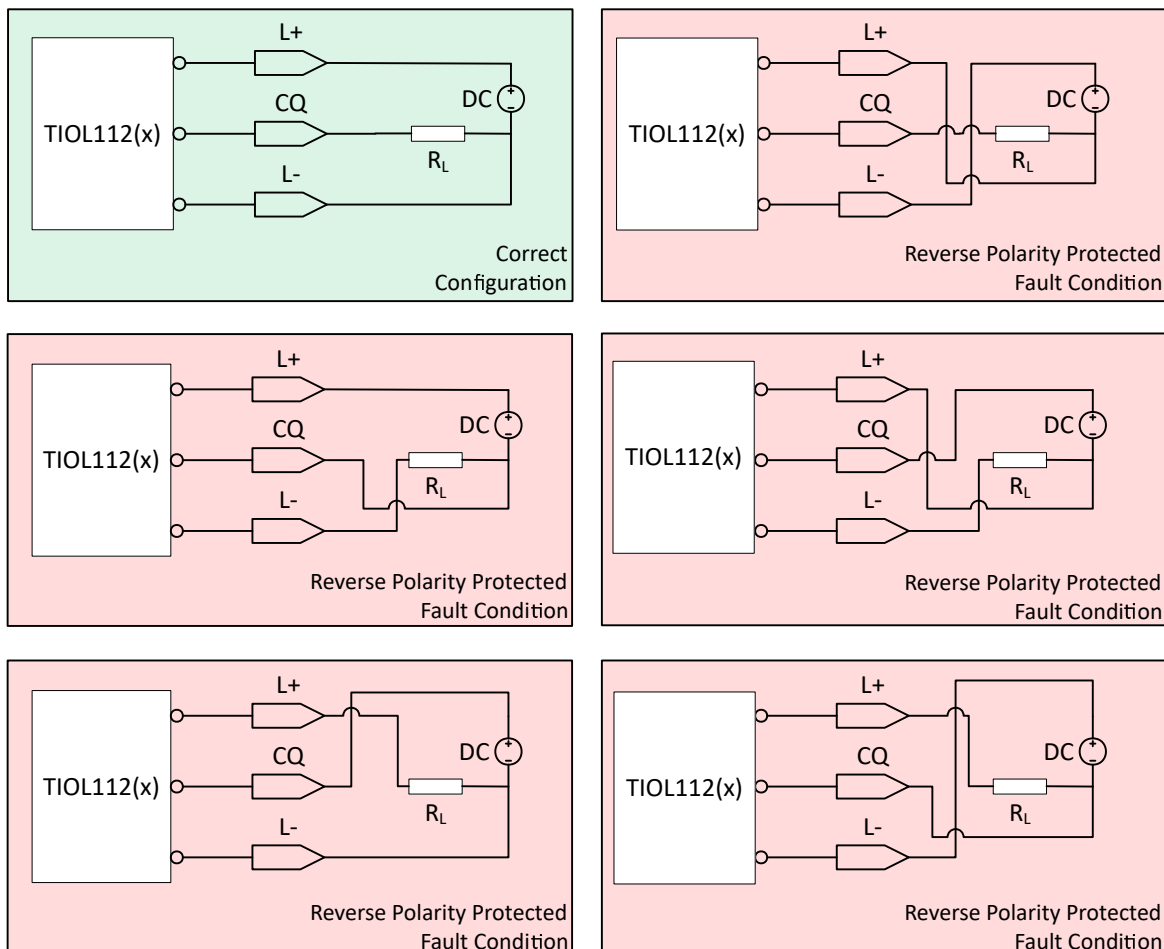
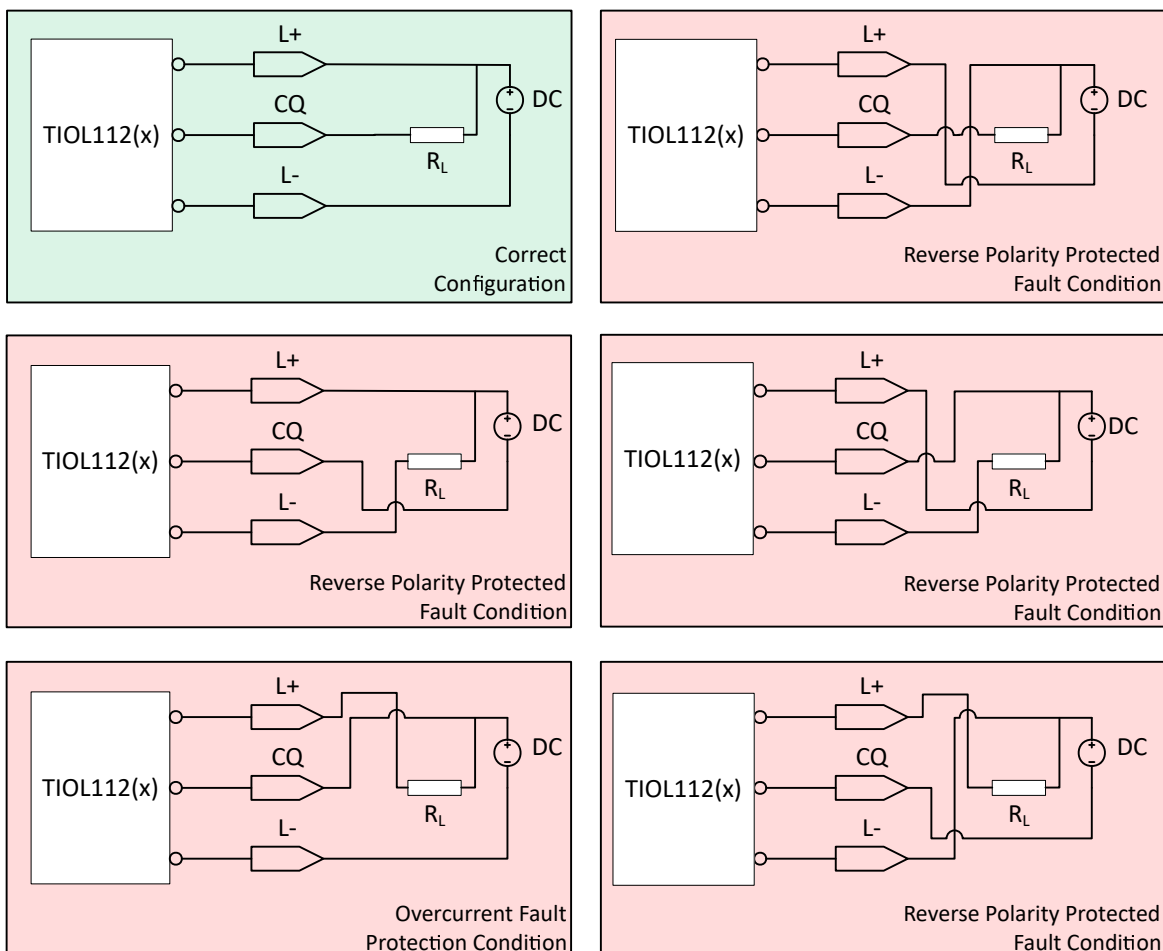


Figure 8-4. High-Side Driver Configuration

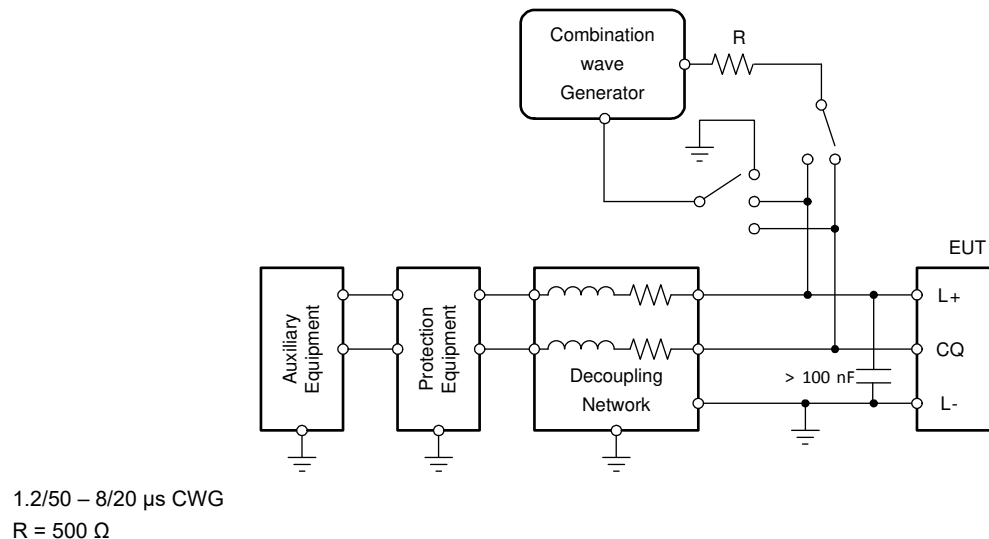


8-5. Low-Side Driver Configuration

8.3.9 Integrated Surge Protection and Transient Waveform Tolerance

The L+ and CQ pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 μ s IEC 61000-4-5 surge with a source impedance of 500 Ω . The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between L+ and L-, and 1 μ F between VCC_IN/OUT and L-.

External TVS diodes may be required for higher transient protection levels. The system designer should make sure the maximum clamping voltage of the external diodes is < 65 V at the desired current level. The device is capable of withstanding up to $\pm$ 70-V transient pulses < 100 μ s.



✎ 8-6. Surge Test Setup

8.3.10 Power Up Sequence (TIOL112)

VCC_IN and L+ domains can be powered up in any sequence. In the event of L+ is powered and VCC_IN is not, the CQ pin will remain in high impedance.

8.3.11 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the L+ voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to L+. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$, NFAULT is pulled low, and the driver (CQ) is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present). The CQ output is turned on after $t_{(UVLO)}$ delay.

8.4 Device Functional Modes

These devices can operate in three different modes.

8.4.1 NPN Configuration (N-Switch SIO Mode)

Set TX pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on CQ.

8.4.2 PNP Configuration (P-Switch SIO Mode)

Set TX pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on CQ.

8.4.3 Push-Pull, Communication Mode

Set EN pin high and toggle TX as control for realizing the function of a push-pull output on CQ. 表 8-7, 表 8-8 and 表 8-9 summarize the pin configurations to accomplish the functional modes.

表 8-7. NPN Mode

EN	TX	CQ
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 8-8. PNP Mode

EN	TX	CQ
L / Open	L	Hi-Z
H	L	P-Switch

表 8-9. Push-Pull, Communication Mode

EN	TX	CQ
L / Open	X	Hi-Z
H	H	N-Switch
H	L	P-Switch

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

When TIOL112(x) is connected to an IO-Link master through a three-wire interface (図 9-1), the master can initiate communication and exchange data with a remote node with the TIOL112(x) IO-Link transceiver acting as a complete physical layer for the communication.

9.2 Typical Application

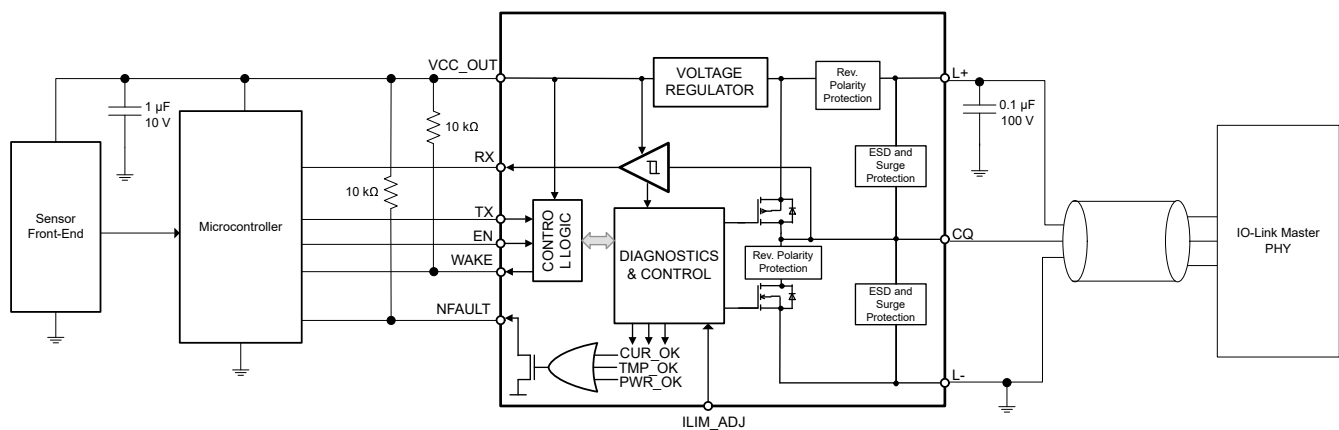


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

TIOL112 and TIOL112x IO-Link transceivers can be used to communicate using the IO-Link protocol, or as standard digital outputs to either sense or drive a wide range of sensors and loads. 表 9-1 shows recommended components for a typical system design.

表 9-1. Design Parameters

PARAMETERS	Design Requirement	TIOL112(x) Specification
Input voltage range (L+)	24 V (typ), 30 V (max)	7 V to 36 V
Output current (CQ)	200 mA	Choose 250 mA limit with $R_{SET} = 27 \text{ k}\Omega$
LDO Output voltage	5 V	Choose TIOL1125; $VCC_OUT = 5 \text{ V}$
LDO output current	5 mA	$I_{(VCC_OUT)}$: Up to 20 mA
Pull-up resistors for NFAULT and WAKE	10 kΩ	10 kΩ
L+ decoupling capacitor	0.1 μF / 100 V	0.1 μF / 100 V
LDO output capacitor	1 μF / 10 V	1 μF / 10 V
Maximum Ambient Temperature, T_A	105 °C	TIOL112 can support up to T_A of 125 °C if $T_J < T_{(SDN)}$

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- Choose driver output current limit, $I_{O(LIM)} = 250 \text{ mA}$ (allowing for current limit tolerance); $R_{SET} = 27 \text{ k}\Omega$
- The maximum voltage drop across the high-side switch at 250 mA current is $V_{DS(ON)} = 1.1 \text{ V}$.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \times I_{O(LIM)} = 1.1 \text{ V} \times 250 \text{ mA} = 275 \text{ mW} \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = (V_{L+} - V_{VCC_{OUT}}) \times I_{VCC_{OUT}} = (30 - 5) \text{ V} \times 5 \text{ mA} = 125 \text{ mW} \quad (2)$$

Total power dissipation,

$$PD = PD_{LDO} + PD_{OP} = 275 \text{ mW} + 125 \text{ mW} = 400 \text{ mW} \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of $\theta_{JA} = 45.9 \text{ }^{\circ}\text{C/W}$ (taken from the *Thermal Information table* table) to receive the difference between junction temperature, T_J , and ambient temperature, T_A :

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 400 \text{ mW} \times 45.9 \text{ }^{\circ}\text{C/W} = 18.36 \text{ }^{\circ}\text{C} \quad (4)$$

Add this value to the maximum ambient temperature of $T_A = 105^{\circ}\text{C}$ to receive the final junction temperature:

$$T_J = T_A + \Delta T = T_A + PD \times \theta_{JA} = 105 \text{ }^{\circ}\text{C} + 400 \text{ mW} \times 45.9 \text{ }^{\circ}\text{C/W} = 105 \text{ }^{\circ}\text{C} + 18.36 \text{ }^{\circ}\text{C} = 123.36 \text{ }^{\circ}\text{C} \quad (5)$$

As long as T_J is below the recommended maximum value of 150°C , no thermal shutdown will occur. However, the junction temperature is closer to T_{WRN} and thermal warning may be generated if the junction temperature rises above T_{WRN} .

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

9.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the CQ output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \times t_{SC}]}{V_{(L+)}} \quad (6)$$

To drive higher capacitive loads and avoid overcurrent condition disabling the driver, it is recommended leave ILIM_ADJ pin floating. With ILIM_ADJ floating, TIOL112(x) indicates overcurrent fault without blanking time delay (t_{SC}) but does not disable the driver. Another approach is to drive high capacitive loads with a series resistor between the CQ output and the load to avoid overcurrent condition. Capacitive loads can be connected to L- or L+.

9.2.2.3 Driving Inductive Loads

The TIOL112(x) family is capable of magnetizing and demagnetizing large inductive loads. These devices contain internal circuitry that enables fast and safe demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the CQ output is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the CQ pin. This voltage is safely clamped internally at about -15 V.

Similarly, in N-switch configuration, the load inductor L is magnetized when the CQ output is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the CQ pin. This voltage is safely clamped internally at about 15 V.

The equivalent protection circuits are shown in [Figure 9-2](#) and [Figure 9-3](#). The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(L+)}}{I_{O(LIM)}} \quad (7)$$

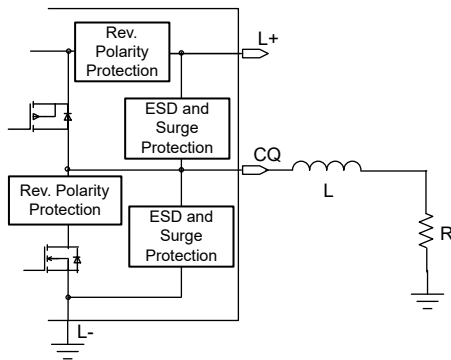


Figure 9-2. P-Switch Mode

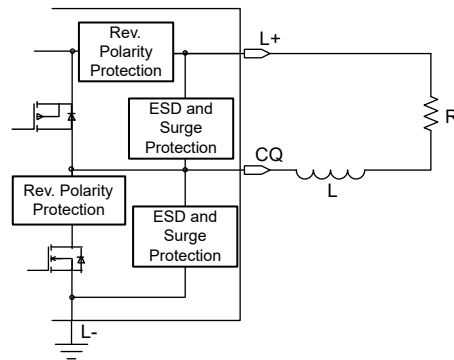
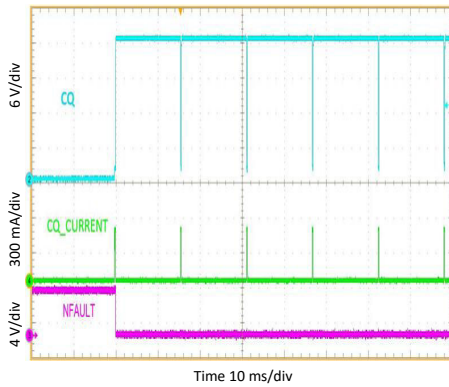
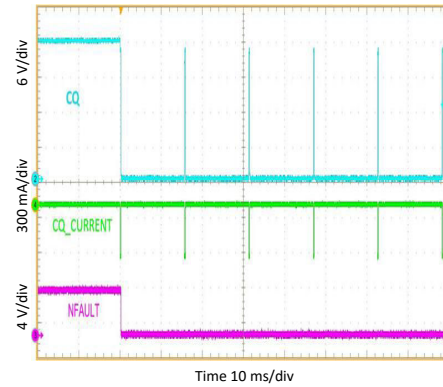


Figure 9-3. N-Switch Mode

9.2.3 Application Curves



9-4. CQ in Current Fault Auto Recovery, Low Side Mode



9-5. CQ in Current Fault Auto Recovery, High Side Mode



$L^+ = 36\text{ V}$ $L = 1.5\text{ H}$ $R_L = 360\ \Omega$ $R_{SET} = 10\text{ k}\Omega$ $T_A = 25\text{ }^\circ\text{C}$

9-6. CQ Driving Inductive Load, Low Side Mode (NPN mode)



$L^+ = 36\text{ V}$ $L = 1.5\text{ H}$ $R_L = 360\ \Omega$ $R_{SET} = 10\text{ k}\Omega$ $T_A = 25\text{ }^\circ\text{C}$

9-7. CQ Driving Inductive Load, High Side Mode (PNP mode)



NFAULT is indicated for the duration of charging and discharging of the capacitor but driver is not disabled when ILIM_ADJ is floating
 $L^+ = 24\text{ V}$ $C_L = 20\ \mu\text{F}$ $R_L = 100\ \Omega$ $R_{SET} = 1\text{ M}\Omega$ (ILIM_ADJ Floating) $T_A = 25\text{ }^\circ\text{C}$

9-8. CQ Driving Capacitive Load, Push-Pull Mode

9.3 Power Supply Recommendations

The TIOL112 and TIOL112x transceivers are designed to operate from a 24-V nominal supply at L+, which can vary by +12 V and -17 V from the nominal value to remain within the device recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

9.4 Layout

9.4.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as power ground layer for L-, layer 3 for the 24-V supply plane (L+), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to L- with maximum amount of thermal vias for best thermal performance.
- Use entire planes for L+, VCC_IN/OUT and L- to assure minimum inductance.
- The L+ terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor. The recommended minimum capacitor value is 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- The optimum placement of the capacitor is closest to the transceiver's L+ and L- terminals to reduce supply drops during large supply current loads. See [Figure 9-9](#) for a PCB layout example.
- Connect all open-drain control outputs via 10 kΩ pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and L-.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, ≥ 1-μF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

9.4.2 Layout Example

- VIA to Layer 2: Power Ground Plane (L-)
- VIA to Layer 3: 24V Supply Plane (L+)
- VIA to Layer 4: Regulated Supply Plane (VCC_IN/OUT)

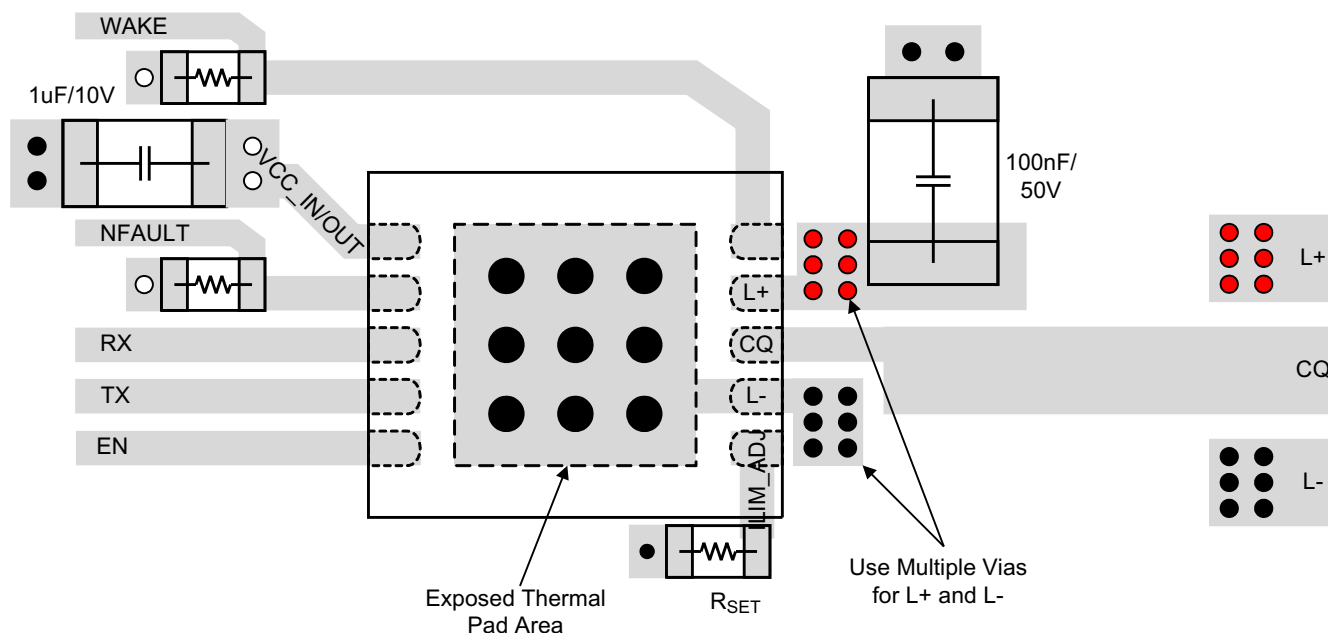


Figure 9-9. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#)を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

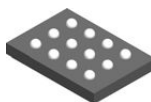
ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

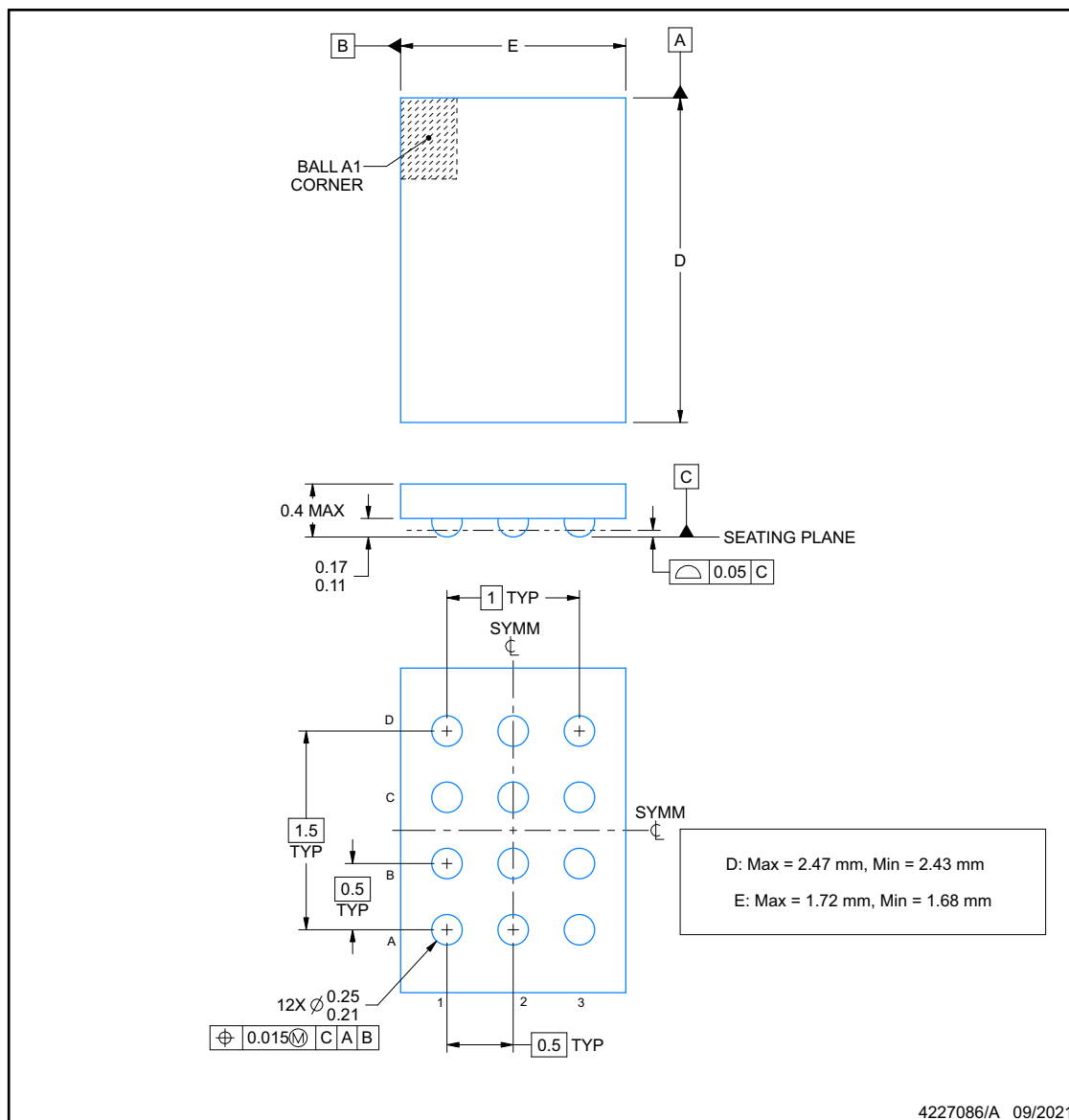


YAH0012-C01

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

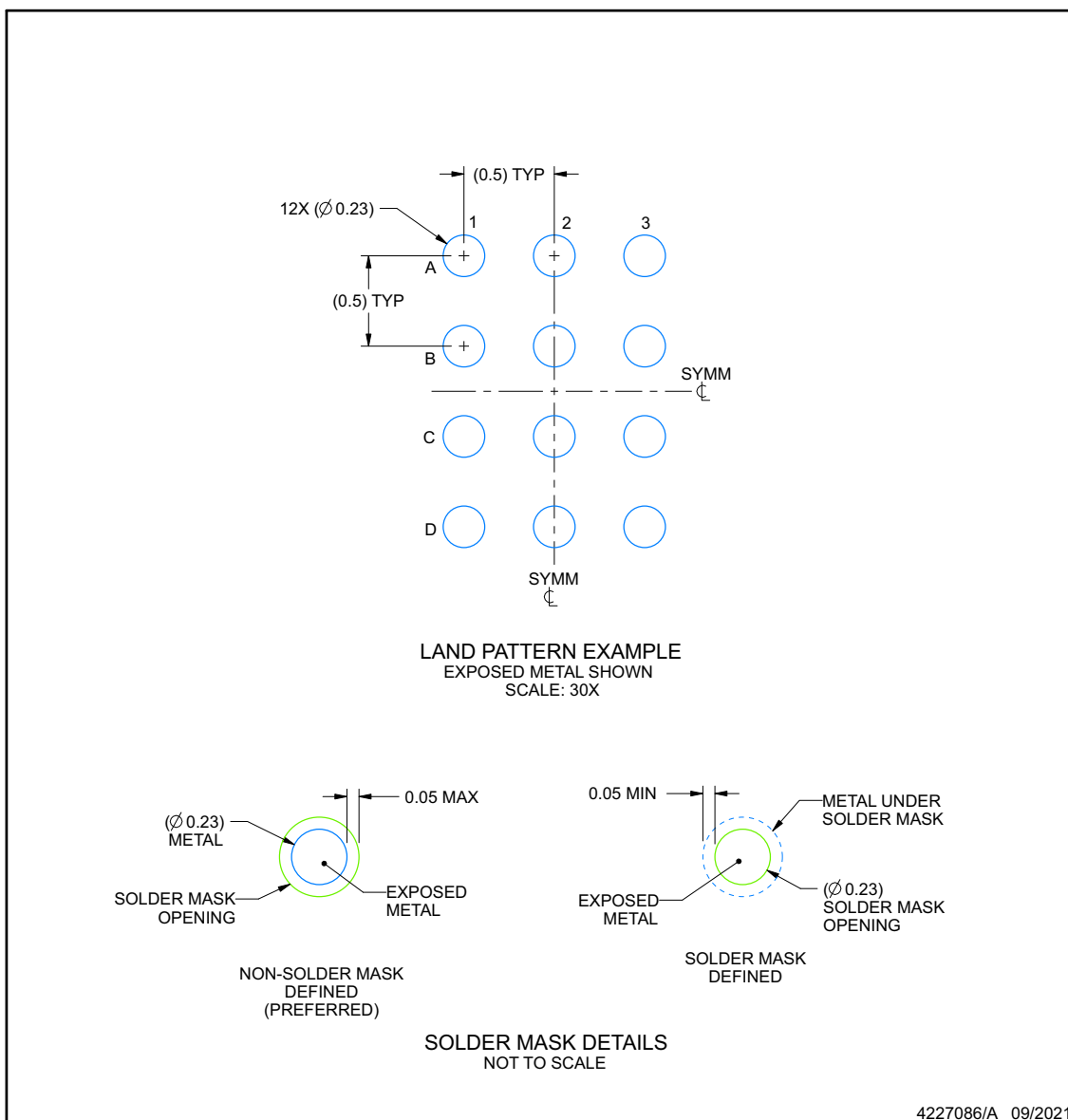
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



4227086/A 09/2021

NOTES: (continued)

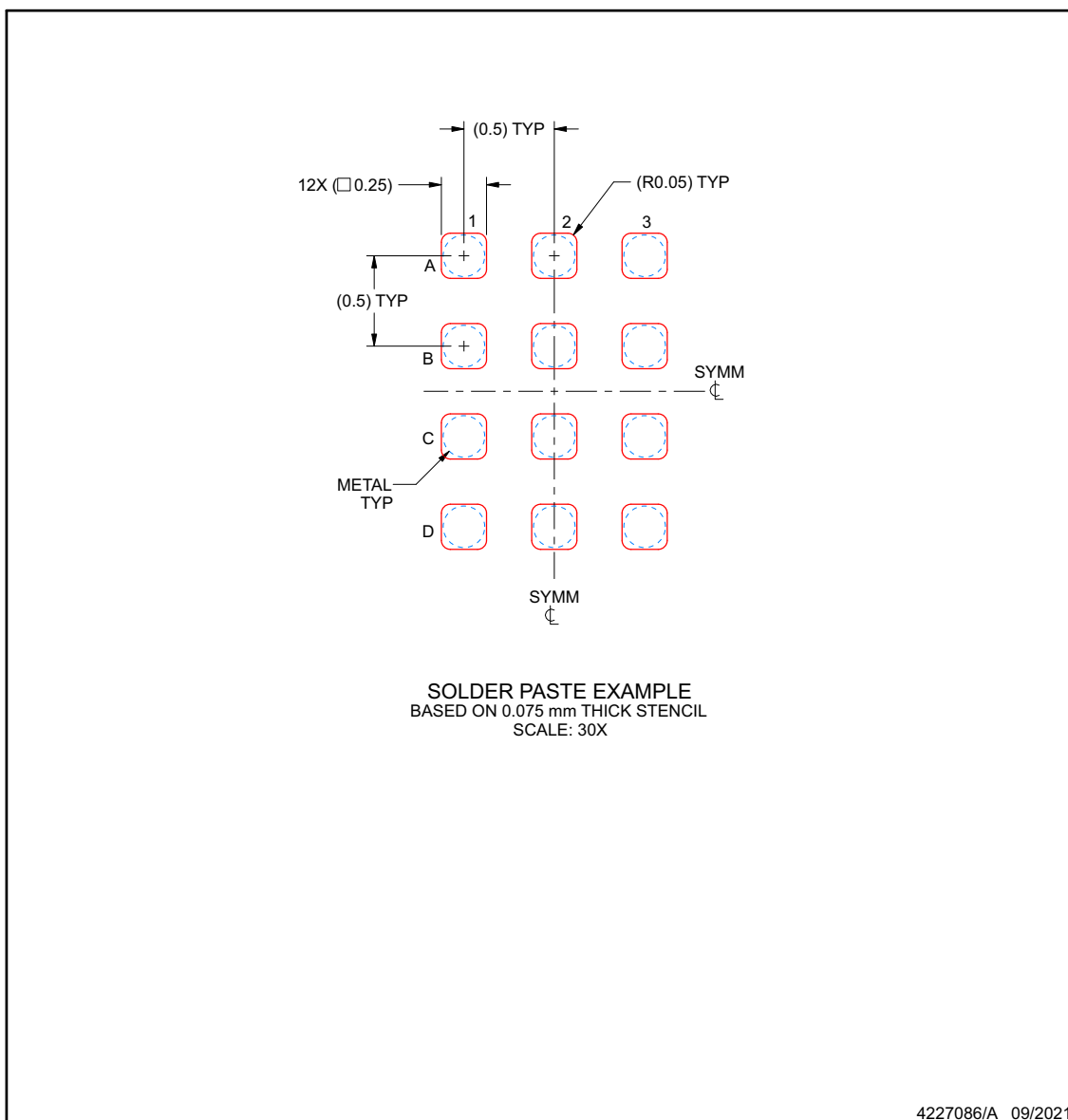
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TIOL1123DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1123
TIOL1123DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1123
TIOL1123LYAHR	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T1123L
TIOL1123LYAHR.A	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T1123L
TIOL1125DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1125
TIOL1125DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1125
TIOL112DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	112
TIOL112DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	112
TIOL112DRCRG4.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	112
TIOL112YAHR	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL112
TIOL112YAHR.A	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL112

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOL1123DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOL1123LYAHR	DSBGA	YAH	12	1500	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q1
TIOL1125DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOL112DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOL112YAHR	DSBGA	YAH	12	1500	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOL1123DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOL1123LYAHR	DSBGA	YAH	12	1500	182.0	182.0	20.0
TIOL1125DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOL112DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOL112YAHR	DSBGA	YAH	12	1500	182.0	182.0	20.0

GENERIC PACKAGE VIEW

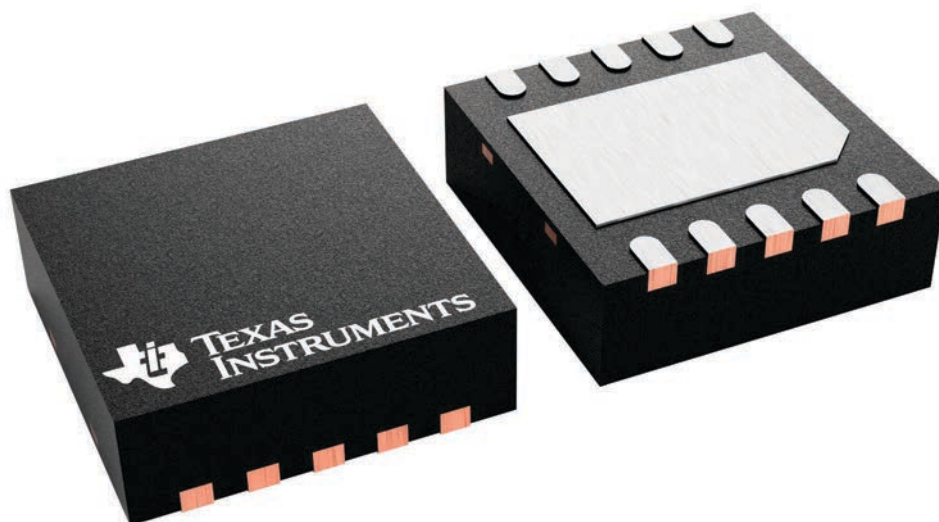
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

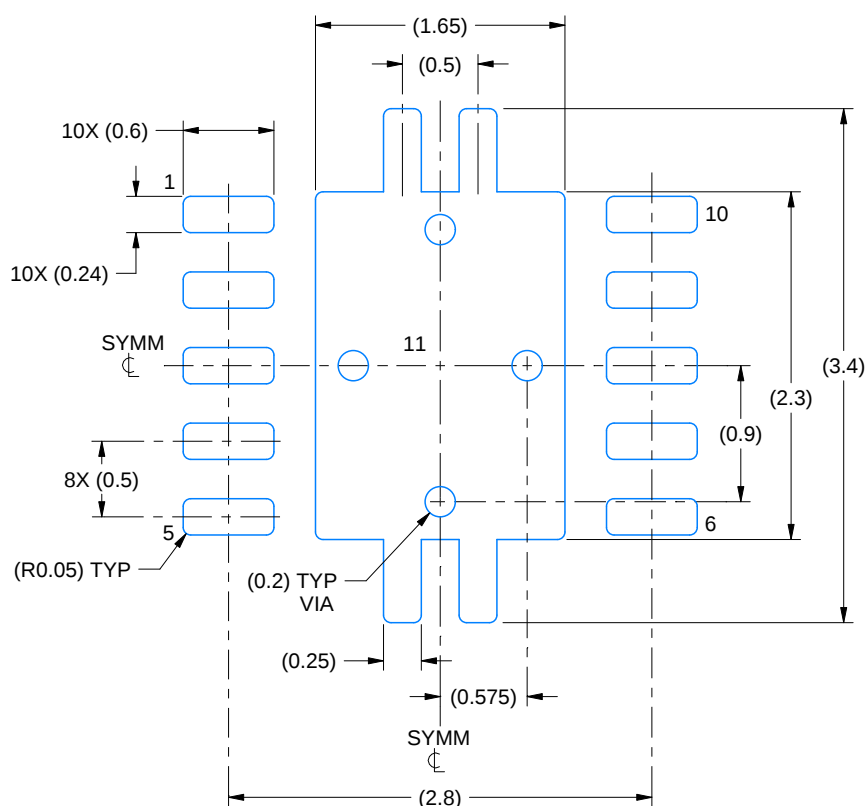


EXAMPLE BOARD LAYOUT

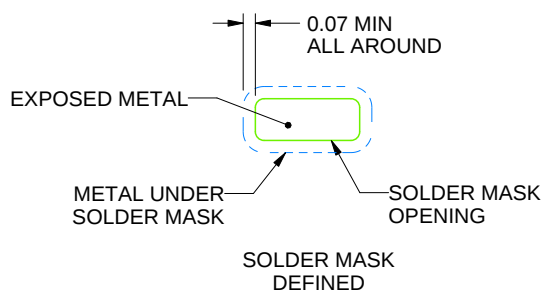
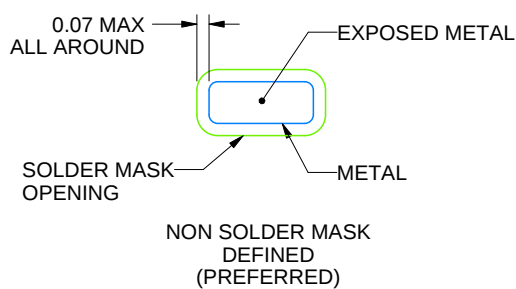
DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4226575/A 02/2021

NOTES: (continued)

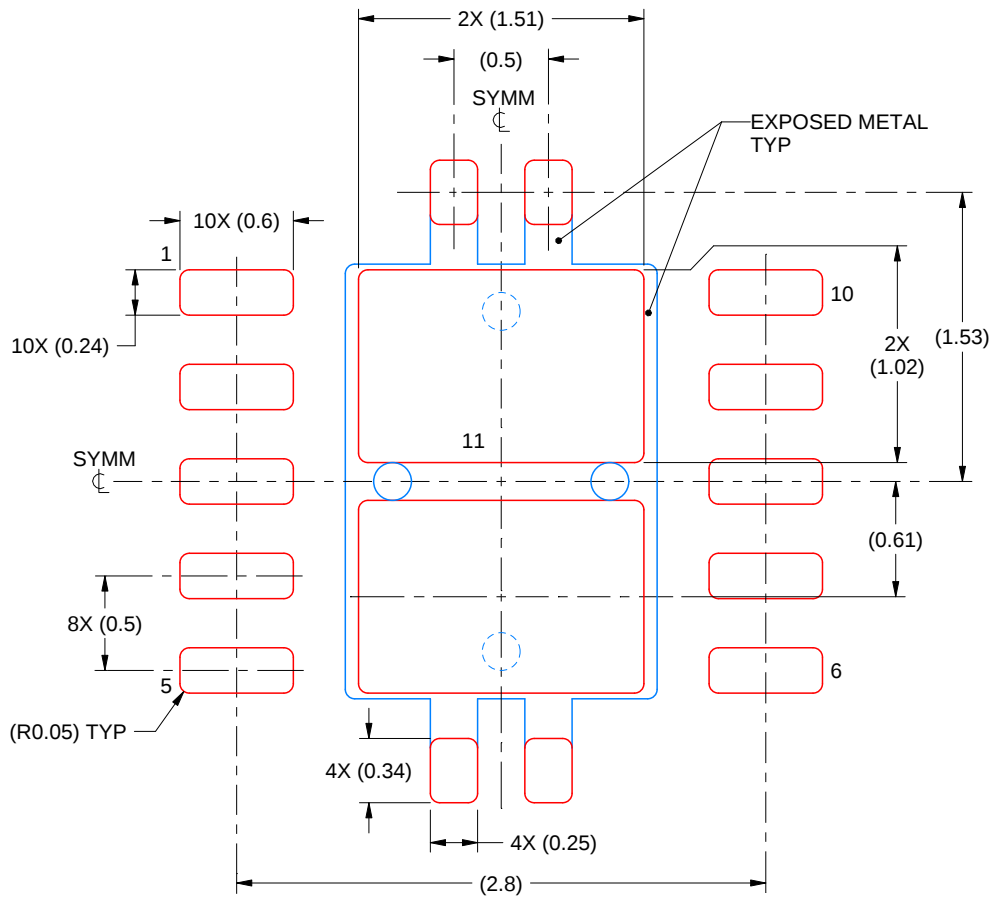
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226575/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated