DP83825I 低消費電力 10/100 Mbps イーサネット物理層トランシーバ

1 特長

- 超小型フォーム ファクタ 10/100Mbps PHY：QFN 3mm×3mm、24 ピン
- ケーブルの到達範囲：最大 150m
- 127mW 未満の超低消費電力
- MDI と MAC の終端抵抗を内蔵
- プログラム可能な省エネルギー モード
  - アクティブ スリープ
  - ディープ パワーダウン
  - Energy Efficient Ethernet (EEE) IEEE 802.3az
  - レガシー MAC での EEE サポート
  - Wake-on-LAN (WoL)
- 電圧モード ライン ドライバ
- MAC インターフェイス：RMII (マスタおよびスレーブ モード)
- 3.3V の単一電源電圧
- I/O 電圧：1.8V および 3.3V
- リピータ：アンマネージド モードでの RMII 双方向モード
- 構成およびステータス用 MDC/MDIO インターフェイス
- 高速なリンクドロップ モード
- 診断ツール：ケーブル診断、内蔵自己テスト (BIST)、ループバック モード
- プログラマブルなハードウェア割り込みピン
- 動作温度範囲：–40℃ ～ 85℃
- IEEE 802.3 100BASE-TX および 10BASE-Te 仕様に準拠

2 アプリケーション

- ビルディング オートメーション：IP カメラ、HMI
- モーター ドライブ
- POS システム
- ファクトリ オートメーション

3 概要

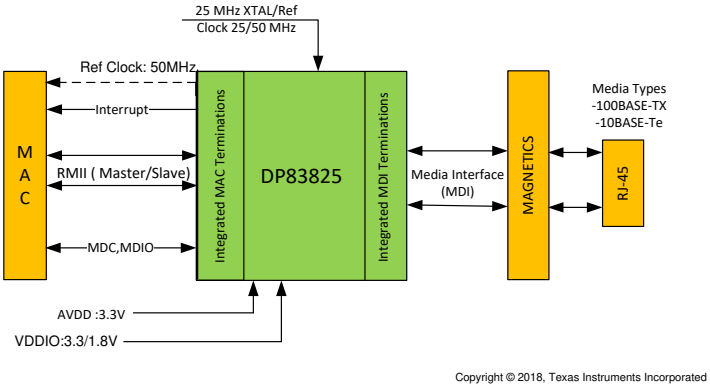
DP83825I は、10BASE-Te および 100BASE-TX イーサネット プロトコルをサポートする PMD サブレイヤを内蔵した超小型フォーム ファクタ、超低消費電力のイーサネット物理層 (PHY) トランシーバです。この PHY は、CAT5e ケーブルで最大 150m の伝送距離をサポートします。DP83825I は、外付けトランスを介してツイスト ペア メディアに直接接続できます。

DP83825I は、Energy Efficient Ethernet (EEE)、Wake-on-LAN (WoL)、MAC 絶縁にも対応しているため、システムの消費電力をさらに低減できます。MAC 上での EEE 信号処理をサポートしていないレガシー MAC の場合でも、レジスタ構成を使って Energy Efficient モードを有効にできます。DP83825I はアンマネージド リピータ モードで動作できます。このモードでは、DP83825I はレジスタ設定なしでリピータとして動作します。DP83825I にはケーブル診断ツール、組み込みの自己テスト、ループバック機能が内蔵されており、開発やデバッグが容易です。

デバイス ファミリ情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)	属性
DP83826E	VQFN (32)	5.00mm × 5.00mm	最小のレイテンシ、一般的なピン配置
DP83825I	WQFN (24)	3.00mm × 3.00mm	小さなサイズ、最適化されたコスト
DP83822HF/IF/H/I	VQFN (32)	5.00mm × 5.00mm	広い温度範囲、ファイバー、RGMII のサポート

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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DP83825I アプリケーション図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

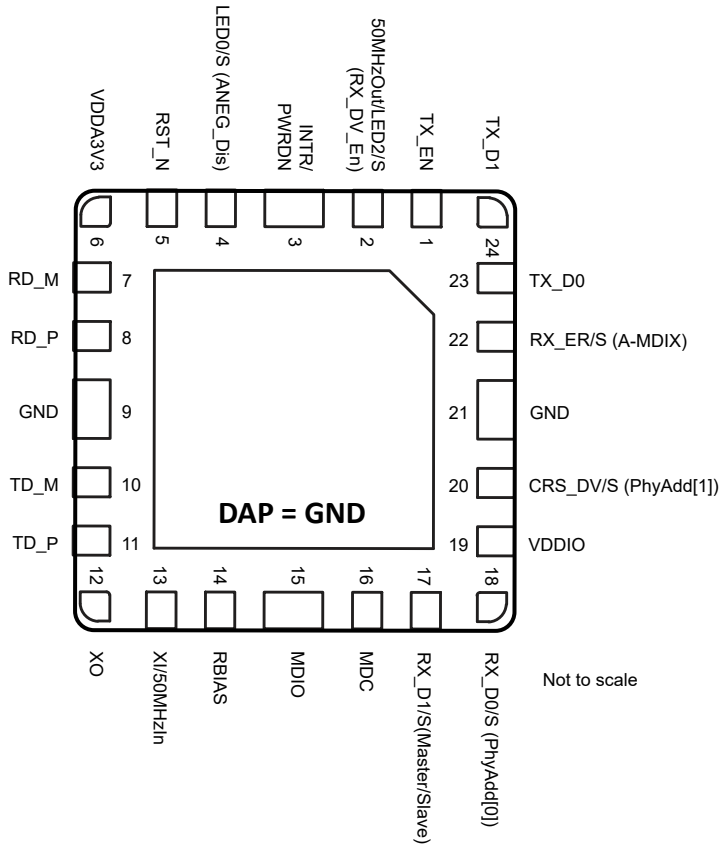

図 4-1. DP83825 RMQ Package 24-Pin QFN Top View

DP83825I Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
TX_EN	1	Reset: I, PD Active: I, PD	RMII Transmit Enable: TX_EN is active high signal and is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D [1:0].
50MHzOut/LED2	2	Reset: I, PD, S Active: O	RMII Master Mode: 50MHz Clock Out(default). RMII Slave Mode: LED_2(default). This pin can be configured as GPIO using register configuration.
INTR/PWRDN	3	Reset: I, PU Active: I/O, PU	Interrupt / Power Down(default): The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power-down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup (9.5kΩ). Some applications can require an external pullup resistor.
LED0	4	Reset: I, PD, S Active: O	LED0 : Activity Indication LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when Link is good. The LED blinks when the transmitter or receiver is active. This pin can also act as GPIO through register configuration. **This pin is at 3.3V always and not linked to voltage supplied to VDDIO pin. This is to avoid external components when operating PHY at VDDIO 1.8V.**

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RST_N	5	Reset: I, PU Active: I, PU	RST_N: This pin is an active low reset input. Asserting this pin low for at least 25µs forces a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value. **This pin is at 3.3V always and not linked to voltage supplied to VDDIO pin. This is to avoid external components when operating PHY at VDDIO 1.8V.**
VDDA3V3	6	Power	Input Analog Supply: 3.3V. For decoupling capacitor requirements, refer to the *セクション 7.3* section.
RD_M	7	A	Differential Receive Input (PMD): These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX specific signaling mode
RD_P	8	A	
GND	9	GND	Ground: Connect to Ground
TD_M	10	A	Differential Transmit Output (PMD): These differential outputs are configured to either 10BASE-Te, 100BASE-TX signaling mode based on configuration chosen for PHY.
TD_P	11	A	
XO	12	A	Crystal Output: Reference Clock output. XO pin is used for crystal only. This pin can be left floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	13	A	Crystal / Oscillator Input Clock RMII Master mode: 25MHz ±50ppm-tolerance crystal or oscillator clock RMII Slave mode: 50MHz ±50ppm-tolerance CMOS-level oscillator clock
RBIAS	14	A	This pin needs a biasing resistor. Connect a 6.49kΩ ±1% tolerance resistor between RBIAS pin and ground.
MDIO	15	Reset: I, PU-10kΩ Active: I/O, PU-10kΩ	Management Data I/O: Bidirectional management data signal that can be source by the management station or the PHY. This pin has internal pullup of 10kΩ. External pullup of up to 2.2kΩ can be added if needed
MDC	16	Reset: I, PD Active: I, PD	Management Data Clock: Synchronous clock to the MDIO serial management input/output data. This clock can be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 24MHz. There is no minimum clock rate.
RX_D1	17	Reset: I, PD, S Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. These symbols contain valid data when RX_DV is asserted.
RX_D0	18	Reset: I, PD, S Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. These symbols contain valid data when RX_DV is asserted.
VDDIO	19	Power	I/O Supply : 3.3V/1.8V. For decoupling capacitor requirements, refer to the *セクション 7* section.
CRS_DV	20	Reset: I, PD, S Active: O	Carrier Sense / Receive Data Valid: This pin combines the RMII Carrier and Receive Data Valid indications.
GND	21	GND	Ground pin
RX_ER	22	Reset: I, PD, S Active: O	RMII Receive Error: This pin indicates an error symbol has been detected within a received packet in RMII mode. RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required by the MAC in RMII mode, because the PHY automatically corrupts data on a receive error.
TX_D0	23	Reset: I, PD Active: I, PD	RMII Transmit Data: TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock.
TX_D1	24	Reset: I, PD Active: I, PD	

(1) The pin functions are defined below:
Type I: Input
Type O: Output
Type I/O: Input/Output
Type PD or PU: Internal Pulldown or Pullup
Type S: Strap Configuration Pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Analog supply voltage	AVDD3V3	–0.3	4	V
IO supply voltage	VDDIO3V3	–0.3	4	V
	VDDIO1V8	–0.3	2.1	V
Junction Temperature	Tj		105	°C
Storage Temperature	Tstg	–65	150	°C
MDI pins	TD–, TD+, RD–, RD+	-0.3	4	V
MAC interface pins		–0.3	4	V
SMI interface pins		–0.3	4	V
XI		–0.3	4	V
Reset		–0.3	4	V

(1) Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

5.2 ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
Human-body model (HBM), per ANSI/ ESDA/JEDEC JS-001(1)	All Pins (except MDI)	±1.5		kV
	MDI (Media Dependent Interface) pins	±5		kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500V HBM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD3V3	3	3.3	3.6	V
IO supply voltage	VDDIO3V3	3	3.3	3.6	V
	VDDIO1V8	1.62	1.8	1.98	V
Operating Free Air Temperature (DP83825I)	Ta	–40	25	85	C
Pins	TX_EN, TX_D0, TX_D1, RX_D0, RX_D1, RX_DV, RX_ER, MDIO, MDC, INT/PWDN, LED2	VDDIO-10%	VDDIO	VDDIO+10 %	V
Pins	XI Osclliator Input	VDDIO-10%	VDDIO	VDDIO+10 %	V
Pins	LED0, RST_N	AVDD3V3-1 0%	AVDD3V3	AVDD3V3+1 0%	V

5.4 Thermal Information

(1)

THERMAL METRIC(1)			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	°C/W

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(1)

THERMAL METRIC(1)			UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.3	°C/W
Y_{JT}	Junction-to-top characterization parameter	28.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	14.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx CONFORMANCE (100BaseTx)						
	Differential Output Voltage	100 Base Tx idle transmission		1.0		V
IEEE Tx CONFORMANCE (10BaseTe)						
	Differential Voltage	10BaseTe data transmission		1.75		V
POWER CONSUMPTION (Power Optimised Mode)						
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 50%		37.5		mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 50%		37.5		mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 50%		7.5		mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 50%		3.5		mA
I(VDDIO=1V8)	RMII Master (100BaseTx)	Traffic = 50%		4.5		mA
I(VDDIO=1V8)	RMII Slave (100BaseTx)	Traffic = 50%		1.6		mA
POWER CONSUMPTION (Cable Reach Optimised Mode)						
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 50%		41		mA
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 100%		41	50	mA
I(AVDD3V3)	RMII Master (10BaseTe)	Traffic = 50%		28		mA
I(AVDD3V3)	RMII Master (10BaseTe)	Traffic = 100%		32	40	mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 50%		41	50	mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 100%		41	50	mA
I(AVDD3V3)	RMII Slave (10BaseTe)	Traffic = 50%		28		mA
I(AVDD3V3)	RMII Slave (10BaseTe)	Traffic = 100%		32	40	mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 50%		7.5		mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 100%		10	14	mA
I(VDDIO=3V3)	RMII Master (10BaseTe)	Traffic = 50%		6.5		mA
I(VDDIO=3V3)	RMII Master (10BaseTe)	Traffic = 100%		7.5	12	mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 50%		3.5		mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 100%		5	8	mA
I(VDDIO=3V3)	RMII Slave (10BaseTe)	Traffic = 50%		2.5	6	mA
I(VDDIO=3V3)	RMII Slave (10BaseTe)	Traffic = 100%		2.5	6	mA

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over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO =1V8)	RMII Master (100BaseTx)	Traffic = 50%		4	14	mA
I(VDDIO =1V8)	RMII Master (100BaseTx)	Traffic = 100%		5.5	14	mA
I(VDDIO =1V8)	RMII Master (10BaseTe)	Traffic = 50%		4		mA
I(VDDIO =1V8)	RMII Master (10BaseTe)	Traffic = 100%		4	14	mA
I(VDDIO =1V8)	RMII Slave (100BaseTx)	Traffic = 50%		1.5		mA
I(VDDIO =1V8)	RMII Slave (100BaseTx)	Traffic = 100%		2.5	6	mA
I(VDDIO =1V8)	RMII Slave (10BaseTe)	Traffic = 50%		1		mA
I(VDDIO =1V8)	RMII Slave (10BaseTe)	Traffic = 100%		1	6	mA
POWER CONSUMPTION (Low Power Modes)						
I(AVDD= 3V3)	100 BaseTx EEE mode	100 BaseTx link in EEE mode with LPIs ON		15.5		mA
	Deep Power Down			3.5		mA
	IEEE Power Down			4		mA
	Active Sleep			11		mA
	Active but not Link			37		mA
	RESET			5.5		mA
I(VDDIO =3V3)	100 BaseTx EEE mode			2		mA
	Deep Power Down			2.5		mA
	IEEE Power Down			2		mA
	Active Sleep			5		mA
	Active but not Link			5		mA
	RESET			2.5		mA
I(VDDIO =1V8)	100 BaseTx EEE mode			2		mA
	Deep Power Down			1.5		mA
	IEEE Power Down			1.5		mA
	Active Sleep			3		mA
	Active but not Link			3		mA
	RESET			1.5		mA
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{IH_3v3}	High Level Bootstrap Threshold : 3V3		1.3			V
V_{IL_3v3}	Low Level Bootstrap Threshold : 3V3				0.6	V
V_{IH_1v8}	High Level Bootstrap Threshold:1V8		1.3			V
V_{IL_1v8}	Low Level Bootstrap Threshold :1V8				0.6	V
Crystal oscillator						
	Load Capacitance			15	30	pF
IO						

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over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3V3	V_{IH} High Level Input Voltage	VDDIO= 3V3+/- 10%	1.7			V
	V_{IL} Low Level Input Voltage	VDDIO= 3V3+/- 10%			0.8	V
	V_{OH} High Level Output Voltage	I_{oH}= -2mA, VDDIO=3V3 +/-10%	2.4			V
	V_{OL}Low Level Output Voltage	I_{oL}= 2mA, VDDIO=3V3 +/- 10%			0.4	V
1V8	V_{IH} High Level Input Voltage	VDDIO= 1V8+/- 10%	0.65*VDDIO			V
	V_{IL} Low Level Input Voltage	VDDIO= 1V8+/- 10%			0.35*VDDIO	V
	V_{OH} High Level Output Voltage	I_{oH}= -2mA, VDDIO=1V8 +/-10%	VDDIO-0.45			V
	V_{OL}Low Level Output Voltage	I_{oL}= 2mA, VDDIO=1V8 +/- 10%			0.45	V
	Iih (VIN=VCC)	T_A=-40 TO 85C, VIN=VDDIO			15	uA
	Iil (VIN=GND)	T_A=-40 TO 85C, VIN=GND			15	uA
	Iozh	Tri State Output High Current	-15		15	uA
	Iozl	Tri State Output Low Current	-15		15	uA
	Cin (Input Capacitance)			5		pF
	R Pull Down		8	10	13	Kohms
	R Pull UP		8	10	13	Kohms
	XI input osc clock pk-pk			VDDIO		V
	XI input osc clock common mode			VDDIO/2		V

(1) Specified by production test, characterization or design

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5.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
POWER-UP TIMING					
T1	Voltage Ramp Duration (0 to 100% VDDIO)(1)	0.5		40	ms
T2	Supply Sequencing: VDDIO shall ramp first and then AVDD	0		200	ms
T3	Voltage Ramp Duration (0 to 100% of AVDD)	0.5		40	ms
T4	POR release time / Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access			50	ms
T5	Powerup to FLP		1500		ms
	Pedestal Voltage on AVDD, VDDIO before Power Ramp			0.3	V
	All inputs must not be driven low or high until AVDD and VDDIO are stable				
RESET TIMING					
T1	RESET PULSE Width: Miminum Reset pulse width to be able to reset (w/o debouncing caps)	25			us
T2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access			2	ms
T3	Reset to FLP		1500		ms
	Reset to 100M signaling (strapped mode)		0.5		ms
	Reset to RMII Master clock		0.2		ms
100M EEE TIMING					
	Sleep time (Ts)		210		us
	Quiet time (Tq)		20		ms
	Refresh time (Tr)		200		us
	Wake time (Tw_sys_tx)		36		us
RMII TRANSMIT TIMING					
T1	RMII Master Clock Period		20		ns
	RMII Master Clock Duty Cycle	35		65	%
T2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock	4			ns
T3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock	2			ns
RMII RECEIVE TIMING					
T1	Input Reference Clock Period		20		ns
	Reference Clock Duty Cycle	35		65	%
T2	RX_D[1:0], RX_ER, RX_DV Hold from XI Clock rising	2			ns
SMI TIMING					
T1	MDC to MDIO (Output) Delay Time	0		10	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	20	MHz
OUTPUT CLOCK TIMING (50M RMII Master Clock)					
	Frequency (PPM)	-50		50	ppm
	Duty Cycle	35		65	%
	Rise time			4000	ps
	Fall Time			4000	ps
	Jitter (Long Term)			450	ps
	RefCLK to clock out delay with multiple resets			40	ns
INPUT CLOCK tolerance					

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PARAMETER		MIN	NOM	MAX	UNIT
25MHz	Frequency Tolerance	-50		50	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (Accumulated over 100,000 cycles)			1.75	ns
	Duty Cycle	40		60	%
	input phase noise at 1KHz			-98	dBc/Hz
	input phase noise at 10KHz			-113	dBc/Hz
	input phase noise at 100KHz			-113	dBc/Hz
	input phase noise at 1MHz			-113	dBc/Hz
	input phase noise at 10MHz			-113	dBc/Hz
50MHz	Frequency Tolerance	-50		50	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (Accumulated over 100,000 cycles)			1.75	ns
	Duty Cycle	40		60	%
	input phase noise at 1KHz			-87	dBc/Hz
	input phase noise at 10KHz			-107	dBc/Hz
	input phase noise at 100KHz			-107	dBc/Hz
	input phase noise at 1MHz			-107	dBc/Hz
	input phase noise at 10MHz			-107	dBc/Hz
LATENCY TIMING					
Tx	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI (100M)		105		ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI (100M)		105		ns
	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI (10M)		1350		ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI (10M)		1300		ns
Rx	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV (100M)		350		ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV (100M)		325		ns
	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV (10M)		2150		ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV (10M)		2150		ns

(1) Clock shall be available at power ramp. If Clock is provided after power ramp, external Reset of PHY is needed once clock is available

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5.7 Timing Diagrams

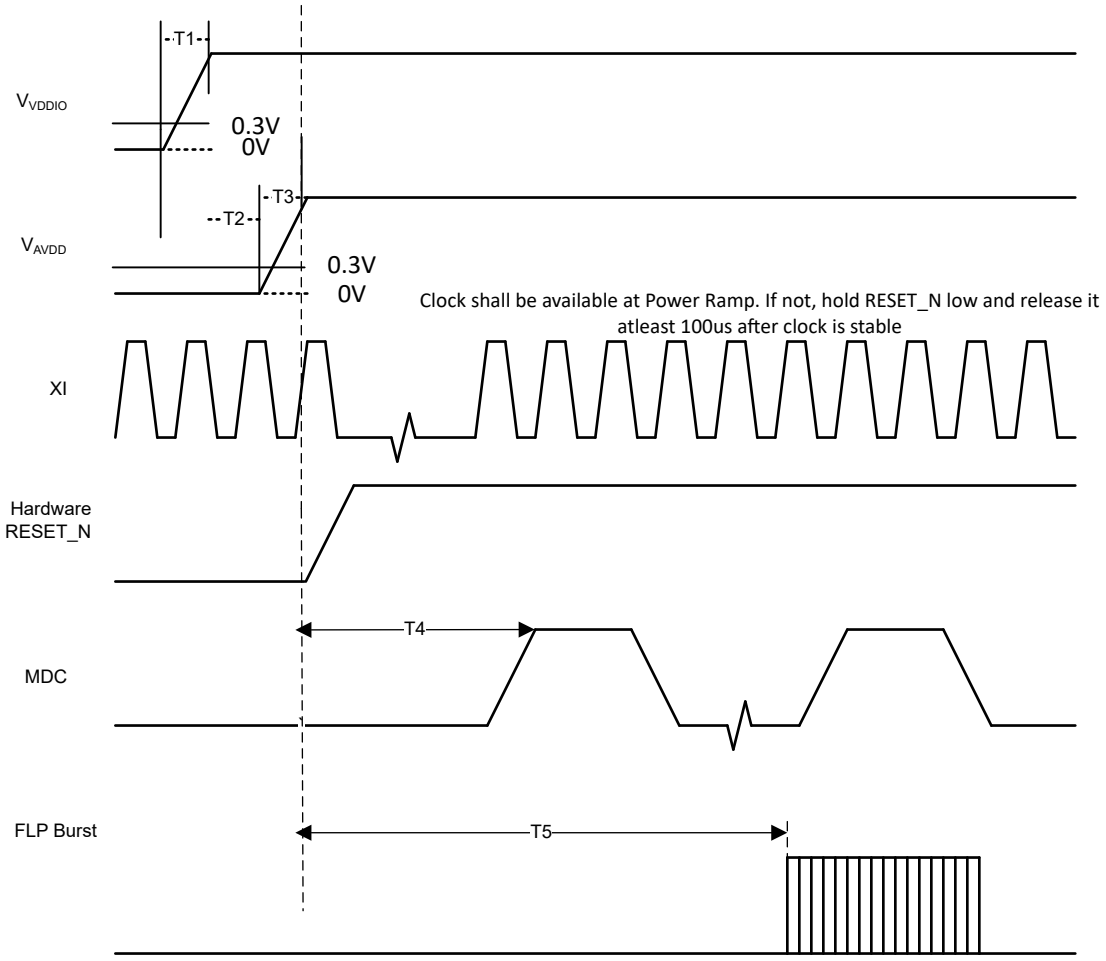

図 5-1. Power-Up Timing

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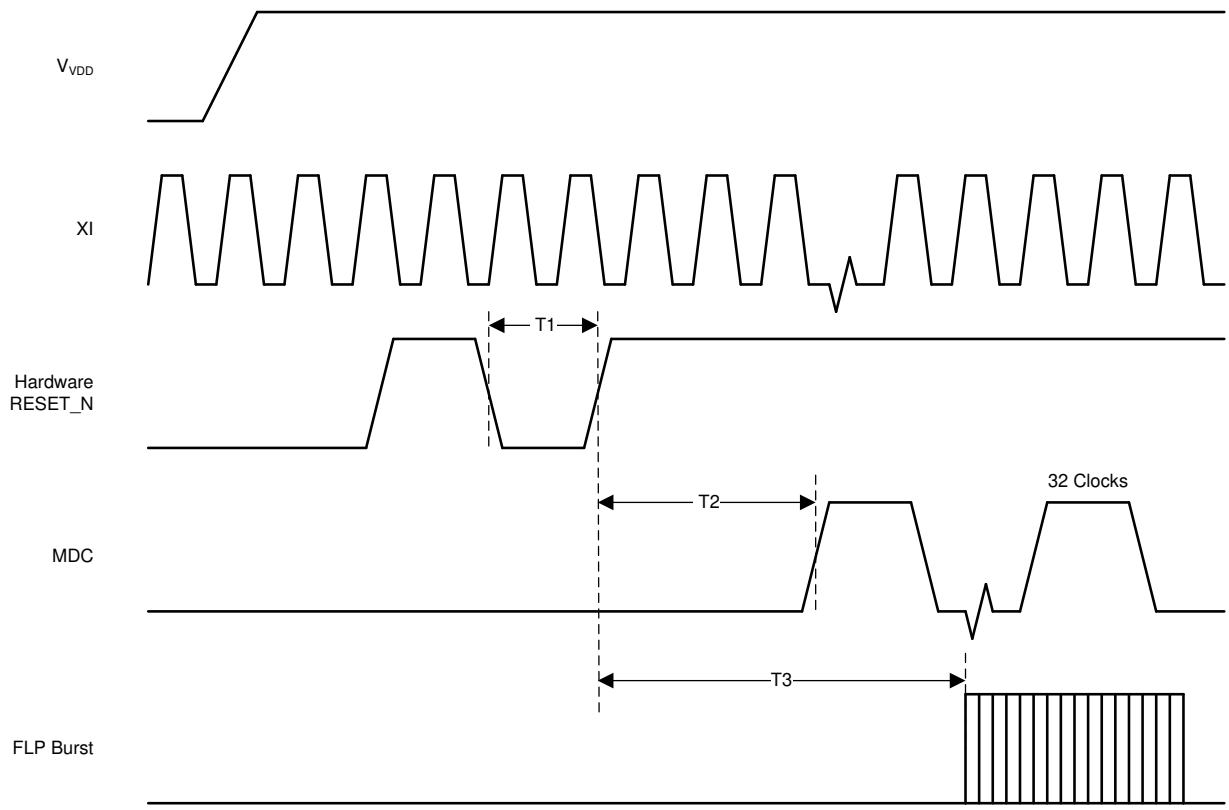

図 5-2. Reset Timing

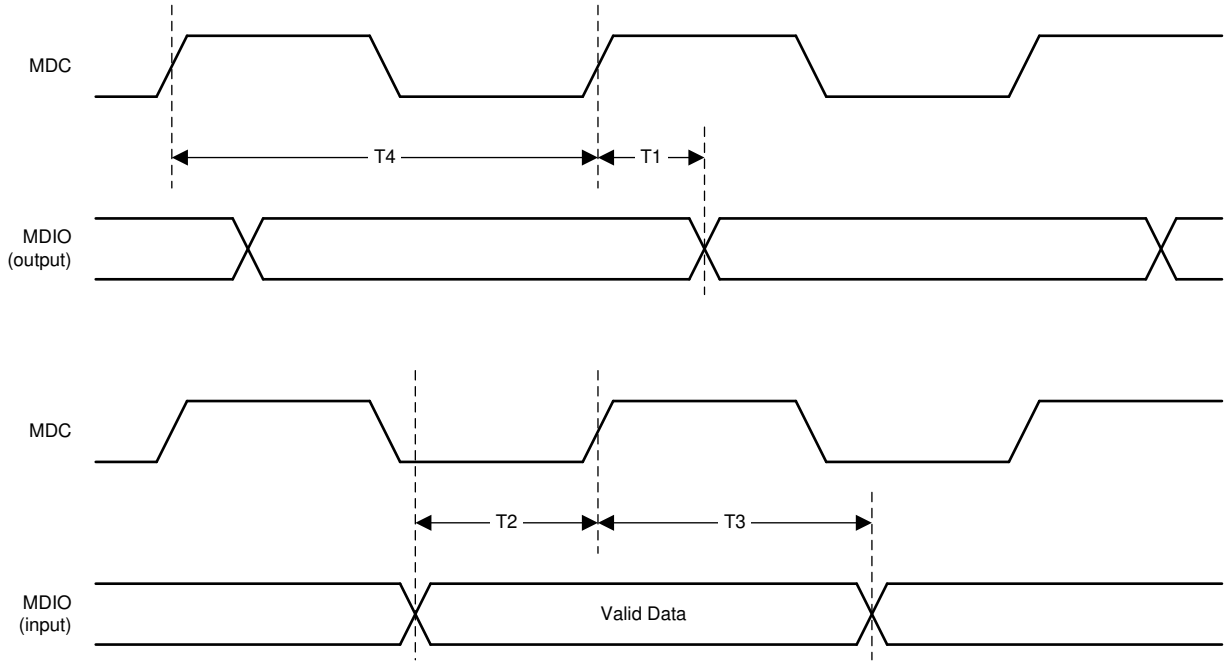

図 5-3. Serial Management Timing

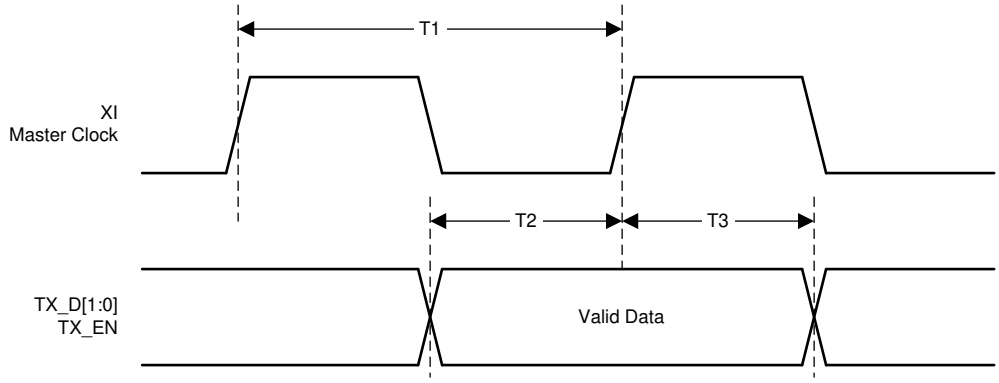

図 5-4. RMII Transmit Timing

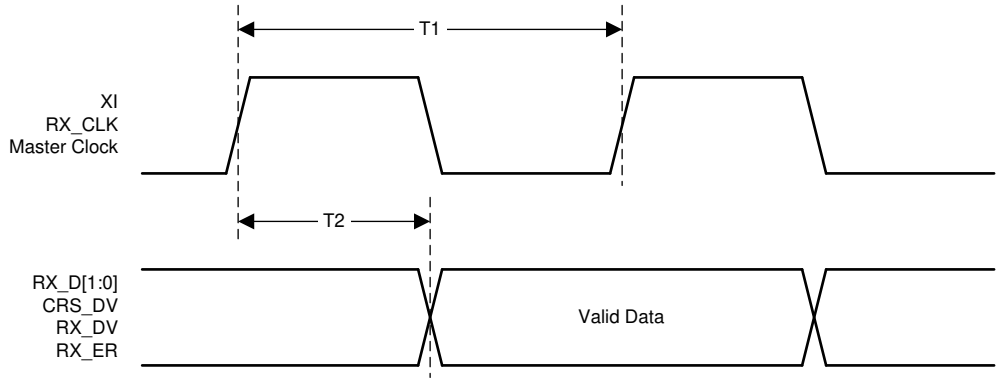

図 5-5. RMII Receive Timing

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5.8 Typical Characteristics

This section describes the DP83825 Drive characteristics for VDDIO 3.3V and 1.8V.

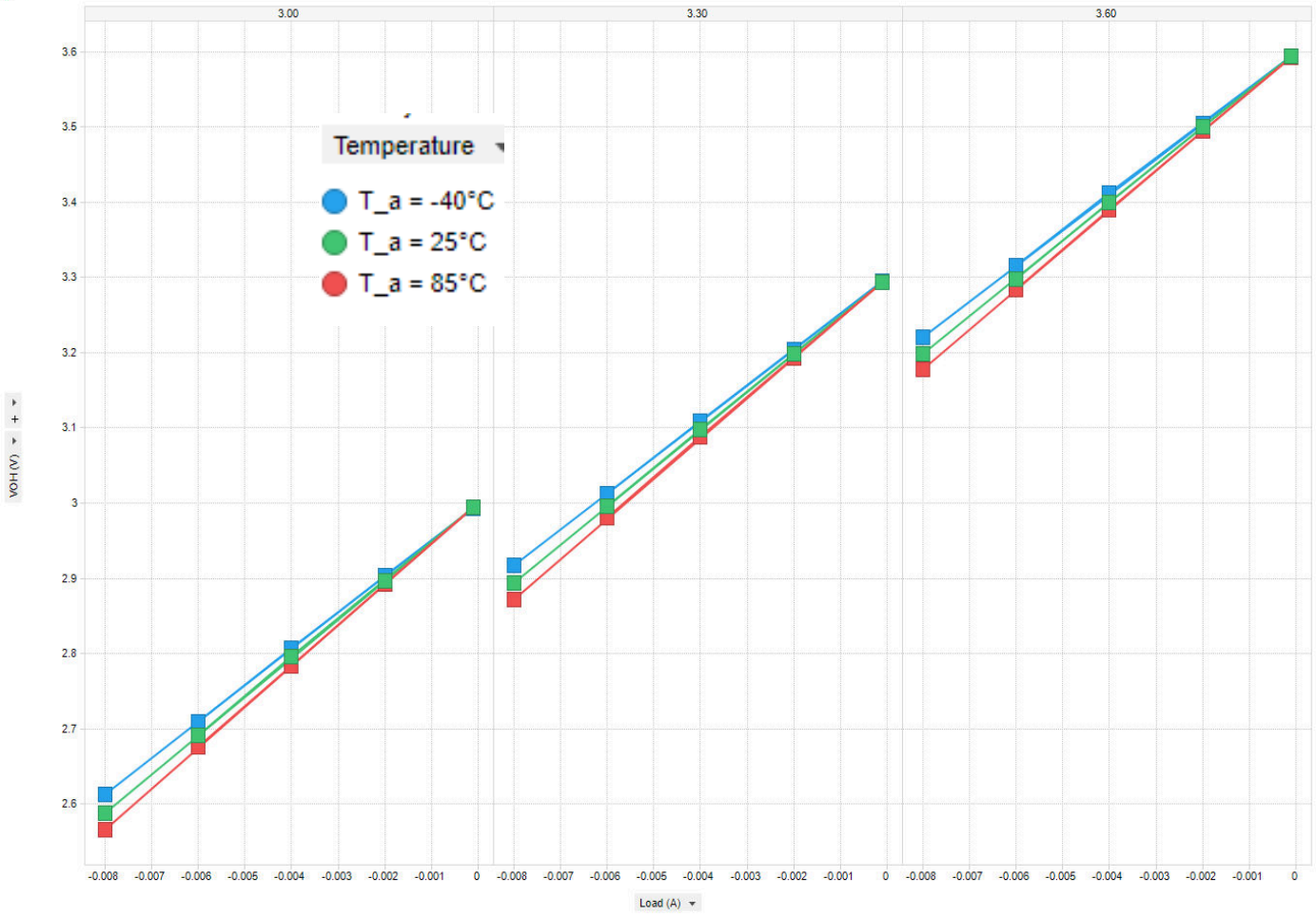

図 5-6. LED_0, LED_2, CLKOUT VOH 3.3V

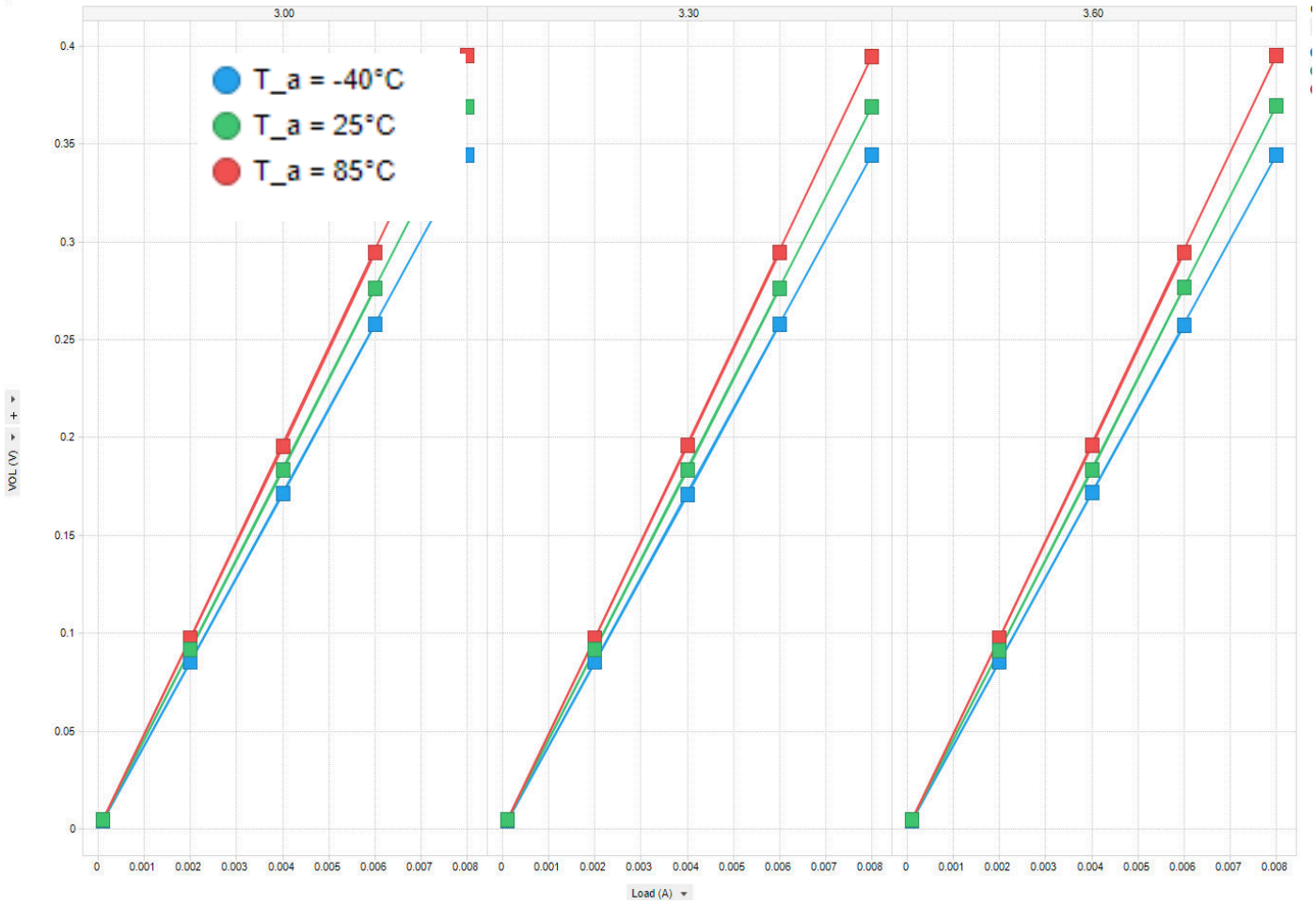

図 5-7. LED_0, LED_2, CLKOUT VOL 3.3V

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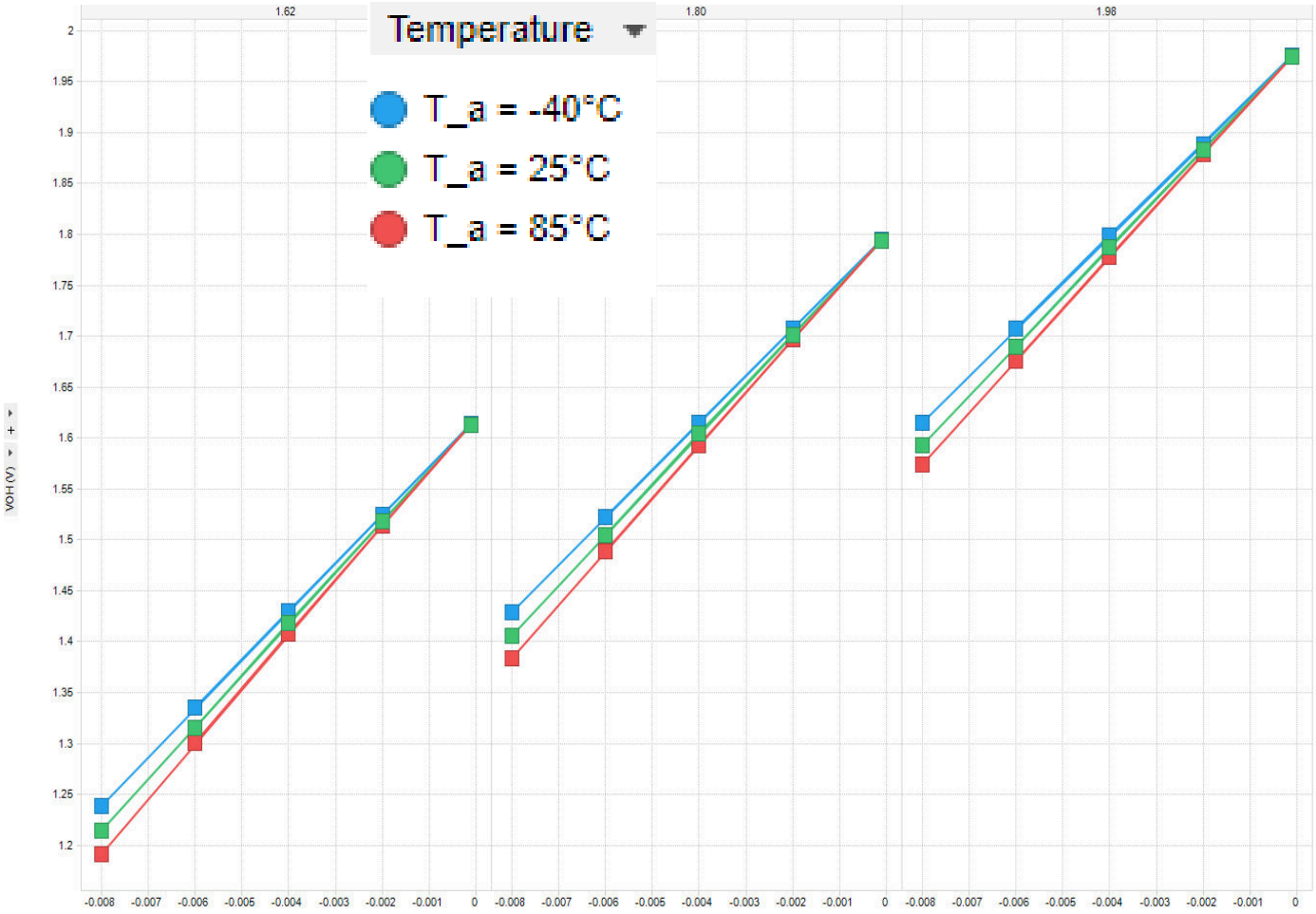

図 5-8. LED_0, LED_2, CLKOUT VOH 1.8V

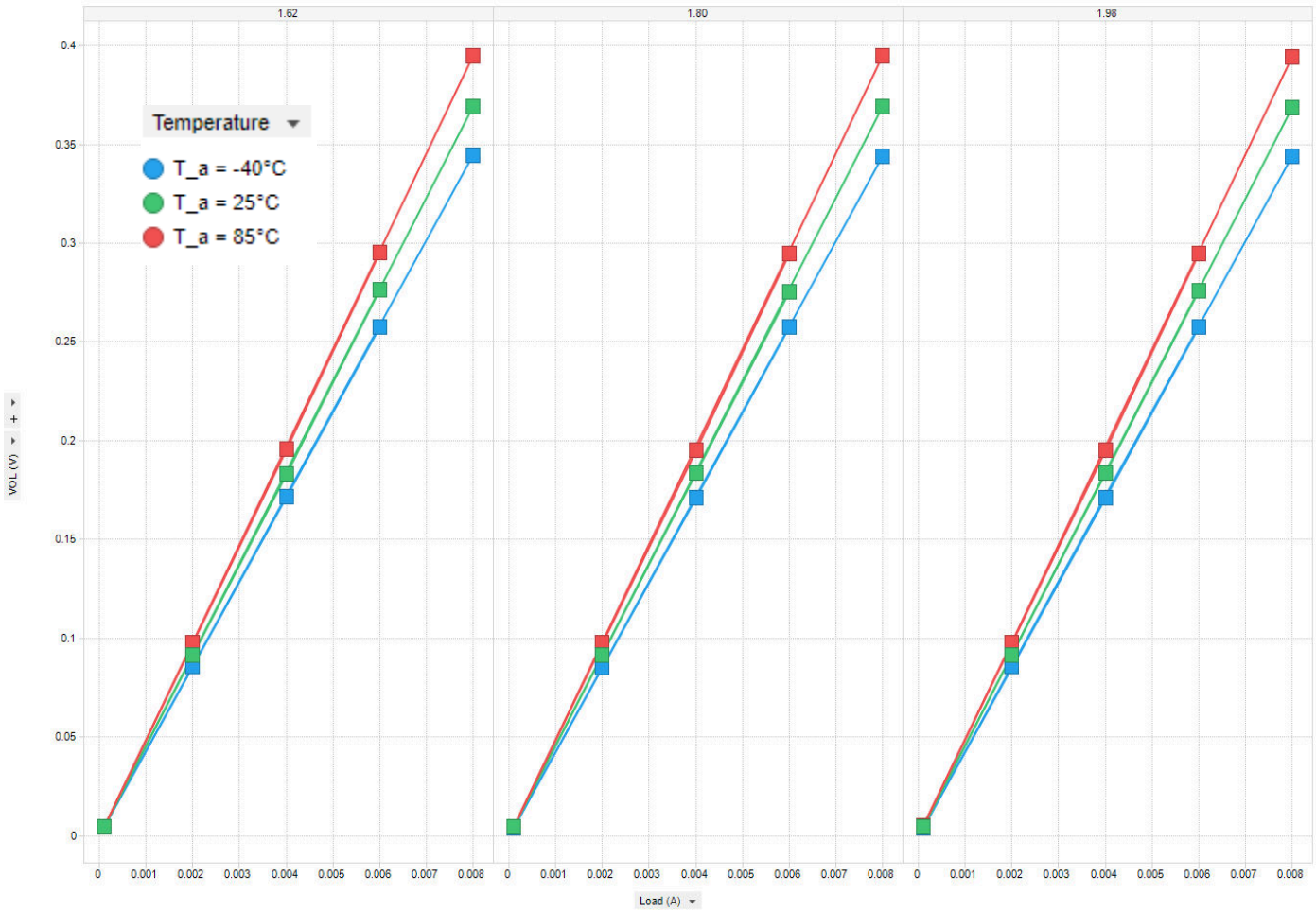

図 5-9. LED_0, LED_2, CLKOUT VOL 1.8V

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6 Detailed Description

6.1 Overview

The DP83825I is a fully-featured single-port Physical Layer transceiver compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The device supports the standard Reduced Media Independent Interface (RMII) for direct connection to Media Access Controller (MAC).

The device is designed for a single 3.3V power supply with an integrated LDO to provide voltage rails needed for internal blocks. The device allows I/O voltage interfaces for 3.3V or 1.8V. Automatic supply configuration within the DP83825I allows for any combination of VDDIO supply and AVDD supply without the need for additional configuration settings.

The DP83825I uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5e twisted-pair cables up to 150 meters long. DP83825I supports various Low Power features like Active Sleep, IEEE Power Down and Deep Power Down. The DP83825I also supports Energy Efficient Ethernet and Wake-on-LAN.

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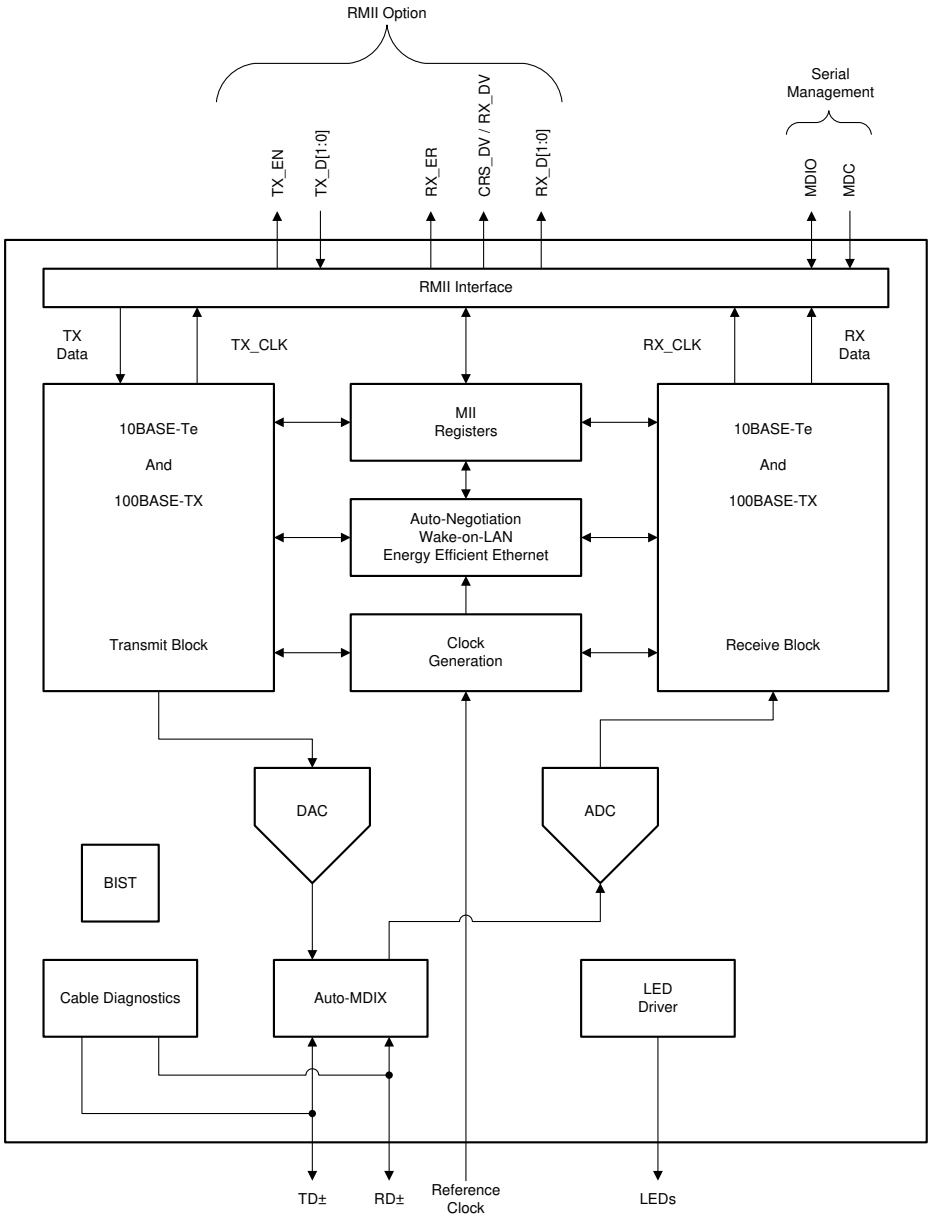
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Auto-Negotiation (Speed / Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83825I supports 100BASE-TX and 10BASE-Te modes of operation for Auto-Negotiation. Auto-Negotiation makes sure that the highest common speed is selected based on the advertised abilities of the Link Partner and the local device. Auto-Negotiation can be enabled or disabled in hardware, using the bootstrap, or by register configuration, using bit[12] in the Basic Mode Control Register (BMCR, address 0x0000). For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification.

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6.3.2 Auto-MDIX Resolution

The DP83825I can determine if a “straight” or “crossover” cable is used to connect to the link partner. The DP83825I can automatically re-assign channel A and B to establish link with the link partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. Auto-MDIX is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Forced modes.

Auto-MDIX can be enabled or disabled in hardware, using the hardware bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished using register configuration, using bit[14] of the PHYCR.

6.3.3 Energy Efficient Ethernet

6.3.3.1 EEE Overview

Energy Efficient Ethernet (EEE), defined by IEEE 802.3az, is a capability integrated into Layer 1 (Physical Layer) and Layer 2 (Data Link Layer) to operate in Low Power Idle (LPI) mode. In LPI mode, power is saved during periods of low packet utilization. EEE defines the protocol to enter and exit LPI mode without dropping the link or corrupting packets.

The DP83825I EEE supports 100Mbps and 10Mbps speeds. In 10BASE-Te operation, EEE operates with a reduced transmit amplitude that is fully interoperable with a 10BASE-T PHY.

6.3.3.2 EEE Negotiation

EEE is advertised during Auto-Negotiation. Auto-Negotiation is performed at power up, on management command, after link failure, or due to user intervention. EEE is supported if and only if both link partners advertise EEE capabilities. If EEE is not supported, all EEE functions are disabled and the MAC must not assert LPI. To advertise EEE capabilities, the PHY needs to exchange an additional formatted next page and unformatted next page in sequence.

EEE Negotiation can be activated using Register Access. IEEE 802.3az defines MMD3 and MMD7 as the locations for EEE control and status registers. The MMD3 registers 0x1014, 0x1001, 0x1016, and MMD7 registers 0x203C and 0x203D contain all the required controls and status indications for operating EEE. The Energy Efficient Ethernet Configuration Register #3 (EEECFG3, address 0x04D1) contains controls for EEE configuration bypass. By default, EEE capabilities are bypassed. To advertise EEE based on MMD3 and MMD7 registers, EEE capabilities bypass needs to be disabled (0x04D1.0 = 0, 0x04D1.3 = 0) and EEE Advertisement shall be enabled (MMD7 0x203C.1 = 1).

6.3.4 EEE for Legacy MACs Not Supporting 802.3az

The device can be configured to initiate LPI signaling (Idle and Refresh) through register programming as well. This feature enables the system to perform EEE even when the MAC used is not supporting EEE. In this mode, responsibility of enabling and disabling LPI signaling lies on the Host Controller Application. While the DP83825I is in LPI signaling mode, this application moves the DP83825I into active mode before sending any data over the MAC interface. The DP83825I does not have buffering capability to store the data while in LPI signaling mode. To enable EEE through register configuration, the following registers must be configured:

1. Enable EEE capabilities by writing 0x04D1.0 = 0, 0x04D1.3 = 0
2. Advertise EEE capabilities during auto-negotiation by writing (MMD7 0x203C.1 = 1)
3. Renegotiate the link by writing 0x0000.9 = 1
4. Forced Tx LPI idles by writing 0x04D1.12 = 1
5. Write 0x04D1.12=0 to stop transmitting LPI Idles

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6.3.5 Wake-on-LAN Packet Detection

Wake-on-LAN (WoL) provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83825I allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet and Magic Packet with Secure-ON Match. When a qualifying WoL frame is received, the DP83825I WoL logic circuit is able to generate a user-defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. Additionally, the DP83825I includes a CRC Gate to prevent invalid packets from triggering a wake-up event. The Wake-on-LAN feature includes:

- Identification of WoL frames in all supported speeds (100BASE-TX and 10BASE-Te).
- Wake-up interrupt generation upon reception of a WoL frame.
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames.

6.3.5.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83825I scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which can be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF.

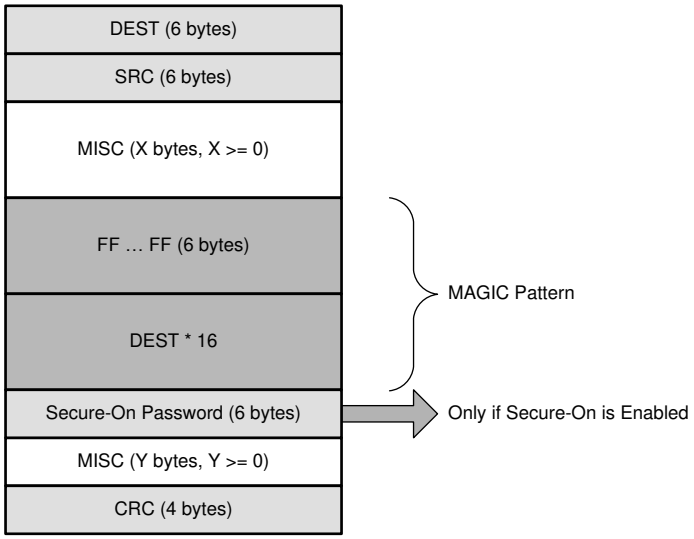

図 6-1. Magic Packet Structure

6.3.5.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a secure-on password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
```


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```
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

6.3.5.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Receiver Status Register (RXFS, address 0x04A1). The Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register #2 (MISR2, address 0x0013).

6.3.6 Low Power Modes

The DP83825I supports three Low Power Modes. This section discusses the principles behind these low power modes and configuration to enable them.

6.3.6.1 Active Sleep

When the DP83825I enters into Active Sleep mode, all internal circuitry shuts down in the PHY except for the SMI and energy detection circuitry on the TD± and RD± pins. In this mode, the DP83825 sends out NLPs every 1.4 seconds to wake up the link partner. Automatic power up occurs when a link partner is detected.

Active Sleep is enabled by setting bits[14:12] = 0b110 in the PHY Specific Control Register (PHYSCR, address 0x0011).

6.3.7 IEEE Power Down

IEEE Power Down shuts down all PHY circuitry except the SMI and internal clock circuitry.

IEEE Power Down can be activated by either register access or through the INTR/PWRDN pin when the pin is configured for power-down function.

To enable IEEE Power Down through the INTR/PWRDN pin, the pin must be driven LOW to ground.

To enable IEEE Power Down through the SMI, set bit[11] = 1 in the Basic Mode Control Register (BMCR, address 0x0000).

6.3.8 Deep Power Down

Deep Power Down shuts down all PHY circuitry except the SMI. In this mode, the PHY PLL is shut-down to further reduce power consumption.

Deep Power Down is activated by first enabling IEEE Power Down (from either the SMI or INT/PWDN_N pin) and then setting bit[2] = 1 in the Deep Power Down Control Register (DPDWN, address 0x0428).

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6.3.9 Reduced Media Independent Interface (RMII)

The incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The offers two types of RMII operations: RMII Slave and RMII Master. In RMII Master operation, the operates off either a 25MHz CMOS-level oscillator connected to XI pin or a 25MHz crystal connected across XI and XO pins. A 50MHz output clock referenced from can be connected to the MAC. In RMII Slave operation, the operates off of a 50MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII Slave mode, the PHY can run from 50MHz clock provided by the Host MAC.

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te.
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are two bits for every clock cycle using the internal 50MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in 表 6-1:

表 6-1. RMII Signals

FUNCTION	PINS
Receive Data Lines	TX_D[1:0]
Transmit Data Lines	RX_D[1:0]
Receive Control Signal	TX_EN
Transmit Control Signal	CRS_DV

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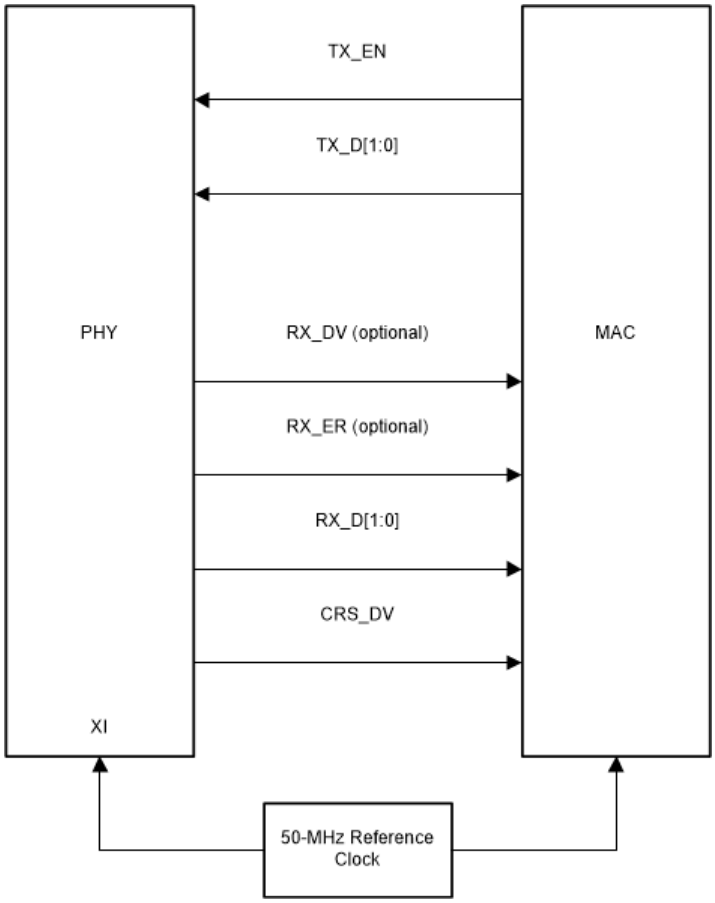

図 6-2. RMII Slave Signaling

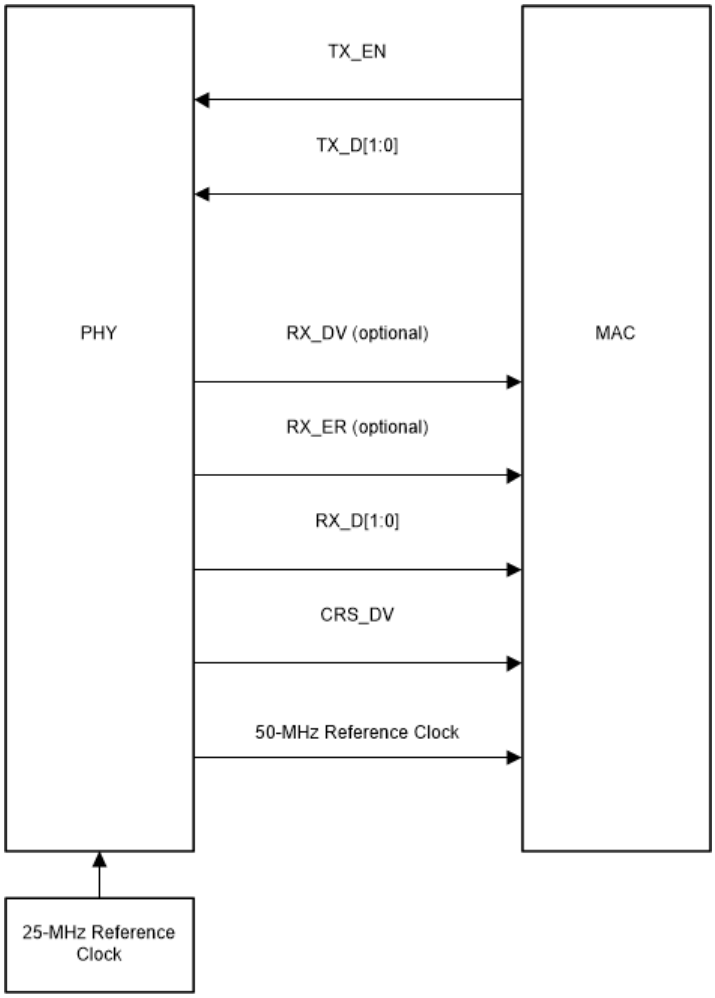

図 6-3. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the clock edges on the XI pin. Data on RX_D[1:0] are latched at the MAC with reference to the same clock edges on the XI pin.

In addition, CRX_DV can be configured as RX_DV signal. This allows for a simpler method of recovering received data without the need to separate RX_DV from the CRS_DV indication.

6.3.10 RMII Repeater Mode

The DP83825I provides an option to enable repeater mode functionality to extend the cable reach in un-managed mode (without the need of additional register configuration). Two DP83825I can be connected in back-to-back mode without any external configuration. This provides a Hardware Strap to configure the CRS_DV pin of RMII interface to RX_DV pin for back-to-back operation. 図 6-4 shows the RMII pin connection that can enable DP83825I Repeater mode. If using managed mode, external Reset to both PHYs are triggered at the same time.

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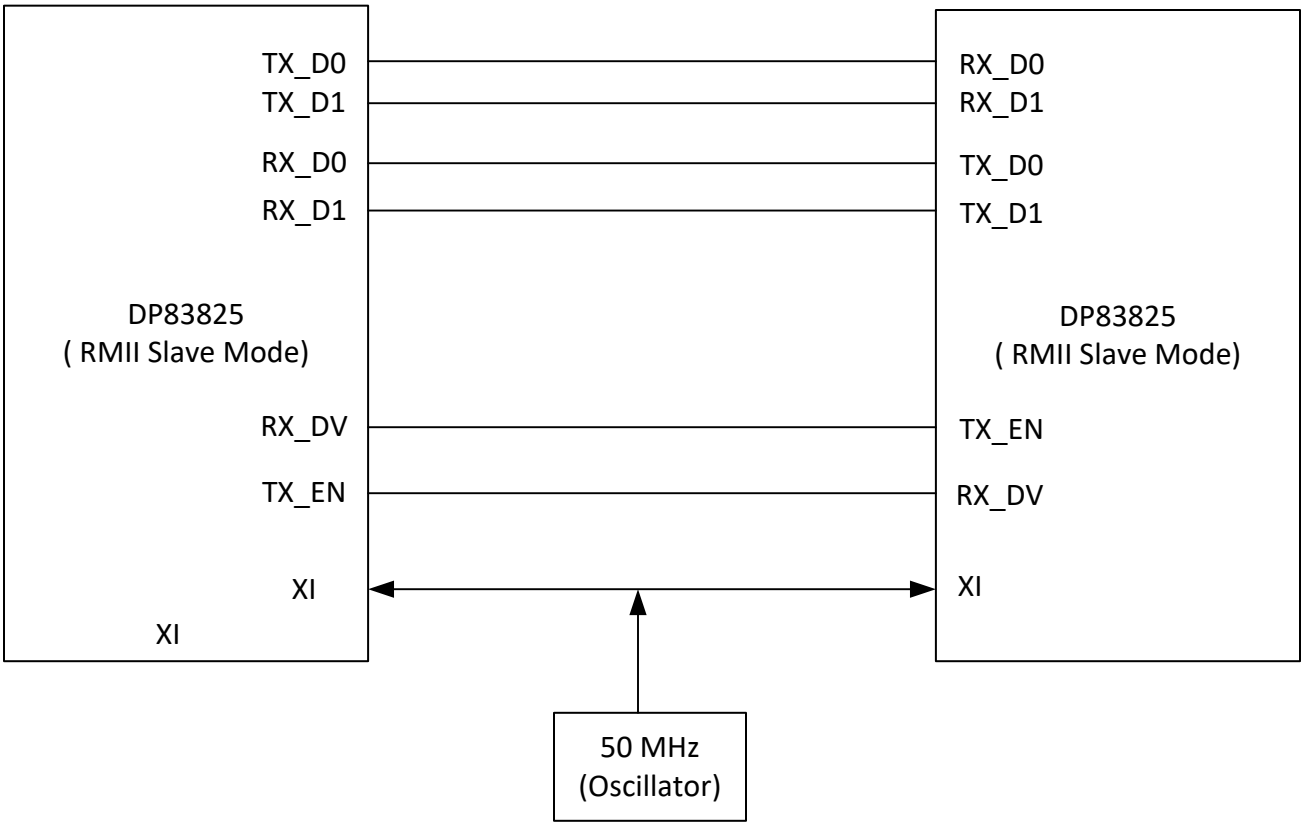

図 6-4. RMII Repeater Mode

6.3.11 Serial Management Interface

The Serial Management Interface provides access to the DP83825I internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83825I.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2kΩ), which pulls MDIO high during IDLE and turnaround.

Up to 4 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83825I latches the Phy_Address[1:0] configuration pins to determine the address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor-specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device can actively drive the MDIO signal during the first bit of turnaround. The addressed DP83825I drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83825I, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

表 6-2. SMI Protocol

SMI PROTOCOL	<idle><start><op code><PHY address><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

6.3.11.1 Extended Register Space Access

The DP83825I's SMI function supports read or write access to the extended register set using registers REGCR (0x0D) and ADDAR (0x0E) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR (0x0D) and ADDAR (0x0E), which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR (0x0D) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR (0x0E) register to the appropriate MMD.

The DP83825I's supports one MMD device address. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.

All accesses through registers REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

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表 6-3. REGCR DEVAD Functions

REGCR[15:14]	Function
00	Accesses to register ADDAR modify the extended register 'set address' register. This address register must always be initialized to access any of the registers within the extended register set.
01	Accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
10	Access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
11	Access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111).

6.3.11.2 Read Operation

To read a register in the extended register set:

Instruction	Example: Read 0x0170
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

6.3.11.3 Write Operation

To write a register in the extened register set:

Instruction	Example: Set reg 0x0170 = 0C50
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR (0x0D).	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR (0x0E).	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

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6.3.12 100BASE-TX

6.3.12.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in 表 6-4 below.

The transmitter section consists of the following functional blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83825I implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

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表 6-4. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T, and R in data fields are mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

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6.3.12.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to 表 6-4 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

6.3.12.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable can peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed-loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed-loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20dB.

6.3.12.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI-encoded to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5, unshielded twisted-pair cable. There is no ability to bypass this block within the DP83825I. The NRZI data is sent to the 100Mbps Driver.

6.3.12.1.4 Binary to MLT-3 Converter

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted-pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output Pair common driver is controlled by the slew rate. The designer must consider this when selecting AC-coupling magnetics to make sure TP-PMD standard-compliant transition times (3ns < Trise/fall < 5ns).

The 100BASE-TX transmit TP-PMD function within the DP83825I is capable of sourcing only MLT-3-encoded data. Binary output from the PMD Output Pair is not possible in 100Mbps mode. Fully-encoded MLT-3 on both Tx+ and Tx– and can be configured through Register 0x0404 (for example, in transformer-less designs).

6.3.12.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125Mbps serial data stream to synchronous 2-bit wide data that is provided to the RMII.

The receive section consists of the following functional blocks:

1. Input and BLW Compensation
2. Signal Detect
3. Digital Adaptive Equalization
4. MLT-3 to Binary Decoder
5. Clock Recovery Module
6. NRZI to NRZ Decoder
7. Descrambler

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8. Serial to Parallel
9. Code-Group Alignment
10. 4B/5B Decoder
11. Link Integrity Monitor
12. Bad SSD Detection

6.3.13 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3-compliant. This includes the receiver, transmitter, collision detection, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

6.3.13.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50ns. Finally, the signal must again exceed the original squelch level no earlier than 50ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

6.3.13.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100ns in duration and transmitted every 16ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

6.3.13.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83825I output and disables the transmitter if the transmitter attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be deasserted for approximately 500ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te mode.

6.3.13.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair can cause polarity errors, and the wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because it's based on MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

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6.3.14 Loopback Modes

There are several loopback options within the DP83825I that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83825I can be configured to any one of the Loopback modes described below. MII Loopback is configured using the Basic Mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

Auto-Negotiation must be disabled before selecting the Loopback modes. This constraint does not apply for external-loopback mode.

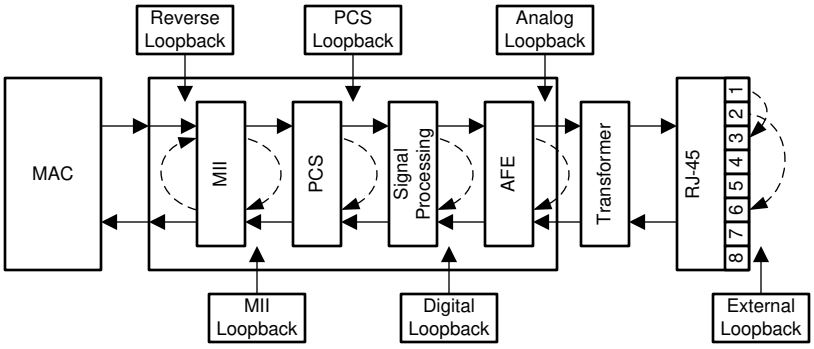

図 6-5. Loopback Test Modes

6.3.14.1 MII Loopback

MII Loopback is the most shallow loop through the PHY. MII Loopback is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83825I to the RX pins where the data can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR and bit[2] in BISCR.

6.3.14.2 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

6.3.14.3 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuitry.

Digital Loopback is enabled by setting bit[2] in the BISCR.

6.3.14.4 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end. Analog Loopback requires 100Ω terminations across pins #1 and #2, as well as 100Ω terminations across pins #3 and #6 at the RJ45.

Analog Loopback is enabled by setting bit[3] in the BISCR.

6.3.14.5 Reverse Loopback

Reverse loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then

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transmitted back to the Link Partner. All data signals that come from the MAC are ignored in this mode. This requires 100Ω terminations across pins #1 and #2.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

6.3.15 BIST Configurations

The DP83825I incorporates an internal PRBS built-in self-test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST Packet Length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG Length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This locks the current value of the BIST errors for reading. Note that setting bit[15] also clears the BIST Error Counter.

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6.3.16 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive, and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed require a non-intrusively way to identify and report cable faults. The DP83825I offers Time Domain Reflectometry (TDR) capabilities to detect opens and shorts on the cable.

6.3.16.1 TDR

The DP83825I uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations, in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The DP83825I transmits a test pulse of known amplitude (1V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable defect, fault, connector and from the end of the cable. After the pulse transmission, the DP83825I measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1m accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the Link Partner is disconnected – cable is unplugged at the other side
- Link Partner is connected but remains “quiet” (for example, in power down mode)
- TDR can be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Register #1 (CR1, address 0x0009). When a link drops, TDR automatically executes and store the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170).

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6.3.16.2 Fast Link-Drop Functionality

The DP83825I includes advanced link-drop capabilities that support various real-time applications. The link-drop mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83825I supports an enhanced link-drop mechanism, also called Fast Link-Drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference. Fast Link-Drop can be enabled in software using register configuration. FLD can be configured using the Control Register #3 (CR3, address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When a link-drop occurs, the indication of a particular fault condition can be read from the Fast Link-Drop Status Register (FLDS, address 0x000F).

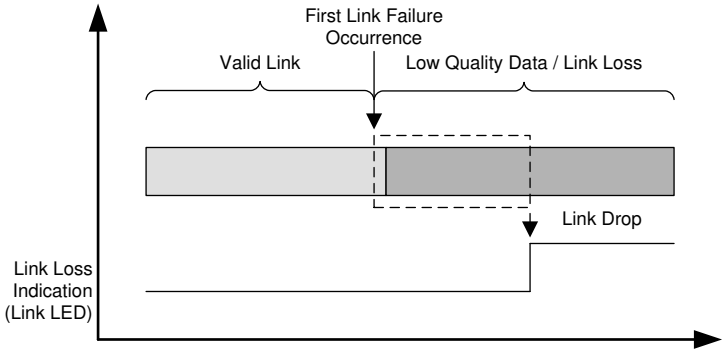

図 6-6. Fast Link Drop

Fast Link-Drop criteria include:

- RX Error Count - when a predefined number of 32 RX_ERs occur in a 10µs window, the link is dropped.
- MLT3 Error Count - when a predefined number of 20 MLT3 errors occur in a 10µs window, the link is dropped.
- Low SNR Threshold - when a predefined number of 20 threshold crossings occur in a 10µs window, the link is dropped.
- Signal/Energy Loss - when the energy detector indicates energy loss, the link is dropped.

The Fast Link-Drop functionality allows the use of each of these options separately or in any combination.

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Because this mode enables extremely quick reaction time, it's more exposed to temporary bad link-quality scenarios.

6.4 Device Functional Modes

DP83825I offers modes to optimize cable reach and power consumption. In default mode, The DP83825I offers a cable reach of 100 meters and above. To achieve a 150-meter cable with the lowest power consumption and Energy Efficient Ethernet, the designer must program a configuration after PHY is out of reset. The following section describes the various modes available and configuration required to achieve these.

- **Default Mode**

  This mode offers a 100+ meters cable reach mode where no additional configuration programming is needed.
- **Power Optimized Mode**

  This mode offers the lowest power consumption along with a cable reach of 130 meters and more. 表 6-5 shows the required register configuration that is programmed through the MDC/MDIO interface.

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表 6-5. Configurations for Power Optimized Mode, 130-Meter Cable Reach

Register Address	Value
0x0416	0x1F30
0x040D	0x000D
0x0429	0x0200
0x030B	0x0BC0
0X030C	0x0011
0x033C	0x0001
0X0311	0x0000
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0000
0x033D	0x8110
0x031B	0x0048
0x001F	0x4000

- **Cable Reach Optimized Mode**

  This mode offers a cable reach of up to 150 meters. 表 6-6 shows the required register configuration that is programmed through the MDC/MDIO interface.

表 6-6. Configurations for Cable Reach Optimized Mode, 150-Meter Cable Reach

Register Address	Value
0x0416	0x1F30
0x040D	0x000D
0x0429	0x0200
0x030B	0x0BC0
0X030C	0x0011
0x033C	0x0001
0X0311	0x0000
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0080
0x033D	0x8110
0x031B	0x0048
0x001F	0x4000

- **Cable Reach Optimized Mode with EEE**

  Energy Efficient Ethernet (EEE) is disabled by default in the DP83825I. EEE must be enabled through register programming. 表 6-7 shows the required register configuration that is programmed through the MDC/MDIO interface

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表 6-7. Configurations for EEE

Register Address	Value
0x0416	0x1F30
0x040D	0x000d
0x0429	0x0200
0x030B	0x0BC0
0x30C	0x0011
0x33C	0x0001
0x0311	0x0000
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0080
0x0130	0x4750
0x0123	0x0800
0x030F	0x0400
0x04D4	0x6633
0x4D5	0x027F
0x4D6	0x01B0
0x4D7	0x01B0
0x031F	0xFC36
0x031C	0x1103
0x0101	0x0882
0x010A	0x2010
0x04CE	0x00FF
0x04CD	0xA5A5
0x0308	0x0982
0x04CF	0x231D
0x04D0	0x0F8F
0x033E	0x861E
0x04D1	0x00C2
0x04D2	0x215B
0x033D	0x8110
0x031B	0x0048
0x001F	0x4000

6.5 Programming

The DP83825I provide IEEE-defined register set for programming and status, and also provides an additional register set to configure other features not supported through IEEE registers.

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6.5.1 Straps Configuration

The DP83825 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. Configuration of the device can be done through the strap pins or through the management register interface. A pullup resistor or a pulldown resistor of suggested values can be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes. The MAC interface pins must support I/O voltages of 3.3V and 1.8V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3V and 1.8V supplies depending on what voltage was selected for I/O. All strap pins have two levels.

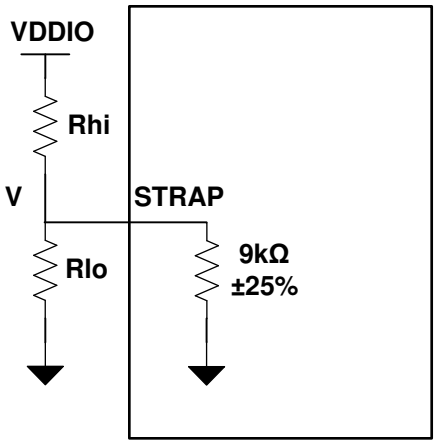

図 6-7. Strap Circuit

表 6-8. 2-Level Strap Resistor Ratio

MODE	RECOMMENDED RESISTORS	
	Rhi (kΩ)	Rlo (kΩ)
0	OPEN	2.49
1	2.49	OPEN

6.5.1.1 Straps for PHY Address

表 6-9. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_D0	PhyAdd[0](1)	18	0		PHY_ADD0
				MODE 0	0
				MODE 1	1
CRS_DV	PhyAdd[1](1)	20	0		PHY_ADD1
				MODE 0	0
				MODE 1	1

(1) PhyAdd[1:0] is determined by the two straps on pin 18 and 20 that translate to the bit[0] and bit[1] respectively.

表 6-10. RMII MAC Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_D1	Master/Slave	17	0	0	RMII Master Mode
				1	RMII Slave Mode

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表 6-10. RMII MAC Mode Strap Table (続き)

PIN NAME	STRAP NAME	PIN #	DEFAULT		
50MHzOut/LED2	RX_DV_En	2	0	0	Pin 20 is configured as CRS_DV
				1	Pin 20 is configured as RX_DV (For RMII Repeater Mode)

表 6-11. Auto_Neg Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_ER	A-MDIX	22	0	0	Auto MDIX Enable
				1	Auto MDIX Disable
LED0	ANeg_Dis	4	0	0	Auto Negotiation Enable
				1	Auto-Negotiation Disable. Force Mode 100M Enabled

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6.6 Device Registers

表 6-12 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in 表 6-12 should be considered as reserved locations and the register contents should not be modified.

表 6-12. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	BMCR_Register		Go
1h	BMSR_Register		Go
2h	PHYIDR1_Register		Go
3h	PHYIDR2_Register		Go
4h	ANAR_Register		Go
5h	ALNPAR_Register		Go
6h	ANER_Register		Go
7h	ANNPTR_Register		Go
8h	ANLNPTR_Register		Go
9h	CR1_Register		Go
Ah	CR2_Register		Go
Bh	CR3_Register		Go
Ch	Register_12		Go
Dh	REGCR_Register		Go
Eh	ADDAR_Register		Go
Fh	FLDS_Register		Go
10h	PHYSTS_Register		Go
11h	PHYSCR_Register		Go
12h	MISR1_Register		Go
13h	MISR2_Register		Go
14h	FCSCR_Register		Go
15h	RECR_Register		Go
16h	BISCR_Register		Go
17h	RCSR_Register		Go
18h	LEDCR_Register		Go
19h	PHYCR_Register		Go
1Ah	10BTSCR_Register		Go
1Bh	BICSR1_Register		Go
1Ch	BICSR2_Register		Go
1Eh	CDCR_Register		Go
1Fh	PHYRCR_Register		Go
25h	MLEDCR_Register		Go
27h	COMPT_Regsiter		Go
101h	Register_101		Go
10Ah	Register_10a		Go
123h	Register_123		Go
130h	Register_130		Go
170h	CDSCR_Register		Go
171h	CDSCR2_Register		Go
172h	TDR_172_Register		Go
173h	CDSCR3_Register		Go

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表 6-12. DEVICE Registers (続き)

Offset	Acronym	Register Name	Section
174h	TDR_174_Register		Go
175h	TDR_175_Register		Go
176h	TDR_176_Register		Go
177h	CDSCR4_Register		Go
178h	TDR_178_Register		Go
180h	CDLRR1_Register		Go
181h	CDLRR2_Register		Go
182h	CDLRR3_Register		Go
183h	CDLRR4_Register		Go
184h	CDLRR5_Register		Go
185h	CDLAR1_Register		Go
186h	CDLAR2_Register		Go
187h	CDLAR3_Register		Go
188h	CDLAR4_Register		Go
189h	CDLAR5_Register		Go
18Ah	CDLAR6_Register		Go
302h	IO_CFG_Register		Go
305h	IO_CFG_2_Register		Go
308h	SPARE_OUT		Go
30Bh	DAC_CFG_0		Go
30Ch	DAC_CFG_1		Go
30Fh	DSP_CFG_0		Go
311h	DSP_CFG_2		Go
313h	DSP_CFG_4		Go
31Ch	DSP_CFG_13		Go
31Fh	DSP_CFG_16		Go
33Ch	DSP_CFG_25		Go
33Eh	DSP_CFG_27		Go
404h	ANA_LD_PRG_SL_Register		Go
40Dh	ANA_RX10BT_CTRL_Register		Go
416h	Register_416		Go
429h	Register_429		Go
456h	GENCFG_Register		Go
460h	LEDCFG_Register		Go
461h	IOCTRL_Register		Go
467h	SOR1_Register		Go
468h	SOR2_Register		Go
469h	Register_0x469_Register		Go
4A0h	RXFCFG_Register		Go
4A1h	RXFS_Register		Go
4A2h	RXFPMD1_Register		Go
4A3h	RXFPMD2_Register		Go
4A4h	RXFPMD3_Register		Go
4CDh	Register_0x4cd		Go
4CEh	Register_0x4ce		Go

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表 6-12. DEVICE Registers (続き)

Offset	Acronym	Register Name	Section
4CFh	Register_0x4cf		Go
4D0h	EEECFG2_Register		Go
4D1h	EEECFG3_Register		Go
4D2h	Register_0x4d2		Go
4D4h	Register_0x4d4		Go
4D5h	DSP_100M_STEP_2_Register		Go
4D6h	DSP_100M_STEP_3_Register		Go
4D7h	DSP_100M_STEP_4_Register		Go
1000h	MMD3_PCS_CTRL_1_Register		Go
1001h	MMD3_PCS_STATUS_1		Go
1014h	MMD3_EEE_CAPABILITY_Register		Go
1016h	MMD3_WAKE_ERR_CNT_Register		Go
203Ch	MMD7_EEE_ADVERTISEMENT_Register		Go
203Dh	MMD7_EEE_LP_ABILITY_Register		Go

Complex bit access types are encoded to fit into small table cells. 表 6-13 shows the codes that are used for access types in this section.

表 6-13. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.1 BMCR_Register (Offset = 0h) [Reset = 3100h]

BMCR_Register is shown in 表 6-14.

Return to the Summary Table.

表 6-14. BMCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reset	W	0h	PHY Software Reset: Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers are not cleared. 0h = Normal Operation 1h = Initiate software Reset / Reset in PRgress
14	MII_Loopback	R/W	0h	MII Loopback: When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally. Applicable for the only available RMII interface. This also needs to set following additional bit BISCR 0x0016[4:0] = 0b00100 for 100Base-TX and BISCR 0x0016[4:0] = 00001b for 10Base-Te 0h = Normal Operation 1h = MII Loopback enabled

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表 6-14. BMCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
13	Speed_Selection	R/W	1h	Speed Select: When Auto-Negotiation is disabled (bit [12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected. 0h = 10Mbps 1h = 100Mbps
12	Auto-Negotiation_Enable	R/W	1h	Auto-Negotiation Enable: 0h = Disable Auto-Negotiation - bits [8] and [13] determine the port speed and duplex mode 1h = Enable Auto-Negotiation - bits [8] and [13] of this register are ignored when this bit is set
11	IEEE_Power_Down	R/W	0h	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set. 0h = Normal Operation 1h = IEEE Power Down
10	Isolate	R/W	0h	Isolate: 0h = Normal Operation 1h = Isolates the port from the MII with the exception of the serial management interface. This also disables 50MHz clock in RMII Master Mode
9	Restart_Auto-Negotiation	R/W	0h	Restart Auto-Negotiation: If Auto-Negotiation is disabled (bit [12] = 0), bit [9] is ignored. This bit is self-clearing and returns a value of 1 until Auto-Negotiation is initiated, whereupon this self-clears. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0h = Normal Operation 1h = Restarts Auto-Negotiation, Re-initiates the Auto-Negotiation process
8	Duplex_Mode	R/W	1h	Duplex Mode: When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected. 0h = Half-Duplex 1h = Full-Duplex
7	Collision_Test	R/W	0h	Collision Test: When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN. 0h = Normal Operation 1h = Enable COL Signal Test
6-0	RESERVED	R	0h	Reserved

6.6.2 BMSR_Register (Offset = 1h) [Reset = 7849h]

BMSR_Register is shown in 表 6-15.

Return to the Summary Table.

表 6-15. BMSR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0h	100Base-T4 Capable: This protocol is not available. Always reads as 0.
14	100Base-TX_Full-Duplex	R	1h	100Base-TX Full-Duplex Capable: 0h = Device not able to perform Full-Duplex 100Base-TX 1h = Device able to perform Full-Duplex 100Base-TX
13	100Base-TX_Half-Duplex	R	1h	100Base-TX Half-Duplex Capable: 0h = Device not able to perform Half-Duplex 100Base-TX 1h = Device able to perform Half-Duplex 100Base-TX

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表 6-15. BMSR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
12	10Base-T_Full-Duplex	R	1h	10Base-T Full-Duplex Capable: 0h = Device not able to perform Full-Duplex 10Base-T 1h = Device able to perform Full-Duplex 10Base-T
11	10Base-T_Half-Duplex	R	1h	10Base-T Half-Duplex Capable: 0h = Device not able to perform Half-Duplex 10Base-T 1h = Device able to perform Half-Duplex 10Base-T
10-7	RESERVED	R	0h	Reserved
6	SMI_Preamble_Suppression	R	1h	Preamble Suppression Capable: If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaRund. he device requires minimum of 500ns gap between two transactions, followed by one posedge of MDC and MDIO=1, before starting the next transaction. 0h = Device not able to perform management transaction with preambles suppressed 1h = Device able to perform management transaction with preamble suppressed
5	Auto-Negotiation_Complete	R	0h	Auto-Negotiation Complete: 0h = Auto Negotiation process not completed (either still in process, disabled or reset) 1h = Auto-Negotiation process completed
4	Remote_Fault	R	0h	Remote Fault: Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset. 0h = No remote fault condition detected 1h = Remote fault condition detected
3	Auto-Negotiation_Ability	R	1h	Auto-Negotiation Ability: 0h = Device is not able to perform Auto-Negotiation 1h = Device is able to perform Auto-Negotiation
2	Link_Status	R	0h	Link Status: 0h = Link not established 1h = Valid link established (for either 10Mbps or 100Mbps operation)
1	Jabber_Detect	R	0h	Jabber Detect: 0h = No jabber condition detected This bit only has meaning for 10Base-T operation. 1h = Jabber condition detected
0	Extended_Capability	R	1h	Extended Capability: 0h = Basic register set capabilities only 1h = Extended register capabilities

6.6.3 PHYIDR1_Register (Offset = 2h) [Reset = 2000h]

PHYIDR1_Register is shown in 表 6-16.

Return to the Summary Table.

表 6-16. PHYIDR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally_Unique_Identifier_Bits_21:6	R	2000h	PHY Identifier Register #1

6.6.4 PHYIDR2_Register (Offset = 3h) [Reset = A140h]

PHYIDR2_Register is shown in 表 6-17.

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表 6-17. PHYIDR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally_Unique_Identifier_Bits_5:0	R	28h	PHY Identifier Register #2
9-4	Model_Number	R	14h	Vendor Model Number: The six bits of vendor model number are mapped from bits [9] to [4]
3-0	Revision_Number	R	0h	Model Revision Number: Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

6.6.5 ANAR_Register (Offset = 4h) [Reset = 01E1h]

ANAR_Register is shown in 表 6-18.

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表 6-18. ANAR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0h	Next Page Indication: 0h = Next Page Transfer not desired 1h = Next Page Transfer desired
14	RESERVED	R	0h	Reserved
13	Remote_Fault	R/W	0h	Remote Fault: 0h = No Remote Fault detected 1h = Advertises that this device has detected a Remote Fault. Please note DP83825 does not support Remote Fault. This bit shall not be set by Application
12	RESERVED	R	0h	Reserved
11	Asymmetric_Pause	R/W	0h	Asymmetric Pause Support For Full-Duplex Links: 0h = Do not advertise asymmetric pause ability 1h = Advertise asymmetric pause ability
10	Pause	R/W	0h	Pause Support for Full-Duplex Links: 0h = Do not advertise pause ability 1h = Advertise pause ability
9	100Base-T4	R	0h	100Base-T4 Support: 0h = Do not advertise 100Base-T4 ability 1h = Advertise 100Base-T4 ability
8	100Base-TX_Full-Duplex	R/W	1h	100Base-TX Full-Duplex Support: Values does not matter in forced-mode 0h = Do not advertise 100Base-TX Full-Duplex ability Values does not matter in forced-mode 1h = Advertise 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex	R/W	1h	100Base-TX Half-Duplex Support: Values does not matter in forced-mode 0h = Do not advertise 100Base-TX Half-Duplex ability Values does not matter in forced-mode 1h = Advertise 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex	R/W	1h	10Base-T Full-Duplex Support: Values does not matter in forced-mode 0h = Do not advertise 10Base-T Full-Duplex ability Values does not matter in forced-mode 1h = Advertise 10Base-T Full-Duplex ability
5	10Base-T_Half-Duplex	R/W	1h	10Base-T Half-Duplex Support: Values does not matter in forced-mode 0h = Do not advertise 10Base-T Half-Duplex ability Values does not matter in forced-mode 1h = Advertise 10Base-T Half-Duplex ability

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表 6-18. ANAR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	Selector_Field	R/W	1h	protocol Selection Bits: Technology selector field (IEEE802.3u <00001>)

6.6.6 ALNPAR_Register (Offset = 5h) [Reset = 0000h]

ALNPAR_Register is shown in 表 6-19.

Return to the Summary Table.

表 6-19. ALNPAR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R	0h	Next Page Indication: 0h = Link partner does not desire Next Page Transfer 1h = Link partner desires Next Page Transfer
14	Acknowledge	R	0h	Acknowledge: 0h = Link partner does not acknowledge reception of link code word 1h = Link partner acknowledges reception of link code word
13	Remote_Fault	R	0h	Remote Fault: 0h = Link partner does not advertise remote fault event detection 1h = Link partner advertises remote fault event detection
12	RESERVED	R	0h	Reserved
11	Asymmetric_Pause	R	0h	Asymmetric Pause: 0h = Link partner does not advertise asymmetric pause ability 1h = Link partner advertises asymmetric pause ability
10	Pause	R	0h	Pause: 0h = Link partner does not advertise pause ability 1h = Link partner advertises pause ability
9	100Base-T4	R	0h	100Base-T4 Support: 0h = Link partner does not advertise 100Base-T4 ability 1h = Link partner advertises 100Base-T4 ability
8	100Base-TX_Full-Duplex	R	0h	100Base-TX Full-Duplex Support: 0h = Link partner does not advertise 100Base-TX Full-Duplex ability 1h = Link partner advertises 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex	R	0h	100Base-TX Half-Duplex Support: 0h = Link partner does not advertise 100Base-TX Half-Duplex ability 1h = Link partner advertises 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex	R	0h	10Base-T Full-Duplex Support: 0h = Link partner does not advertise 10Base-T Full-Duplex ability 1h = Link partner advertises 10Base-T Full-Duplex ability
5	10Base-T_Half-Duplex	R	0h	10Base-T Half-Duplex Support: 0h = Link partner does not advertise 10Base-T Half-Duplex ability 1h = Link partner advertises 10Base-T Half-Duplex ability
4-0	Selector_Field	R	0h	protocol Selection Bits: Technology selector field (IEEE802.3 <00001>)

6.6.7 ANER_Register (Offset = 6h) [Reset = 0004h]

ANER_Register is shown in 表 6-20.

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表 6-20. ANER_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved

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表 6-20. ANER_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	Parallel_Detection_Fault	R	0h	Parallel Detection Fault: 0h = No fault detected 1h = A fault has been detected during the parallel detection process
3	Link_Partner_Next_Page_Able	R	0h	Link Partner Next Page Ability: 0h = Link partner is not able to exchange next pages 1h = Link partner is able to exchange next pages
2	Local_Device_Next_Page_Able	R	1h	Next Page Ability: 0h = Local device is not able to exchange next pages 1h = Local device is able to exchange next pages
1	Page_Received	R	0h	Link Code Word Page Received: 0h = A new page has not been received 1h = A new page has been received
0	Link_Partner_Auto-Negotiation_Able	R	0h	Link Partner Auto-Negotiation Ability: 0h = Link partner does not support Auto-Negotiation 1h = Link partner supports Auto-Negotiation

6.6.8 ANNPTR_Register (Offset = 7h) [Reset = 2001h]

ANNPTR_Register is shown in 表 6-21.

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表 6-21. ANNPTR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0h	Next Page Indication: 0h = Do not advertise desire to send additional next pages 1h = Advertise desire to send additional next pages
14	RESERVED	R	0h	Reserved
13	Message_Page	R/W	1h	Message Page: 0h = Current page is an unformatted page 1h = Current page is a message page
12	Acknowledge_2	R/W	0h	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0h = Cannot comply with message 1h = Comply with message
11	Toggle	R	0h	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0h = Value of toggle bit in previously transmitted Link Code Word was 1 1h = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	CODE	R/W	1h	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. OtheR/Wise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

6.6.9 ANLNPTR_Register (Offset = 8h) [Reset = 0000h]

ANLNPTR_Register is shown in 表 6-22.

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表 6-22. ANLNPTR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R	0h	Next Page Indication: 0h = Do not advertise desire to send additional next pages 1h = Advertise desire to send additional next pages
14	Acknowledge	R	0h	Acknowledge: 0h = Link partner does not acknowledge reception of link code work 1h = Link partner acknowledges reception of link code word
13	Message_Page	R	0h	Message Page: 0h = Current page is an unformatted page 1h = Current page is a message page
12	Acknowledge_2	R	0h	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0h = Cannot comply with message 1h = Comply with message
11	Toggle	R	0h	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0h = Value of toggle bit in previously transmitted Link Code Word was 1 1h = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	Message/ Unformatted_Field	R	0h	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. OtheR/Wise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

6.6.10 CR1_Register (Offset = 9h) [Reset = 0000h]

CR1_Register is shown in 表 6-23.

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表 6-23. CR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	TDR_Auto-Run	R/W	0h	TDR Auto-Run at Link Down 0h = Disable automatic execution of TDR 1h = Enable execution of TDR procedure after link down event
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	robust_Auto_MDIX	R/W	0h	robust Auto-MDIX: If link partners are configured for operational modes that are not supported by normal Auto-MDIX, robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. 0h = Disable Auto-MDIX 1h = Enable robust Auto-MDIX
4	RESERVED	R	0h	Reserved
3-2	RESERVED	R	0h	Reserved

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表 6-23. CR1_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	Fast_RXDV_Detection	R/W	0h	Fast RXDV Detection: 0h = Disable Fast RX_DV detection. The PHY operates in normal mode. RX_DV assertion after detection of /JK/. 1h = Enable assertion high of RX_DV on receive packet due to detection of /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated.
0	RESERVED	R	0h	Reserved

6.6.11 CR2_Register (Offset = Ah) [Reset = 0100h]

CR2_Register is shown in 表 6-24.

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表 6-24. CR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	Extended_Full-Duplex_Ability	R/W	0h	Extended Full-Duplex Ability: 0h = Diable Extended Full-Duplex Ability. Decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification 1h = Enable Full-Duplex while working with link partner in forced 100Base-TX. When the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RX_ER_During_IDLE	R/W	0h	Detection of Receive Symbol error During IDLE State: 0h = Disable detection of Receive symbol error during IDLE state 1h = Enable detection of Receive symbol error during IDLE state
1	Odd-Nibble_Detection_Disable	R/W	0h	Detection of Transmit error: 0h = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle 1h = Disable detection of transmit error in odd-nibble boundary
0	RESERVED	R	0h	Reserved

6.6.12 CR3_Register (Offset = Bh) [Reset = 0000h]

CR3_Register is shown in 表 6-25.

Return to the Summary Table.

表 6-25. CR3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	Descrambler_Fast_Link_Down_Mode	R/W	0h	Descrambler Fast Link drop: This option can be enabled in parallel to the other fast link down modes in bits [3:0]. 0h = Do not drop the link on descrambler link loss 1h = Drop the link on descrambler link loss
9	RESERVED	R	0h	Reserved

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表 6-25. CR3_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	Polarity_Swap	R/W	0h	Polarity Swap: Port MirRr Function: To enable port mirRring, set this bit and bit [5] high. 1h = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0h = Normal polarity
5	MDI/MDIX_Swap	R/W	0h	MDI/MDIX Swap: Port MirRr Function: To enable port mirRring, set this bit and bit [6] high. 0h = MDI pairs normal (Receive on RD pair, Transmit on TD pair) 1h = Swap MDI pairs (Receive on TD pair, Transmit on RD pair)
4	RESERVED	R	0h	Reserved
3-0	Fast_Link_Down_Mode	R/W	0h	Fast Link Down Modes: a) Bit 3 drop the link based on RX error count of the MII interface. When a predefined number of 32 RX error occurences in a 10us interval is reached, the link is dropped. b) Bit 2 drop the link based on MLT3 error count (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 error occurences in10us interval is reached, the link is dropped. c) Bit 1 drop the link based on Low SNR Threshold. When a predefined number of 20 Threshold crossing occurences in a 10us interval is reached, the link is dropped. d) Bit 0 drop the link based on Signal/Energy Loss indication. When the Energy detector indicates Energy Loss, the link is dropped. Typical reaction time is 10us. The Fast Link Down function is an OR of all 5 options (bits [10] and [3:0]), the designer can enable any combination of these conditions.

6.6.13 Register_12 (Offset = Ch) [Reset = 0000h]

Register_12 is shown in 表 6-26.

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表 6-26. Register_12 Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_interrupt	RC	0h	interrupt for Link quality indication
14	energy_detect_interrupt	RC	0h	interrupt for energy detect indication
13	link_interrupt	RC	0h	Interrupt for link status
12	speed_interrupt	RC	0h	interrupt for speed status
11	duplex_interrupt	RC	0h	interrupt for duplex
10	auto_negotiation_complete_interrupt	RC	0h	interrupt for autonegotiation
9	false_carrier_half_full_interrupt	RC	0h	interrupt for false carrier
8	rhf_interrupt	RC	0h	interrupt for rhf
7	Link_Quality_interrupt_enable	R/W	0h	interrupt enable for Link quality indication
6	energy_detect_interrupt_enable	R/W	0h	interrupt enable for energy detect indication
5	link_interrupt_enable	R/W	0h	Interrupt enable for link status
4	speed_interrupt_enable	R/W	0h	interrupt enalble for speed status
3	duplex_interrupt_enable	R/W	0h	interrupt enable for duplex
2	auto_negotiation_complete_interrupt_enable	R/W	0h	interrupt enable for autonegotiation

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表 6-26. Register_12 Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	false_carrier_half_full_interrupt_enable	R/W	0h	interrupt enable for false carrier
0	rhf_interrupt_enable	R/W	0h	interrupt enable for rhf

6.6.14 REGCR_Register (Offset = Dh) [Reset = 0000h]

REGCR_Register is shown in 表 6-27.

Return to the Summary Table.

表 6-27. REGCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended_Register_Command	R/W	0h	Extended Register Command: 0h = Address 1h = Data, no post increment 2h = Data, post increment on read and write 3h = Data, post increment on write only
13-5	RESERVED	R	0h	Reserved
4-0	DEVAD	R/W	0h	Device Address: Bits [4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83825 uses the vendor specific DEVAD [4:0] = '11111' for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR must use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

6.6.15 ADDAR_Register (Offset = Eh) [Reset = 0000h]

ADDAR_Register is shown in 表 6-28.

Return to the Summary Table.

表 6-28. ADDAR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0h	If REGCR register bits [15:14] = '00', holds the MMD DEVAD's address register, otheR/Wise holds the MMD DEVAD's data.

6.6.16 FLDS_Register (Offset = Fh) [Reset = 0000h]

FLDS_Register is shown in 表 6-29.

Return to the Summary Table.

表 6-29. FLDS_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8-4	Fast_Link_Down_Status	R	0h	Fast Link Down Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled) 1h = Signal/Energy Lost 2h = SNR Level 4h = MLT3 Errors 8h = RX Errors 10h = Descrambler Loss Sync

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表 6-29. FLDS_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0h	Reserved

6.6.17 PHYSTS_Register (Offset = 10h) [Reset = 0000h]

PHYSTS_Register is shown in 表 6-30.

Return to the Summary Table.

表 6-30. PHYSTS_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	MDI/MDIX_Mode	R	0h	MDI/MDIX Mode Status: 0h = MDI Pairs normal (Receive on RD pair, Transmit on TD pair) 1h = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair)
13	Receive_error_Latch	R	0h	Receive error Latch: This bit is cleared upon a read of the RECR register 0h = No receive error event has occurred 1h = Receive error event has occurred since last read of RXERCNT register (0x0015)
12	Polarity_Status	R	0h	Polarity Status: This bit is a duplication of bit [4] in the 10BTSCR register (0x001A). This bit is cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 0h = Correct Polarity detected 1h = Inverted Polarity detected
11	False_Carrier_Sense_Latch	R	0h	False Carrier Sense Latch: This bit is cleared upon a read of the FCSR register. 0h = No False Carrier event has occurred 1h = False Carrier even has occurred since last read of FCSCR register (0x0014)
10	Signal_Detect	R	0h	Signal Detect: Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler_Lock	R	0h	Descrambler Lock: Active high 100Base-TX Descrambler Lock indication from PMD
8	Page_Received	R	0h	Link Code Word Page Received: This bit is a duplicate of Page Received (bit [1]) in the ANER register and it's cleared on read of the ANER register (0x0006). 0h = Link Code Word Page has not been received 1h = A new Link Code Word Page has been received
7	MII_Interrupt	R	0h	MII Interrupt Pending: Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR clears this interrupt bit indication. 0h = No interrupt pending 1h = Indicates that an internal interrupt is pending
6	Remote_Fault	R	0h	Remote Fault: Cleared on read of BMSR register (0x0001) or by reset. 1h = Remote Fault condition detected. Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation 0h = No Remote Fault condition detected
5	Jabber_Detect	R	0h	Jabber Detection: This bit is only for 10Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001) and is not cleared upon a read of the PHYSTS register. 0h = No Jabber 1h = Jabber condition detected
4	Auto-Negotiation_Status	R	0h	Auto-Negotiation Status: 0h = Auto-Negotiation not complete 1h = Auto-Negotiation complete

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表 6-30. PHYSTS_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	MII_Loopback_Status	R	0h	MII Loopback Status: 0h = Normal operation 1h = Loopback enabled
2	Duplex_Status	R	0h	Duplex Status: 0h = Half-Duplex mode 1h = Full-Duplex mode
1	Speed_Status	R	0h	Speed Status: 0h = 100Mbps mode 1h = 10Mbps mode
0	Link_Status	R	0h	Link Status: This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and is not cleared upon a read of the PHYSTS register. 0h = No link established 1h = Valid link established (for either 10Mbps or 100Mbps)

6.6.18 PHYSCR_Register (Offset = 11h) [Reset = 0108h]

PHYSCR_Register is shown in 表 6-31.

Return to the Summary Table.

表 6-31. PHYSCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable_PLL	R/W	0h	Disable PLL: Note: clock circuitry can be disabled only in IEEE power down mode. 0h = Normal operation 1h = Disable internal clocks circuitry
14	Power_Save_Mode_Enable	R/W	0h	Power Save Mode Enable: 0h = Normal operation 1h = Enable power save modes
13-12	Power_Save_Modes	R/W	0h	Power Save Mode: 0h = Normal operation mode. PHY is fully functional 1h = Reserved 2h = Active Sleep, Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
11	Scrambler_Bypass	R/W	0h	Scrambler Bypass: 0h = Scrambler bypass disabled 1h = Scrambler bypass enabled
10	RESERVED	R	0h	Reserved
9-8	Loopback_FIFO_Depth	R/W	1h	Far-End Loopback FIFO Depth: This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles. 0h = 4 nibbles FIFO 1h = 5 nibbles FIFO 2h = 6 nibbles FIFO 3h = 8 nibbles FIFO
7-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	Interrupt_Polarity	R/W	1h	Interrupt Polarity: 0h = Steady state (normal operation) is 0 logic and during interrupt is 1 logic 1h = Steady state (normal operation) is 1 logic and during interrupt is 0 logic

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表 6-31. PHYSCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	Test_Interrupt	R/W	0h	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts continue to be generated as long as this bit remains set. 0h = Do not generate interrupt 1h = Generate an interrupt
1	Interrupt_Enable	R/W	0h	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register (0x0012). 0h = Disable event based interrupts 1h = Enable event based interrupts
0	Interrupt_Output_Enable	R/W	0h	Interrupt Output Enable: Enable active low interrupt events via the INTR/PWERDN pin by configuring the INTR/PWRDN pin as an output. 0h = INTR/PWRDN is a Power Down pin 1h = INTR/PWRDN is an interrupt output

6.6.19 MISR1_Register (Offset = 12h) [Reset = 0000h]

MISR1_Register is shown in 表 6-32.

Return to the Summary Table.

表 6-32. MISR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_Interrupt	R	0h	Change of Link Quality Status Interrupt: 0h = Link quality is Good 1h = Change of link quality when link is ON
14	Energy_Detect_Interrupt	R	0h	Change of Energy Detection Status Interrupt: 0h = No change of energy detected 1h = Change of energy detected
13	Link_Status_Changed_Interrupt	R	0h	Change of Link Status Interrupt: 0h = No change of link status 1h = Change of link status interrupt is pending
12	Speed_Changed_Interrupt	R	0h	Change of Speed Status Interrupt: 0h = No change of speed status 1h = Change of speed status interrupt is pending
11	Duplex_Mode_Changed_Interrupt	R	0h	Change of Duplex Status Interrupt: 0h = No change of duplex status 1h = Change of duplex status interrupt is pending
10	Auto-Negotiation_Completed_Interrupt	R	0h	Auto-Negotiation Complete Interrupt: 0h = No Auto-Negotiation complete event is pending 1h = Auto-Negotiation complete interrupt is pending
9	False_Carrier_Counter_Half-Full_Interrupt	R	0h	False Carrier Counter Half-Full Interrupt: 0h = False Carrier half-full event is not pending 1h = False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending
8	Receive_error_Counter_Half-Full_Interrupt	R	0h	Receiver error Counter Half-Full Interrupt: 0h = Receive Error half-full event is not pending 1h = Receive Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending
7	Link_Quality_Interrupt_Enable	R/W	0h	Enable interrupt on change of link quality
6	Energy_Detect_Interrupt_Enable	R/W	0h	Enable interrupt on change of energy detection
5	Link_Status_Changed_Enable	R/W	0h	Enable interrupt on change of link status

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表 6-32. MISR1_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	Speed_Changed_Interrupt_Enable	R/W	0h	Enable Interrupt on change of speed status
3	Duplex_Mode_Changed_Interrupt_Enable	R/W	0h	Enable Interrupt on change of duplex status
2	Auto-Negotiation_Completed_Enable	R/W	0h	Enable Interrupt on Auto-negotiation complete event
1	False_Carrier_HF_Enable	R/W	0h	Enable Interrupt on False Carrier Counter Register half-full event
0	Receive_error_HF_Enable	R/W	0h	Enable Interrupt on Receive error Counter Register half-full event

6.6.20 MISR2_Register (Offset = 13h) [Reset = 0000h]

MISR2_Register is shown in 表 6-33.

Return to the Summary Table.

表 6-33. MISR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EEE_error_Interrupt	R	0h	Energy Efficient Ethernet error Interrupt: 0h = EEE error has not occurred 1h = EEE error has occurred
14	Auto-Negotiation_error_Interrupt	R	0h	Auto-Negotiation error Interrupt: 0h = No Auto-Negotiation error even pending 1h = Auto-Negotiation error interrupt is pending
13	Page_Received_Interrupt	R	0h	Page Receiver Interrupt: 0h = Page has not been received 1h = Page has been received
12	Loopback_FIFO_OF/UF_Event_Interrupt	R	0h	Loopback FIFO Overflow/Underflow Event Interrupt: 0h = No FIFO Overflow/Underflow event pending 1h = FIFO Overflow/Underflow event interrupt pending
11	MDI_CRssover_Change_Interrupt	R	0h	MDI/MDIX CRssover Status Change Interrupt: 0h = MDI crossover status has not changed 1h = MDI crossover status changed interrupt is pending
10	Sleep_Mode_Interrupt	R	0h	Sleep Mode Event Interrupt: 0h = No Sleep mode event pending 1h = Sleep mode event interrupt is pending
9	Inverted_Polarity_Interrupt__/_WoL_Packet_Received_Interrupt	R	0h	Inverted Polarity Interrupt / WoL Packet Received Interrupt: 0h = No Inverted polarity event pending / No WoL oacket received 1h = Inverted Polarity interrupt pending / WoL packet was recieved
8	Jabber_Detect_Interrupt	R	0h	Jabber Detect Event Interrupt: 0h = No Jabber detect event pending 1h = Jabber detect even interrupt pending
7	EEE_error_Interrupt_Enable	R/W	0h	Enable interrupt on EEE error
6	Auto-Negotiation_error_Interrupt_Enable	R/W	0h	Enable Interrupt on Auto-Negotiation error event
5	Page_Received_Interrupt_Enable	R/W	0h	Enable Interrupt on page receive event
4	Loopback_FIFO_OF/UF_Enable	R/W	0h	Enable Interrupt on loopback FIFO Overflow/Underflow event
3	MDI_CRssover_Change_Enable	R/W	0h	Enable Interrupt on change of MDI/X status

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表 6-33. MISR2_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	Sleep_Mode_Event_Enable	R/W	0h	Enable Interrupt on sleep mode event
1	Polarity_Changed_/_WoL_Packet_Enable	R/W	0h	Enable Interrupt on change of polarity status
0	Jabber_Detect_Enable	R/W	0h	Enable Interrupt on Jabber detection event

6.6.21 FCSCR_Register (Offset = 14h) [Reset = 0000h]

FCSCR_Register is shown in 表 6-34.

Return to the Summary Table.

表 6-34. FCSCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	False_Carrier_Event_Counter	R	0h	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter stops when the maximum count is reached (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

6.6.22 RECR_Register (Offset = 15h) [Reset = 0000h]

RECR_Register is shown in 表 6-35.

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表 6-35. RECR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive_error_Counter	R	0h	RX_ER Counter: When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when the maximum count is reached (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

6.6.23 BISCR_Register (Offset = 16h) [Reset = 0100h]

BISCR_Register is shown in 表 6-36.

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表 6-36. BISCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	BIST_error_Counter_Mode	R/W	0h	BIST error Counter Mode: 0h = Single mode, when BIST Error Counter reaches the max value, PRBS checker stops counting. 1h = Continuous mode, when the BIST Error counter reaches the max value, a pulse is generated and the counter starts counting from zeR again.

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表 6-36. BISCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
13	PRBS_Checker_Config	R/W	0h	PRBS Checker Config:bit[13:12] 0h = PRBS Generator and Checker both are disabled 1h = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 2h = PRBS Generation is disabled. PRBS Checker is Enabled 3h = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C
12	Packet_Generation_Enable	R/W	0h	Packet Generation Enable:bit[13:12] 0h = PRBS Generator and Checker both are disabled 1h = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 2h = PRBS Generation is disabled. PRBS Checker is Enabled 3h = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C
11	PRBS_Checker_Lock/Sync	R	0h	PRBS Checker Lock/Sync Indication: 0h = PRBS checker is not locked 1h = PRBS checker is locked and synced on received bit stream
10	PRBS_Checker_Sync_Loss	R	0h	PRBS Checker Sync Loss Indication: 0h = PRBS checker has not lost sync 1h = PRBS checker has lost sync
9	Packet_Generator_Status	R	0h	Packet Generation Status Indication: 0h = Packet Generator is off 1h = Packet Generator is active and generating packets
8	Power_Mode	R	1h	Sleep Mode Indication: 0h = Indicates that the PHY is in active sleep mode 1h = Indicates that the PHY is in normal power mode
7	RESERVED	R	0h	Reserved
6	Transmit_in_MII_Loopback	R/W	0h	Transmit Data in MII Loopback Mode (valid only at 100Mbps) 0h = Data is not transmitted to the line in MII loopback 1h = Enable transmission of data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit can be set only in MII Loopback mode - setting bit [14] in in BMCR register (0x0000)
5	RESERVED	R	0h	Reserved
4-0	Loopback_Mode	R/W	0h	Loopback Mode Select: The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83825 digital and analog data paths 1h = PCS Input Loopback (Use for 10Base-Te only) 2h = PCS Output Loopback 4h = Digital Loopback (Use for 100Base-TX Only) 8h = Analog Loopback (requires 100Ω termination) 10h = Reverse Loopback

6.6.24 RCSR_Register (Offset = 17h) [Reset = 0061h]

RCSR_Register is shown in 表 6-37.

Return to the Summary Table.

表 6-37. RCSR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved

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表 6-37. RCSR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
9	RESERVED	R	0h	Reserved
8	RMII_TX_Clock_Shift	R/W	0h	RMII TX Clock Shift: Applicable only in RMII Slave Mode 0h = Transmit path internal clock shift is disabled 1h = Transmit path internal clock shift is enabled
7	RMII_Clock_Select	R/W	0h	RMII Reference Clock Select: Strap (Master/Slave) determines the clock reference requirement. 0h = 25MHz clock reference, crystal or CMOS-level oscillator 1h = 50MHz clock reference, CMOS-level oscillator
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RMII_Revision_Select	R/W	0h	RMII Revision Select: 0h = (RMII revision 1.2) CRS_DV does toggle at the end of a packet to indicate de-assertion of CRS 1h = (RMII revision 1.0) CRS_DV remains asserted until final data is transferred. CRS_DV does not toggle at the end of a packet
3	RMII_Overflow_Status	RC	0h	RX FIFO Overflow Status: 0h = Normal 1h = Overflow detected
2	RMII_Underflow_Status	RC	0h	RX FIFO Underflow Status: 0h = Normal 1h = Underflow detected
1-0	Receive_Elasticity_Buffer_Size	R/W	1h	Receive Elasticity Buffer Size: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy. For greater frequency tolerance, the packet lengths can be scaled (for ±100ppm), divide the packet lengths by 2). 0h = 14 bit tolerance (up to 16800 byte packets) 1h = 2 bit tolerance (up to 2400 byte packets) 2h = 6 bit tolerance (up to 7200 byte packets) 3h = 10 bit tolerance (up to 12000 byte packets)

6.6.25 LEDCR_Register (Offset = 18h) [Reset = 0400h]

LEDCR_Register is shown in 表 6-38.

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表 6-38. LEDCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-9	Blink_Rate	R/W	2h	LED Blinking Rate (ON/OFF duration): 0h = 20Hz (50ms) 1h = 10Hz (100ms) 2h = 5Hz (200ms) 3h = 2Hz (500ms)
8	RESERVED	R	0h	Reserved
7	LED_Link_Polarity	R/W	0h	LED Link Polarity Setting: Link LED polarity defined by strapping value of this pin. This register allows for override of this strap value. 0h = Active Low polarity setting 1h = Active High polarity setting
6-5	RESERVED	R	0h	Reserved
4	Drive_Link_LED	R/W	0h	Drive Link LED Select: 0h = Normal operation 1h = Drive value of ON/OFF bit [1] onto LED_0 output pin

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表 6-38. LEDCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-2	RESERVED	R	0h	Reserved
1	Link_LED_ON/ OFF_Setting	R/W	0h	Value to force on Link LED output
0	RESERVED	R	0h	Reserved

6.6.26 PHYCR_Register (Offset = 19h) [Reset = 8000h]

PHYCR_Register is shown in 表 6-39.

Return to the Summary Table.

表 6-39. PHYCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Auto_MDI/X_Enable	R/W	1h	Auto-MDIX Enable: 0h = Disable Auto-Negotiation Auto-MDIX capability 1h = Enable Auto-Negotiation Auto-MDIX capability
14	Force_MDI/X	R/W	0h	Force MDIX: 0h = Normal operation (Receive on RD pair, Transmit on TD pair) 1h = Force MDI pairs to cRss (Receive on TD pair, Transmit on RD pair)
13	Pause_RX_Status	R	0h	Pause Receive Negotiation Status: Indicates that pause receive can be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause_TX_Status	R	0h	Pause Transmit Negotiated Status: Indicates that pause can be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function can be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
11	MII_Link_Status	R	0h	MII Link Status: 0h = No active 100Base-TX Full-Duplex link, established using Auto-Negotiation 1h = 100Base-TX Full-Duplex link is active and was established using Auto-Negotiation
10-8	RESERVED	R	0h	Reserved
7	Bypass_LED_Stretching	R/W	0h	Bypass LED Stretching: Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value. 0h = Normal LED operation 1h = Bypass LED stretching
6	RESERVED	R	0h	Reserved
5	LED_Configuration	R/W	0h	
4-0	PHY_Address	R	0h	PHY ADDRESS

6.6.27 10BTSCR_Register (Offset = 1Ah) [Reset = 0000h]

10BTSCR_Register is shown in 表 6-40.

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表 6-40. 10BTSCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved

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表 6-40. 10BTSCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
13	Receiver_Threshold_Enable	R/W	0h	Lower Receiver Threshold Enable: 0h = Normal 10Base-T operation 1h = Enable 10Base-T lower receiver threshold to allow operation with longer cables
12-9	Squelch	R/W	0h	Squelch Configuration: Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0h = 200mV 1h = 250mV 2h = 300mV 3h = 350mV 4h = 400mV 5h = 450mV 6h = 500mV 7h = 550mV 8h = 600mV
8	RESERVED	R	0h	Reserved
7	NLP_Disable	R/W	0h	NLP Transmission control: 0h = Enable transmission of NLPs 1h = Disable transmission of NLPs
6-5	RESERVED	R	0h	Reserved
4	Polarity_Status	R	0h	Polarity Status: This bit is a duplication of bit [12] in the PHYSTS register (0x0010). Both bits are cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 0h = Correct Polarity detected 1h = Inverted Polarity detected
3-1	RESERVED	R	0h	Reserved
0	Jabber_Disable	R/W	0h	Jabber Disable: Note: This function is only applicable in 10Base-Te operation. 0h = Jabber function enabled 1h = Jabber function disabled

6.6.28 BICSR1_Register (Offset = 1Bh) [Reset = 007Dh]

BICSR1_Register is shown in 表 6-41.

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表 6-41. BICSR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	BIST_error_Count	R	0h	BIST error Count: Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit [15]. When BIST error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) Note: Writing '1' to bit [15] locks the counter's value for successive read operation and clear the BIST error Counter.
7-0	BIST_IPG_Length	R/W	7Dh	BIST IPG Length: Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes*4 = 500 bytes). Binary values shall be multiplied by 4 to get the actual IPG length

6.6.29 BICSR2_Register (Offset = 1Ch) [Reset = 05EEh]

BICSR2_Register is shown in 表 6-42.

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表 6-42. BICSR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-0	BIST_Packet_Length	R/W	5EEh	BIST Packet Length: Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5DC, which is equal to 1500 bytes.

6.6.30 CDCR_Register (Offset = 1Eh) [Reset = 0000h]

CDCR_Register is shown in 表 6-43.

Return to the Summary Table.

表 6-43. CDCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Cable_Diagnostic_Start	R/W	0h	Cable Diagnostic process Start: Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered. 0h = Cable Diagnostic is disabled 1h = Start cable measurement
14	cfg_rescal_en	R/W	0h	Resistor calibration Start
13-2	RESERVED	R	0h	Reserved
1	Cable_Diagnostic_Status	R	0h	Cable Diagnostic process Done: 0h = Cable Diagnostic had not completed 1h = Indication that cable measurement process is complete
0	Cable_Diagnostic_Test_Fail	R	0h	Cable Diagnostic process Fail: 0h = Cable Diagnostic has not failed 1h = Indication that cable measurement process failed

6.6.31 PHYRCR_Register (Offset = 1Fh) [Reset = 0000h]

PHYRCR_Register is shown in 表 6-44.

Return to the Summary Table.

表 6-44. PHYRCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software_Hard_Reset	R/W	0h	Software Hard Reset: 0h = Normal Operation 1h = Reset PHY. This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital_reset	R/W	0h	Software Restart: 0h = Normal Operation 1h = Restart PHY. This bit is self cleared and resets all PHY circuitry except the registers.
13	RESERVED	R	0h	Reserved
12-0	RESERVED	R	0h	Reserved

6.6.32 MLEDCR_Register (Offset = 25h) [Reset = 0041h]

MLEDCR_Register is shown in 表 6-45.

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表 6-45. MLEDCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	MLED_Polarity_Swap	R/W	0h	MLED Polarity Swap: The polarity of MLED depends on the Ruting configuration and the strap on COL pin. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high.
8-7	RESERVED	R	0h	Reserved
6-3	LED_0_Configuration	R/W	8h	MLED Configurations: 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (EEE) Ch = TX/RX MII error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved
2-1	RESERVED	R	0h	Reserved
0	cfg_mled_en	R/W	1h	MLED Rute to LED_0: 0h = Link status Ruted to LED_0 1h = MLED Ruted to LED_0

6.6.33 COMPT_Regsiter Register (Offset = 27h) [Reset = 0000h]

COMPT_Regsiter is shown in 表 6-46.

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表 6-46. COMPT_Regsiter Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved

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表 6-46. COMPT_Regsiter Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	Compliance_Test_Configuration	R/W	0h	Compliance Test Configuration Select: Bit [4] in Register 0x0027 = 1, Enables 10Base-T Test Patterns Bit [4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits [3:0] select the 10Base-T test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10 ') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001 ' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' ... 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register Note 1: To reconfigure the 100Base-TX Test Mode, bit [4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. Note 2: When performing 100Base-TX or 10Base-T tests modes, the speed must be forced using the Basic Mode control Register (BMCR), address 0x0000.

6.6.34 Register_101 (Offset = 101h) [Reset = 2082h]

Register_101 is shown in 表 6-47.

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表 6-47. Register_101 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_energy_lost_th_normal	R/W	20h	DSP_ENERGY_THR_VAL register
7	cfg_dfe_freeze	R/W	1h	DSP_FRZ_CTRL_REGISTER
6-5	RESERVED	R	0h	Reserved
4	cfg_seq_wd_off	R/W	0h	WD_TIMER_CTRL Register
3-1	cfg_ss_bad_mse_tc_sel	R/W	1h	DSP_100M_MSE_TIMER VAL
0	cfg_use_nrg_det_le_only_as_int	R/W	0h	DSP_100M_CTRL register

6.6.35 Register_10a (Offset = 10Ah) [Reset = 2040h]

Register_10a is shown in 表 6-48.

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表 6-48. Register_10a Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_energy_window_len_normal	R/W	20h	DSP_100M_ENERGY_VAL Register
7-0	cfg_energy_on_th_normal	R/W	40h	DSP_ENERGY_THR_VAL register

6.6.36 Register_123 (Offset = 123h) [Reset = 051Ch]

Register_123 is shown in 表 6-49.

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表 6-49. Register_123 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	cfg_100m_mse_good2_th	R/W	51Ch	MSE threshold for loop convergence check

6.6.37 Register_130 (Offset = 130h) [Reset = 4F28h]

Register_130 is shown in 表 6-50.

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表 6-50. Register_130 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	cfg_100m_retrain_tc_sel	R/W	4h	Timer for gain recalibration
11	cfg_retrain_cagc_bypass	R/W	1h	Enable Gain recalibration
10	cfg_retrain_cagc_gear	R/W	1h	Gain recalibration step select
9	cfg_energy_lost_usec	R/W	1h	Trigger select for energy lost
8	cfg_energy_lost_clear_sel	R/W	1h	Selection for energy lost clr
7-0	cfg_seq_wd_sel	R/W	28h	WD Timer cnt sel

6.6.38 CDSCR_Register (Offset = 170h) [Reset = 0C12h]

CDSCR_Register is shown in 表 6-51.

Return to the Summary Table.

表 6-51. CDSCR_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Cable_Diagnostic_CRss_Disable	R/W	0h	CRss TDR Diagnostic Mode: 0h = TDR looks for reflections on channel other than the transmit channel configured by 0x170[13] 1h = TDR looks for reflections on same channel as transmit channel configured by 0x170[13]
13	cfg_tdr_chan_sel	R/W	0h	TDR TX channel select: 0h = Select channel A as transmit channel. 1h = Select channel B as transmit channel.
12	cfg_tdr_dc_rem_no_init	R/W	0h	To make sure DC removal module is not reset before TDR and dc removal is effective on TDR reflection

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表 6-51. CDSCR_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11	RESERVED	R	0h	Reserved
10-8	Cable_Diagnostic_Average_Cycles	R/W	4h	Number of TDR Cycles to Average: 0h = 1 TDR cycle 1h = 2 TDR cycles 2h = 4 TDR cycles 3h = 8 TDR cycles 4h = 16 TDR cycles 5h = 32 TDR cycles 6h = 64 TDR cycles 7h = Reserved
7	RESERVED	R	0h	Reserved
6-4	cfg_tdr_seg_num	R/W	1h	Selects cable segment on which TDR is to be performed - 000b = Reserved 001b = 0m to 10m 010b = 10m to 20m 011b = 20m to 40m 100b = 40m to 80m 101b = 80m and beyond 110b = Reserved 111b = Reserved
3-0	RESERVED	R	0h	Reserved

6.6.39 CDSCR2_Register (Offset = 171h) [Reset = C850h]

CDSCR2_Register is shown in 表 6-52.

Return to the Summary Table.

表 6-52. CDSCR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.40 TDR_172_Register (Offset = 172h) [Reset = 0000h]

TDR_172_Register is shown in 表 6-53.

Return to the Summary Table.

表 6-53. TDR_172_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.41 CDSCR3_Register (Offset = 173h) [Reset = 1304h]

CDSCR3_Register is shown in 表 6-54.

Return to the Summary Table.

表 6-54. CDSCR3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_tdr_seg_duration	R/W	13h	Duration of the segment selected for TDR, calculated by - (Length_in_meters*2*5.2)/8 For Segment #1, 8'hD For Segment #2, 8'hD For Segment #3, 8'h1A For Segment #4, 8'h34 For Segment #5, 8'h8F
7-0	cfg_tdr_initial_skip	R/W	4h	No of samples to be avoided before start of segment configured - For Segment #1, 8'h7 For Segment #2, 8'h14 For Segment #3, 8'h21 For Segment #4, 8'h3B For Segment #5, 8'h6F

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6.6.42 TDR_174_Register (Offset = 174h) [Reset = 0000h]

TDR_174_Register is shown in 表 6-55.

Return to the Summary Table.

表 6-55. TDR_174_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.43 TDR_175_Register (Offset = 175h) [Reset = 1004h]

TDR_175_Register is shown in 表 6-56.

Return to the Summary Table.

表 6-56. TDR_175_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-11	cfg_tdr_sdw_avg_loc	R/W	2h	TDR shadow average location - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h2
10-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	cfg_tdr_fwd_shadow	R/W	4h	Length of foR/Ward shadow for the segment configured (to avoid shadow of a fault peak be seen as another fault peak) - For Segment #1, 4'h4 For Segment #2, 4'h4 For Segment #3, 4'h5 For Segment #4, 4'h8 For Segment #5, 4'hB

6.6.44 TDR_176_Register (Offset = 176h) [Reset = 0005h]

TDR_176_Register is shown in 表 6-57.

Return to the Summary Table.

表 6-57. TDR_176_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4-0	cfg_tdr_p_loc_thresh_seg	R/W	5h	

6.6.45 CDSCR4_Register (Offset = 177h) [Reset = 1E00h]

CDSCR4_Register is shown in 表 6-58.

Return to the Summary Table.

表 6-58. CDSCR4_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	Short_Cables_Threshold	R/W	1Eh	TH to compensate for stRng reflections in short cables
7-0	RESERVED	R	0h	Reserved

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6.6.46 TDR_178_Register (Offset = 178h) [Reset = 0002h]

TDR_178_Register is shown in 表 6-59.

Return to the Summary Table.

表 6-59. TDR_178_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2-0	cfg_tdr_tx_pulse_width_seg	R/W	2h	TDR TX Pulse width for Segment - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h6

6.6.47 CDLRR1_Register (Offset = 180h) [Reset = 0000h]

CDLRR1_Register is shown in 表 6-60.

Return to the Summary Table.

表 6-60. CDLRR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	TD_Peak_Location_1	R	0h	Location of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

6.6.48 CDLRR2_Register (Offset = 181h) [Reset = 0000h]

CDLRR2_Register is shown in 表 6-61.

Return to the Summary Table.

表 6-61. CDLRR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.49 CDLRR3_Register (Offset = 182h) [Reset = 0000h]

CDLRR3_Register is shown in 表 6-62.

Return to the Summary Table.

表 6-62. CDLRR3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.50 CDLRR4_Register (Offset = 183h) [Reset = 0000h]

CDLRR4_Register is shown in 表 6-63.

Return to the Summary Table.

表 6-63. CDLRR4_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

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6.6.51 CDLRR5_Register (Offset = 184h) [Reset = 0000h]

CDLRR5_Register is shown in 表 6-64.

Return to the Summary Table.

表 6-64. CDLRR5_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.52 CDLAR1_Register (Offset = 185h) [Reset = 0000h]

CDLAR1_Register is shown in 表 6-65.

Return to the Summary Table.

表 6-65. CDLAR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-0	TD_Peak_Amplitude_1	R	0h	Amplitude of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

6.6.53 CDLAR2_Register (Offset = 186h) [Reset = 0000h]

CDLAR2_Register is shown in 表 6-66.

Return to the Summary Table.

表 6-66. CDLAR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.54 CDLAR3_Register (Offset = 187h) [Reset = 0000h]

CDLAR3_Register is shown in 表 6-67.

Return to the Summary Table.

表 6-67. CDLAR3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.55 CDLAR4_Register (Offset = 188h) [Reset = 0000h]

CDLAR4_Register is shown in 表 6-68.

Return to the Summary Table.

表 6-68. CDLAR4_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

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6.6.56 CDLAR5_Register (Offset = 189h) [Reset = 0000h]

CDLAR5_Register is shown in 表 6-69.

Return to the Summary Table.

表 6-69. CDLAR5_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

6.6.57 CDLAR6_Register (Offset = 18Ah) [Reset = 0000h]

CDLAR6_Register is shown in 表 6-70.

Return to the Summary Table.

表 6-70. CDLAR6_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	TD_Peak_Polarity_1	R	0h	Polarity of the First peak discovered by the TDR mechanism on Transmit Channel (TD).
10-6	RESERVED	R	0h	Reserved
5	CRss_Detect_on_TD	R	0h	CRss Reflections were detected on TD. Indicate on Short between TD and TD
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

6.6.58 IO_CFG_Register (Offset = 302h) [Reset = 0000h]

IO_CFG_Register is shown in 表 6-71.

Return to the Summary Table.

表 6-71. IO_CFG_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MaC_Impedance_control	R/W	0h	MAC Impedance control: MAC interface impedance control sets the series termination for the digital pins. 0h = 50 Ohms termination 1h = 25 Ohms termination
13	RESERVED	R	0h	Reserved
12-9	RESERVED	R	0h	Reserved
8	CRS_DV/RX_DV	R/W	0h	Valid in RMII mode. Configures the pin20 (CRS_DV) to function as RX_DV or CRS_DV (RX_DV + CRS) 0h = CRS_DV 1h = RX_DV
7	RESERVED	R	0h	Reserved
6	cfg_clkout25m_off	R/W	0h	This bit shall be set by Application to reduce the current consumption 0h = CLKOUT25 available 1h = LED_1_GPIO is available
5-0	RESERVED	R	0h	Reserved

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6.6.59 IO_CFG_2_Register (Offset = 305h) [Reset = 0008h]

IO_CFG_2_Register is shown in 表 6-72.

Return to the Summary Table.

表 6-72. IO_CFG_2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-3	RESERVED	R	0h	Reserved
2-0	Pin2_GPIO_Configuration	R/W	0h	GPIO Configuration: 0h = clkout50m (only in master mode) 1h = LED_2 2h = WoL 3h = 0 4h = MDINT 5h = 0 6h = 1 7h = 0

6.6.60 SPARE_OUT Register (Offset = 308h) [Reset = 0002h]

SPARE_OUT is shown in 表 6-73.

Return to the Summary Table.

表 6-73. SPARE_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	spare_out	R/W	1h	Analog Spare Bits Bit 1 - Tied to 1'b1 to act as revision ID Bit 2 - cfg_rmii_rx_clk_sel Bit 4 - Freeze all loops when rx_is_dis is high Bit 5: Bypass MSE checker in LPI_WAKE state Bit 6 - Enable freeze in STEADY_STATE before entering LPI_FREEZE Bit 7: Enable counter based Freeze mechanism for LPI Freeze cycle Bit 8: Choose tmer of 176us/192us for the Counter based Freeze during LPI refresh cycle Bit 10 - Freeze fagc in LPI_WAIT Bit 11 - Freeze ffe in LPI_WAIT Bit 12 - Freeze dfe in LPI_WAIT Bit 13 - Freeze kp loop in LPI_WAIT Bit 14 - Freeze kf loop in LPI_WAIT Bit 15 - Freeze dc removal in LPI_WAIT
0	cfg_clkout_25m_off_status	R	0h	This bit is applicable in DP83825 only. And is only R 0h = CLKOUT25 available 1h = LED_1_GPIO is available and is controlled by digpad3_3_gpio_ctrl

6.6.61 DAC_CFG_0 Register (Offset = 30Bh) [Reset = 0C00h]

DAC_CFG_0 is shown in 表 6-74.

Return to the Summary Table.

表 6-74. DAC_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-6	cfg_dac_minus_one_val	R/W	30h	LD data for mlt3 encoded data of minus one
5-0	cfg_dac_zeR_val	R/W	0h	LD data for mlt3 encoded data of zeR

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6.6.62 DAC_CFG_1 Register (Offset = 30Ch) [Reset = 0020h]

DAC_CFG_1 is shown in 表 6-75.

Return to the Summary Table.

表 6-75. DAC_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-0	cfg_dac_plus_one_val	R/W	20h	LD data for mlt3 encoded data of plus one

6.6.63 DSP_CFG_0 Register (Offset = 30Fh) [Reset = 0464h]

DSP_CFG_0 is shown in 表 6-76.

Return to the Summary Table.

表 6-76. DSP_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-8	cfg_100m_ffe1_tc_sel	R/W	4h	Timer for FFE_1 State
7	cfg_ffe1_freeze	R/W	0h	Freeze FFE option in FFE_1 State. 1 -> Freeze.
6	cfg_ffe2_freeze	R/W	1h	Freeze FFE option in FFE_2 State. 1 -> Freeze.
5	cfg_ffe3_freeze	R/W	1h	Freeze FFE option in FFE_3 State. 1 -> Freeze.
4-2	cfg_deq_thr_check_en	R/W	1h	Enable bits for different metric checks during DEQ sweep. cfg_deq_thr_check_en[0] -> Enables DFE Coeff thr check. cfg_deq_thr_check_en[1] -> Enables MSE thr check. cfg_deq_thr_check_en[2] -> Enables pre-cursor value thr check.
1	cfg_tloop_freqacc_clr_deq sweep	R/W	0h	Option to re-initialize tloop freq acc during DEQ sweep iterations.
0	cfg_dfe_reset_deqsweep	R/W	0h	Option to reset DFE Coeff during DEQ sweep iterations.

6.6.64 DSP_CFG_2 Register (Offset = 311h) [Reset = 01FCh]

DSP_CFG_2 is shown in 表 6-77.

Return to the Summary Table.

表 6-77. DSP_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	cfg_cagc_gain_mapping_s el	R/W	0h	Option to select different combinations of BPF, PGA gain by CAGC. 0 -> default option. Other options are 1 and 2. (There are only 3 options.)
13	cfg_deq_coeff_sel	R/W	0h	Equalization mode ctrl register 0h = Coefficients for less pre-cursor. 1h = DEQ Coefficients from Table 2 (LS)
12-9	RESERVED	R	0h	Reserved
8-1	cfg_deq_coeff_0_val_1	R/W	FEh	Equalization Force coefficient_0 Value for CabeLength < 75m
0	RESERVED	R	0h	Reserved

6.6.65 DSP_CFG_4 Register (Offset = 313h) [Reset = 06F8h]

DSP_CFG_4 is shown in 表 6-78.

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Return to the Summary Table.

表 6-78. DSP_CFG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_deq_coeff_0_val_4	R/W	6h	Equalization Force coefficient_0 Value for CabeLength >130m
7-0	cfg_deq_coeff_1_val_1	R/W	F8h	Equalization Force coefficient_1 Value for CabeLength < 75m

6.6.66 DSP_CFG_13 Register (Offset = 31Ch) [Reset = 1101h]

DSP_CFG_13 is shown in 表 6-79.

Return to the Summary Table.

表 6-79. DSP_CFG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_kp_force_en	R/W	0h	Enable forcing of timing loop pRp arm gain
14	cfg_kf_force_en	R/W	0h	Enable forcing of timing loop integral arm gain
13-11	cfg_kp_force_val	R/W	2h	Value to force for timing loop pRp arm gain
10-7	cfg_kf_force_val	R/W	2h	Value to force for timing loop integral arm gain
6	cfg_kp_freeze_en	R/W	0h	Enable to freeze pRp arm
5	cfg_kp_freeze_val	R/W	0h	Value to freeze pRp arm. 0h = unfreeze 1h = freeze;
4	cfg_kf_freeze_en	R/W	0h	Enable to freeze integral arm
3	cfg_kf_freeze_val	R/W	0h	Value to freeze integral arm. 0h = unfreeze 1h = freeze
2	cfg_pd_pol	R/W	0h	TED polarity inversion
1	cfg_energy_det_in_sel	R/W	0h	Option to select input for Energy Calc. 0h = Slicer inp (default) 1h = ADC out (no DC)
0	cfg_compute_pre_cursor_metric_en	R/W	1h	Enable pre cursor metric calculation

6.6.67 DSP_CFG_16 Register (Offset = 31Fh) [Reset = FC36h]

DSP_CFG_16 is shown in 表 6-80.

Return to the Summary Table.

表 6-80. DSP_CFG_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	cfg_100m_frz_frz	R/W	1Fh	Freeze cmd at Seq State : LPI_FREEZE by gRups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
10-6	cfg_100m_wake_frz	R/W	10h	Freeze cmd at Seq State : LPI_Wake, by gRups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
5-1	cfg_100m_flush_frz	R/W	1Bh	Freeze cmd at Seq State : LPI_Wake, by gRups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
0	RESERVED	R	0h	Reserved

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6.6.68 DSP_CFG_25 Register (Offset = 33Ch) [Reset = EC00h]

DSP_CFG_25 is shown in 表 6-81.

Return to the Summary Table.

表 6-81. DSP_CFG_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	deq_coeff_1	R	ECh	Reserved
7	RESERVED	R	0h	Reserved
6-0	cfg_deq_coeff_force	R/W	0h	EQUALIZATION_FRC_CTRL REGISTER

6.6.69 DSP_CFG_27 Register (Offset = 33Eh) [Reset = 261Eh]

DSP_CFG_27 is shown in 表 6-82.

Return to the Summary Table.

表 6-82. DSP_CFG_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_wait_lpi_el_dis	R/W	0h	EEE_WAKE_CTRL register
14-13	cfg_dfe_coeff_lim_sel	R/W	1h	Enable limit on the max limit of dfe coefficient
12-8	cfg_dfe_coeff_lim_val	R/W	6h	Limit value for dfe coefficeint
7	cfg_wait_lpi_ed_dis	R	0h	EEE_WAKE_CTRL register
6	cfg_mse_th_scaled_en	R/W	0h	Enable scaling of mse threshold based on PGA gain for DEQ sweep
5	cfg_dfe_th_scaled_en	R/W	0h	Enable scaling of dfe threshold based on PGA gain for DEQ sweep
4-0	cfg_dfe_mse_th_offset	R/W	1Eh	Offset to be added to PGA attenuation level used for scaling of mse and dfe thresholds

6.6.70 ANA_LD_PRG_SL_Register (Offset = 404h) [Reset = 0080h]

ANA_LD_PRG_SL_Register is shown in 表 6-83.

Return to the Summary Table.

表 6-83. ANA_LD_PRG_SL_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ld_pRg_sl	R/W	80h	<15:12> ld_bias <11:8> cm_control: debug mode for changing output common mode <7:5> iq_control: ld power consumption - 000-12.7mA; 100:15.7mA; 111:19.5mA <4:0> unused <0>ld_burnin_mode

6.6.71 ANA_RX10BT_CTRL_Register (Offset = 40Dh) [Reset = 0000h]

ANA_RX10BT_CTRL_Register is shown in 表 6-84.

Return to the Summary Table.

表 6-84. ANA_RX10BT_CTRL_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4-0	rx10bt_comp_sl	R/W	0h	10B-T current Gain, common for both POS and NEG, Starting from 200mV to 575mV, step size of 25mV PG1.1 change : Bit 3 is internally inverted

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6.6.72 Register_416 (Offset = 416h) [Reset = 083Ch]

Register_416 is shown in 表 6-85.

Return to the Summary Table.

表 6-85. Register_416 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	hpf_cal_force_ctrl	R/W	0h	ANA RX PATH CTRL REGISTER
11-8	hpf_cal_sl	R/W	8h	Reserved
7	hpf_gain_force_ctrl	R/W	0h	ANA RX PATH CTRL REGISTER
6	RESERVED	R	0h	Reserved
5-4	hpf_gain_sl	R/W	3h	ANA RX PATH CTRL REGISTER
3-2	RESERVED	R	0h	Reserved
1	hpf_en_force_ctrl	R/W	0h	ANA RX PATH CTRL REGISTER
0	hpf_en_sl	R/W	0h	ANA RX PATH CTRL REGISTER

6.6.73 Register_429 (Offset = 429h) [Reset = 0000h]

Register_429 is shown in 表 6-86.

Return to the Summary Table.

表 6-86. Register_429 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	top_pRg_vbgbyr_control	R/W	0h	IVBGR_CTRL register
7-0	RESERVED	R	0h	Reserved

6.6.74 GENCFG_Register (Offset = 456h) [Reset = 0008h]

GENCFG_Register is shown in 表 6-87.

Return to the Summary Table.

表 6-87. GENCFG_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	Min_IPG_Enable	R/W	1h	Min IPG Enable: 0h = IPG set to 0.20µs 1h = Enable Minimum Interpacket Gap (IPG is set to 120ns instead of 0.20µs)
2-0	RESERVED	R	0h	Reserved

6.6.75 LEDCFG_Register (Offset = 460h) [Reset = 0515h]

LEDCFG_Register is shown in 表 6-88.

Return to the Summary Table.

表 6-88. LEDCFG_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-8	RESERVED	R	0h	Reserved

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表 6-88. LEDCFG_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
7-4	LED_2_control	R/W	1h	LED_2 control:Selects the source for LED_2. 0h = LINK OK 1h = RX/TX Activity 2h = TX Activity 3h = RX Activity 4h = Collision 5h = Speed, High for 100BASE-TX 6h = Speed, High for 10BASE-T 7h = Full-Duplex 8h = LINK OK / BLINK on TX/RX Activity 9h = Active Stretch Signal Ah = MII LINK (100BT+FD) Bh = LPI Mode (Energy Efficient Ethernet) Ch = TX/RX MII error Dh = Link Lost (remains on until register 0x0001 is read) Eh = Blink for PRBS error (remains ON for single error, remains until counter is cleared) Fh = Reserved
3-0	RESERVED	R	0h	Reserved

6.6.76 IOCTRL_Register (Offset = 461h) [Reset = 0010h]

IOCTRL_Register is shown in 表 6-89.

Return to the Summary Table.

表 6-89. IOCTRL_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10-7	RESERVED	R	0h	Reserved
6-5	RESERVED	R	0h	Reserved
4-0	RESERVED	R	0h	Reserved

6.6.77 SOR1_Register (Offset = 467h) [Reset = 0533h]

SOR1_Register is shown in 表 6-90.

Return to the Summary Table.

表 6-90. SOR1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	CRS_DV/RX_DV	R	0h	Reserved
13	CFG_PHY_AD_1	R	0h	Latched Value of PhyAddress[1]
12	CFG_PHY_AD_0	R	0h	Latched Value of PhyAddress[0]
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	CFG_AMDIX	R	1h	1 = Auto MDI 0 = Manual MDI
7	RESERVED	R	0h	Reserved

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表 6-90. SOR1_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	CFG_RMII_Master/Slave	R	0h	0 = RMII Master : 25MHz clock reference at XI 1 = RMII Slave : 50MHz clock reference at XI
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	Autonegotiation_enable	R	1h	1: Auto Neg Enable 0: Auto Neg Disable

6.6.78 SOR2_Register (Offset = 468h) [Reset = 1290h]

SOR2_Register is shown in 表 6-91.

Return to the Summary Table.

表 6-91. SOR2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	CRS_DV_vs_RX_DV	R	0h	
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	CFG_LED_LINK_POL	R	1h	1 = LED_LINK is active high 0 = LED_LINK is active low
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

6.6.79 Register_0x469_Register (Offset = 469h) [Reset = 0040h]

Register_0x469_Register is shown in 表 6-92.

Return to the Summary Table.

表 6-92. Register_0x469_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	led_2_polarity	R/W	1h	led 2 polarity 0h = active low, 1h = active high

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表 6-92. Register_0x469_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	led_2_drv_val	R/W	0h	led 2 drive value
4	led_2_drv_en	R/W	0h	led 2 drive enable 0h = Normal operation 1h = drive LED polarity,
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

6.6.80 RXFCFG_Register (Offset = 4A0h) [Reset = 1081h]

RXFCFG_Register is shown in 表 6-93.

Return to the Summary Table.

表 6-93. RXFCFG_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	CRC_Gate	R/W	1h	CRC Gate: If Magic Packet has Bad CRC there is no indication (status, interrupt, GPIO) when enabled. 0h = Bad CRC does not gate Magic Packet or Pattern Indications 1h = Bad CRC gates Magic Packet and Pattern Indications
11	WoL_Level_Change_Indication_Clear	W	0h	WoL Level Change Indication Clear: If WoL Indication is set for Level change mode, this bit clears the level upon a write. 0h = Clear
10-9	WoL_Pulse_Indication_Select	R/W	0h	WoL Pulse Indication Select: Only valid when WoL Indication is set for Pulse mode. 0h = 8 clock cycles (of 125MHz clock) 1h = 16 clock cycles 2h = 32 clock cycles 3h = 64 clock cycles
8	WoL_Indication_Select	R/W	0h	WoL Indication Select: 0h = Pulse mode 1h = Level change mode
7	WoL_Enable	R/W	1h	WoL Enable: 0h = normal operation 1h = Enable Wake-on-LAN (WoL)
6	Bit_Mask_Flag	R/W	0h	Bit Mask Flag
5	Secure-ON_Enable	R/W	0h	Enable Secure-ON password for Magic Packets
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	WoL_Magic_Packet_Enable	R/W	1h	Enable Interrupt upon reception of Magic Packet

6.6.81 RXFS_Register (Offset = 4A1h) [Reset = 1000h]

RXFS_Register is shown in 表 6-94.

Return to the Summary Table.

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表 6-94. RXFS_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	WoL_Interrupt_Source	R/W	1h	WoL Interrupt Source: Source of Interrupt for bit [1] of register 0x0013. When enabling WoL, this bit is automatically set to WoL Interrupt. 0h = Data Polarity Interrupt 1h = WoL Interrupt
11-8	RESERVED	R	0h	Reserved
7	SFD_error	RC	0h	SFD error: 0h = No SFD error 1h = Packet with SFD error (without the SFD byte indicated in bit [13] register 0x04A0)
6	Bad_CRC	RC	0h	Bad CRC: 0h = No bad CRC received 1h = Bad CRC was received
5	Secure-On_Hack_Flag	RC	0h	Secure-ON Hack Flag: 0h = Valid Secure-ON Password 1h = Invalid Password detected in Magic Packet
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	WoL_Magic_Packet_Status	RC	0h	WoL Magic Packet Status:

6.6.82 RXFPMD1_Register (Offset = 4A2h) [Reset = 0000h]

RXFPMD1_Register is shown in 表 6-95.

Return to the Summary Table.

表 6-95. RXFPMD1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_4	R/W	0h	Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_5__MSB	R/W	0h	Match Data: Configured for MAC Destination Address

6.6.83 RXFPMD2_Register (Offset = 4A3h) [Reset = 0000h]

RXFPMD2_Register is shown in 表 6-96.

Return to the Summary Table.

表 6-96. RXFPMD2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_2	R/W	0h	Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_3	R/W	0h	Match Data: Configured for MAC Destination Address

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6.6.84 RXFPMD3_Register (Offset = 4A4h) [Reset = 0000h]

RXFPMD3_Register is shown in 表 6-97.

Return to the Summary Table.

表 6-97. RXFPMD3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_0	R/W	0h	Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_1	R/W	0h	Match Data: Configured for MAC Destination Address

6.6.85 Register_0x4cd (Offset = 4CDh) [Reset = 0408h]

Register_0x4cd is shown in 表 6-98.

Return to the Summary Table.

表 6-98. Register_0x4cd Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_lpi_energy_lost_th	R/W	4h	CFG_EEE_ENERGY_CTRL register
7-0	cfg_lpi_energy_on_th	R/W	8h	CFG_EEE_ENERGY_CTRL register

6.6.86 Register_0x4ce (Offset = 4CEh) [Reset = 0012h]

Register_0x4ce is shown in 表 6-99.

Return to the Summary Table.

表 6-99. Register_0x4ce Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	cfg_lpi_energy_window_len	R/W	12h	CFG_EEE_ENERGY_CTRL register

6.6.87 Register_0x4cf (Offset = 4CFh) [Reset = 261Dh]

Register_0x4cf is shown in 表 6-100.

Return to the Summary Table.

表 6-100. Register_0x4cf Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_sd_on_win_len	R/W	2h	EEE_WAKE_CTRL register
11-8	cfg_100m_tloop_kf_step_ss	R/W	6h	DSP100M_TLOOP_CTRL register
7-4	cfg_sd_on_thr_100m	R/W	1h	Reserved
3	cfg_100m_use_sd_en	R/W	1h	Reserved
2	cfg_sd_cnt_level	R/W	1h	Reserved
1	cfg_en_zc_cnt	R/W	0h	Reserved
0	cfg_en_cmp_cnt	R/W	1h	Reserved

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6.6.88 EEECFG2_Register (Offset = 4D0h) [Reset = 0302h]

EEECFG2_Register is shown in 表 6-101.

Return to the Summary Table.

表 6-101. EEECFG2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-7	RESERVED	R	0h	Reserved
6-5	RESERVED	R	0h	Reserved
4-0	RESERVED	R	0h	Reserved

6.6.89 EEECFG3_Register (Offset = 4D1h) [Reset = 018Bh]

EEECFG3_Register is shown in 表 6-102.

Return to the Summary Table.

表 6-102. EEECFG3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-13	Force_EEE_Enable	R/W	0h	Force EEE: Note: Both Link Partners need to be configured to Force EEE. 0h = EEE Force Mode OFF 1h = Reserved0 2h = Reserved1 3h = EEE Forced LPI Enabled
12	Force_LPI_Request_TX	R/W	0h	Force LPI Request TX: This bit shall be set after setting bits [14:13] to EEE Force LPI Enabled. 0h = normal operation 1h = Force LPI request on transmit enabled
11	RESERVED	R	0h	Reserved
10	cfg_dis_lpi_bypass_rvrs_loop	R/W	0h	Energy Efficient Ethernet Configuration Register #3
9	cfg_dis_lpi_bypass_fifo	R/W	0h	Energy Efficient Ethernet Configuration Register #3
8	cfg_100m_en_lpi_wake_fallback	R/W	1h	Energy Efficient Ethernet Configuration Register #3
7-4	cfg_lpi_mse_timer_tc_val	R/W	8h	Energy Efficient Ethernet Configuration Register #3
3	EEE_Capabilities_Bypass	R/W	1h	EEE Advertise Option: Allow for EEE Advertisment during Auto-Negotiation to be determined by bit [0] in register 0x04D1 rather than the Next Page Registers (Register 0x003C and Register 0x003D in MMD7). 0h = Bit [0] determines EEE Auto-Negotiation Abilities 1h = Registers in MMD3 and MMD7 determine EEE Auto-Negotiation Abilities
2	EEE_Next_Page_Disable	R/W	0h	EEE Next Page Disable: 0h = Reception of EEE Next Pages is enabled 1h = Reception of EEE Next Pages is disabled
1	EEE_RX_Path_Shutdown	R/W	1h	EEE RX Path Shutdown: 0h = Analog RX path is active during LPI_Quiet 1h = Enable shutdown of Analog RX path at LPI_Quiet

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表 6-102. EEECFG3_Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	EEE_Capabilities_Enable	R	1h	EEE Capabilities Disable 0h = PHY support EEE capability, Auto-Negotiation negotiates to EEE as defined by Register 0x003C and Register 0x003D in MMD7. 1h = PHY does not support EEE (Register 0x0014 in MMD3, Register 0x003C and Register 0x003D in MMD7 are ignored)

6.6.90 Register_0x4d2 (Offset = 4D2h) [Reset = 354Ah]

Register_0x4d2 is shown in 表 6-103.

Return to the Summary Table.

表 6-103. Register_0x4d2 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	cfg_flush_ph_shift_updn	R/W	0h	PI_CTRL Register
13	cfg_ph_shift_toggle_en	R/W	1h	PI_CTRL Register
12	cfg_fast_slave_wake_100	R/W	1h	DSP_100M_EEE_LINK CTRL register
11	cfg_dis_dscr_100_tout	R/W	0h	DSP_100M_EEE_LINK CTRL register
10	cfg_lpi_pre_flush_en	R/W	1h	DSP_EEE_SEQ CTRL register
9-5	cfg_100m_rx_lpi_ts_timer	R/W	Ah	DSP_100M_EEE_LINK CTRL register
4-0	cfg_100m_rx_lpi_link_fail	R/W	Ah	DSP_100M_EEE_LINK CTRL register

6.6.91 Register_0x4d4 (Offset = 4D4h) [Reset = 6633h]

Register_0x4d4 is shown in 表 6-104.

Return to the Summary Table.

表 6-104. Register_0x4d4 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	cfg_100m_tloop_kp_step_1	R/W	6h	DSP_100M_STEP_1_Register
11	RESERVED	R	0h	Reserved
10-8	cfg_100m_tloop_kp_step_0	R/W	6h	DSP_100M_STEP_0_Register
7	RESERVED	R	0h	Reserved
6-4	cfg_100m_tloop_kf_step_1	R/W	3h	DSP_100M_STEP_1_Register
3	RESERVED	R	0h	Reserved
2-0	cfg_100m_tloop_kf_step_0	R/W	3h	DSP_100M_STEP_0_Register

6.6.92 DSP_100M_STEP_2_Register (Offset = 4D5h) [Reset = 02F1h]

DSP_100M_STEP_2_Register is shown in 表 6-105.

Return to the Summary Table.

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表 6-105. DSP_100M_STEP_2_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-7	cfg_100m_tloop_kp_step_2	R/W	5h	DSP_100M_STEP_2 Register
6-4	cfg_100m_tloop_kf_step_2	R/W	7h	DSP_100M_STEP_2 Register
3-2	cfg_100m_mse_step_2	R/W	0h	DSP_100M_STEP_2 Register
1	cfg_100m_dfe_step_2	R/W	0h	DSP_100M_STEP_2 Register
0	cfg_100m_fagc_step_2	R/W	1h	DSP_100M_STEP_2 Register

6.6.93 DSP_100M_STEP_3_Register (Offset = 4D6h) [Reset = 0171h]

DSP_100M_STEP_3_Register is shown in 表 6-106.

Return to the Summary Table.

表 6-106. DSP_100M_STEP_3_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-7	cfg_100m_tloop_kp_step_3	R/W	2h	DSP_100M_STEP_3 Register
6-4	cfg_100m_tloop_kf_step_3	R/W	7h	DSP_100M_STEP_3 Register
3-2	cfg_100m_mse_step_3	R/W	0h	DSP_100M_STEP_3 Register
1	cfg_100m_dfe_step_3	R/W	0h	DSP_100M_STEP_3 Register
0	cfg_100m_fagc_step_3	R/W	1h	DSP_100M_STEP_3 Register

6.6.94 DSP_100M_STEP_4_Register (Offset = 4D7h) [Reset = 0171h]

DSP_100M_STEP_4_Register is shown in 表 6-107.

Return to the Summary Table.

表 6-107. DSP_100M_STEP_4_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-7	cfg_100m_tloop_kp_step_4	R/W	2h	DSP_100M_STEP_4 Register
6-4	cfg_100m_tloop_kf_step_4	R/W	7h	DSP_100M_STEP_4 Register
3-2	cfg_100m_mse_step_4	R/W	0h	DSP_100M_STEP_4 Register
1	cfg_100m_dfe_step_4	R/W	0h	DSP_100M_STEP_4 Register
0	cfg_100m_fagc_step_4	R/W	1h	DSP_100M_STEP_4 Register

6.6.95 MMD3_PCS_CTRL_1_Register (Offset = 1000h) [Reset = 4000h]

MMD3_PCS_CTRL_1_Register is shown in 表 6-108.

Return to the Summary Table.

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表 6-108. MMD3_PCS_CTRL_1_Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS_Reset	R/W	0h	PCS Reset: Reset clears MMD3, MMD7 and PCS registers. Reset does not clear Vendor Specific Registers (DEVAD = 31). 0h = Normal operation 1h = Soft Reset of MMD3, MMD7 and PCS registers
14-11	RESERVED	R	0h	Reserved
10	RX_Clock_Stoppable	R/W	0h	RX Clock Stoppable: 0h = Receive Clock not stoppable 1h = Receive Clock stoppable during LPI
9-0	RESERVED	R	0h	Reserved

6.6.96 MMD3_PCS_STATUS_1 Register (Offset = 1001h) [Reset = 0040h]

MMD3_PCS_STATUS_1 is shown in 表 6-109.

Return to the Summary Table.

表 6-109. MMD3_PCS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	TX_LPI_Received	R	0h	TX LPI Received: 0h = LPI not received 1h = TX PCS has received LPI
10	RX_LPI_Received	R	0h	RX LPI Received: 0h = LPI not received 1h = RX PCS has received LPI
9	TX_LPI_Indication	R	0h	TX LPI Indication: 0h = TX PCS is not currently receiving LPI 1h = TX PCS is currently receiving LPI
8	RX_LPI_Indication	R	0h	RX LPI Indication: 0h = RX PCS is not currenly receiving LPI 1h = RX PCS is currently receiving LPI
7	RESERVED	R	0h	Reserved
6	TX_Clock_Stoppable	R	1h	TX Clock Stoppable: 0h = TX Clock is not stoppable 1h = MAC can stop clock during LPI
5-0	RESERVED	R	0h	Reserved

6.6.97 MMD3_EEE_CAPABILITY_Register (Offset = 1014h) [Reset = 0002h]

MMD3_EEE_CAPABILITY_Register is shown in 表 6-110.

Return to the Summary Table.

表 6-110. MMD3_EEE_CAPABILITY_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	EEE_1Gbps_Enable	R	0h	EEE 1Gbps Enable: 0h = EEE is not supported for 1000Base-T 1h = EEE is supported for 1000Base-T
1	EEE_100Mbps_Enable	R	1h	EEE 100Mbps Enable: 0h = EEE is not supported for 100Base-TX 1h = EEE is supported for 100Base-TX
0	RESERVED	R	0h	Reserved

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6.6.98 MMD3_WAKE_ERR_CNT_Register (Offset = 1016h) [Reset = 0000h]

MMD3_WAKE_ERR_CNT_Register is shown in 表 6-111.

Return to the Summary Table.

表 6-111. MMD3_WAKE_ERR_CNT_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	EEE_Wake_error_Counter	R	0h	EEE Wake error Counter: This register counts the wake time faults where the PHY fails to complete the normal wake sequence within the time requiered for the specific PHY type. This counter is cleared after a read and holds at all ones in the case of overflow. PCS Reset also clears this register

6.6.99 MMD7_EEE_ADVERTISEMENT_Register (Offset = 203Ch) [Reset = 0000h]

MMD7_EEE_ADVERTISEMENT_Register is shown in 表 6-112.

Return to the Summary Table.

表 6-112. MMD7_EEE_ADVERTISEMENT_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	Advertise_100Base-TX_EEE	R/W	0h	Advertise 100Base-TX EEE: 0h = Energy Efficient Ethernet is not advertised 1h = Energy Efficient Ethernet is advertised for 100Base-TX
0	RESERVED	R	0h	Reserved

6.6.100 MMD7_EEE_LP_ABILITY_Register (Offset = 203Dh) [Reset = 0000h]

MMD7_EEE_LP_ABILITY_Register is shown in 表 6-113.

Return to the Summary Table.

表 6-113. MMD7_EEE_LP_ABILITY_Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	Link_Partner_EEE_Capability	R	0h	Link Partner EEE Capability: 0h = Link Partner is not advertising EEE capability for 100Base-TX 1h = Link Partner is advertising EEE capability for 100Base-TX
0	RESERVED	R	0h	Reserved

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DP83825I is a single-port, 10/100-Mbps Ethernet PHY. The DP83825I supports connections to an Ethernet MAC through RMII. Connections to the Ethernet media are made through the IEEE 802.3-defined Media Dependent Interface.

When using the device for Ethernet applications, it's necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

7.2 Typical Applications

図 7-1 shows a typical application for the DP83825I.

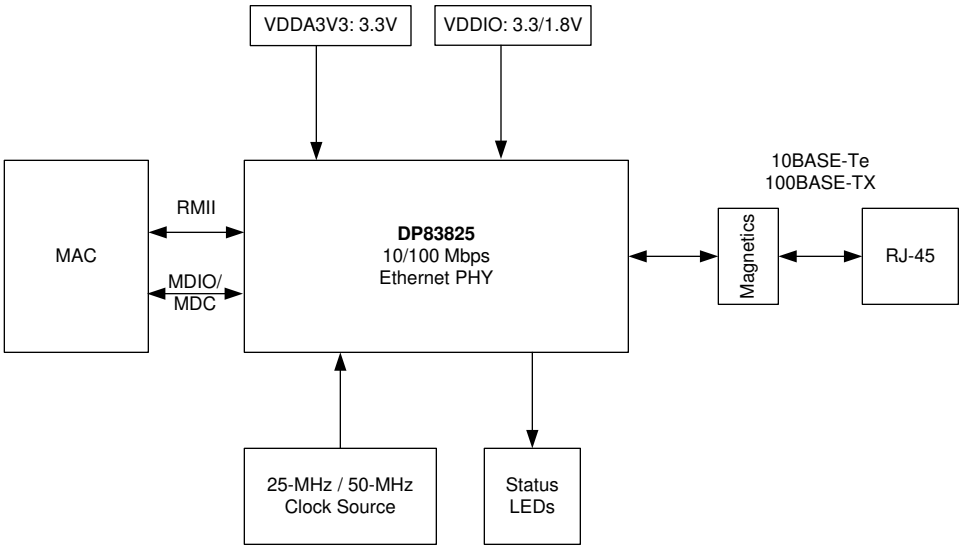

図 7-1. Typical DP83825I Application

7.2.1 Design Requirements

The design requirements for the DP83825I in TPI operation (100BASE-TX or 10BASE-Te) are:

1. AVD Supply = 3.3V
2. VDDIO Supply = 3.3V or 1.8V
3. Reference Clock Input = 25MHz or 50MHz (RMII Slave)

7.2.1.1 Clock Requirements

The DP83825I supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

7.2.1.1.1 Oscillator

If an external clock source is used, XI must be tied to the clock source and XO must be left floating. The amplitude of the oscillator must be a nominal voltage of VDDIO.

7.2.1.1.2 Crystal

The use of a 25MHz, parallel resonant, 20pF load crystal is recommended if operating with a crystal. A typical connection diagram is shown below for a crystal resonator circuit. Note that the load capacitor values vary with the crystal vendors. Check with the vendor for the recommended loads. Series resistance value shall be adjusted to meet the crystal drive level. For more details, refer to the *Selection and Specification of Crystals for Texas Instruments Ethernet Physical Layer Transceivers* application report (SNLA290).

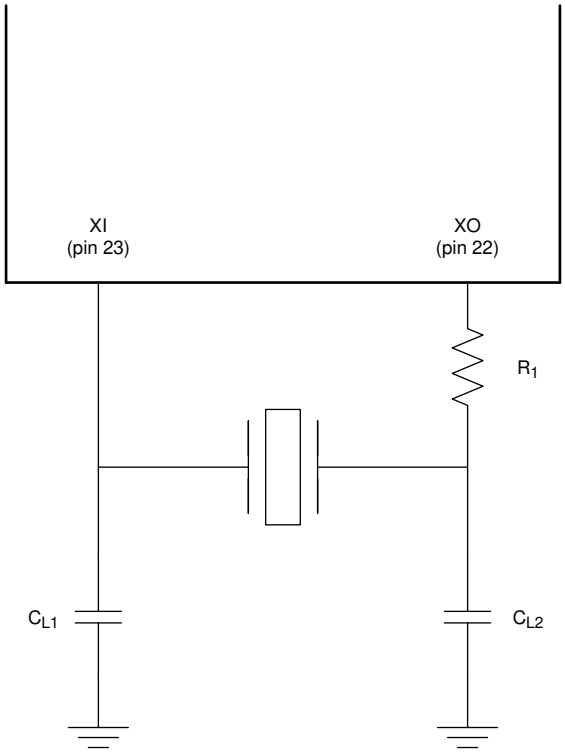

図 7-2. Crystal Oscillator Circuit

表 7-1. 25MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Including Operational Temperature, aging and other factors	–50		50	ppm
Load Capacitance			15	40	pF
ESR				50	Ω

7.2.2 Detailed Design Procedure

The Media Independent Interface RMII connects the DP83825I to the Media Access Controller (MAC). The MAC can in fact be a discrete device or integrated into a microprocessor, CPU, FPGA, or ASIC. The Media Dependent Interface (MDI) connects the DP83825I to the transformer of the Ethernet network or to AC isolation capacitors when interfacing with a fiber transceiver.

7.2.2.1 RMII Layout Guidelines

1. Remember that RMII signals as single-ended signals.

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2. Traces must be routed with 50Ω impedance to ground.
3. Keep trace lengths as short as possible. TI recommends to keep the trace lengths between two to six inches long.

7.2.2.2 MDI Layout Guidelines

1. Remember that MDI signals are differential.
2. Traces must be routed with 50Ω impedance to ground and 100Ω differential controlled impedance.
3. Route MDI traces to the transformer on the same layer.
4. Use a metal-shielded RJ-45 connector and electrically connect the shield to chassis ground.
5. Avoid supplies and ground beneath the magnetics.
6. Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

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7.2.2.3 TPI Network Circuit

図 7-3 shows the recommended twisted-pair interface network circuit for 10/100 Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

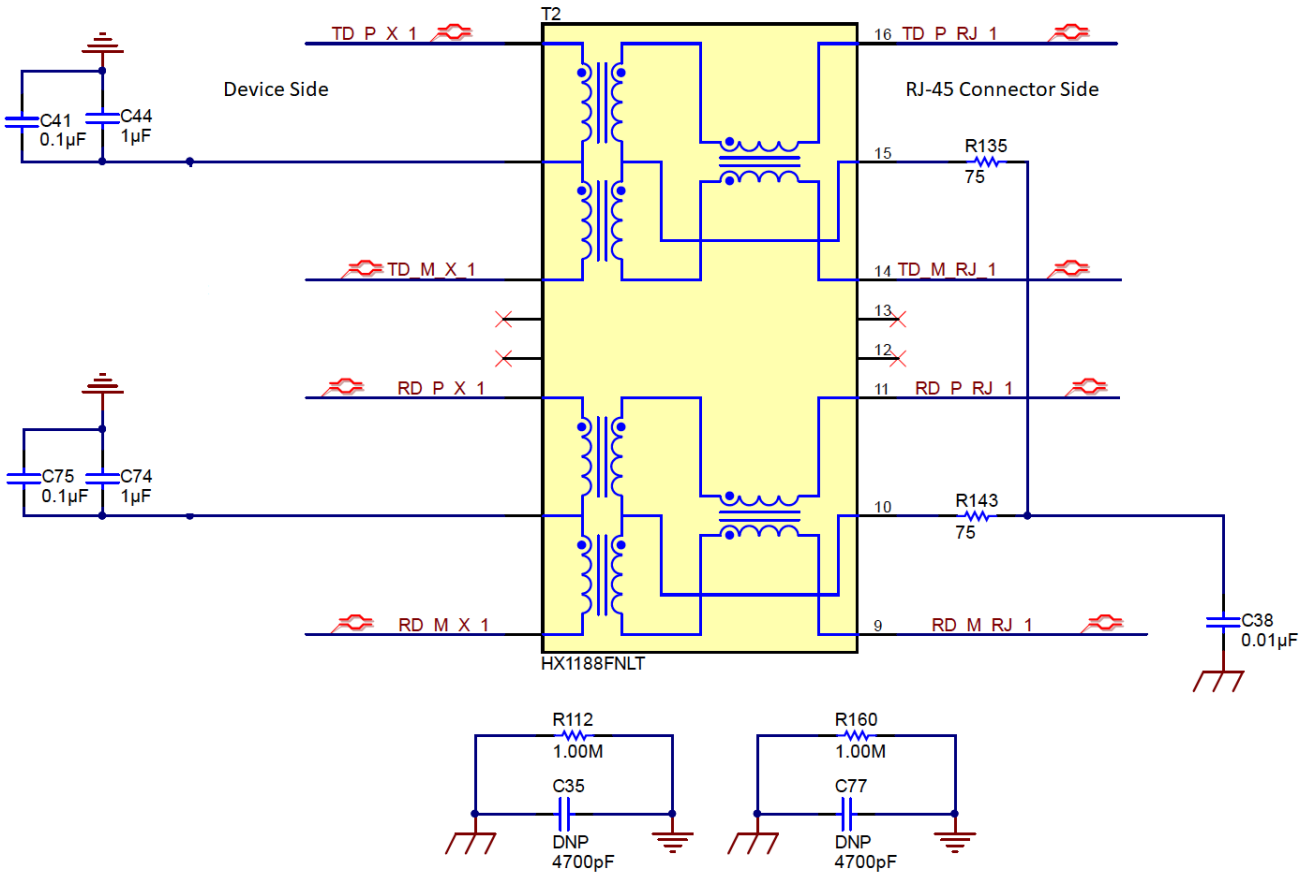

図 7-3. TPI Network Circuit

7.2.2.4 VOD Configuration

Registers DAC_CFG_0 (0x30B) and DAC_CFG_1 (0x30C) also function as VOD control registers. This is shown in VOD Configuration Description.

表 7-2. VOD Configuration Description

VoD Change	0x30B	0x30C
150%	0x0A00	0x0018
143.75%	0x0A40	0x0017
137.50%	0x0A80	0x0016
131.25%	0x0AC0	0x0015
125%	0x0B00	0x0014
118.75%	0x0B40	0x0013
112.50%	0x0B80	0x0012

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表 7-2. VOD Configuration Description (続き)

VoD Change	0x30B	0x30C
106.25%	0x0BC0	0x0011
100%	0x0C00	0x0010
93.75%	0x0C40	0x000F
87.50%	0x0C80	0x000E
81.25%	0x0CC0	0x000D
75%	0x0D00	0x000C
68.75%	0x0D40	0x000B
62.50%	0x0D80	0x000A
56.25%	0x0DC0	0x0009
50%	0x00E0	0x0008

表 7-3. VOD Fine Tuning

VOD Change	0x30E
+2.5%	Offset_2
+1.25%	Offset_1
Default (from 0x30B 0x30C)	Offset_0
+1.25%	Offset_-1
-2.5%	Offset_-2

Register 0x30E is used to fine-tune the VOD value in 1.25% increments, to a maximum of +/-2.5% from the original value chosen through registers 0x30B and 0x30C.

To calculate Offset_X:

1. Read Reg 0x333. Note this value varies between units
2. A = 0x333[15:11] converted to decimal
3. B = 0x333[10:6] converted to decimal
4. C = 8 - A + B. This variable is bounded between 0 and 15. If C is calculated to be outside the bounds, the variable C must be rounded back to the nearest bound. If C is calculated to be -2, set C to equal 0
5. D(x) = C + x, where x is determined using Reg 0x30E column
6. Offset_x = $[2D(x) + 1] \times 2048$; converted to hexadecimal

A starting point is change RBIAS to 6.34kΩ and setting VoD to -8% to further improve margins.

7.3 Power Supply Recommendations

The DP83825I is capable of operating with a 3.3V or 1.8V of I/O supply voltages along with analog supply of 3.3V. DP83825I needs VDDA3V3 after VDDIO is fully ramped. Details are captured in the *セクション 5.7*. If power sequencing is not feasible on the customer board, then an external Reset (RST_N) is needed on pin 5 when both power VDDA3V3 and VDDIO supplies are ramped.

図 7-4 shows the recommended power supply de-coupling network.

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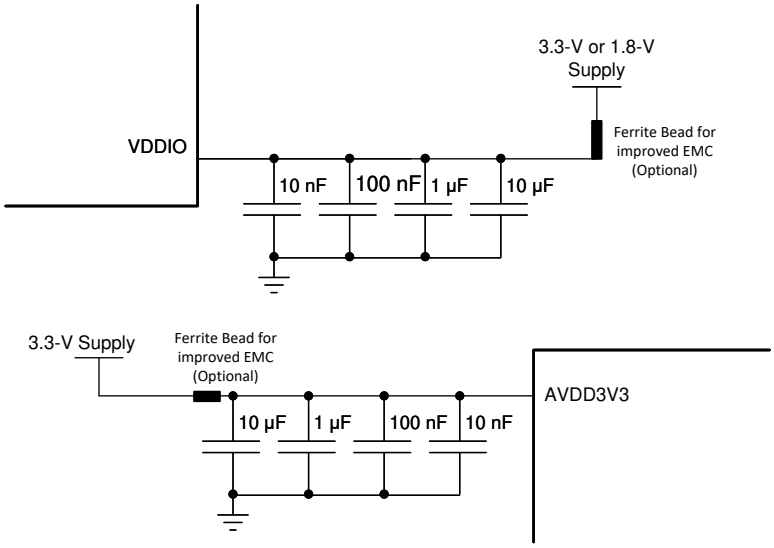

図 7-4. DP83825I Power Supply Decoupling Recommendation

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Signal Traces

PCB traces are lossy, and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50Ω single-ended impedance. Differential traces must be 100Ω differential. Take care to make sure impedance is controlled throughout. Impedance discontinuities cause reflections, leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

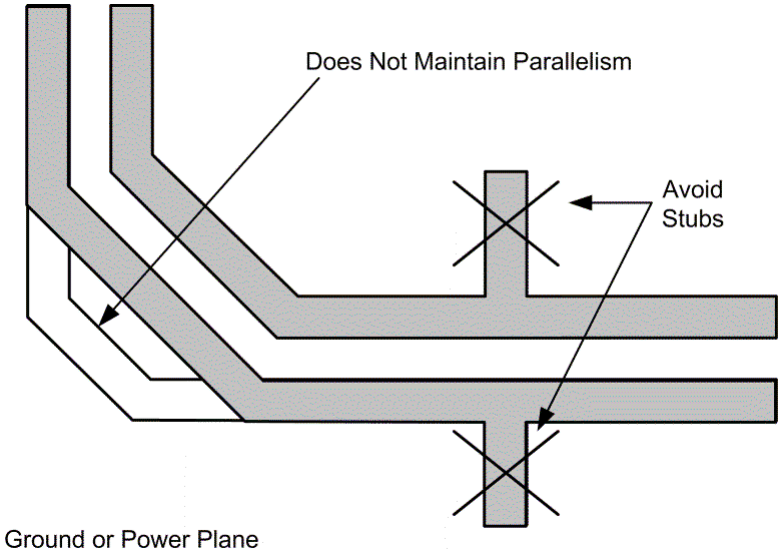

図 7-5. Differential Signal Traces

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and emissions. Length matching is also important for MAC interface connections. All RMII transmit signal trace lengths must match each other, and all RMII receive signal trace lengths must match each other, too.

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There must be no crossover or vias on signal path traces. Vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

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7.4.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces must be avoided at all cost. A signal crossing a split plane can cause unpredictable return path currents and can impact signal quality and result in emissions issues.

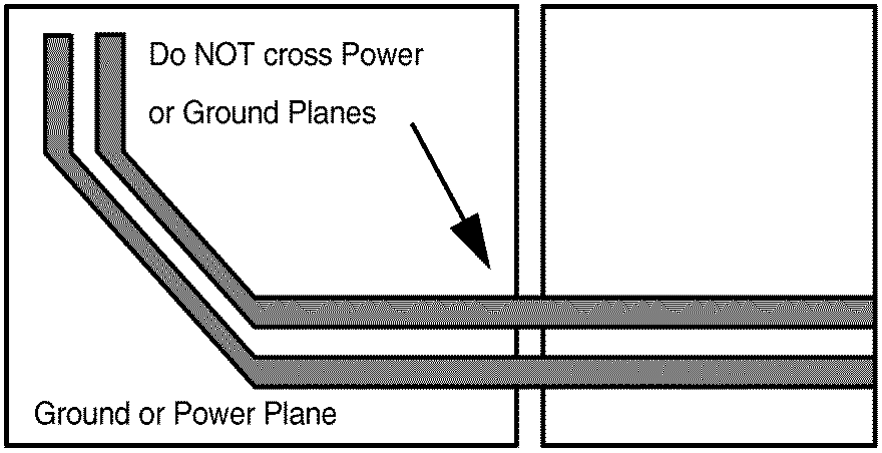

図 7-6. Differential Signal Pair and Plane Crossing

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7.4.1.3 Transformer Layout

Make sure there is no metal layer running beneath the transformer. Transformers can inject noise into the metal beneath them, which can affect the performance of the system. See 図 7-3.

7.4.1.3.1 Transformer Recommendations

The following magnetics have been tested with the DP83825I using the DP83825IEVM.

表 7-4. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse Electronics	HX1188NL
	HX1198FNL
	HX1188FNL

表 7-5. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn Ratio	±2%	1:1	-
Insertion Loss	1 - 100MHz	–1	dB
Return Loss	1 - 30MHz	–16	dB
	30 - 60MHz	–10	dB
	60 - 80MHz	–7.5	dB
Differential to Common Rejection Ratio	1	-61	dB
	50MHz	–33	dB
	150MHz	–25	dB
Crosstalk	30MHz	–45	dB
	60MHz	–39	dB
Isolation	HPOT	1500	Vrms

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7.4.1.4 Capacitive DC Blocking

To meet the operational requirements of transformer-less network applications, the following design showed in the schematic in 図 7-7 must be used.

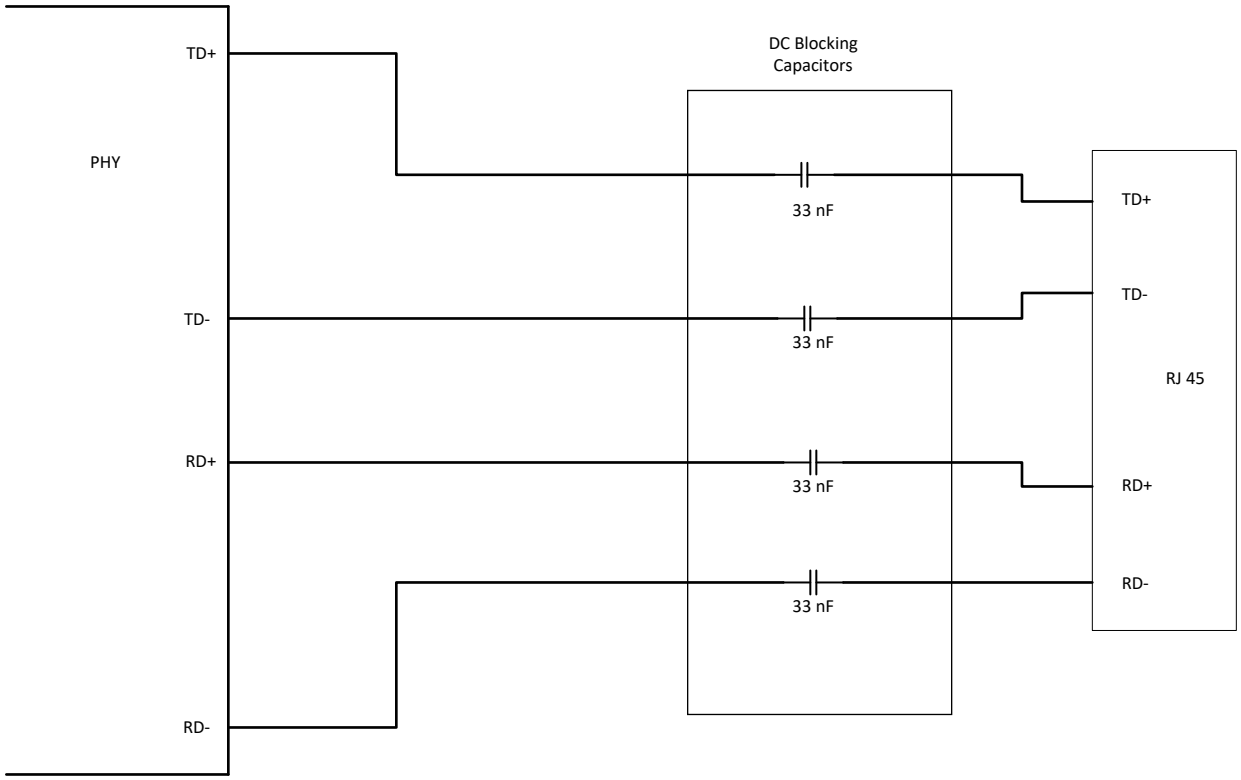

図 7-7. Transformer-less DC Blocking Configuration

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7.4.1.5 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

7.4.1.6 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB must be used when possible.

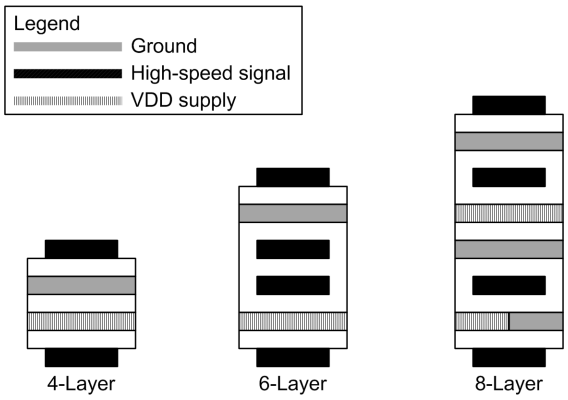

図 7-8. Recommended Layer Stack-Up

7.4.2 Layout Example

See the DP83825EVM for more information regarding layout.

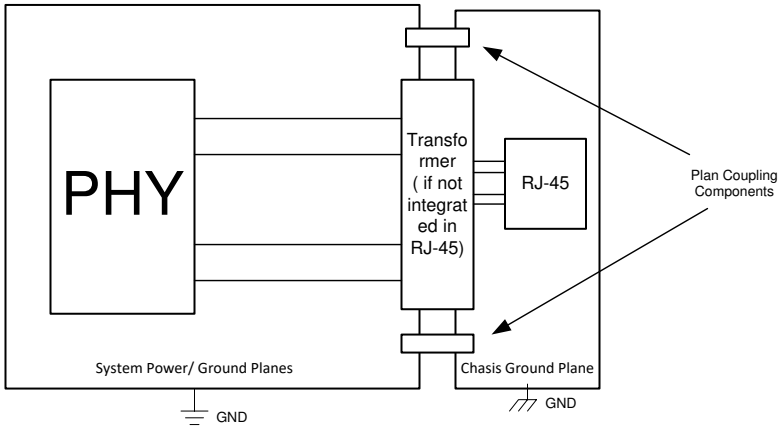

図 7-9. Layout Example

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2019) to Revision B (January 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Changed the amount of time to hold RST_N in Pin Functions Table	3
• Changed Power Supply sequencing to say VDDIO before AVDD under Power-Up Timing (T2)	10
• Added 0ms as minimum time for T2 under Power-up Timing	10
• RMII Master/Slave changed to RMII Transmit/Receive to better reflect the timing diagrams	10
• Added how long to hold down reset in case of unstable clock	12
• Changed 図 6-2 and 図 6-3	24
• Changed extended register access section for clarity	28
• Changed 表 6-5, 表 6-6 and 表 6-7 to move write to address 0x001F as the last step	37
• Flipped the bit values in register 0x17 (bits 2 and 3) and 0x4D1 (bits 0 and 3)	40
• Added VOD Configuration section	90
• Added Capacitive Blocking section	96

Changes from Revision * (December 2018) to Revision A (August 2019)	Page
• 製品ステータスを「事前情報」から「量産データ」	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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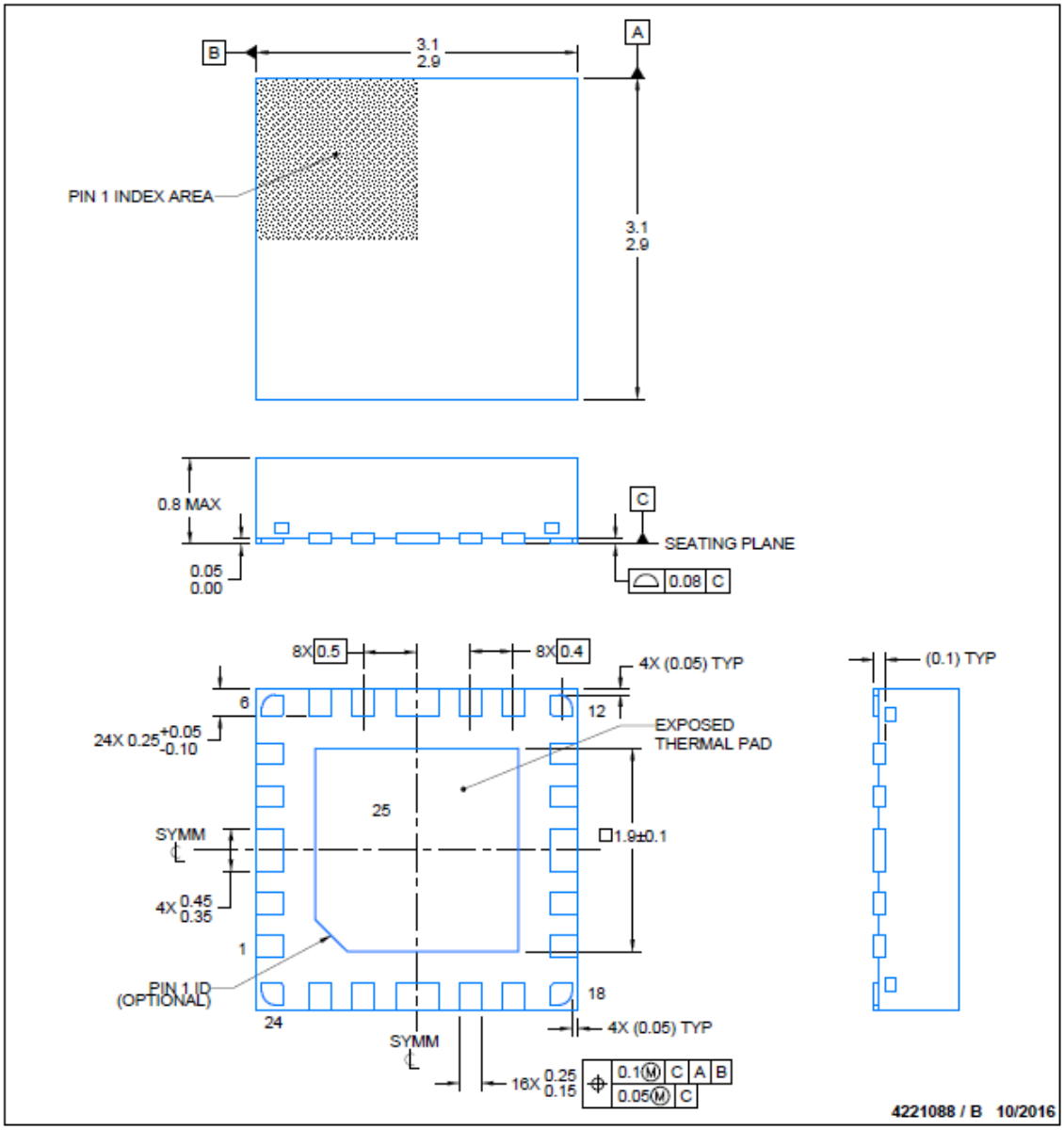
PACKAGE OUTLINE

RMQ0024A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

図 10-1. DP83825I Package Drawing

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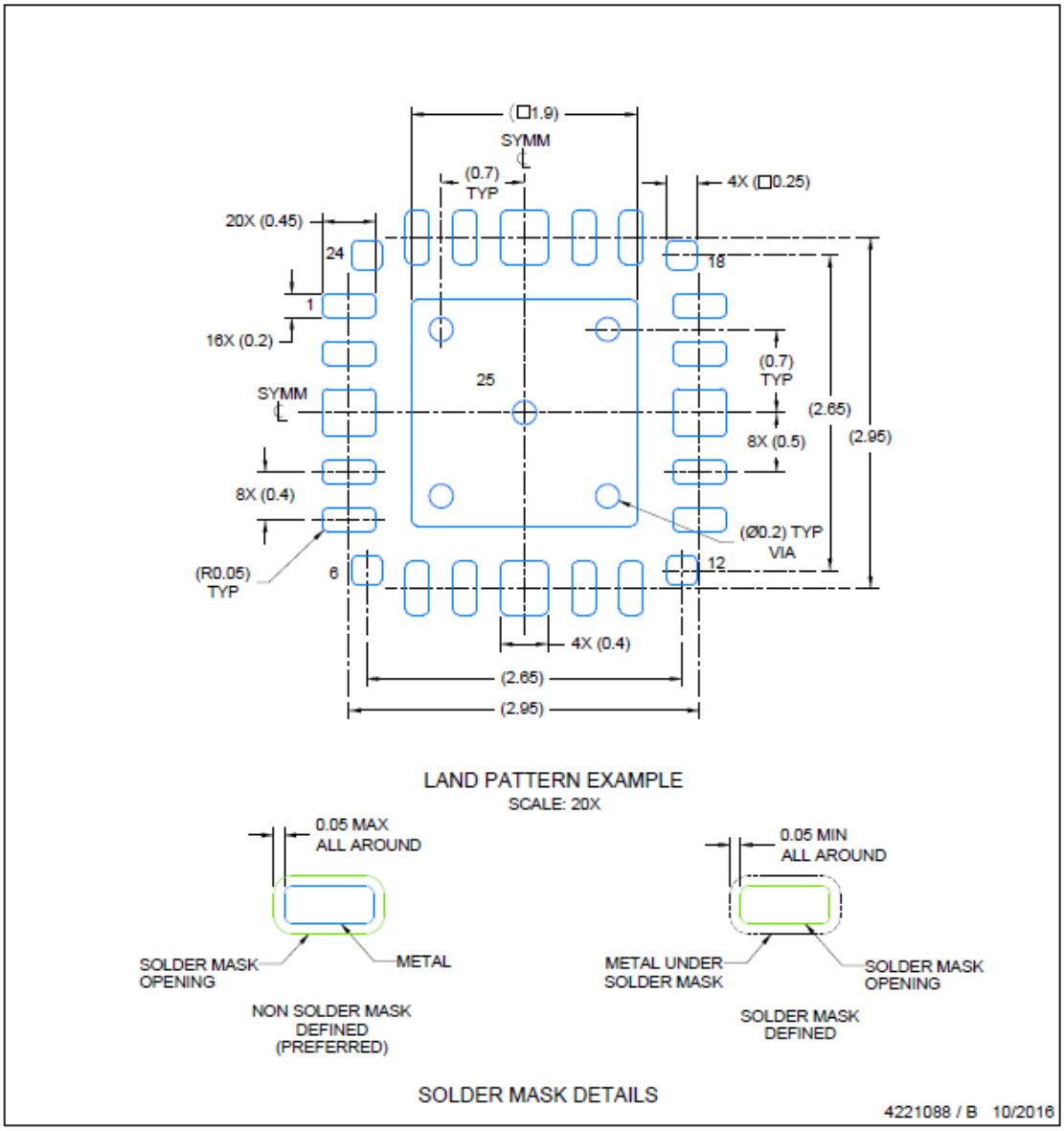
EXAMPLE BOARD LAYOUT

RMQ0024A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

図 10-2. DP83825I Package Drawing

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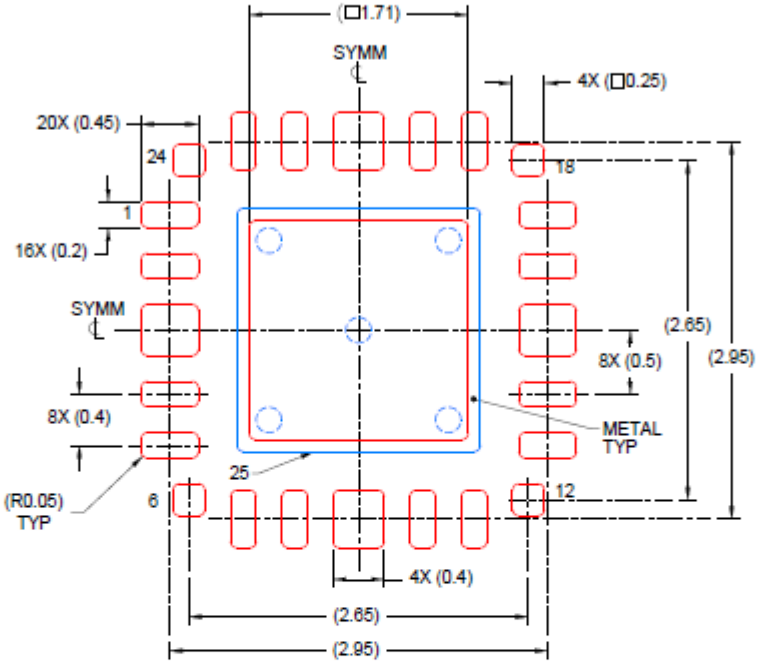
EXAMPLE STENCIL DESIGN

RMQ0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4221088 / B 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

図 10-3. DP83825I Package Drawing

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83825IRMQR	Active	Production	WQFN (RMQ) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I
DP83825IRMQR.A	Active	Production	WQFN (RMQ) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I
DP83825IRMQRG4.A	Active	Production	WQFN (RMQ) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I
DP83825IRMQT	Active	Production	WQFN (RMQ) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I
DP83825IRMQT.A	Active	Production	WQFN (RMQ) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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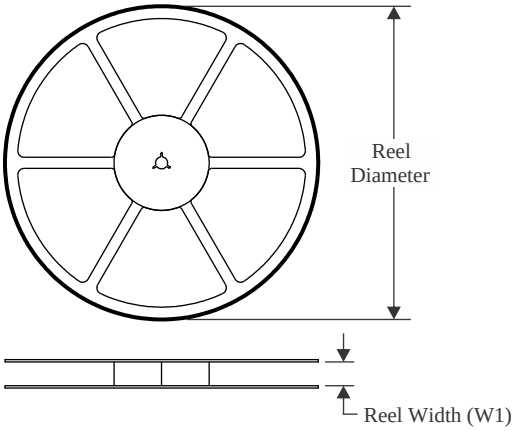
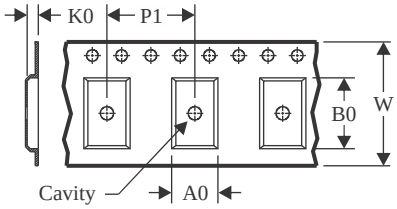
TAPE AND REEL INFORMATION

REEL DIMENSIONS

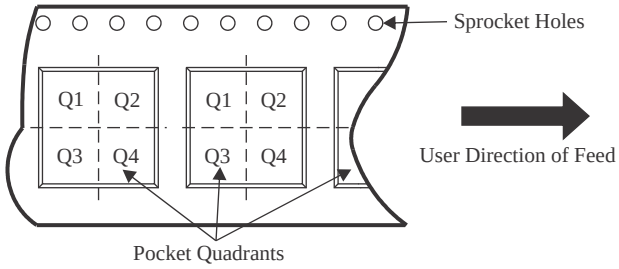


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

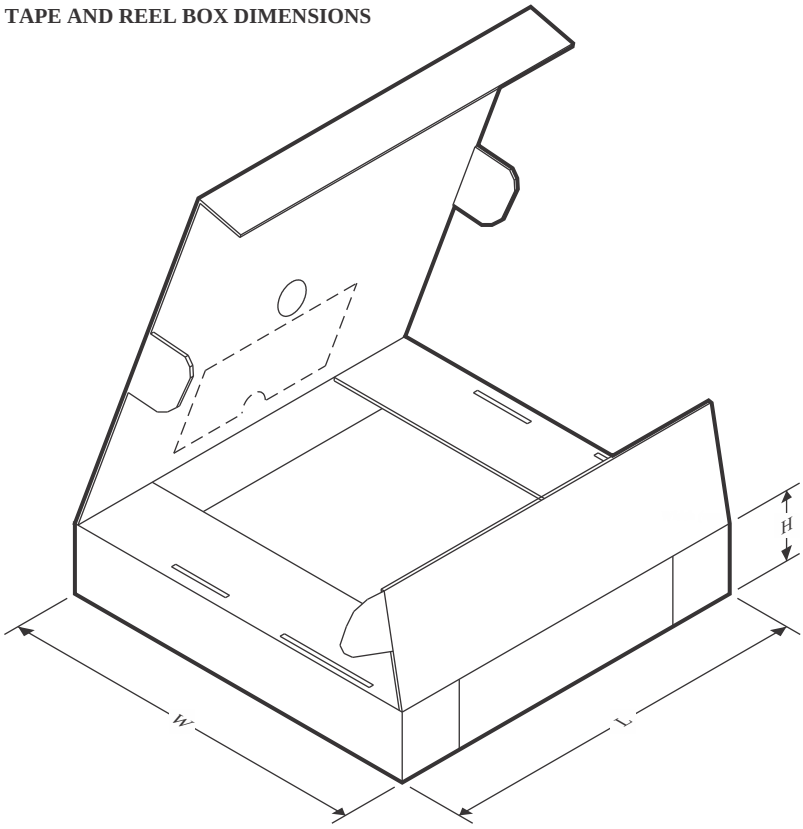
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83825IRMQR	WQFN	RMQ	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DP83825IRMQT	WQFN	RMQ	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

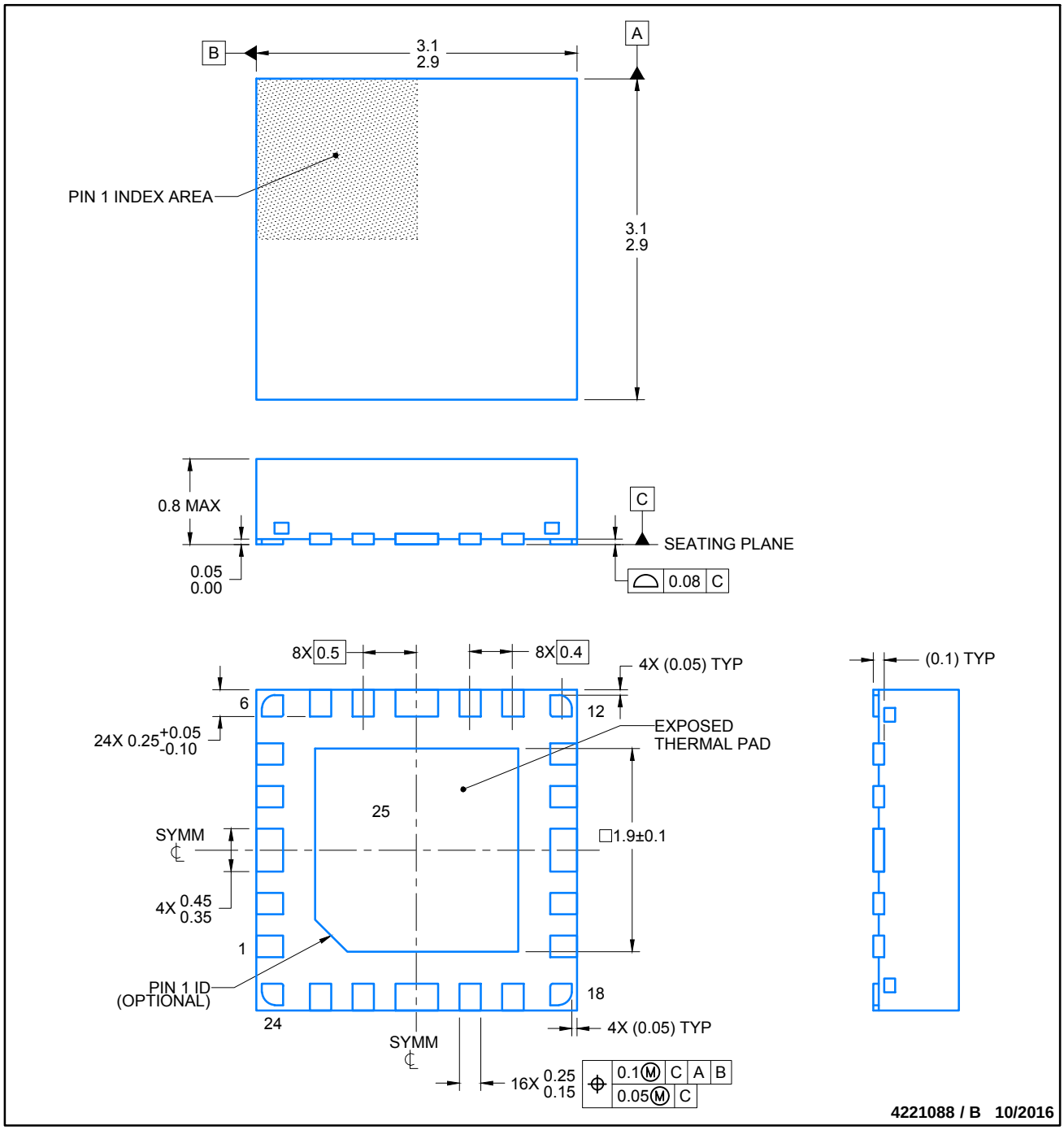
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83825IRMQR	WQFN	RMQ	24	3000	367.0	367.0	35.0
DP83825IRMQT	WQFN	RMQ	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RMQ0024A

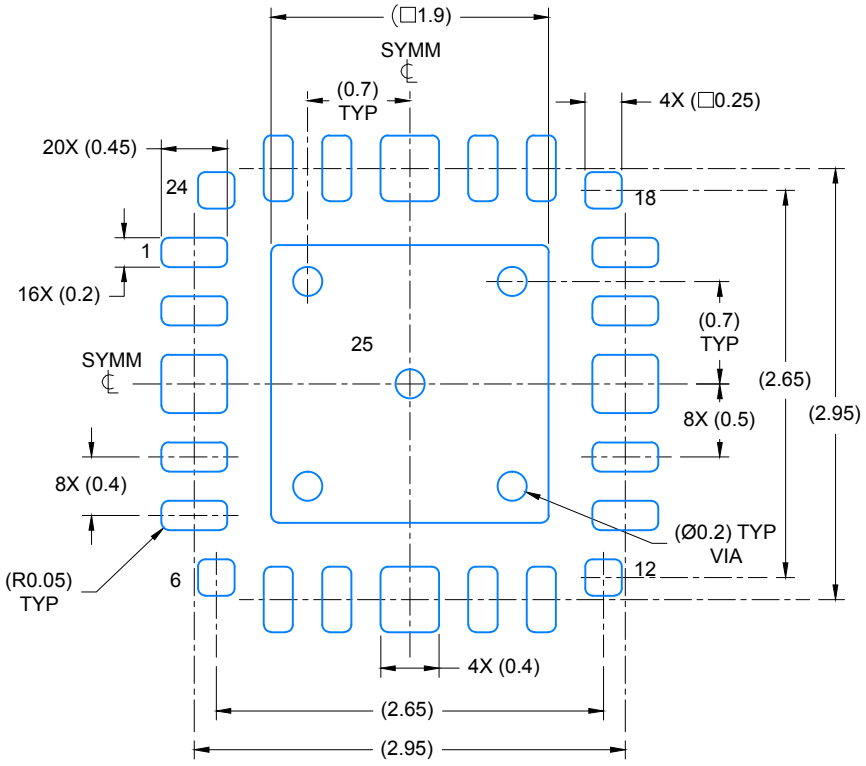
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



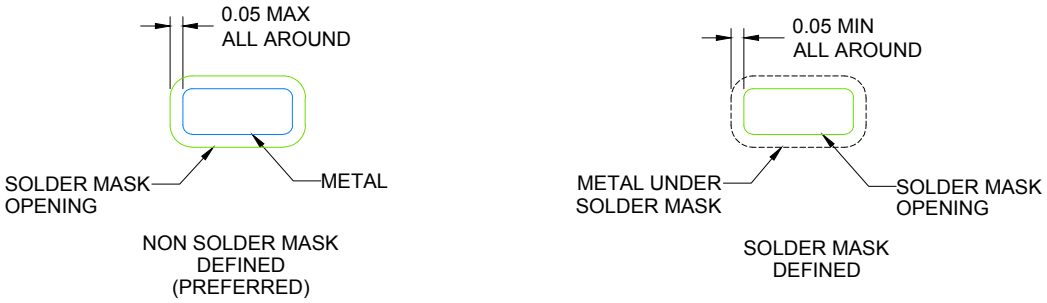
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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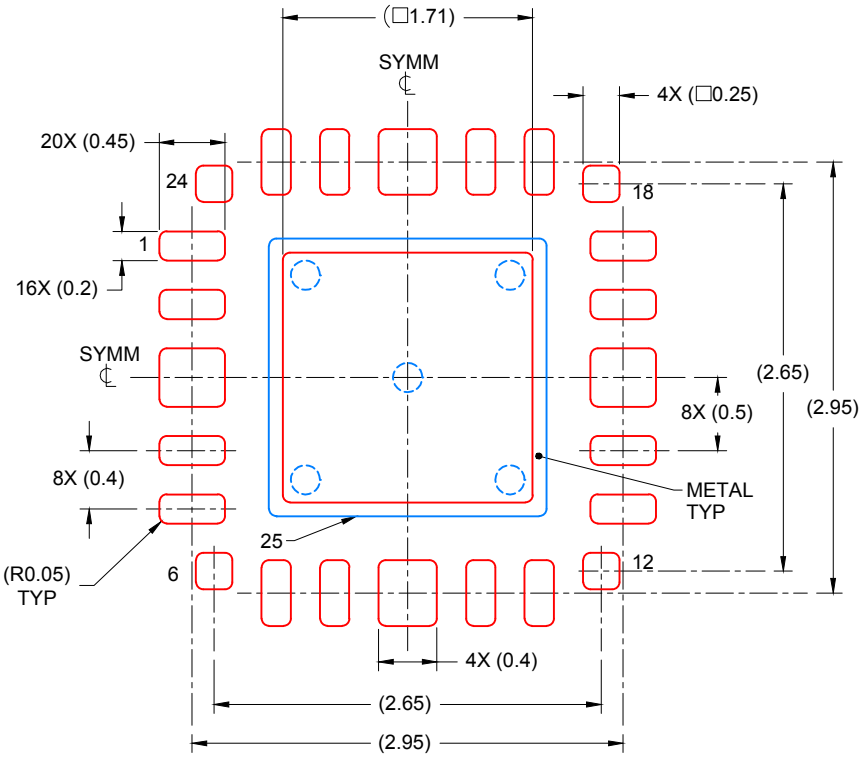
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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