



**LM27762 低ノイズ、正負電圧出力
チャージ・ポンプ、LDO内蔵**

1 特長

- ・ 可変の正電源電圧(1.5V~5V)と負電源電圧(-1.5V~-5V)を低ノイズで生成
- ・ 入力電圧範囲: 2.7V~5.5V
- ・ $\pm 250\text{mA}$ の出力電流
- ・ 反転チャージ・ポンプに続く負のLDO
- ・ 2MHzの低ノイズ固定周波数動作
- ・ 2.5Ω のインバータ出力インピーダンス、 $V_{\text{IN}} = 5\text{V}$
- ・ 負のLDOドロップアウト電圧: 100mAで30mV、 $V_{\text{OUT}} = -5\text{V}$
- ・ 正のLDOドロップアウト電圧: 100mAで45mV、 $V_{\text{OUT}} = 5\text{V}$
- ・ 静止電流: 390 μA (標準値)
- ・ シャットダウン時消費電流: 0.5 μA (標準値)
- ・ 電流制限と過熱保護
- ・ パワー・グッド・ピン(アクティブLOW)
- ・ **WEBENCH® Power Designer**により、LM27762を使用するカスタム設計を作成

2 アプリケーション

- Hi-Fiオーディオ・ヘッドフォン用アンプ
- オペアンプの電力バイアス
- データ・コンバータの電源供給
- ワイヤレス通信システム
- インターフェイス電源
- ハンドヘルド計測機器

3 概要

LM27762は、 $\pm 1.5V \sim \pm 5V$ の範囲で調整可能な非常に低ノイズの正および負の出力電圧を供給できます。入力電圧範囲は $2.7V \sim 5.5V$ で、出力電流は最大 $\pm 250mA$ です。動作電流がわずか $390\mu A$ で、シャットダウン時の電流は $0.5\mu A$ (標準値)であるため、LM27762はパワー・アンプ、DACバイアスなど、大電流で低ノイズの負電圧を必要とする用途で、理想的な性能を発揮します。このデバイスは、必要な外付け部品もわずかで、サイズの小さなソリューションを実現できます。

負の電圧は、レギュレートされた反転チャージ・ポンプと、それに続く低ノイズの負のLDOによって生成されます。LM27762デバイスの反転チャージ・ポンプは2MHz (標準値)のスウィッチング周波数で動作するため、出力抵抗と電圧リップルが減少します。正の電圧は、低ノイズの正のLDOを使用して、入力から生成されます。

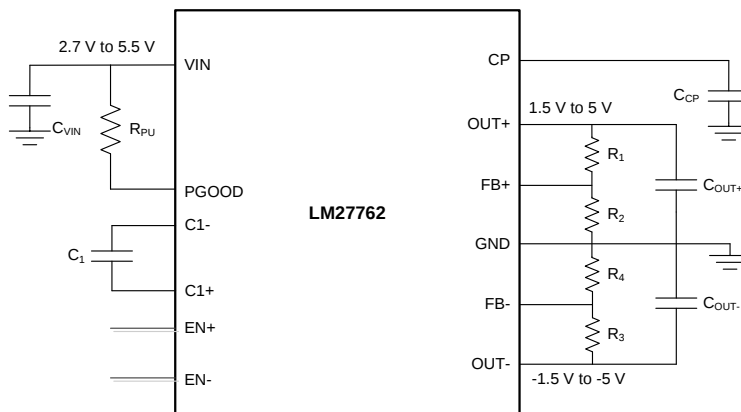
LM27762の正と負の出力には、それぞれ専用のイネーブル入力があります。これらの出力は、システム固有の電源シーケンス要件に対応するため、正と負のレールについて、それぞれ独立したタイミングをサポートしています。イネーブル入力を互いに短絡させ、入力電圧へ接続することもできます。**LM27762**には、オプションのパワー・グッド機能があります。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
LM27762	WS0N (12)	2.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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English Data Sheet: [SNVSAF7](#)

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2016) から Revision B に変更 Page

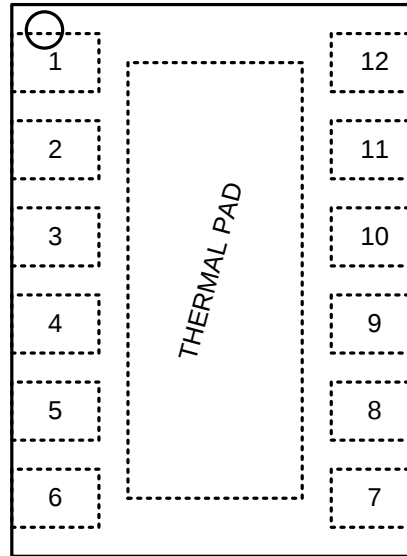
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2016年7月発行のものから更新 Page

•	タイトルの「スイッチト・キャパシタ」を「チャージ・ポンプ」へ 変更	1
•	「特長」で「 $\pm 1.5V \sim \pm 5V$ の低ノイズの可変の正および負の電源電圧を生成」を「可変の正電源電圧 ($1.5V \sim 5V$) と、負電源電圧 ($-1.5V \sim -5V$) を低ノイズで生成」へ 変更	1

5 Pin Configuration and Functions

**DSS Package
12-Pin WSON With Thermal Pad
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
C1+	10	Power	Positive terminal for C ₁
C1–	9	Power	Negative terminal for C ₁
CP	5	Power	Negative unregulated output voltage
EN+	12	Input	Enable input for the positive LDO, Active high
EN–	8	Input	Enable input for the charge pump and negative LDO, Active high
FB+	2	Power	Feedback input. Connect FB+ to an external resistor divider between OUT+ and GND. DO NOT leave unconnected.
FB–	7	Power	Feedback input. Connect FB– to an external resistor divider between OUT– and GND. DO NOT leave unconnected.
GND	4	Ground	Ground
OUT+	11	Power	Regulated positive output voltage
OUT–	6	Power	Regulated negative output voltage
PGOOD	1	Output	Power Good flag; open drain; Logic 0 = power good, Logic 1 = power not good. Connect to ground if not used.
VIN	3	Power	Positive power supply input
Thermal Pad	—	Ground	Ground. DO NOT leave unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
V _{IN} to GND or GND to V _{OUT}		5.8	V
EN+, EN-	GND – 0.3	V _{IN}	V
C _{POUT} , OUT+ and OUT- , continuous output current		300	mA
OUT+, OUT- short-circuit duration to GND ⁽³⁾		1	s
Continuous power dissipation ⁽⁴⁾	Internally limited		
T _{JMAX} ⁽⁴⁾		150	°C
Operating input voltage, V _{IN}	2.7	5.5	V
Operating output current, I _{OUT}	0	250	mA
Operating ambient temperature, T _A	–40	85	°C
Operating junction temperature, T _J	–40	125	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
- (3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V_{IN} may damage the device and must be avoided. Also, for temperatures above T_A = 85°C, V_{OUT} must not be shorted to GND or V_{IN} or device may be damaged.
- (4) Internal thermal shutdown circuitry protects the device from damage.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature, T _A	–40	85	°C
Operating junction temperature, T _J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM27762	UNIT
		DSS (WSON)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	25.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	25.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.2	°C/W

- (1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Typical limits apply for $T_A = 25^\circ\text{C}$; minimum and maximum limits apply over the full temperature range. Unless otherwise specified $V_{IN} = 5\text{ V}$, $C_{IN} = C_{OUT+} = C_{OUT-} = 2.2\text{ }\mu\text{F}$, $C_1 = 1\text{ }\mu\text{F}$, $C_{POUT} = 4.7\text{ }\mu\text{F}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Supply current	Open circuit, no load, EN+, EN– connected to VIN. ⁽¹⁾		390		μA
I_{SD}	Shutdown supply current			0.5	5	μA
f_{SW}	Switching frequency	$V_{IN} = 3.6\text{ V}$	1.7	2	2.3	MHz
R_{NEG}	Output resistance to C_{POUT}	$V_{IN} = 5.5\text{ V}$, $I_L = 100\text{ mA}$		2.5		Ω
V_{LDO-}	LDO dropout voltage	$I_L = 100\text{ mA}$, $V_{OUT-} = -5\text{ V}$		30		mV
PSRR	Power supply rejection ratio, OUT–	$I_L = 100\text{ mA}$, $V_{OUT-} = -1.8\text{ V}$, 10 kHz		50		dB
V_{N-}	Output noise voltage	$I_L = 80\text{ mA}$, 10 Hz to 100 kHz		22		μV_{RMS}
V_{FB-}	Feedback pin reference voltage		–1.238	–1.22	–1.202	V
V_{OUT-}	Adjustable output voltage	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$	–5		–1.5	V
	Load regulation	0 to 250 mA, $V_{OUT-} = -1.8\text{ V}$		34		$\mu\text{V}/\text{mA}$
	Line regulation	$5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$, $I_L = 50\text{ mA}$		1.5		mV/V
V_{LDO+}	LDO dropout voltage	$I_L = 100\text{ mA}$, $V_{OUT+} = 5\text{ V}$		45		mV
PSRR	Power supply rejection ratio, OUT+	$I_L = 100\text{ mA}$, $V_{OUT+} = 1.8\text{ V}$, 10 kHz		43		dB
V_{N+}	Output noise voltage	$I_L = 80\text{ mA}$, 10 Hz to 100 kHz		22		μV_{RMS}
V_{FB+}	Feedback pin reference voltage		1.182	1.2	1.218	V
V_{OUT+}	Adjustable output voltage	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$	1.5		5	V
	Load regulation	0 to 250 mA, $V_{OUT+} = 1.8\text{ V}$		11		$\mu\text{V}/\text{mA}$
	Line regulation	$5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$, $I_L = 50\text{ mA}$		1.9		mV/V
V_{IH}	Enable pin input voltage high	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$	1.2			V
V_{IL}	Enable pin input voltage low	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$			0.4	V

(1) When $V_{IN} = 5.5\text{ V}$ charge pump may enter PWM mode in hot conditions.

6.6 Typical Characteristics

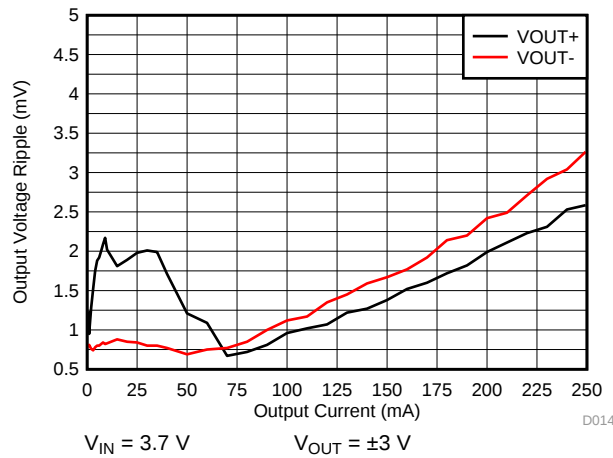


FIG 1. Output Voltage Ripple vs Output Current

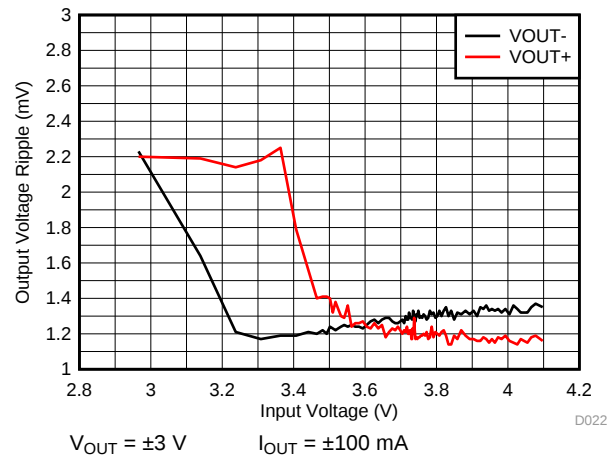


FIG 2. Output Voltage Ripple vs Input Voltage

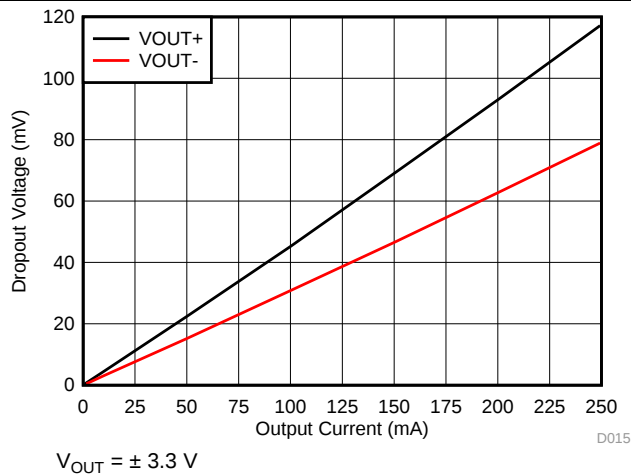


FIG 3. LDO Dropout Voltage vs Output Current

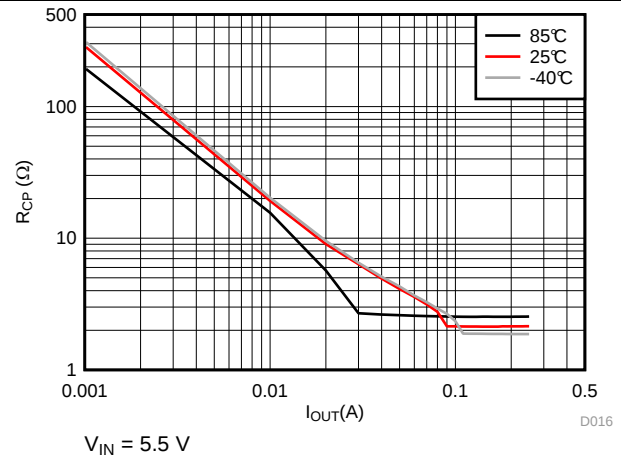


FIG 4. Charge Pump Output Resistance vs Output Current

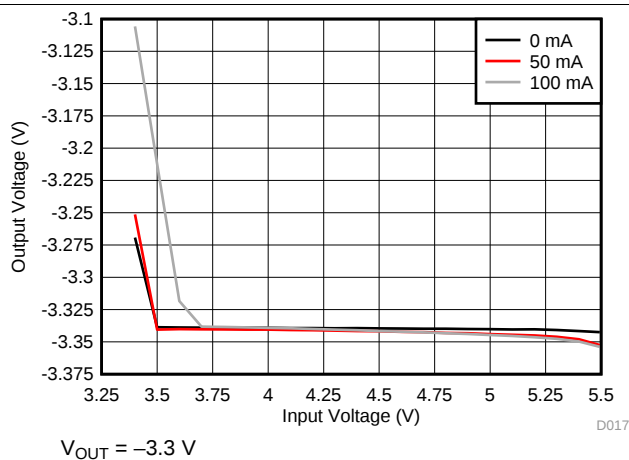


FIG 5. Line Regulation for OUT-

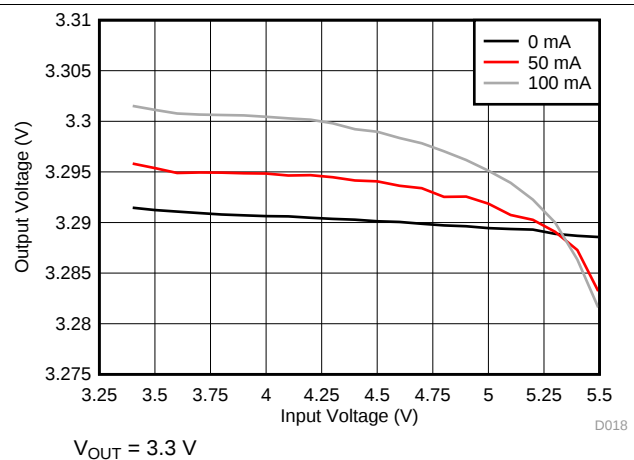


FIG 6. Line Regulation for OUT+

Typical Characteristics (continued)

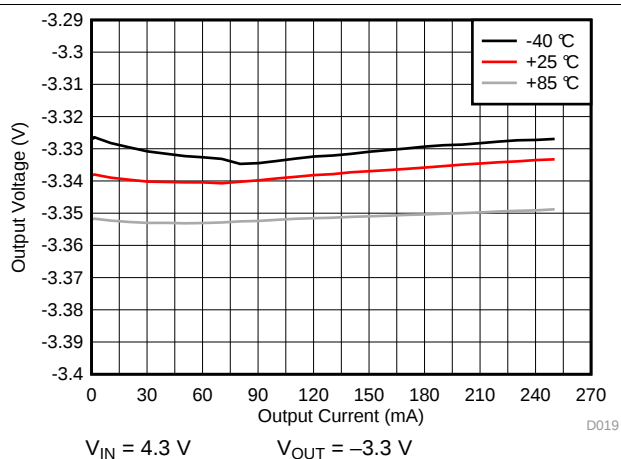


图 7. Load Regulation for OUT-

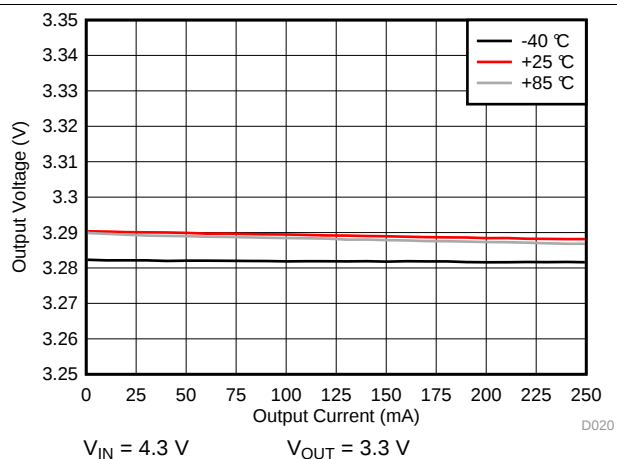


图 8. Load Regulation for OUT+

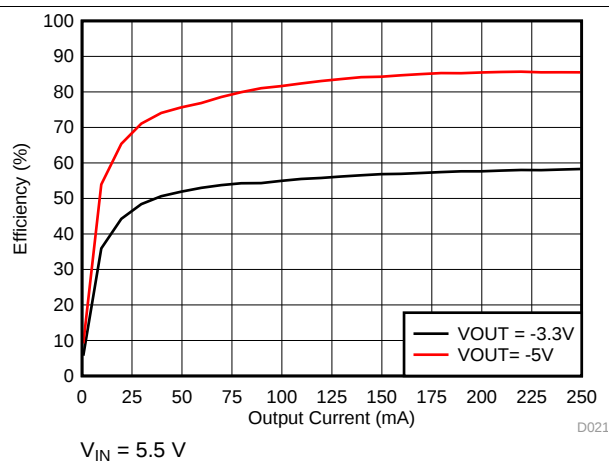


图 9. Efficiency for OUT-

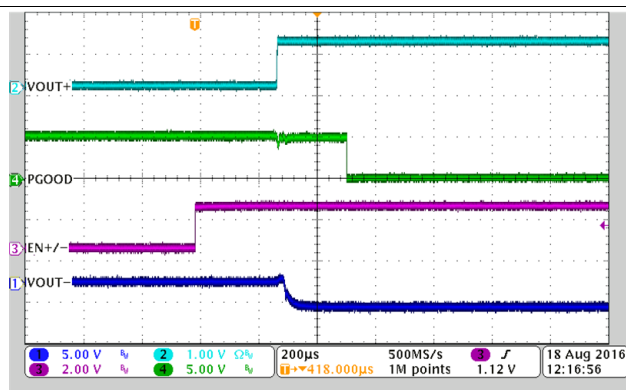


图 10. Start-Up

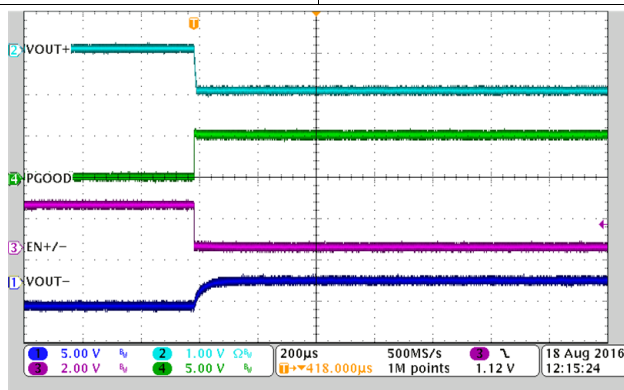


图 11. Shutdown

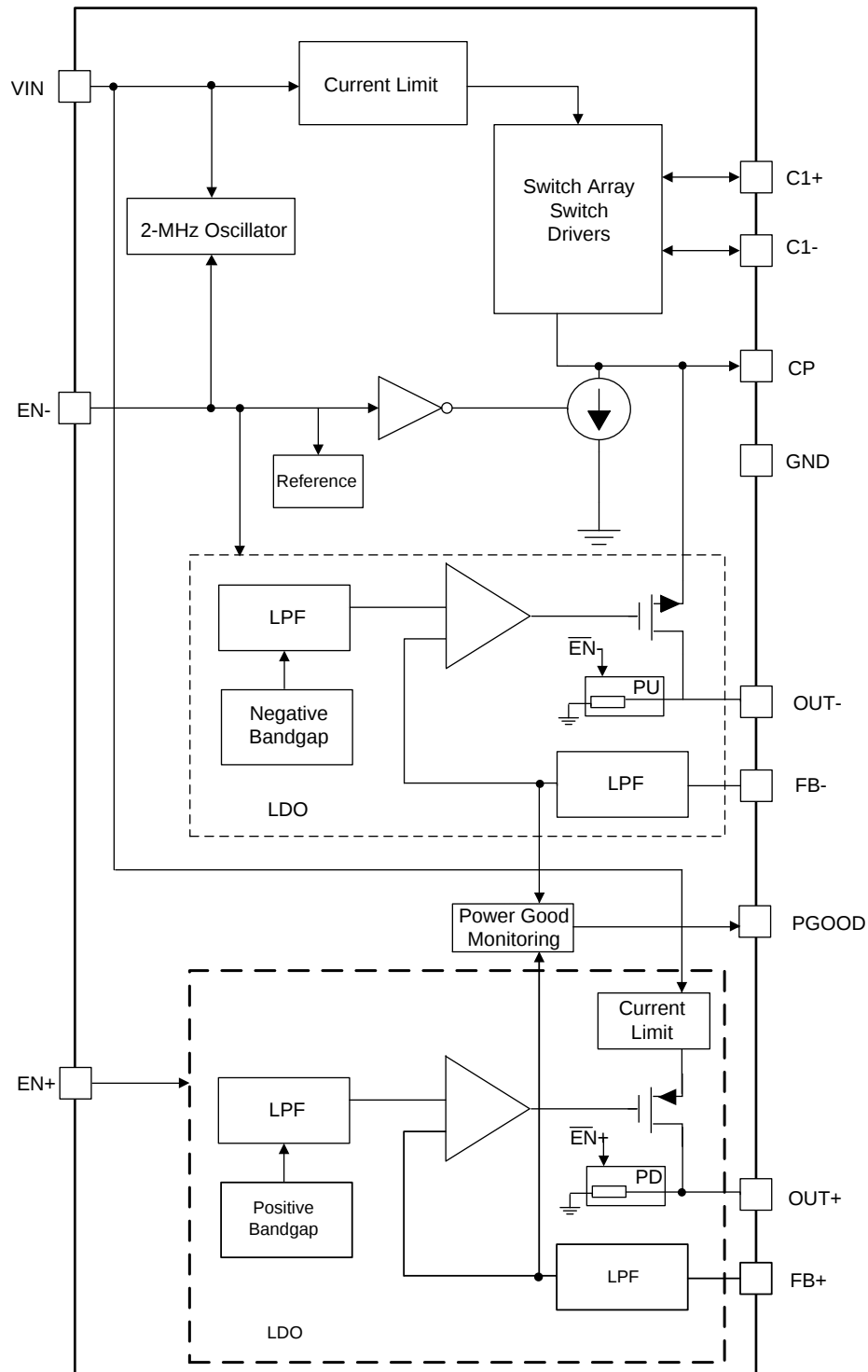
7 Detailed Description

7.1 Overview

The LM27762 low-noise inverting charge pump with both positive and negative LDOs delivers very low-noise adjustable positive and negative outputs between ± 1.5 V and ± 5 V. The output voltage levels of the positive and negative LDO are independently controllable with external resistors. Input voltage range of LM27762 is from 2.7 V to 5.5 V. Five low-cost capacitors are used in this circuit to provide up to ± 250 mA of output current. The LM27762 operates at 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. With an typical operating current of only 390 μ A and 0.5- μ A typical shutdown current, the LM27762 provides ideal performance for power amplifiers and DAC bias and other high-current, low-noise negative voltage needs.

The LM27762 device has an enable input (EN+) for the positive LDO and another enable input (EN–) for the negative charge pump and LDO. This supports independent timing for the positive and negative rails in system power sequence. Enable inputs can be also shorted together and connected to VIN. When LDO is disabled, output of the positive LDO has 50-k Ω pulldown to ground, and output of the negative LDO has 50-k Ω pullup to ground. The LM27762 has power good monitoring for OUT+ and OUT– outputs. The PGOOD pin is an open-drain output and requires an external pullup resistor. When Power Good feature is not used, PGOOD pin can be connected to ground.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Undervoltage Lockout

The LM27762 has an internal comparator that monitors the voltage at V_{IN} and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM27762 resumes normal operation.

7.3.2 Input Current Limit

The LM27762 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The charge pump and positive LDO both have 500 mA (typical) input current limit when the output is shorted directly to ground. When the LM27762 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

7.3.3 PFM Operation

To minimize quiescent current during light load operation, the LM27762 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is low, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-2-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency in the LM27762 is 2 MHz.

7.3.4 Output Discharge

In shutdown, the LM27762 actively pulls down on the outputs (OUT+, OUT–) of the device until the output voltage reaches GND.

7.3.5 Power Good Output (PGOOD)

The LM27762 has monitoring for the OUT+ and OUT– output voltage levels and open-drain PGOOD output.

表 1. PGOOD (Active Low) Operation

EN+	EN–	OUT+	OUT–	PGOOD
Low	Low	Don't care	Don't care	High
High	Low	< 95% of target value	Don't care	High
High	Low	> 95% of target value	Don't care	Low
Low	High	Don't care	< 95% of target value	High
Low	High	Don't care	> 95% of target value	Low
High	High	< 95% of target value	Don't care	High
High	High	Don't care	< 95% of target value	High
High	High	> 95% of target value	> 95% of target value	Low

7.3.6 Thermal Shutdown

The LM27762 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the device switches into shutdown mode. The LM27762 releases thermal shutdown when the junction temperature is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. The LM27762 device power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped by reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the device.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

When enable pins (EN+, EN–) are low, both positive and negative outputs of LM27762 are disabled, and the device is in shutdown mode reducing the quiescent current to minimum level. In shutdown, the outputs of the LM27762 are pulled to ground (internal 50 k Ω between each OUT pin and ground).

7.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN+ pin enables the positive LDO. Applying a voltage greater than 1.2 V to the EN– pin enables the negative CP and LDO. When enabled, the positive and negative output voltages are equal to levels set by external resistors. Care must be taken to both the positive LDO and the inverting charge pump followed by negative LDO have enough headroom. Power Good output PGOOD indicates the status of OUT+ and OUT– voltage levels.

8 Application and Implementation

注

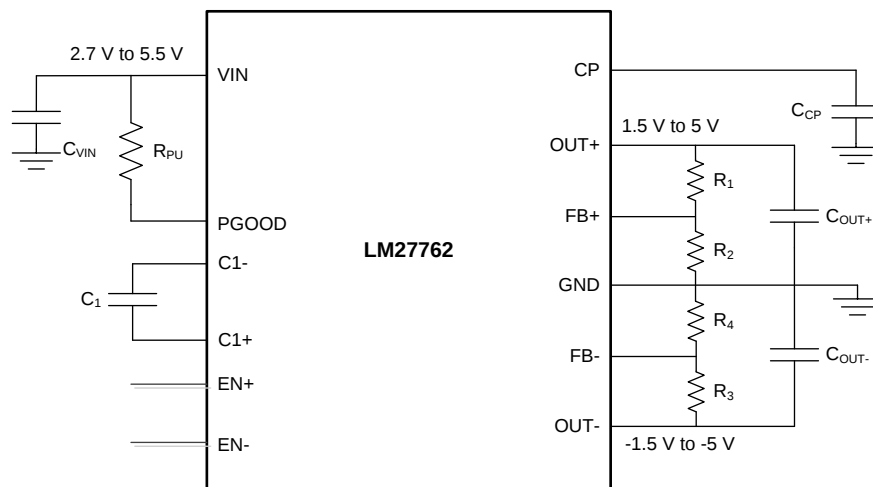
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM27762 input voltage range is from 2.7 V to 5.5 V. The positive LDO provides a positive voltage configurable with external gain setting resistors R_1 , R_2 . The low-noise charge-pump voltage converter inverts the input voltage V to a negative output voltage. Charge pump is followed by the negative LDO which regulates a negative output voltage configurable with external gain setting resistors R_3 , R_4 . Output voltage range is ± 1.5 V to ± 5 V. When selecting input (VIN) and output (OUT+, OUT-) voltages ranges, headroom required by the charge pump and LDOs must be considered. Charge-pump minimum headroom can be estimated based on the maximum load current and charge pump output resistance.

The device uses five low-cost capacitors to provide up to 250 mA of output current. The LM27762 operates at a 2-MHz oscillator frequency to reduce charge-pump output resistance and voltage ripple under heavy loads. When using the optional open-drain PGOOD feature, connect a 10-k Ω pullup resistor (R_{PU}) to VIN. Connect pin to ground if PGOOD is not used.

8.2 Typical Application



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✎ 12. LM27762 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

The following example describes powering an amplifier driving high impedance headphones. Input voltage is from a smart-phone battery. Amplifier is driving 2-V_{RMS} to 600-Ω stereo headphones.

表 2. Application Example Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V to 4.2 V
Output voltage	±3 V
Output current	10 mA (LM27762 capability 250 mA maximum)
C _{VIN} , C _{OUT+} , C _{OUT-}	2.2 μF
C _{CP}	4.7 μF
R _{PU}	10 kΩ (optional, connect PGOOD pin to ground if feature is not used)

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM27762 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Positive Low-Dropout Linear Regulator and OUT+ Voltage Setting

LM27762 features a low-dropout, linear positive voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The positive output voltage of the LM27762 is externally configurable. The value of R₁ and R₂ determines the output voltage setting. The output voltage can be calculated using 式 1:

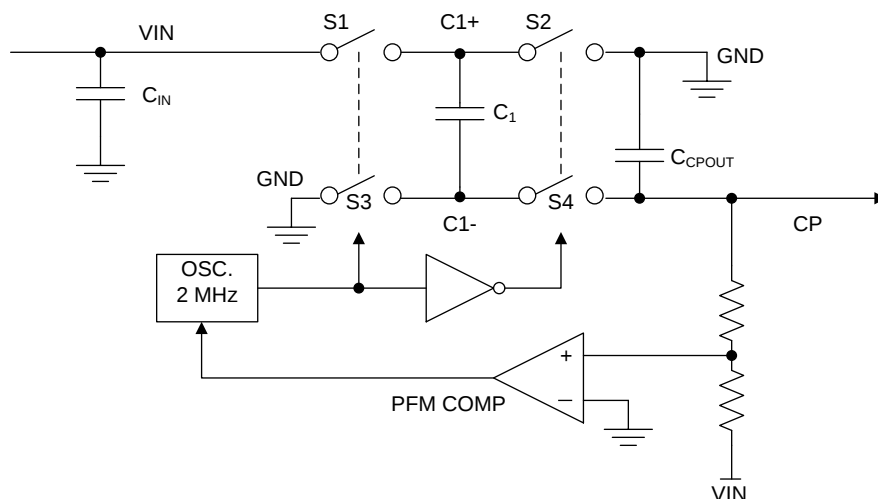
$$V_{OUT} = 1.2 \text{ V} \times (R_1 + R_2) / R_2 \quad (1)$$

The value for R₂ must be no less than 50 kΩ.

8.2.2.3 Charge-Pump Voltage Inverter

The main application of the LM27762 is to generate a regulated negative supply voltage. The voltage inverter circuit uses only three external capacitors, and the LDO regulator circuit uses one additional output capacitor.

The voltage inverter portion of the LM27761 contains four large CMOS switches which are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. 图 13 shows the voltage switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, and C₁ is charging C_{CP}. After a number of cycles, the voltage across C_{CP} is pumped into V_{IN}. Because the anode of C_{CP} is connected to ground, the output at the cathode of C_{CP} equals –(V_{IN}) when there is no load current. When a load is added, the output voltage drop is determined by the parasitic resistance (R_{DS(on)} of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between the capacitors.



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13. Voltage Inverting Principle

The output characteristic of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals $-(V_{IN})$. The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance, and the ESR of C_1 and C_{CP} . Because the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The charge-pump output capacitor C_{CP} is charging and discharging at a current approximately equal to the output current; therefore, its ESR only counts once in the output resistance. A good approximation of charge-pump R_{OUT} is shown in 式 2:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C_1)] + (4 \times ESR_{C1}) + ESR_{CCP}$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in 13. (2)

High capacitance and low-ESR ceramic capacitors reduce the output resistance.

8.2.2.4 Negative Low-Dropout Linear Regulator and OUT– Voltage Setting

At the output of the inverting charge-pump the LM27762 features a low-dropout, linear negative voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This negative LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The negative output voltage of the LM27762 is externally configurable. The value of R_3 and R_4 determines the output voltage setting. The output voltage can be calculated using 式 1:

$$V_{OUT} = -1.22 \text{ V} \times (R_3 + R_4) / R_4 \quad (3)$$

The value for R_4 must be no less than 50 kΩ.

8.2.2.5 External Capacitor Selection

The LM27762 requires 5 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low ESR ($\leq 15 \text{ m}\Omega$ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM27762 due to their high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferable for use with the LM27762. These capacitors have tight capacitance tolerances (as good as $\pm 10\%$) and hold their value over temperature (X7R: $\pm 15\%$ over -55°C to $+125^\circ\text{C}$; X5R $\pm 15\%$ over -55°C to $+85^\circ\text{C}$).

Using capacitors with a Y5V or Z5U temperature characteristic is generally not recommended for the LM27762. These capacitors typically have wide capacitance tolerance (80%,20%) and vary significantly over temperature (Y5V: 22%, –82% over –30°C to +85°C range; Z5U: 22%, –56% over 10°C to 85°C range). Under some conditions a 1-μF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 μF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27762.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower-than-expected capacitance on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. TI strongly recommends that the LM27762 circuit be evaluated thoroughly early in the design-in process with the mass-production capacitor of choice. This helps ensure that any such variability in capacitance does not negatively impact circuit performance.

8.2.2.5.1 Charge-Pump Output Capacitor

In typical applications, Texas Instruments recommends a 4.7-μF low-ESR ceramic charge-pump output capacitor (C_{CP}). Different output capacitance values can be used to reduce charge pump ripple, shrink the solution size, and/or cut the cost of the solution. However, changing the output capacitor may also require changing the flying capacitor or input capacitor to maintain good overall circuit performance.

In higher-current applications, a 10-μF, 10-V low-ESR ceramic output capacitor is recommended. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2-μF capacitance is recommended. For example, 10-μF, 10-V output capacitor in a 0402 case size typically has only 2-μF capacitance when biased to 5 V.

8.2.2.5.2 Input Capacitor

The input capacitor (C_2) is a reservoir of charge that aids in a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. It also filters noise on the input pin, keeping this noise out of the sensitive internal analog circuitry that is biased off the input line.

Input capacitance has a dominant and first-order effect on the input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, a 4.7-μF low-ESR ceramic capacitor is recommended on the input. When operating near the maximum load of 250 mA, after taking into the DC bias derating, a minimum recommended input capacitance is 2 μF or larger. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution.

8.2.2.5.3 Flying Capacitor

The flying capacitor (C_1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM27762 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and charge pump output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 0.47-μF or 1-μF 10-V low-ESR ceramic capacitors are recommended for the flying capacitors. Polarized capacitors (tantalum, aluminum, electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM27762 operation.

8.2.2.5.4 LDO Output Capacitor

The LDO output capacitor (C_{OUT+} , C_{OUT-}) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27762 only requires the use of a 2.2-μF ceramic output capacitor for stable operation. For typical applications, a 2.2-μF ceramic output capacitor located close to the output is sufficient.

8.2.2.6 Power Dissipation

The allowed power dissipation for any package is a measure of the ability of the device to pass heat from the junctions of the device to the heatsink and the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation can be calculated by 式 4:

$$P_{D-MAX} = (T_{J-MAX} - T_A) / R_{\theta JA} \quad (4)$$

The actual power being dissipated in the device can be represented by 式 5:

$$P_D = P_{IN} - P_{OUT} = V_{IN} \times (-I_{OUT-} + I_{OUT+} + I_Q) - (V_{OUT+} \times I_{OUT+} + V_{OUT-} \times I_{OUT-}) \quad (5)$$

式 4 and 式 5 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These equations must be used to determine the optimum operating conditions for the device in a given application.

In lower power dissipation applications the maximum ambient temperature (T_{A-MAX}) may be increased. In higher power dissipation applications the maximum ambient temperature (T_{A-MAX}) may have to be derated. T_{A-MAX} can be calculated using 式 6:

$$T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$$

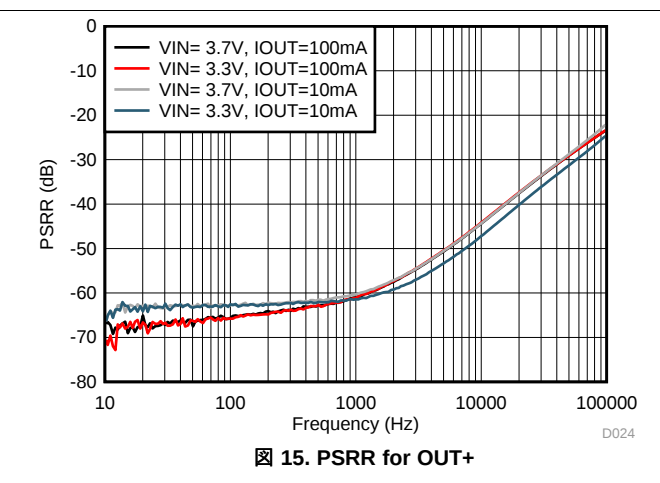
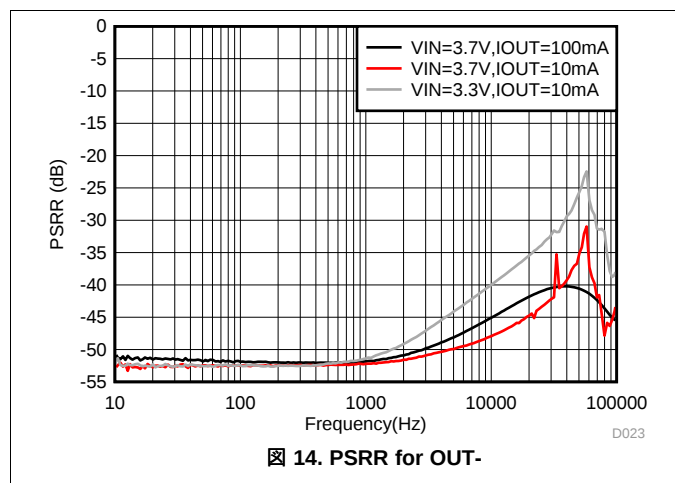
where

- $T_{J-MAX-OP}$ = maximum operating junction temperature (125°C)
 - P_{D-MAX} = the maximum allowable power dissipation
 - $R_{\theta JA}$ = junction-to-ambient thermal resistance of the package
- (6)

Alternately, if T_{A-MAX} cannot be derated, the power dissipation value must be reduced. This can be accomplished by reducing the input voltage as long as the minimum V_{IN} is not violated, or by reducing the output current, or some combination of the two.

8.2.3 Application Curves

Refer also to [Typical Characteristics](#)



9 Power Supply Recommendations

The LM27762 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the LM27762, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

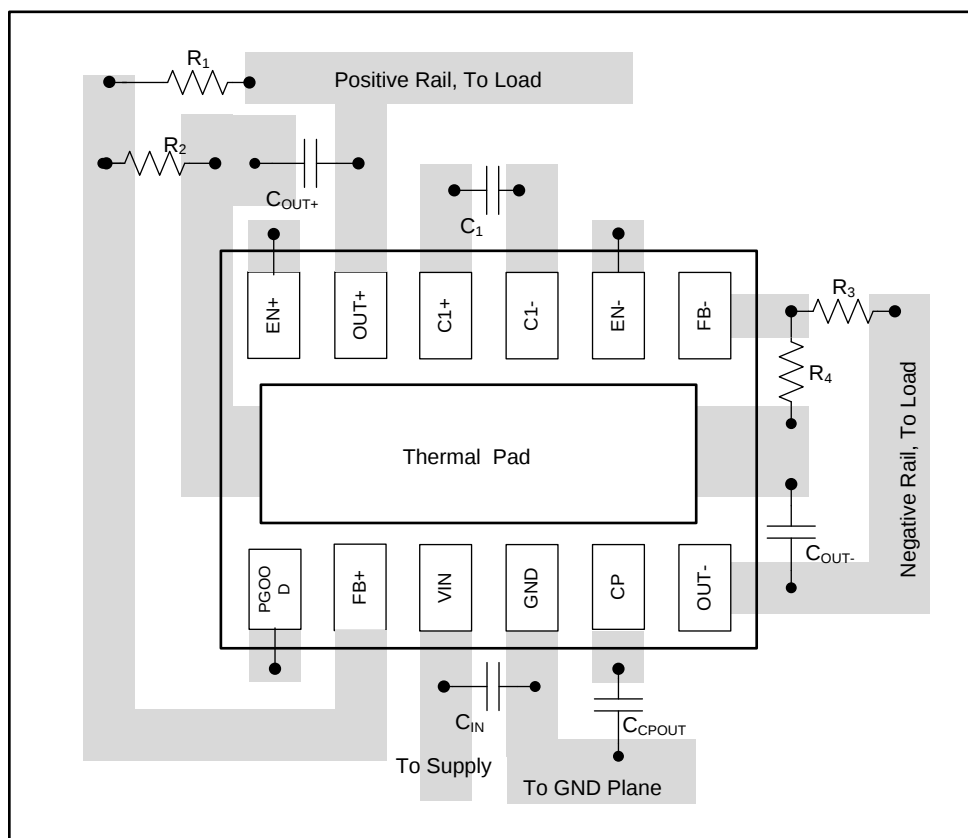
10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM27762 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place C_{IN} on the top layer (same layer as the LM27762) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching, which can corrupt the VIN line.
- Place C_{CPOUT} on the top layer (same layer as the LM27762) and as close as possible to the VOUT and GND pins. The returns for both C_{IN} and C_{CPOUT} must come together at one point, as close as possible to the GND pin. Connecting C_{CPOUT} through short, wide traces reduces the series inductance on the VCPOUT and GND pins that can corrupt the VCPOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C_1 on top layer (same layer as the LM27762) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.
- Place C_{OUT+} , C_{OUT-} on the top layer (same layer as the LM27762) and as close to the respective OUT pin as possible. For best performance the ground connection for C_{OUT} must connect back to the GND connection at the thermal pad of the device.
- Place R_1 to R_4 on the top layer (same layer as LM27762) and as close as possible to the respective FB pin. For best performance the ground connection of R_2 , R_4 must connect back to the GND connection at the thermal pad of the device.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

10.2 Layout Example



✕ 16. LM27762 Layout Example
(Note: Pullup resistor for PGOOD not shown in example.)

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

- 『[LM27762EVM評価モジュールの使用法](#)』

11.1.1 開発サポート

11.1.1.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、LM27762デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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11.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM27762DSSR	Active	Production	WSO (DSS) 12	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSSR.A	Active	Production	WSO (DSS) 12	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSSRG4.A	Active	Production	WSO (DSS) 12	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSST	Active	Production	WSO (DSS) 12	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSST.A	Active	Production	WSO (DSS) 12	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

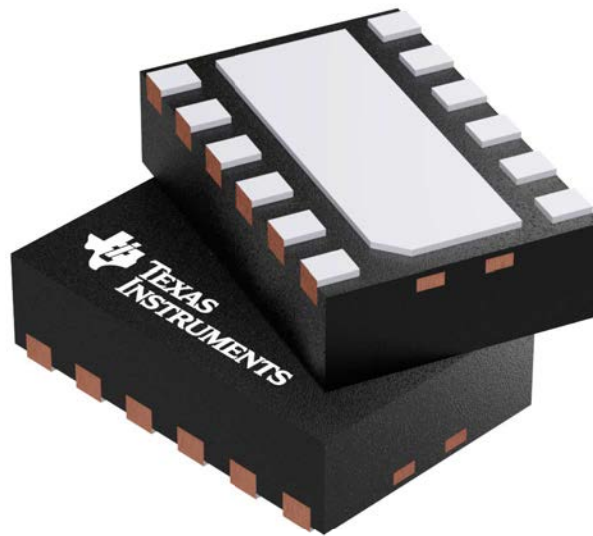
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27762DSSR	WSO	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LM27762DSST	WSO	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

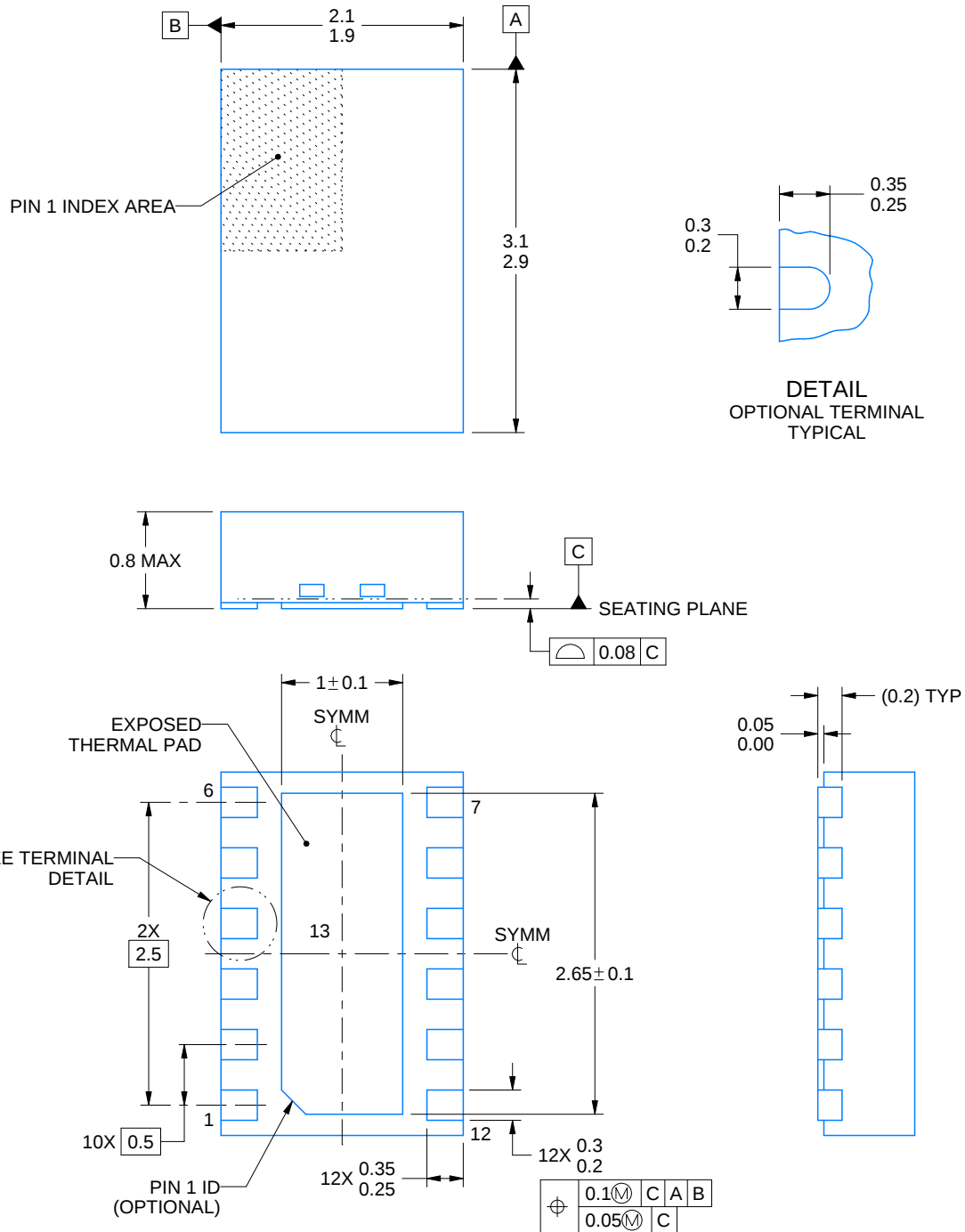
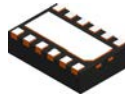


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27762DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
LM27762DSST	WSON	DSS	12	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4218908/A 01/2017

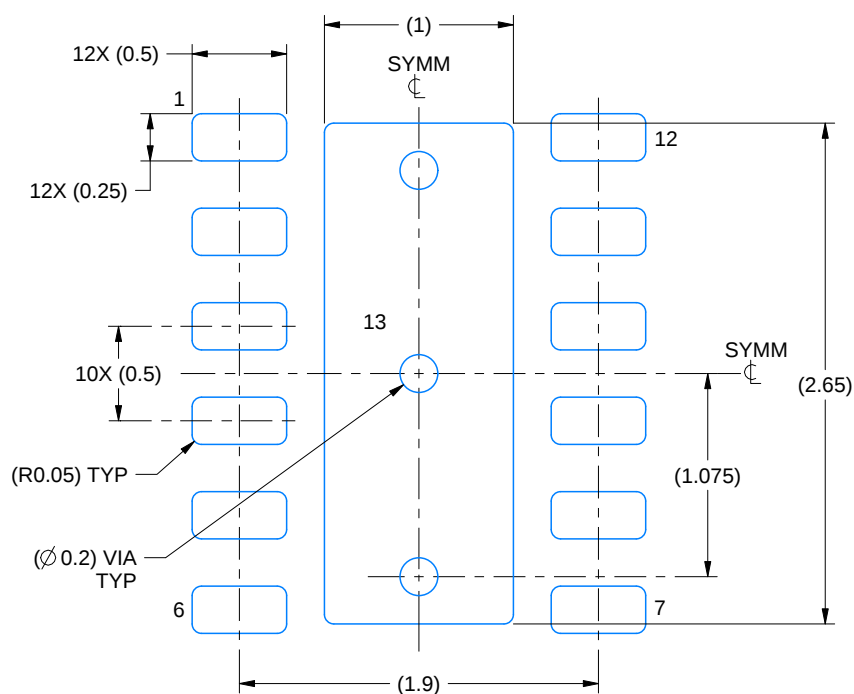
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

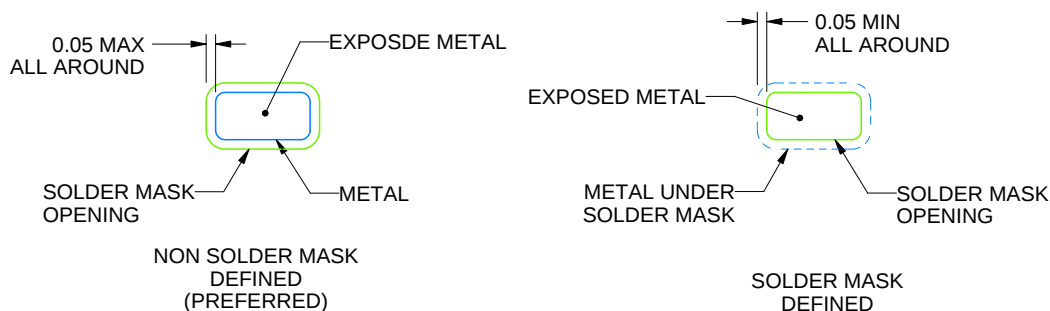
DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4218908/A 01/2017

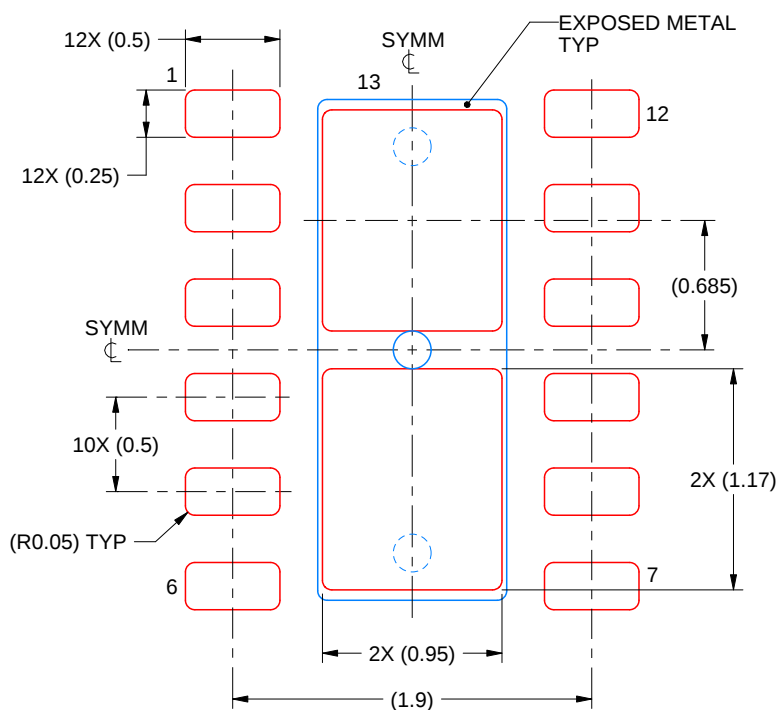
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218908/A 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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