THS4509 広帯域、低ノイズ、低歪み率、完全差動アンプ

1 特長

- 完全差動アーキテクチャ
- 電源電圧の中点の同相入力範囲
- 出力同相モード制御
- 2V/V (6dB)の最小ゲイン
- 帯域幅: 1900MHz
- スルーレート: 6600V/µs
- 1%セトリング·タイム: 2ns
- HD_2: 100MHzで–75dBc
- HD_3: 100MHzで–80dBc
- OIP_3: 70MHzで37dBm
- 入力電圧ノイズ: 1.9 nV/√Hz (f > 10MHz)
- 電源電圧: 3V～5V
- 電源電流: 37.7mA
- パワーダウン時電流: 0.65mA

2 アプリケーション

- 5Vデータ収集システム
  高直線性ADCアンプ
- ワイヤレス通信
- 医療用画像処理
- 試験/測定機器

3 概要

THS4509は広帯域の完全差動オペアンプで、5Vのデータ収集システム用に設計されています。1.9nV/√Hzの低ノイズで、高調波歪みも100MHz、$2V_{PP}$、G = 10dB、1kΩ負荷で–75dBc HD_2および–80dBc HD_3と低いのが特長です。スルーレートが6600V/µsと高く、セトリング·タイムは1% (2Vステップ)に対して2nsであるため、パルスを使用するアプリケーションに理想的です。最小ゲインは6dBに設計されていますが、10dBのゲインに最適化されています。

A/Dコンバータ(ADC)へのDCカップリングを可能にするため、独自の出力同相制御回路により、設定電圧から3mVオフセット(標準値)内に出力同相電圧が維持されます。このときの条件は、設定電圧が電源電圧の中点から0.5Vの範囲内であり、差動オフセット電圧が4mV未満です。同相電圧の設定点は内部回路により電源電圧の中点に設定され、また外部電源からオーバードライブすることができます。

入力および出力は、同相電圧を電源電圧の中点に設定したときに最高の特性になるように最適化されています。低電源電圧時の高性能と合わせて、この設計は高性能の単一電源5Vデータ収集システムに理想的です。THS4509の総合的な性能は、ADS5500 ADCを駆動し、10dBゲイン、125MSPSのサンプリング速度のとき、SFDRが81dBc、SNRが69.1dBc、70MHzにおいて-1dBFS信号です。

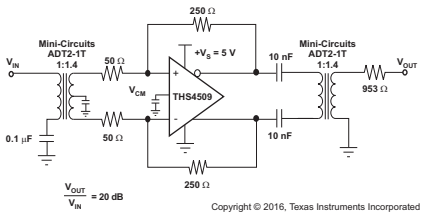
THS4509はクワッドのリードレスVQFN-16パッケージ(RGT)で供給され、完全な工業用温度範囲の-40℃～-85℃で動作が規定されています。

製品情報(1)

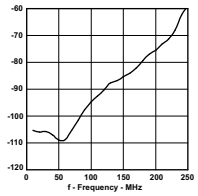
型番	パッケージ	本体サイズ(公称)
THS4509	VQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

テスト構成



測定された3次の相互変調スプリアス信号レベル



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision H (November 2009) から **Revision I** に変更 **Page**

- 「*ESD定格*」の表、「*熱に関する情報*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「*パッケージング/注文情報*」表を削除、データシートの末尾にあるPOAを参照 ... 1
- Deleted the *THS4509 EVM* section to the *Layout Example* section ... 37

Revision G (May 2008) から **Revision H** に変更 **Page**

- Changed title of *Typical Characteristics: $V_{S+} – V_{S–}$ = 5 V* ... 10
- Deleted conditions from *Typical Characteristics: $V_{S+} – V_{S–}$ = 5 V* table of graphs ... 10
- Changed title of *Typical Characteristics: $V_{S+} – V_{S–}$ = 3 V* ... 18
- Deleted conditions from *Typical Characteristics: $V_{S+} – V_{S–}$ = 3 V* table of graphs ... 18
- Added y-axis to Figure 87 ... 33
- Added y-axis to Figure 90 ... 35
- Changed item 10 in *Layout Recommendations* section ... 36
- Added the *PowerPAD PCB Layout Considerations* section ... 36
- Moved Figure 92 and associated paragraph to *PowerPAD PCB Layout Considerations* section ... 36
- Added the *PowerPAD Design Considerations* section ... 38

Revision F (October 2007) から **Revision G** に変更 **Page**

- ドキュメントのフォーマットを更新 ... 1
- Changed common-mode range column for THS4509 and THS4513 rows in the *Related Products* table ... 4
- Added footnote 1 to Absolute Maximum Ratings table ... 5
- Added V (volts) to unit column of ESD ratings rows in Absolute Maximum Ratings table ... 5

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- Changed $V_{S+} – V_{S–}$ = 5 V *Input* specifications from 1.75 V typ (common-mode input range high) to 1.4 V typ; –1.75 V (common-mode input range low) to –1.4 V; 1.35 MΩ || 1.77 pF (differential input impedance) to 1.3 MΩ || 1.8 pF; 1.02 MΩ || 2.26 pF (common-mode input impedance) to 1.0 MΩ || 2.3 pF 6
- Changed $V_{S+} – V_{S–}$ = 5 V *Input* specifications from 1.75 V typ (common-mode input range high) to 1.4 V typ; –1.75 V (common-mode input range low) to –1.4 V; 1.35 MΩ || 1.77 pF (differential input impedance) to 1.3 MΩ || 1.8 pF; 1.02 MΩ || 2.26 pF (common-mode input impedance) to 1.0 MΩ || 2.3 pF 7
- Changed $V_{S+} – V_{S–}$ = 3 V *Input* specifications from 0.75 V typ (common-mode input range high) to 0.4 V typ; –0.75 V (common-mode input range low) to –0.4 V; 1.35 MΩ || 1.77 pF (differential input impedance) to 1.3 MΩ || 1.8 pF; 1.02 MΩ || 2.26 pF (common-mode input impedance) to 1.0 MΩ || 2.3 pF 8

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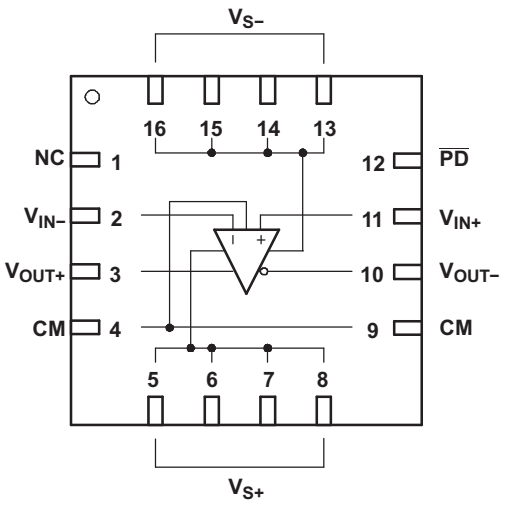
5 Device Comparison Table

DEVICE	MIN. GAIN	COMMON-MODE RANGE OF INPUT(1)
THS4508	6 dB	–0.3 V to 2.3 V
THS4509	6 dB	1.1 V to 3.9 V
THS4511	0 dB	–0.3 V to 2.3 V
THS4513	0 dB	1.1 V to 3.9 V

(1) Assumes a 5-V single-ended power supply

6 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1	N/A	No internal connection
$V_{IN–}$	2	I	Inverting amplifier input
V_{OUT+}	3	O	Noninverting amplifier output
CM	4, 9	I	Common-mode voltage input
V_{S+}	5-8	P	Positive amplifier power-supply input
$V_{OUT–}$	10	O	Inverted amplifier output
V_{IN+}	11	I	Noninverting amplifier input
$\overline{PD}$	12	I	Power-down; $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation
$V_{S–}$	13, 14, 15, 16	P	Negative amplifier power-supply input

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		6	V
V_I	Input voltage		$\pm V_S$	
V_{ID}	Differential input voltage		4	V
I_O	Output current(2)		200	mA
	Continuous power dissipation	See *Dissipation Ratings*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The THS4509 incorporates a (QFN) exposed thermal pad on the underside of the chip. This pad acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the QFN thermally-enhanced package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	3	5	5.25	V
Ambient temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS4509 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V

Test conditions are at V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
Small-signal bandwidth	G = 6 dB, V_O = 100 mV_{PP}		C		2		GHz
	G = 10 dB, V_O = 100 mV_{PP}				1.9		GHz
	G = 14 dB, V_O = 100 mV_{PP}				600		MHz
	G = 20 dB, V_O = 100 mV_{PP}				275		MHz
Gain-bandwidth product	G = 20 dB				3		GHz
Bandwidth for 0.1-dB flatness	G = 10 dB, V_O = 2 V_{PP}				300		MHz
Large-signal bandwidth	G = 10 dB, V_O = 2 V_{PP}				1.5		GHz
Slew rate (differential)	2-V step				6600		V/µs
Rise time					0.5		ns
Fall time					0.5		
Settling time to 1%					2		
Settling time to 0.1%					10		
2nd-order harmonic distortion	f = 10 MHz				–104		dBc
	f = 50 MHz				–80		
	f = 100 MHz				–68		
3rd-order harmonic distortion	f = 10 MHz				–108		dBc
	f = 50 MHz				–92		
	f = 100 MHz				–81		
2nd-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–78		dBc
		f_C = 140 MHz			–64		
3rd-order intermodulation distortion		f_C = 70 MHz			–95		
		f_C = 140 MHz			–78		
2nd-order output intercept point	200-kHz tone spacing R_L = 100 Ω, referenced to 50-Ω output	f_C = 70 MHz			78		dBm
		f_C = 140 MHz			58		
3rd-order output intercept point		f_C = 70 MHz			43		
		f_C = 140 MHz			38		
1-dB compression point	f_C = 70 MHz				12.2		dBm
	f_C = 140 MHz				10.8		
Noise figure	50-Ω system, 10 MHz				17.1		dB
Input voltage noise	f > 10 MHz				1.9		nV/√Hz
Input current noise	f > 10 MHz				2.2		pA/√Hz
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})			C		68		dB
Input offset voltage	T_A = +25°C		A		1	4	mV
	T_A = –40°C to +85°C				1	5	mV
Average offset voltage drift	T_A = –40°C to +85°C		B		2.6		µV/°C
Input bias current	T_A = +25°C		A		8	15.5	µA
	T_A = –40°C to +85°C				8	18.5	
Average bias current drift	T_A = –40°C to +85°C		B		20		nA/°C
Input offset current	T_A = +25°C		A		1.6	3.6	µA
	T_A = –40°C to +85°C				1.6	7	
Average offset current drift	T_A = –40°C to +85°C		B		4		nA/°C

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions are at V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL (1)	MIN	TYP	MAX	UNIT
INPUT							
Common-mode input range high			B		1.4		V
Common-mode input range low					–1.4		
Common-mode rejection ratio					90		dB
Differential input impedance			C		1.3 || 1.8		MΩ || pF
Common-mode input impedance			C		1.0 || 2.3		MΩ || pF
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to midsupply	T_A = +25°C	A	1.2	1.4		V
		T_A = –40°C to +85°C		1.1	1.4		
Minimum output voltage low		T_A = +25°C			–1.4	–1.2	V
		T_A = –40°C to +85°C			–1.4	–1.1	
Differential output voltage swing				4.8	5.6		V
	T_A = –40°C to +85°C			4.4			
Differential output current drive	R_L = 10 Ω		C		96		mA
Output balance error	V_O = 100 mV, f = 1 MHz				–49		dB
Closed-loop output impedance	f = 1 MHz				0.3		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth			C		700		MHz
Slew rate					110		V/μs
Gain					1		V/V
Output common-mode offset from CM input	1.25 V < CM < 3.5 V				5		mV
CM input bias current	1.25 V < CM < 3.5 V				±40		μA
CM input voltage high					1.5		V
CM input voltage low					–1.5		
CM input impedance					23 || 1		kΩ || pF
CM default voltage					0		V
POWER SUPPLY							
Specified operating voltage			C	3	5	5.25	V
Maximum quiescent current	T_A = +25°C		A		37.7	40.9	mA
	T_A = –40°C to +85°C				37.7	41.9	
Minimum quiescent current	T_A = +25°C			34.5	37.7		mA
	T_A = –40°C to +85°C			33.5	37.7		
Power-supply rejection (±PSRR)			C		90		dB
POWER-DOWN - Referenced to V_{S-}							
Enable voltage threshold	Assured *on* above 2.1 V + V_{S-}		C		> 2.1 + V_{S-}		V
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}				< 0.7 + V_{S-}		V
Power-down quiescent current	T_A = +25°C		A		0.65	0.9	mA
	T_A = –40°C to +85°C				0.65	1	
Input bias current	$\overline{PD}$ = V_{S-}		C		100		μA
Input impedance					50 || 2		kΩ || pF
Turnon time delay	Measured to output on				55		ns
Turnoff time delay	Measured to output off				10		μs

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7.6 Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5 V, G = 10 dB, CM = open, V_O = 1 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
Small-signal bandwidth	G = 6 dB, V_O = 100 mV_{PP}		C		1.9		GHz
	G = 10 dB, V_O = 100 mV_{PP}				1.6		GHz
	G = 14 dB, V_O = 100 mV_{PP}				625		MHz
	G = 20 dB, V_O = 100 mV_{PP}				260		MHz
Gain-bandwidth product	G = 20 dB				3		GHz
Bandwidth for 0.1-dB flatness	G = 10 dB, V_O = 1 V_{PP}				400		MHz
Large-signal bandwidth	G = 10 dB, V_O = 1 V_{PP}				1.5		GHz
Slew rate (differential)	2-V step				3500		V/µs
Rise time					0.25		ns
Fall time					0.25		
Settling time to 1%					1		
Settling time to 0.1%					10		
2nd-order harmonic distortion	f = 10 MHz				–107		dBc
	f = 50 MHz				–83		
	f = 100 MHz				–60		
3rd-order harmonic distortion	f = 10 MHz				–87		dBc
	f = 50 MHz				–65		
	f = 100 MHz				–54		
2nd-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–77		dBc
		f_C = 140 MHz			–54		
3rd-order intermodulation distortion		f_C = 70 MHz			–77		
		f_C = 140 MHz			–62		
2nd-order output intercept point	200-kHz tone spacing R_L = 100 Ω	f_C = 70 MHz			72		dBm
		f_C = 140 MHz			52		
3rd-order output intercept point		f_C = 70 MHz			38.5		
		f_C = 140 MHz			30		
1-dB compression point	f_C = 70 MHz				2.2		dBm
	f_C = 140 MHz				0.25		
Noise figure	50 Ω system, 10 MHz				17.1		dB
Input voltage noise	f > 10 MHz				1.9		nV/√Hz
Input current noise	f > 10 MHz				2.2		pA/√Hz
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})			C		68		dB
Input offset voltage	T_A = +25°C				1		mV
Average offset voltage drift	T_A = –40°C to +85°C				2.6		µV/°C
Input bias current	T_A = +25°C				6		µA
Average bias current drift	T_A = –40°C to +85°C				20		nA/°C
Input offset current	T_A = +25°C				1.6		µA
Average offset current drift	T_A = –40°C to +85°C				4		nA/°C

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5 V, G = 10 dB, CM = open, V_O = 1 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
INPUT							
Common-mode input range high			B		0.4		V
Common-mode input range low					–0.4		
Common-mode rejection ratio					80		dB
Differential input impedance			C		1.3 || 1.8		MΩ || pF
Common-mode input impedance			C		1.0 || 2.3		MΩ || pF
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to midsupply	T_A = +25°C	C		0.45		V
Minimum output voltage low		T_A = +25°C			–0.45		V
Differential output voltage swing					1.8		V
Differential output current drive	R_L = 10 Ω				50		mA
Output balance error	V_O = 100 mV, f = 1 MHz				–49		dB
Closed-loop output impedance	f = 1 MHz				0.3		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth			C		570		MHz
Slew rate					60		V/μs
Gain					1		V/V
Output common-mode offset from CM input	1.25 V < CM < 3.5 V				4		mV
CM input bias current	1.25 V < CM < 3.5 V				±40		μA
CM input voltage high					1.5		V
CM input voltage low					–1.5		
CM input impedance					20 || 1		kΩ || pF
CM default voltage					0		V
POWER SUPPLY							
Specified operating voltage			C		3		V
Quiescent current	T_A = +25°C		A		34.8		mA
Power-supply rejection (±PSRR)			C		70		dB
POWER-DOWN Referenced to V_{S-}							
Enable voltage threshold	Assured *on* above 2.1 V + V_{S-}		C		> 2.1 + V_{S-}		V
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}				< 0.7 + V_{S-}		V
Power-down quiescent current					0.46		mA
Input bias current	$\overline{PD}$ = V_{S-}				65		μA
Input impedance					50 || 2		kΩ || pF
Turnon time delay	Measured to output on				100		ns
Turnoff time delay	Measured to output off				10		μs

7.7 Dissipation Ratings

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \le$ +25°C	T_A = +85°C
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

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7.8 Typical Characteristics

7.8.1 Typical Characteristics: $V_{S+} - V_{S-} = 5$ V

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

Table 1. Table of Graphs

			FIGURE
Small-Signal Frequency Response			Figure 1
Large-Signal Frequency Response			Figure 2
Harmonic Distortion	HD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 3
	HD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 4
	HD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 5
	HD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 6
	HD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 7
	HD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 8
	HD_2, G = 10 dB	vs Output Voltage	Figure 9
	HD_3, G = 10 dB	vs Output Voltage	Figure 10
	HD_2, G = 10 dB	vs Common-Mode Input Voltage	Figure 11
	HD_3, G = 10 dB	vs Common-Mode Input Voltage	Figure 12
Intermodulation Distortion	IMD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 13
	IMD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 14
	IMD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 15
	IMD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 16
	IMD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 17
	IMD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 18
Output Intercept Point	OIP_2	vs Frequency	Figure 19
	OIP_3	vs Frequency	Figure 20
0.1-dB Flatness			Figure 21
S-Parameters		vs Frequency	Figure 22
Transition Rate		vs Output Voltage	Figure 23
Transient Response			Figure 24
Settling Time			Figure 25
Rejection Ratio		vs Frequency	Figure 26
Output Impedance		vs Frequency	Figure 27
Overdrive Recovery			Figure 28
Output Voltage Swing		vs Load Resistance	Figure 29
Turnoff Time			Figure 30
Turnon Time			Figure 31
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 32
Open-Loop Gain		vs Frequency	Figure 33
Input-Referred Noise		vs Frequency	Figure 34
Noise Figure		vs Frequency	Figure 35
Quiescent Current		vs Supply Voltage	Figure 36
Power-Supply Current		vs Supply Voltage in Power-Down Mode	Figure 37
Output Balance Error		vs Frequency	Figure 38
CM Input Impedance		vs Frequency	Figure 39
CM Small-Signal Frequency Response			Figure 40
CM Input Bias Current		vs CM Input Voltage	Figure 41
Differential Output Offset Voltage		vs CM Input Voltage	Figure 42

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Typical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

Table 1. Table of Graphs (continued)

		FIGURE
Output Common-Mode Offset	vs CM Input Voltage	Figure 43

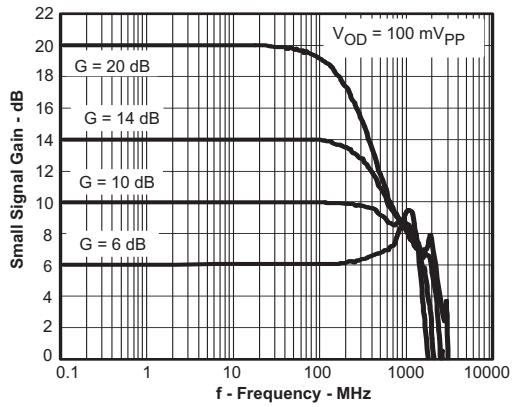

Figure 1. Small-Signal Frequency Response

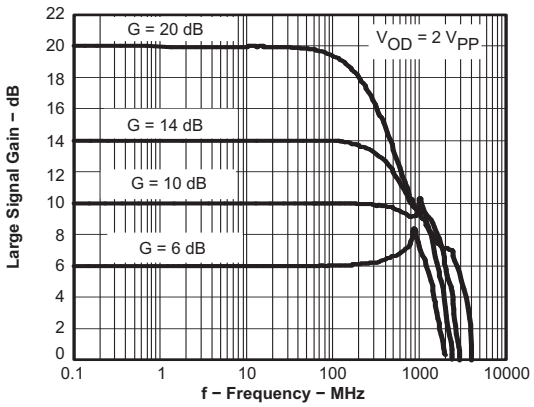

Figure 2. Large-Signal Frequency Response

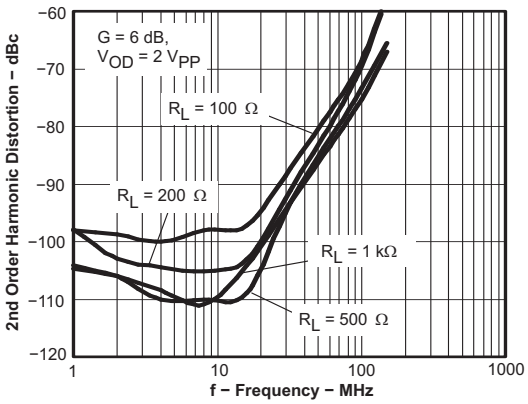

Figure 3. HD_2 vs Frequency

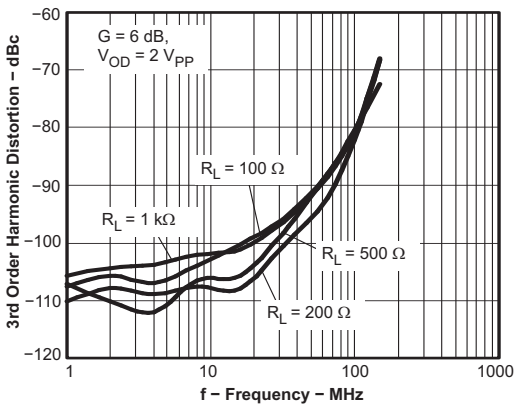

Figure 4. HD_3 vs Frequency

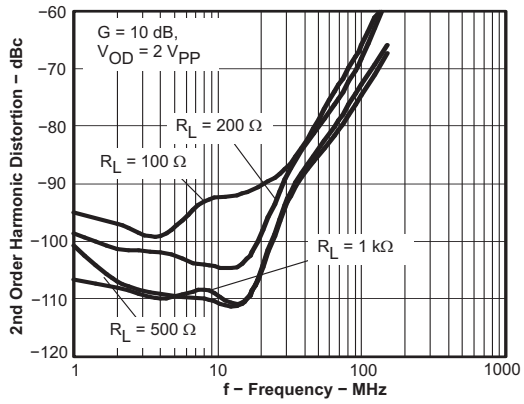

Figure 5. HD_2 vs Frequency

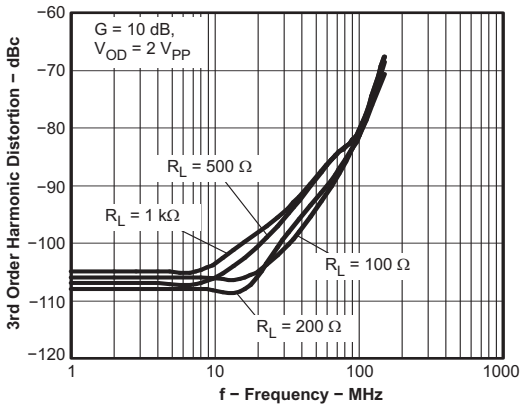

Figure 6. HD_3 vs Frequency

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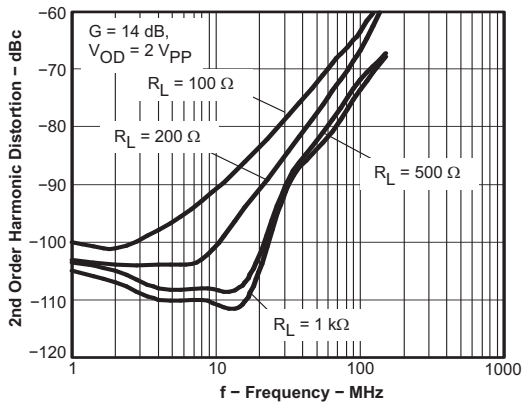

Figure 7. HD_2 vs Frequency

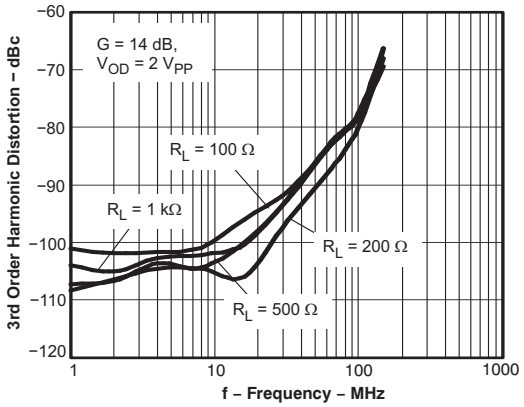

Figure 8. HD_3 vs Frequency

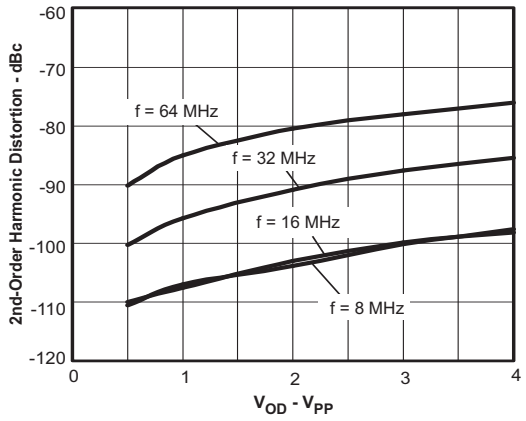

Figure 9. HD_2 vs Output Voltage

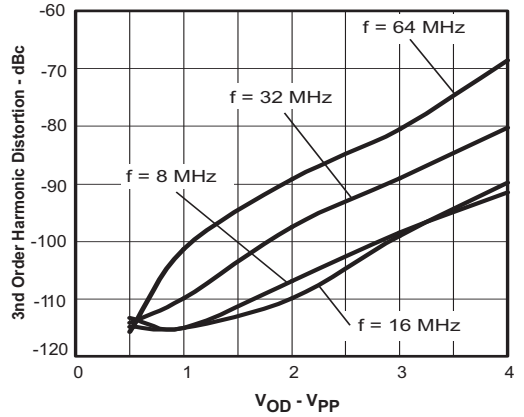

Figure 10. HD_3 vs Output Voltage

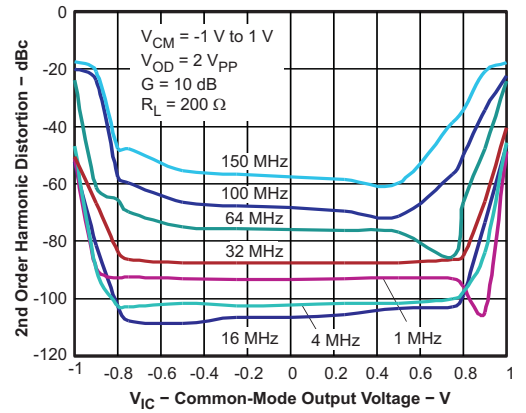

Figure 11. HD_2 vs Common-Mode Output Voltage

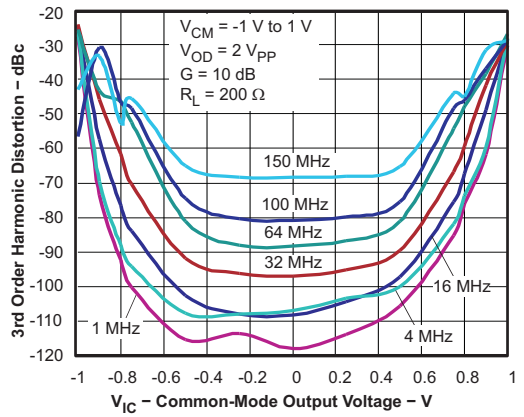

Figure 12. HD_3 vs Common-Mode Output Voltage

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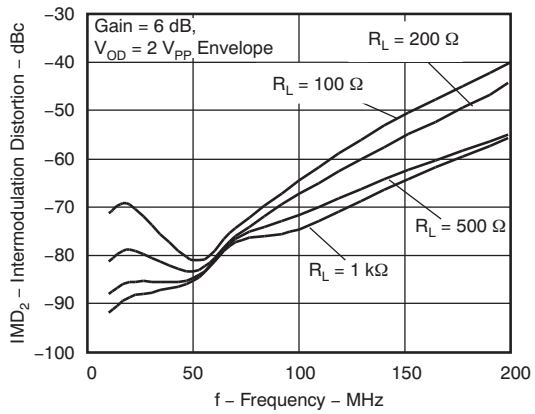

Figure 13. IMD_2 vs Frequency

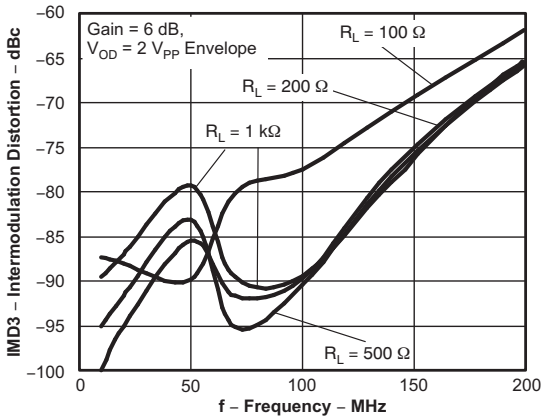

Figure 14. IMD_3 vs Frequency

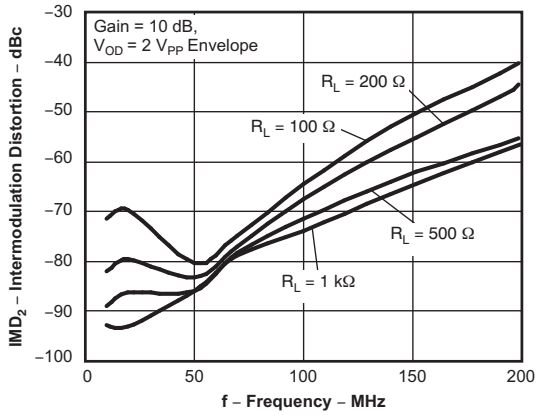

Figure 15. IMD_2 vs Frequency

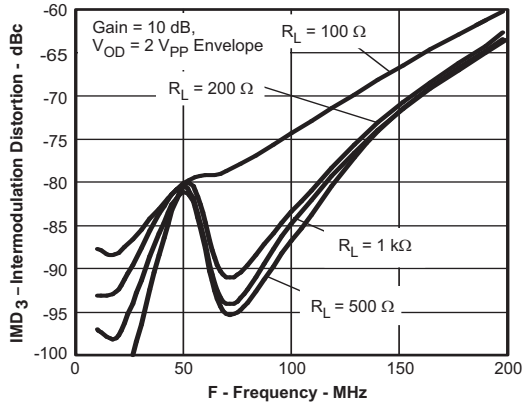

Figure 16. IMD_3 vs Frequency

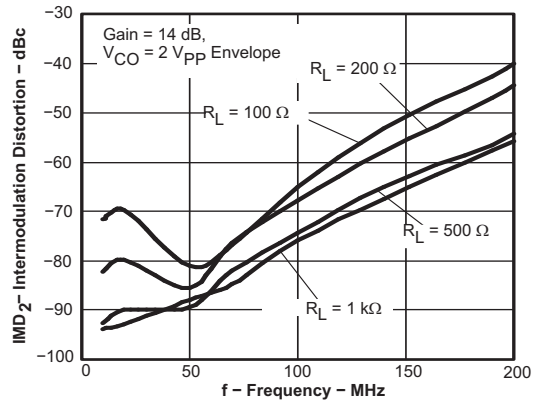

Figure 17. IMD_2 vs Frequency

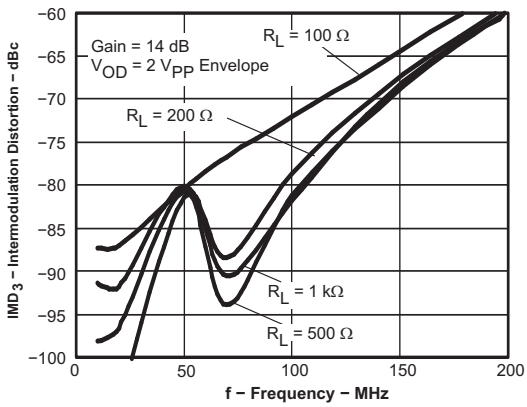

Figure 18. IMD_3 vs Frequency

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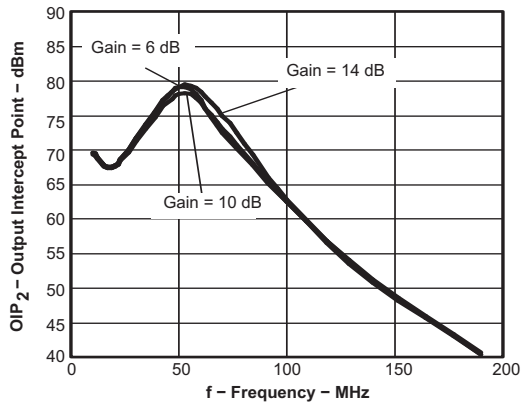

Figure 19. OIP_2 vs Frequency

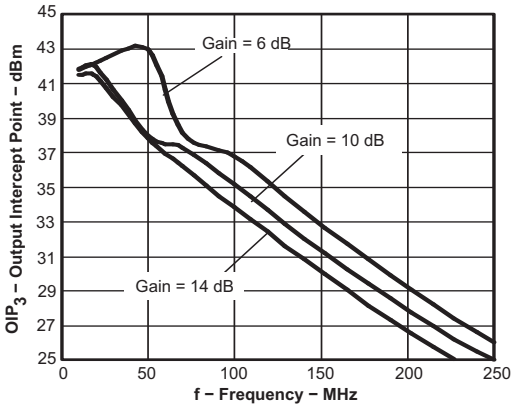

Figure 20. OIP_3 vs Frequency

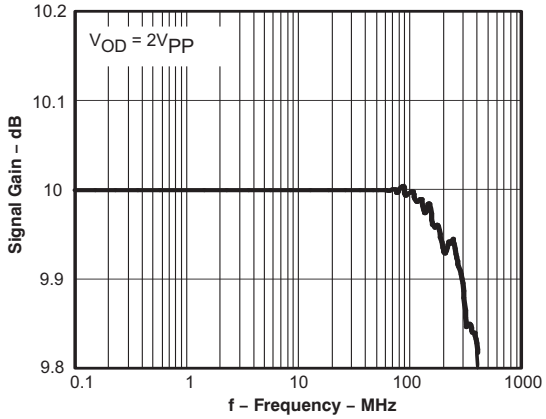

Figure 21. 0.1-dB Flatness

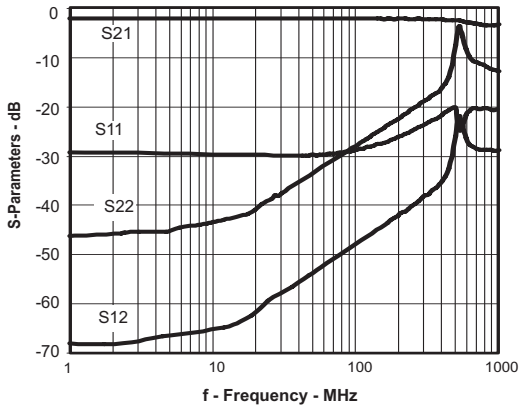

Figure 22. S-Parameters vs Frequency

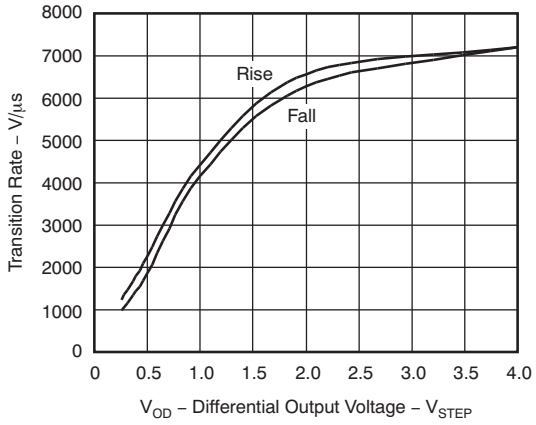

Figure 23. Transition Rate vs Output Voltage

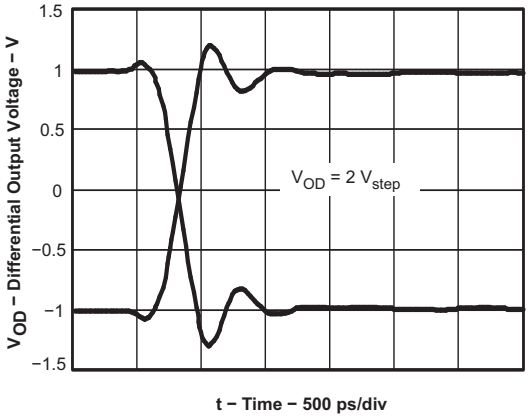

Figure 24. Transient Response

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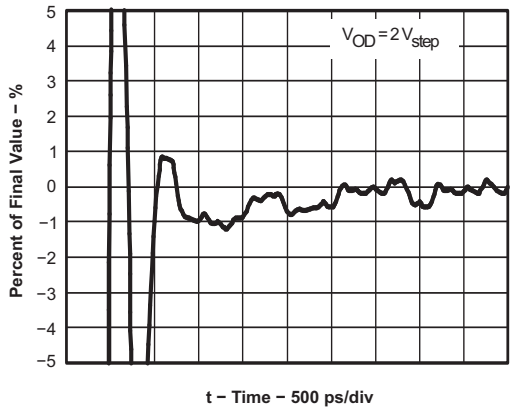

Figure 25. Settling Time

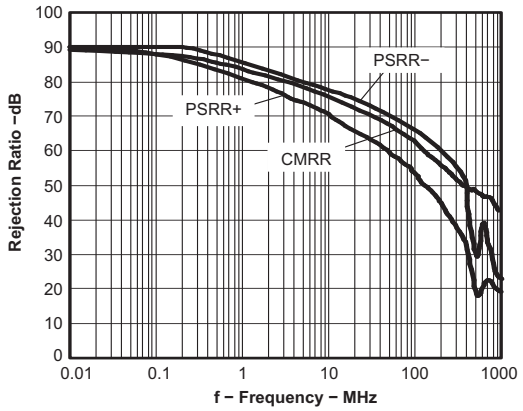

Figure 26. Rejection Ratio vs Frequency

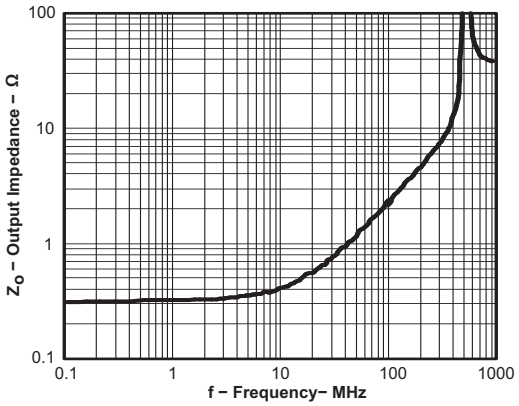

Figure 27. Output Impedance vs Frequency

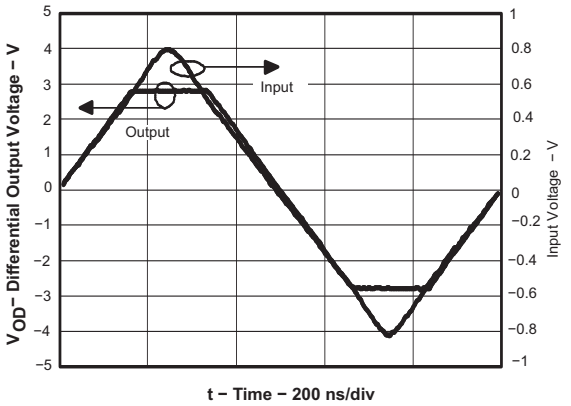

Figure 28. Overdrive Recovery

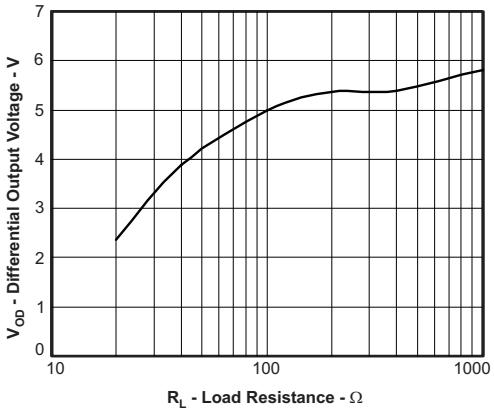

Figure 29. Output Voltage Swing vs Load Resistance

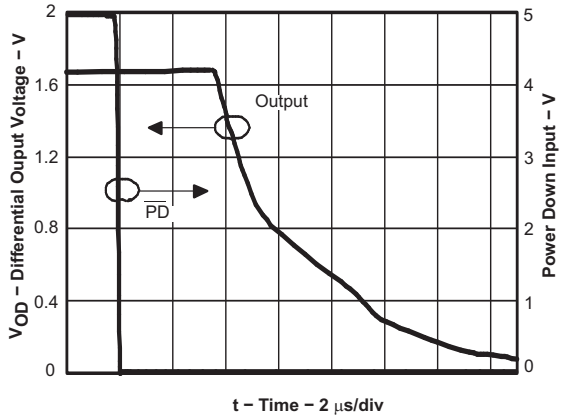

Figure 30. Turnoff Time

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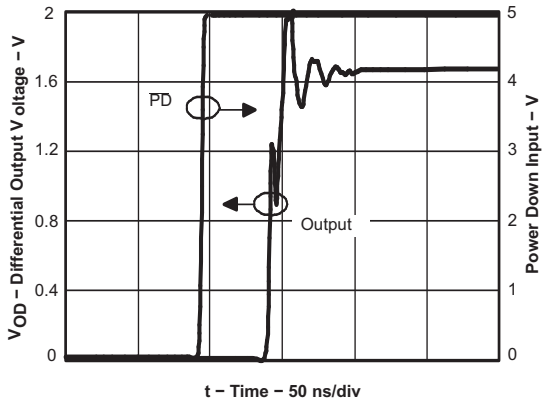

Figure 31. Turnon Time

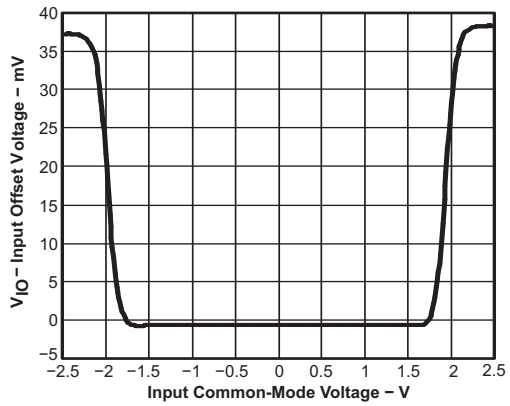

Figure 32. Input Offset Voltage vs Input Common-Mode Voltage

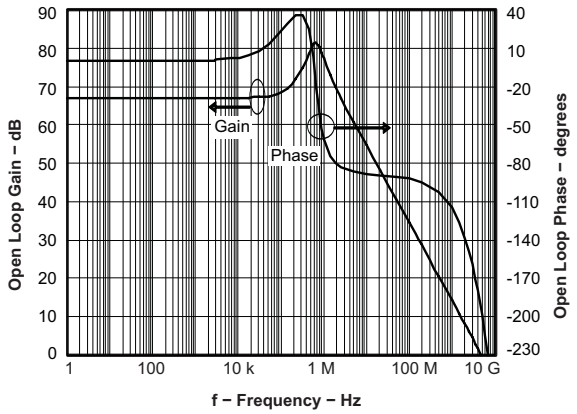

Figure 33. Open-Loop Gain and Phase vs Frequency

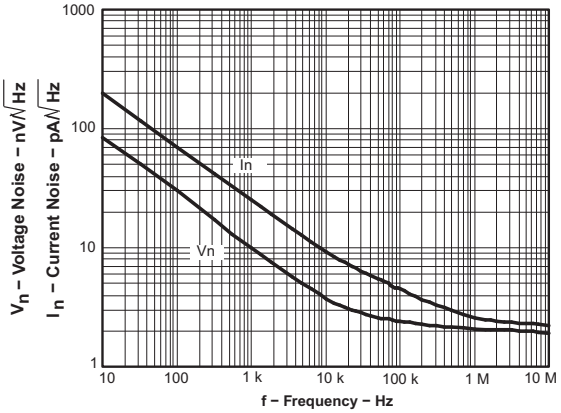

Figure 34. Input-Referred Noise vs Frequency

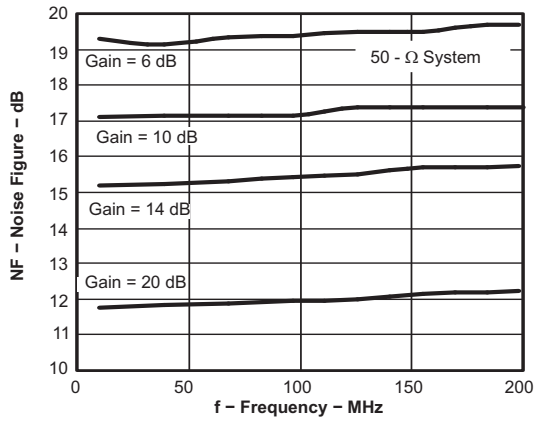

Figure 35. Noise Figure vs Frequency

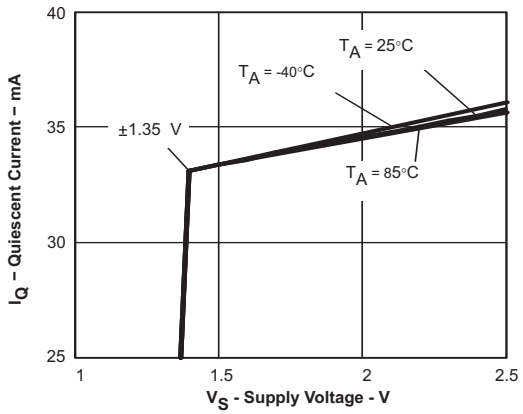

Figure 36. Quiescent Current vs Supply Voltage

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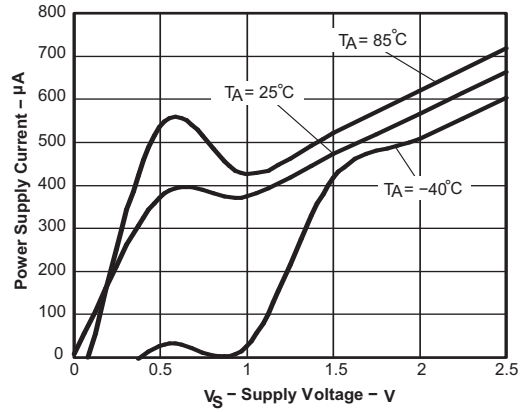

Figure 37. Power-Supply Current vs Supply Voltage in Power-Down Mode

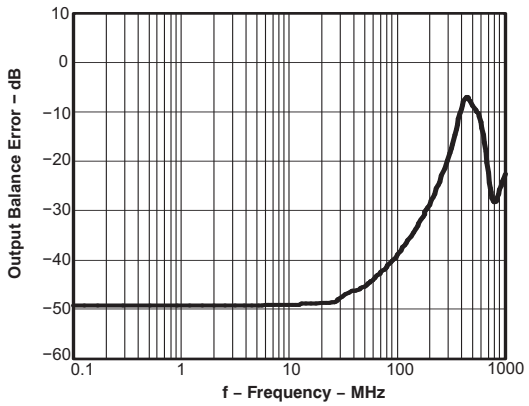

Figure 38. Output Balance Error vs Frequency

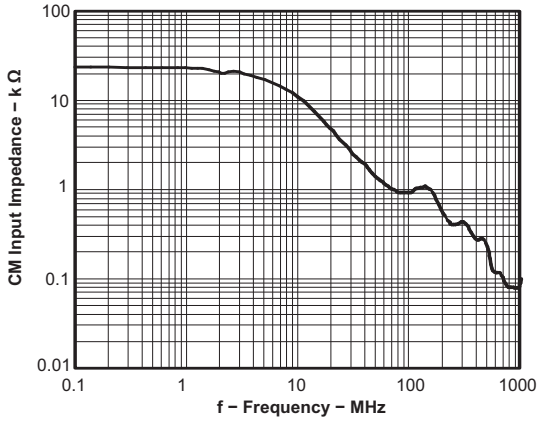

Figure 39. CM Input Impedance vs Frequency

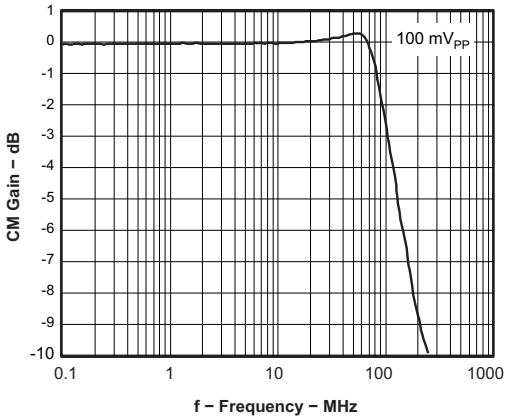

Figure 40. CM Small-Signal Frequency Response

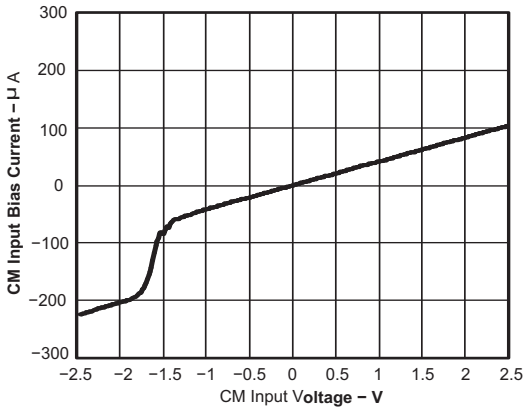

Figure 41. CM Input Bias Current vs CM Input Voltage

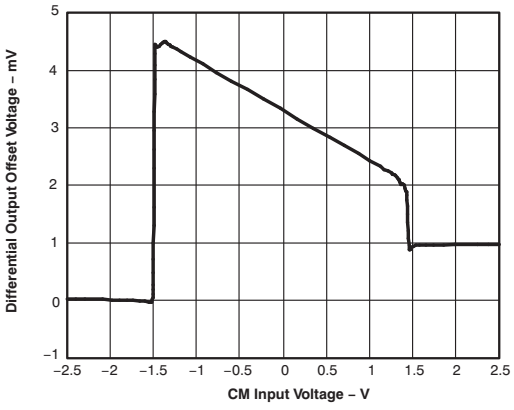

Figure 42. Differential Output Offset Voltage vs CM Input Voltage

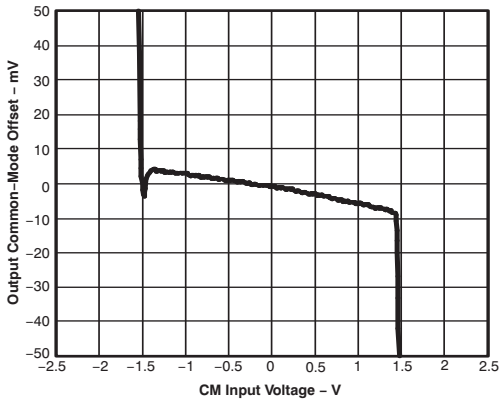

Figure 43. Output Common-Mode Offset vs CM Input Voltage

7.8.2 Typical Characteristics: $V_{S+} - V_{S-} = 3$ V

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5 V, CM = open, V_{OD} = 1 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, G = 10 dB, single-ended input, and input and output referenced to midrail, unless otherwise noted.

Table 2. Table of Graphs

			FIGURE
Small-Signal Frequency Response			Figure 44
Large-Signal Frequency Response			Figure 45
Harmonic Distortion	HD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 46
	HD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 47
	HD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 48
	HD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 49
	HD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 50
	HD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 51
Intermodulation Distortion	IMD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 52
	IMD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 53
	IMD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 54
	IMD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 55
	IMD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 56
	IMD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 57
Output Intercept Point	OIP_2	vs Frequency	Figure 58
	OIP_3	vs Frequency	Figure 59
0.1 dB Flatness			Figure 60
S-Parameters		vs Frequency	Figure 61
Transition Rate		vs Output Voltage	Figure 62
Transient Response			Figure 63
Settling Time			Figure 64
Output Voltage Swing		vs Load Resistance	Figure 65
Rejection Ratio		vs Frequency	Figure 66
Overdrive Recovery			Figure 67
Output Impedance		vs Frequency	Figure 68
Turnoff Time			Figure 69
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Output Balance Error		vs Frequency	Figure 71
Noise Figure		vs Frequency	Figure 72
CM Input Impedance		vs Frequency	Figure 73

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Typical Characteristics: $V_{S+} - V_{S-} = 3$ V (continued)

Table 2. Table of Graphs (continued)

		FIGURE
Differential Output Offset Voltage	vs CM Input Voltage	Figure 74
Output Common-Mode Offset	vs CM Input Voltage	Figure 75

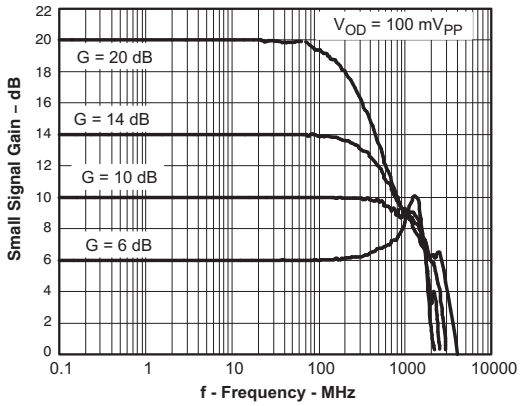

Figure 44. Small-Signal Frequency Response

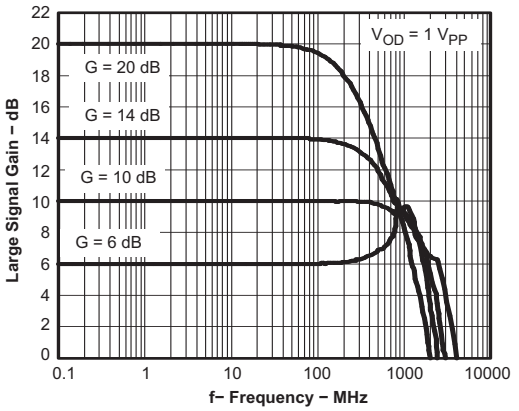

Figure 45. Large-Signal Frequency Response

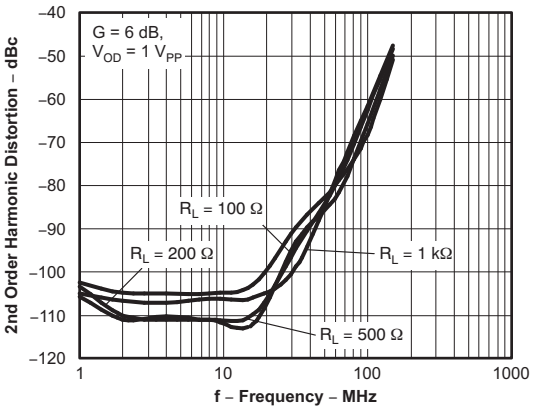

Figure 46. HD_2 vs Frequency

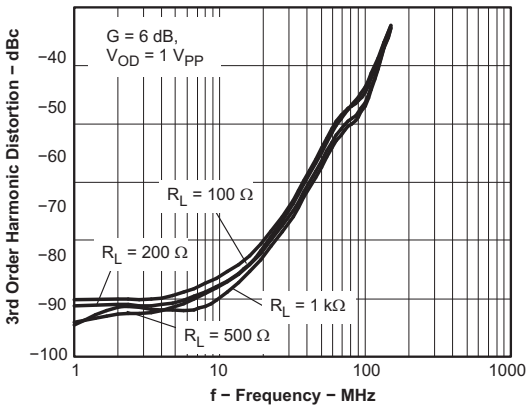

Figure 47. HD_3 vs Frequency

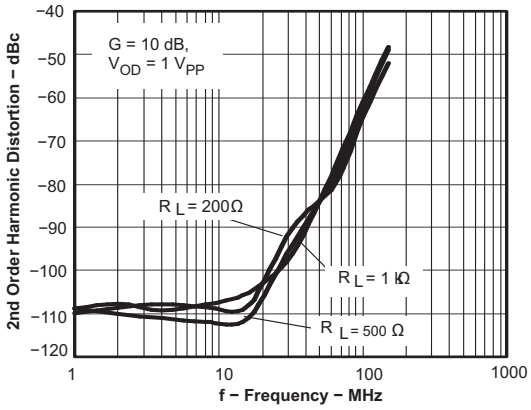

Figure 48. HD_2 vs Frequency

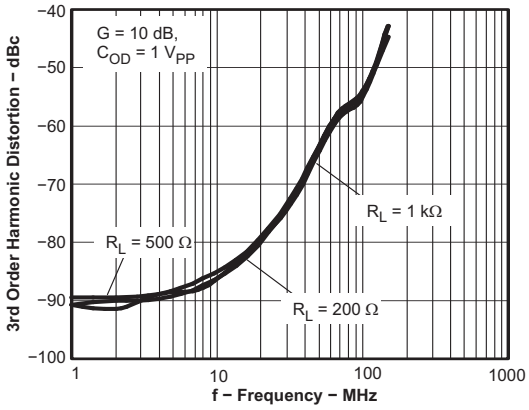

Figure 49. HD_3 vs Frequency

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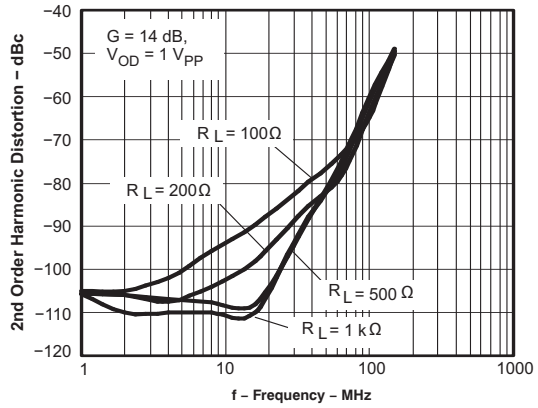

Figure 50. HD_2 vs Frequency

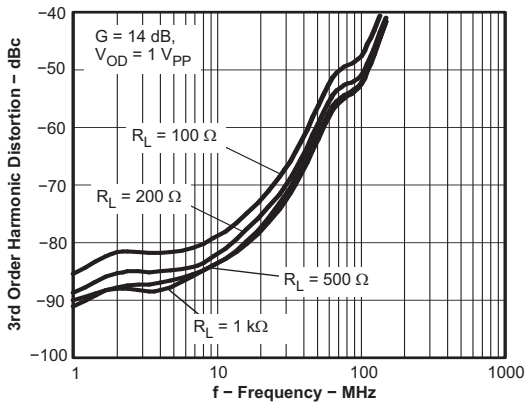

Figure 51. HD_3 vs Frequency

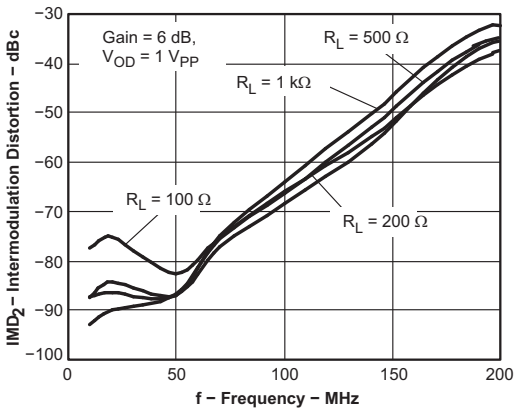

Figure 52. IMD_2 vs Frequency

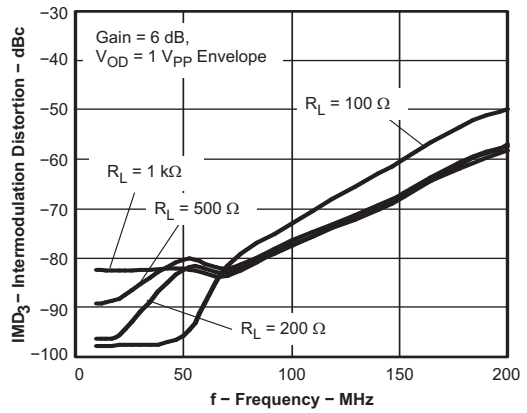

Figure 53. IMD_3 vs Frequency

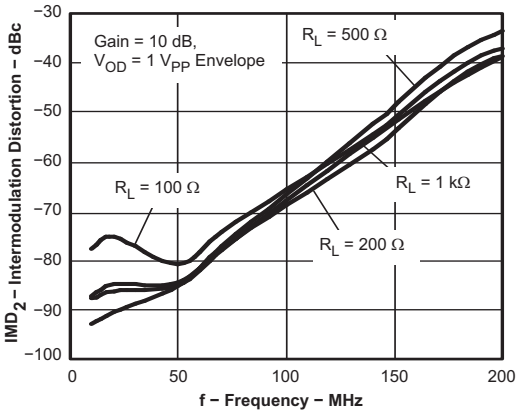

Figure 54. IMD_2 vs Frequency

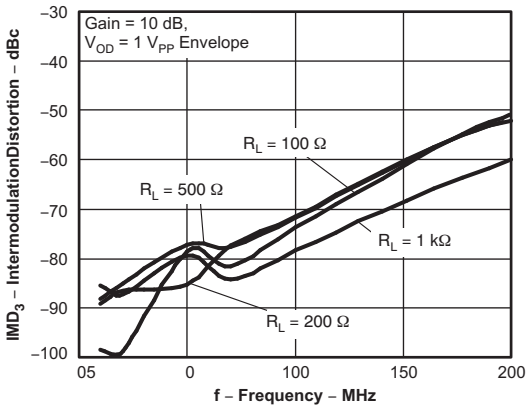

Figure 55. IMD_3 vs Frequency

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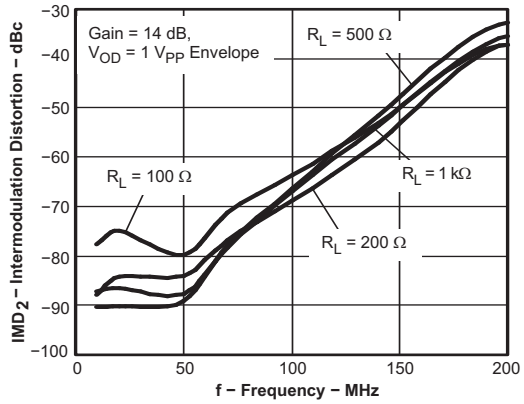

Figure 56. IMD_2 vs Frequency

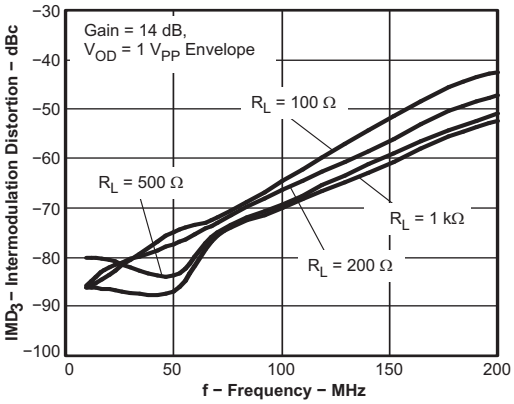

Figure 57. IMD_3 vs Frequency

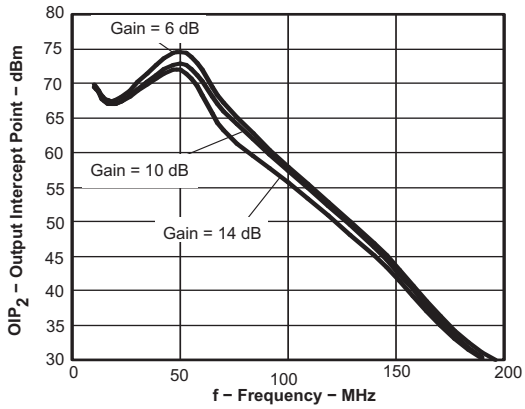

Figure 58. OIP_2, dBm vs Frequency

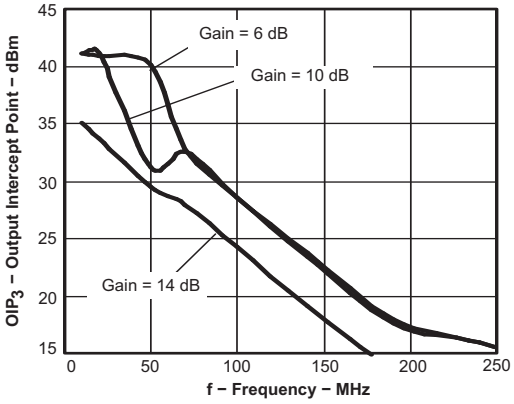

Figure 59. OIP_3, dBm vs Frequency

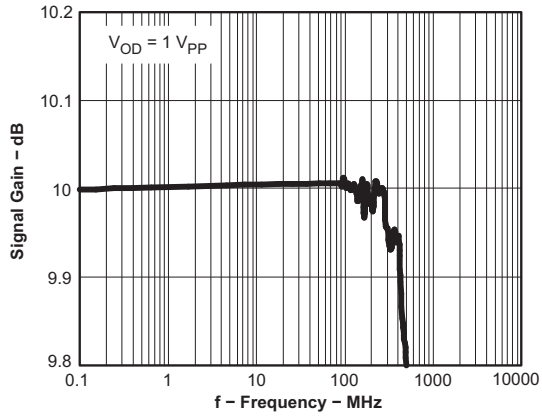

Figure 60. 0.1-dB Flatness

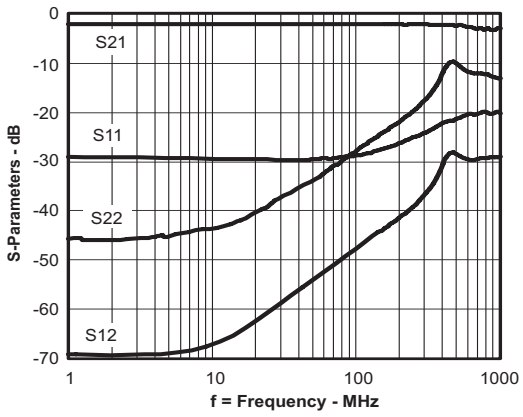

Figure 61. S-Parameters vs Frequency

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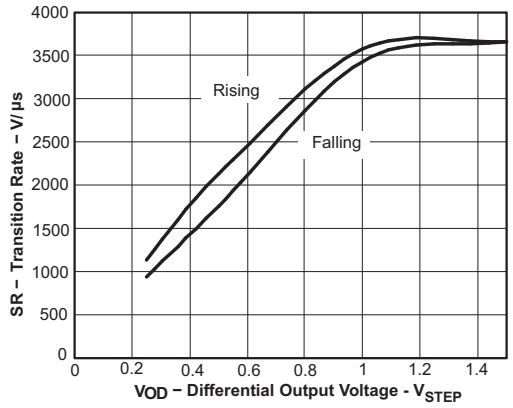

Figure 62. Transition Rate vs Output Voltage

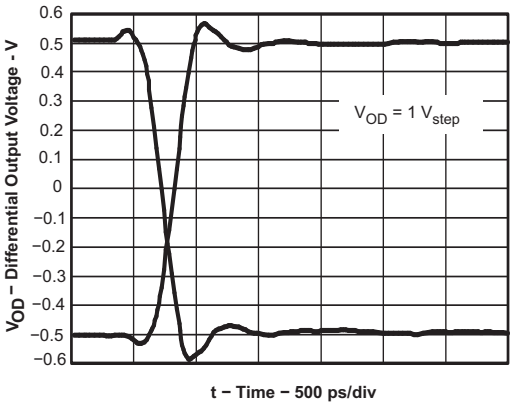

Figure 63. Transient Response

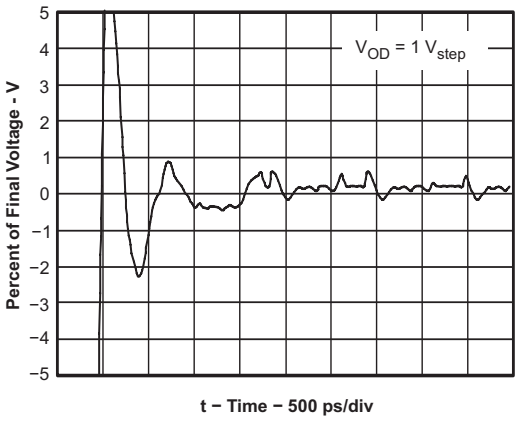

Figure 64. Settling Time

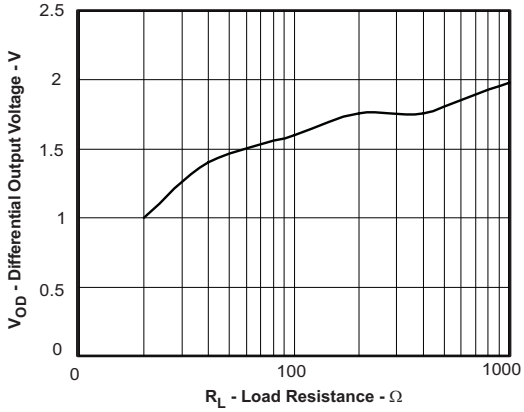

Figure 65. Output Voltage Swing vs Load Resistance

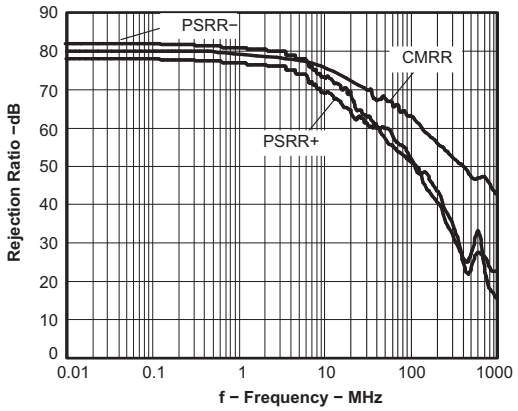

Figure 66. Rejection Ratio vs Frequency

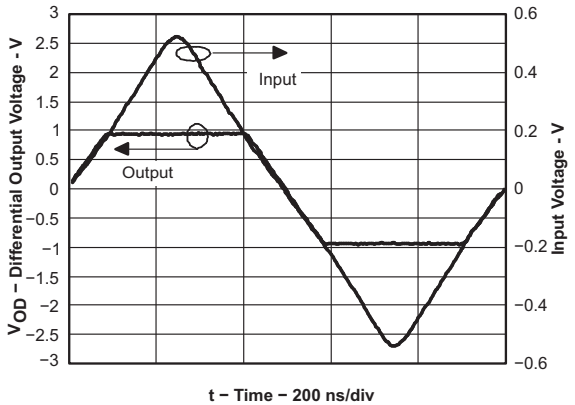

Figure 67. Overdrive Recovery

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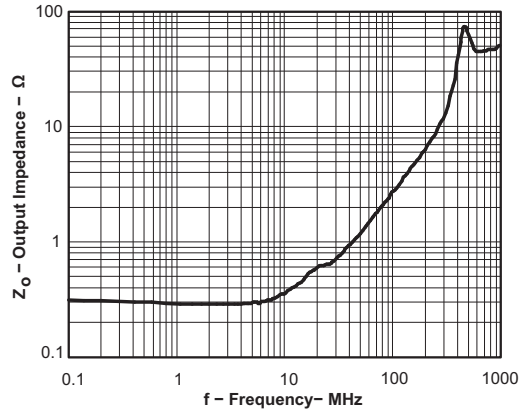

Figure 68. Output Impedance vs Frequency

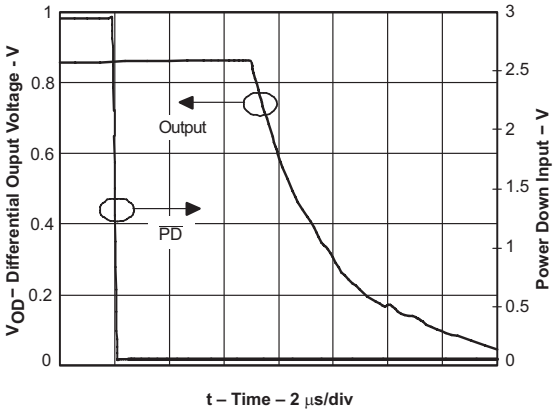

Figure 69. Turnoff Time

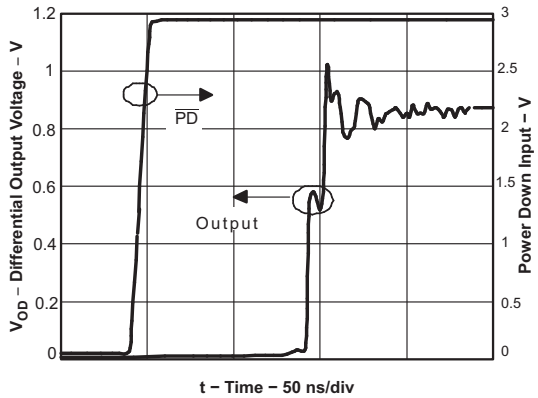

Figure 70. Turnon Time

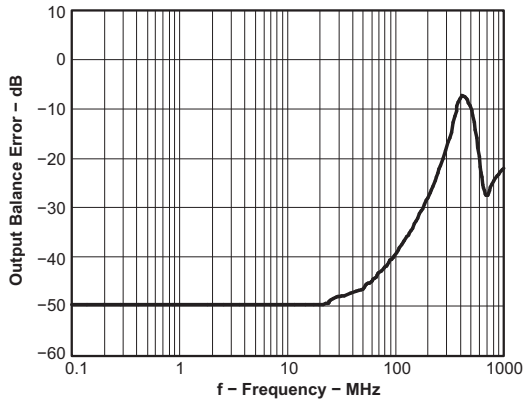

Figure 71. Output Balance Error vs Frequency

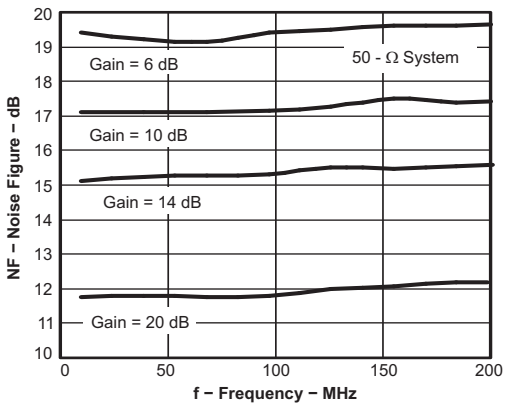

Figure 72. Noise Figure vs Frequency

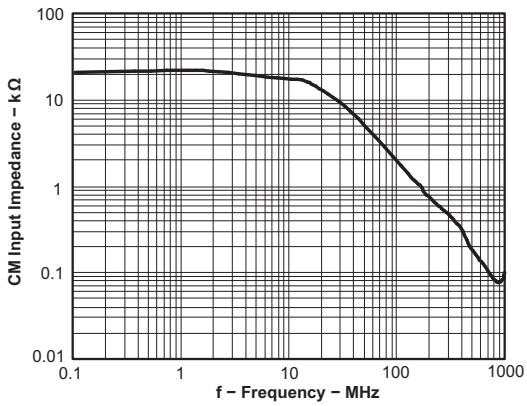

Figure 73. CM Input Impedance vs Frequency

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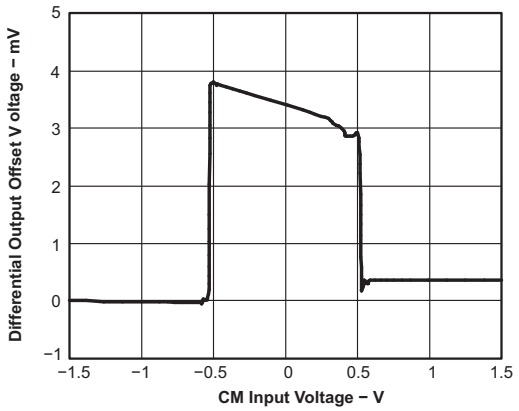

Figure 74. Differential Output Offset Voltage vs CM Input Voltage

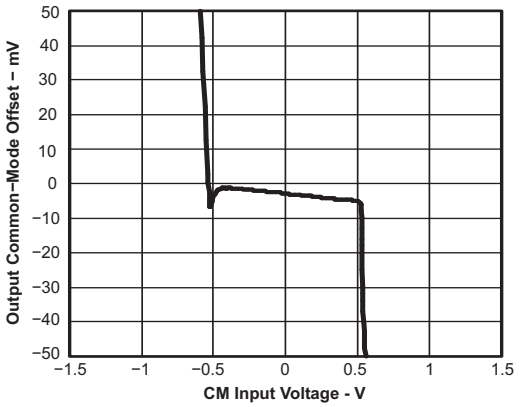

Figure 75. Output Common-Mode Offset vs CM Input Voltage

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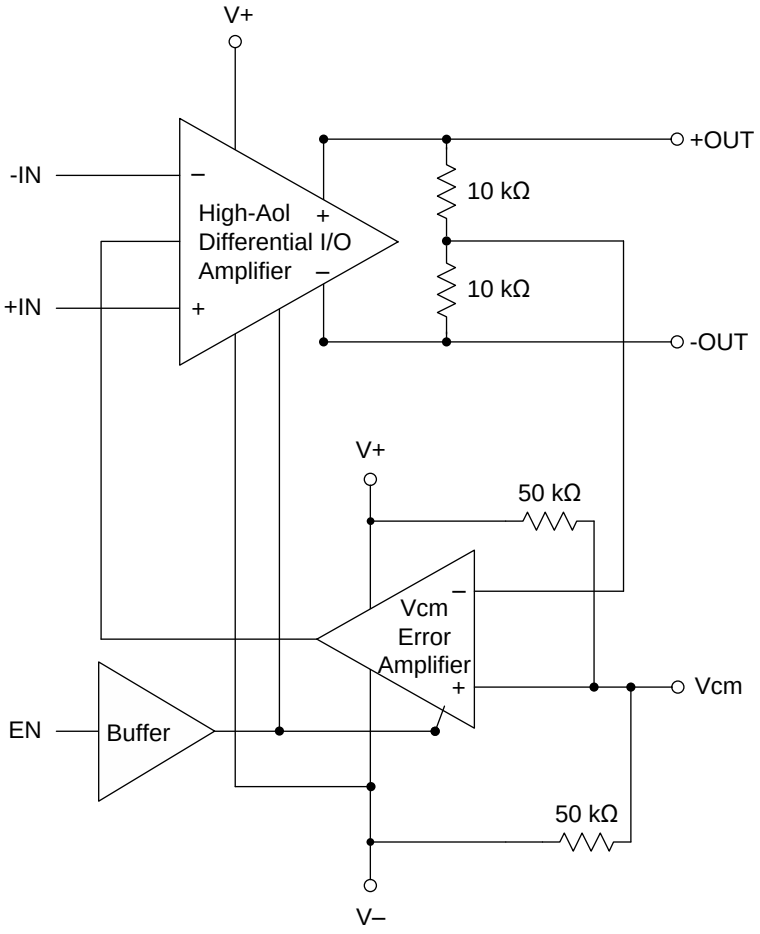
8 Detailed Description

8.1 Overview

The THS4509 is a fully differential amplifier with integrated common-mode control designed to provide low distortion amplification to wide bandwidth differential signals. The common-mode feedback circuit sets the output common-mode voltage independent of the input common mode, as well as forcing the V+ and V − outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Test Circuits

The THS4509 is tested with the following test circuits built on the evaluation module (EVM). For simplicity, power-supply decoupling is not shown—see *Layout* for recommendations. Depending on the test conditions, component values are changed per Table 3 and Table 4, or as otherwise noted. The signal generators used are AC-coupled, 50-Ω sources, and a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in *Typical Applications* with no impact on performance.

Feature Description (continued)

Table 3. Gain Component Values

GAIN	R_F	R_G	R_{IT}
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 4. Load Component Values

R_L	R_O	R_{OT}	ATTEN.
100 Ω	25 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The column *Atten* in Table 4 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 77, the signal sees slightly more loss, and these numbers are approximate.

8.3.1.1 Frequency Response

The circuit shown in Figure 76 is used to measure the frequency response of the circuit.

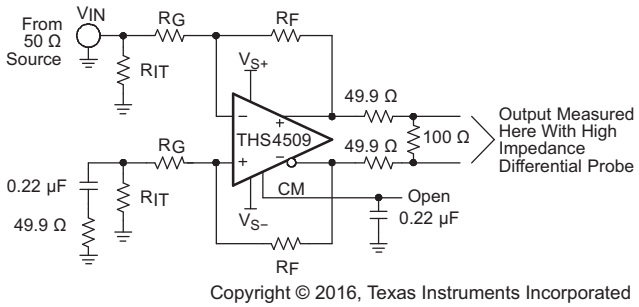

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Figure 76. Frequency Response Test Circuit

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

8.3.1.2 Distortion and 1-dB Compression

The circuit shown in Figure 77 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

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Feature Description (continued)

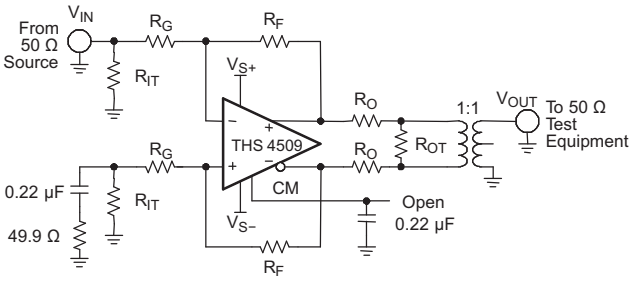

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Figure 77. Distortion Test Circuit

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination; see Table 4. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

8.3.1.3 S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, Turnon, and Turnoff Time

The circuit shown in Figure 78 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, turnon, and turnoff times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9-Ω resistor is used to calculate the impedance seen looking into the amplifier output.

Because S_{21} is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier output as a differential signal.

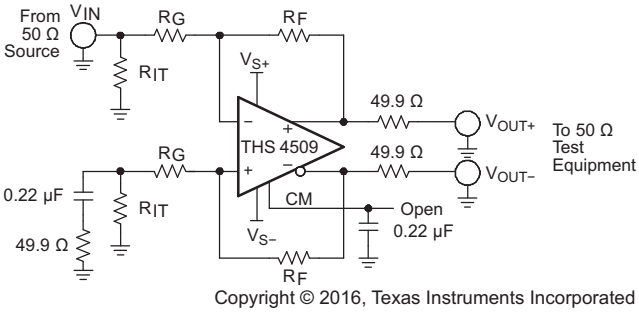

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Figure 78. S-Parameter, SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, Turnon, and Turnoff Test Circuit

Feature Description (continued)

8.3.1.4 CM Input

The circuit shown in Figure 79 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or $V_{OUT–}$ with the input injected at V_{IN}, R_{CM} = 0 Ω, and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

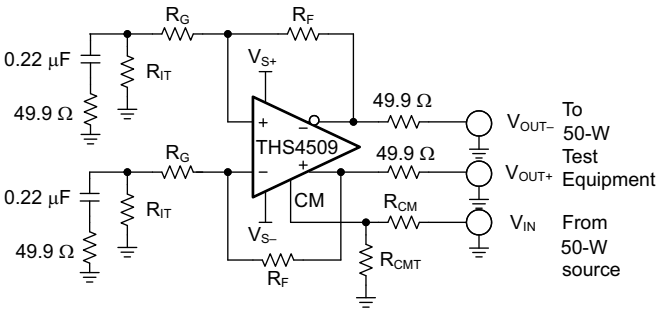

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Figure 79. CM Input Test Circuit

8.3.1.5 CMRR and PSRR

The circuit shown in Figure 80 is used to measure the CMRR and PSRR of V_{S+} and $V_{S–}$. The input is switched appropriately to match the test being performed.

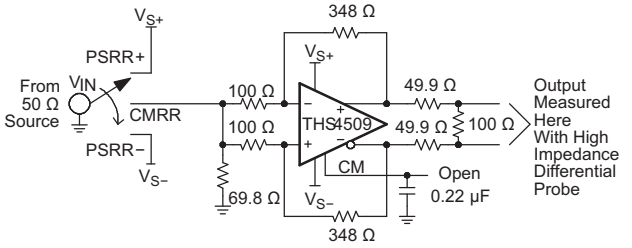

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Figure 80. CMRR and PSRR Test Circuit

8.4 Device Functional Modes

The THS4509 has one main functional mode with two variants. The amplifier functions as either a differential to differential or a single-ended to differential amplifier. In either of these modes the amplifier output operating point (common-mode voltage) is set independently by the CM pin.

The THS4509 also features a power-down state for reduced power consumption when the amplifier is not required to be operational.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THS4509 is a fully-configurable, differential operational amplifier. The closed-loop gain is set by external resistors. Many performance metrics are set by the matching of these external resistors, so 0.1% or better tolerance resistors are recommended.

The amplifier output common-mode voltage is set by the CM pin. From the CM pin to the amplifier outputs there is a fixed gain of 1 V/V so that the amplifier output voltage is identical to the voltage applied to the CM pin. This pin must be driven by a low impedance reference and must also be bypassed to ground using a 0.1-µF ceramic, low ESR resistor. The ideal common-mode voltage is equal to the voltage that is midway between the positive and negative supply voltages.

The THS4509 can be operated from either single or split power supplies with a range of 3 V to 5 V of total supply voltage. When selecting a power supply voltage, make sure to provide adequate margin for input and output voltage levels. In many cases, split supplies are the best option. It is not necessary to have power supply voltages symmetrical around ground. For example, –1 V and +4 V is a valid power supply configuration.

9.2 Typical Applications

The following circuits show application information for the THS4509. For simplicity, power-supply decoupling capacitors are not shown in these diagrams. See the *Layout* section for recommendations. For more detail on the use and operation of fully-differential op amps refer to the application report, *Fully-Differential Amplifiers* (SLOA054).

9.2.1 Differential Input to Differential Output Amplifier

The THS4509 is a fully-differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 81 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

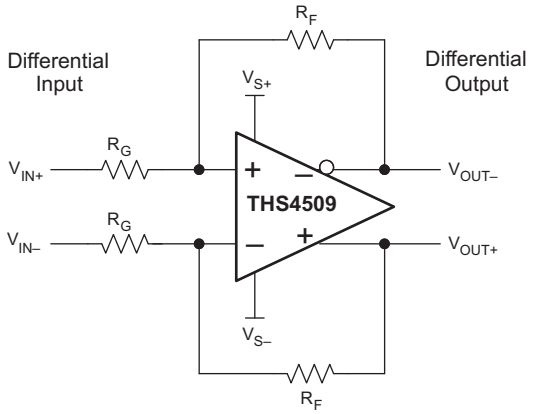

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Figure 81. Differential Input to Differential-Output Amplifier

9.2.1.1 Design Requirements

The following sections detail how to determine if your design meets these requirements.

Typical Applications (continued)

The main design requirements for the THS4509 are the input common mode, the output swing voltage. Other design requirements are signal linearity and accuracy. With flexible supply voltage ranges and externally configurable resistors the THS4509 can be configured to meet many design requirements.

Table 5 lists the design parameters of this example.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Gain	6 dB
Output swing	2 Vpp
Harmonic distortion	>75 dBc
Load resistance	100 Ω

9.2.1.2 Detailed Design Procedure

The first parameter is gain. Gain is set by external resistors as shown in Table 3. With a gain of 6 dB, the appropriate resistor values are 348 Ω for R_F and 165 Ω for R_G and 61.9 Ω for the termination resistor. These resistor values are for a 50-Ω source. The desired output swing of 2 Vpp and distortion of –75 dBc means that a supply voltage of 5 V is required. Further design details are covered in this section.

9.2.1.2.1 Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the + and – input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

9.2.1.2.2 Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typical) from the set voltage, when set within 0.5 V of midsupply, with less than 4-mV differential offset voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source. Figure 82 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where

- V_{CM} is the voltage applied to the CM pin

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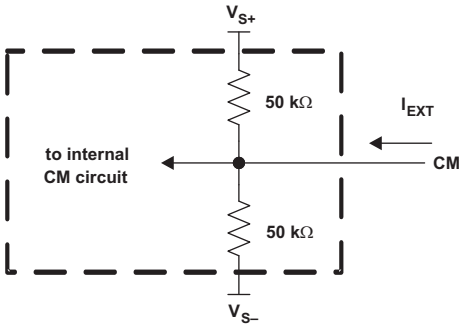

Figure 82. CM Input Circuit

9.2.1.2.3 Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4509 EVM allows split-supply operation, and the characterization data presented in this data sheet were taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 83, Figure 84, and Figure 85 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to midsupply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 83, the source is referenced to the same voltage as the CM pin (V_{CM}). V_{CM} is set by the internal circuit to midsupply. R_T along with the input impedance of the amplifier circuit provides input termination, which is also referenced to V_{CM}.

NOTE

R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value R_G+ R_S || R_T on this input. This is also true of the circuits shown in Figure 84 and Figure 85.

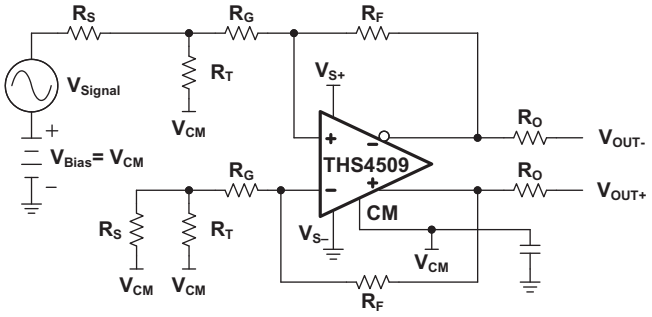

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Figure 83. THS4509 DC-Coupled Single-Supply With Input Biased to V_{CM}

In Figure 84 the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \quad (3)$$

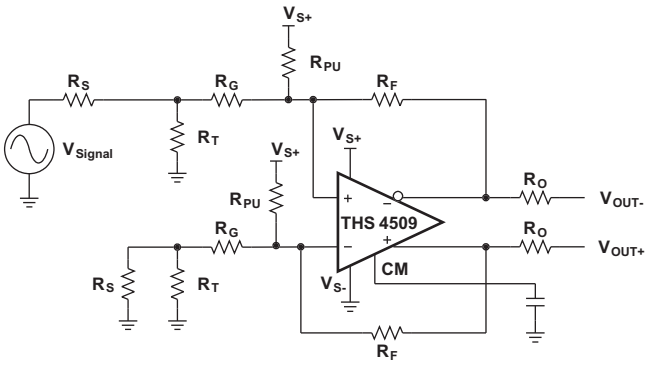

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Figure 84. THS4509 DC-Coupled Single-Supply With R_{PU} Used to Set V_{IC}

V_{IC} is the desired input common-mode voltage, V_{CM} = CM, and $R_{IN} = R_G + R_S \parallel R_T$. To set to midsupply, make the value of $R_{PU} = R_G + R_S \parallel R_T$.

Table 6 is a modification of Table 3 to add the proper values with R_{PU} assuming a 50-Ω source impedance and setting the input and output common-mode voltage to midsupply.

Table 6. R_{PU} Values for Various Gains

GAIN	R_F	R_G	R_{IT}	R_{PU}
6 dB	348 Ω	169 Ω	64.9 Ω	200 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	133 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	97.6 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	80.6 Ω

There are two drawbacks to this configuration. One is that it requires additional current from the power supply. Using the values shown for a gain of 10 dB requires 37 mA more current with 5-V supply, and 22-mA more current with 3-V supply.

The other drawback is that this configuration also increases the noise gain of the circuit. In the 10-dB gain case, noise gain increases by a factor of 1.5.

Figure 85 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to midsupply.

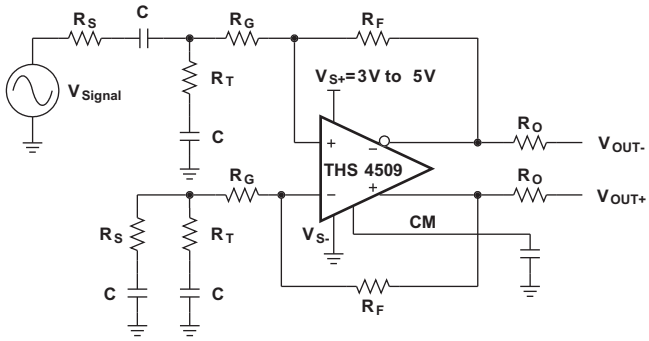

Figure 85. THS4509 AC-Coupled Single-Supply

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9.2.1.2.4 THS4509 and ADS5500 Combined Performance

The THS4509 is designed to be a high-performance drive amplifier for high-performance data converters like the ADS5500 14-bit 125-MSPS ADC. Figure 86 shows a circuit combining the two devices, and Figure 87 shows the combined SNR and SFDR performance versus frequency with –1-dBFS input signal level sampling at 125 MSPS. The THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished through the 69.8-Ω resistor and 0.22-μF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-μF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-μF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. Refer to Table 6 for component values to set proper 50-Ω termination for other common gains. A split power supply of +4 V and –1 V is used to set the input and output common-mode voltages to approximately midsupply while setting the input common-mode of the ADS5500 to the recommended +1.55 V. This configuration maintains maximum headroom on the internal transistors of the THS4509 to insure optimum performance.

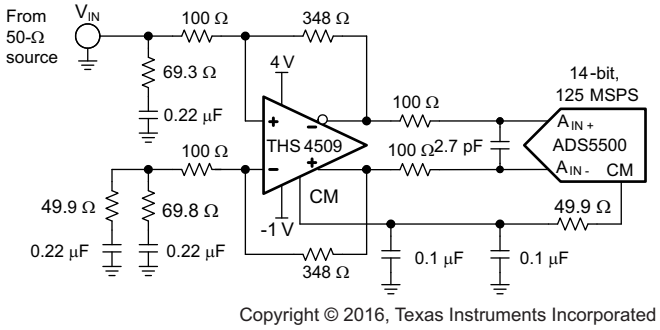

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Figure 86. THS4509 and ADS5500 Circuit

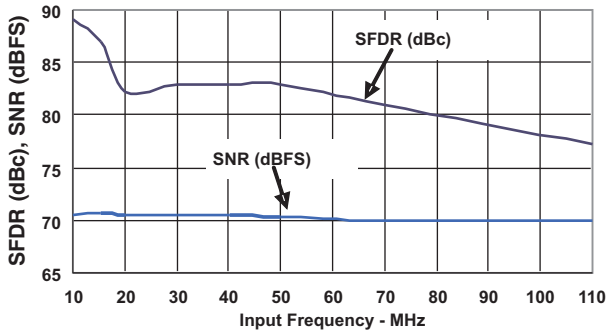

Figure 87. THS4509 and ADS5500 SFDR and SNR Performance vs Frequency

Figure 88 shows the two-tone FFT of the THS4509 and ADS5500 circuit with 65-MHz and 70-MHz input frequencies. The SFDR is 90 dBc.

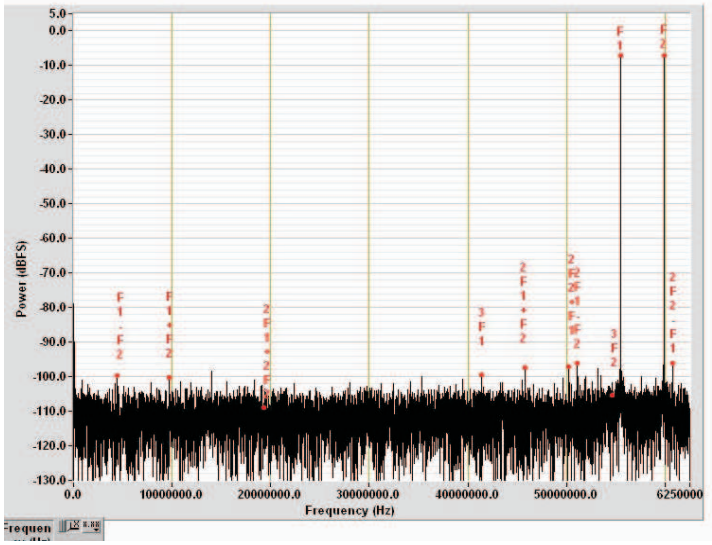

Figure 88. THS4509 and ADS5500 2-Tone FFT With 65-MHz and 70-MHz Inputs

9.2.1.2.5 THS4509 and ADS5424 Combined Performance

Figure 89 shows the THS4509 driving the ADS5424 ADC, and Figure 90 shows the combined SNR and SFDR performance versus frequency with –1-dBFS input signal level and sampling at 80 MSPS.

As before, the THS4509 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4509 and ADS5500 circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz (–3 dB).

Because the ADS5424 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power-supply input with V_{S+} = 5 V and $V_{S–}$ = 0 V (ground).

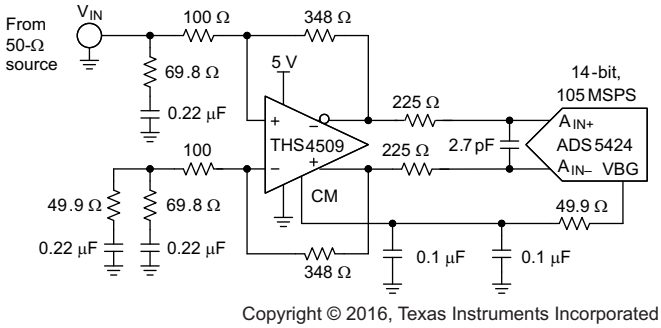

Figure 89. THS4509 and ADS5424 Circuit

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9.2.1.3 Application Curve

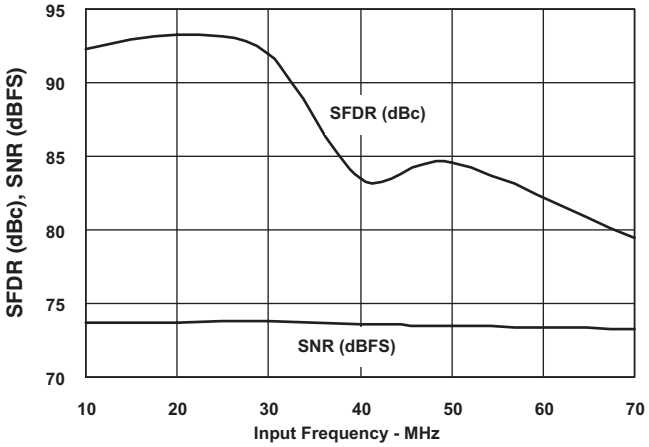

Figure 90. THS4509 and ADS5424 SFDR and SNR Performance vs Frequency

9.2.2 Single-Ended Input to Differential Output Amplifier

The THS4509 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 91 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

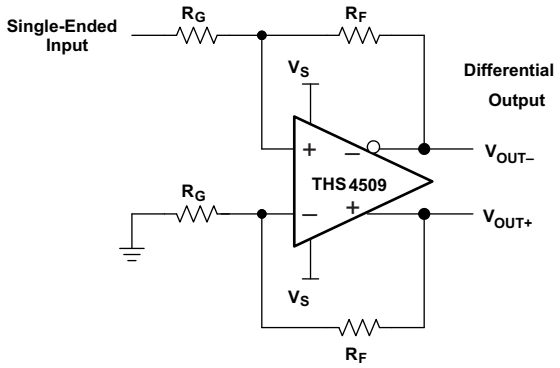

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Figure 91. Single-Ended Input to Differential Output Amplifier

10 Power Supply Recommendations

The THS4509 can accommodate supply voltages from 3 V to 5 V, either single supply or split supply. Unless the application calls for AC coupling and a very small signal the 5-V supply option must be chosen. In many cases, split supplies are necessary because it is important to have the output common-mode voltage set very close to the midsupply voltage. For example, when driving an ADC with an input common-mode voltage of 1 V the ideal power supply voltage would be +3.5 V and –1.5 V.

Power supply decoupling capacitors must be placed within 2 mm of the amplifier power supply pins. These capacitors must be very low ESR and must have a self resonant frequency above 200 mHz.

11 Layout

11.1 Layout Guidelines

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible.

11.1.1 General Guidelines

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct; avoid vias.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-μF and two 0.1-μF power-supply decoupling capacitors must be placed as near to the power-supply pins as possible.
6. Two 0.1-μF capacitors must be placed between the CM input pins and ground. This configuration limits noise coupled into the pins. One each must be placed to ground near pin 4 and pin 9.
7. TI recommends splitting the ground panel on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection must be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This configuration must be applied to the input gain resistors if termination is not used.
9. The THS4509 recommended PCB footprint is shown in Figure 92.

11.1.2 PowerPAD PCB Layout Considerations

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach:

1. Prepare the PCB with a top side etch pattern as shown in Figure 92. There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. The holes must be 13 mils (0.013 in, 0.33 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC PowerPAD package should make the connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This process results in a part that is properly installed.

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Layout Guidelines (continued)

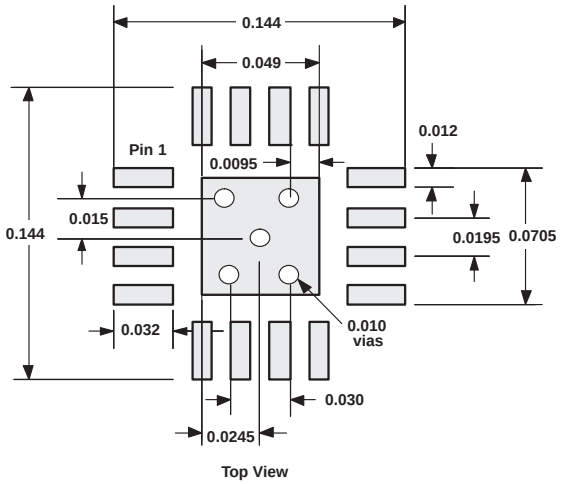

Figure 92. PowerPAD PCB Etch and Via Pattern

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer must never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages must be used to choose the proper package.

11.2 Layout Example

Figure 93 is the THS4509 EVAL1 EVM schematic; layers 1 through 4 of the PCB are shown Figure 94.

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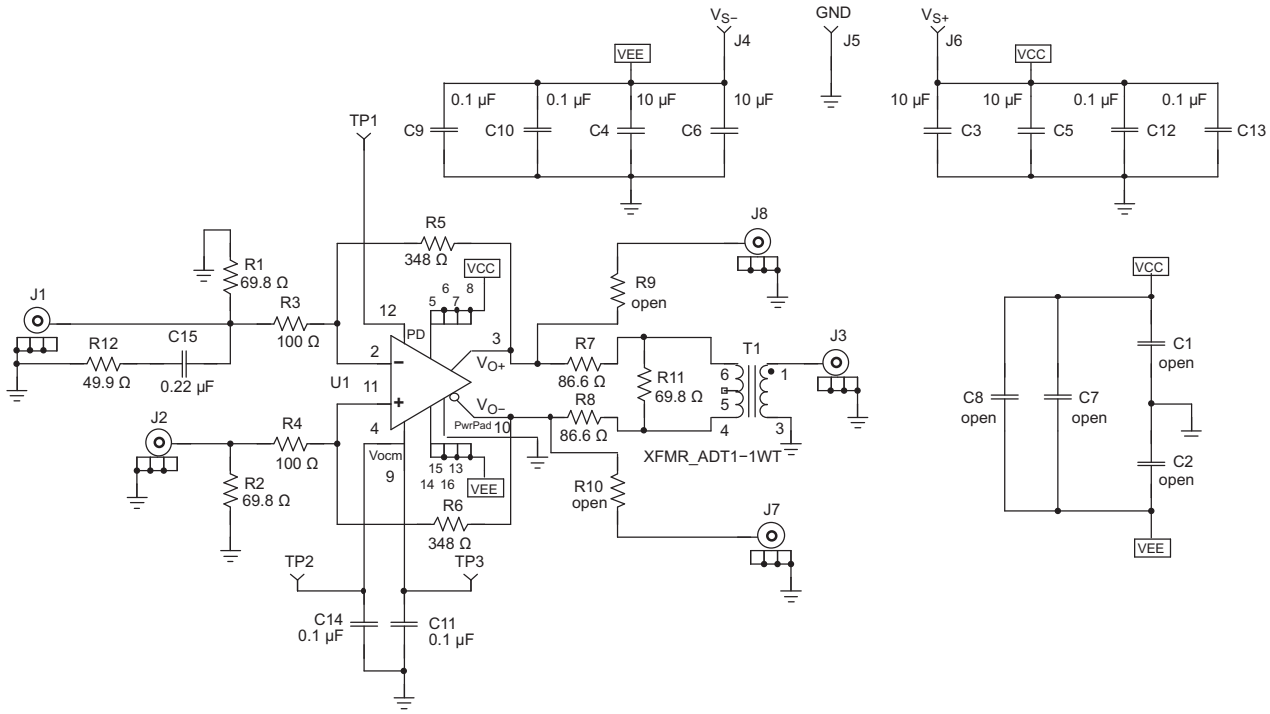

Figure 93. THS4509 EVAL1 EVM Schematic

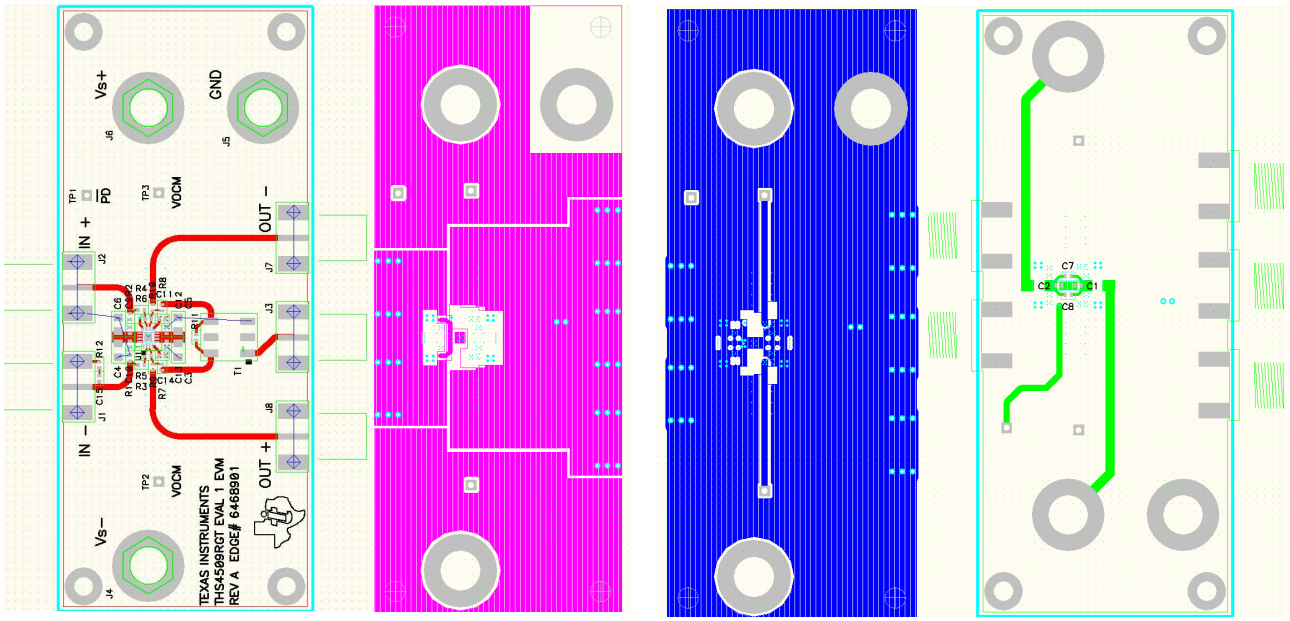

Figure 94. THS4509 EVAL1 EVM Layer 1 Through Layer 4

11.3 PowerPAD™ Design Considerations

The THS4509 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted (see Figure 95a and Figure 95b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 95c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

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PowerPAD™ Design Considerations (continued)

NOTE

The THS4509 has no electrical connection between the PowerPAD and circuitry on the die. Connecting the PowerPAD to any potential voltage between V_{S+} and $V_{S–}$ is acceptable. It is most important that it be connected for maximum heat dissipation.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface-mount with the previously awkward mechanical methods of heatsinking.

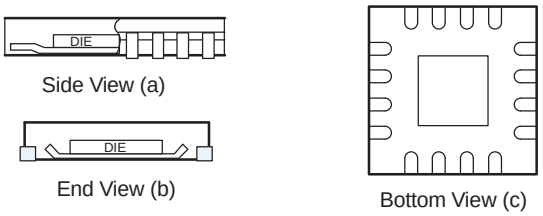

Figure 95. Views of Thermally-Enhanced Package

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

THS4509デバイスのサポートについては、以下を参照してください。

- ADS5500
- ADS5424
- THS4509EVM 評価モジュール

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

『完全差動アンプ』(SLOA054)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 静電気放電に関する注意事項

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4509RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4509
THS4509RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4509
THS4509RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4509
THS4509RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4509
THS4509RGTTG4	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4509

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4509 :

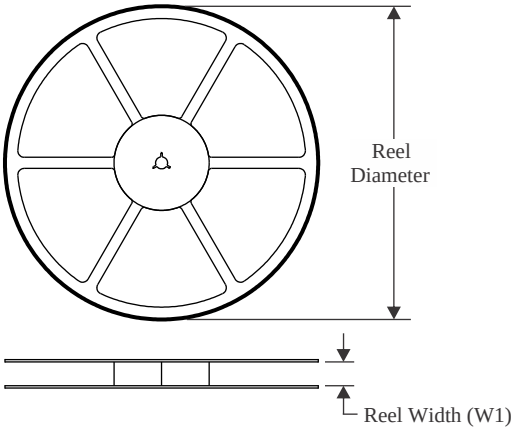
- Automotive : THS4509-Q1

NOTE: Qualified Version Definitions:

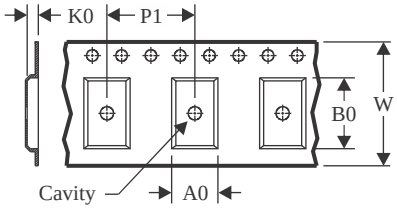
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

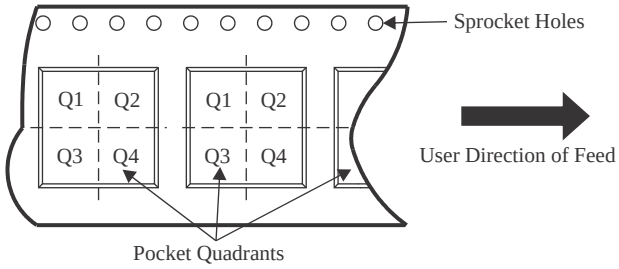


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

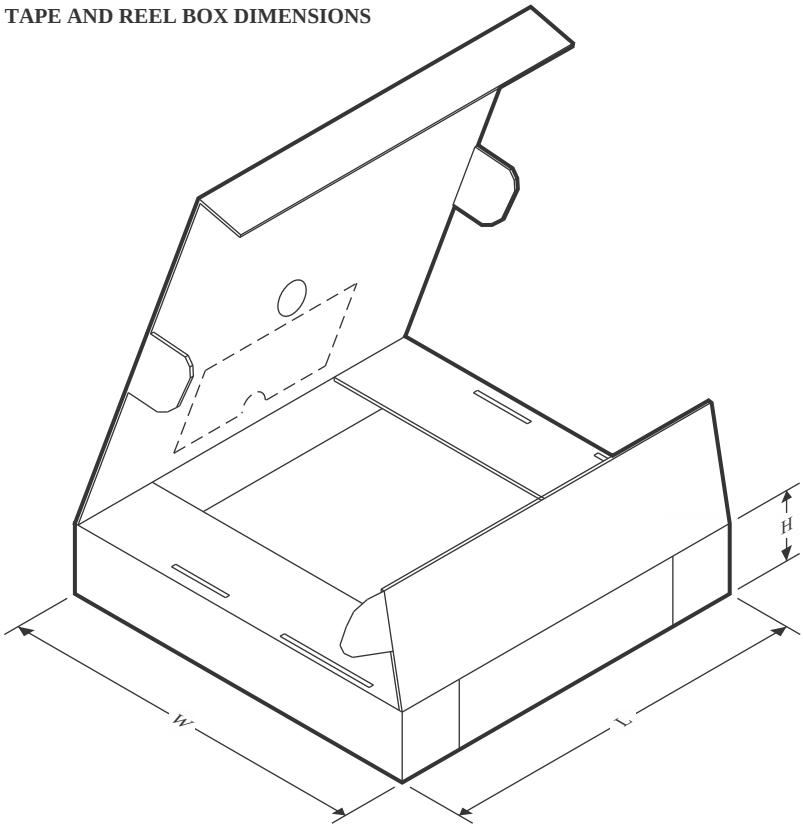
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4509RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4509RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

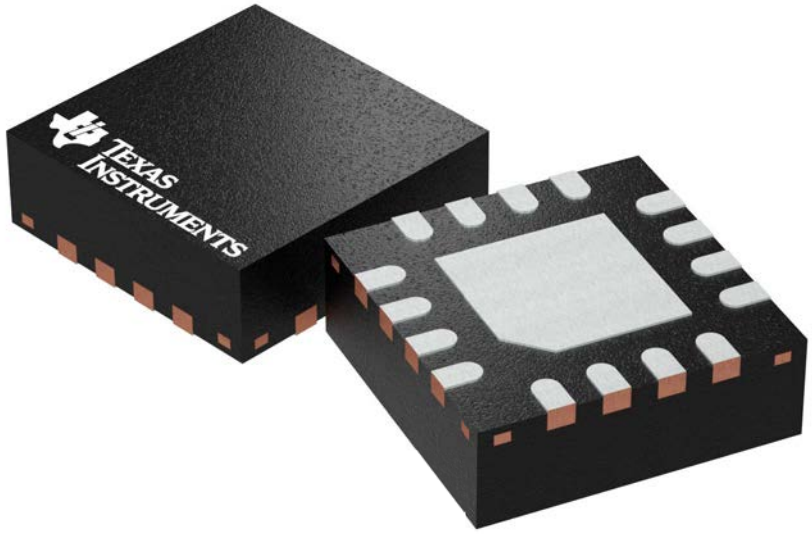
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4509RGTR	VQFN	RGT	16	3000	356.0	356.0	35.0
THS4509RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

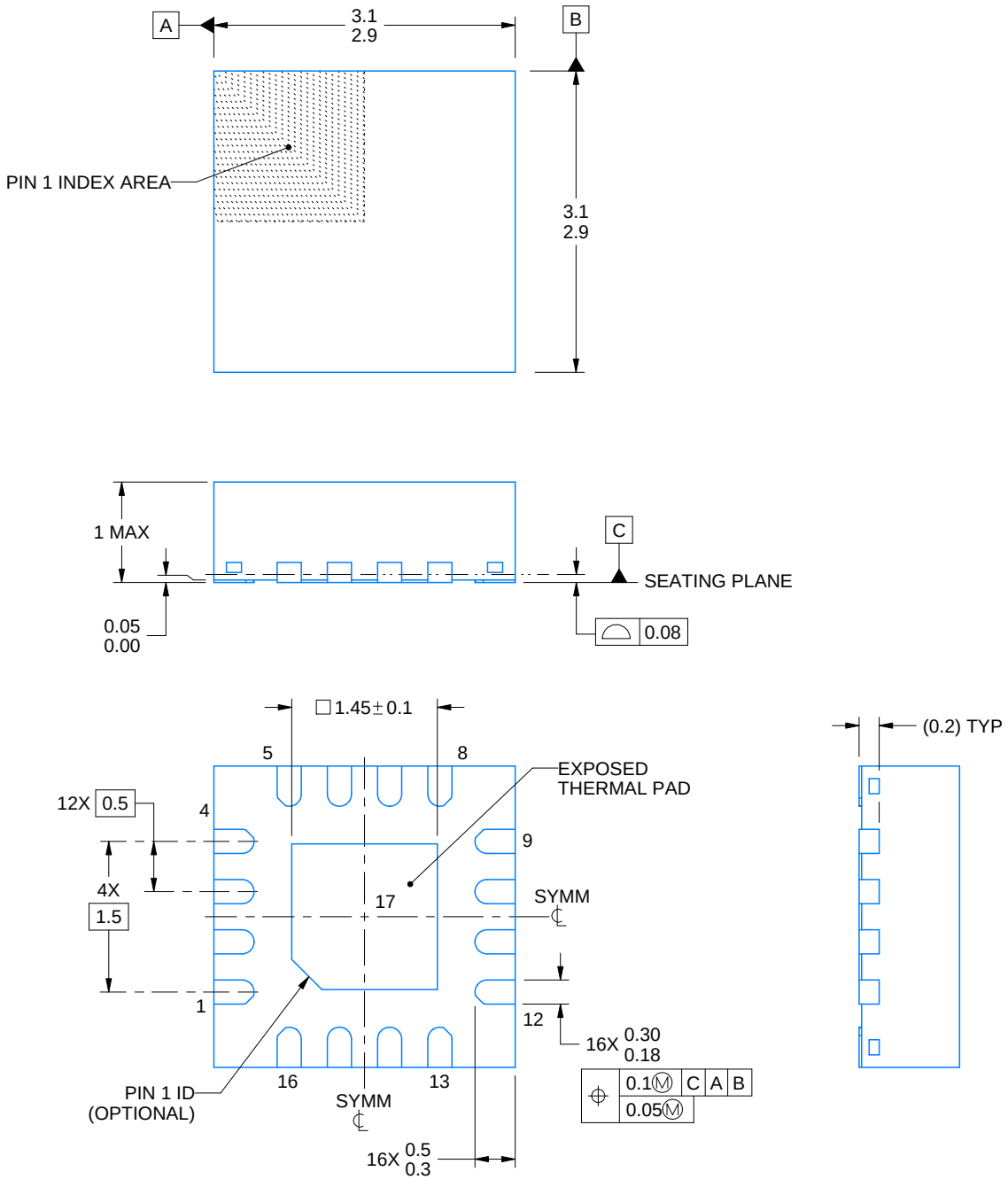
4203495/I

RGT0016A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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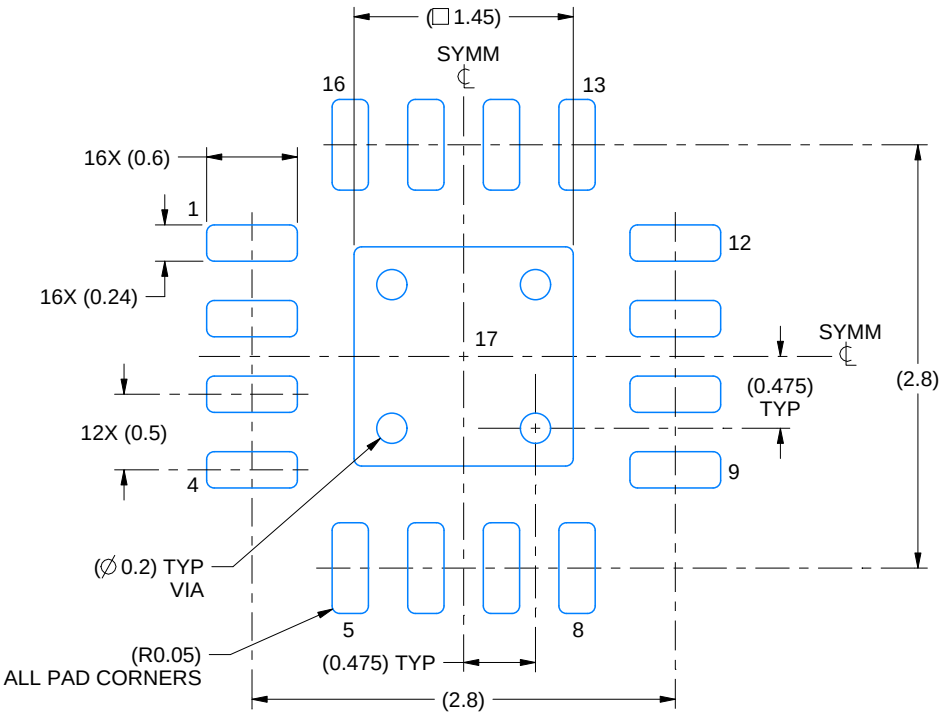
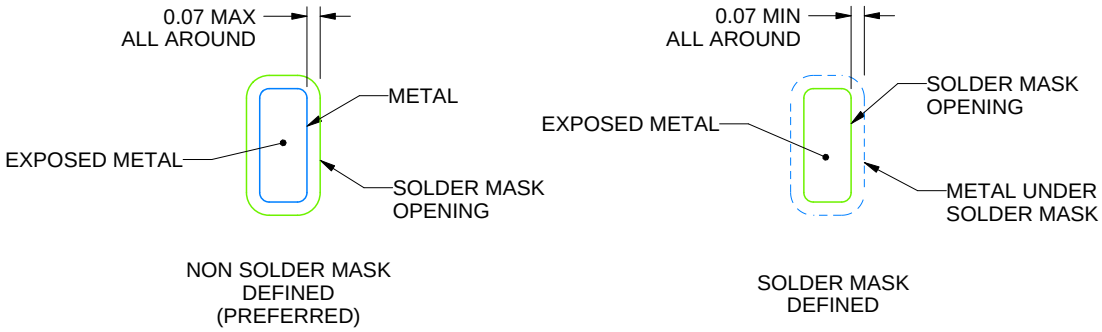
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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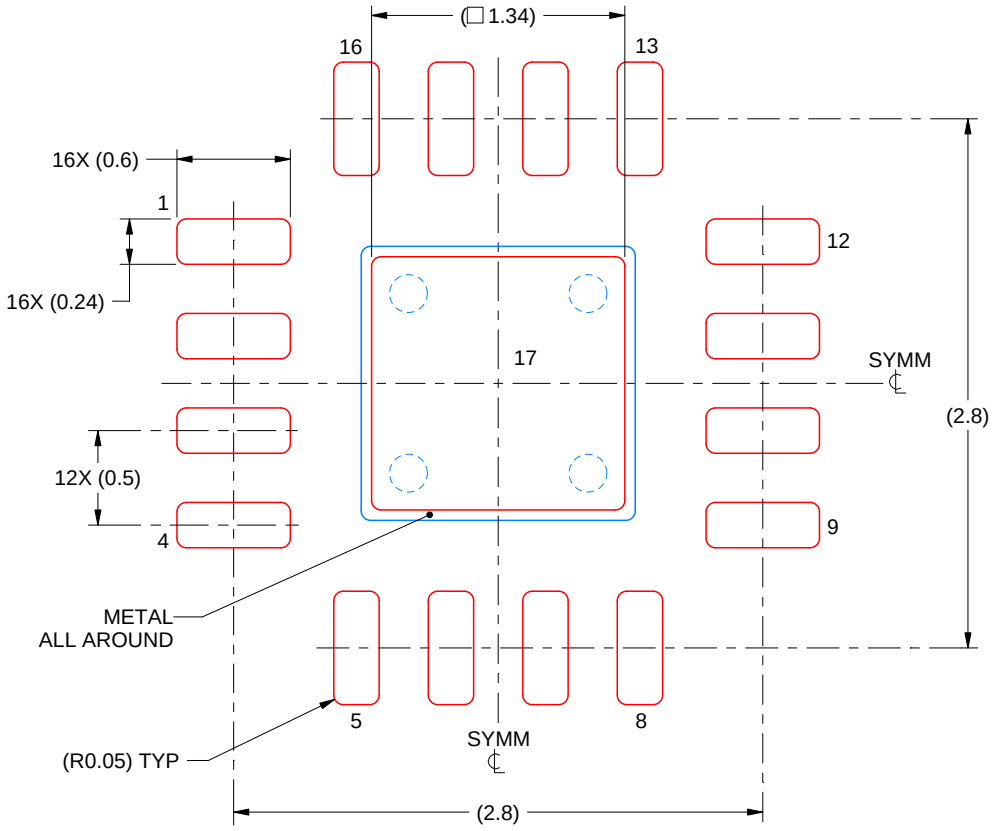
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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