参考資料

デザイン・ガイド: TIDA-050026-23882
マルチポート・アプリケーション向けの 24 ポート (2 ペア) 電源装置のリファレンス・デザイン

概要

このリファレンス・デザインは、24 ポート (2 ペア) PSE システムの評価モジュールで、ハードウェア・キット、システム・ファームウェアのイメージ、およびシステム・ファームウェアの GUI が含まれています。ハードウェア・キットは、マザーボード (PSEMTHR24EVM-081)、MSP430 ドーター・カード (PSEMCUDAUEVM-082)、および PSE ドーター・カード (TPS23882EVM-084) で構成されます。システム (ハードウェアとソフトウェアの両方) を評価するには、USB2ANY および MSP-FET アダプタも必要です。

PSEMCUDAUEVM-082 上の MSP430F5234 は、EVM テスト目的用の量産前ファームウェアでプログラムされています。評価前に、このユーザー・ガイドの指示に従い、TI.com からの最新版のファームウェアをフラッシュしてください。

リソース

TIDA-050026-23882	デザイン・フォルダ
TPS23882EVM-084	ツール・フォルダ
PSEMTHR24EVM-081	ツール・フォルダ
PSEMCUDAUEVM-082	ツール・フォルダ
TPS23882	プロダクト・フォルダ
MSP430F5234	プロダクト・フォルダ
CSD19538Q3A	プロダクト・フォルダ

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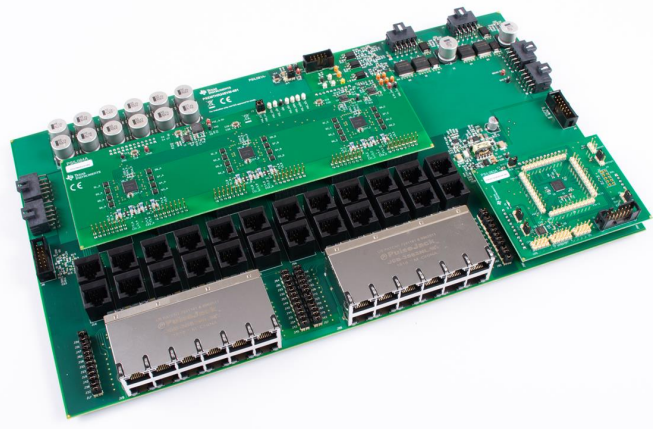
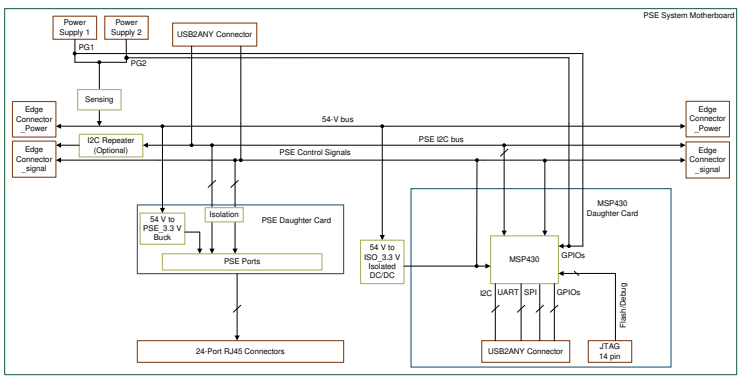
特長

- オンボードの電源監視
- 24 (2 ペア) ポートのシステムで、48 ポートに拡張可能
- GUI を構成可能で、ホスト・インターフェイス (I^2C または UART) を選択可能な、柔軟性の高いシステム
- マルチポートの電力管理
- 複数の電源
- レガシー電源を使用するデバイス (PD) をサポート

アプリケーション

- キャンパス / 分岐スイッチ
- ビデオ・レコーダ
- エッジ・ルータ





1 System Description

This reference design provides a competitive and alternative solution.

In a multiport PSE system, the system-level software is the biggest challenge. The software handles complicated situations and addresses the following challenges:

- The power supply is usually not able to support all ports with a full load due to size and cost constraints. The system software manages the port power with priority to keep the total power consumption below the power budget.
- There are multiple power supplies in the system. These power supplies could be in sharing mode or backup mode. The system software shuts down low-priority ports fast enough to keep the total power consumption below the remaining power budget.
- There are some legacy PD devices that do not present the standard PoE PD signature. The system software finds a way to supply power to these devices.
- System software limits the port power based on the PD class levels or host configuration.
- When there are load-step changes on multiple ports, the system software acts quickly enough to keep the power consumption below the power budget.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	44 V–57 V	
Port power limit	2 W–60 W	> 30 W is considered as nonstandard power
Compliance	IEEE 802.3bt Type 3	
PD class level supported	Class 0 to class 4	
Number of power supply supported	1–2	In sharing mode and redundant mode
Max port number supported	48	Referred to RJ45 ports

1.2 Description

This reference design features the TPS23882 daughtercard, the octal channel, the TPS23882 device, and the IEEE802.3bt ready PoE PSE controller. When paired with the PSE motherboard PSEMTHR24-081 (sold separately) and MCU daughtercard PSEMCUDAUEVM-082 (sold separately), users can evaluate the TPS23882 device and PSE system firmware solution.

The full PoE evaluation ecosystem includes the following:

- PSEMTHR24EVM-081: motherboard for 24-port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24-port PoE PSE applications (sold separately)
- TPS23882EVM-084: TPS23882 daughtercard for 24 port Type 3 (2 pair) PSE PoE PSE applications (sold separately)
- USB2ANY interface adapter: used with PSE system firmware GUI for I^2C/UART interaction with the PSEMCUDAU-082 daughtercard (sold separately)

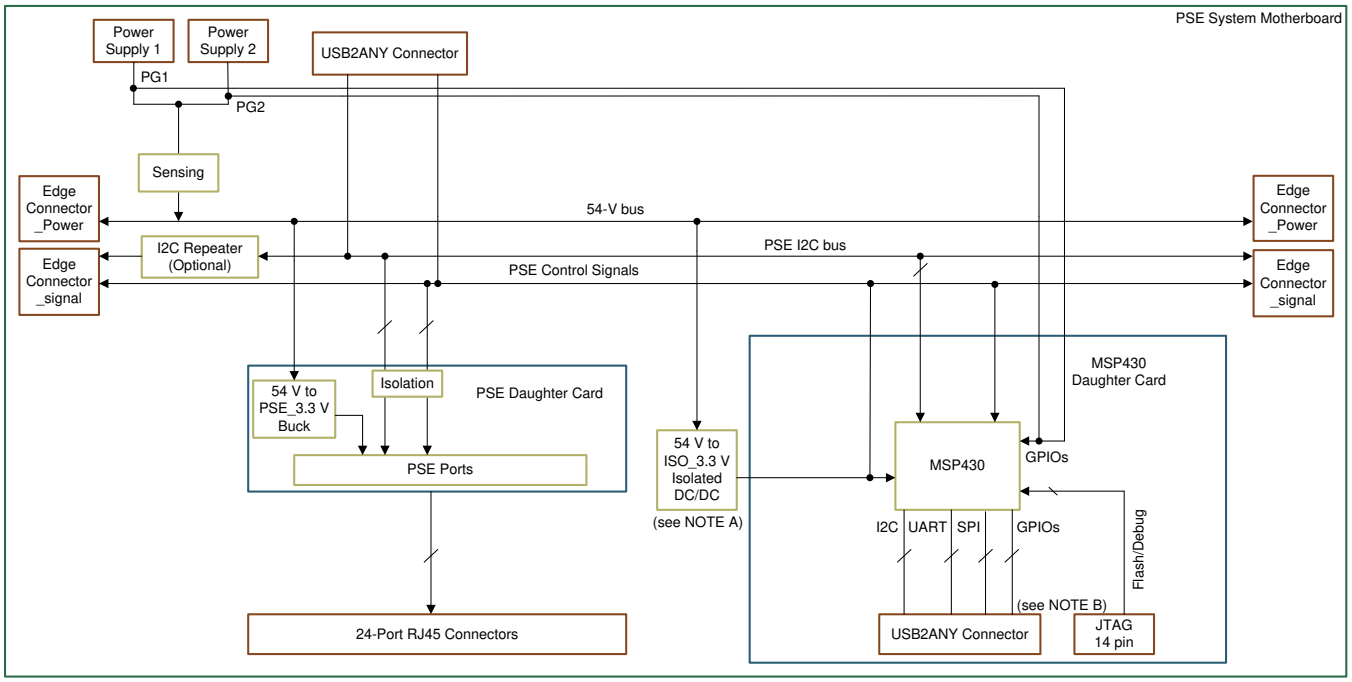
- MSP-FET programmer: used with Uniflash GUI for programming the MSP430 device
- PSE system firmware code image (request access to the code image through TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder)
- PSE system firmware GUI (request access to the code image through TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder)

注: The MSP430F5234 on PSEMCUDAUEVM-082 has been programmed with pre-production firmware for EVM testing purposes. Please follow the instructions in this user's guide to flash the latest firmware from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder before evaluation.

2 System Overview

2.1 Block Diagram

図 1. TIDA-050026-23882 Block Diagram



A The 54-V to 3.3-V isolated DC/DC is for demonstration purposes only. It is not needed in a real system.

B Only connect a USB2ANY connector or JTAG to avoid GND loops.

2.2 Design Considerations

2.2.1 Input Power

2.2.1.1 Vpwr

DC input voltage is provided through J1 and J3. This board supports a dual power source in sharing mode and redundant mode. If the power supplies are in redundant mode, make sure the main power supply is connected to J1 and a backup power supply is connected to the J3 connector.

The minimum PSE port voltage is 44 VDC for Type 1, 50 V for Type 2 and Type 3, and 52 V for Type 4. The maximum DC voltage at VPWR is 57 V for all types. During evaluation, choose the appropriate DC power supply for the different type environment.

2.2.1.2 3.3 V

A local 3.3 V for local devices (labeled as 3.3 V) is provided by the onboard LM5017 buck converter. The LM5017 device provides a basic power-on sequence and provides a well-controlled and consistent startup to prevent erratic operation. In addition to 44 V to 57 V, the TPS238x requires 3.3 V for the digital circuitry and each TPS2388x device consumes 6-mA typical and 12-mA maximum.

2.2.1.3 3.3 V_ISO

The reference design kit provides galvanic isolation between PoE power side and host side using digital isolators. The host side power is provided by 3.3 V_ISO.

2.2.2 Communication Interface

2.2.2.1 PSE I²C Communication

The board provides two I²C interfaces communicating to PSE:

1. J10 on the motherboard (PSEMTHR24EVM-081) provides I²C access to all PSE devices directly. The TPS2388x GUI can communicate to PSE devices with the USB2ANY interface adapter.
2. J11 and J12 on the motherboard (PSEMTHR24EVM-081) provides I²C access and system control signal to the MSP430 daughtercard.

2.2.2.2 MCU - Host Communication

The MSP430 daughtercard provides I²C/UART communication port to host through J12 to J14 on MSP430 daughtercard (PSEMCUDAUEVM-082). The PSE system GUI provides host configurations to the PSE system.

Host interface user's guide can be accessed from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder.

2.2.3 MSP430F523x Hardware Design

表 2. MSP430 GPIO Pin Assignment

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
COMMUNICATION			
22	P3.0	I²C SDA USCI_B0	I²C to PSEs
23	P3.1	I²C SCL USCI_B0	I²C to PSEs
30	P4.1	I²C SDA USCI_B1	I²C to host
31	P4.2	I²C SCL USCI_B1	I²C to host
33	P4.4	UART TX USCI_A1	UART to host (debug only)
34	P4.5	UART RX USCI_A1	UART to host (debug only)
21	P2.7	SPI CLK USCI_A0	SPI to host (reserved)
24	P3.2	SPI slave TX enable, USCI_A0	SPI to host (reserved)
25	P3.3	UART TX,USCI_A0 or SPI slave in, master out	UART to host TX or SPI to host (reserved)

表 2. MSP430 GPIO Pin Assignment (continued)

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
26	P3.4	UART RX, USCI_A0 or SPI slave out, master in	UART to host RX or SPI to host (reserved)
HARDWARE INTERRUPT			
13	P1.0	PSE INT	Connect to PSE INT pin
16	P1.3	OC Alert	Connect to external current sensing circuit if not used, connect to 3.3 V
18	P1.5	Power supply 1	Connect to power supply 1 power good signal. In RPS mode, P1.5 must be connected to main power supply. **If there's only one power supply, the power good signal must be connected to P1.5.**
19	P1.6	Power supply 2	Connect to power supply 2 power good signal, if not used, connect to GND. In RPS mode, P1.6 must be connected to backup power supply
20	P1.7	Disable all ports	This is for hardware disable ports(Reserved)
GENERAL I/O			
4	P5.0	RESET	PSE RESET Connect to PSE RESET pin
17	P1.4	OSS	PSE OSS Connect to PSE OSS pin
46	P6.0	Interrupt pin to host	
35	P4.6	BSL mode indication to host	MCU configures as output. If MCU is in BSL mode, output high. If in normal operation mode, output low.
48	P6.2	Guard-band indication	Need an external LED
47	P6.1	Selection between I^2C and SPI/UART	(Need to pullup or pulldown)
PROGRAM DOWNLOAD AND DEBUG			
44	PJ.3	TCK	JTAG clock input
43	PJ.2	TMS	JTAG state control
42	PJ.1	TDI/TCLK	JTAG data input, TCLK input
41	PJ.0	TDO	JTAG data output
40		TEST/SBWTCK	Enable JTAG pins
45		RSTDVCC/SBWTDIO	External reset
EXTERNAL CRYSTAL			
7	P5.4	XTIN	External low frequency clock (use if needed)
8	P5.5	XTOUT	External low frequency clock (use if needed)

Pre-configure the host interface protocol through hardware as 表 3 shows.

表 3. Host Interface Protocol

	P6.1	CS(P3.2)
I^2C	high	Don't care
UART	low	low
SPI (Reserved)	low	high

2.3 Highlighted Products

2.3.1 TPS23882

The TPS2388x device is the main IC to handle PoE functions to deliver power to PDs through Ethernet cable.

The TPS23882 is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt standard. The PSE controller can detect powered devices (PDs) that have a valid signature, determine the power requirements of the devices according to their classification, and apply power. The TPS23882 improves on the TPS2388 with reduced current sense resistors, selectable Autonomous operation, SRAM programmability, programmable power limiting, capacitance measurement, and compatibility with TI's FirmPSE system firmware (see Device Comparison Table). Dedicated per port ADCs provide continuous port current monitoring and the ability to perform parallel classification measurements for faster port turn on times. A 1.25A port current limit and adjustable power limiting allows for the support of non-standard applications above 60W sourced. The 200 mΩ current sense resistor and external FET architecture allow designs to balance size, efficiency, thermal, and solution cost requirements. Port remapping and pin-to-pin compatibility with the TPS2388/80/81 devices eases migration from previous generation PSE designs and enables interchangeable 2-layer PCB designs to accommodate different system PoE power configurations.

2.3.2 MSP430F523x

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from lowpower modes to active mode in 3.5 µs (typical). The MSP430F524x series are microcontroller configurations with four 16-bit timers, a high-performance 10-bit ADC, two USCIs, a hardware multiplier, DMA, a comparator, and an RTC module with alarm capabilities. The MSP430F523x series microcontrollers include all of the peripherals of the MSP430F524x series except for the ADC.

MSP430F523x is the main controller to control PSE devices(TPS2388x) through the I^2C bus and also communicates to host CPU through I^2C or UART to receive configurations and report system status.

2.3.3 ISO7741

The ISO7741 isolator is used to isolate I^2C signals between PSE devices and the MCU.

The ISO774x devices are high-performance, quadchannel digital isolators with 5000 VRMS (DW package) and 3000 VRMS (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward and one reverse-direction channels, and the ISO7742 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is high for devices without suffix F and low for devices with suffix F.

2.3.4 ISO7731

The ISO7731 digital isolator is used to isolate control signals (OSS, RESET, INT) between MSP430 and PSE devices.

The ISO773x devices are high-performance, triple channel digital isolators with 5000 VRMS (DW package) and 3000 VRMS (DBQ package) isolation ratings per UL 1577.

This family of devices has reinforced insulation ratings according to VDE, CSA, TUV, and CQC.

The ISO773x family of devices provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7730 device has all three channels in the same direction and the ISO7731 device has two forward and one reverse-direction channel. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F. See the device *Functional Modes* section for further details.

Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO773x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

2.3.5 CSD19538

This 100-V, 49-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize conduction losses and reduce the board footprint in PoE applications.

2.3.6 LM5017

The LM5017 device is used to generate 3.3 V to supply PSE devices.

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 device requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers. A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

2.3.7 LM5020

The LM5020 device is used to generate isolated LM5020 to supply MSP430 and isolators.

The LM5020 high-voltage pulse-width modulation (PWM) controller contains all of the features needed to implement single-ended primary power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent line feed-forward. The LM5020 device includes a high-voltage start-up regulator that operates over a wide-input range up to 100 V. The PWM controller is designed for high-speed capability including an oscillator frequency range to 1 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, line undervoltage lockout, cycle-by-cycle current limit, slope compensation, softstart, oscillator synchronization capability and thermal shutdown.

2.3.8 LM5050

The LM5050 device is used to support 2 power supplies in the system to work in backup mode.

The LM5050-1 and LM5050-1-Q1 high-side ORing FET controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5050-1 and LM5050-1-Q1 controllers provide charge pump MOSFET gate drive for an external N-channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1 and LM5050-1-Q1 can connect power supplies ranging from 5 V to 75 V and can withstand transients up to 100 V.

2.3.9 INA240

The INA240 amplifier is used to measure the total current from the input to support fast shutdown in an event of load step change.

The INA240 device is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating the flyback period of typical solenoid applications. Enhanced PWM rejection provides high levels of suppression for large common-mode transients ($\Delta V/\Delta t$) in systems that use PWM signals (such as motor drives and solenoid control systems). This feature allows for accurate

current measurements without large transients and associated recovery ripple on the output voltage. This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

2.3.10 REF3425

The REF3425 device is used to provide a threshold to output the INA240 and generate a signal to MCU for overcurrent alert.

The REF34xx device is a low temperature drift (6 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 95 μA. This device also offers very low output noise of 3.8 μVp-p /V, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems. With a small SOT-23 package, the REF34xx offers enhanced specifications and pin-to-pin replacement for MAX607x and ADR34xx. The REF34xx family is compatible to most of the ADC and DAC such as the ADS1287, ADUCM360, and ADS1112 devices. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (95 μA) can benefit portable and battery-powered applications.

2.3.11 TPS3890

The TPS3890 device is used to monitor the existence of the power supply and generate power good signal to MCU. The MCU can adjust the total power budget of the system.

The TPS3890 device is a precision voltage supervisor with low-quiescent current that monitors system voltages as low as 1.15 V, asserting an open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (MR) return above the respective thresholds. The TPS3890 family uses a precision reference to achieve 1% threshold accuracy. The reset delay time can be user-adjusted between 40 μs and 30 s by connecting the CT pin to an external capacitor. The TPS3890 device has a very low quiescent current of 2.1 μA and is available in a small 1.5-mm × 1.5-mm package, making the device well-suited for battery-powered and space-constrained applications.

3 Hardware, Software, Testing Requirement and Test Result

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware is required to get started with the reference design:

- PSEMTHR24EVM-081: motherboard for 24 port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24 Port PoE PSE applications (sold separately)
- TPS23882EVM-084: TPS23882 daughtercard for 24-port Type 3 (2 pair) PoE PSE applications (sold separately)
- USB2ANY interface adapater: used with PSE system firmware GUI for I^2C/UART interaction with PSEMCUDAU-082 daughtercard (sold separately)
- MSP-FET programmer: used with the Uniflash GUI for programming the MSP430 device

3.1.2 Software

- FirmPSE code image (request access to the code image through the TIDA-050026-23882 folder or the PSEMCUDAUEVM-082 tool folder)
- FirmPSE GUI (request access to the GUI through the TIDA-050026-23882 folder or the

PSEMCUDAUEVM-082 tool folder)

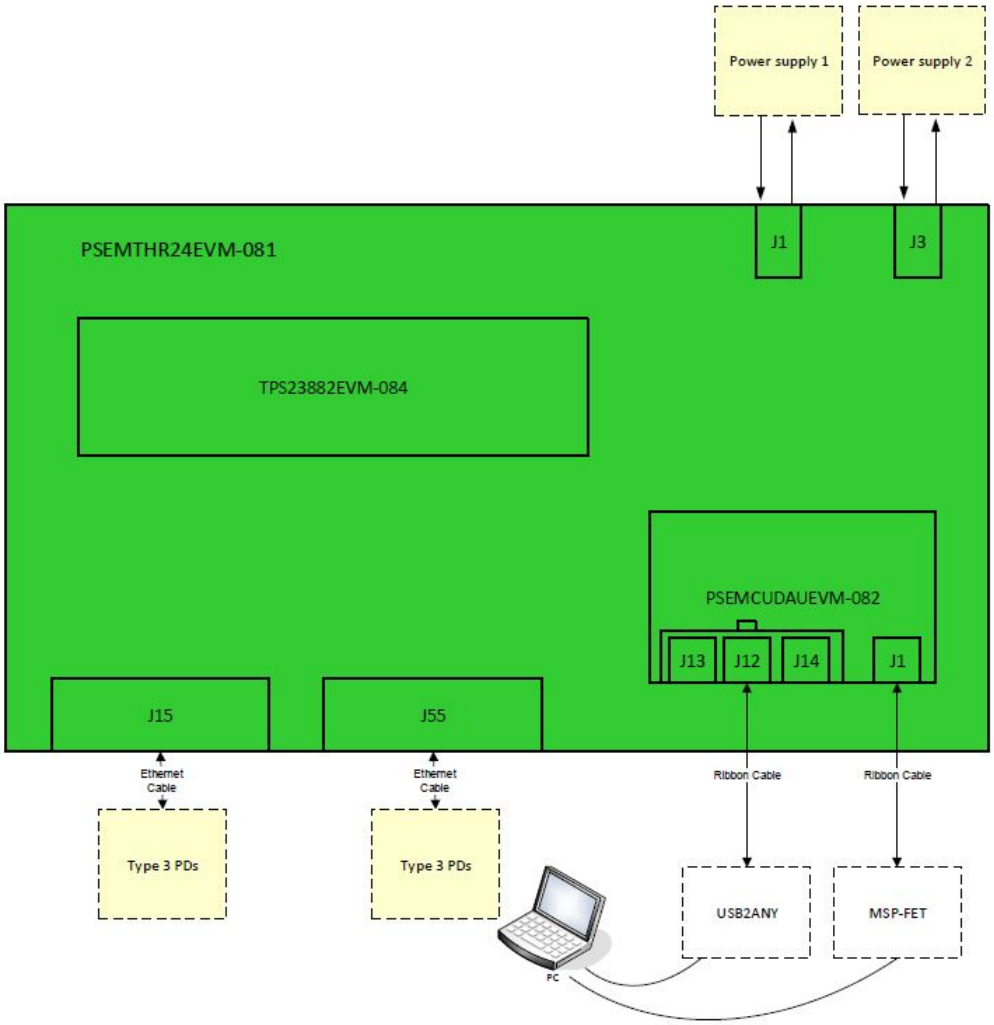
3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Hardware Setup

図 2 shows the hardware test setup of the ecosystem.

図 2. Ecosystem Setup



注: A 30-pin ribbon cable is required to enable the full features of PSE system firmware GUI.

3.2.1.2 LED, Test Point, Jumper and Connector Settings

3.2.1.2.1 EVM LEDs

表 4 lists the EVM LEDs and their descriptions.

表 4. EVM LEDs

LED	COLOR	DESCRIPTION
PSEMTHR24EVM-081		
J15, J55	Green, Yellow	There is one green and yellow LED on each RJ45 port
PSEMCUDAUEVM-082		
D1	Green	The total power consumption is within the pre-configured guardband

3.2.1.2.2 EVM Test Points

表 5 lists the EVM test points.

表 5. EVM Test Points

TP	LABEL	DESCRIPTION
PSEMTHR24EVM-081		
TP1	55VDC	VPWR
TP2	GND	VPWR ground
TP3	OC-ALERT	System over current alert signal
TP4	SDA	I^2C data
TP5	SCL	I^2C clock
TP6	PG1	Power good signal for power supply #1
TP7	PG2	Power good signal for power supply #2
TP8	PSE_3.3V	3.3 V for PSE devices
TP9	GND	PSE_3.3V ground
TP10	3.3V_ISO	Isolated 3.3V for MSP430
TP11	3.3V	3.3 V for debug
TPS12 , TP13	GND_ISO	3.3V_ISO ground
TP14	OSS	OSS signal from MCU to PSE
TPS23882EM-084		
TP1	PSE_3.3	3.3 V for PSE devices
TP2	VPWR	VPWR for PSE devices
TP3, TP4, TP14, TP19	GND	VPWR and PSE_3.3V ground
TP5	3.3V_ISO	Isolated 3.3 V
TP6	RESET	Reset signal from MCU
TP7	OSS	OSS signal from MCU
TP8	INT	INT signal to MCU
TP9	SDA	I^2C data from/to MCU
TP10	SCL	I^2C clock from MCU
TP11	PSE_RST	Reset signal to PSE
TP12	PSE_OSS	OSS signal to PSE
TP13	PSE_INT	INT signal from PSE
TP15	GND_ISO	3.3V_ISO ground
TP16	PSE_SCL	I^2C clock signal to PSE
TP17	PSE_SDAI	I^2C data to PSE
TP18	PSE_SDAO	I^2C data from PSE

3.2.1.2.3 EVM Jumpers

表 6 lists the EVM test jumpers and their descriptions.

表 6. EVM Test Jumpers

JUMPER	DEFAULT PIN POSITION	DESCRIPTION
PSEMTHR24EVM-081		
J13	1-2	3.3 V comes from PSE daughtercard
J14	1-2	Connect 3.3V_ISO to supply the circuit
J17, J22, J38, J43, J19, J23, J32, J28, J52, J47, J31, J26	1-2	Enable port LED
J45, J42, J24, J21, J44, J49, J53, J30, J33, J51, J54	1-2	Enable port LED
J57, J62, J78, J83, J59, J63, J72, J68, J92, J87, J71, J66	1-2	Enable port LED
J85, J82, J64, J61, J84, J80, J89, J93, J70, J91, J94	1-2	Enable port LED
TPS23882EVM-084		
J3	1-2, 3-4	PSE devices' address configuration

3.2.1.2.4 EVM Input and Output Connectors

表 7 lists the EVM input and output connectors.

表 7. EVM Input and Output Connectors

CONNECTOR	DESCRIPTION
PSEMTHR24EVM-081	
J1, J3	DC power supply input (44-57 V VDC, 41 A)
J2, J4, J6, J7	Edge connector for DC bus when connecting 2 boards together
J5	Power to PSE daughtercard
J8, J9	Edge connector for PSE signals (I^2C, OSS, RESET and INT) when connecting 2 boards together
J10	Connector to USB2ANY for direct I^2C access to PSE devices(for debug purpose only)
J11	Connectors to PSE daughter for PSE signals (I^2C, OSS, RESET and INT)
J12	Connectors to MSP430 daughter for PSE signals (I^2C, OSS, RESET and INT), system level signals (OC-ALERT, PG) and isolated 3.3 V
J15, J55	PSE ports magjacks
J34, J35, J36, J74, J75, J76	PSE port connector to PSE daughter card
J95, J96	For MSP430 daughter card mechanical mounting purpose
TPS23882EM-084	
J1	Pair with J5 on motherboard
J4	Pair with J11 on motherboard
J5	Pair with J34, J35, J36, J74, J75, J76 on motherboard
PSEMCUDAUEVM-082	
J1	JTAG connector
J3, J7, J8, J9	Extended GPIO access
J11	Pair with J12 on motherboard
J12, J13, J14	USB2ANY connector (30 pin)
J17, J18	For MSP430 daughter card mechanical mouting purpose

3.2.1.3 System Firmware GUI Setup

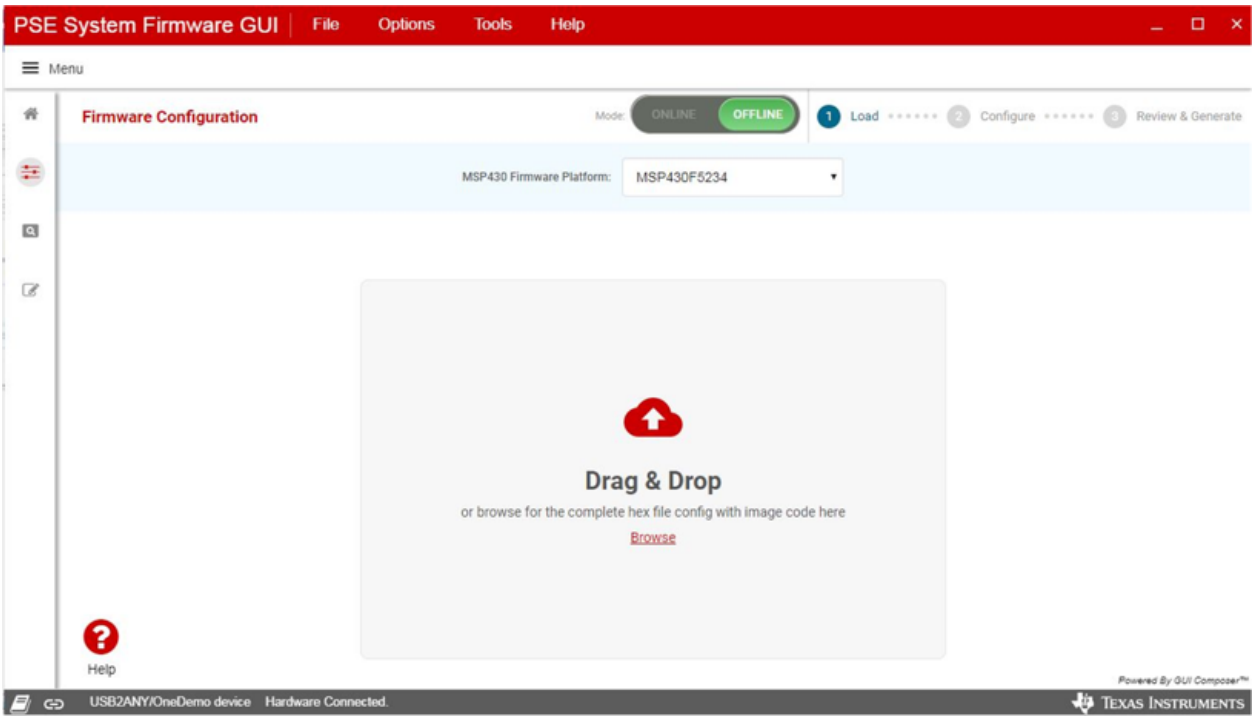
3.2.1.3.1 PSE System Firmware GUI Installation

TI's PSE system firmware GUI is used with the PSE system EVM kit (PSEMTHR24EVM-081, PSEMCUDAUEVM-082, TPS23882EVM-084) to configure the system, generate the code image and flash to MSP430 device. Download the PSE system firmware GUI from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder.

3.2.1.3.2 PSE System Firmware GUI Operation

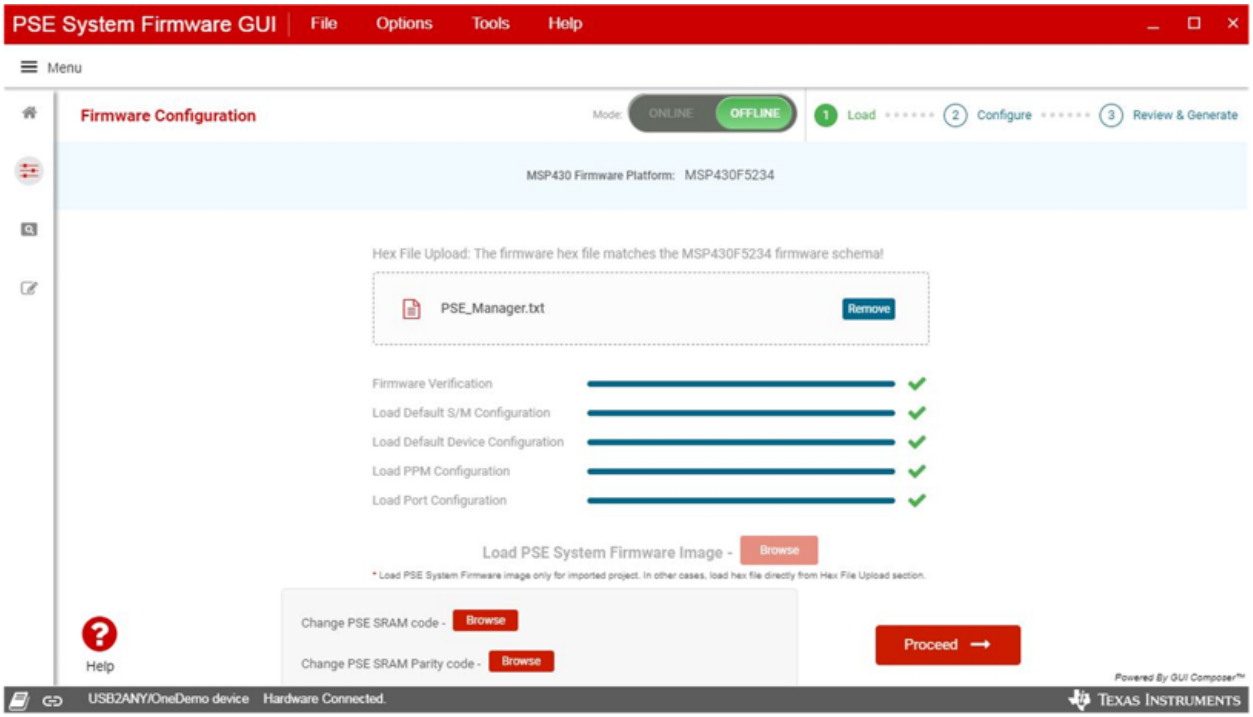
Start the PSE system firmware GUI by double clicking the GUI icon and clicking the Start button. A window similar to 図 3 appears. The Offline mode is selected by default.

図 3. GUI Startup



Select the MSP430 device you want to start with and then load the PSE system firmware code image (access from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder). When finished, click *Proceed* to go to the configuration page.

図 4. GUI Device Selection and Image Load



The configurations are split into four sections: system configuration, PPM (Port Power Management) configuration, device configuration, and port configuration.

The system configuration is applied to the whole system. This tab is always available on the to the right of the GUI. The following parameters can be configured through the system configuration tab:

- Legacy detection functions

  Legacy devices released prior to the PoE standard can be powered through the Ethernet cable. The PSE system firmware detects these legacy PDs and powers on with protection.

- Use of external sensing circuit

  The external sensing circuit is used to measure the total power consumption of the system. When the current exceeds the power budget, the MCU shuts down low priority ports. This increases the system response to the load step change.

- System bootup setting
  1. Turn on the PSE port as soon as the power is up.
  2. Turn on the PSE port after the PoE enable command is sent from the host

- Port overload retry mode
  1. Re-enable immediately: after overload happens, the port is re-enabled immediately. If the overload still presents, it will try at most five times and shuts down the port if the overload is not removed within five retries. The port is re-enabled after the PD is removed from the port and reconnects to the port.
  2. Re-enable after PD is disconnected and connected: after overload happens, the port is disabled immediately and is re-enabled after the PD is removed from the port and reconnects to the port.
  3. Timer controlled: the port is re-enabled immediately after overload happens. The port keeps retrying for a period (controller by timer) and is disabled after the timer expires. The port is re-enabled after the PD is removed from the port and reconnects to the port.

- OSS signal source (from MCU or CPLD):In a multi-power supply system, when one power supply has

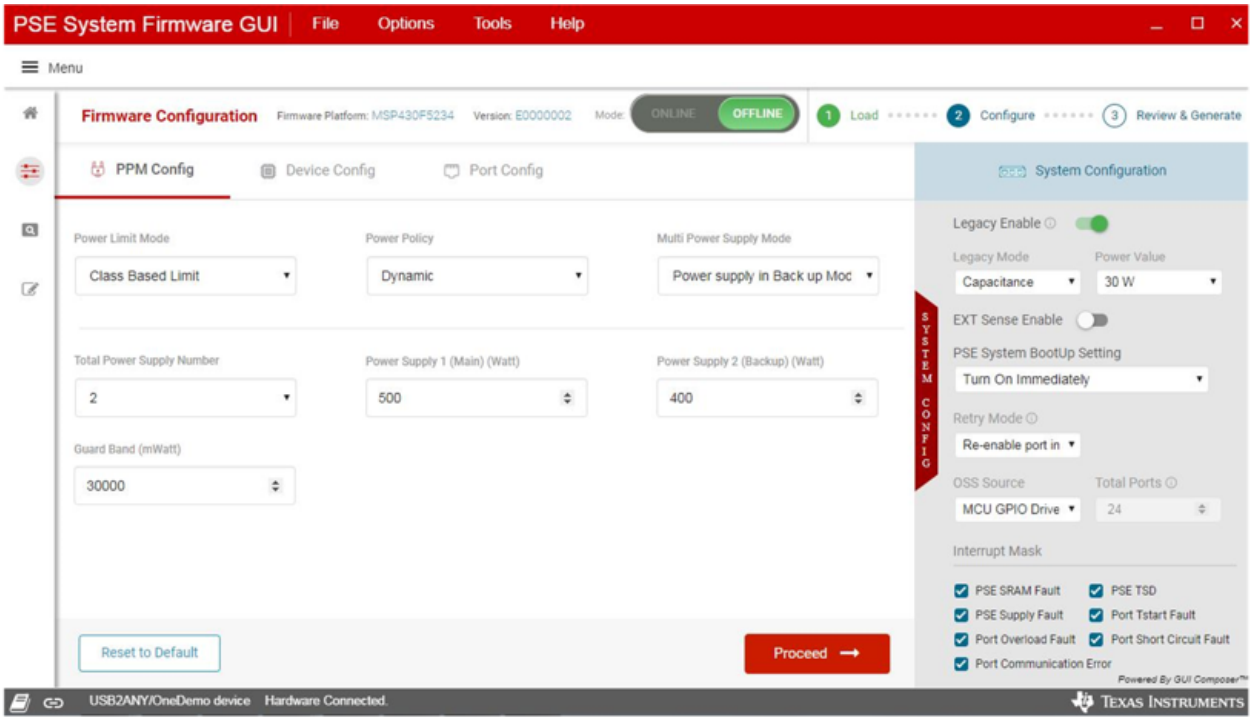
faults and the remaining power supply is not able to supply the current power consumption, turn off low priority ports to protect the remaining power supply. The OSS function of the PSE is used to fast shutdown the low priority ports. There are 2 sources to generate the OSS signal:

1. MSP430 generates the OSS signal
2. CPLD generates the OSS signal

- Interrupt mask

  The interrupt mask in 図 5 can be configured to enable interrupt events to notify the host through the MSP430 P6.0.

図 5. GUI System Configuration and PPM Configuration



PPM configuration is applied to the port power management mechanism. The following parameters can be configured through the PPM configuration tab:

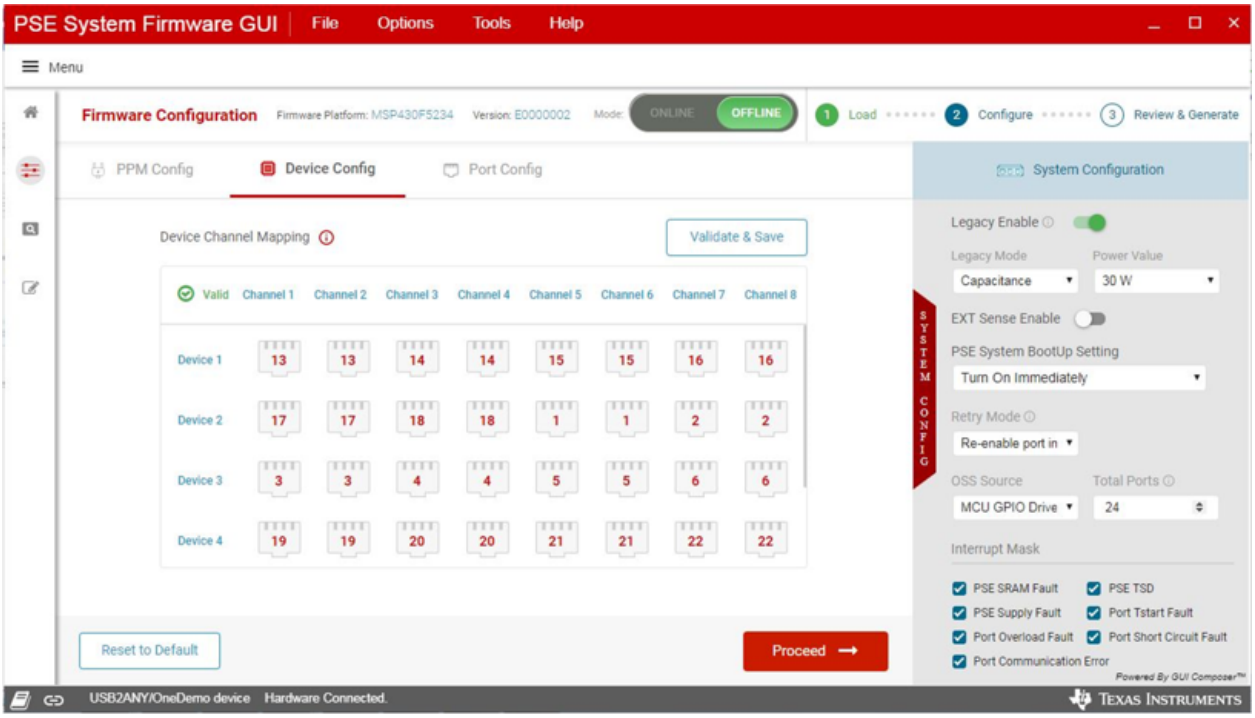
- Power limit mode:class limit mode and port limit mode
  1. Class limit mode:in class limit mode, the port power is limited by the PD's class level. For example, if the PD is class 8, the port power limit(PCUT) is set to 90W.
  2. Port limit mode:in port limit mode, the port power is limited by the host. The host should set port power limit before the port is powered on.
- Power policy: static and dynamic mode
  1. Static mode:in static mode, the port power allocation is set to port power limit. In class limit mode, port power allocation is class level power of the PD and in port limit mode, the port power allocation is the port power limit configured from the host.
  2. Dynamic mode: in dynamic mode, the port power allocation equals to the port's actual consumed power. It allocates the port's unused power to other ports.
- Multi-power supply mode: RPS and sharing mode:
  1. Redundant power supply (RPS) mode:in RPS mode, the total power budget equals to main power supply's power budget when both main power supply and backup power supply are connected. The total power budget equals to backup power supply's power budget when the main power supply is disconnected.

2. Sharing power supply mode:in sharing mode, the total power budget equals to the sum of two power supplies' power budget when both power supplies are connected. The total power budget equals to remaining power supply's power budget if one of the power supplies is disconnected.

- Total number of power supplies and the power budget of each power supply. **If there's only one power supply, the power good signal must be connected to P1.5.**
- Power guard band: when the total allocated power < total power budget — guard band, there's no more low priority ports to be turned on and the guard band LED will turn on.

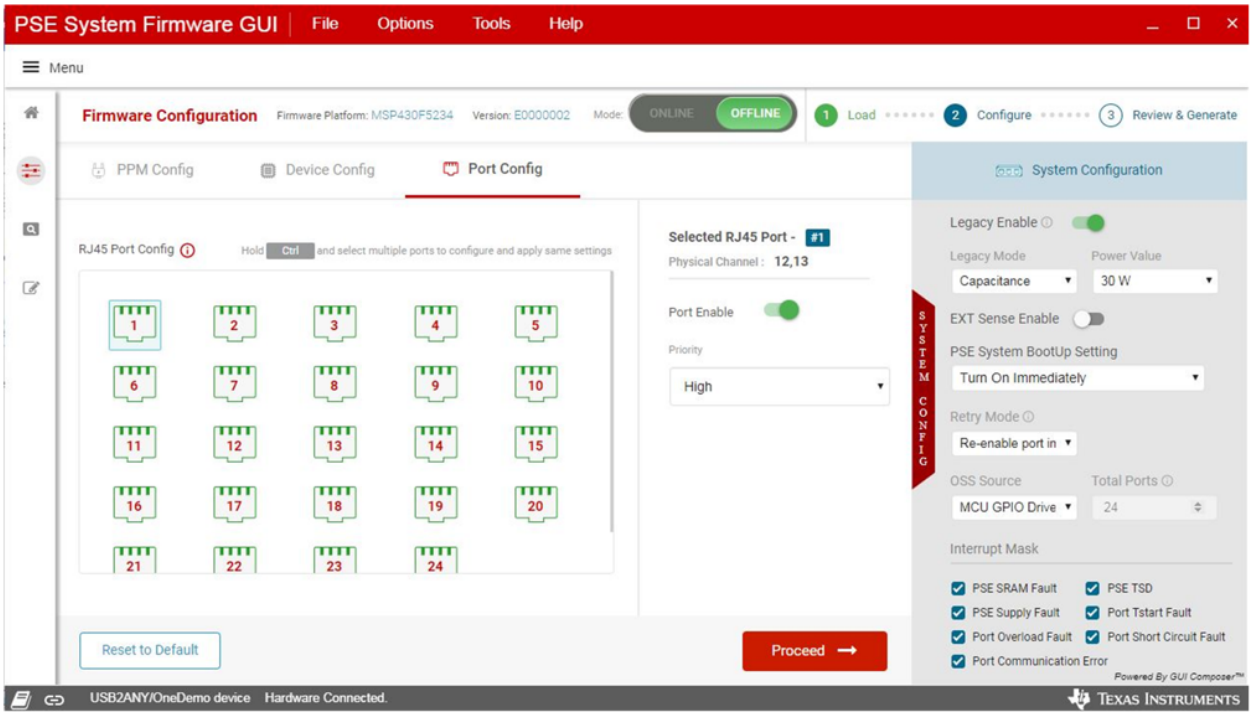
Device configuration is mainly used to configure the mapping between the PSE device channels and the logical RJ45 ports. When mapping a 4-pair port, only channels within the same quad (channel 1–4 or channel 5–8) can be mapped to one 4-pair port.

図 6. GUI Device Configuration



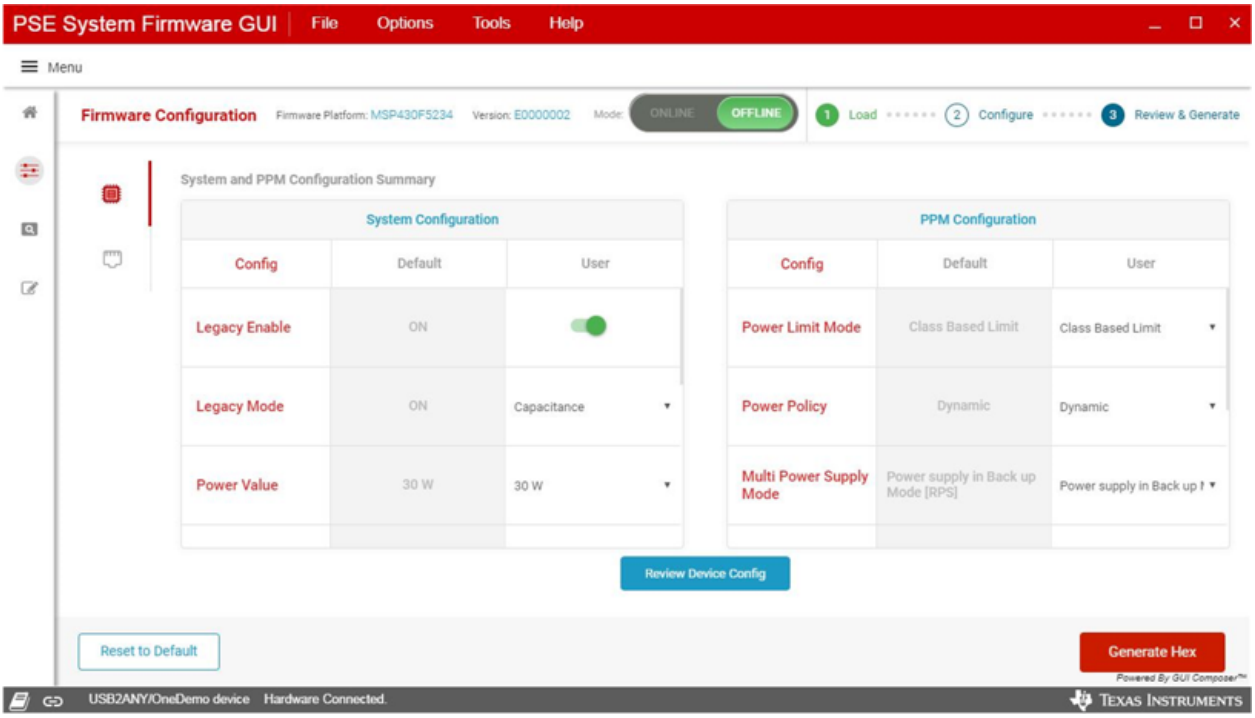
The *Port Configuration* is applied to the port by port settings, such as port PoE enable and disable, port priority, and port power limit (only in port limit mode).

図 7. GUI Port Configuration



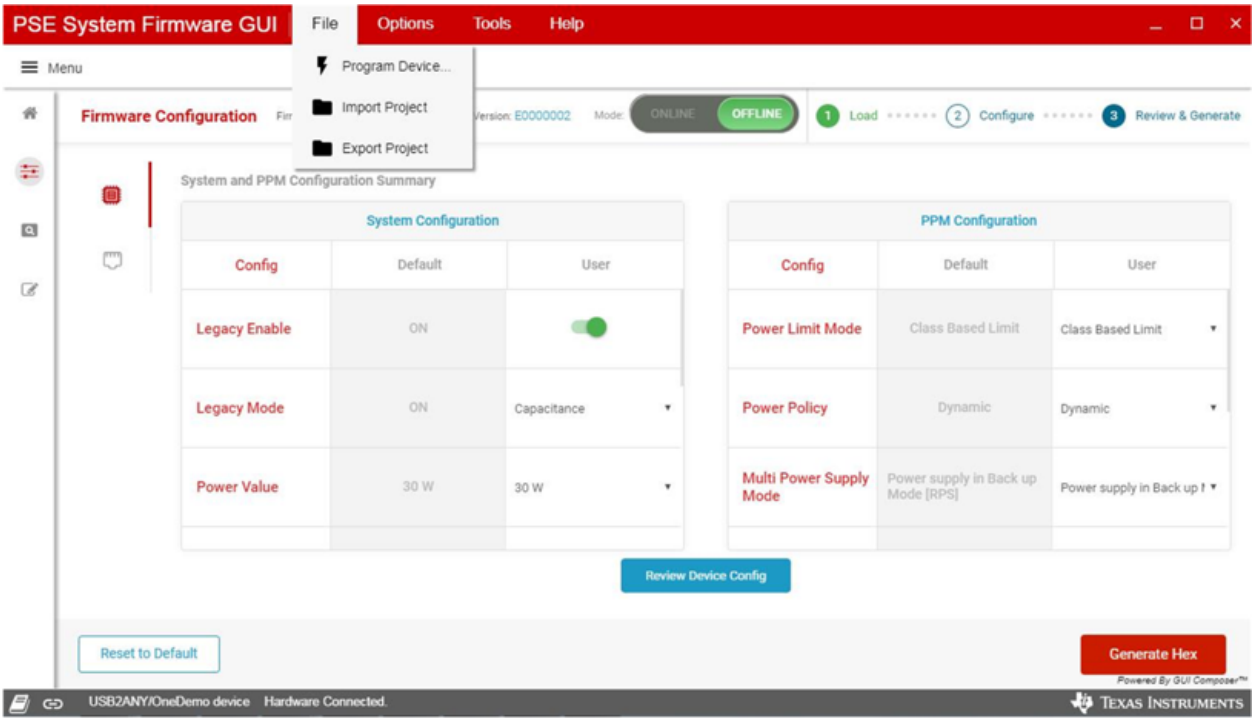
When everything has been configured, click the *Proceed* button. The summary page displays all of the configurations being set compared to the factory default configurations. When everything is verified, you can generate the hex file or flash the code to the MSP430 device directly.

図 8. GUI Configuration Summary



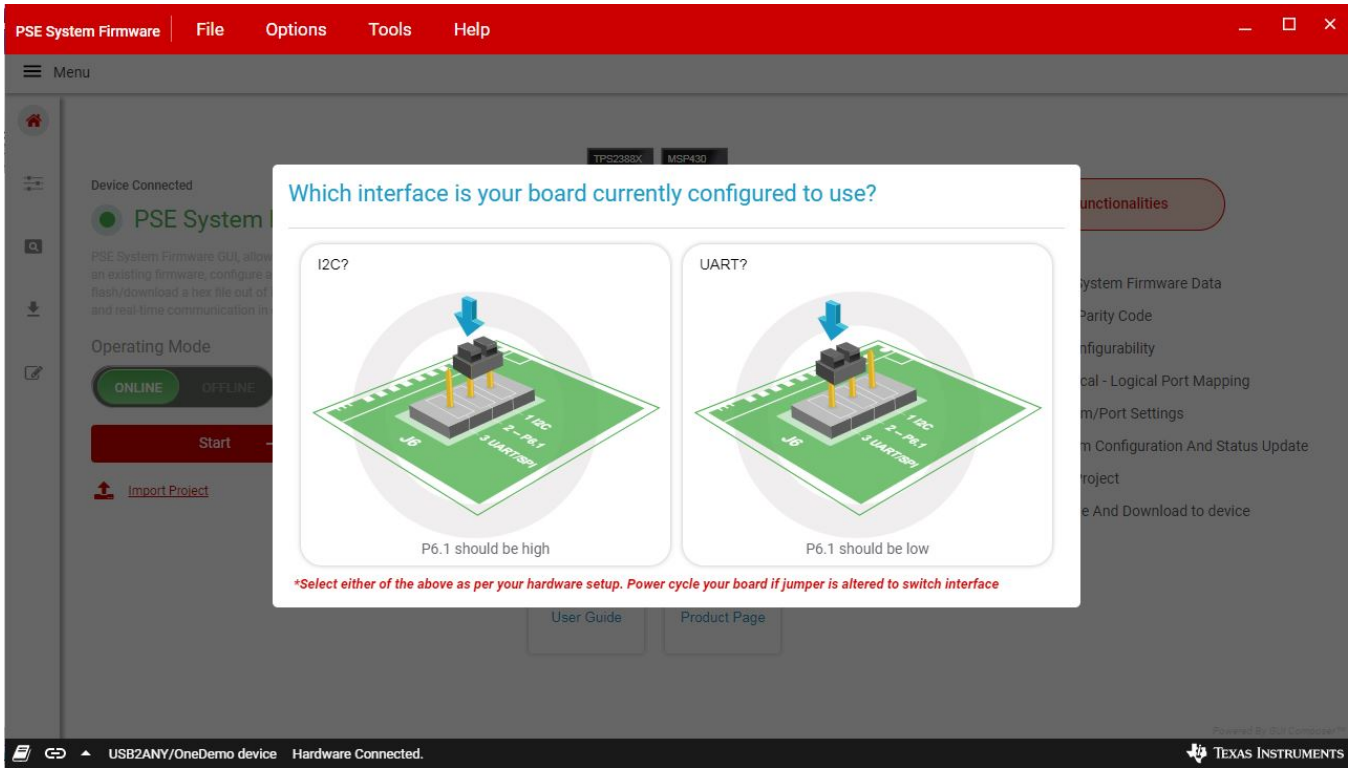
When configurations are reviewed, the GUI can generate the default code image and program the device directly through **MSP-FET**.

図 9. GUI Program Device and Generate Hex



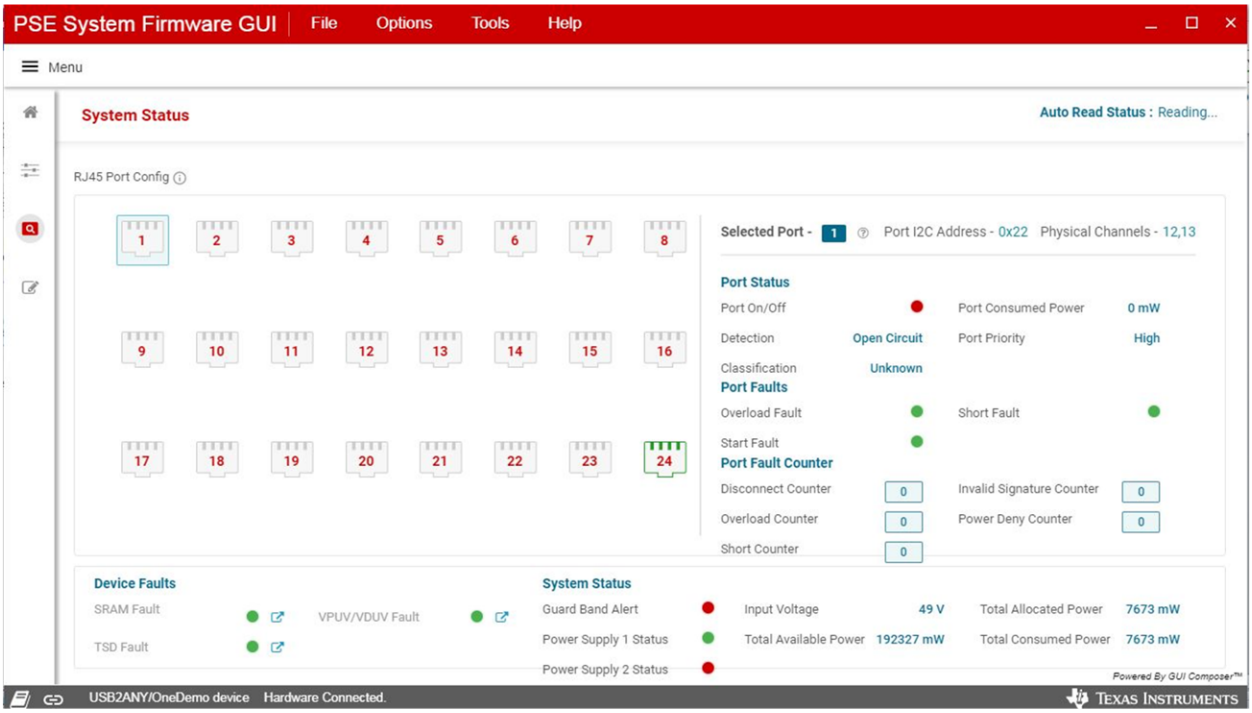
When the code is successfully flashed to the MSP430, the system will be up and running. MSP-FET can be disconnected from the laptop or PC. Connect the USB2ANY (with 30-pin ribbon cable) to a laptop or PC and the GUI will be in online mode after selecting host interface protocol.

図 10. Host Interface Protocol Selection in Online Mode



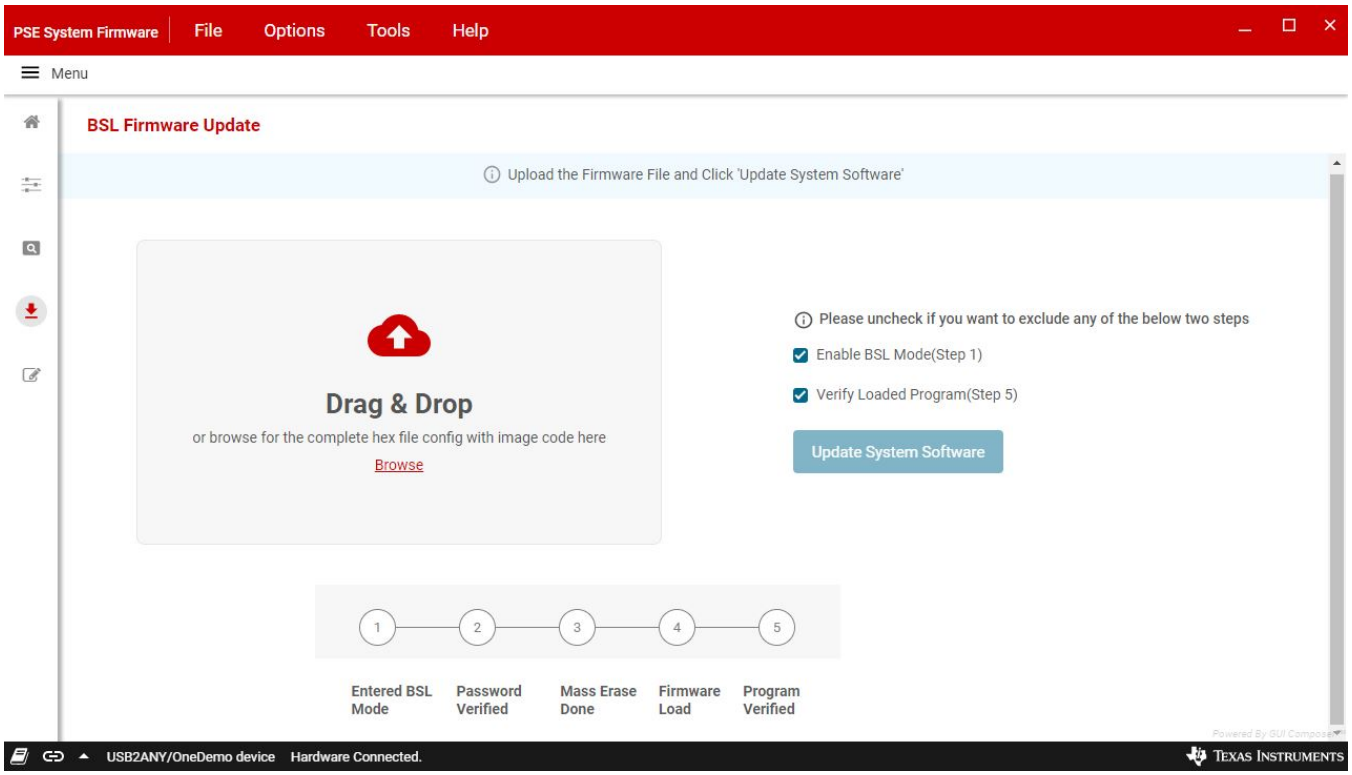
When the device is connected to GUI, real-time changes can be made on the configuration page and status page shows the real time system status. The status page shows the system, device, and port real-time status. The user can also change the system configuration in the configuration page: each change is converted to a host command to the MSP430 MCU. The user can also press the *Save Configuration* button to save the current configuration as the default setting.

図 11. GUI Status Page



The BSL firmware update page provides the field firmware upgrade functions that the firmware can be upgraded through the same I^2C or UART port as the normal communication. This is beneficial to firmware upgrade after the product is released to customers.

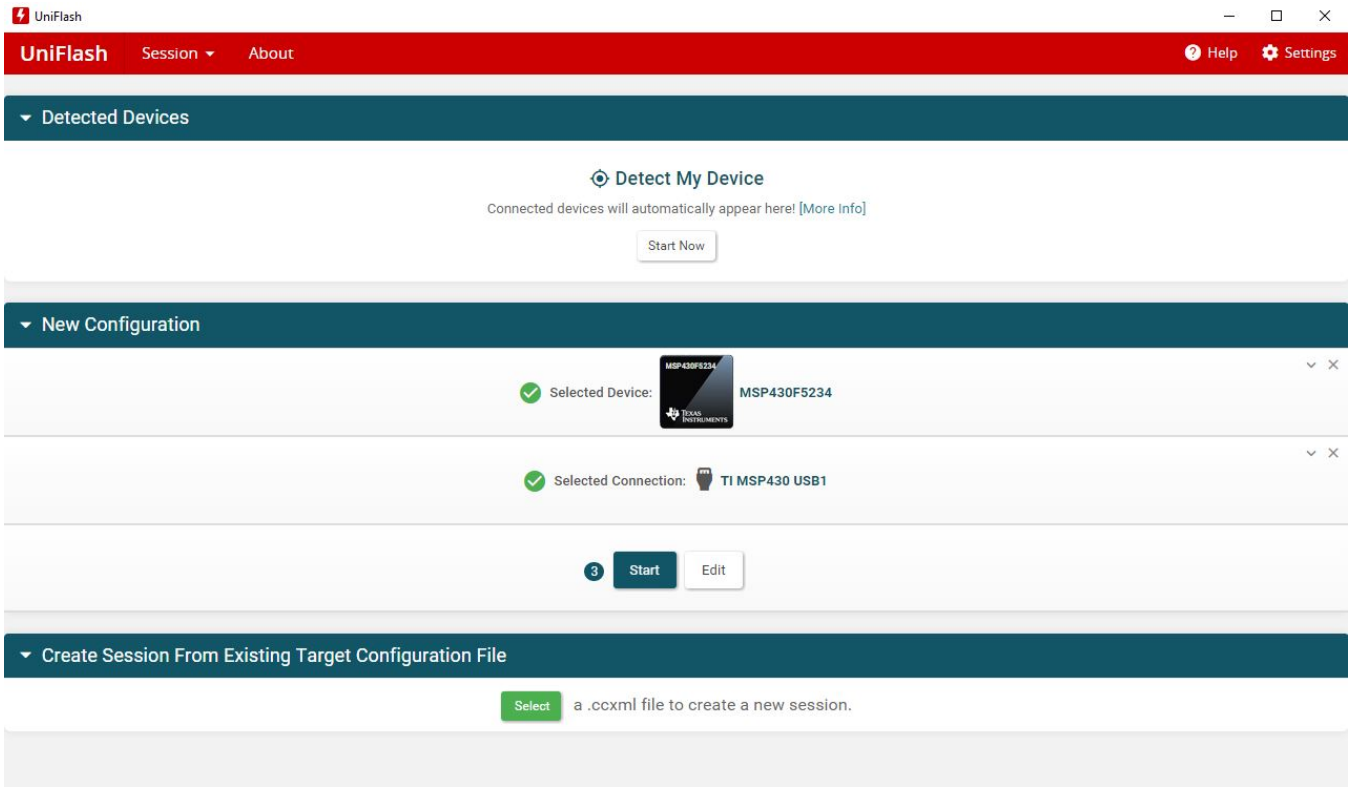
図 12. BSL Firmware Update Page



Before using BSL page to update the MSP430 firmware, BSL code needs to be flashed to MSP430 if it hasn't been flashed. Download Uniflash from ti.com and use it to flash the BSL code by following the steps:

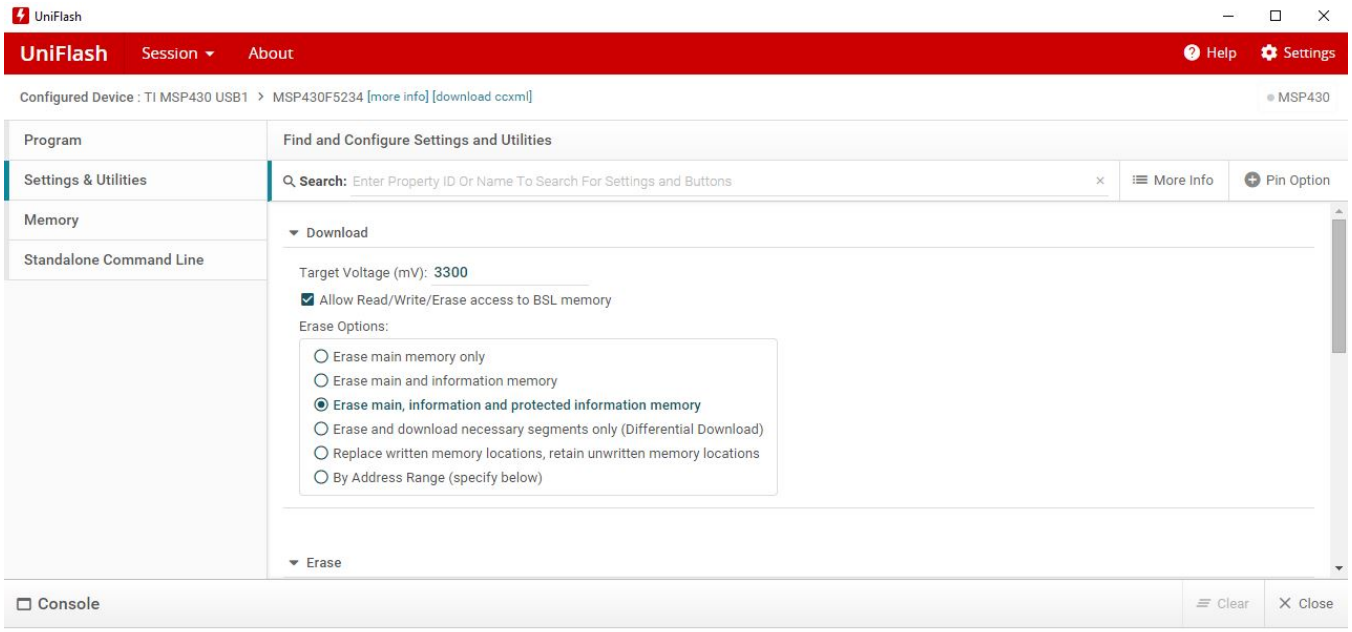
Select MCU device to MSP430F5234.

図 13. MCU Device Selection Page



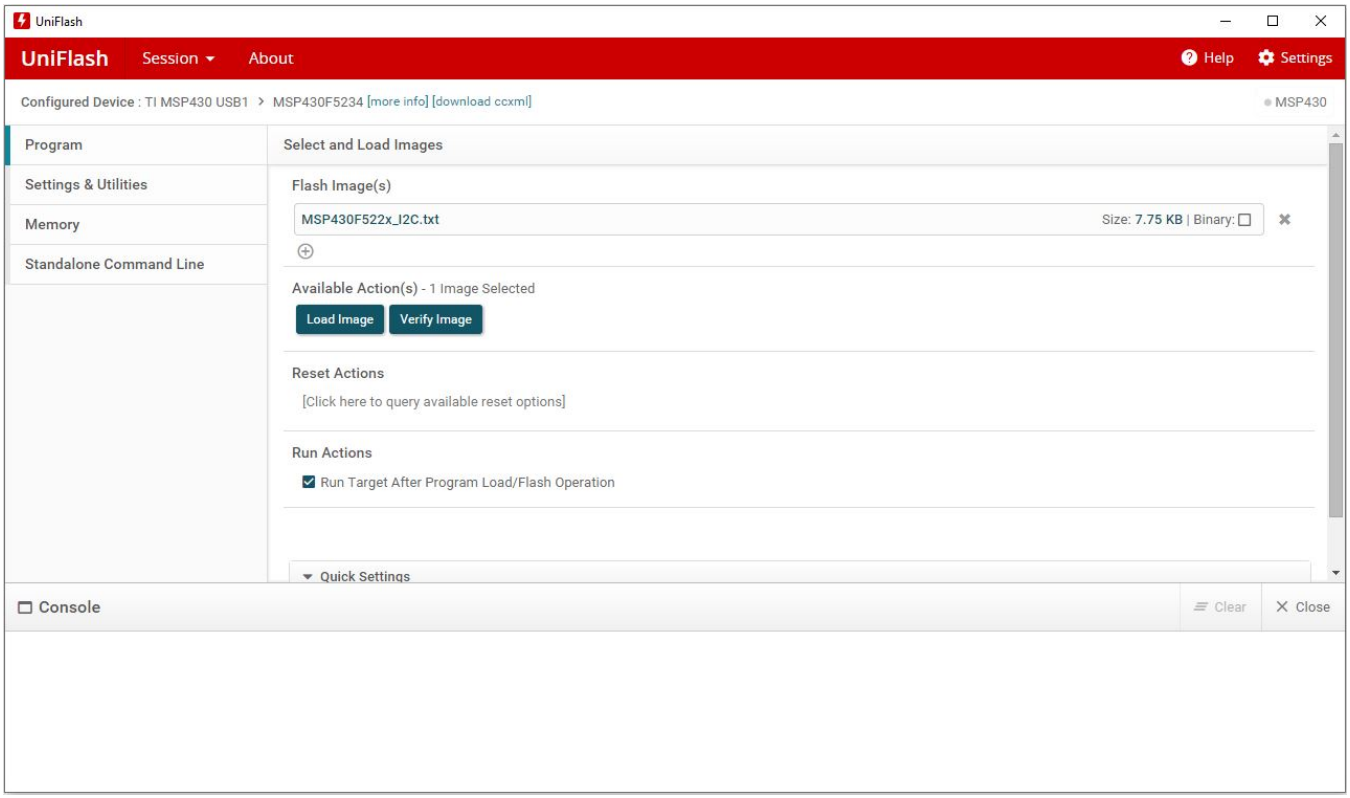
Configure the flash section.

図 14. Configure Settings and Utilities Page



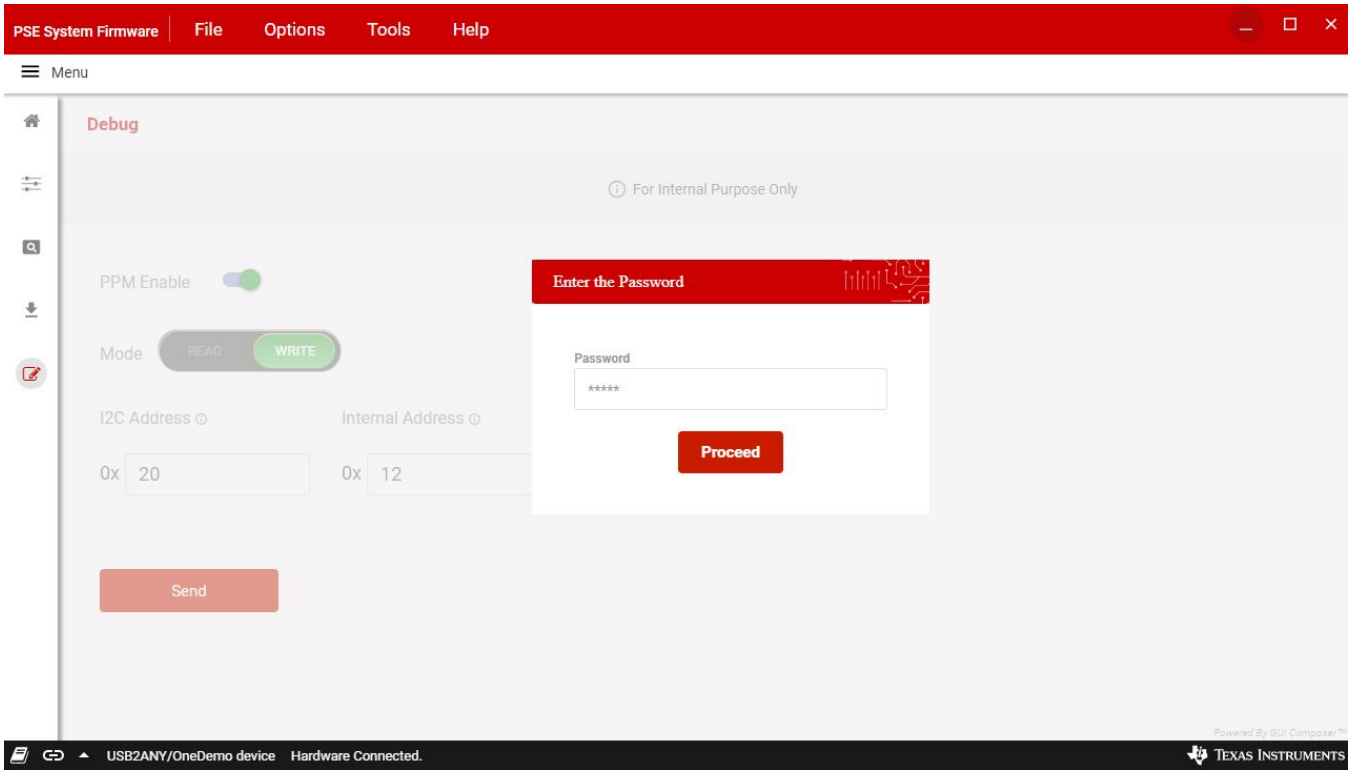
Load BSL code and flash to MSP430.

図 15. Select and Load Images Page



In the debug page, user's can read and write raw data to MSP430 following host interface protocol and to each PSE device's registers by providing I^2C address and register number. The password is "C430".

図 16. Debug Page



3.2.2 Test Results

The IEEE 802.3bt compliance test suite is currently not available. The test report will be added in the fourth quarter of 2019.

4 Design Files

4.1 Schematic

To download the schematics, see the design files at TIDA-050026-23882.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050026-23882.

4.3 PCB Layout Recommendations

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSEC is shared between SEN5 and SEN6, KSENSED is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize the impact of PCB trace resistance. Refer to the TPS23882 Layout section as an example.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050026-23882.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-050026-23882.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050026-23882.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050026-23882.

5 Software Files

To download the software files, see the design files at TIDA-050026-23882.

6 Related Documentation

1. Texas Instruments, *TPS23882 High-Power, 8-Channel, Power-Over-Ethernet PSE With 200-mΩ R_{SENSE}*
2. Texas Instruments, *TPS2388x PSE System Firmware Host Interface Protocol User's Guide*

6.1 商標

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