TEXAS INSTRUMENTS

XTR115, XTR116
JAJS367B – JANUARY 2000 – REVISED JUNE 2023

XTR11x 4～20mA 電流ループ･トランスミッタ

1 特長

- 低静止電流：200μA
- 外部回路用の 5V レギュレータ
- センサ起動用の V_{REF}：
  - XTR115：2.5V
  - XTR116：4.096V
- 低いスパン誤差：0.05%
- 低い非直線性誤差：0.003%
- 広いループ電源電圧範囲：7.5V～36V
- SO-8 パッケージ

2 アプリケーション

- 2 線式、4～20mA 電流ループ
- トランスミッタ
- スマート・ トランスミッタ
- 産業用プロセス制御
- テスト・ システム
- HART モデムと互換
- 電流アンプ
- 電圧電流アンプ

3 概要

XTR115 および XTR116 (XTR11x) は、業界標準の電流ループを介してアナログ 4mA～20mA 信号を送信するように設計された高精度電流出力コンバータです。これらのデバイスは、正確な電流スケーリングと出力電流制限機能を提供します。

オンチップ電圧レギュレータ (5V) を使用して、外部回路に電力を供給できます。高精度のオンチップ V_{REF} (XTR115 では 2.5V、XTR116 では 4.096V) を使用して、オフセットやトランスデューサの起動を行うことができます。電流帰還ピン (I_{RET}) は、外部回路で使用される電流を検出し、出力電流を正確に制御します。

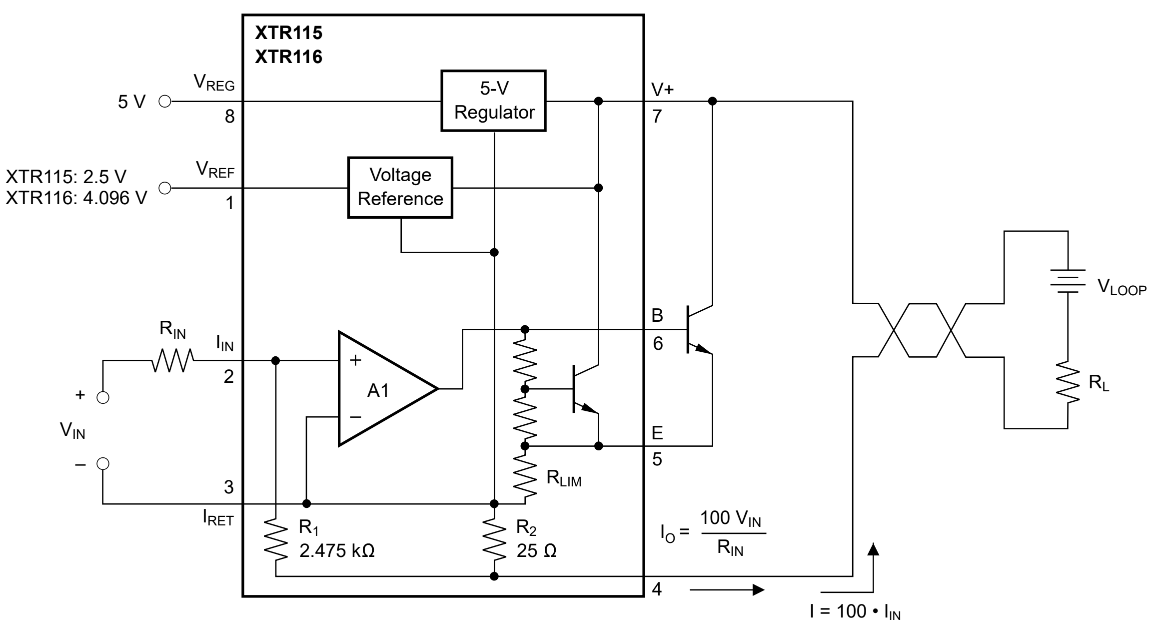
XTR11x は、4mA～20mA の電流伝送を使用するスマート・ センサの基本的なビルディング・ ブロックです。

XTR11x は、拡張産業用温度範囲の -40℃～+85℃で動作が規定されています。

製品情報

部品番号	オンチップ V_{REF}	パッケージ(1)
XTR115	2.5V	D (SOIC、8)
XTR116	4.096V	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2003) to Revision B (March 2022) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.................... 1
- 「ピンの機能」、「ESD 定格」、「熱に関する情報」、「推奨動作条件」、「電気的特性」の各表、および「詳細説明」、「概要」、「機能ブロック図」、「機能説明」、「アプリケーションと実装」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを追加.................... 1
- Added *Pin Functions* table.................... 3
- Changed operating temperature minimum value from –55°C to –40°C in *Absolute Maximum Ratings* 4
- Deleted thermal resistance, θ_{JA} specification of 150 °C/W from *Electrical Characteristics*; added a *Thermal Information* table, with $R_{\theta JA}$ = 128.2 °C/W and other detailed thermal parameters.................... 4
- Changed span error test condition from: I_{IN} = 250 µA to 25 mA to: I_{OUT} = 250 µA to 25 mA in *Electrical Characteristics* 5
- Changed V_{REF} voltage accuracy vs load typical value from ±100 ppm/mA to ±200 ppm/mA in *Electrical Characteristics* 5
- Changed bias current vs temperature typical value from 150 pA/°C to 300 pA/°C in *Electrical Characteristics* 5
- Changed *Basic Circuit Connections* application diagram.................... 9
- Changed *External Transistor* applications information section to incorporate additional guidance regarding transistor power dissipation and thermal concerns.................... 10
- Added *Circuit Stability* application information section.................... 12

5 Pin Configuration and Functions

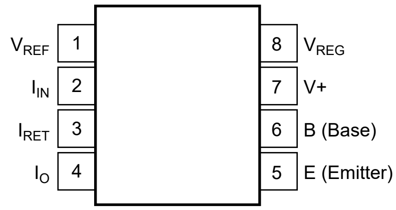


図 5-1. D Package, SOIC-8 (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{REF}	Output	Reference voltage output (2.5 V for XTR115, 4.096 V for XTR116)
2	I_{IN}	Input	Current input pin
3	I_{RET}	Input	Local ground return pin for V_{REG} and V_{REF}
4	I_O	Output	Regulated 4-mA to 20-mA current-loop output
5	E (Emitter)	Input	Emitter connection for external transistor
6	B (Base)	Output	Base connection for external transistor
7	V+	Power	Loop power supply
8	V_{REG}	Output	5-V regulator voltage output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V+	Power supply (referenced to I_O pin)		40	V
	Input voltage (referenced to I_{RET} pin)	0	V+	V
	Output current limit	Continuous		
	V_{REG}, short-circuit	Continuous		
	V_{REF}, short-circuit	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		165	°C
T_{stg}	Storage temperature	–55	125	°C
	Lead temperature (soldering, 10 s)		300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply voltage	7.5	24	36	V
T_A	Specified temperature	–40		85	°C

6.3 Thermal Information

THERMAL METRIC[(1)]		XTR11x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.4 Electrical Characteristics

at T_A = 25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

PARAMETER		TEST CONDITIONS	XTR115U, XTR116U			XTR115UA, XTR116UA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT									
I_O	Output current equation			$I_O = I_{IN} \times 100$			$I_O = I_{IN} \times 100$		
	Output current, linear range		0.25		25	0.25		25	mA
I_{LIM}	Overscale limit			32			32		mA
I_{MIN}	Underscale limit	I_{REG} = 0, I_{REF} = 0		0.2	0.25		0.2	0.25	mA
SPAN									
S	Span (current gain)			100			100		A/A
	Error(1)	I_{OUT} = 250 mA to 25 mA		±0.05	±0.2		±0.05	±0.4	%
	vs Temperature	T_A = –40°C to +85°C		±3	±20		±3	±20	ppm/°C
	Nonlinearity	I_{IN} = 250 mA to 25 mA		±0.003	±0.01		±0.003	±0.02	%
INPUT									
V_{OS}	Offset voltage (op amp)	I_{IN} = 40 mA		±100	±250		±100	±500	µV
	vs Temperature	T_A = –40°C to +85°C		±0.7	±3		±0.7	±6	µV/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		±0.1	±2		±0.1	±2	µV/V
I_B	Bias current			–35			–35		nA
	vs Temperature			300			300		pA/°C
e_n	Noise: 0.1 Hz to 10 Hz			0.6			0.6		µVp-p
DYNAMIC RESPONSE									
	Small signal bandwidth	C_{LOOP} = 0, R_L = 0		380			380		kHz
	Slew rate			3.2			3.2		mA/µs
V_{REF} (2)									
	XTR115			2.5			2.5		V
	XTR116			4.096			4.096		V
	Voltage accuracy	I_{REF} = 0		±0.05	±0.25		±0.05	±0.5	%
	vs Temperature	T_A = –40°C to +85°C		±20	±35		±20	±75	ppm/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		±1	±10		±1	±10	ppm/V
	vs Load	I_{REF} = 0 mA to 2.5 mA		±200			±200		ppm/mA
	Noise	0.1 Hz to 10 Hz		10			10		µVp-p
	Short-circuit current			16			16		mA
V_{REG} (2)									
	Voltage			5			5		V
	Voltage accuracy	I_{REG} = 0		±0.05	±0.1		±0.05	±0.1	V
	vs Temperature	T_A = –40°C to +85°C		±0.1			±0.1		mV/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		1			1		mV/V
	vs Output current			See *Typical Characteristics*			See *Typical Characteristics*		
	Short-circuit current			12			12		mA
POWER SUPPLY, V+									
	Quiescent current			200	250		200	250	µA
		T_A = –40°C to +85°C		240	300		240	300	µA

(1) Does not include initial error or TCR of R_{IN}.
(2) Voltage measured with respect to I_{RET} pin.

6.5 Typical Characteristics

At T_A = 25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

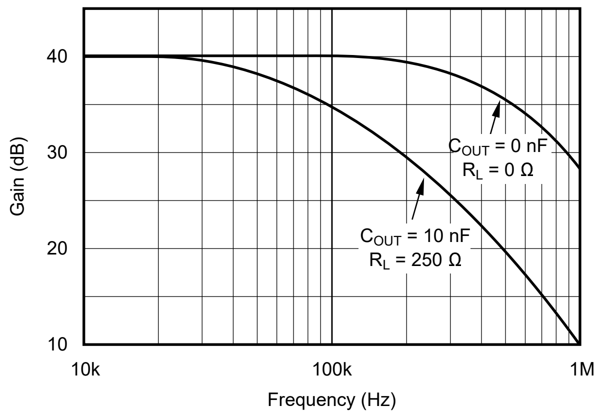


図 6-1. Current Gain vs Frequency

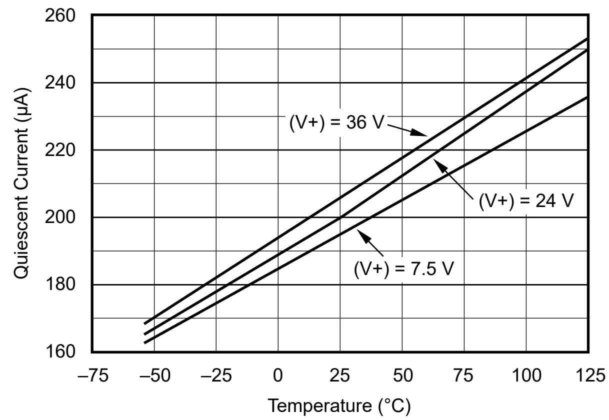


図 6-2. Quiescent Current vs Temperature

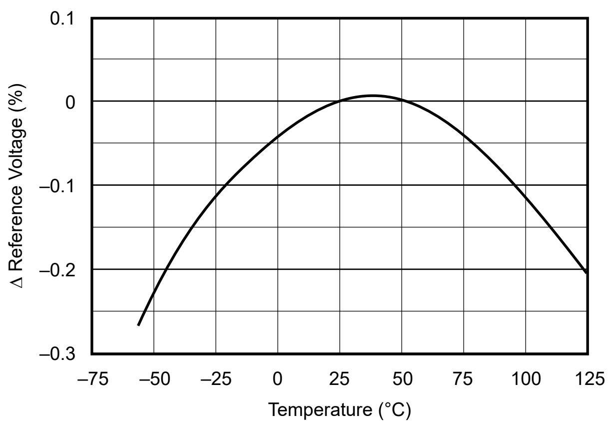


図 6-3. Reference Voltage vs Temperature

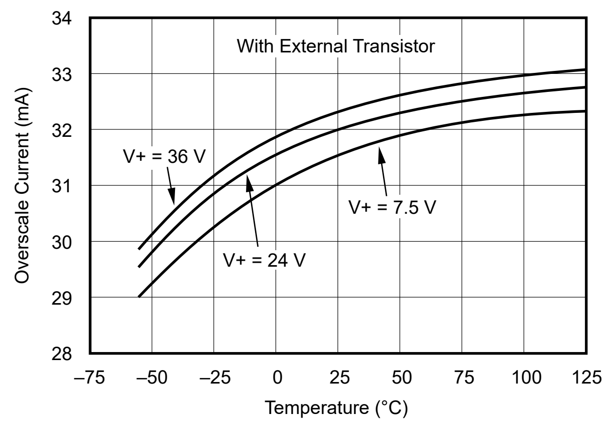


図 6-4. Overscale Current vs Temperature

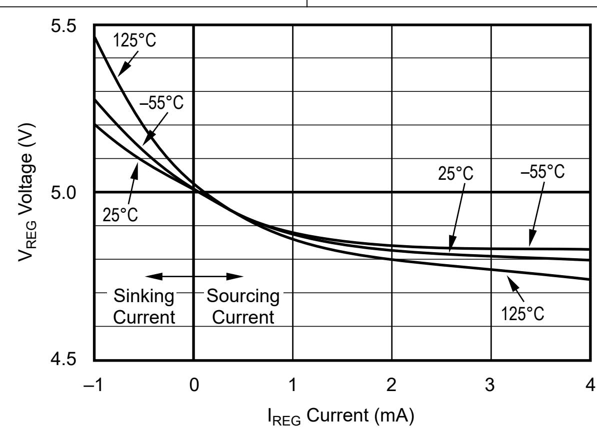


図 6-5. V_{REG} Voltage vs V_{REG} Current

7 Detailed Description

7.1 Overview

The XTR115 and XTR116 are precision current output converters designed to transmit analog 4-mA-to-20-mA signals over an industry standard current loop. The regulator and reference voltages power a sensor, such as a bridge as shown in 図 7-1. The sensor output, as a current signal I_{IN}, is gained up and transmitted over the loop to be read by a receiver.

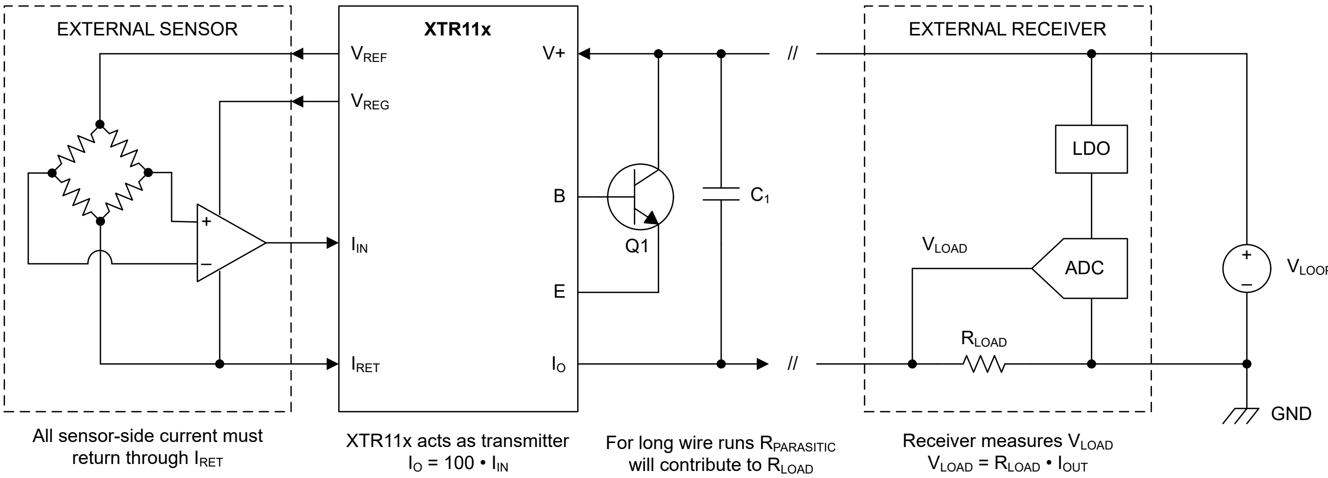
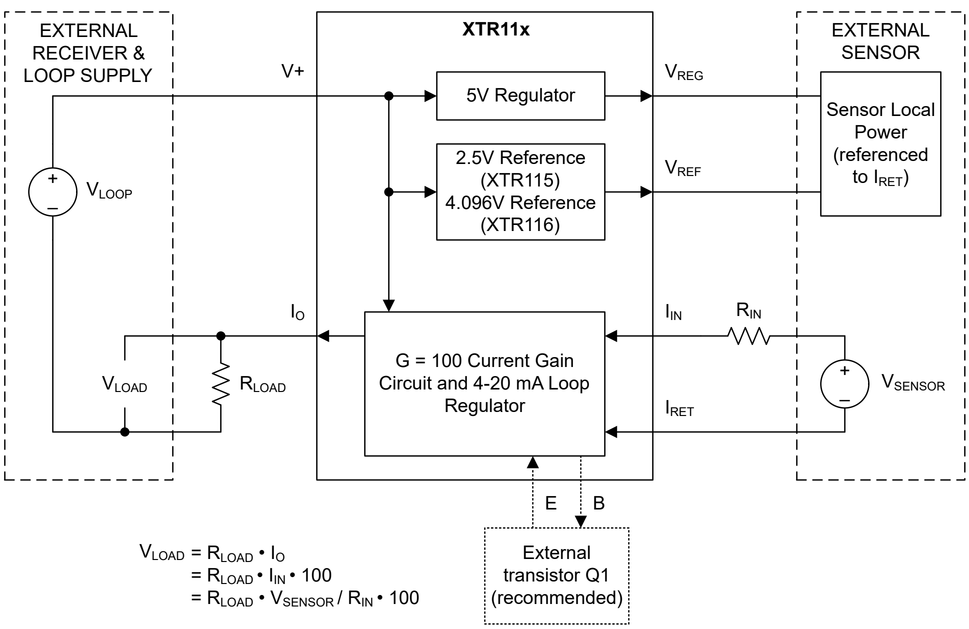


図 7-1. Typical Schematic

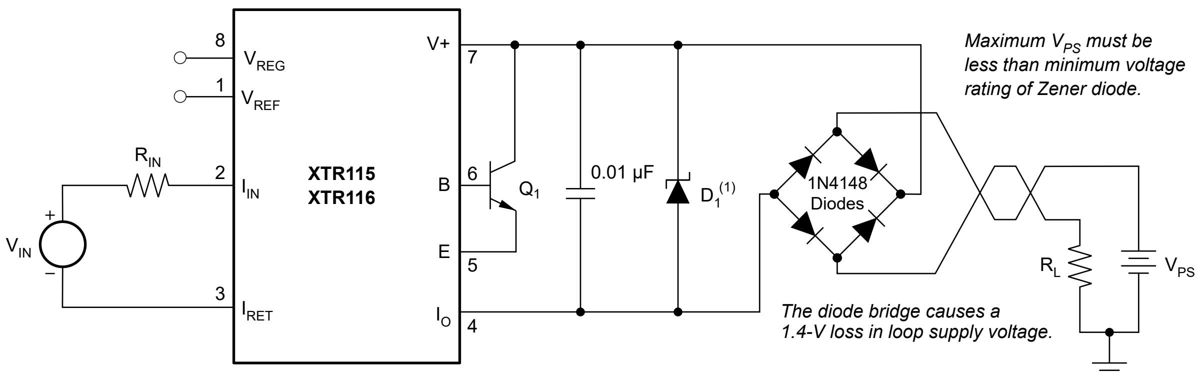
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reverse-Voltage Protection

The XTR11x low compliance voltage rating (7.5 V) permits the use of various voltage protection methods without compromising the operating range. 図 7-2 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two-diode drop (approximately 1.4 V) loss in loop supply voltage. This loss results in a compliance voltage of approximately 9 V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7-V loss in loop supply voltage.



(1) Zener Diode 36 V: 1N4753A or Motorola P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages less than 30 V for increased protection; see セクション 7.3.2.

図 7-2. Reverse Voltage Operation and Overvoltage Surge Protection

7.3.2 Overvoltage Surge Protection

Remote connections to current transmitters can sometimes be subjected to voltage surges. Best practice is to limit the maximum surge voltage applied to the XTR11x to as low as practical. Various Zener and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36-V protection diode provides proper transmitter operation at normal loop voltages, and also provides an appropriate level of protection against voltage surges. Characterization tests on several production lots showed no damage with loop supply voltages up to 65 V.

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, also use a series diode or diode bridge for protection against reversed connections.

8 Application and Implementation

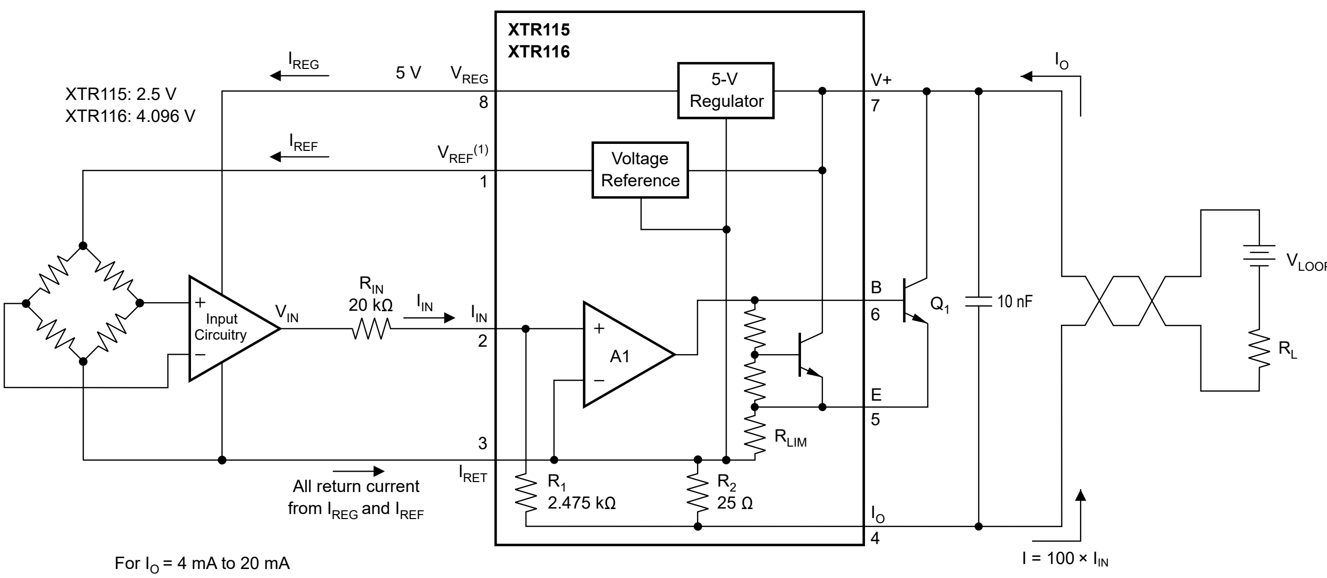
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The XTR115 and XTR116 are identical devices except for the reference voltage output, pin 1. This voltage is available for external circuitry and is not used internally. Further discussions that apply to both devices refer to the XTR11x.

図 8-1 shows basic circuit connections with representative simplified input circuitry. The XTR11x is a two-wire current transmitter. The device input signal (pin 2) controls the output current. A portion of this current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the XTR11x can be powered from VREG or VREF. Current drawn from these terminals must be returned to IRET, pin 3. This IRET pin is a *local ground* for input circuitry driving the XTR11x.



For I_O = 4 mA to 20 mA
I_{IN} = 40 µA to 200 µA

With R_{IN} = 20 kΩ
V_{IN} = 0.8 V to 4 V

Possible choices for Q_1(2)

TYPE	PACKAGE
2N4922G	TO-126
FCX690BTA	SOT-89-3
MMBTA28-7-F	SOT-23-3

(1) Also see 図 8-4.
(2) See セクション 8.1.1.

図 8-1. Basic Circuit Connections

The XTR11x is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \cdot I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is created with an external input resistor, as shown. Common full-scale input voltages range from 1 V and upward. Full-scale inputs greater than 0.5 V are recommended to minimize the effect of offset voltage and drift of A1.

8.1.1 External Transistor

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8 W with high loop voltage (40 V) and 20 mA of output current. The XTR11x is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 still causes ambient temperature changes that can affect the XTR11x. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including the XTR11x. Mount Q_1 so that heat is conducted to the outside of the transducer housing and away from the XTR11x.

The XTR11x is designed to use virtually any NPN transistor with sufficient voltage, current, and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in 図 8-1. A MOSFET transistor does not improve the accuracy of the XTR11x and is not recommended. Although the XTR11x can be used without an additional external transistor, this configuration is not always practical at higher loop voltages and currents because of self-heating concerns.

8.1.2 Minimum Scale Current

The quiescent current of the XTR11x (typically 200 µA) is the lower limit of the device output current. Zero input current (I_{IN} = 0 A) produces an I_O equal to the quiescent current. Output current does not begin to increase until $I_{IN} > I_Q / 100$. Current drawn from V_{REF} or V_{REG} adds to this minimum output current. This means that more than 3.7 mA is available to power external circuitry while still allowing the output current to go below 4 mA.

8.1.3 Offsetting the Input

A low scale of 4 mA is produced by creating a 40-µA input current. This low-scale offset can be created with the proper value resistor from V_{REF} (as shown in 図 8-2, or by generating offset in the input drive circuitry.

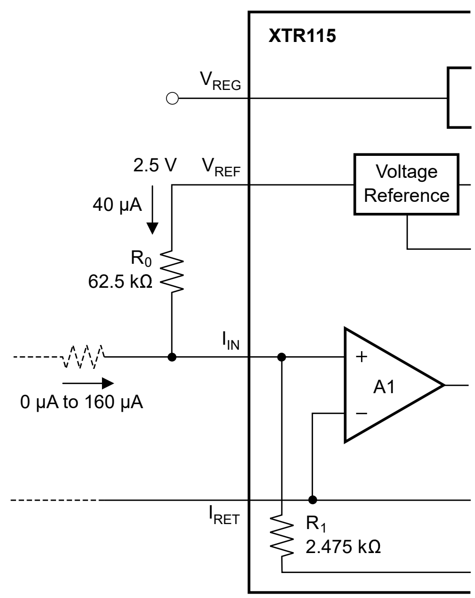


図 8-2. Creating Low-Scale Offset

8.1.4 Maximum Output Current

The XTR11x provide accurate, linear output up to 25 mA. Internal circuitry limits the output current to approximately 32 mA to protect the transmitter and loop power or measurement circuitry.

Extending the output current range of the XTR11x is possible by connecting an external resistor from pin 3 to pin 5 to change the current limit value.

注意

All output current must flow through internal resistors; therefore, damage is possible with excessive current. Output currents greater than 45 mA can cause permanent damage.

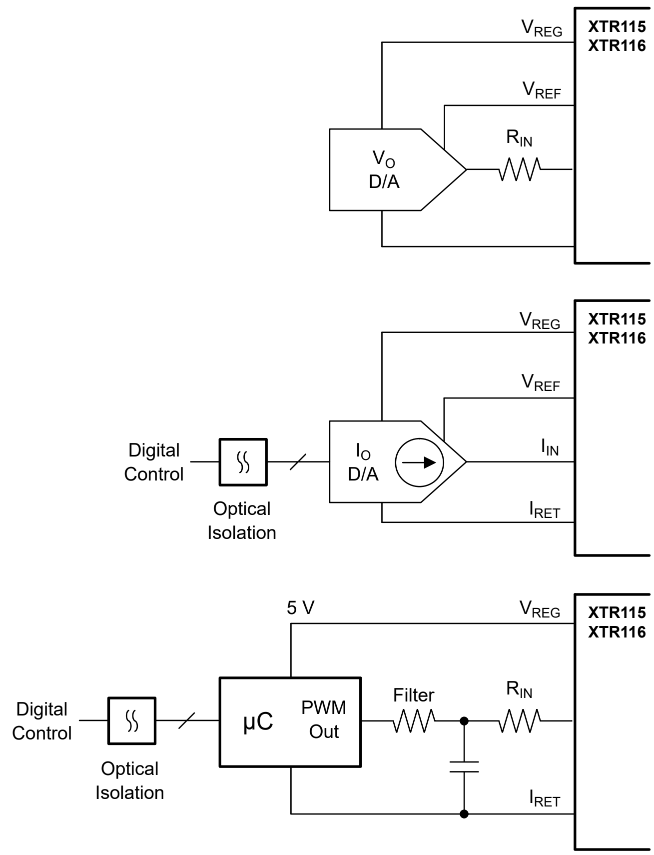


図 8-3. Digital Control Methods

8.1.5 Radio Frequency Interference

The long wire lengths of current loops invite radio frequency interference (RF). RF can be rectified by the input circuitry of the XTR11x or preceding circuitry. This RF generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference can also enter at the input pins. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current-loop connections.

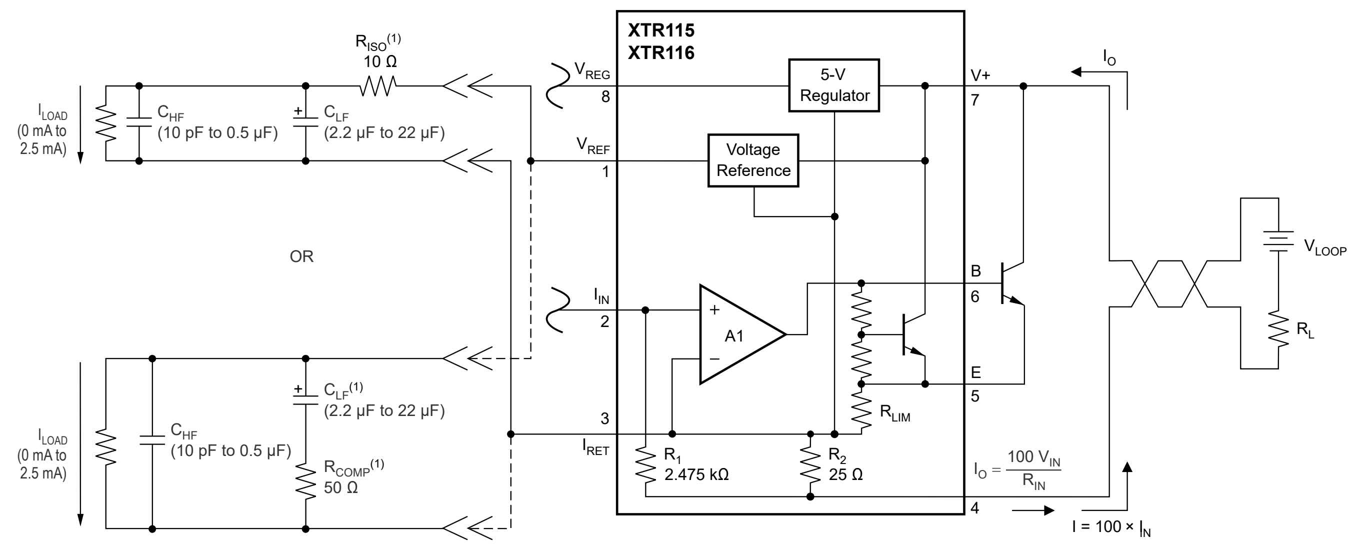
8.1.6 Circuit Stability

The 4-20 mA control-loop stability must be evaluated for any XTR11x design. A 10-nF decoupling capacitor between V+ and I_O is recommended for most applications. As this capacitance appears in parallel with the load resistance R_{LOAD} from a stability perspective, the capacitor and resistor form a filter corner that can limit the bandwidth of the system. Therefore, for HART applications, use a bypass capacitance of 2 nF to 3 nF instead.

For applications with EMI and EMC concerns, use a bypass capacitor with sufficiently low ESR to decouple any ripple voltage from the V_{LOOP} supply. Otherwise, the ripple voltage couples onto the 4-mA to 20-mA current source, and appears as noise across R_{LOAD} after the current-to-voltage conversion.

Additionally, stability concerns apply to the V_{REF} reference buffer when driving capacitive loads. 図 8-4 shows that two filtering capacitors are required, one C_{HF} of 10 pF to 0.5 µF and another C_{LF} of 2.2 µF to 22 µF. Either a series isolation resistance R_{ISO} or a snubber R_{COMP} is used, depending on application requirements.

If capacitive loading must be placed on the VREF pin, use one of the following compensation schemes to maintain stable operation. Values of capacitance must remain within the given ranges.



(1) Required compensation components.

図 8-4. Stable Operation With Capacitive Load on V_{REF}

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers*: TI Precision Labs introduction video on Current Loop Transmitters
- Texas Instruments, *TIPD190* 2-wire, 4-20mA Transmitter, EMC/EMI Tested Reference Design with the XTR116

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTR115U	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	XTR 115U
XTR115U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	XTR 115U
XTR115U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 115U
XTR115UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U A
XTR115UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U A
XTR116U	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	XTR 116U
XTR116U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	XTR 116U
XTR116U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 116U
XTR116UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	XTR 116U A
XTR116UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U A
XTR116UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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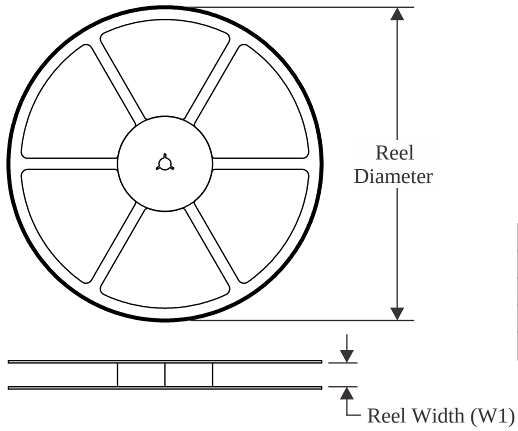
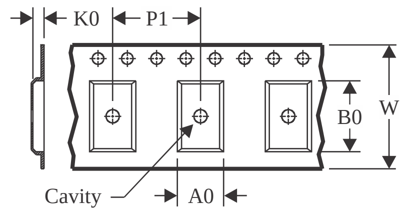
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

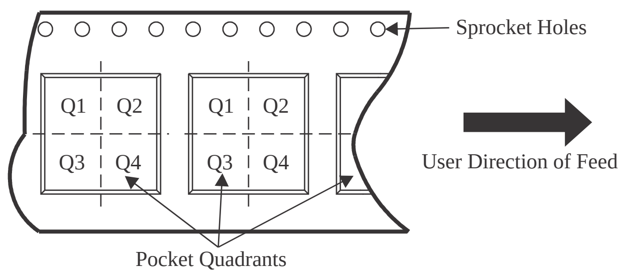


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

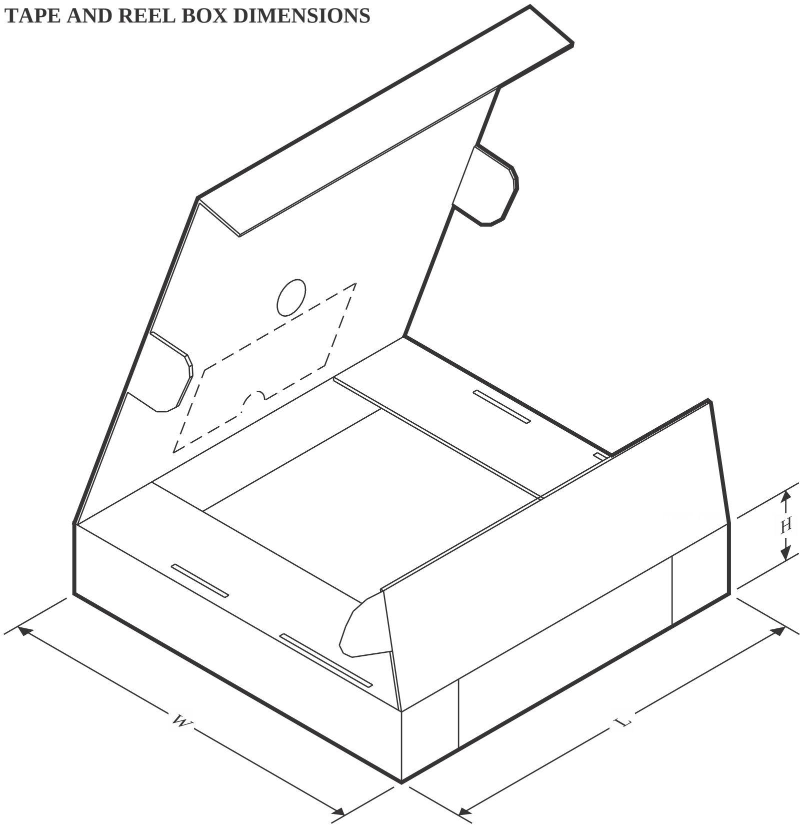
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

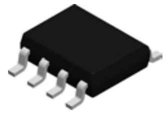
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR115U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

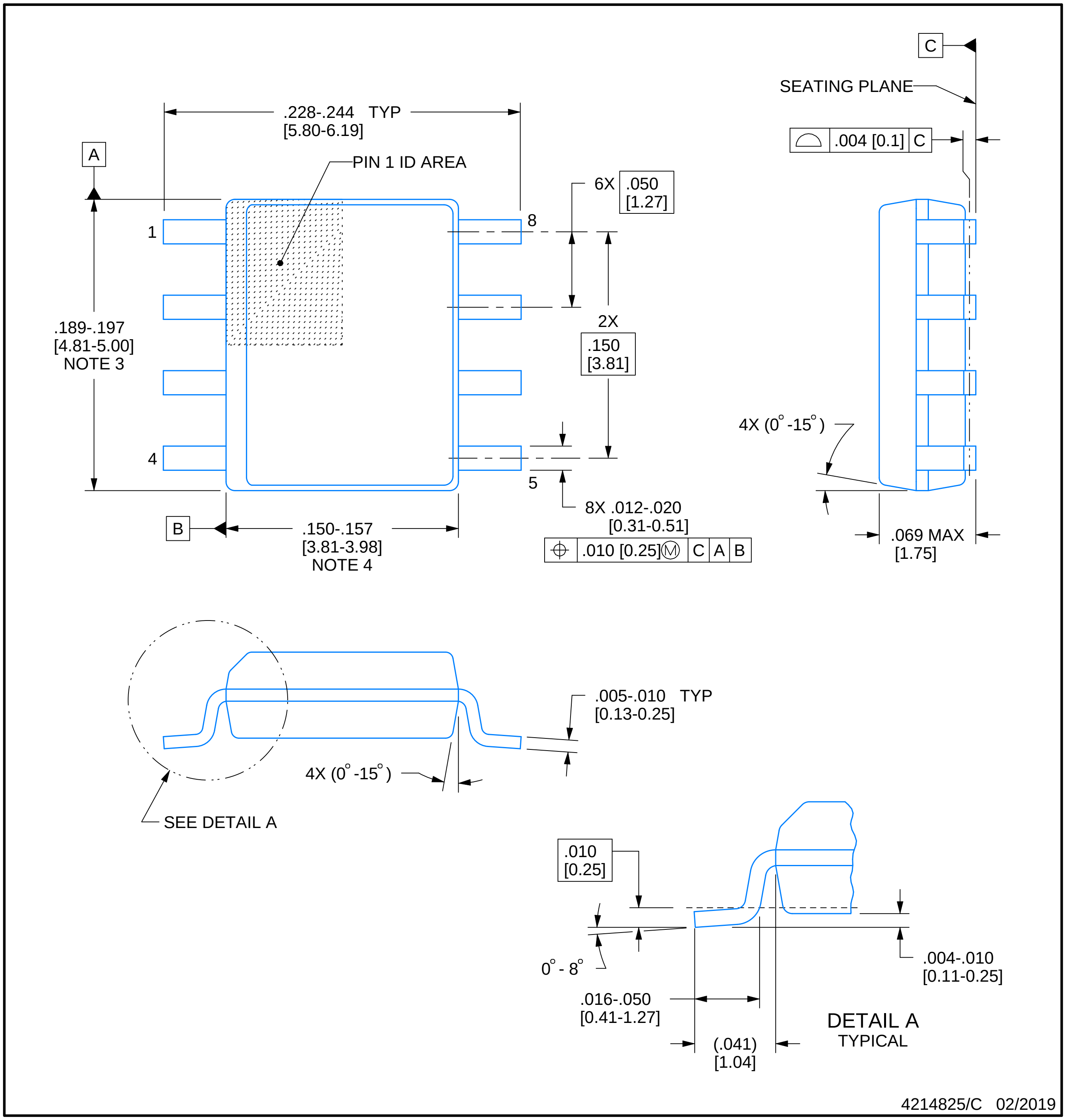
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR115U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR115UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR116U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR116UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0



D0008A

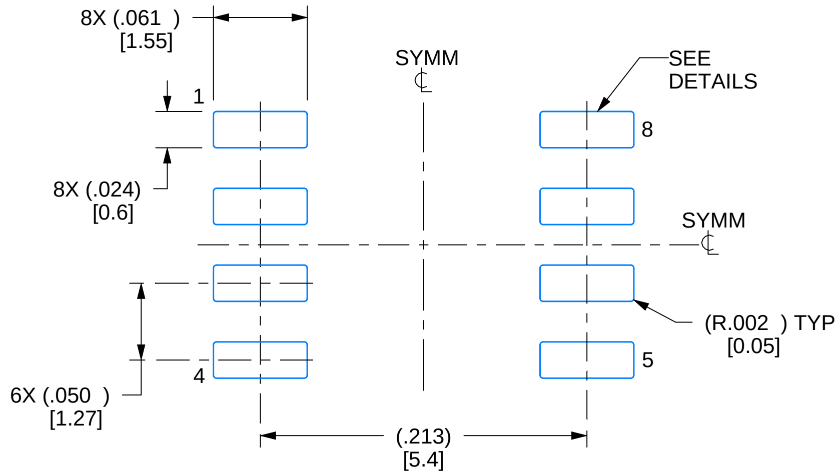
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

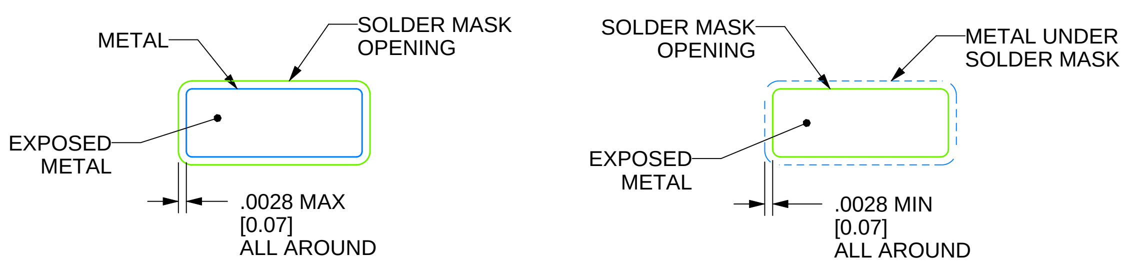


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

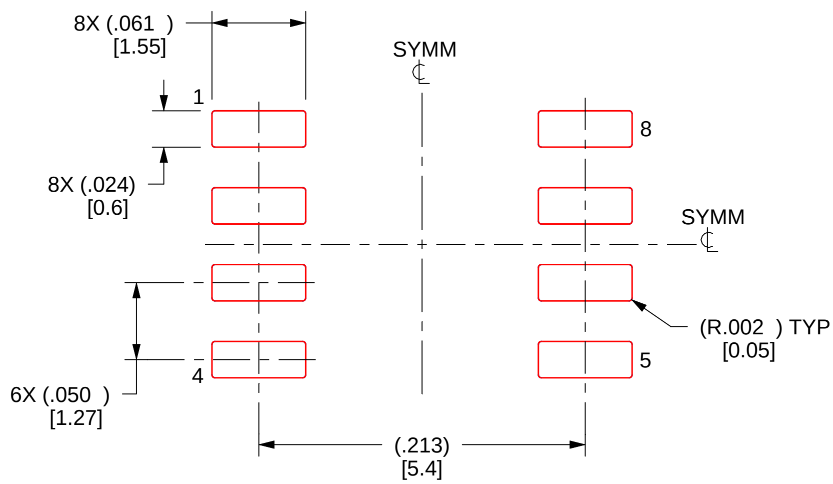
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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