参考資料

XTR106 4mA ～ 20mA 電流トランスミッター、センサ励起および線形化機能付き

1 特長

- 低い全体未調整誤差
- 2.5V、5V のブリッジ励起リファレンス
- 5.1V レギュレータ出力
- 低いスパン ドリフト：最大値 ±25ppm/°C
- 小さいオフセット ドリフト：0.25μV/°C
- 高い PSR：110dB 以上
- 高い CMR：86dB 以上
- 幅広い電源電圧範囲：7.5V～36V
- 14 ピン DIP および SOIC パッケージ オプション

2 アプリケーション

- フィールド トランスミッタとセンサ
- ファクトリ オートメーション
- HART モデムと互換
- 圧力 / 温度ブリッジ トランスミッター
- 産業用プロセス制御
- SCADA リモート データ アクイジション
- 計量システム
- ひずみゲージ トランスミッタ
- 加速度計

3 概要

XTR106 は、コストを最適化したブリッジ センサ アプリケーション用に設計されたモノリシック 4mA ～ 20mA への 2 線式電流トランスミッターです。このデバイスは包括的なブリッジ励起 (2.5V または 5V の基準電圧)、計測アンプ、センサの線形化、電流出力回路を提供します。追加の外部入力回路に電力を供給するための電流は、V_{REG} ピンから供給できます。

計装アンプは広いゲインで使用でき、さまざまな種類の入力信号に対応します。線形化ブリッジを含める電流トランスミッター全体の総合未調整誤差は十分に低く、多くのアプリケーションで調整なしに使用できます。XTR106 は、最低 7.5V のループ電源電圧で動作します。

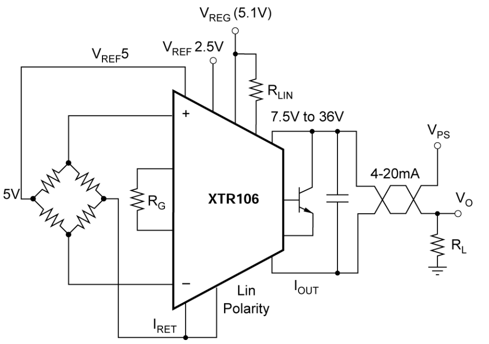
線形化回路は、ブリッジ励起電圧を制御することにより、伝達関数に 2 次補正を行います。このデバイスは、コスト最適化されたトランスデューサでも、非直線性が最大 20:1 改善されています。

XTR106 は 14 ピンのプラスチック DIP および SOIC 表面実装パッケージで供給され、-40℃ ～ +85℃ の温度範囲で動作が規定されています。このデバイスは、–40°℃ から +125°℃ の温度で動作します。

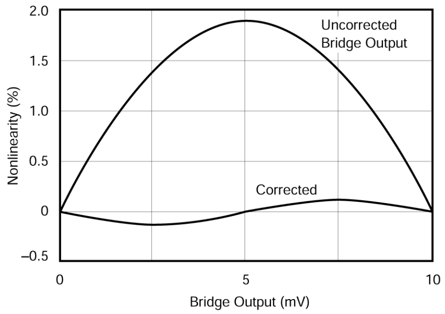
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
XTR106	D (SOIC、14)	8.65mm × 6mm
	N (PDIP、14)	19.3mm × 9.4mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



XTR106 を使用したブリッジの非直線性補正 回路図



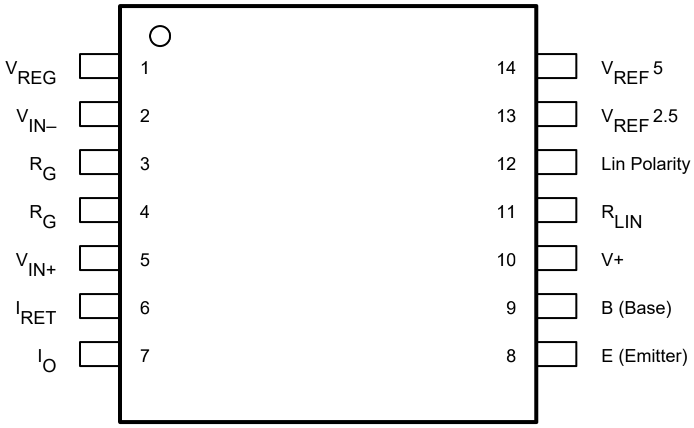
XTR106 ブリッジの非直線性補正

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

English Data Sheet: SBOS092

Table of Contents

4 Pin Configuration and Functions



Not to scale

図 4-1. D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
B (Base)	9	Output	Base connection for external transistor
E (Emitter)	8	Input	Emitter connection for external transistor
I_O	7	Output	Regulated 4mA to 20mA current loop output
I_{RET}	6	Input	*Local ground* return pin for V_{REG}, V_{REF}5, and V_{REF}2.5
Lin Polarity	12	Input	Linearity correction circuit polarity setting. Connect to I_{RET} to correct for positive nonlinearity, or connect to V_{REG} to correct for negative nonlinearity or if not using the linearity correction feature
R_G	3, 4	—	Input stage gain setting pins. The resistance R_G between pins 3 and 4 sets the gain of the voltage-to-current transfer function
R_{LIN}	11	—	Linearity correction resistor pin. The resistance R_{LIN} between pins 1 and 11 sets the corrective factor of the linearity correction circuit
V+	10	Power	Loop power supply
$V_{IN–}$	2	Input	Negative (inverting) differential voltage input
V_{IN+}	5	Input	Positive (noninverting) differential voltage input
V_{REF}5	14	Output	5V reference voltage output
V_{REF}2.5	13	Output	2.5V reference voltage output
V_{REG}	1	Output	5.1V regulator voltage output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V+	Power supply (referenced to IO pin)		40	V
	Input voltage, V_{IN+} or $V_{IN–}$ (referenced to IRET pin)	0	V+	V
	Output current limit		Continuous	
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		165	°C
T_{stg}	Storage temperature	–55	125	°C
	Lead temperature (soldering, 10s)		300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply (referenced to the I_O pin)	7.5	24	36	V
T_A	Specified temperature	−40		85	°C

5.3 Thermal Information

THERMAL METRICS(1)		XTR106		UNIT
		D (SOIC)	N (PDIP)	
		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.8	51.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.9	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.0	24.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.6	7.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.6	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

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5.4 Electrical Characteristics

at T_A = +25°C, V+ = 24V, and TIP29C external transistor (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT							
I_O	Output current equation				$I_O = V_{IN} \cdot (40/R_G) + 4mA$, V_{in} in Volts, R_G in Ω		A
	Output current, specified range			4		20	mA
I_{OVER}	Overscale limit			24	28	30	mA
I_{UNDER}	Underscale limit	$I_{REG} = 0$, $I_{REF} = 0$		1	1.6	2.2	mA
		$I_{REF} + I_{REG}$ = 2.5mA		2.9	3.4	4	
ZERO OUTPUT[1] (V_{IN} = 0V, R_G = ∞)							
I_{ZERO}	Zero output				4		mA
	Initial error	XTR106P, XTR106U			±5	±25	µA
		XTR106PA, XTR106UA			±5	±50	
	vs temperature	T_A = −40°C to +85°C			±0.07	±0.9	µA/°C
	vs supply voltage, V+	V+ = 7.5V to 36V			0.04	0.2	µA/V
	vs common-mode voltage (CMRR)	V_{CM} = 1.1V to 3.5V[5]			0.02		µA/V
	vs V_{REG} (I_O)				0.8		µA/mA
i_n	Noise: 0.1Hz to 10Hz				0.035		µAp-p
SPAN							
S	Span equation (transconductance)				$S = 40/R_G$		A/V
	Untrimmed error	Full scale (V_{IN}) = 50mV	XTR106P, XTR106U		±0.05	±0.2	%
			XTR106PA, XTR106UA		±0.05	±0.4	
	vs temperature [2]	T_A = −40°C to +85°C			±3	±25	ppm/°C
	Nonlinearity: ideal input[3]	Full scale (V_{IN}) = 50mV			±0.001	±0.01	%
INPUT[4]							
V_{OS}	Offset voltage	V_{CM} = 2.5V	XTR106P, XTR106U		±50	±100	µV
			XTR106PA, XTR106UA		±50	±250	
	vs temperature	T_A = −40°C to +85°C	XTR106P, XTR106U		±0.25	±1.5	µV/°C
			XTR106PA, XTR106UA		±0.25	±3	
	vs supply voltage, V+	V+ = 7.5V to 36V			±0.1	±3	µV/V
CMRR	vs common-mode voltage, RTI	V_{CM} = 1.1V to 3.5V[5]	XTR106P, XTR106U		±10	±50	µV/V
			XTR106PA, XTR106UA		±10	±100	
V_{CM}	Common-mode range[5]			1.1		3.5	V
I_B	Input bias current	XTR106P, XTR106U			5	25	nA
		XTR106PA, XTR106UA			5	50	
	vs temperature	T_A = −40°C to +85°C			20		pA/°C
I_{OS}	Input offset current	XTR106P, XTR106U			±0.2	±3	nA
		XTR106PA, XTR106UA			±0.2	±10	
	vs temperature	T_A = −40°C to +85°C			5		pA/°C
Z_{IN}	Impedance: differential				0.1 || 1		GΩ || pF
	Common-mode				5 || 10		GΩ || pF
V_n	Noise: 0.1Hz to 10Hz				0.6		µVp-p

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5.4 Electrical Characteristics (続き)

at T_A = +25°C, V+ = 24V, and TIP29C external transistor (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
VOLTAGE REFERENCES[5] **(Lin Polarity Connected to V_{REG}, R_{LIN} = 0)**							
V_{REF}2.5	Initial: 2.5V reference				2.5		V
V_{REF}5	5V reference				5		V
	Accuracy	V_{REF} = 2.5V or 5V	XTR106P, XTR106U		±0.05	±0.25	%
			XTR106PA, XTR106UA		±0.05	±0.5	
	vs temperature[6]	T_A = −40°C to +85°C	XTR106P, XTR106U		±20	±35	ppm/°C
			XTR106PA, XTR106UA		±20	±75	
	vs supply voltage, V+	V+ = 7.5V to 36V			±5	±20	ppm/V
	vs load	I_{REF} = 0mA to 2.5mA			60		ppm/mA
	Noise: 0.1Hz to 10Hz				10		μVp-p
V_{REG} [5]							
	V_{REG}				5.1		V
	Accuracy				±0.02	±0.1	V
	vs temperature	T_A = −40°C to +85°C			±0.5		mV/°C
	vs supply voltage, V+	V+ = 7.5V to 36V			1		mV/V
I_{REG}	Output current				See Typical Curves		mA
	Output impedance	I_{REG} = 0mA to 2.5mA			80		Ω
LINEARIZATION[7]							
R_{LIN}	R_{LIN} (external) equation				RLIN = KLIN • (4B/(1−2B)), K_{LIN} in Ω, B is nonlinearity relative to V_{FS}		Ω
K_{LIN}	K_{LIN} linearization factor	V_{REF} = 5V			6.645		kΩ
		V_{REF} = 2.5V			9.905		kΩ
	Accuracy				±1	±5	%
	vs Temperature	T_A = −40°C to +85°C			±50	±100	ppm/°C
B	Maximum correctable sensor nonlinearity	V_{REF} = 5V			±5		% of V_{FS}
		V_{REF} = 2.5V			−2.5, +5		% of V_{FS}

(1) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero.
(2) Does not include initial error or TCR of gain-setting resistor, R_G.
(3) Increasing the full-scale input range improves nonlinearity.
(4) Does not include zero output initial error.
(5) Voltage measured with respect to I_{RET} pin.
(6) Calculated using the box method: $(MAX_{(-40°C\ to\ 85°C)} - MIN_{(-40°C\ to\ 85°C)}) / MIN_{(-40°C\ to\ 85°C)} / (85°C - (-40°C))$.
(7) See also セクション 6.3.1. V_{FS} = full-scale V_{IN}.

5.5 Typical Characteristics

at T_A = +25°C, V+ = 24V (unless otherwise noted)

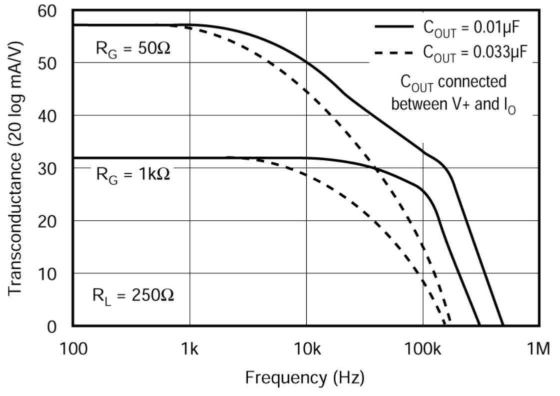

図 5-1. Transconductance vs Frequency

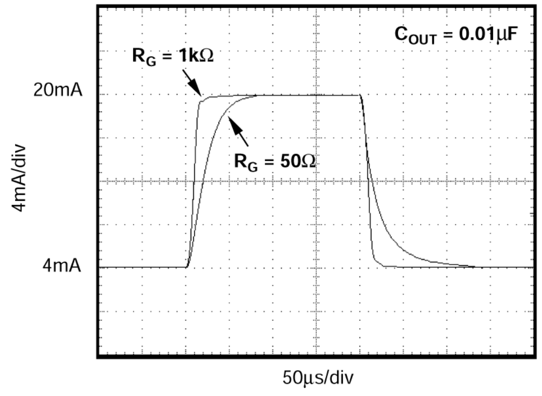

図 5-2. Step Response

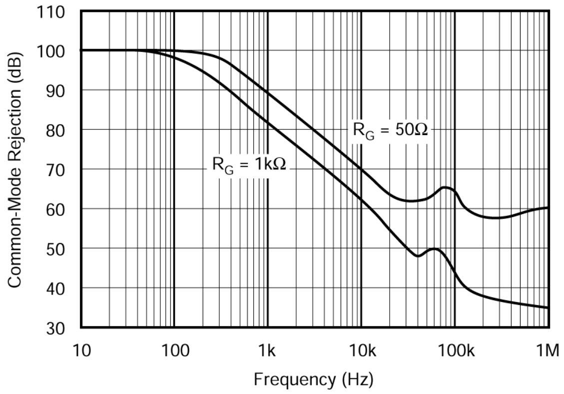

図 5-3. Common-Mode Rejection vs Frequency

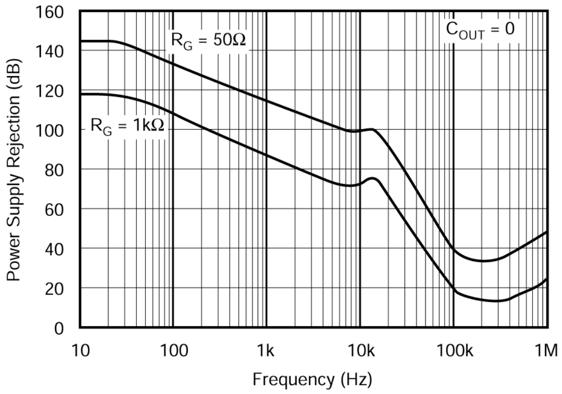

図 5-4. Power Supply Rejection vs Frequency

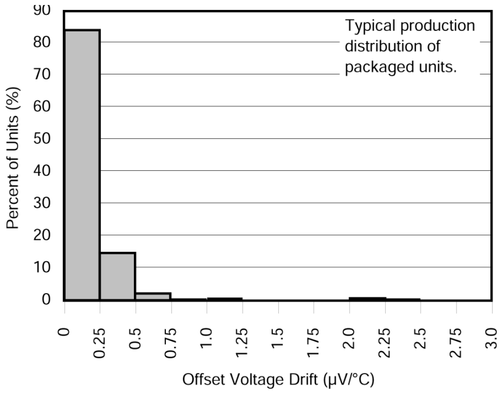

図 5-5. Input Offset Voltage Drift Production Distribution

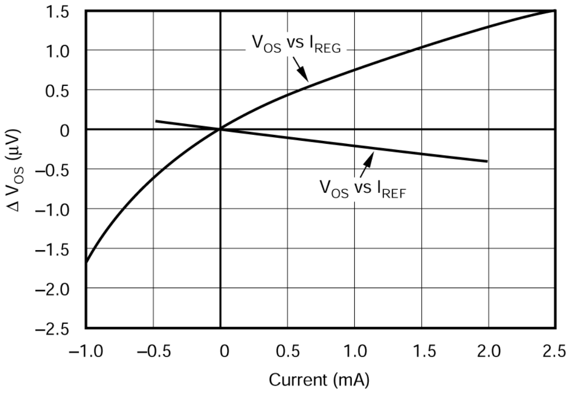

図 5-6. Input Offset Voltage Change vs V_{REG} And V_{REF} Currents

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5.5 Typical Characteristics (continued)

at T_A = +25°C, V+ = 24V (unless otherwise noted)

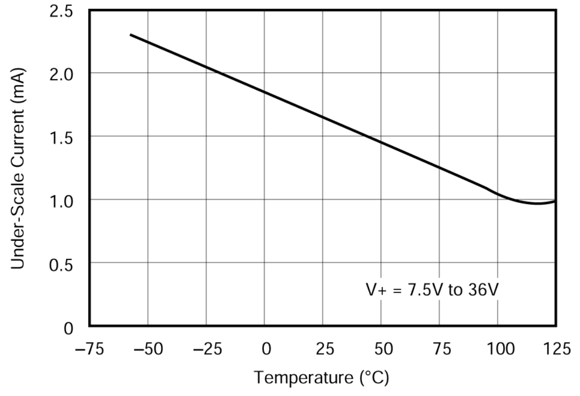

図 5-7. Underscale Current vs Temperature

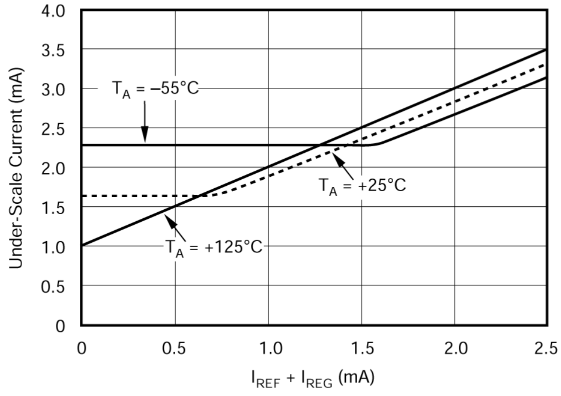

図 5-8. Underscale Current vs I_{REF} + I_{REG}

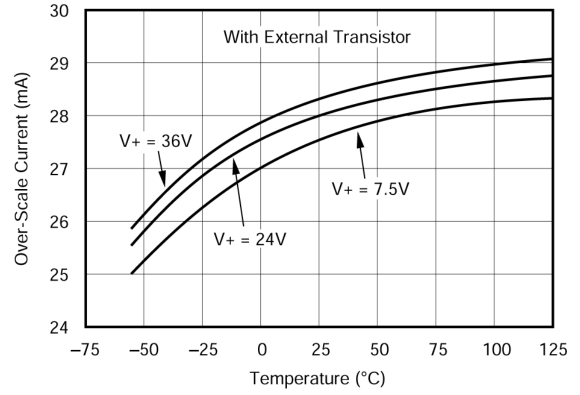

図 5-9. Overscale Current vs Temperature

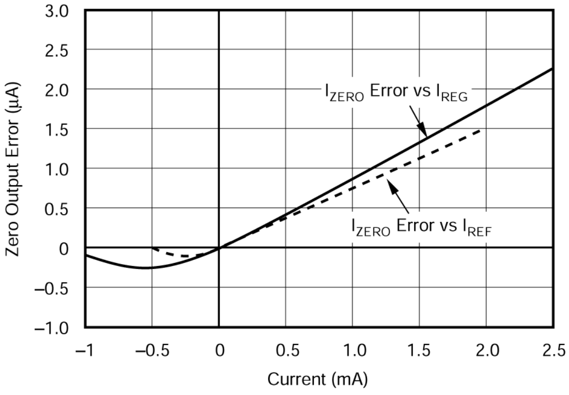

図 5-10. Zero Output Error vs V_{REF} and V_{REG} Currents

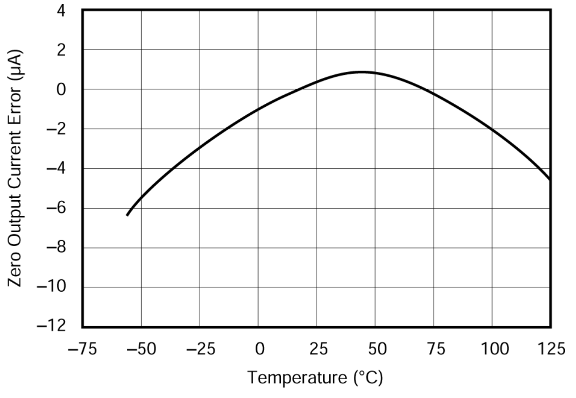

図 5-11. Zero Output Current Error vs Temperature

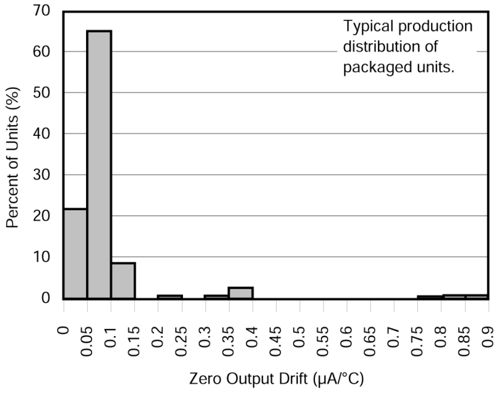

図 5-12. Zero Output Drift Production Distribution

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5.5 Typical Characteristics (continued)

at T_A = +25°C, V+ = 24V (unless otherwise noted)

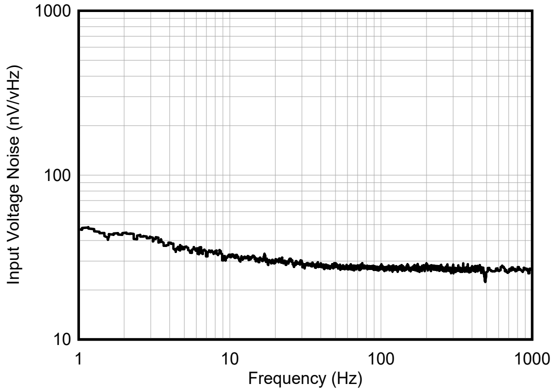


図 5-13. Input Voltage Noise Density vs Frequency

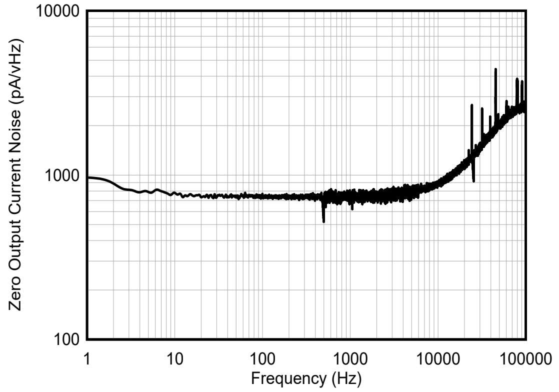


図 5-14. Zero Output Current Noise Density vs Frequency

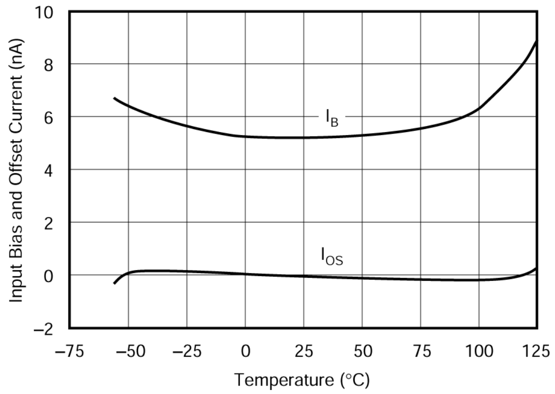


図 5-15. Input Bias and Offset Current vs Temperature

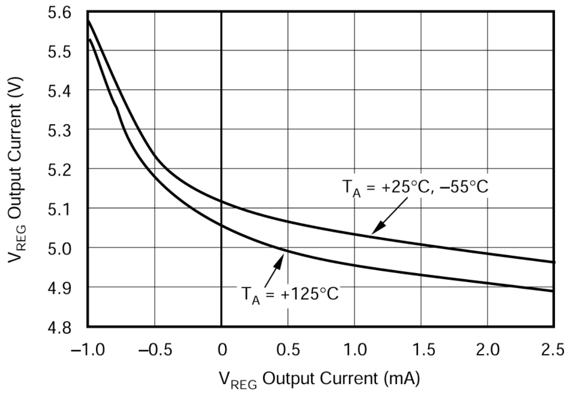


図 5-16. V_{REG} Output Voltage vs V_{REG} Output Current

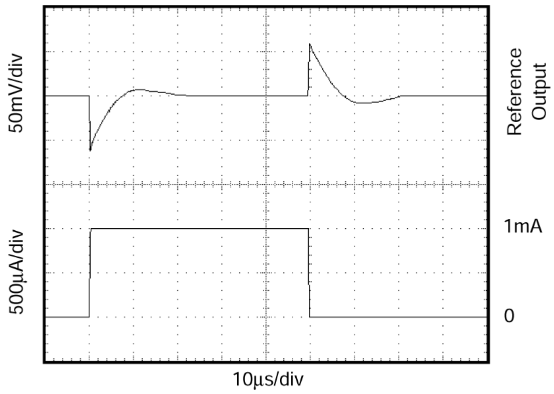


図 5-17. $V_{REF}5$ Reference Transient Response

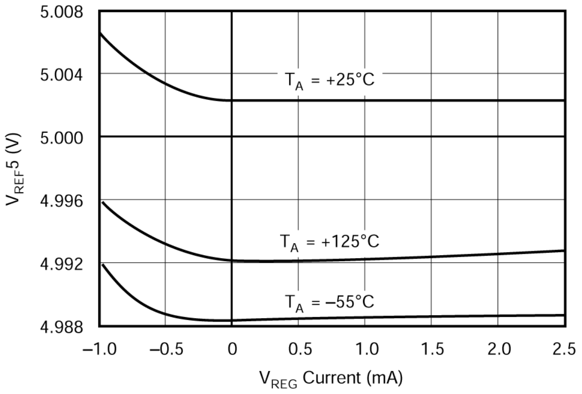


図 5-18. $V_{REF}5$ vs V_{REG} Output Current

5.5 Typical Characteristics (continued)

at T_A = +25°C, V+ = 24V (unless otherwise noted)

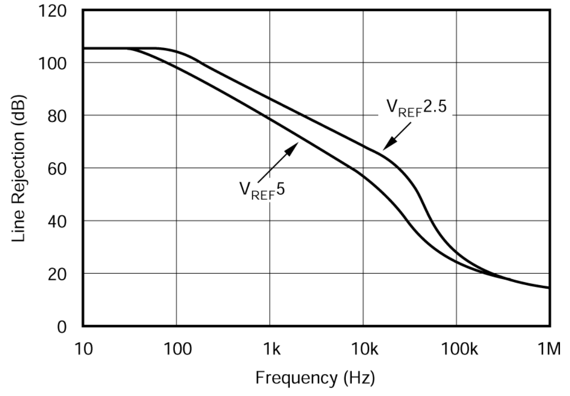


図 5-19. Reference AC Line Rejection vs Frequency

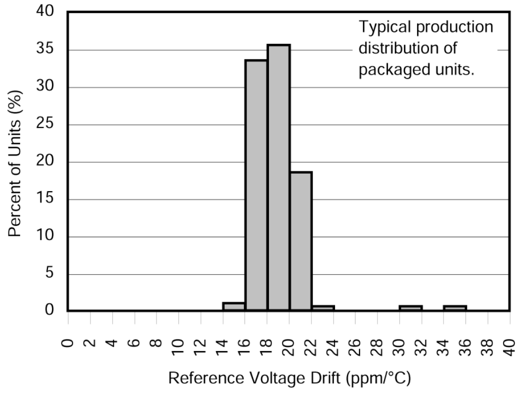


図 5-20. Reference Voltage Drift Production Distribution

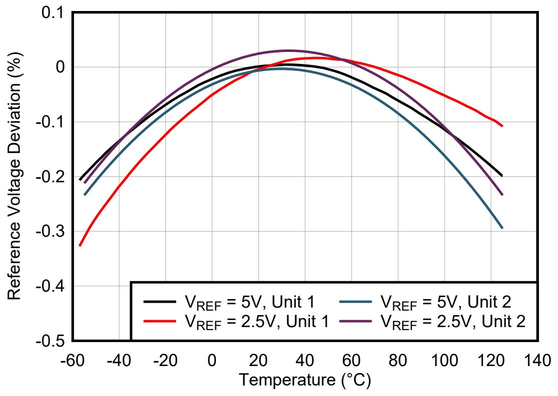


図 5-21. Reference Voltage Deviation vs Temperature

6 Detailed Description

6.1 Overview

The XTR106 is a monolithic 4mA-to-20mA, 2-wire current transmitter with a differential voltage input. 図 6-1 shows the simplified schematic of the XTR106. The loop power supply, V+, provides power for all circuitry. The output loop current is modulated by the XTR106 and is typically measured as a voltage across a series load resistor (R_L).

The instrumentation amplifier input of the XTR106 measures the voltage difference between the noninverting and inverting inputs. This difference is then gained up according to the value of R_G, and expressed as a regulated current output.

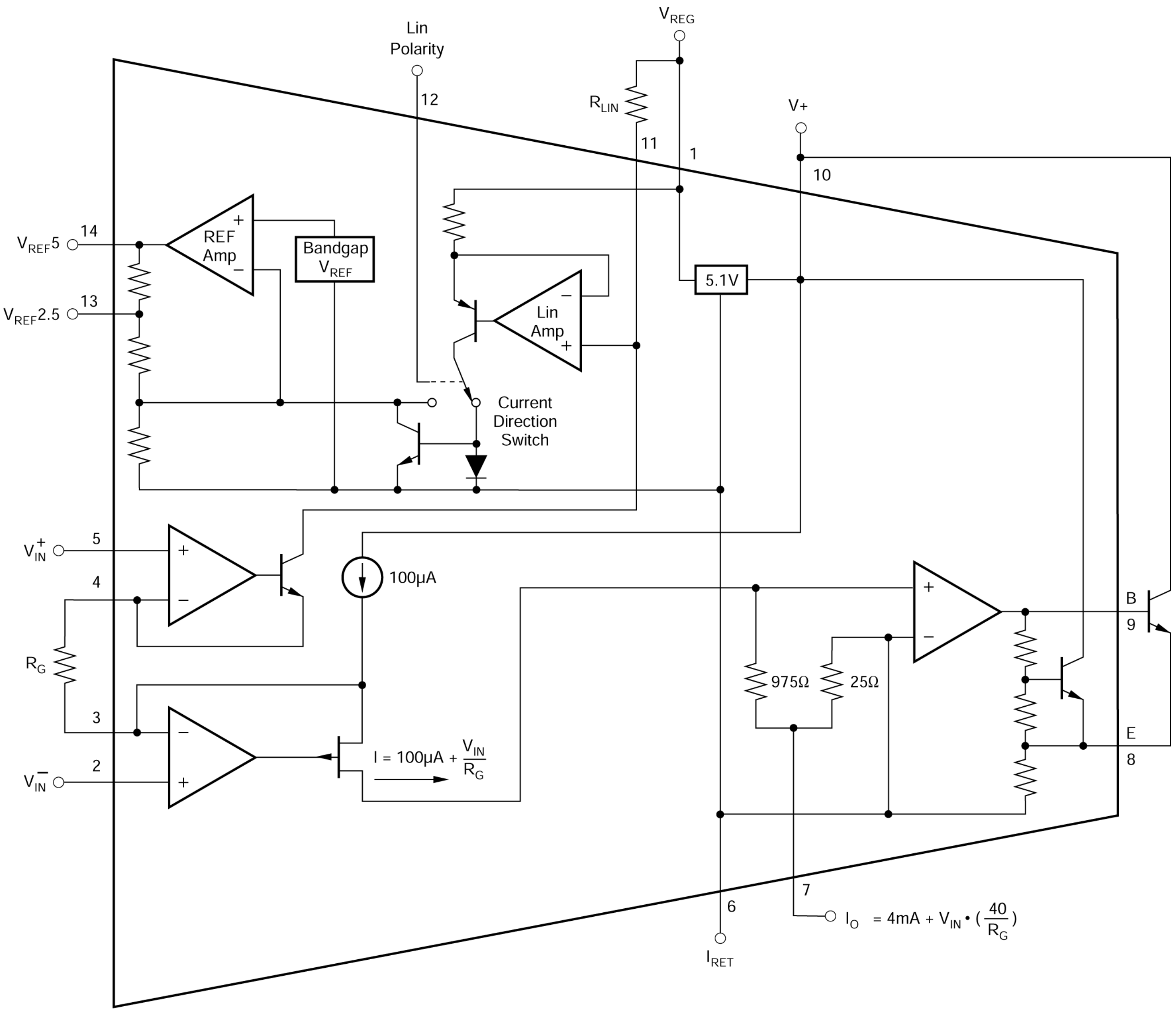
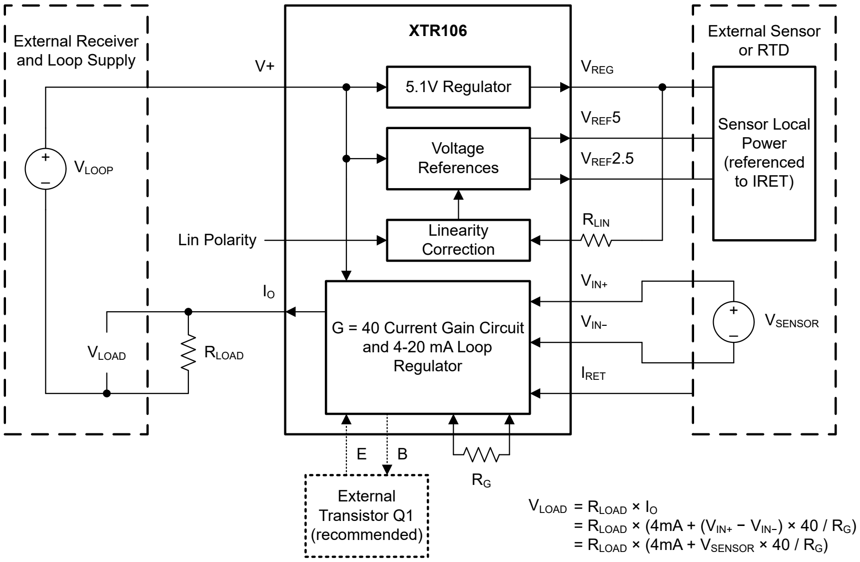


図 6-1. Simplified Schematic

6.2 Functional Block Diagram



$$\begin{aligned} V_{LOAD} &= R_{LOAD} \times I_O \\ &= R_{LOAD} \times (4mA + (V_{IN+} - V_{IN-}) \times 40 / R_G) \\ &= R_{LOAD} \times (4mA + V_{SENSOR} \times 40 / R_G) \end{aligned}$$

6.3 Feature Description

6.3.1 Linearization

Many bridge sensors are inherently nonlinear. With the addition of one external resistor, compensating for parabolic nonlinearity with up to a 20:1 improvement over an uncompensated bridge output is possible.

Linearity correction is accomplished by varying the bridge excitation voltage. Signal-dependent variation of the bridge excitation voltage adds a second-order term to the overall transfer function (including the bridge). This configuration can be tailored to correct for bridge sensor nonlinearity.

Either positive or negative bridge nonlinearity errors can be compensated by proper connection of the Lin Polarity pin. To correct for positive bridge nonlinearity (upward bowing), connect Lin Polarity (pin 12) to I_{RET} (pin 6); see also 図 6-2. This correction causes V_{REF} to increase with bridge output, which compensates for a positive bow in the bridge response. To correct negative nonlinearity (downward bowing), connect Lin Polarity to V_{REG} (pin 1); see also 図 6-3. This correction causes V_{REF} to decrease with bridge output. The Lin Polarity pin is a high-impedance node.

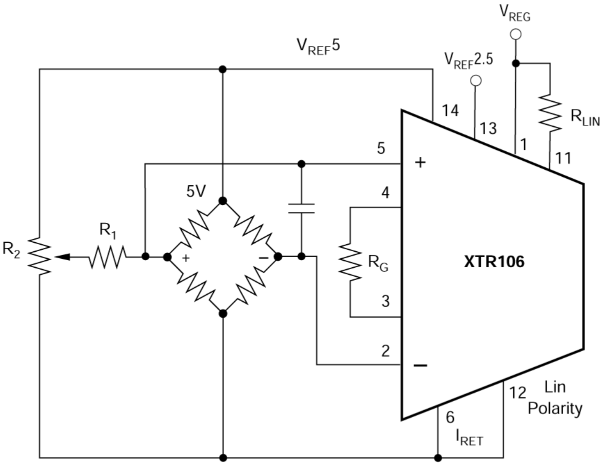


図 6-2. Connection for Positive Bridge Nonlinearity, V_{REF} = 5V

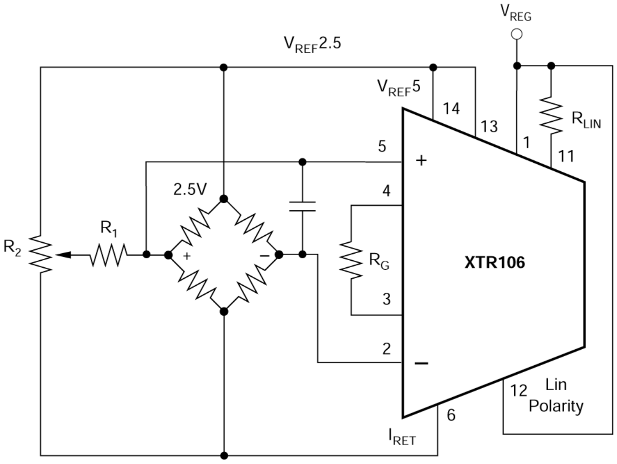


図 6-3. Connection for Negative Bridge Nonlinearity, V_{REF} = 2.5V

If no linearity correction is desired, connect both the R_{LIN} and Lin Polarity pins to V_{REG} (see also 図 6-4). This connection results in a constant reference voltage independent of input signal.

注

Do not leave the R_{LIN} or Lin Polarity pins open or connected to another potential.

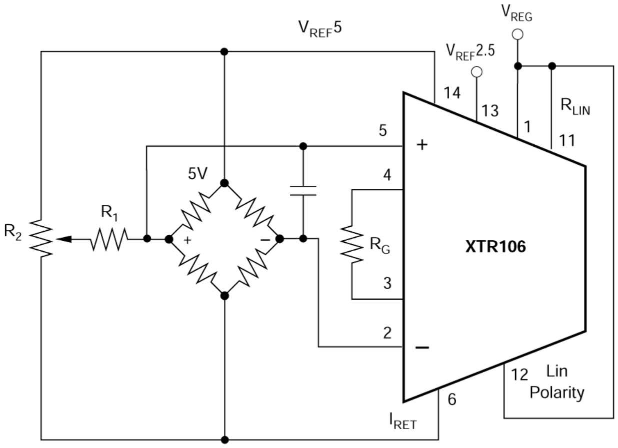


図 6-4. Connection if No Linearity Correction is Desired, V_{REF} = 5V

R_{LIN} is the external linearization resistor and is connected between pin 11 and pin 1 (V_{REG}); see also 図 6-2 and 図 6-3. To determine the value of R_{LIN}, the nonlinearity of the bridge sensor with constant excitation voltage must be known. The XTR106 linearity circuitry can only compensate for the parabolic-shaped portions of a sensor nonlinearity. Optimized correction occurs when maximum deviation from linear output occurs at midscale (see 図 7-3 and 図 7-4). Sensors with nonlinearity curves similar to that shown in 図 7-3 and 図 7-4, but not peaking exactly at midscale can be substantially improved.

A sensor with an S-shaped nonlinearity curve (equal positive and negative nonlinearity) cannot be improved with the XTR106 correction circuitry. The value of R_{LIN} is chosen according to 式 1. R_{LIN} depends on a linearization factor, K_{LIN}, which differs for the 2.5V reference and 5V reference. The sensor nonlinearity term, B (relative to full scale), is positive or negative depending on the direction of the bow.

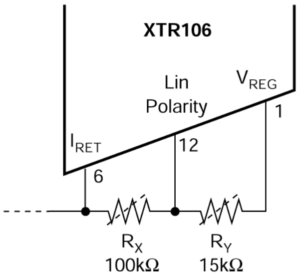
Linearization resistor:

$$R_{LIN} = \left| K_{LIN} \times \frac{4B}{1 - 2B} \right| \tag{1}$$

where:

- K_{LIN} is the linearization factor (in Ω)
- K_{LIN} is 9905Ω for the 2.5V reference
- K_{LIN} is 6645Ω for the 5V reference
- B is the sensor nonlinearity relative to V_{FS} (for –2.5% nonlinearity, B = –0.025)
- V_{FS} is the full-scale bridge output without linearization (in V)

A maximum ±5% nonlinearity can be corrected when the 5V reference is used. Sensor nonlinearity of +5%/–2.5% can be corrected with 2.5V excitation. The trim circuit shown in 図 6-5 can be used for bridges with unknown bridge nonlinearity polarity.



Open R_X for negative bridge nonlinearity
Open R_Y for positive bridge nonlinearity

図 6-5. Onboard Resistor Circuit for Unknown Bridge Nonlinearity Polarity

Gain is affected by the varying excitation voltage used to correct bridge nonlinearity. The corrected value of the gain resistor is calculated from 式 2.

Gain-set resistor:

$$R_G = \frac{V_{FS}}{400\mu A} \times \frac{1 + 2B}{1 - 2B} \tag{2}$$

where:

- V_{FS} is the full-scale bridge output without linearization (in V)

When using linearity correction, keep the sensor output common-mode voltage within the XTR106 allowable input range of 1.1V to 3.5V. 式 3 can be used to calculate the XTR106 new excitation voltage. The common-mode voltage of the bridge output is simply half this value if no common-mode resistor is used (see also the examples in 図 6-2 and 図 6-3). Exceeding the common-mode range can yield unpredictable results.

Adjusted excitation voltage at full-scale output:

$$V_{REF\ (Adj)} = V_{REF\ (Initial)} \times \frac{1 + 2B}{1 - 2B} \tag{3}$$

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For high-precision applications (errors < 1%), a two-step calibration process can be employed. First, the nonlinearity of the sensor bridge is measured with the initial gain resistor and R_{LIN} = 0 (R_{LIN} pin connected directly to V_{REG}). Using the resulting sensor nonlinearity, B, values for R_G and R_{LIN} are calculated using 式 1 and 式 2. A second calibration measurement is then taken to adjust R_G to account for the offsets and mismatches in the linearization.

Example:

Calculate R_{LIN} and the resulting R_G for a bridge sensor with 2.5% downward bow nonlinearity relative to V_{FS} and determine if the input common-mode range is valid.

For V_{REF} = 2.5V and V_{FS} = 50mV

For a 2.5% downward bow, B = –0.025 (Lin Polarity pin connected to V_{REG})

For V_{REF} = 2.5V, K_{LIN} = 9905Ω

$$R_{LIN} = \left| \frac{(9905\Omega)(4)(-0.025)}{1-(2)(-0.025)} \right| = 943\Omega \tag{4}$$

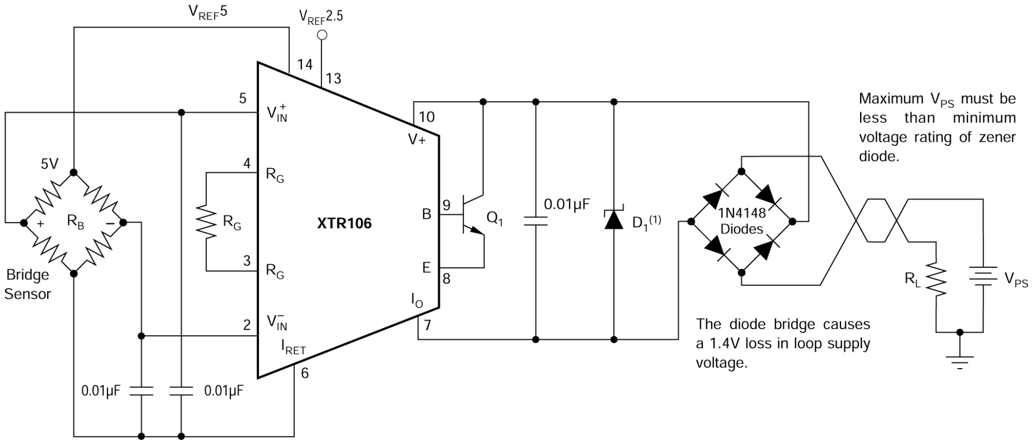
$$R_G = \frac{0.05V}{400\mu A} \times \frac{1+(2)(-0.025)}{1-(2)(-0.025)} = 113\Omega \tag{5}$$

$$V_{CM} = \frac{V_{REF\ (Adj)}}{2} = \frac{1}{2} \times 2.5V \times \frac{1+(2)(-0.025)}{1-(2)(-0.025)} = 1.13V \tag{6}$$

which falls within the 1.1V to 3.5V input common-mode range.

6.3.2 Reverse-Voltage Protection

The XTR106 low compliance rating (7.5V) permits the use of various voltage protection methods without compromising operating range. 図 6-6 shows a diode bridge circuit which allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop-supply voltage. This results in a compliance voltage of approximately 9V—satisfactory for most applications. If a 1.4V drop in loop supply is too much, a diode can be inserted in series with the loop supply voltage and the V+ pin, as shown in 図 7-6. This protects against reverse output connection lines with only a 0.7V loss in loop-supply voltage.



Maximum V_{PS} must be less than minimum voltage rating of zener diode.

The diode bridge causes a 1.4V loss in loop supply voltage.

(1) 36V Zener diode, such as 1N4753A or P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages < 30V for increased protection.

図 6-6. Reverse-Voltage Operation and Overvoltage Surge Protection

6.3.3 Overvoltage Surge Protection

Remote connections to current transmitters are sometimes subjected to voltage surges. Limit the maximum surge voltage applied to the XTR106 to the lowest practical value. Various Zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36V protection diode maintains proper transmitter operation at normal loop voltages, yet provides an appropriate level of protection against voltage surges. The XTR106 is specified to an absolute maximum loop voltage of 40V.

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry, if the loop connections are reversed. If a surge protection diode is used, use a series diode or diode bridge for protection against reversed connections.

6.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

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7 Application and Implementation

注

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7.1 Application Information

図 7-1 shows the basic connection diagram for the XTR106. The loop power supply, V_{PS}, provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L. A 0.01μF to 0.03μF supply bypass capacitor connected between V+ and I_O is recommended. For applications where fault, overload conditions, or both can saturate the inputs, a 0.03μF capacitor is recommended.

A 2.5V or 5V reference is available to excite a bridge sensor. For 5V excitation, connect pin 14 ($V_{REF}5$) to the bridge; see also 図 7-1. For 2.5V excitation, connect pin 13 ($V_{REF}2.5$) to pin 14; see also 図 6-3. The output terminals of the bridge are connected to the instrumentation amplifier inputs, V_{IN+} and V_{IN-}. A 0.01μF capacitor is shown connected between the inputs and is recommended for high impedance bridges (> 10kΩ). The resistor R_G sets the gain of the instrumentation amplifier as required by the full-scale bridge voltage, V_{FS}.

Lin Polarity and R_{LIN} provide second-order linearization correction to the bridge, achieving up to a 20:1 improvement in linearity. Connections to Lin Polarity (pin 12) determine the polarity of nonlinearity correction; connect either to I_{RET} or V_{REG}. Connect Lin Polarity to V_{REG} even if linearity correction is not desired. R_{LIN} is chosen according to 式 7 and depends on K_{LIN} (linearization constant) and the bridge nonlinearity relative to V_{FS} (see セクション 6.3.1).

$$R_{LIN} = \left|K_{LIN} \times \frac{4B}{1-2B}\right| \tag{7}$$

where:

- K_{LIN} is in Ω

$$R_G = \left(\frac{V_{FS}}{400\mu A}\right) \times \frac{1+2B}{1-2B} \tag{8}$$

where:

- V_{FS} is in V
- K_{LIN} = 9.905kΩ for 2.5V reference
- K_{LIN} = 6.645kΩ for 5V reference
- B is the bridge nonlinearity relative to V_{FS}
- V_{FS} is the full-scale input voltage

The transfer function for the complete current transmitter is:

$$I_O = 4mA + V_{IN} \times \left(\frac{40}{R_G}\right) \tag{9}$$

Where:

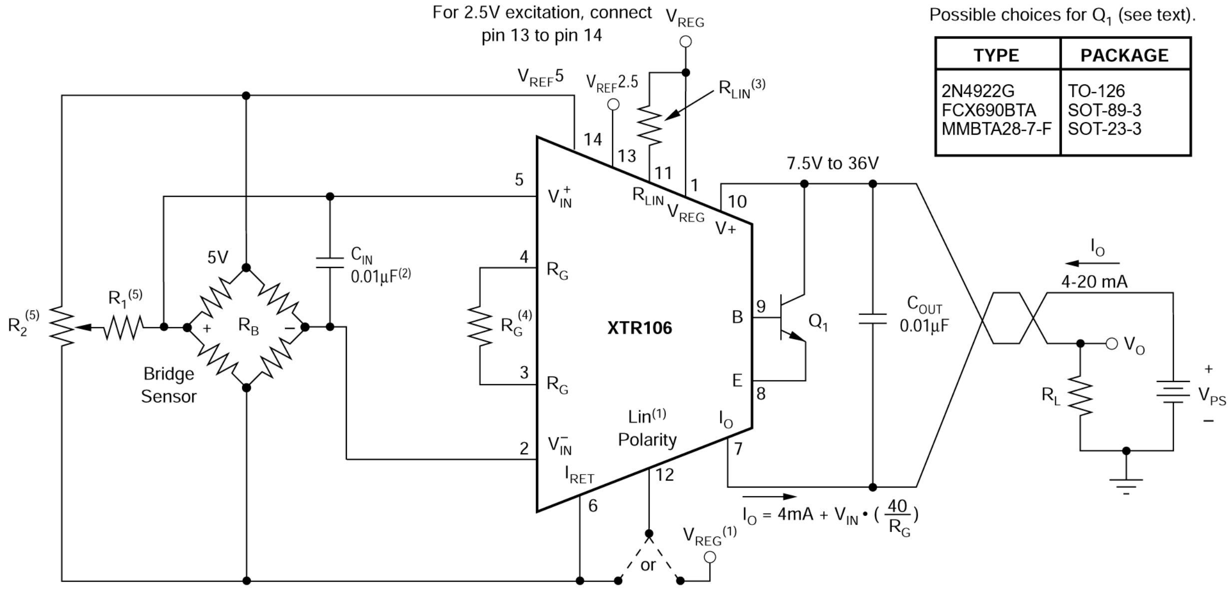
- V_{IN} V_{IN} is the differential input voltage in Volts
- R_G is in Ohms

As evident from the transfer function, if no R_G is used ($R_G = \infty$), the gain is zero and the output is simply the XTR106 zero current.

A negative input voltage, V_{IN}, causes the output current to be less than 4mA. Increasingly negative V_{IN} causes the output current to limit at approximately 1.6mA. If current is being sourced from the reference and/or V_{REG}, the current limit value can increase. See also 図 5-7 and 図 5-8.

Increasingly positive input voltage (greater than the full-scale input, V_{FS}) produces increasing output current according to the transfer function, up to the output current limit of approximately 28mA. See also 図 5-9.

The I_{RET} pin is the return path for all current from the references and V_{REG}. I_{RET} also serves as a local ground and is the reference point for V_{REG} and the onboard voltage references. The I_{RET} pin allows any current used in external circuitry to be sensed by the XTR106 and to be included in the output current without causing error. The input voltage range of the XTR106 is referred to this pin.



Possible choices for Q_1 (see text).

TYPE	PACKAGE
2N4922G	TO-126
FCX690BTA	SOT-89-3
MMBTA28-7-F	SOT-23-3

(1) Connect Lin Polarity (pin 12) to I_{RET} (pin 6) to correct for positive bridge nonlinearity or connect to V_{REG} (pin 1) for negative bridge nonlinearity. The R_{LIN} pin and Lin Polarity pin must be connected to V_{REG} if linearity correction is not desired. Refer to the *Linerization* section.

(2) Recommended for bridge impedances > 10kΩ.

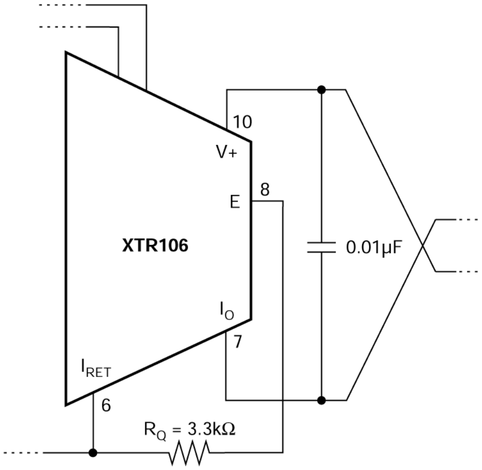
(3) R_1 and R_2 form bridge trim circuit to compensate for the initial accuracy of the bridge. See the *Bridge Balance* text.

図 7-1. Basic Bridge Measurement Circuit With Linearization

7.1.1 External Transistor

External pass transistor, Q_1, conducts the majority of the signal-dependent 4mA-to-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR106, maintaining excellent accuracy.

The external transistor is inside a feedback loop; therefore, the characteristics are not critical. Requirements are: V_{CEO} = 45V min, β = 40 min and P_D = 800mW. Power dissipation requirements can be lower if the loop power supply voltage is less than 36V. Some possible choices for Q_1 are listed in 図 7-1. The XTR106 can be operated without an external pass transistor. Accuracy, however, is somewhat degraded as a result of the internal power dissipation and subsequent self-heating. Operation without Q_1 is not recommended for extended temperature ranges. A resistor (R = 3.3kΩ) connected between the I_{RET} pin and the E (emitter) pin is advised for operation less than 0°C without Q_1 to maintain the full 20mA full-scale output, especially with V+ near 7.5V.



(1) For operation without external transistor, connect a 3.3kΩ resistor between pin 6 and pin 8. See text for discussion of performance.

図 7-2. Operation Without an External Transistor

7.1.2 Loop Power Supply

The voltage applied to the XTR106, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 7.5V to 36V. The loop-supply voltage, V_{PS}, differs from the voltage applied to the XTR106 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop-supply voltage is used, R_L (including the loop wiring resistance) must be made a relatively low value so that V+ remains 7.5V or greater for the maximum loop current of 20mA:

$$R_{L\,MAX} = \left(\frac{(V+) - 7.5V}{20mA}\right) - R_{WIRING} \tag{10}$$

For loop currents up to 30mA, design for V+ equal or greater than 7.5V to allow for out-of-range input conditions. V+ must be at least 8V if 5V sensor excitation is used and if correcting for bridge nonlinearity greater than +3%.

The low operating voltage (7.5V) of the XTR106 allows operation directly from personal computer power supplies (12V ±5%). When used with the RCV420 Current Loop Receiver (図 7-6), load resistor voltage drop is limited to 3V.

7.1.3 Bridge Balance

図 7-1 shows a bridge trim circuit (R_1, R_2). This adjustment can be used to compensate for the initial accuracy of the bridge, to trim the offset voltage of the XTR106, or both. The values of R_1 and R_2 depend on the impedance of the bridge, and the trim range required. This trim circuit places an additional load on the V_{REF} output. Be sure the additional load on V_{REF} does not affect zero output. See 図 5-8. The effective load of the trim circuit is nearly equal to R_2. An approximate value for R_1 can be calculated:

$$R_1 \approx \frac{5V \times R_B}{4 \times V_{TRIM}} \tag{11}$$

Where:

- R_B is the resistance of the bridge
- V_{TRIM} is the desired ±voltage trim range (in V)

Make R_2 equal or lower in value to R_1.

7.1.4 Underscale Current

The total current being drawn from the V_{REF} and V_{REG} voltage sources, as well as temperature, affect the XTR106 underscale current value (see 図 5-8). Consider this when choosing the bridge resistance and excitation voltage, especially for transducers operating over a wide temperature range (see 図 5-7).

7.1.5 Low-Impedance Bridges

The XTR106 two available excitation voltages (2.5V and 5V) allow the use of a wide variety of bridge values. Bridge impedances as low as 1kΩ can be used without any additional circuitry. Lower impedance bridges can be used with the XTR106 by adding a series resistance to limit excitation current to ≤ 2.5mA (図 7-5). Add resistance to the upper and lower sides of the bridge to keep the bridge output within the 1.1V to 3.5V common-mode input range. Bridge output is reduced so a preamplifier can be needed to reduce offset voltage and drift.

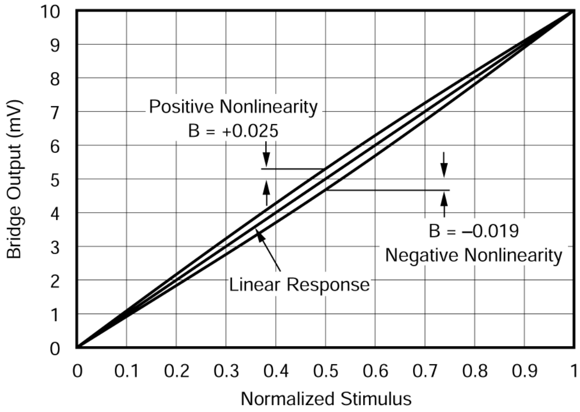


図 7-3. Bridge Transducer Transfer Function with Parabolic Nonlinearity

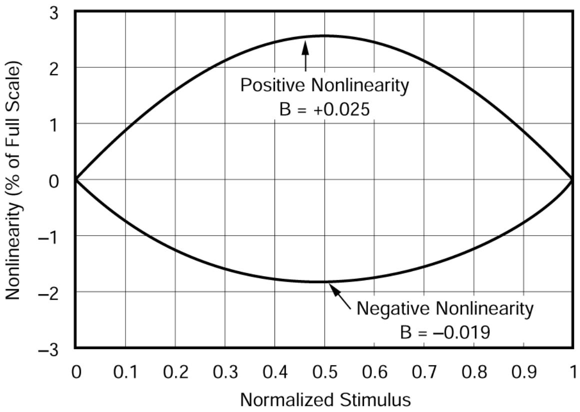
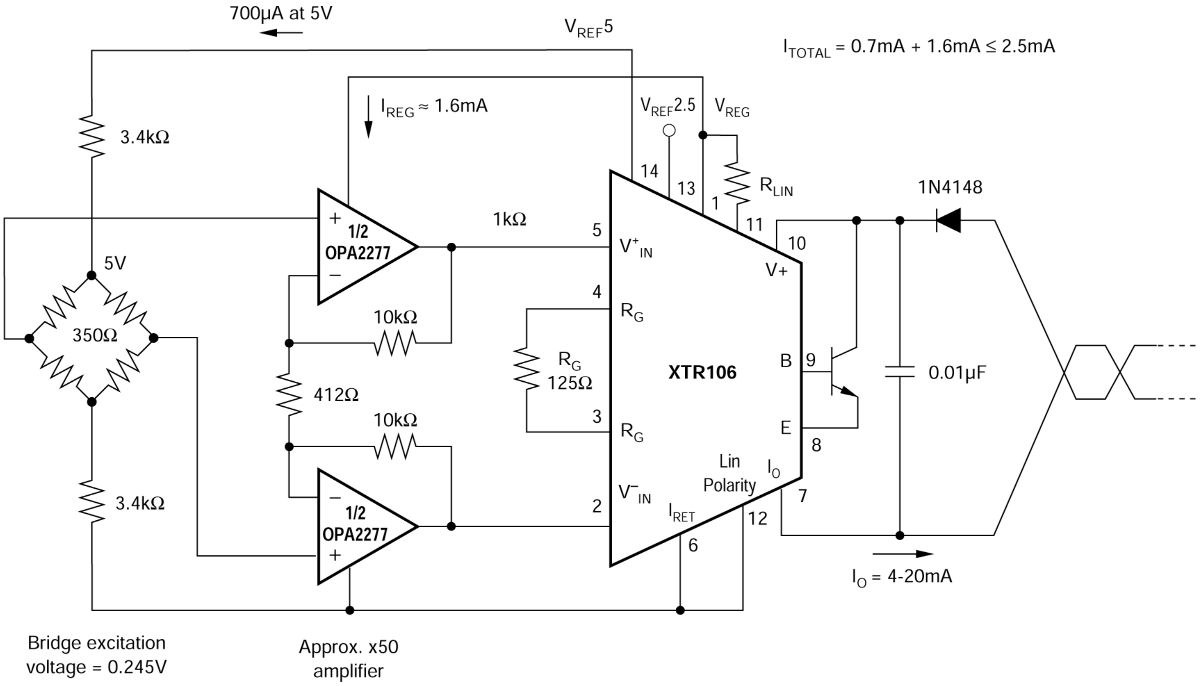


図 7-4. Nonlinearity vs Stimulus



(1) Shown connected to correct positive bridge nonlinearity. For negative bridge nonlinearity, see 図 6-3.

図 7-5. 350Ω Bridge With x50 Preamplifier

7.1.6 Other Sensor Types

The XTR106 can be used with a wide variety of inputs. The high input impedance instrumentation amplifier is versatile and can be configured for differential input voltages from millivolts to a maximum of 2.4V full scale. The linear range of the inputs is from 1.1V to 3.5V, referenced to I_{RET}. The linearization feature of the XTR106 can be used with any sensor whose output is ratiometric with an excitation voltage.

7.1.7 Radio Frequency Interference

The long wire lengths of current loops invite radio frequency (RF) interference. RF interference can be rectified by the sensitive input circuitry of the XTR106 causing errors. These errors generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the bridge sensor is remotely located, the interference can enter at the input terminals. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input reduce or eliminate this input interference. 図 6-6 shows to connect these bypass capacitors to the I_{RET} pin. Although the dc voltage at the I_{RET} pin is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter ground. The 0.01µF capacitor connected between V+ and I_O can help minimize output interference.

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7.1.8 Error Analysis

表 7-1 shows how to calculate the effect various error sources have on circuit accuracy. A sample error calculation for a typical bridge sensor measurement circuit (5kΩ bridge, V_{REF} = 5V, V_{FS} = 50mV) is provided. The results reveal the XTR106 excellent accuracy, in this case 1.2% unadjusted. Adjusting gain and offset errors improves circuit accuracy to 0.33%. These are worst-case errors; maximum values were used in the calculations and all errors were assumed to be positive (additive). The XTR106 achieves performance that is difficult to obtain with discrete circuitry and requires less board space.

表 7-1. Error Calculation

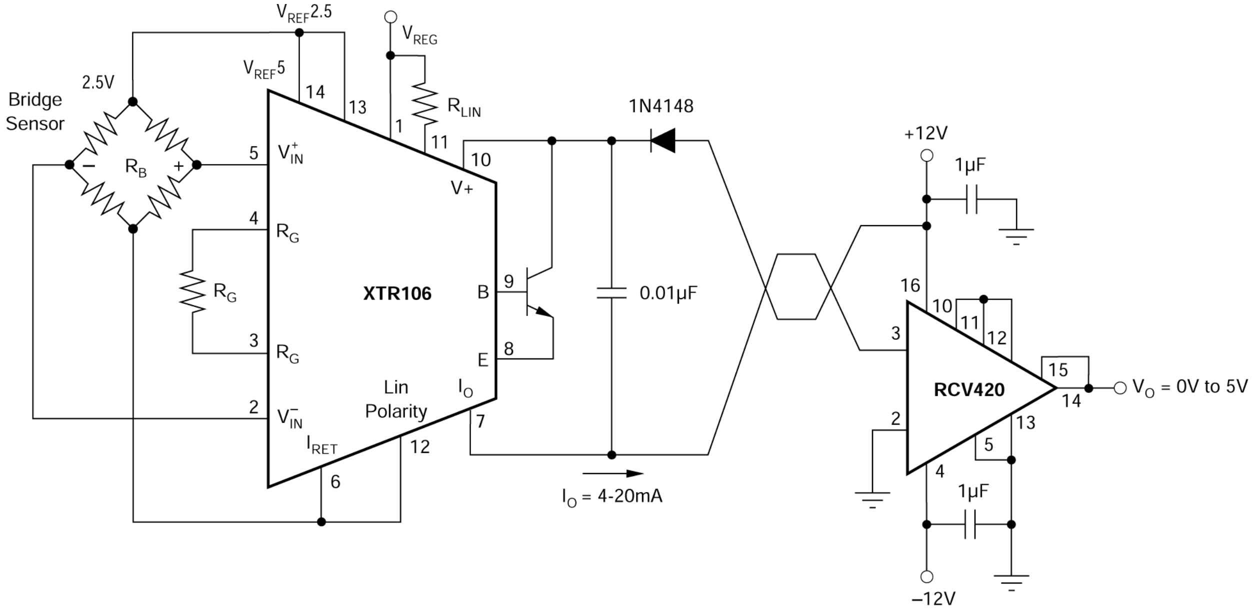
SAMPLE ERROR CALCULATION(1)				
Bridge Impedance (R_B) 5kΩ		**Full Scale Input (V_{FS}) 50mV**		
Ambient Temperature Range (ΔT_A) 20°C		**Excitation Voltage (V_{REF}) 5V**		
Supply Voltage Change (ΔV+) 5V		**Common-Mode Voltage Change (ΔCM) 25mV (= V_{FS}/2)**		
			ERROR (ppm of Full Scale)	
ERROR SOURCE	**SAMPLE ERROR EQUATION**	**ERROR CALCULATION**	**UNADJ**	**ADJUST**
INPUT				
Input offset voltage	$V_{OS}/V_{FS} \cdot 10^6$	200μV/50mV · 10^6	2000	0
vs common-mode	CMRR · $\Delta CM/V_{FS} \cdot 10^6$	50μV/V · 0.025V/50mV · 10^6	25	25
vs power supply	(V_{OS} vs V+) · (ΔV+)/V_{FS} · 10^6	3μV/V · 5V/50mV · 10^6	300	300
Input bias current	CMRR · I_B · (R_B/2)/V_{FS} · 10^6	50μV/V · 25nA · 2.5kΩ/50mV · 10^6	0.1	0
Input offset current	$I_{OS} \cdot R_B/V_{FS} \cdot 10^6$	3nA · 5kΩ/50mV · 10^6	300	0
		Total Input Error	**2625**	**325**
EXCITATION				
Voltage reference accuracy	V_{REF} Accuracy (%)/100% · 10^6	0.25%/100% · 10^6	2500	0
vs supply	(V_{REF} vs V+) · (ΔV+) · (V_{FS}/V_{REF})	20ppm/V · 5V (50mV/5V)	1	1
		Total Excitation Error	**2501**	**1**
GAIN				
Span	Span Error (%)/100% · 10^6	0.2%/100% · 10^6	2000	0
Nonlinearity	Nonlinearity (%)/100% · 10^6	0.01%/100% · 10^6	100	100
		Total Gain Error	**2100**	**100**
OUTPUT				
Zero output	| I_{ZERO} – 4mA |/16000μA · 10^6	25μA/16000μA · 10^6	1563	0
vs supply	(I_{ZERO} vs V+) · (ΔV+)/16000μA · 10^6	0.2μA/V · 5V/16000μA · 10_6	62.5	62.5
		Total Output Error	**1626**	**63**
DRIFT (ΔT_A = 20°C)				
Input offset voltage	Drift · ΔT_A/(V_{FS}) · 10^6	1.5μV/°C · 20°C/(50mV) · 10^6	600	600
Input offset current (typical)	Drift · ΔT_A· R_B/(V_{FS}) · 10^6	5pA/°C · 20°C · 5kΩ/(50mV) · 10^6	10	10
Voltage reference accuracy		35ppm/°C · 20°C	700	700
Span		225ppm/°C · 20°C	500	500
Zero output	Drift · ΔT_A/16000μA · 10^6	0.9μA/°C · 20°C/16000μA · 10^6	1125	1125
		Total Drift Error	**2936**	**2936**
NOISE (0.1Hz to 10Hz, typical)				
Input offset voltage	V_n(p-p)/V_{FS} · 10^6	0.6μV/50mV · 10^6	12	12
Zero output	I_{ZERO} Noise / 16000μA · 10^6	0.035μA/16000μA · 10^6	2.2	2.2
Thermal R_B noise	$[\sqrt{2} \cdot \sqrt{(R_B/2)/1k\Omega} \cdot 4nV/\sqrt{Hz} \cdot \sqrt{10Hz}]/V_{FS} \cdot 10^6$	$[\sqrt{2} \cdot \sqrt{2.5k\Omega/1k\Omega} \cdot 4nV/\sqrt{Hz} \cdot \sqrt{10Hz}]]/$ 50mV · 10^6	0.6	0.6
Input current noise	$(i_n \cdot 40.8 \cdot \sqrt{2} \cdot R_B/2)/V_{FS} \cdot 10^6$	$(200fA/\sqrt{Hz} \cdot 40.8 \cdot \sqrt{2} \cdot 2.5k\Omega)/50mV\cdot$ 10^6	0.6	0.6
		Total Noise Error	**15**	**15**

表 7-1. Error Calculation (続き)

SAMPLE ERROR CALCULATION[(1)]				
Bridge Impedance (R_B) 5kΩ		**Full Scale Input (V_{FS}) 50mV**		
Ambient Temperature Range (ΔT_A) 20°C		**Excitation Voltage (V_{REF}) 5V**		
Supply Voltage Change (ΔV+) 5V		**Common-Mode Voltage Change (ΔCM) 25mV (= V_{FS}/2)**		
			ERROR (ppm of Full Scale)	
ERROR SOURCE	**SAMPLE ERROR EQUATION**	**ERROR CALCULATION**	**UNADJ**	**ADJUST**
		TOTAL ERROR:	**11803**	**3340**
			1.18%	**0.33%**

(1) All errors are minimum and maximum, and referred to input, unless otherwise stated.

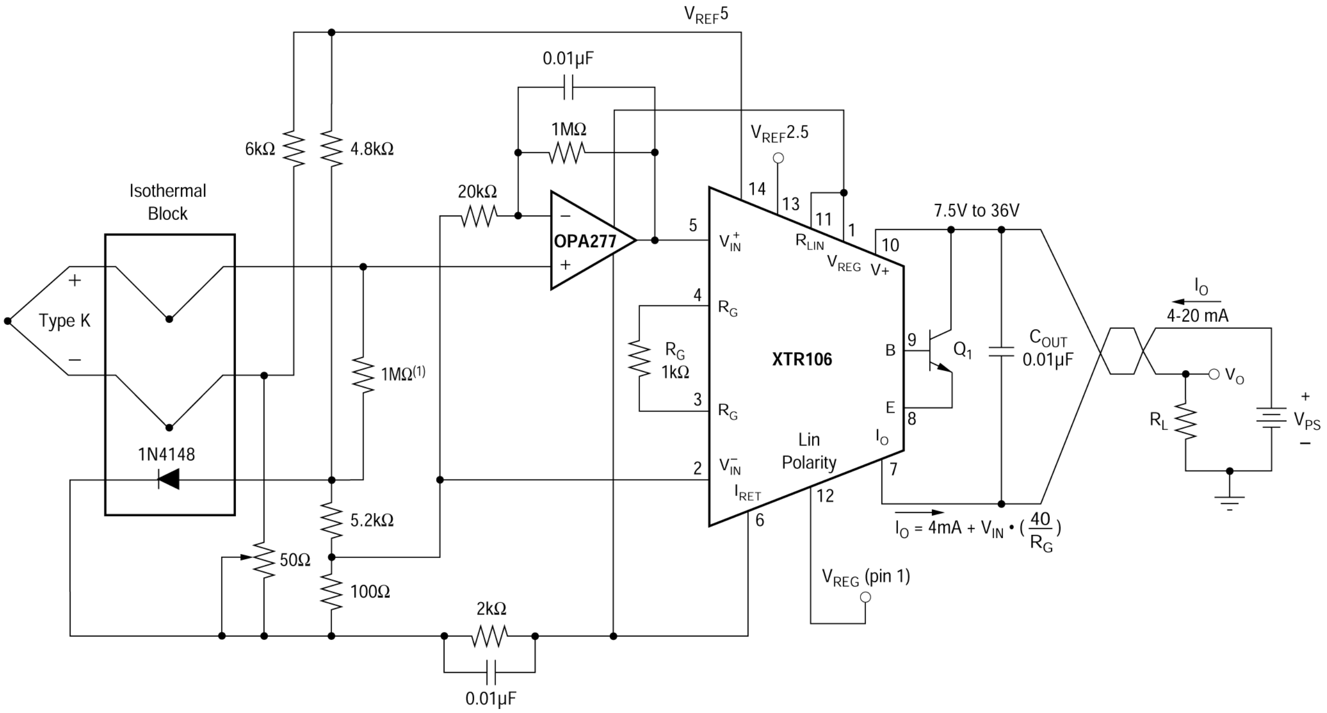
7.2 Typical Applications



(1) Lin Polarity shown connected to correct positive bridge nonlinearity. See 図 6-3 to correct negative bridge nonlinearity.

(2) See ISO124 data sheet if isolation is needed.

図 7-6. ±12V-Powered Transmitter and Receiver Loop



(1) For burn-out indication.

(2) See ISO124 data sheet if isolation is needed.

図 7-7. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold-Junction Compensation

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7.3 Layout

7.4 Layout Guidelines

The XTR106 is typically used with an external transistor (Q_1) to regulate the power dissipation of the 4mA to 20mA loop. This allows the resulting localized self-heating to be distanced from the precision circuitry of the XTR106 and reduces overtemperature drift errors.

The XTR106 can be used without the Q_1 transistor if the application requirements do not lead to violation of the device *Absolute Maximum Requirements*, such as the maximum junction temperature. Calculate the peak power dissipation and multiply by thermal resistance to approximate the associated junction temperature rise. Minimize overheat conditions for reliable long-term operation.

Place supply bypass capacitors close to the package and make connections with low-impedance conductors. Reduce trace lengths for R_G to minimize coupled environmental noise. If the loop power supply is electrically noisy, implement filtering using decoupling capacitors and small resistors or dampening inductors in series with V+.

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers* Precision Labs video series on Current Loop Transmitters
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* technical article
- Texas Instruments, *A Basic Guide to RTD Measurements* application note

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.5 Trademarks

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8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2003) to Revision B (January 2025) — Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- *「ピンの構成および機能」、「推奨動作条件」、「熱に関する情報」、「電気的特性」、「詳細説明」「機能ブロック図」、「アプリケーションと実装」、「代表的なアプリケーション」、「デバイスおよびドキュメントへのサポート」、「メカニカル、パッケージ、および注文情報」*の各セクションを追加しました 1
- *「アプリケーション」*セクションに最終機器を調整 1
- Moved operating and storage temperature parameters from *Electrical Characteristics* to *Absolute Maximum Ratings* 4
- Changed minimum operating temperature from −55°C to −40°C in *Absolute Maximum Ratings* 4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTR106P	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR106P A
XTR106P.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR106P A
XTR106PA	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-	XTR106P A
XTR106PA.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR106P A
XTR106U/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	XTR106U
XTR106U/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	XTR106U
XTR106U/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	XTR106U
XTR106UA	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	XTR106U A
XTR106UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	(XTR106U, XTR106UA) A
XTR106UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	(XTR106U, XTR106UA) A
XTR106UA/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	(XTR106U, XTR106UA) A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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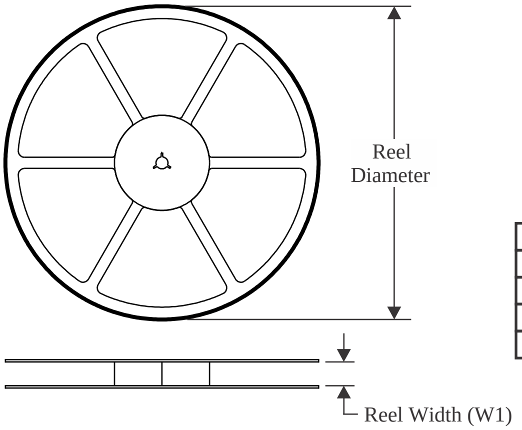
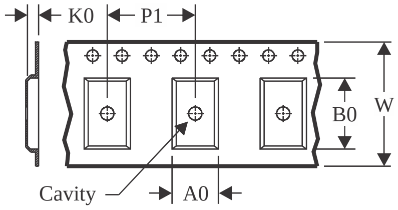
TAPE AND REEL INFORMATION

REEL DIMENSIONS

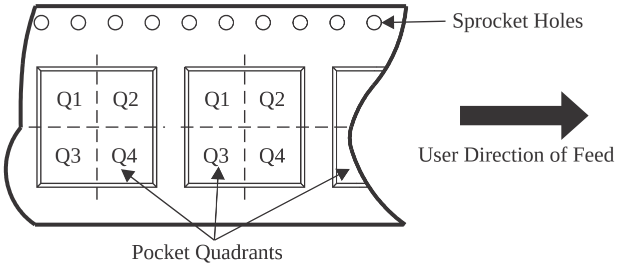


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

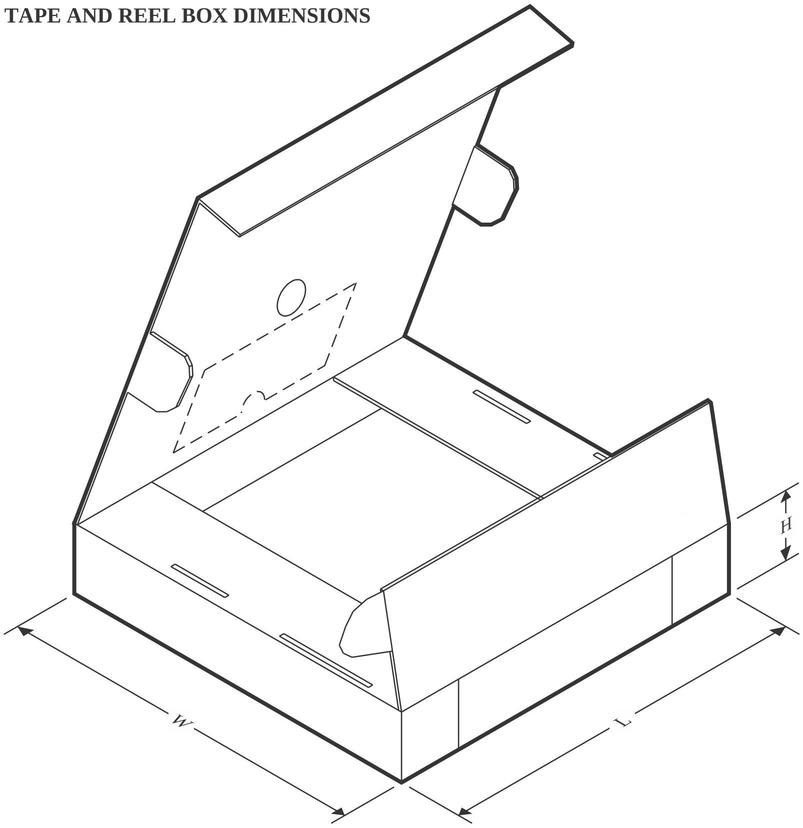
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR106U/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
XTR106UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

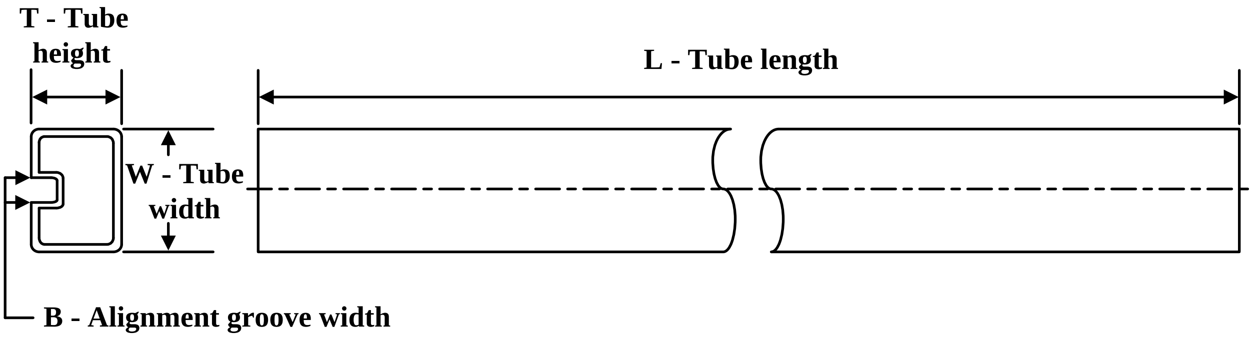
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

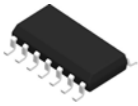
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR106U/2K5	SOIC	D	14	2500	353.0	353.0	32.0
XTR106UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
XTR106P	N	PDIP	14	25	506	13.97	11230	4.32
XTR106P.A	N	PDIP	14	25	506	13.97	11230	4.32
XTR106PA	N	PDIP	14	25	506	13.97	11230	4.32
XTR106PA.A	N	PDIP	14	25	506	13.97	11230	4.32

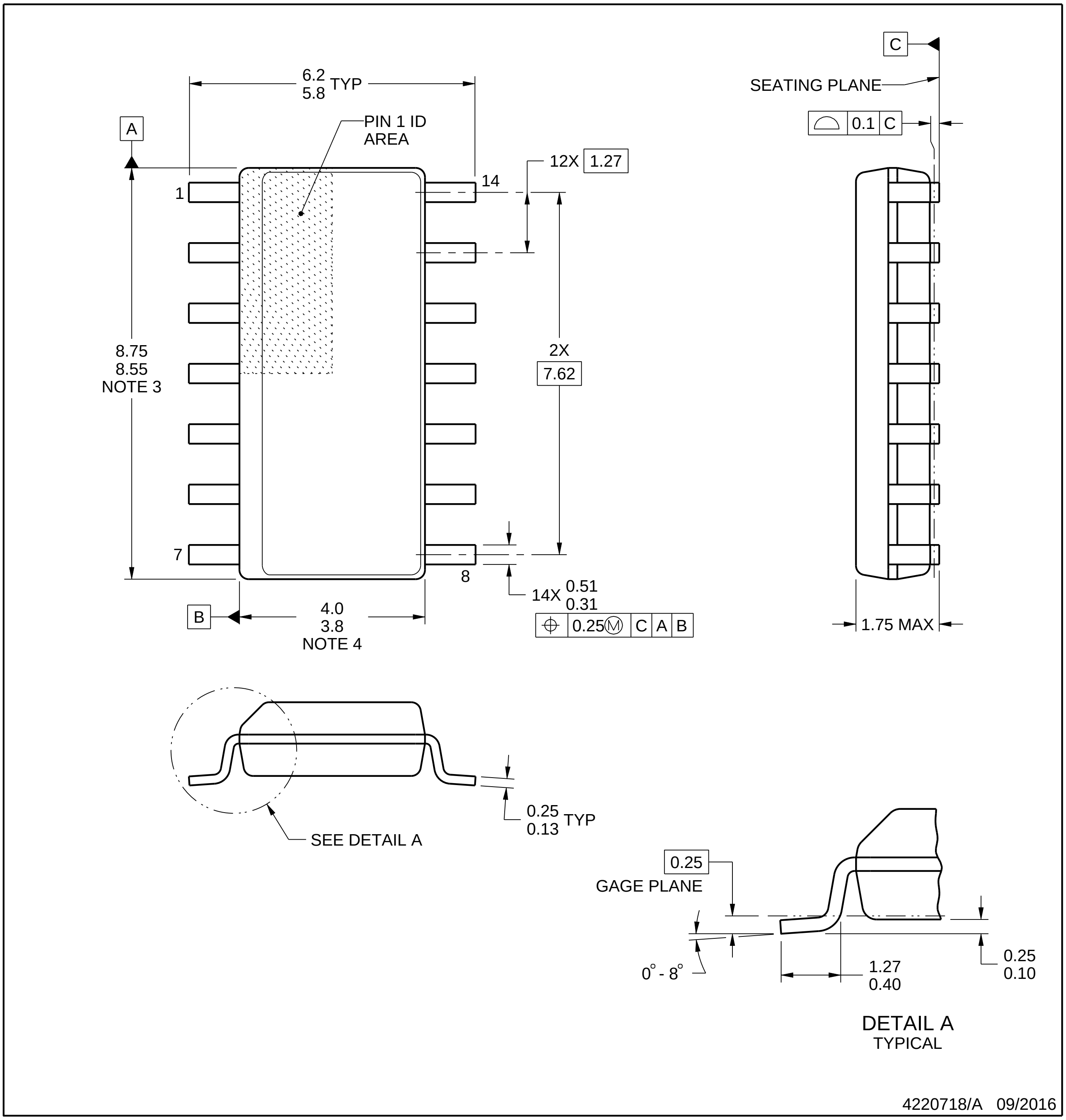


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

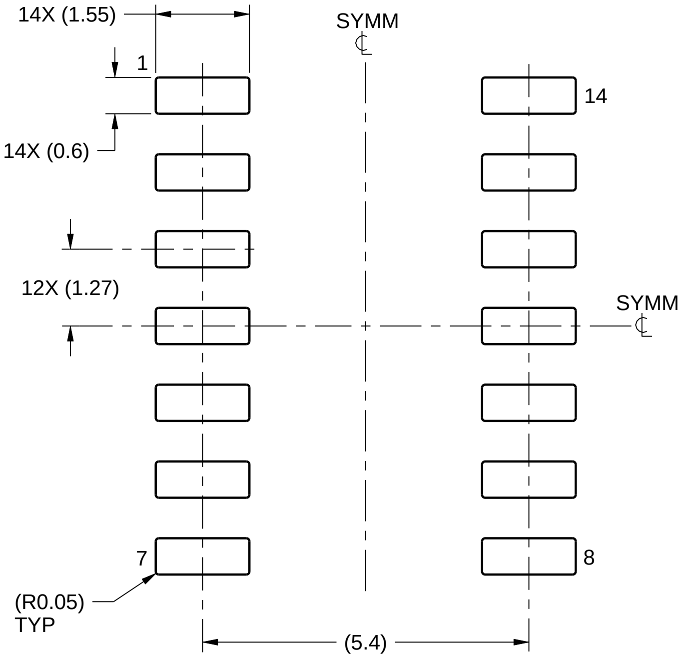
SMALL OUTLINE INTEGRATED CIRCUIT



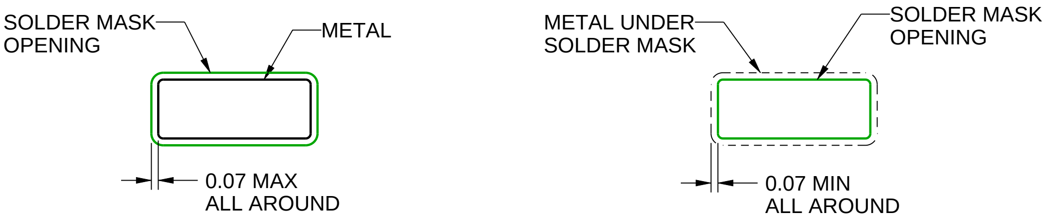
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



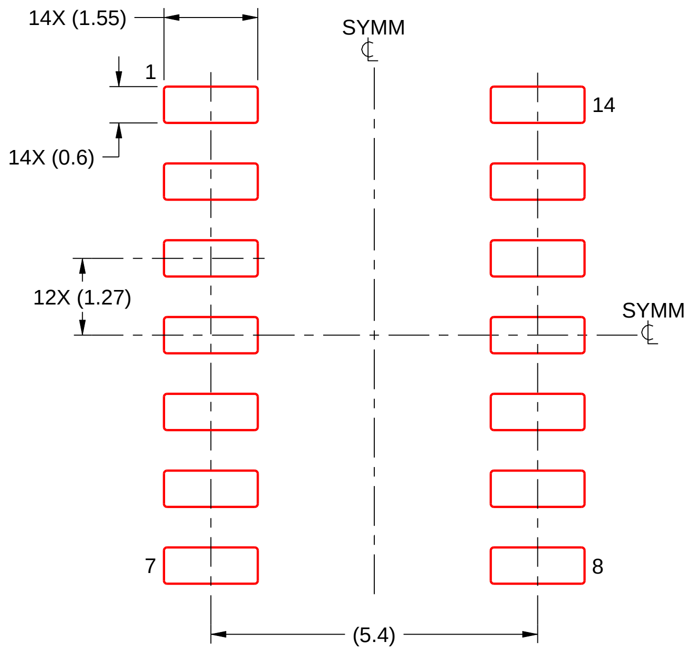
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

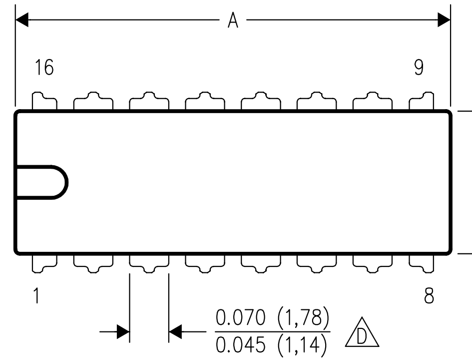
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

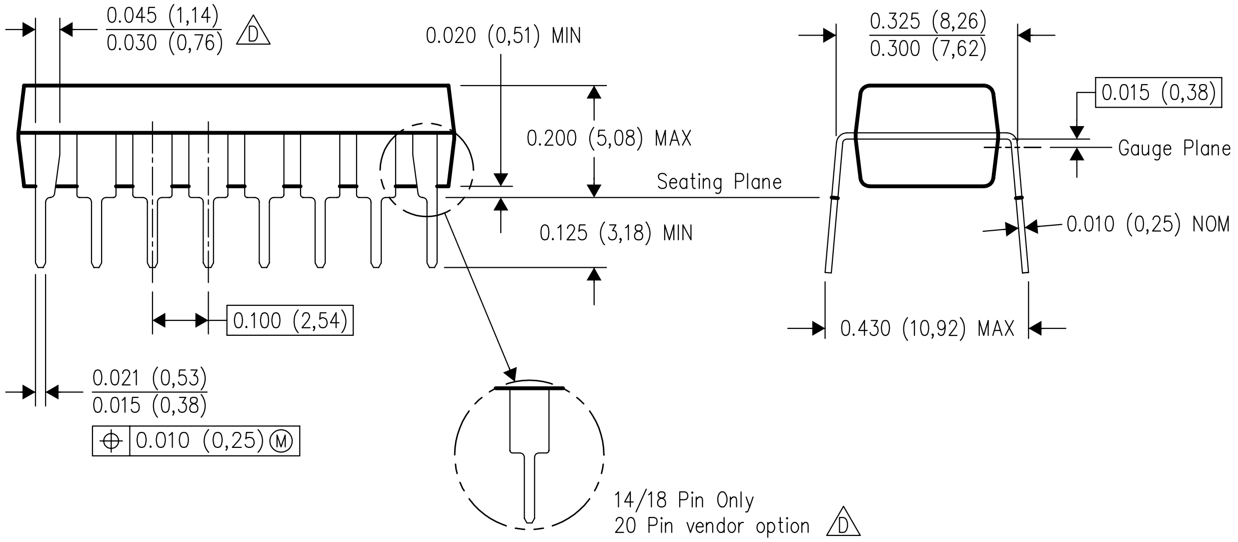
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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