TEXAS INSTRUMENTS
UCC5870-Q1
JAJSKM1C – OCTOBER 2019 – REVISED SEPTEMBER 2021

UCC5870-Q1 30A 絶縁型 IGBT/SiC MOSFET ゲート・ドライバ、車載アプリケーション用先進保護機能付き

1 特長

- 分割出力ドライバは、30A のピーク・ソース (供給) 電流と 30A のピーク・シンク (吸い込み) 電流を実現
- ゲート・ドライブの強度に応じて「即時」調整可能
- 150ns (最大値) の伝搬遅延時間とプログラマブルな最小パルス除去を備えたインターロックおよび貫通電流保護機能
- 1 次側と 2 次側のアクティブ短絡をサポート
- 設定可能なパワー・トランジスタ保護機能
  - DESAT に基づく短絡保護機能
  - シャント抵抗を使った過電流および短絡保護機能
  - NTC を使った過熱保護機能
  - パワー・トランジスタ障害時のプログラマブル・ソフト・ターンオフ (STO) と 2 レベル・ターンオフ (2LTOFF)
- 機能安全準拠
  - 機能安全アプリケーション向けに開発
  - ASIL D までの ISO 26262 システム設計を支援するドキュメントを提供
- 診断機能内蔵:
  - 保護コンパレータのための内蔵セルフ・テスト (BIST)
  - IN+ からトランジスタのゲートへの経路の整合性
  - パワー・トランジスタのスレッショルドの監視
  - 内部クロックの監視
  - フォルト・アラーム (nFLT1) および警告 (nFLT2) 出力
- 内蔵の 4A アクティブ・ミラー・クランプまたは外付けのミラー・クランプ・トランジスタ用外部駆動 (任意)
- 先進の高電圧クランプ制御
- 内部および外部電源の低電圧および過電圧保護機能
- 低電源またはフローティング入力時の、アクティブ出力プルダウンおよびデフォルト LOW 出力
- ドライバ・ダイ温度センシングおよび過熱保護機能
- V_{CM} = 1000V で 100kV/µs 以上のコモン・モード過渡耐性 (CMTI)
- SPI ベースのデバイス再構成、検証、監視、診断機能
- 内蔵 10 ビット ADC によるパワー・トランジスタ温度、電圧、電流の監視
- 安全関連認証:
  - UL1577 に準拠した絶縁耐圧:3750 V_{RMS}、1 分間 (予定)
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 0:–40℃～125℃の動作時周囲温度
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4b

2 アプリケーション

- HEV および EV トラクション・インバータ
- HEV および EV 電源モジュール

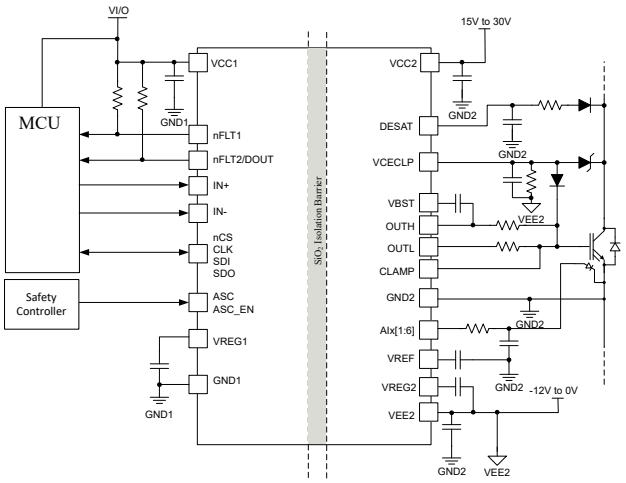
3 概要

UCC5870-Q1 デバイスは、EV/HEV アプリケーションの大電力 SiC MOSFET および IGBT を駆動するための高度に構成可能な絶縁型シングル・チャネル・ゲート・ドライバです。シャント抵抗を使った過電流保護、NTC を使った過熱保護、DESAT 検出などのパワー・トランジスタ保護機能には、これらのフォルト中の選択可能なソフト・ターンオフまたは 2 レベルのターンオフが含まれます。アプリケーションのサイズをさらに小さくするため、UCC5870-Q1 は、スイッチング中の 4A アクティブ・ミラー・クランプとドライバに電力が供給されていない間のアクティブ・ゲート・プルダウンを内蔵しています。内蔵の 10 ビット ADC を使うと、最大 6 つのアナログ入力とゲート・ドライバ温度を監視することでシステム管理を強化できます。ASIL-D 準拠システムの設計を簡素化する診断および検出機能を内蔵しています。これらの機能のパラメータとスレッショルドは SPI インターフェイスを使って設定できるため、本デバイスはほとんどすべての SiC MOSFET または IGBT と組み合わせて使用できます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
UCC5870-Q1	SSOP (36)	12.8mm × 7.5mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (November 2020) to Revision C (July 2021)	Page
• ピーク電流を 30A (標準値) に更新し、機能安全に関する情報を追加	1
• 特長の機能安全の箇条書き項目を更新	1
• Q100 の箇条書き項目で特長を更新	1
• Removed values from VCECLP and DESAT components as these are customer selected	3
• Updated drive strength to 30 A to align with typical value	24
• Updated secondary side TSD behavior to clarify the functions operation	44
• Added information about gate monitoring during secondary side ASC operation	45
• Corrected equation	49
• Corrected CONTROL2 bit name in list	50
• Corrected CONTROL2 bit name	54
• Corrected OVLO1_LEVEL selections	59
• Updated DESATTH description for clarity	59
• Updated SPI_FAULT description for clarity	59
• Corrected OR_NFLT1_SEC and OR_NFLT2_SEC descriptions	59
• Removed graph to prevent confusion.	99

Changes from Revision A (June 2020) to Revision B (November 2020)	Page
• マーケティング・ステータスを「事前情報」から初回リリースに更新	1

5 Pin Configuration and Functions

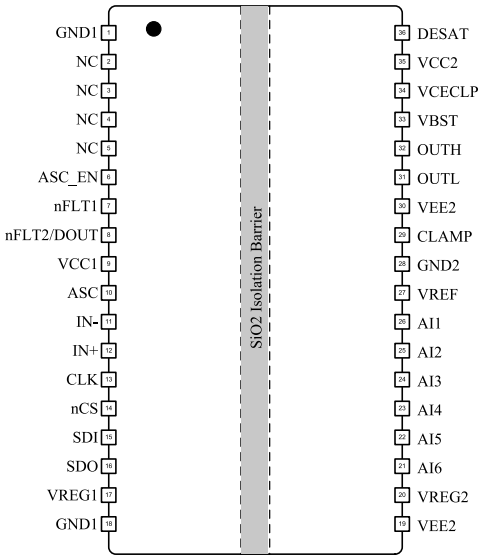


図 5-1. (DWJ) 36-Pin SOIC Top View

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	GND1	G	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side.
2	NC	—	No internal connection. Connect to GND1.
3	NC	—	No internal connection. Connect to GND1.
4	NC	—	No internal connection. Connect to GND1.
5	NC	—	No internal connection. Connect to GND1.
6	ASC_EN	I	Active Short Circuit Enable Input. ASC_EN enables the ASC function and forces the output of the driver to the state defined by the ASC input. If ASC is high, OUTH is pulled high. If ASC is low, OUTL is pulled low. See the Active Short Circuit (ASC) section for additional details.
7	nFLT1	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked. See the Fault and Warning Classification section for additional details.
8	nFLT2/DOUT	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Additionally, nFLT2 may be configured as DOUT to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked. See the Fault and Warning Classification or DOUT Functionality section for additional details.
9	V_{CC1}	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible. See the VCC1, VCC2, VEE2 Bypass Capacitors section for more details on selecting the values.
10	ASC	I	Active Short Circuit Control Input. ASC sets the drive state when ASC_EN is high. If ASC is high, OUTH is pulled high. If ASC is low, OUTL is pulled low. See the Active Short Circuit Support (ASC) section for additional details.
11	IN–	I	Negative PWM Input. IN- is connected to the IN+ from the opposite arm of the half-bridge. If IN+ and IN- overlap, the Shoot Through Protection (STP) fault is asserted. See the Shoot-Through Protection section for additional details.
12	IN+	I	Positive PWM Input. IN+ drives the state of the driver output. With the driver enabled, when IN+ is high, OUTH is pulled high. When IN+ is low, OUTL is pulled low. Drive IN+ with a 1kHz to 50kHz PWM signal, with a logic level determined by the VCC1 voltage. IN+ is connected to the IN- of the opposite arm of the half-bridge. If IN+ and IN- overlap, the Shoot Through Protection (STP) fault is asserted. See the Shoot-Through Protection section for additional details.

表 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
13	CLK	I	SPI Clock. CLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz. See the SPI Communication section for more details.
14	nCS	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI slave device. Drive nCS low during SPI communication. When nCS is high, the CLK and SDI inputs are ignored. See the SPI Communication section for more details.
15	SDI	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication. See the SPI Communication section for more details.
16	SDO	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK. See the SPI Communication section for more details.
17	V_{REG1}	P	Internal Voltage Regulator Output. VREG1 provides a 1.8V rail for internal primary-side circuits. Bypass VREG1 to GND1 with at least 4.7µF of ceramic capacitance. Do not put any additional load on VREG1.
18	GND1	G	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side.
19	V_{EE2}	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to the VEE1 pin as possible. See the VCC1, VCC2, and VEE2 Bypass Capacitors section for more details on selecting the values.
20	V_{REG2}	P	Internal voltage regulator output. VREG2 provides a 1.8V rail for internal secondary-side circuits. Bypass VREG2 to VEE2 with at least 4.7µF of ceramic capacitance. Do not put any additional load on VREG2.
21	AI6	I	Analog Input 6. AI6 is a multi-function input. It is configurable as an input to the internal ADC, a power FET current sense protection comparator input, and an ASC input for the secondary side. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI6 to be read by the ADC. See the Shunt Resistor based Overcurrent Protection (OCP) and Short Circuit Protection (SCP) section for details on configuring AI6 as a power FET current sense protection input. Finally, see the Active Short Circuit Support (ASC) section for details on configuring AI6 as an ASC input.
22	AI5	I	Analog Input 5. AI5 is a multi-function input. It is configurable as an input to the internal ADC, a power FET over temperature protection comparator input, and an ASC_EN input for the secondary side. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI5 to be read by the ADC. See the Temperature Monitoring and Protection for the Power Transistors section for details on configuring AI5 as a power FET over temperature protection input. Finally, see the Active Short Circuit Support (ASC) section for details on configuring AI5 as an ASC_EN input.
23	AI4	I	Analog Input 4. AI4 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI4 to be read by the ADC. See the Shunt Resistor based Overcurrent Protection (OCP) and Short Circuit Protection (SCP) section for details on configuring AI4 as a power FET current sense protection input.
24	AI3	I	Analog Input 3. AI3 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI3 to be read by the ADC. See the Temperature Monitoring and Protection for the Power Transistors section for details on configuring AI3 as a power FET over temperature protection input.
25	AI2	I	Analog Input 2. AI2 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI2 to be read by the ADC. See the Shunt Resistor based Overcurrent Protection (OCP) and Short Circuit Protection (SCP) section for details on configuring AI2 as a power FET current sense protection input.
26	AI1	I	Analog Input 1. AI1 is a multi-function input. It is configurable as an input to the internal ADC and a power FET current sense protection comparator input. See the Integrated ADC for Front-End Analog (FEA) Signal Processing section for details on configuring AI1 to be read by the ADC. See the Temperature Monitoring and Protection for the Power Transistors section for details on configuring AI1 as a power FET over temperature protection input.
27	V_{REF}	P	Internal ADC Voltage Regulator Output. VREF provides an internal 4V, reference for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance. If an external reference is desired, disable the internal VREF using the SPI register, and connect a 4V reference supply to VREF. Loads up to 5mA on VREF are allowed.
28	GND2	G	Gate Drive Common Input. Connect GND2 to the power FET source/ IGBT emitter. All AIx inputs, VREF, and DESAT are referenced to GND2.

表 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
29	CLAMP	IO	Miller Clamp Input. The CLAMP input is used to hold the gate of the power FET strongly to VEE2 while the power FET is "off". CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET. See the Active Miller Clamp section for additional details.
30	V_{EE2}	P	Secondary negative power supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to the VEE2 pin as possible. Additional capacitance may be needed depending on the required drive current. See the VCC1, VCC2, VEE2 Bypass Capacitors section for more details on selecting the values.
31	OUTL	O	Negative Gate Drive Voltage Output. When the driver is active, OUTL drives the gate of the power FET low when INP is low. Connect OUTL to the gate of the power FET through a gate resistor. The value of the gate resistor is chosen based on the slew rate required for the application. See the OUTH/ OUTL Outputs section for details on choosing the gate resistor.
32	OUTH	O	Positive Gate Drive Voltage Output. When the driver is active, OUTH drives the gate of the power FET high when INP is high. Connect OUTH to the gate of the power FET through a gate resistor. The value of the gate resistor is chosen based on the slew rate required for the application. See the OUTH/ OUTL Outputs section for details on choosing the gate resistor.
33	V_{BST}	P	Bootstrap Supply. VBST supplies power for the OUTH drive. Connect a 0.1µF ceramic capacitor between VBST and OUTH.
34	V_{CECLP}	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth threshold. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. Additionally, connect VCECLP to the anode of a zener diode to the collector of the power FET. For details on selecting the values and ratings for the required components, see the VCECLP Input section.
35	V_{CC2}	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the required drive current. See the VCC1, VCC2, VEE2 Bypass Capacitors section for more details on selecting the values.
36	DESAT	I	Desaturation based Short Circuit Detection Input. DESAT is used to detect a short circuit in the power FET. Bypass DESAT to GND2 with a ceramic capacitor to program the DESAT blanking time. In parallel, connect a schottky diode with the cathode connected to the DESAT. Additionally, connect DESAT to a resistor to the anode of a diode to the collector of the power FET to adjust the DESAT protection threshold. DESAT detects a fault when the VCE voltage of the power FET exceeds the defined threshold while the power FET is on. See the DESAT based Short Circuit Protection (DESAT) section for additional details.

(1) P = Power, G = Ground, I = Input, O = Output, - = NA

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage primary side referenced to GND1	–0.3	6	V
V_{CC2}	Positive supply voltage secondary side referenced to GND2	–0.3	33	V
V_{EE2}	Negative supply voltage output side referenced to GND2	–15	0.3	V
V_{SUP2}	Total supply voltage output side (V_{CC2} - V_{EE2})	–0.3	33	V
V_{OUTH}, V_{OUTL}	Voltage on the driver output pins referenced to GND2	V_{EE2}–0.3	V_{CC2}+0.3	V
V_{IOP}	Voltage on IO pins (ASC, ASC_EN, CLK, IN+, IN-, nCS, nFLTx, SDI, SDO) on primary side referenced to GND1	–0.3	V_{CC1}+0.3	V
V_{CLAMP}	Voltage on the Miller clamp pin referenced to GND2	V_{EE2}–0.3	V_{CC2} +0.3	V
V_{DESAT}	Voltage on DESAT referenced to GND2	–0.3	V_{CC2} +0.3	V
V_{CECLP}	Voltage on VCECLP referenced to GND2	V_{EE2}–0.3	V_{CC2} +0.3	V
V_{REG1}	Voltage on VREG1 referenced to GND1	–0.3	2	V
V_{REG2}	Voltage on VREG2 referenced to VEE2	–0.3	2	V
V_{REF}	Voltage on VREF referenced to GND2	–0.3	5.5	V
V_{BST}	Voltage on VBST referenced to OUTH	-0.3	5.3	V
V_{AI}	Voltage on the analog inputs referenced to GND2	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GND1 and VEE2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage input side	3		5.5	V
V_{CC2}	Positive supply voltage secondary side (V_{CC2} - GND2)	15		30	V
V_{EE2}	Negative supply voltage output side (V_{EE2} - GND2)	–12		0	V
V_{SUP2}	Total supply voltage output side (V_{CC2} - V_{EE2})	15		30	V
V_{IH}	High-level IO voltage (ASC, ASC_EN, IN+, IN-, nCS, SCLK, SDI)	0.7*V_{CC1}		V_{CC1}	V
V_{IL}	Low-level IO voltage (ASC, ASC_EN, IN+, IN-, nCS, SCLK, SDI)	0		0.3*V_{CC1}	V
I_{OHP}	Source current for primary side outputs (nFLT2, SDO)			5	mA
I_{OLP}	Sink current for primary side outputs (nFLTx, SDO)			5	mA
I_{OH}	Driver output source current from OUTH (1)			15	A
I_{OL}	Driver output sink current into OUTL (1)			15	A
V_{AI*}	Voltage on analog input (AI) pins referenced to GND2	0		V_{REF}+0.1	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VREG1}	Output voltage at VREG1 referenced to GND1 (2)		1.8		V
V_{VREG2}	Output voltage at VREG2 referenced to VEE2(3)		1.8		V
V_{VBST}	Ouput voltage at VBST referenced to OUTH(4)		V_{cc2} + 4.5		V
V_{VREF}	Voltage on the VREF pin vs GND2(5)	0	4	4.1	V
CMTI	Common mode transient immunity rating (dV/dt rate across the isolation barrier)			100	kV/us
f_{PWM}	PWM input frequency (IN+ and IN- pins)			50	kHz
f_{SPI}	SPI clock frequency			4	MHz
T_J	Maximum junction temperature	– 40		150	℃
t_{PWM}	PWM input pulse width (IN+ and IN- pins)	250			ns

(1) External gate resistor needs to be used to limit the max drive current to be not more than 15A.
(2) Connect a decoupling capacitor of 0.1uF+4.7uF between VREG1 and GND1. Do not connect external supply.
(3) Connect a decoupling capacitor of 0.1uF+4.7uF between VREG2 and VEE2. Do not connect external supply.
(4) Connect a decoupling capacitor of 100nF between VBST and OUTH. Do not connect external supply.
(5) Connect a decoupling capacitor of 1.0uF on the VREF pin.

6.4 Thermal Information

THERMAL METRIC(1)		UCC5870 DWJ 36 SOIC	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	T_A = 125C			500	mW
P_{D1}	Maximum power dissipation (side-1)	T_A = 125C			50	mW
P_{D2}	Maximum power dissipation (side-2)	T_A = 125C			450	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
PACKAGE SPECIFICATIONS				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	600	V
	Material group	According to IEC60664-1	I	

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
UL 1577				
C_{IO}	Barrier capacitance, input to output(2)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	2	pF
R_{IO}	Insulation resistance, input to output(2)	V_{IO} = 500 V, T_A = 25°C	10^12	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	10^11	
		V_{IO} = 500 V at T_S = 150°C	10^9	
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 3750 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 4500 V_{RMS}, t = 1 s (100% production)	3750	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator onthe printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases.Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Electrical Characteristics

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$V_{IT+(UVLO1)}$	UVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 0	2.6	2.75	2.9	V
$V_{IT+(UVLO1)}$	UVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 1	4.5	4.65	4.8	V
$V_{IT-(UVLO1)}$	UVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 0	2.3	2.45	2.6	V
$V_{IT-(UVLO1)}$	UVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 1	4.2	4.35	4.5	V
$V_{HYS(UVLO1)}$	UVLO threshold hysteresis of V_{CC1}			0.30		V
t_{UVLO1}	VCC1 UVLO detection deglitch time			20		µs
$V_{IT-(OVLO1)}$	OVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 0	3.7	3.85	4.0	V
$V_{IT-(OVLO1)}$	OVLO threshold of V_{CC1} falling	UVOV1_LEVEL = 1	5.2	5.35	5.5	V
$V_{IT+(OVLO1)}$	OVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 0	4.0	4.15	4.3	V
$V_{IT+(OVLO1)}$	OVLO threshold of V_{CC1} rising	UVOV1_LEVEL = 1	5.5	5.65	5.8	V
$V_{HYS(OVLO1)}$	OVLO threshold hysteresis of V_{CC1}			0.30		V
t_{OVLO1}	VCC1 OVLO detection deglitch time			20		µs
$V_{IT+(UVLO2)}$	UVLO threshold voltage of V_{CC2} rising with reference to GND2	UVLO2TH = 00b	15.2	16	16.8	V
		UVLO2TH = 01b	13.3	14	14.7	V
		UVLO2TH = 10b	11.4	12	12.6	V
		UVLO2TH = 11b	9.5	10	10.5	V

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT-(UVLO2)}$	UVLO threshold voltage of V_{CC2} falling with reference to GND2	UVLO2TH = 00b	14.25	15	15.75	V
		UVLO2TH = 01b	12.35	13	13.65	V
		UVLO2TH = 10b	10.45	11	11.55	V
		UVLO2TH = 11b	8.55	9	9.45	V
$V_{HYS(UVLO2)}$	UVLO threshold voltage hysteresis of V_{CC2}			1		V
t_{UVLO2}	VCC2 UVLO detection deglitch time			20		µs
$V_{IT-(OVLO2)}$	OVLO threshold voltage of V_{CC2} falling with reference to GND2	OVLO2TH = 00b	21.85	23	24.15	V
		OVLO2TH = 01b	19.95	21	22.05	V
		OVLO2TH = 10b	18.05	19	19.95	V
		OVLO2TH = 11b	16.15	17	17.85	V
$V_{IT+(OVLO2)}$	OVLO threshold voltage of V_{CC2} rising with reference to GND2	OVLO2TH = 00b	22.8	24	25.2	V
		OVLO2TH = 01b	20.9	22	23.1	V
		OVLO2TH = 10b	19	20	21	V
		OVLO2TH = 11b	17.1	18	18.9	V
$V_{HYS(OVLO2)}$	OVLO threshold voltage hysteresis of V_{CC2}			1		V
t_{OVLO2}	VCC2 OVLO detection blanking time			20		µs
$V_{IT-(UVLO3)}$	UVLO threshold voltage of V_{EE2} falling with reference to GND2	UVLO3TH = 00b	–3.15	–3	–2.85	V
		UVLO3TH = 01b	–5.25	–5	–4.75	V
		UVLO3TH = 10b	–8.4	–8	–7.6	V
		UVLO3TH = 11b	–10.5	–10	–9.5	V
$V_{IT+(UVLO3)}$	UVLO threshold voltage of V_{EE2} rising with reference to GND2	UVLO3TH = 00b	–2.1	–2	–1.9	V
		UVLO3TH = 01b	–4.2	–4	–3.8	V
		UVLO3TH = 10b	–7.35	–7	–6.65	V
		UVLO3TH = 11b	–9.45	–9	–8.55	V
$V_{HYS(UVLO3)}$	UVLO threshold voltage hysteresis of V_{EE2}			1		V
t_{UVLO3}	VEE2 UVLO detection blanking time			20		µs
$V_{IT+(OVLO3)}$	OVLO threshold voltage of V_{EE2} rising with reference to GND2	OVLO3TH = 00b	–5.25	–5	–4.75	V
		OVLO3TH = 01b	–7.35	–7	–6.65	V
		OVLO3TH = 10b	–10.5	–10	–9.5	V
		OVLO3TH = 11b	–12.6	–12	–11.4	V
$V_{IT-(OVLO3)}$	OVLO threshold voltage of V_{EE2} falling with reference to GND2	OVLO3TH = 00b	–6.3	–6	–5.7	V
		OVLO3TH = 01b	–8.4	–8	–7.6	V
		OVLO3TH = 10b	–11.55	–11	–10.45	V
		OVLO3TH = 11b	–13.65	–13	–12.35	V
$V_{HYS(OVLO3)}$	OVLO threshold voltage hysteresis of V_{EE2}			1		V
t_{OVLO3}	VEE2 OVLO detection blanking time			20		µs
I_{QVCC1}	Quiescent Current of V_{CC1}	No switching, VCC1 = 5V			7.7	mA
I_{QVCC2}	Quiescent Current of V_{CC2}	No switching, VCC2 = 20V, VEE2 = -10V			15	mA
I_{QVEE2}	Quiescent Current of V_{EE2}	No switching, VCC2 = 20V, VEE2 = -10V			15	mA
$t_{RP(VCC1)}$	Slew rate of V_{CC1}				0.1	V/µs
$t_{RP(VCC2)}$	Slew rate of V_{CC2}				0.1	V/µs

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{RP(VEE2)}$	Slew rate of V_{EE2}				0.1	V/µs
LOGIC IO						
V_{IH}	Input-high threshold voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	Input rising, VCC1 = 3.3V			0.7*V_{CC1}	V
	Input-high threshold voltage of secondary IO in ASC mode (AI5, and AI6)	Input rising, VREF=4V			3.0	V
V_{IL}	Input-low threshold voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	VCC1 = 3.3V	0.3*V_{CC1}			V
	Input-low input-threshold voltage of secondary IO in ASC mode (AI5 and AI6)	Input falling	1.5			V
$V_{HYS(IN)}$	Input hysteresis voltage of primary IO (IN+, IN-, ASC, and ASC_EN)	VCC1=3.3V		0.1*V_{CC1}		V
	Input hysteresis voltage of secondary IO in ASC mode (AI5, and AI6)			0.5		V
I_{LI}	Leakage current on the input IO pins ASC, ASC_EN, IN+, IN-, CLK, and SDI	V_{IO} = GND1, V_{IO} is the voltage on IO pins			5	µA
	Leakage current on nCS	V_{IO} = VCC1, V_{IO} is the voltage on IO pins			5	µA
R_{PUI}	Pullup resistance for nCS		40		100	kΩ
R_{PDI}	Pulldown resistance for ASC, ASC_EN, IN+, IN-, CLK, and SDI		40		100	kΩ
	Pulldown resistance for AI5 and AI6 in ASC mode		800		1200	kΩ
V_{OH}	Output logic-high voltage (SDO)	4.5mA output current, VCC1 = 5V	0.9*V_{CC1}			V
V_{OL}	Output logic-low voltage (nFLT1, nFLT2, and SDO)	4.5mA sink current, VCC1 = 5V			0.1*V_{CC1}	V
f_{DOUT}	Output frequency of DOUT pin	FREQ_DOUT = 00b		13.9		kHz
		FREQ_DOUT = 01b		27.8		kHz
		FREQ_DOUT = 10b		55.7		kHz
		FREQ_DOUT = 11b		111.4		kHz
D_{DOUT}	Duty of DOUT	V_{AI*} = 0.36 V		10		%
		V_{AI*} = 1.8 V		50		%
		V_{AI*} = 3.24 V		90		%
I_{LO}	Leakage current on pin nFLT*	nFLT* = HiZ, VCC1 on nFLT* pin	–5		5	µA
	Leakage current on pin SDO	nCS = 1	–5		5	µA
R_{PUO}	Pullup resistance for pin nFLT*		40		100	kΩ
DRIVER STAGE						
V_{OUTH}	High-level output voltage (OUT and OUTH)	I_{OUT} = -100 mA	VCC2 – 0.033			V
V_{OUTL}	Low-level output voltage (OUT and OUTL)	I_{OUT} = 100 mA			33	mV
I_{OUTH}	Gate driver high output current	IN+= high, IN- = low, VCC2 - VOUTH = 5 V	15			A
I_{OUTL}	Gate driver low output current	IN- = low, IN + = high, VOUTL - VEE2 = 5 V	15			A

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STO}	Driver low output current during SC and OC faults	VOUTL - VEE2 = 6 V and STO_CURR = 00b, 100℃ to 150℃	0.24	0.3	0.36	A
		VOUTL - VEE2 = 6 V and STO_CURR = 01b, 100℃ to 150℃	0.48	0.6	0.72	A
		VOUTL - VEE2 = 6 V and STO_CURR = 10b, 100℃ to 150℃	0.72	0.9	1.08	A
		VOUTL - VEE2 = 6 V and STO_CURR = 11b, 100℃ to 150℃	0.96	1.2	1.44	A
ACTIVE MILLER CLAMP						
V_{CLP}	Low-level clamp voltage (internal Miller clamp)	I_{CLP} = 100 mA			100	mV
	Miller clamp current	MCLPTH=11b, V_{CLAMP} = V_{EE2}+4 V	3.2			A
V_{CLPTH}	Clamp threshold voltage with reference to VEE2	MCLPTH = 00b	1.2	1.5	1.8	V
		MCLPTH = 01b	1.6	2	2.5	V
		MCLPTH = 10b	2.25	3	3.75	V
		MCLPTH = 11b	3	4	5	V
V_{ECLP}	CLAMP output voltage in external Miller clamp mode		4.5	5	5.5	V
R_{ECLP_PD}	CLAMP pulldown resistance in external Miller clamp mode			13		Ω
R_{ECLP_PU}	CLAMP pull-up resistance in external Miller clamp mode			13		Ω
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping voltage (V_{OUTH} - V_{CC2}, V_{CLAMP} - V_{CC2})	IN+= high, IN- = low, t_{CLP} = 10us, I_{OUTH} or I_{CLAMP} = 500 mA		0.8	1.6	V
ACTIVE PULLDOWN						
V_{OUTSD}	Active shut-down voltage on OUTL	I_{OUTL} = 30mA, VCC2 = open			1.55	V
V_{OUTSD}	Active shut-down voltage on OUTL	I_{OUTL} = 0.1xI_{OUTL}, V_{CC2} = open			2.5	V
DESAT SHORT-CIRCUIT PROTECTION						
$V_{DESATth}$	DESAT detection threshold voltage wrt GND2	DESATTH = 0000b	2.25	2.5	2.75	V
		DESATTH = 0001b	2.7	3	3.3	V
		DESATTH = 0010b	3.15	3.5	3.85	V
		DESATTH = 0011b	3.6	4	4.4	V
		DESATTH = 0100b	4.05	4.5	4.95	V
		DESATTH = 0101b	4.5	5	5.5	V
		DESATTH = 0110b	4.95	5.5	6.05	V
		DESATTH = 0111b	5.4	6	6.6	V
		DESATTH = 1000b	5.85	6.5	7.15	V
		DESATTH = 1001b	6.3	7	7.7	V
		DESATTH = 1010b	6.75	7.5	8.25	V
		DESATTH = 1011b	7.2	8	8.8	V
		DESATTH = 1100b	7.65	8.5	9.35	V
		DESATTH = 1101b	8.1	9	9.9	V
		DESATTH = 1110b	8.55	9.5	10.45	V
		DESATTH = 1111b	9	10	11	V
V_{DESATL}	DESAT voltage with respect to GND2 when OUTL is driven low				1	V

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG}	Blanking capacitor charging current	V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 00b	0.555	0.6	0.645	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 01b	0.6475	0.7	0.7525	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 10b	0.74	0.8	0.86	mA
		V(DESAT) - GND2 = 2 V, DESAT_CHG_CURR = 11b	0.925	1	1.075	mA
I_{DCHG}	Blanking capacitor discharging current	V(DESAT) - GND2 = 6 V	14			mA
t_{LEB}	DESAT leading edge blanking time		127	158	250	ns
t_{DESFLT}	DESAT pin glitch filter	DESAT_DEGLITCH=0	90	158	190	ns
t_{DESFLT}	DESAT pin glitch filter	DESAT_DEGLITCH=1	270	316	401	ns
t_{DESAT} (90%)	DESAT protection reaction time from event to action (includes deglitch time)	V_{DESAT}>$V_{DESATth}$ to VOUTL 90% of V_{CC2}, C_{LOAD} = 1 nF, DESAT_DEGLITCH=0			160 + t_{DESFLT}	ns
OVERCURRENT PROTECTION						
V_{OCth}	Over current detection threshold voltage	OCTH = 0000b	170	200	225	mV
		OCTH = 0001b	220	250	275	mV
		OCTH = 0010b	270	300	330	mV
		OCTH = 0011b	315	350	375	mV
		OCTH = 0100b	360	400	440	mV
		OCTH = 0101b	410	450	475	mV
		OCTH = 0110b	460	500	525	mV
		OCTH = 0111b	520	550	575	mV
		OCTH = 1000b	570	600	630	mV
		OCTH = 1001b	610	650	690	mV
		OCTH = 1010b	660	700	740	mV
		OCTH = 1011b	710	750	790	mV
		OCTH = 1100b	760	800	840	mV
		OCTH = 1101b	807	850	893	mV
		OCTH = 1110b	855	900	945	mV
		OCTH = 1111b	902	950	998	mV
V_{SCth}	Short circuit protection threshold	SCTH = 00b	460	500	530	mV
		SCTH = 01b	700	750	785	mV
		SCTH = 10b	945	1000	1050	mV
		SCTH = 11b	1185	1250	1312	mV
t_{SCBLK}	Short circuit protection blanking time with reference to system clock	SC_BLK = 00b		100		ns
		SC_BLK = 01b		200		ns
		SC_BLK = 10b		400		ns
		SC_BLK = 11b		800		ns

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCBLK}	Over current protection blanking time with reference to system clock	OC_BLK = 000b		500		ns
		OC_BLK = 001b		1000		ns
		OC_BLK = 010b		1500		ns
		OC_BLK = 011b		2000		ns
		OC_BLK = 100b		2500		ns
		OC_BLK = 101b		3000		ns
		OC_BLK = 110b		5000		ns
		OC_BLK = 111b		10000		ns
t_{SCFLT}	Short circuit protection deglitch filter		50	150	200	ns
t_{OCFLT}	Over current protection deglitch filter		50	150	200	ns
$t_{SC(90\%)}$	Short circuit protection reaction time from event to action (includes deglitch time)	V_{AIx} > V_{SCth} to VOUTL at 90% of VCC2, C_{LOAD} = 1nF, t_{SCBLK} expired			175 + t_{SCFLT}	ns
$t_{OC(90\%)}$	Over current protection reaction time from event to action (includes deglitch time)	V_{AIx} > V_{OCth} to VOUTL at 90% of VCC2, C_{LOAD} = 1nF, t_{OCBLK} expired			175 + t_{OCFLT}	ns
TWO-LEVEL TURN-OFF PLATEAU VOLTAGE LEVEL						
$V_{2\ LOFF}$	Plateau voltage (w.r.t. GND2) during two-level turnoff	2LOFF_VOLT = 000b	5	6	7	V
		2LOFF_VOLT = 001b	6	7	8	V
		2LOFF_VOLT = 010b	7	8	9	V
		2LOFF_VOLT = 011b	8	9	10	V
		2LOFF_VOLT = 100b	9	10	11	V
		2LOFF_VOLT = 101b	10	11	12	V
		2LOFF_VOLT = 110b	11	12	13	V
		2LOFF_VOLT = 111b	12	13	14	V
$t_{2\ LOFF}$	Plateau voltage during two-level turnoff hold time	2LOFF_TIME = 000b		150		ns
		2LOFF_TIME = 001b		300		ns
		2LOFF_TIME = 010b		450		ns
		2LOFF_TIME = 011b		600		ns
		2LOFF_TIME = 100b		1000		ns
		2LOFF_TIME = 101b		1500		ns
		2LOFF_TIME = 110b		2000		ns
		2LOFF_TIME = 111b		2500		ns
$I_{2\ LOFF}$	Discharge current for transition to plateau voltage level	2LOFF_CURR = 00b, 100℃ to 150℃	0.24	0.3	0.36	A
		2LOFF_CURR = 01b, 100℃ to 150℃	0.48	0.6	0.72	A
		2LOFF_CURR = 10b, 100℃ to 150℃	0.72	0.9	1.08	A
		2LOFF_CURR = 11b, 100℃ to 150℃	0.96	1.2	1.44	A
HIGH VOLTAGE CLAMPING						
$V_{CECLPTH}$	VCE clamping threshold with respect to VEE2		1.5	2.2	2.9	V
$V_{CECLPHYS}$	VCE clamping threshold hysteresis			200		mV
t_{VCECLP}	VCE clamping intervention-time			30		ns

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VCECLP_HLD}	VCE clamping hold on time	VCE_CLMP_HLD_TIME = 00b		100		ns
		VCE_CLMP_HLD_TIME = 01b		200		ns
		VCE_CLMP_HLD_TIME = 10b		300		ns
		VCE_CLMP_HLD_TIME = 11b		400		ns
OVERTEMPERATURE PROTECTION						
T_{SD_SET}	Overtemperature protection set for driver		155			°C
T_{SD_CLR}	Overtemperature protection clear for driver		135			°C
T_{WN_SET}	Overtemperature warning set for driver		130			°C
T_{WN_CLR}	Overtemperature warning clear for driver		110			°C
T_{HYS}	Hysteresis for thermal comparators			20		°C
I_{TO}	Bias current for temp sensing diode for pins AI1, AI3, and AI5	TEMP_CURR = 00b, Tj = 100C to 150C	0.097	0.1	0.103	mA
		TEMP_CURR = 01b, Tj = 100C to 150C	0.291	0.3	0.309	mA
		TEMP_CURR = 10b, Tj = 100C to 150C	0.582	0.6	0.618	mA
		TEMP_CURR = 11b, Tj = 100C to 150C	0.97	1	1.03	mA
V_{PS_TSDth}	The threshold of power switch over temperature protection.	TSDTH_PS = 000b	0.95	1	1.05	V
		TSDTH_PS = 001b	1.1875	1.25	1.3125	V
		TSDTH_PS = 010b	1.425	1.5	1.575	V
		TSDTH_PS = 011b	1.6625	1.75	1.8375	V
		TSDTH_PS = 100b	1.9	2	2.1	V
		TSDTH_PS = 101b	2.1375	2.25	2.3625	V
		TSDTH_PS = 110b	2.375	2.5	2.625	V
		TSDTH_PS = 111b	2.6125	2.75	2.8875	V
t_{PS_TSDFLT}	Power switch thermal shutdown deglitch time	PS_TSD_DEGLITCH = 00b		250		ns
		PS_TSD_DEGLITCH = 01b		500		ns
		PS_TSD_DEGLITCH = 10b		750		ns
		PS_TSD_DEGLITCH = 11b		1000		ns
GATE VOLTAGE MONITOR						
V_{GMH}	Gate monitor threshold value with reference to VCC2	IN+= high and IN- = low	– 4	– 3	– 2	V
V_{GML}	Gate monitor threshold value with reference to VEE2	IN + = low and IN- = high	2	3	4	V
t_{GMBLK}	Gate voltage monitor blanking time after driver receives PWM transition	GM_BLK = 00b		500		ns
		GM_BLK = 01b		1000		ns
		GM_BLK = 10b		2500		ns
		GM_BLK = 11b		4000		ns
t_{GMFLT}	Gate voltage monitor deglitch time			250		ns
I_{VGTHM}	Charge current for VGTH measurement	VCC2 - VOUTH = 10V		2		mA
t_{dVGTHM}	Delay time between VGTH measurement control command to gate voltage sampling point.			2300		µs
ADC						
FSR	Full scale input voltage range for A1 to A6		0	3.6	3.636	V

6.7 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Required voltage for external VREF	Accuracy of external reference directly affects the accuracy of the ADC		4		V
	Internal VREF output voltage			4		V
INL	Integral non-linearity	External reference, VREF = 4V	-1.2		1.2	LSB
		Internal reference	-4		9	LSB
DNL	Differential non-linearity	External reference, VREF = 4V	-0.75		0.75	LSB
		Internal reference	-0.75		0.75	LSB
$t_{ADREFEXT}$	External ADC reference turn on delay time from VCC2 > $V_{IT-(UVLO2)}$	$V_{IT-(UVLO2)}$ to 10% of VREF	10			µs
I_{TO2}	Pull up current on AI2,4,6 pins	$V_{AI2,4,6}$= VREF/2, ITO2_EN=H		10	15	µA
t_{hybrid}	IN+ hold time to cause switchover between center mode and edge mode	ADC in hybrid mode configuration		0.4		ms
t_{CONV}	Time to complete ADC conversion			5.1		µs
t_{RR}	Time between ADC conversions in Edge mode	ADC in edge mode or hybrid mode (after t_{HYBRID}) configuration		7.5		µs

6.8 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock frequency(1)			4	MHz
t_{CLK}	SPI clock period(1)	250			ns
t_{CLKH}	CLK logic high duration(1)	90			ns
t_{CLKL}	CLK logic low duration(1)	90			ns
t_{SU_NCS}	time between falling edge of nCS and rising edge of CLK(1)	50			ns
t_{SU_SDI}	setup time of SDI before the falling edge of CLK(1)	30			ns
t_{HD_SDI}	SDI data hold time (1)	45			ns
t_{D_SDO}	time delay from rising edge of CLK to data valid at SDO$$blue|[[\1]]			60	ns
t_{HD_SDO}	SDO output hold time(1)	40			ns
t_{HD_NCS}	time between the falling edge of CLK and rising edge of nCS(1)	50			ns
t_{HI_NCS}	SPI transfer inactive time(1)	250			ns
t_{ACC}	nCS low to SDO out of high impedance$$blue|[[\1]]		60	80	ns
t_{DIS}	time between rising edge of nCS and SDO in tri-state$$blue|[[\1]]		30	50	ns

(1) Ensured by bench char.

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	OUTH rise time	C_{LOAD} = 10 nF			150	ns
t_f	OUTL fall time	C_{LOAD} = 10 nF			150	ns
t_{PLH}, t_{PHL}	Propagation delay from INP to OUTx	C_{LOAD} = 0.1 nF, t_{GLITCH_IO} = 00b			150	ns
$t_{sk(p)}$	Pulse skew |t_{PHL} - t_{PLH}|	C_{LOAD} = 0.1 nF		20	50	ns
t_{sk-pp}	Part-to-part skew - same edge	C_{LOAD} = 0.1 nF		20	50	ns
f_{max}	Maximum switching frequency	C_{LOAD} = 0.1 nF, ADC disabled			50	kHz
t_{dFLT1}	Delay from fault detection to nFLT1 pin goes LOW.	C_{LOAD} = 100pF, R_{EPU} = 10kΩ			5	µs

6.9 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dFLT2}	Delay from fault detection to nFLT2 pin goes LOW.	C_{LOAD} = 100pF, R_{EPU} = 10kΩ			25	µs
t_{ASC_EN}	Required hold time for ASC after ASC_EN transition			1		µs
t_{ASC_DLY}	Delay from the ASC edge to OUTx transition (primary side)	ASC rising	2			µs
		ASC falling		0.1		µs
t_{ASC_DLY}	Delay from the AI6 (ASC) edge to OUTx transition (secondary side)	AI6 rising		1.8		µs
		AI6 falling		0.3		µs
t_{MUTE}	PWM input mute time in case of DESAT, SC, and PS_TSD fault	PWM_MUTE_EN = 1	10			ms
t_{GLITCH_IO}	Deglitch time for the primary side IO pins (exclude nCS, CLK, SDI, and SDO pins)	IO_DEGLITCH = 00b		0		ns
		IO_DEGLITCH = 01b		70		ns
		IO_DEGLITCH = 10b		140		ns
		IO_DEGLITCH = 11b		210		ns
t_{DEAD}	Dead time for shoot through protection	TDEAD = 000000b		0		ns
		TDEAD = 000001b	93	105	154	ns
		TDEAD = 000010b	159	175	228	ns
		TDEAD = 000011b	225	245	302	ns
		TDEAD = 000100b	291	315	376	ns
		TDEAD = 111111b	4178.3	4445	4748.8	ns
$t_{STARTUP}$	System start-up time (from power ready to nFLTx pins go high)				5	ms
$t_{VREGxOV}$	VREG1 and VREG2 overvoltage detection deglitch time			30		µs

6.10 Typical Characteristics

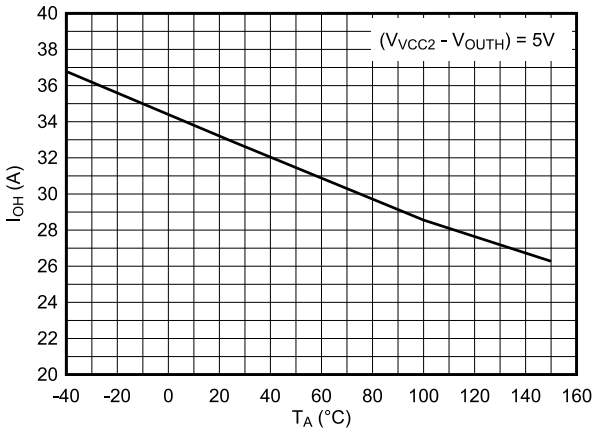


図 6-1. I_{OUTH} vs. Temperature

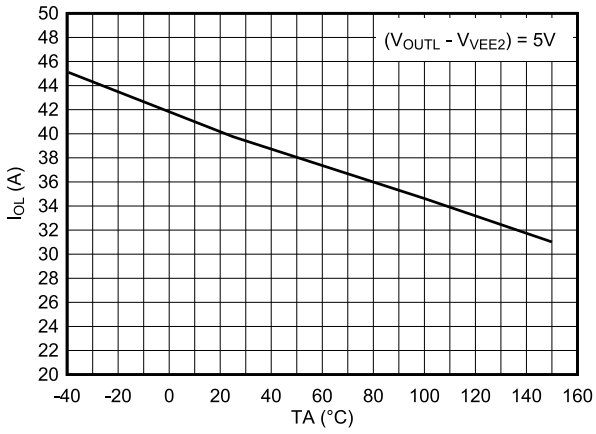


図 6-2. I_{OUTL} vs. Temperature

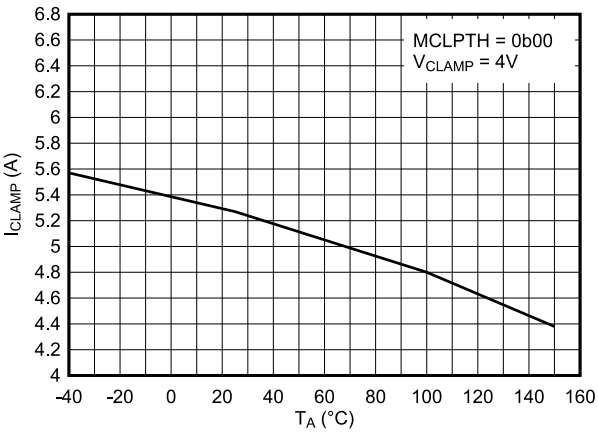


図 6-3. Internal Miller Clamp Current vs. Temperature

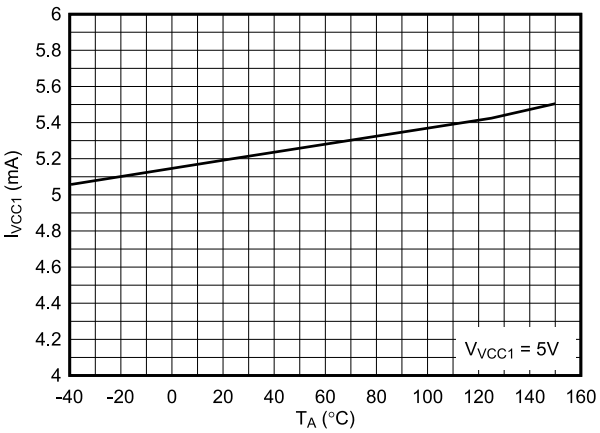


図 6-4. VCC1 Quiescent Current vs. Temperature

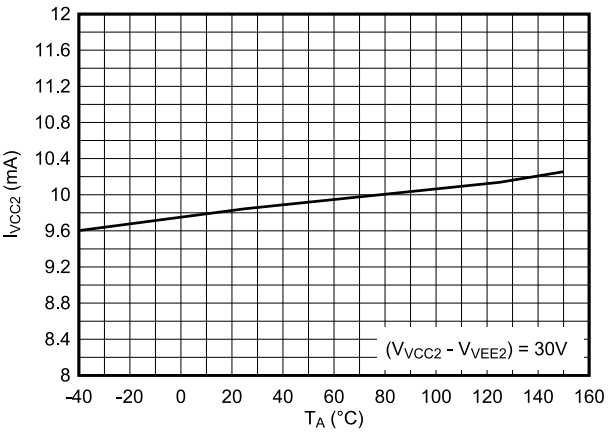


図 6-5. VCC2 Quiescent Current vs. Temperature

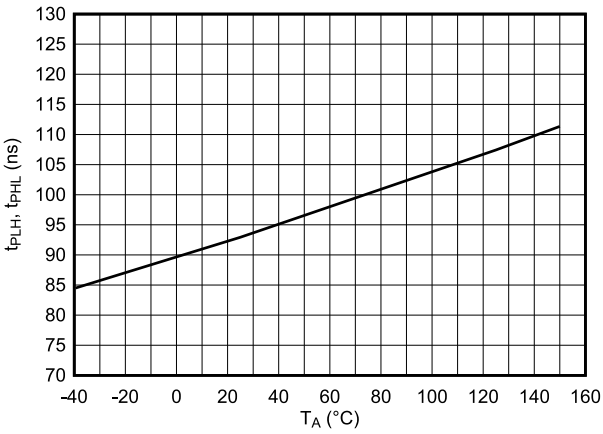


図 6-6. Propagation Delay vs. Temperature

6.10 Typical Characteristics (continued)

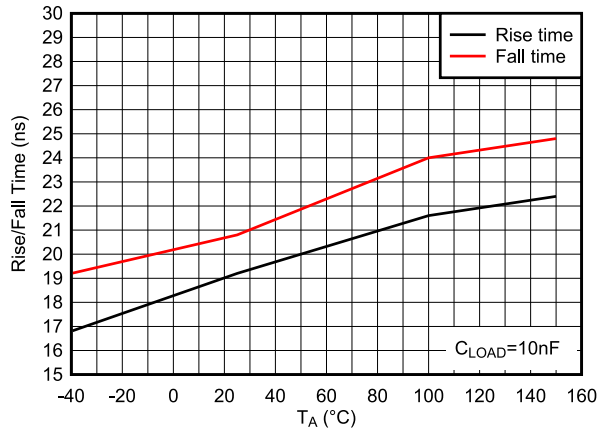


図 6-7. Rise/Fall Time vs. Temperature

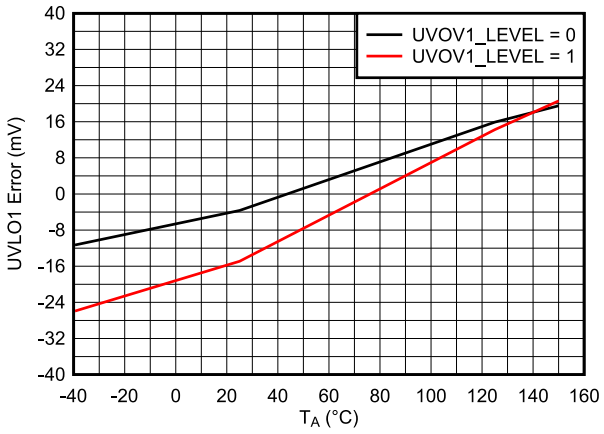


図 6-8. UVLO Threshold Error vs. Temperature

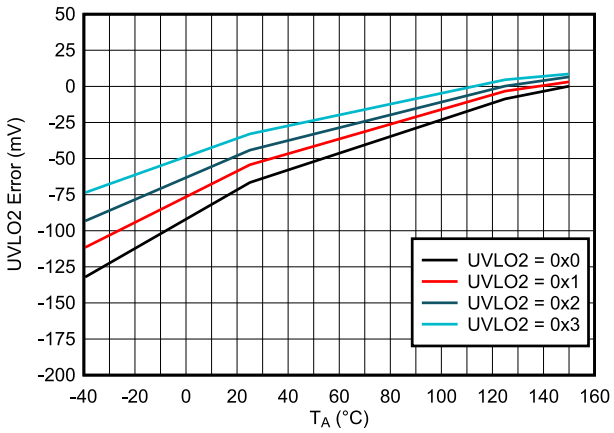


図 6-9. UVLO2 Error vs. Temperature

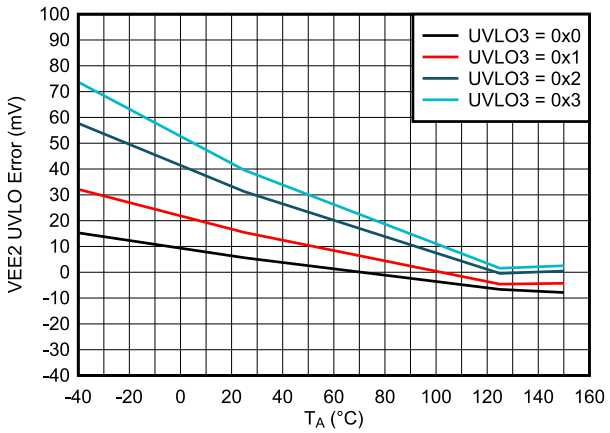


図 6-10. VEE2 UVLO Error vs. Temperature

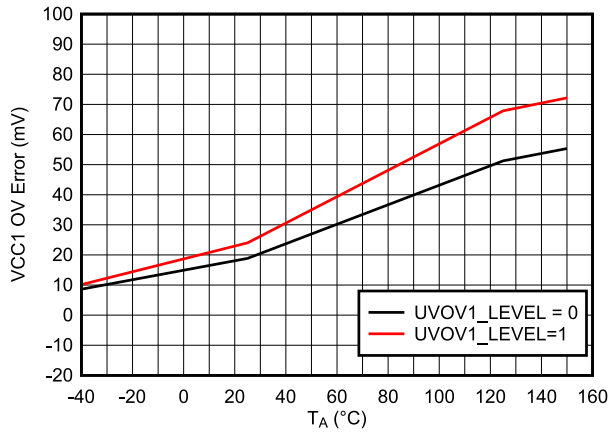


図 6-11. VCC1 OVLO Error vs. Temperature

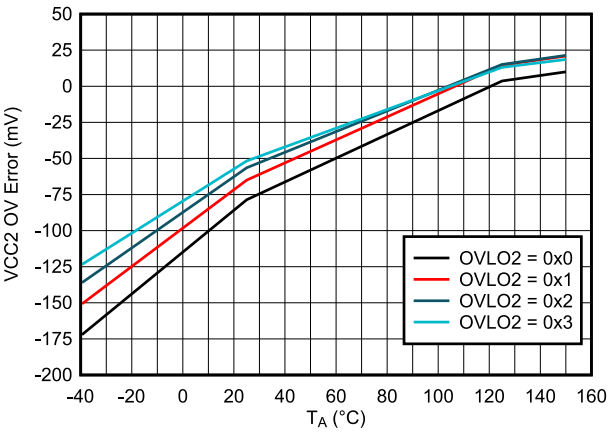


図 6-12. VCC2 OVLO Error vs. Temperature

6.10 Typical Characteristics (continued)

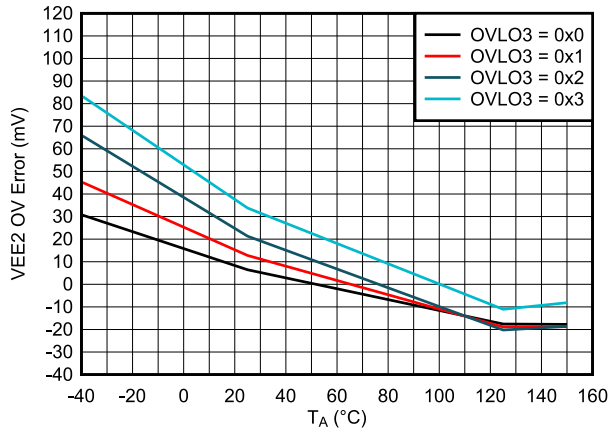


図 6-13. VEE2 OVLO Error vs. Temperature

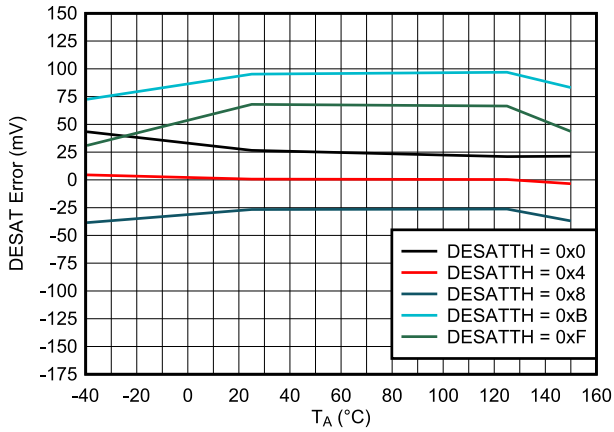


図 6-14. DESAT Threshold Error vs. Temperature

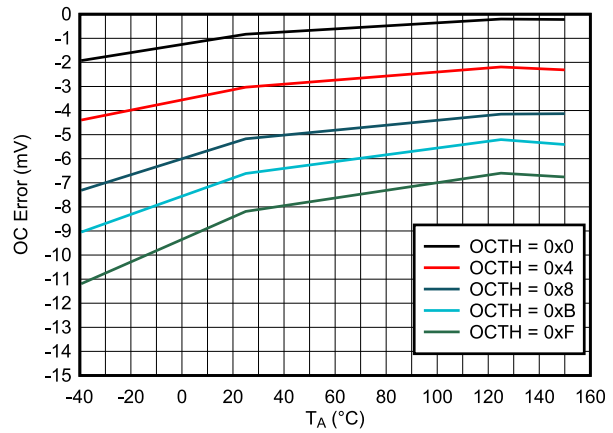


図 6-15. OC Threshold Error vs. Temperature

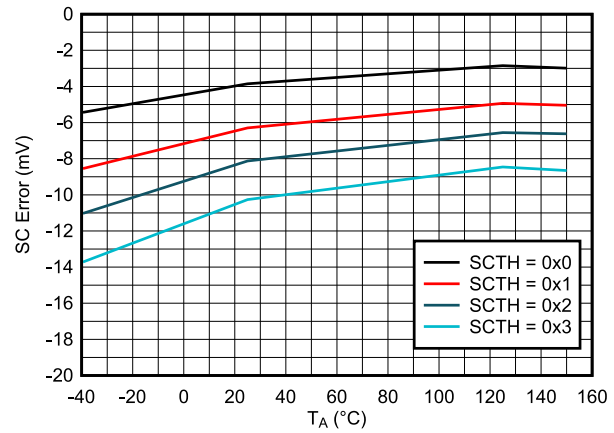


図 6-16. SC Threshold Error vs. Temperature

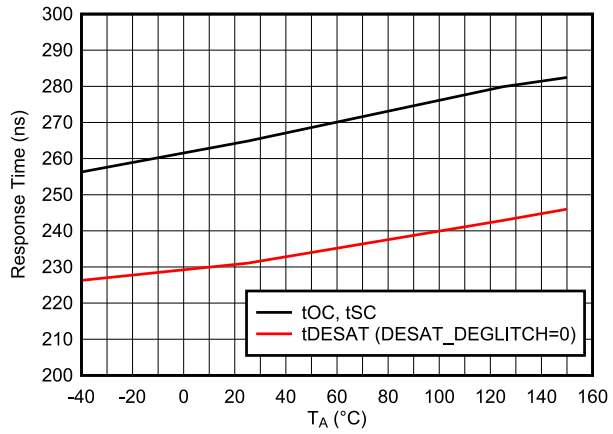


図 6-17. Overcurrent Protection Response Time vs. Temperature

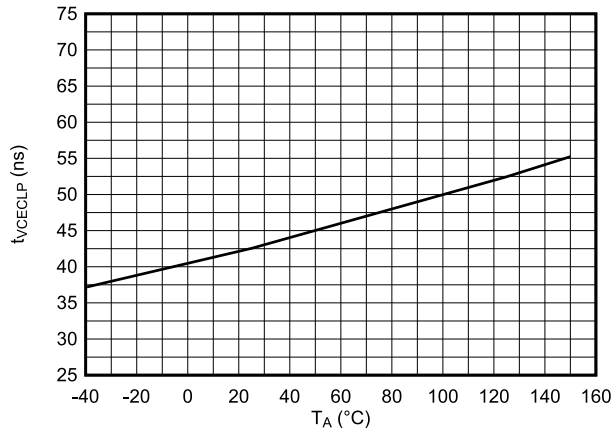


図 6-18. VCECLP Intervention Time vs. Temperature

6.10 Typical Characteristics (continued)

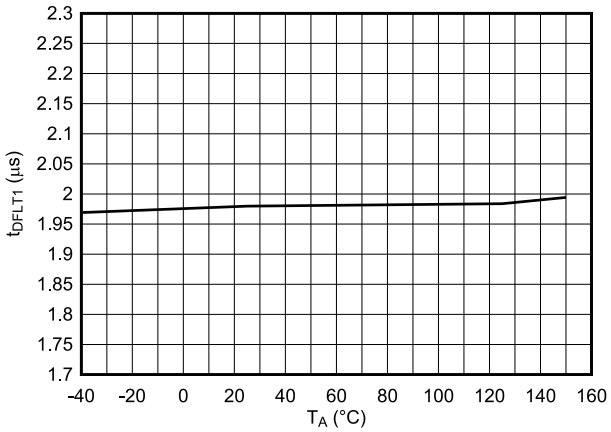


図 6-19. nFLT1 Response Time vs Temperature

7 Detailed Description

7.1 Overview

The UCC5870-Q1 is a platform supporting device, targeted for EV/HEV traction inverter applications. The flexibility of SPI programming of blanking times, deglitches, thresholds, function enables, and fault handling allow the UCC5870-Q1 to support a wide variety of IGBT or SiC power transistors that are used across all EV/HEV traction inverter applications. UCC5870-Q1 integrates all of the protection features required in most traction inverter applications. Additionally, the 30A gate drive capability eliminates the need for external booster circuit, reducing overall solution size. The integrated Miller clamp circuit holds the gate off during transient events and can be configured to use the internal 4A pulldown, or drive an external n-channel MOSFET. Advanced, internal capacitor-based isolation technology maximizes CMTI performance, while minimizing the radiated emissions.

All of the protections for the power transistor are integrated into the UCC5870-Q1. It supports DESAT and resistor based overcurrent protection. A negative temperature coefficient power transistor temperature sensor monitor is built into the device to alert the host and prevent damage from over-temperature conditions in the switch. A zener-breakdown based clamping function is integrated to reduce the gate drive, and thereby the overshoot energy, when over voltage spikes occur during turn-off caused by inductive kick-back. Real time gate monitoring is integrated to ensure proper connection to the power transistor and alert the host to a fault in the gate driver path.

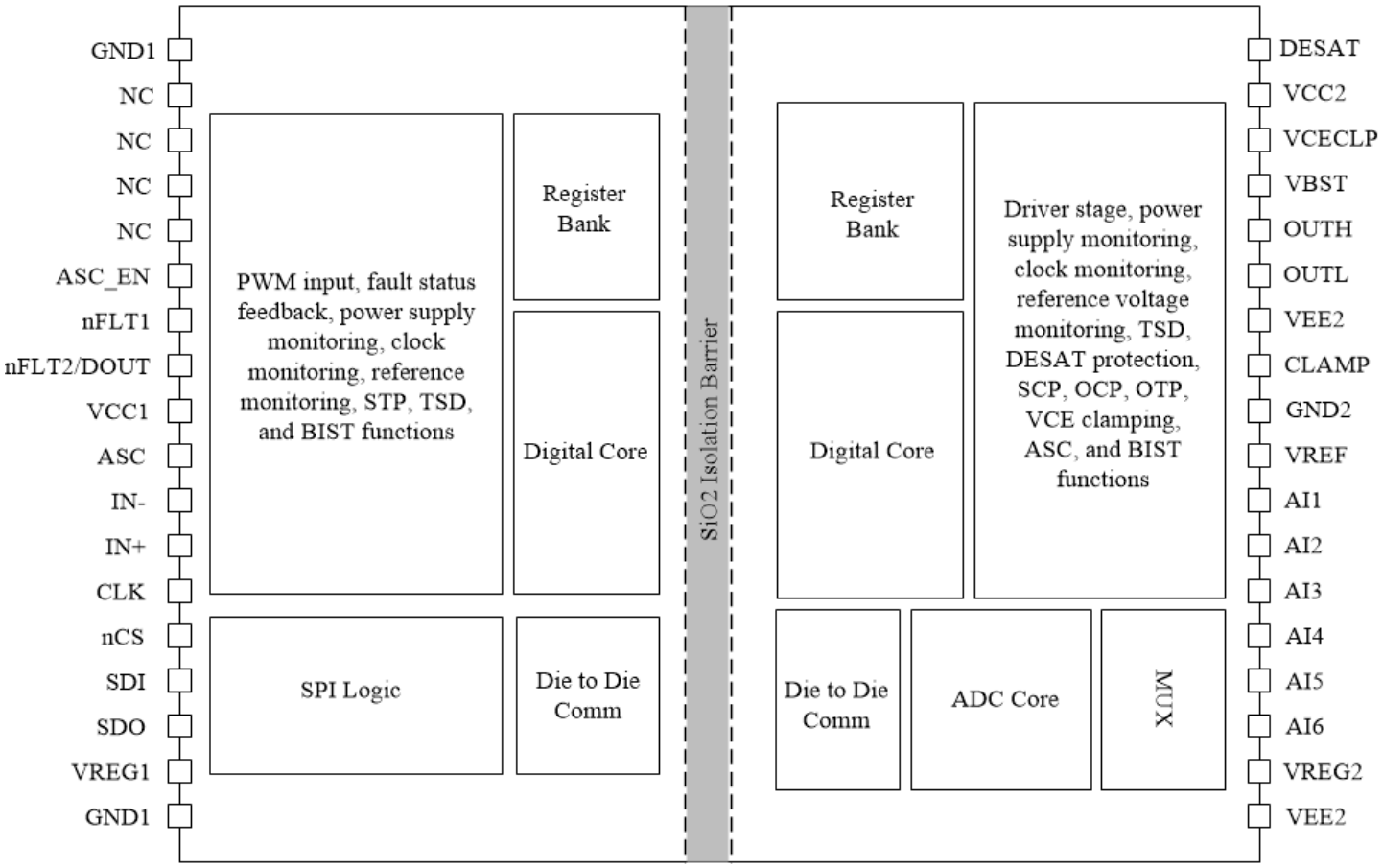
A 10-bit ADC is built-in to the UCC5870-Q1 to provide information on power switch temperature, gate driver temperature, or any voltage that must be monitored on the secondary (high-voltage) side of the gate driver. There are six inputs (AIx) available to measure voltages with the ADC. This is convenient for acquire information on the DC-LINK voltage, or for measuring the VCE/VDS voltage of the power transistor during operation. The ADC features "center mode" operation to ensure low noise measurements, or can be used in a traditional "edge mode" to achieve as many measurements as possible during a PWM cycle. In addition to reading back the ADC information over SPI, a DOUT function provides a feedback signal representing one of the user-selected AIx voltages that can be monitored real-time on the primary side.

The UCC5870-Q1 integrates many safety diagnostics that enable designers to more easily implement an ASIL rated system. There are diagnostics for all of the protection features, as well as latent fault detection for circuits in the gate driver IC itself. The faults are indicated using open-drain outputs, and the specific fault is easily determined using the SPI readback. In addition to all of the safety diagnostic features, the IC integrates a primary side and secondary side "active short circuit" circuits to provide the system designer with a secondary path to control a zero-vector state for the traction inverter in the case of motor controller failure.

注

Throughout the document, "*" are used as wild cards (typically to indicate numbers such as AI* means AI1 - AI6. Additionally, SPI bits are referred to in the following convention: REGNAME[BITNAME]

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supplies

The device uses three external supplies for power. VCC1 supplies the low voltage primary side that interfaces with the controller. VCC2 and VEE2 provide the gate drive supplies for the power FET. In addition, there are 3 integrated supplies (VREG1, VREG2, and VREF) used to power internal circuits.

7.3.1.1 VCC1

VCC1 supports an input range of 3V to 5.5V in order to support both 3.3V and 5V controller signaling. VCC1 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC1 are recorded in STATUS2[UVLO1_FAULT] and STATUS2[OVLO_FAULT1], respectively(STATUS2). See the Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) section for more specifics regarding the OV and UV functions.

7.3.1.2 VCC2

VCC2 operates within an input range of 15V and 30V, allowing for use in IGBT and SiC applications. VCC2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC2 are recorded in STATUS3[UVLO2_FAULT] and STATUS3[OVLO2_FAULT], respectively (STATUS3). See the Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) section for more specifics regarding the OV and UV functions.

7.3.1.3 VEE2

VEE2 operates with an input range of -12V to 0V, allowing a negative gate bias on the power FET during turn-off in both IGBT and SiC applications. This prevents the power FET from unintentionally turning on due to current

inducted from the Miller effect. For operation with a unipolar supply, connect VEE2 to GND2. VEE2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VEE2 are recorded in STATUS3[UVLO3_FAULT] and STATUS3[OVLO3_FAULT], respectively (STATUS3). See the Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) section for more specifics regarding the OV and UV functions.

7.3.1.4 VREG1

VREG1 is internally generated from VCC1. VREG1 regulates to 1.8V, and supplies internal circuits on the primary side. VREG1 requires a 4.7µF bypass capacitance from VREG1 to GND1 for proper operation. The current out of VREG1 is limited and this current limit is monitored. If the current limit is active for the deglitch time, a internal regulation overcurrent fault is recorded in STATUS2[VREG1_ILIMIT_FAULT]. If unmasked, nFLT1 goes low. Additionally, VREG1 is monitored for both undervoltage and overvoltage conditions. Any VREG1 UV fault is recorded in STATUS2[INT_REG_PRI_FAULT] (STATUS2). Any OV condition on VREG1 causes the VREG1 output to latch off and shuts down the device. This action results in a secondary communication failure, which shuts down the driver output according to CFG10[FS_STATE_INT_COMM_SEC] bit (CFG10). The VCC1 and VCC2 power must be recycled in order to restart the device.

7.3.1.5 VREG2

VREG2 is internally generated from VCC2. VREG2 regulates to 1.8V with respect to VEE2, and supplies internal circuits on the secondary side. VREG2 requires a 4.7µF bypass capacitance from VREG2 to VEE2 for proper operation. The current out of VREG2 is limited and this current limit is monitored. If the current limit is active for the deglitch time, a internal regulation overcurrent fault is recorded in STATUS3[VREG2_ILIMIT_FAULT] (STATUS3). If unmasked, nFLT1 goes low. Additionally, VREG2 is monitored for both undervoltage and overvoltage conditions. Any VREG2 OV/UV faults are recorded in STATUS3[INT_REG_SEC_FAULT] (STATUS3). Any OV condition on VREG2 causes the VREG2 output to latch off and shuts down the driver output. The VCC2 power must be recycled in order to restart the driver output. Additionally, the driver must be reconfigured to ensure correct operation.

7.3.1.6 VREF

VREF is the reference for the ADC. VREF requires a 4V supply for the ADC to function properly. The error of the VREF translates directly to the error at the ADC. VREF is selectable to be powered internally, or alternatively, an external precision reference may be used to enhance the accuracy of the ADC. Use the CFG8[VREF_SEL] (CFG8) bit to select between the internal and external reference. The current out of VREF is limited and this current limit is monitored. If the current limit is active for the deglitch time, a internal regulation overcurrent fault is detected. Additionally, VREF is monitored for both undervoltage and overvoltage conditions. When any VREFILIM and/or OV/UV faults occur, the faults are recorded in STATUS5[ADC_FAULT] (STATUS5). If unmasked, nFLT1 goes low.

7.3.1.7 Other Internal Rails

There are several internal rails that are used to power the device. All of the internal rails are monitored for OV and UV conditions. Any OV/UV faults are recorded in the STATUS2[INT_REG_PRI_FAULT] (STATUS2) and STATUS3[INT_REG_SEC_FAULT] (STATUS3) bits.

Bootstrap (VBST) and charge pump circuits generate the 4.5V power supply for the high side NMOS of internal driver stage. The implementation diagram is shown in 図 7-1. The external cap on BST is charged to 4.5V while OUTL is on (MN2 is on). While OUTH is on (MN1 is on), the capacitor voltage is stacked above OUTH and supplies the gate drive for the high-side NMOS. Under most conditions, the bootstrap circuit is used and the timing operates as shown in 図 7-2. However, for slow switching frequencies at high duty cycles the external capacitor may not be able to charge enough during the OUTH off time to supply the gate drive for the entire on-time. In these conditions, the charge pump circuit is used to hold the voltage across the bootstrap capacitor. .

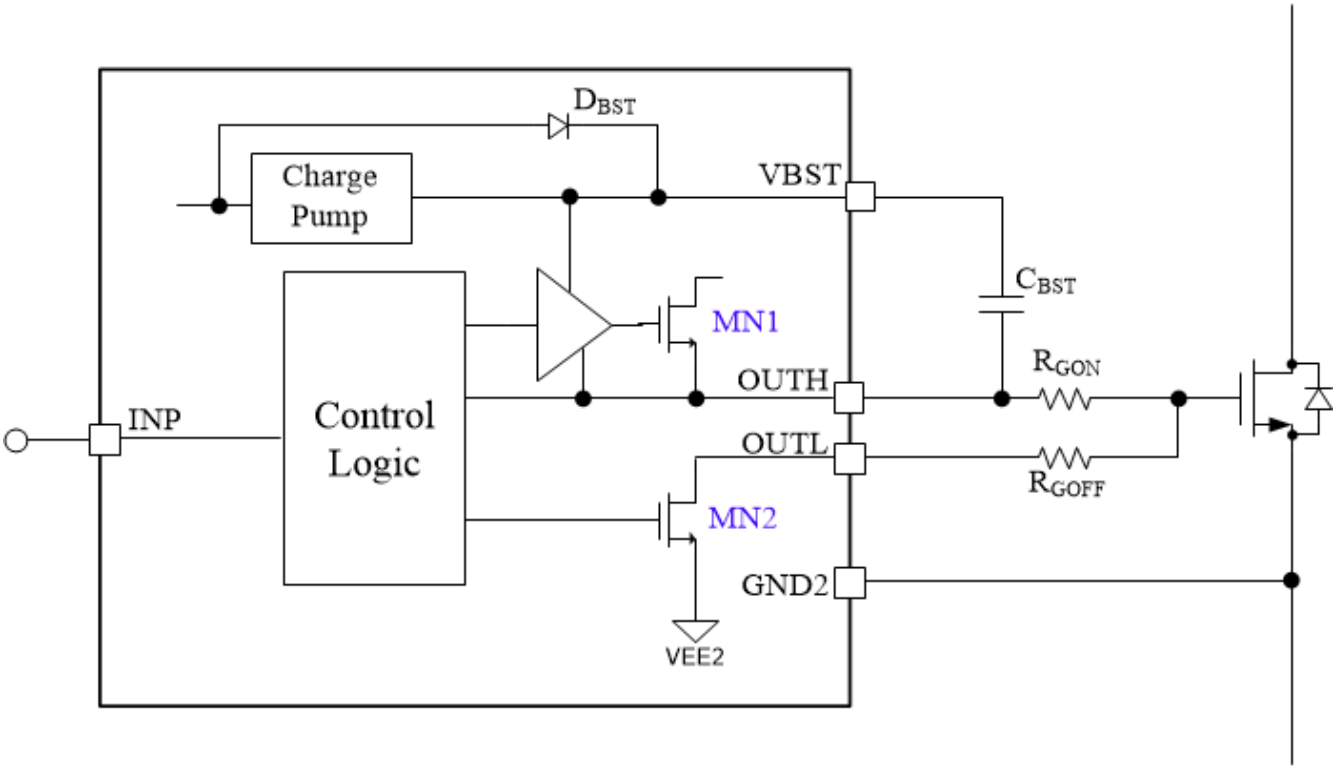


図 7-1. Implementation diagram of bootstrap and charge pump circuits.

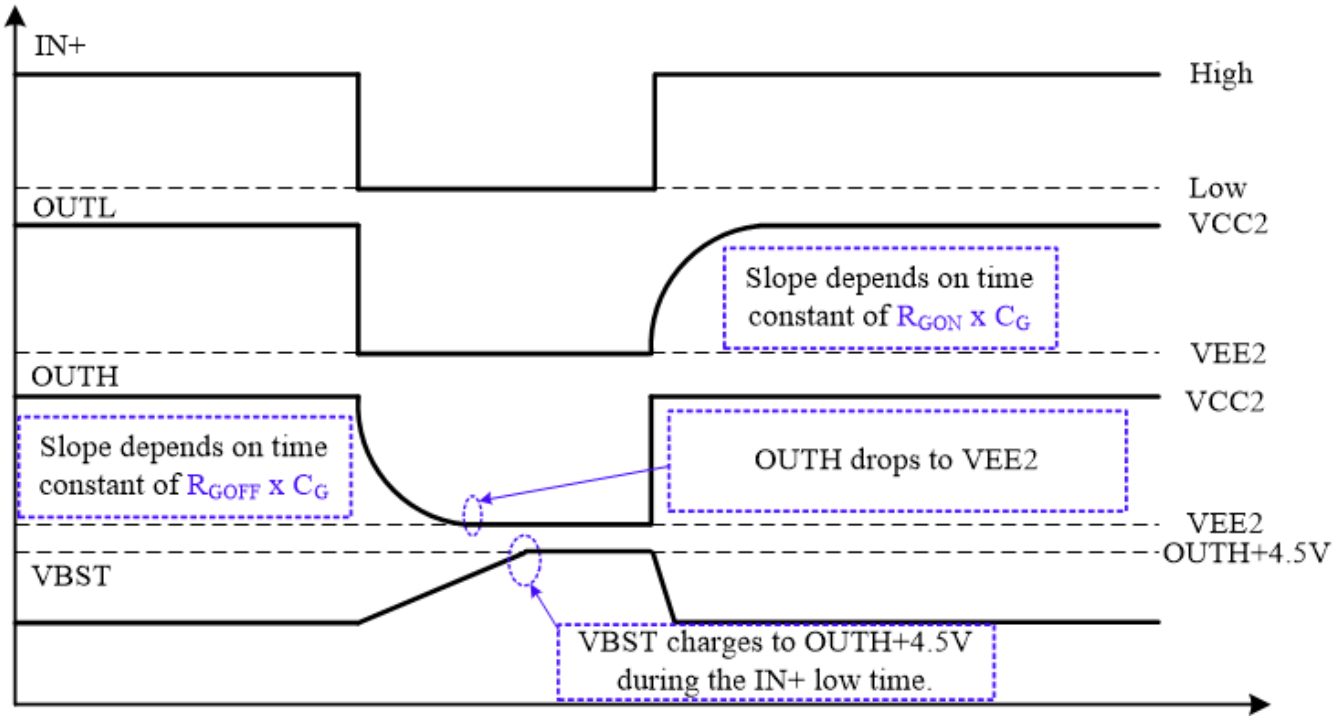


図 7-2. Timing diagram of bootstrap circuit.

7.3.2 Driver Stage

The driver stage is an integrated, 30-A current buffer. The high output drive capability enables the device to directly drive power transistors with current ratings up to 1000A without an external buffer. The drive strength is

selectable to 16.7%, 33%, or 100% using CFG8[IOUT_SEL] (CFG8). The output drive is split, enabling users to customize rise and fall times independently. .

7.3.3 Integrated ADC for Front-End Analog (FEA) Signal Processing

A 10bit ADC is integrated to enable the user to digitally monitor up to 6 analog input voltages (AI*). Additionally, the junction temperature of the device is available as well as an input for measuring the VTH of the power FET. The ADC has a full scale voltage range of 0 to 3.6V, requiring 4V at VREF (either internal or external). The ADC conversions are aligned with the INP signal to ensure the least amount of noise coupling from the switching transients of the power transistors (TI proprietary). Once a conversion is complete, the conversion results are transferred to the primary side of the device with inter-die communication and the result is stored in the ADCDATA* registers. The last ADC result is always available in the register. Every ADC conversion is recorded with time stamp information for that conversion. The time stamp is the INP cycle where the measurement occurs. Once the ADC and the driver are enabled, the time stamp increments with every INP low to high edge. If a fault occurs, or the duty cycle is such that a transition is not seen on INP, the TIME_STAMP does not update.

$$V_{AI*} = V_{ADC} \text{ (in decimal)} \times 3.519\text{mV} \quad (1)$$

$$\text{Die Temperature (C)} = V_{ADC}\text{(in decimal)} * 0.7015°\text{C} - 198.36 \quad (2)$$

The AI* inputs are configurable by the user to enable/disable bias currents and comparator monitoring AI1, AI3, and AI5 are specially designed to monitor the temperature diode that is integrated into the power FET module, while A2, A4, and A6 are designed to measure the power FET current, typically from an integrated sense FET in the module. However, the inputs are not required to be used in these functions, and are configurable to measure any voltage up to 3.6V regardless of the source. The implementation of ADC sensing circuits is presented in 図 7-3.

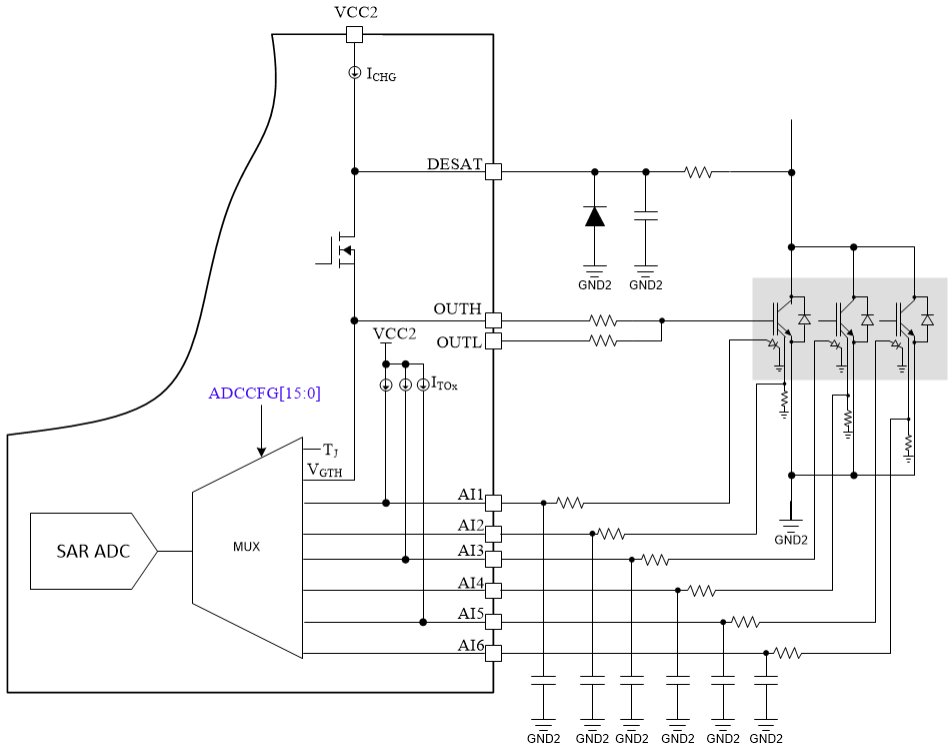


図 7-3. Block diagram of implementation of ADC processing for the case where three power transistors are connected in parallel.

7.3.3.1 AI* Setup

AI5 and AI6 are dual purpose inputs. By default, these inputs are configured to be control inputs for the secondary side ASC function (see the ASC section for more details). If AI5 and AI6 are to be used as current sense/ temperature sense/ ADC inputs, write CFG8[AI_ASC_MUX] = 1 (CFG8) to disable the ASC functionality. All of the AI* inputs have current sources that may be enabled using the CFG3[ITO1_EN] bit (CFG3) for AI1,3,5 and the CFG3[ITO2_EN] bit (CFG3) for the AI2,4,6. Additionally, the AI1, AI3, and AI5 inputs are designed with a zero-temperature coefficient bias current (IZTC) to bias the NTC diodes integrated into the external power switch module. Use CFG3[AI_IZTC_SEL] bits (CFG3) to enable the required bias currents for the application. The AI* inputs require an RC filter for most accurate results. See the セクション 8.2.2.6 section for details on selecting the correct RC values.

7.3.3.2 ADC Setup and Sampling Modes

The ADC is enabled/disabled with SPI communication to CFG7[ADC[ADC_EN] (CFG7). The 6 AI inputs as well as the die junction temperature are selectable to measure with the ADC. Additionally, the channels are selectable as to when it is samples with respect to the INP switching cycle. Use the ADCCFG[ADC_ON_CH_SEL_*] bits (ADCCFG) to select the channels to be measured while INP is high. The sampling order for the PWM ON cycle round robin is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp. Use the ADCCFG[ADC_OFF_CH_SEL_*] bits () to select the channels to be measured while INP is low. Use the CFG7[ADC_SAMP_MODE] bits (ADCCFG) to select one of 3 sampling modes for the ADC. Three modes are available to ensure the least amount of switching noise in the measurement. The three modes are Center Aligned mode (CFG7[ADC_SAMP_MODE]=0b00), where each selected channel is sampled in the center of the ON/OFF time of the INP input (depending on the setting), Edge Mode (CFG7[ADC_SAMP_MODE] = 0b01), where the ADC conversions begin after rising or falling edge (depending on the setting), and Hybrid mode (CFG7[ADC_SAMP_MODE] = 0b10), which is a combination of both modes. The maximum INP frequency supported in order to get at least one full ADC conversion per PWM cycle is 30kHz.

7.3.3.2.1 Center Sampling Mode

When using Center sampling mode (CFG7[ADC_SAMP_MODE]=0b00), the center is calculated for the ON or OFF time on INP (depending on the channel selection setup) based on the previous switching cycle. One channel is sampled during each ON or OFF time depending on the channel selections. The timing for Center mode is illustrated in the following figures.

Center mode scheduling with independent high/low phase channel selection registers

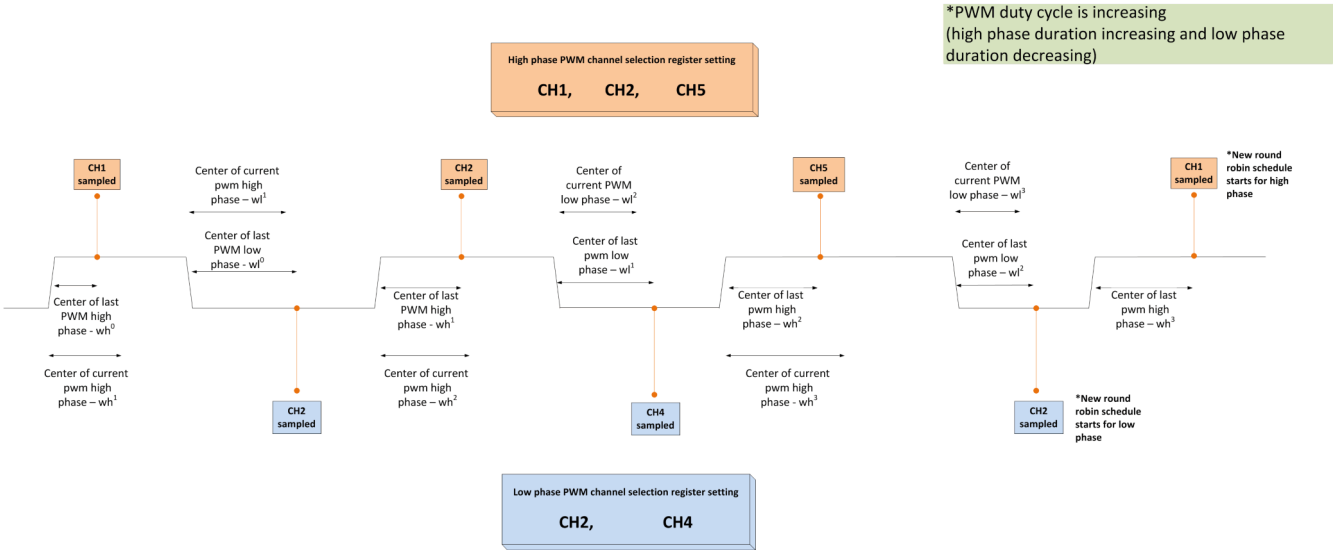


図 7-4. ADC center sampling mode

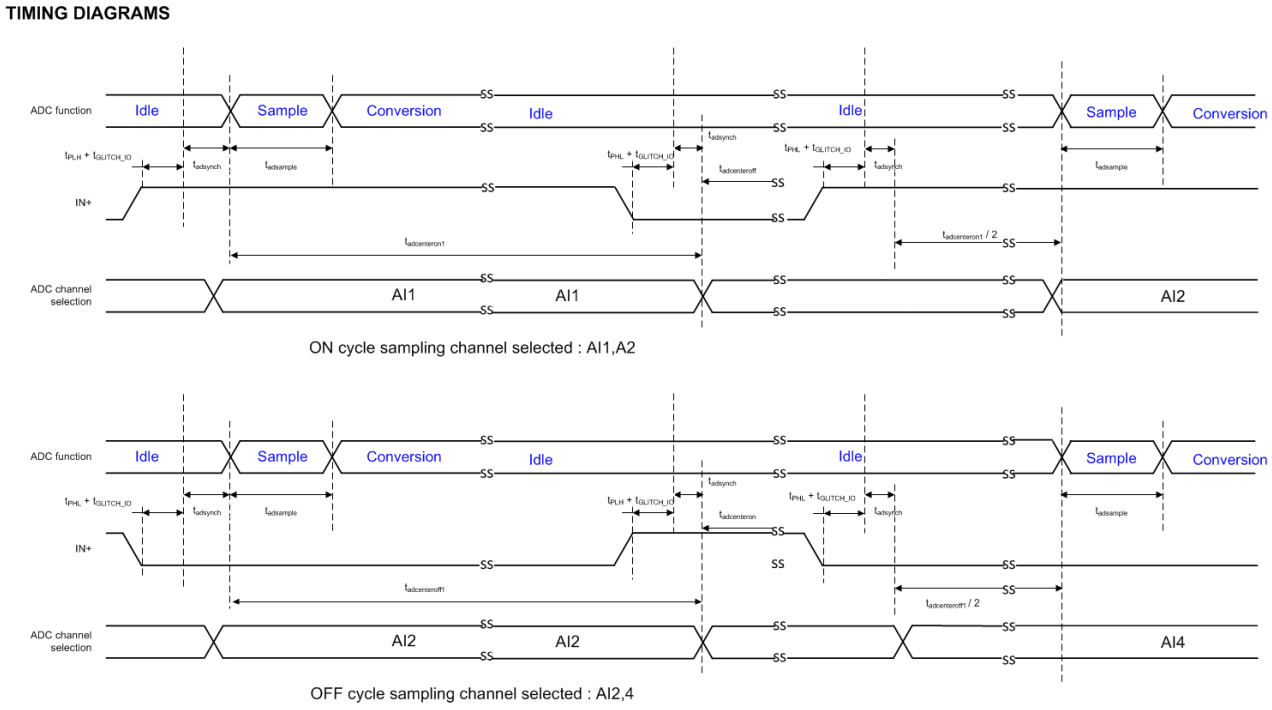


図 7-5. ADC center sample mode timing chart

7.3.3.2.2 Edge Sampling Mode

Edge Mode (CFG7[ADC_SAMP_MODE] = 0b01) begins the ADC conversions based on the INP edge. When INP transitions, the ADC begins conversions for the round robin after the programmable delay time (programmed using CFG7[ADC_SAMP_DLY]). The channels selected for the PWM ON time are sampled after a

rising edge of INP, while the channels selected for the PWM OFF time are sampled after a falling edge. The round robin continues until the next edge of INP. The timing for Edge mode is illustrated in the following figures.

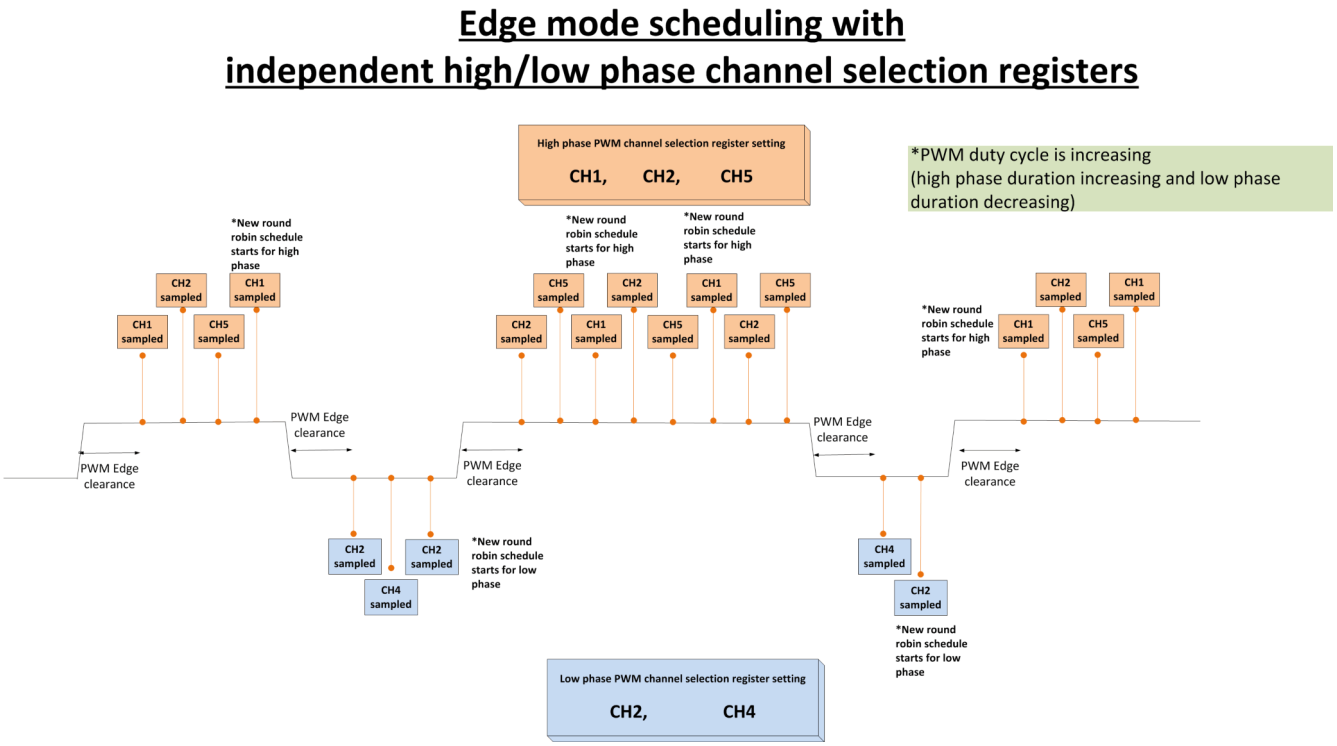


図 7-6. ADC edge sampling mode

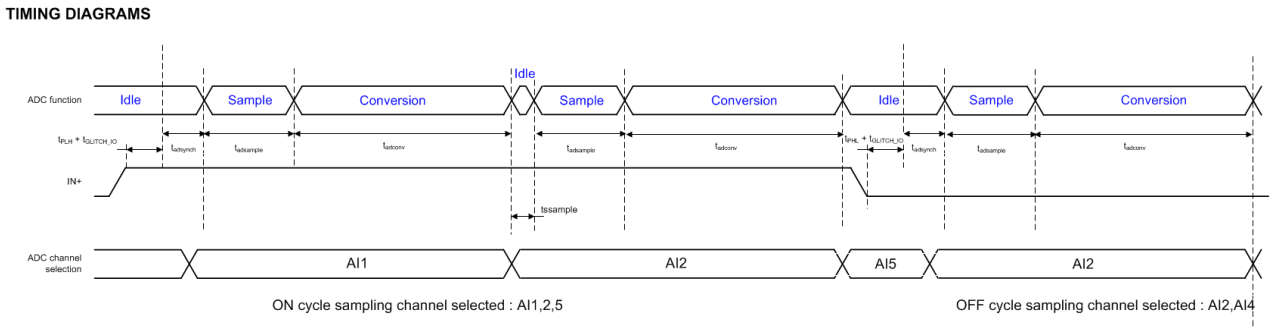


図 7-7. ADC Edge sampling mode timing chart

7.3.3.2.3 Hybrid Mode

Hybrid Mode (CFG7[ADC_SAMP_MODE]=0b10) operates using a combination of the modes. Center mode is used until the INP period is greater than the hybrid period (t_{hybrid}) when edge mode is used. The timing for Hybrid mode is illustrated in the following figures.

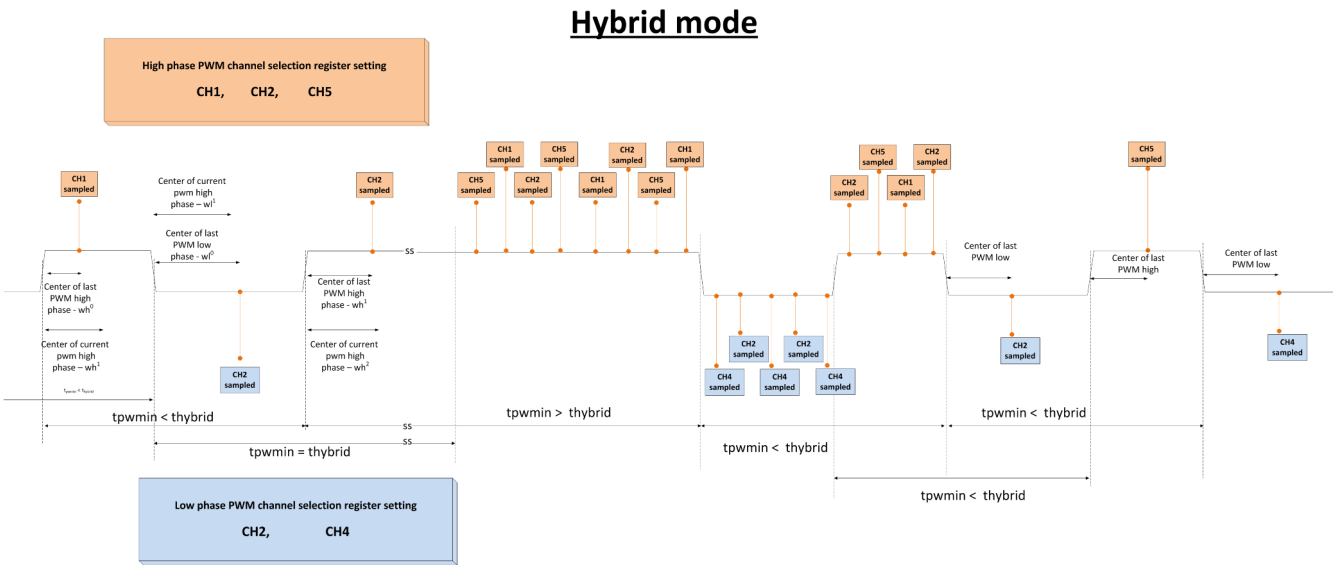


図 7-8. ADC Hybrid sampling mode timing chart

7.3.3.3 DOUT Functionality

The device also provides an analog feedback functionality for the ADC for applications that do not want to maintain continuous SPI communication. When enabled, the DOUT output provides a PWM signal with a duty cycle proportional to the signal that is selected to be monitored. Any of the AI* inputs and the TJ are available for monitoring on the DOUT output. As there is only one DOUT output, only one channel is selectable. Typically, DOUT is either directly monitored by the MCU, or run through an RC filter to convert it to an analog voltage that may be digitized and monitored by the host controller.

In order to use the DOUT function, the nFLT2 pin must be reconfigured to select the DOUT functionality using the CFG1[NFLT2_DOUT_MUX] bit (CFG1). When the DOUT mode is selected, any warning or fault that was selected to report to nFLT2 now reports to nFLT1 automatically. Additionally, the frequency of DOUT is selectable between 4 options using the DOUTCFG[FREQ_DOUT] bits (DOUTCFG). Select the channel to be monitored, using the DOUTCFG[DOUT_TO_AI*] bits (for the AI* inputs, DOUTCFG) or the DOUTCFG[DOUT_TO_TJ] bit (DOUTCFG) for the die junction temperature. If multiple channels are selected in the register, the duty cycle constantly changes as the ADC cycles through each channel read. It is recommended to only select one channel at a time for the DOUT function. In addition to this setup, the ADC must be enabled and setup correctly to read the desired channel to be monitored. See the ADC section for details on configuring the ADC. If a fault occurs that stops the driver output and ADC measurements, the DOUT output continues and represents the last good ADC reading.

7.3.4 Fault and Warning Classification

The device integrates extensive error detection and monitoring features. These features allow the design of a robust system that protects against a variety of system related failure modes. When one of the monitored warnings or faults occurs, if unmasked, the nFLT1 output (for faults) or the nFLT2 output (for warnings) pulls low. All of the fault and warning bits have corresponding configuration bits that allow the user to mask the error or fault from showing up on the nFLT* output. The naming convention is straightforward. The mask bit is in a CFG* register and is named the same as the fault with the addition of an "_P". For example, a power FET short circuit current fault is indicated in the register bit STATUS3[SC_FAULT] (STATUS3)and the mask bit is CFG9[SC_FAULT_P] (CFG9). Throughout this document, the different warning/error bit locations are indicated in the functional description of the block where the warning/fault is monitored. When masked, the nFLT* indication does not occur, but the STATUS* bits still indicate the warning/fault condition. The device classifies error events into two categories, Warnings and Faults, and takes different device actions depending on the error classification.

The Warning error class is used to report non-critical fault conditions. Warning errors are only reported with no action taken to affect the gate driver output or any other block. When a warning condition occurs, it is reported in on of the STATUS* registers and, if unmasked, the nFLT2 output is driven low. The nFLT2 indication for warning is cleared by a successful SPI read of the corresponding status register. Once cleared, warning indication is not repeated until the warning condition is removed and reapplied. For example, in an over temperature warning condition, after reading/clearing the bit the temperature must cool down to the normal operating range and then heat up again to the over temperature warning threshold for the error flag to be reasserted. The status bit always indicates the current state of the warning, and is not cleared until the error condition is removed.

The Fault error class is used to report critical fault conditions. Fault errors have the ability to shut down the gate driver when they occur. When a fault condition occurs, it is reported in one of the STATUS* registers and, if unmasked, the nFLT1 output is driven low. Many faults have a corresponding configuration bit that enables the user to select the functional safe state of the driver when that fault occurs when the fault is not masked. These bits are in the CFG* registers, with bit names that start with "FS_STATE_". Throughout this document, the FS_STATE locations are indicated in the functional description of the block where the fault is monitored. The available options for the output state, depending on the fault, are PL (OUTL pulled low), PH (OUTH pulled high), or no action (gate driver output ignores the fault and continues normal operation). Faults are cleared when the condition is removed, and the CONTROL2[CLR_STAT_REG] bit (CONTROL2) is written. Fault indication reasserts as long as the fault condition exists and is unmasked. 表 7-1 provides an extensive list and details for the available faults and warnings.

表 7-1. Fault and Warning Operating Modes (default)

NAME(1)	INDICATOR BIT	DRIVER OUTPUT (Default Action and Control bit)	SPI	nFLT1 (Default Action and Control bit)	nFLT2	Recovery operation
UVLO of VCC1 fault	STATUS2[UVLO1_FAULT] = 1	PL CFG3[FS_STATE_UVLO1_FAULT]	D (Not latched. SPI is re-enabled if VCC1 voltage is above the UV threshold)	Assert CFG2[UVLO1_FAULT_P]	-	System (MCU) to re-configure the device. Rewrite all SPI configurable registers.
OVLO of VCC1 fault	STATUS2[OVLO1_FAULT] = 1	PL CFG3[FS_STATE_OVLO1_FAULT]	D(Not latched. SPI is re-enabled if VCC1 voltage is below the OV threshold)	Assert CFG2[OVLO1_FAULT_P]	-	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
UVLO of VCC2 fault	STATUS3[UVLO2_FAULT] = 1	PL CFG11[FS_STATE_UVLO2]	E	Assert CFG9[UVLO23_FAULT_P]	-	System (MCU) to re-configure the device. Rewrite all SPI configurable registers.
OVLO of VCC2 fault	STATUS3[OVLO2_FAULT] = 1	PL CFG11[FS_STATE_OVLO2]	E	Assert CFG9[OVLO23_FAULT_P]	-	System (MCU or other controller) to cycle VCC2 and re-configure the device. Rewrite all SPI configurable registers.
UVLO of VEE2 fault	STATUS3[UVLO3_FAULT] = 1	PL CFG11[FS_STATE_UVLO3]	E	Assert CFG9[UVLO23_FAULT_P]	-	CLR_STAT_REG=1
OVLO of VEE2 fault	STATUS3[OVLO3_FAULT] = 1	PL CFG11[FS_STATE_OVLO3]	E	Assert CFG9[OVLO23_FAULT_P]	-	CLR_STAT_REG=1
Driver IC over temperature warning	STATUS1[GD_TWN_PRI_FAULT] = 1 (primary) STATUS4[GD_TWN_SEC_FAULT] = 1 (secondary)	NA	E	-	Assert CFG2[GD_TWN_PRI_FAULT_P]	-
Driver IC over temperature shutdown fault (secondary)	STATUS4[GD_TSD_SEC_FAULT] = 1 Additionally, the STATUS2[CLK_MON_PRI_FAULT] 1 and STATUS2[INT_COMM_PRI_FAULT] indicate faults	PL	E	Assert CFG9[GD_TSD_FAULT_P]	-	System to cycle VCC2 power and re-configure the device after allowing the device to cool. Rewrite all SPI configurable registers.
Driver IC over temperature shutdown fault (primary)	-	PL	D	-	-	System to re-configure the device. Rewrite all SPI configurable registers.
Power transistor over current fault	STATUS3[OC_FAULT] = 1	PL CFG10[FS_STATE_OCP]	E	Assert CFG9[OC_FAULT_P]	-	CLR_STAT_REG=1
Power transistor short circuit fault	STATUS3[SC_FAULT] = 1 or STATUS3[DESAT_FAULT] = 1	PL CFG10[FS_STATE_DESAT_SCP]	E	Assert CFG9[SC_FAULT_P]	-	CLR_STAT_REG=1

表 7-1. Fault and Warning Operating Modes (default) (continued)

NAME(1)	INDICATOR BIT	DRIVER OUTPUT (Default Action and Control bit)	SPI	nFLT1 (Default Action and Control bit)	nFLT2	Recovery operation
Power transistor over temperature fault	STATUS3[PS_TSD_FAULT] = 1	PL CFG10[FS_STATE_PS_TSD]	E	Assert CFG9[PS_TSD_FAULT_P]	-	CLR_STAT_REG=1
Gate voltage monitor fault	STATUS3[GM_FAULT] = 1	HiZ CFG10[FS_STATE_GM]	E	Assert CFG9[GM_FAULT_P]	Not Asserted CFG9[GM_FAULT_P]	CLR_STAT_REG=1
PWM shoot through fault and STP diagnostic	STATUS2[STP_FAULT] = 1	PL CFG3[FS_STATE_STP_FAULT]	E	Assert CFG2[STP_FAULT_P]	-	CLR_STAT_REG=1
Clock monitor fault (primary)	STATUS4[CLK_MON_SEC_FAULT] = 1	PL CFG11[FS_STATE_CLK_MON_SEC_FAULT]	D(Not latched. SPI is re-enabled if the clock recovers)	Assert CFG2[CLK_MON_SEC_FAULT_P]	-	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
Clock monitor fault (secondary)	STATUS2[CLK_MON_PRI_FAULT] = 1	PL	E	Assert CFG2[CLK_MON_PRI_FAULT_P]	-	System (MCU or other controller) to cycle VCC2 and re-configure the device. Rewrite all SPI configurable registers.
Internal regulator UVLO fault	STATUS2[INT_REG_PRI_FAULT] = 1 (priamry) STATUS3[INT_REG_SEC_FAULT] = 1 (secondary)	PL CFG3[FS_STATE_INT_REG_PRI_FAULT] (primary) CFG10[FS_STATE_INT_REG_SEC_FAULT] (secondary)	E	Assert CFG2[INT_REG_PRI_FAULT_P]	-	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
Internal regulator OVLO fault	STATUS2[INT_REG_PRI_FAULT] = 1 (primary) STATUS3[INT_REG_SEC_FAULT] = 1 (secondary)	PL CFG3[FS_STATE_INT_REG_PRI_FAULT] (primary) CFG10[FS_STATE_INT_REG_SEC_FAULT] (secondary)	E	Assert CFG2[INT_REG_PRI_FAULT_P]	-	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
VREG1 OVLO fault	-	Results in a secondary internal communication fault. See the internal communication fault line for behavior	D	Assert	-	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
VREG2 OVLO fault	-	Results in ia primary internal communication fault. See the internal communication fault line for behavior	E	Results in a primary internal communication fault. See the internal communication fault line for behavior	-	System (MCU or other controller) to cycle VCC2 and re-configure the device. Rewrite all SPI configurable registers.
SPI clock fault	STATUS2[SPI_FAULT] = 1	NA CFG3[FS_STATE_SPI_FAULT]	E	Not Asserted CFG2[SPI_FAULT_P]	Assert CFG2[SPI_FAULT_P]	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
SPI address fault	STATUS2[SPI_FAULT] = 1	NA CFG3[FS_STATE_SPI_FAULT]	E	Not Asserted CFG2[SPI_FAULT_P]	Assert CFG2[SPI_FAULT_P]	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
SPI CRC fault	STATUS2[SPI_FAULT] = 1	NA CFG3[FS_STATE_SPI_FAULT]	E	Not Asserted CFG2[SPI_FAULT_P]	Assert CFG2[SPI_FAULT_P]	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
Configuration register CRC fault	STATUS2[CFG_CRC_PRI_FAULT] = 1 (primary) STATUS4[CFG_CRC_SEC_FAULT] = 1 (secondary)	PL CFG3[FS_STATE_CFG_CRC_PRI_FAULT] (primary) CFG10[FS_STATE_CFG_CRC_SEC_FAULT] (secondary)	E	Assert CFG2[CFG_CRC_PRI_FAULT_P] (primary) CFG9[CFG_CRC_SEC_FAULT_P] (secondary)	-	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
TRIM CRC fault	STATUS2[TRIM_CRC_PRI_FAULT] = 1 (primary) TRIM_CRC_SEC_FAULT = 1 (secondary)	PL Always PL (primary) CFG11[FS_STATE_TRIM_CRC_SEC_FAULT] (secondary)	E	Assert CFG2[CFG_CRC_PRI_FAULT_P] (primary) CFG9[CFG_CRC_SEC_FAULT_P] (secondary)	Assert CFG2[CFG_CRC_PRI_FAULT_P] (primary) CFG9[CFG_CRC_SEC_FAULT_P] (secondary)	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
Clock monitor BIST fault	STATUS2[BIST_PRI_FAULT] = 1 (primary) STATUS4[BIST_SEC_FAULT] = 1 (secondary)	PL	E	Assert CFG2[BIST_PRI_FAULT_P] (primary) CFG9[BIST_SEC_FAULT_P] (secondary)	Assert CFG2[BIST_PRI_FAULT_P] (primary) CFG9[BIST_SEC_FAULT_P] (secondary)	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.

表 7-1. Fault and Warning Operating Modes (default) (continued)

NAME(1)	INDICATOR BIT	DRIVER OUTPUT (Default Action and Control bit)	SPI	nFLT1 (Default Action and Control bit)	nFLT2	Recovery operation
Analog BIST fault	STATUS2[BIST_PRI_FAULT] = 1 (primary) STATUS4[BIST_SEC_FAULT] = 1 (secondary)	PL	E	Assert CFG2[BIST_PRI_FAULT_P] (primary) CFG9[BIST_SEC_FAULT_P] (secondary)	Assert CFG2[BIST_PRI_FAULT_P] (primary) CFG9[BIST_SEC_FAULT_P] (secondary)	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
Internal Communication fault (primary)	STATUS2[INT_COMM_PRI_FAULT]=1	PL CFG3[FS_STATE_INT_COMM_PRI_FAULT]	E	Not Asserted CFG2[INT_COMM_PRI_FAULT_P]	-	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
Internal Communication fault (secondary)	STATUS3[INT_COMM_SEC_FAULT]=1	PL CFG10[FS_STATE_INT_COMM_SEC_FAULT]	E	Asserted CFG9[INT_COM M_SEC_FAULT_P]	-	System (MCU or other controller) to cycle VCC1/VCC2 and re-configure the device. Rewrite all SPI configurable registers.
PWM check fault	STATUS1[PWM_COMP_CHK_FAULT] = 1	PL CFG3[FS_STATE_PWM_CHK]	E	Assert CFG2[PWM_CHK_FAULT_P]	-	
VREF UV/OV fault	STATUS5[ADC_FAULT] = 1	NACFG7[FS_STATE_ADC_FAULT]	E	Not Asserted CFG7[ADC_FAULT_P]	-	System (MCU or other controller) to cycle VREF bias and write CLR_STAT_REG=1
VCE over voltage fault	STATUS3[VCEOV_FAULT] = 1	STO	E	-	-	-
VREG1 overcurrent fault	STATUS2[VREG1_ILIMIT_FAULT] = 1	NA	E Very likely that this fault causes a VREG1 UV which disbles SPI	Assert CFG2[VREG1_ILIMIT_FAULT_P]	-	System (MCU or other controller) to cycle VCC1 and re-configure the device. Rewrite all SPI configurable registers.
VREG2 overcurrent fault	STATUS3[VREG2_ILIMIT_FAULT] = 1	NA	E	Assert CFG9[VREG2_ILIMIT_FAULT_P]	-	System (MCU or other controller) to cycle VCC2 and re-configure the device. Rewrite all SPI configurable registers.
VREF overcurrent fault	STATUS5[ADC_FAULT] = 1	NA	E	Assert CFG7[ADC_FAULT_P]	-	System (MCU or other controller) to cycle VREF bias and write CLR_STAT_REG=1

(1) E - Enabled, PL = Pull Low, D = Disabled, HiZ = High Impedance, NA - No Action, STO - Soft Turn-Off

7.3.5 Diagnostic Features

Diagnostics are available covering the following functions:

- Undervoltage and overvoltage monitoring on VCC1, VCC2, and VEE2 power supplies
- Undervoltage and overvoltage monitoring on internal power supplies used for its supporting circuits
- Clock monitor on logic clock
- Configuration Data CRC
- SPI CRC
- TRIM RC
- Built-in self-test (BIST) diagnostics for VCC1, VCC2, VEE2, and internal regulator UV/OV monitoring functions, and main clocks.
- DESAT detection function and function diagnostic
- Power transistor OCP, SCP, and TSD comparators and comparator diagnostics
- Power transistor high voltage clamping circuit detection and function diagnostics
- Active Miller clamp diagnostic

7.3.5.1 Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO)

UVLO functions are implemented for all three gate driver power supplies VCC1, VCC2, and VEE2. The VCC1 UVLO/OVLO ensures a valid supply is connected for the required logic interface. The UVLO/OVLO for VCC2 and VEE2 ensures valid supplies based on the type of transistor used. The UVLO function prevents overheating damage to the IGBTs/MOSFETs from being under-driven. The OVLO functions are implemented to prevent gate oxide degradation (shortened lifetime) of the IGBTs/MOSFETs from an over-voltage supply at turned on. The device powers up when a valid VCC1 supply ($V_{IT+(UVLO1)}$ < V_{VCC1} < $V_{IT+(OVLO1)}$) and non-UV VCC2 supply (V_{VCC2} > $V_{IT+(UVLO2)}$) are connected. The driver outputs are high impedance until the valid supplies are connected and the internal supplies are in regulation. While the driver output is high impedance, the output to the gate of the external power switch is held low with a passive and active pulldown circuit. See the セクション 7.3.5.2 section for more details. Once valid supplies are connected and internal supplies are valid, the output state is determined by the Enable/Disable Driver command any fault conditions that exist. SPI communication is unavailable while VCC1 is lower than the UVLO1 threshold.

The OVLO and UVLO functions are enabled/disabled using the following bits: CFG1[UV1_DIS] for VCC1 UVLO, CFG1[OV1_DIS] for VCC1 OVLO, CFG4[UV2_DIS] for VCC2 UVLO,CFG4[OV2_DIS] for VCC2 OVLO, and CFG4[UVOV3_EN] for both the OVLO and UVLO for VEE2. The UVLO and OVLO thresholds for VCC1, VCC2 and VEE2 are programmable in order to customize the driver for different types of power transistors. Use the CFG1[UVLO1_LEVEL] and CFG1[OVLO1_LEVEL] (for VCC1), CFG7[UVLO2TH] and CFG7[OVLO2TH] (for VCC2), and CFG7[UVLO3TH] and CFG7[IOVLO3TH] (for VEE2) bits to set the desired threshold. See CFG1 and CFG7.

The fault status for the OVLO and UVLO function are located in STATUS2[UVLO1_FAULT] for VCC1 UVLO, STATUS2[OVLO1_FAULT] for VCC1 OVLO, STATUS3[UVLO2_FAULT] for VCC2 UVLO, STATUS3[OVLO2_FAULT] for VCC2 OVLO, STATUS3[UVLO3_FAULT] for VEE2 UVLO, and STATUS3[OVLO3_FAULT] for VEE2 OVLO. See STATUS2 and STATUS3 for additional details. The timing diagrams for the VCC1 and VCC2 UVLO and OVLO functions are shown in and 図 7-10, respectively. The VEE2 timing diagram is shown in 図 7-11.

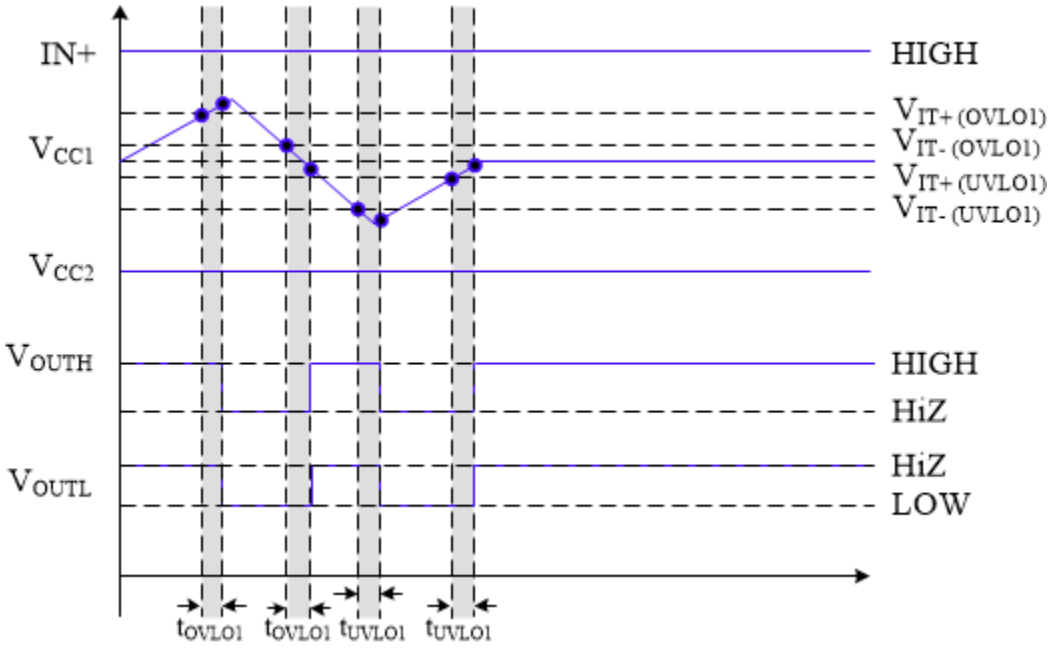


図 7-9. Illustration of UVLO and OVLO timing schemes of VCC1.

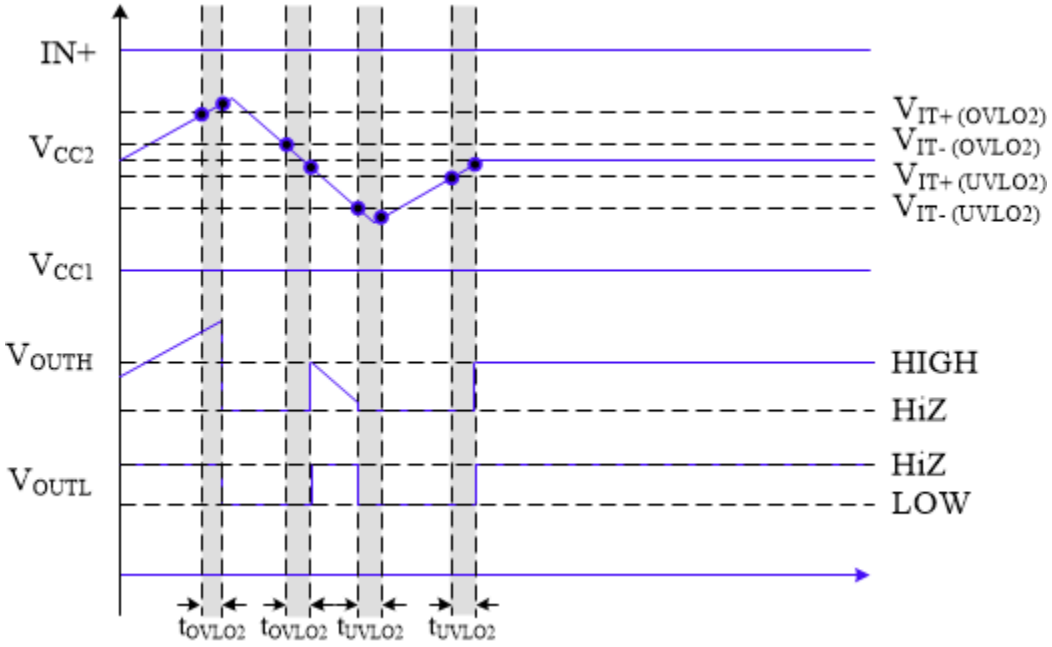


図 7-10. Illustration of UVLO and OVLO timing schemes of VCC2

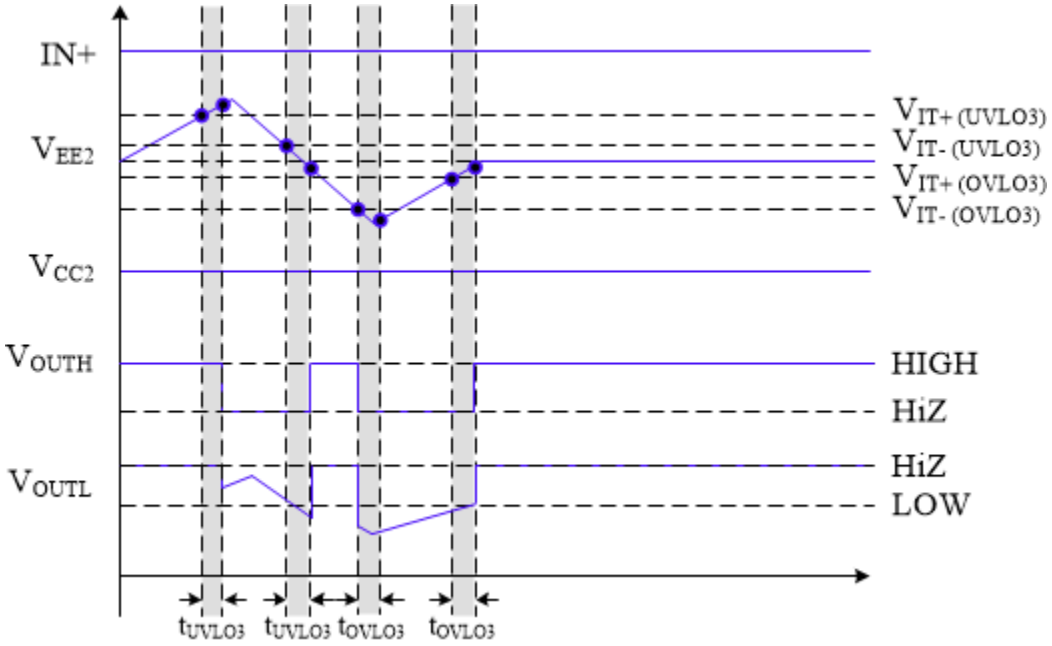


図 7-11. Illustration of UVLO and OVLO timing schemes of VEE2

7.3.5.1.1 Built-In Self Test (BIST)

7.3.5.1.1.1 Analog Built-In Self Test (ABIST)

The device automatically runs diagnostics on all of the under-voltage and over-voltage comparators monitoring VCC1, VCC2, VEE2, and internal regulators during the power up process. During the self-test of the comparators, an over-voltage and under-voltage condition is simulated. The actual monitored voltage rails remain unchanged and the disturbance is not observable. A failure in the ABIST for the primary side sets the STATUS2[BIST_PRI_FAULT] (STATUS2) and for the secondary side sets the SATUS4[BIST_SEC_FAULT] (STATUS4).

7.3.5.1.1.2 Function BIST

In addition to the automatic analog BIST, there are BIST diagnostics available for DESAT, the PWM signal (INP) check, STP, Gate Voltage Monitoring, SCP/OCP, PS_TSD, and VCECLP. Details for the functionality of each of these tests are provided in the CONTROL1 (CONTROL1) and CONTROL2 (CONTROL2) register bit descriptions.

7.3.5.1.1.3 Clock Monitor

The device integrates clock monitor functions to identify clock faults during operation. The Clock monitor detects internal oscillator failures:

- Oscillator clock stuck high or stuck low
- Clock frequency is out of range ±30%

The clock monitor is enabled during a power-up event after the power-on reset is released. The clocks on the primary side and secondary side are monitored. In the event of a clock fault on the primary side, the STATUS4[CLK_MON_SEC_FAULT] bit (STATUS4) is set, the driver is forced to the state determined by the CFG11[FS_STATE_CLK_MON_SEC_FAULT] bit (CFG11) and, if unmasked, the nFLT1 output pulls low. In the event of a clock fault on the secondary side, the STATUS2[CLK_MON_PRI_FAULT] bit (STATUS2) is set, and, if unmasked, the nFLT1 output pulls low. The secondary side clock monitor has no effect on the gate driver output state.

7.3.5.1.1.3.1 Clock Monitor Built-In Self Test

The clock monitor circuit integrates a diagnostic that checks the integrity of the monitoring circuit. The diagnostic is run automatically during the startup process. Additionally, a simulated clock monitor fault is generated by

writing the CONTROL1[CLK_MON_CHK_PRI] bit (図 7-72) for the primary side and the CONTROL2[CLK_MON_CHK_SEC] bit (図 7-73) for the secondary side. When enabled, the enabled diagnostics emulates clock failure that causes a clock monitor fault. During this self-test, the actual oscillator frequency is not changed.

7.3.5.2 CLAMP, OUTH, and OUTL Clamping Circuits

Integrated diodes prevent the OUTH and CLAMP outputs from exceeding VCC2. The short circuit clamping function clamps the voltages at the driver output (OUTH) and active Miller clamp (CLAMP) outputs to be slightly higher than VCC2 during power switch short circuit conditions. The clamped gate voltage limits the short circuit current and prevents the IGBT/MOSFET gate from overvoltage breakdown or degradation. The internal diodes conduct up to 500 mA current for a duration of 10us, and a continuous current of 20mA. Use external Schottky diodes to improve current conduction capability, if needed.

While VCC2 is unpowered, the gate of the external power switch is held off with an active pulldown circuit. If the OUTL suddenly rises due to ramping VCC2 during power up, the active pulldown function pulls the IGBT/MOSFET gate to the low state and maintains the OUTL voltage below V_{OUTSD}. See 図 7-12 for a drawing of the clamping circuits.

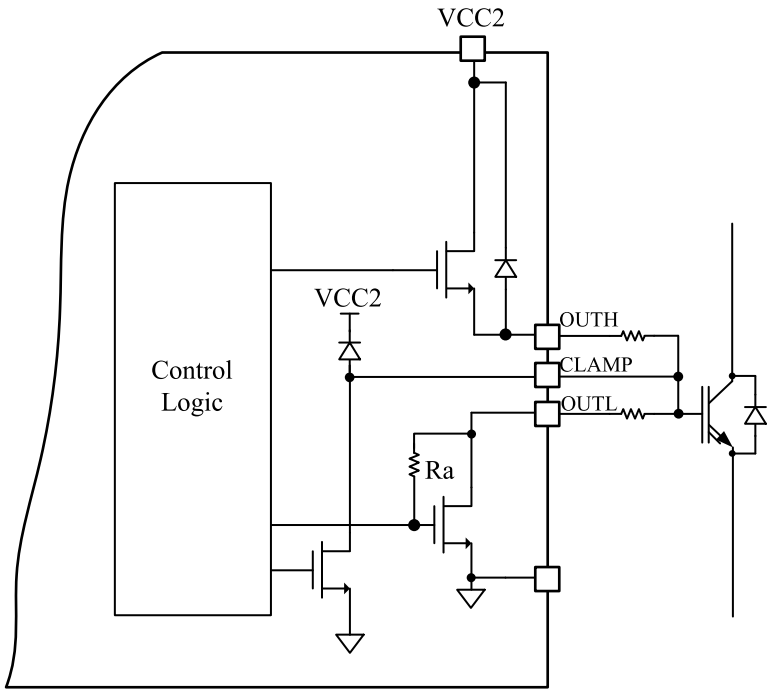


図 7-12. CLAMP, OUTH, and OUTL Clamping Circuits

7.3.5.3 Active Miller Clamp

The Active Miller clamp function (CLAMP output) is used to prevent the power transistor from false turn-on due Miller capacitance induced current. The active Miller clamp adds a low impedance path between power transistor gate terminal and VEE2 to pull the gate of the external FET hard to VEE2, bypassing any external gate resistors. The Miller clamp engages when the OUTH voltage falls below the V_{CLPTH}, which is selected using the CFG5[MCLPTH] bits (CFG5). Additionally, the Miller clamp is enabled/disabled using the CFG4[MCLP_DIS] bit (CFG4). The status of the Miller clamp is available in the STATUS3[MCLP_STATE] bit (STATUS3).

If additional pulldown strength is required, the CLAMP output is configured to drive an external Miller clamp FET. Use the CFG4[MCLP_CFG] bit to select between the internal and external Miller clamp (CFG4). This option can be configured through the register. The implementation block diagram and timing scheme are shown in 図 7-13 and 図 7-15 respectively.

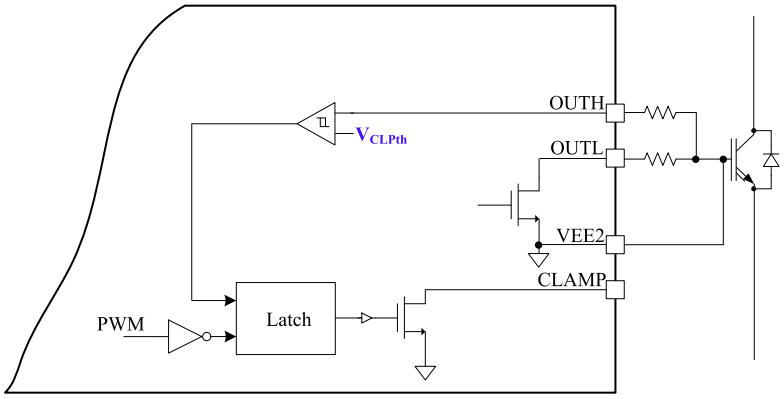


図 7-13. Block diagram of implementation of internal Miller clamp function.

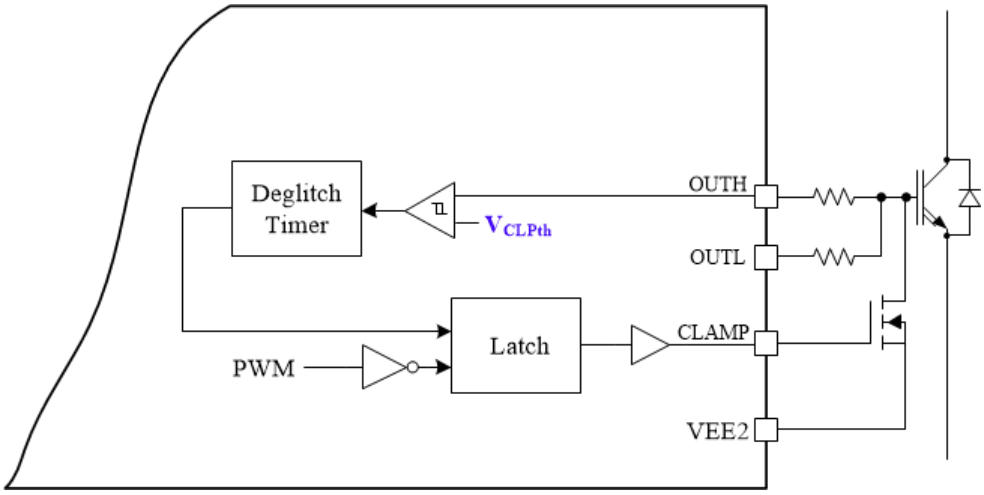


図 7-14. Block diagram of implementation of external Miller clamp function.

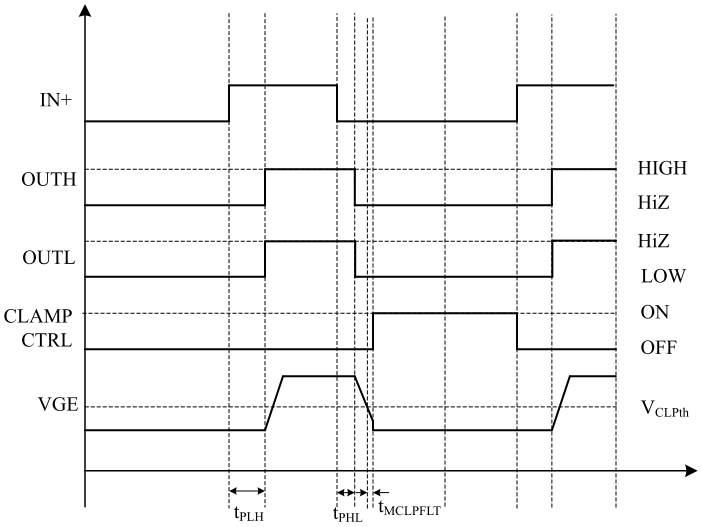


図 7-15. Timing scheme of implementation of Miller clamp function.

7.3.5.4 DESAT based Short Circuit Protection (DESAT)

DESAT protection prevents the power transistor from damage in case of short circuit faults. The DESAT input monitors the VCEsat (IGBT)/VDSon (MOSFET) through an external resistor and diode network (R1, C1, D1 and D2 in 図 7-16). The D1 diode protects the driver IC from high voltage when the power transistor is OFF. The resistor, R1, limits the negative voltage applied on the DESAT input during switching transitions. While the power FET is ON, an internal current source, I_{CHG}, forward biases the DESAT diode and dumps into the collector/drain of the external power switch. Under normal conditions, the V_{CEsat}/V_{DSon} is less than a few volts, however, during short circuit faults the V_{CEsat}/V_{DSon} may rise up to the DC bus voltage when the power transistor operates in the linear region. In this situation, the D1 diode is reverse biased, so the internal current source charges the blanking capacitor (C1) Once the voltage on the DESAT input charges up to the selected threshold ($V_{DESATth}$),the driver output is pulled into the safe state defined by the CFG10[FS_STATE_DESAT_SCP] bit (CFG10), the fault is indicated in the STATUS3[DESAT_FAULT] (STATUS3), and, if unmasked, the NFLT1 output pulls low. The turn-off of the driver output during a DESAT fault is selectable between normal, soft turn-off (STO), or two-level turnoff (2LTO) dictated by the CFG5[2LTOFF_STO_EN] bits (CFG5). See the セクション 7.3.5.9and セクション 7.3.5.8 for additional details on STO and 2LTO, respectively. The blanking capacitor is fully discharged at the falling edge of the PWM signal using the internal discharge current (I_{DCHG}). In addition to the blanking time, DESAT is deglitched to prevent false triggering during transitions. The deglitch is selectable using the CFG4[DESAT_DEGLITCH] bit (CFG4).

The DESAT threshold is selectable using the CFG5[DESATTH] bits (CFG5), and the DESAT charging current (I_{CHG}) is selectable, using the CFG5[DESAT_CHG_CURR] bits (CFG5), to control the blanking time (t_{DS_BLK}). The discharge current is enabled/disabled using the CFG5[DESAT_DCHG_EN] bit (CFG5). The DESAT protection function is enabled or disabled using the CFG4[DESAT_EN] bit (CFG4). The implementation diagram and timing schemes of DESAT based short circuit protection are presented in 図 7-16 and 図 7-17 respectively. See the セクション 8.3.1.1section for details on selecting the R1, C1, and D1 values.

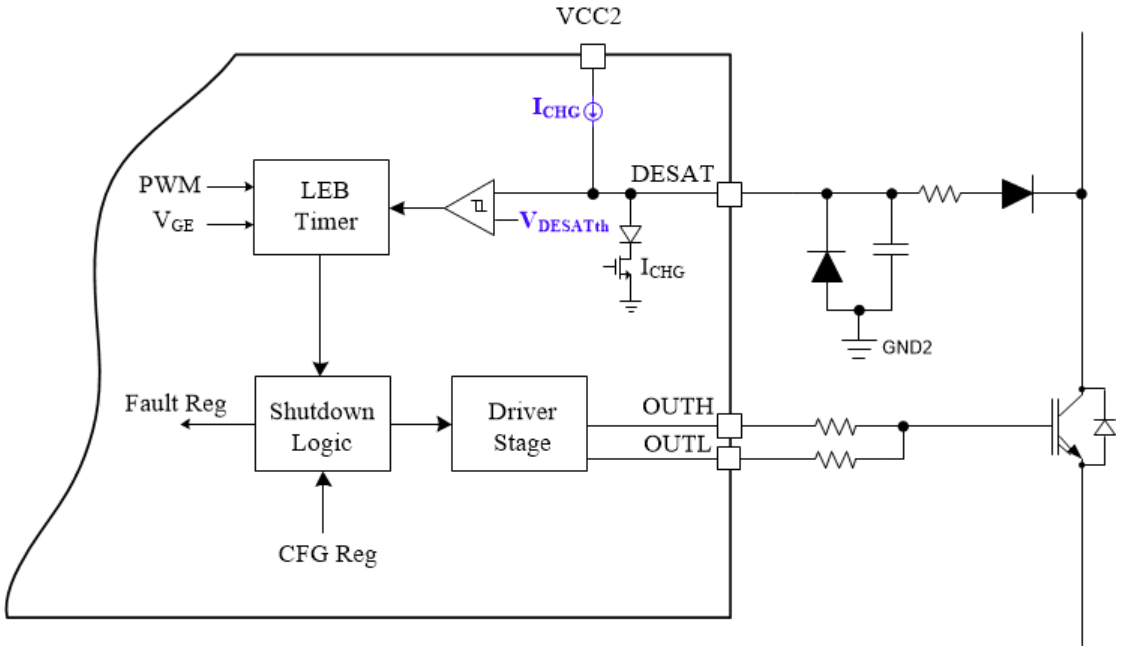


図 7-16. Block diagram of implementation of DESAT protection function.

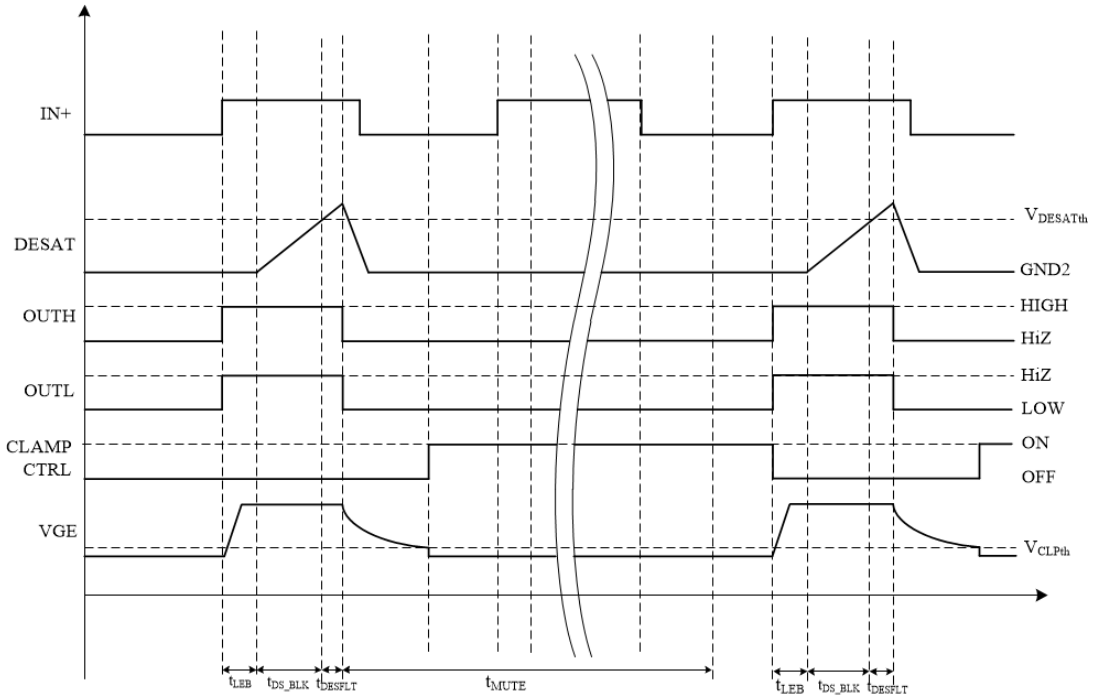


図 7-17. Timing scheme of implementation of DESAT protection function (safe state is LOW).

7.3.5.5 Shunt Resistor based Overcurrent Protection (OCP) and Short Circuit Protection (SCP)

The device designates three AI* inputs (AI2, AI4, AI6) to support shunt resistor based OCP and SCP in order to support up to three power transistors in parallel. Shunt resistor based OCP/SCP protections are intended for power transistors with integrated current sense FETs. The mirrored power transistor currents is fed into a resistor, and the voltage is monitored at the AI* input. Once the voltage at the AI* input exceeds the threshold programmed using CFG6[OCTH] (for OCP, CFG6) or CFG6[SCTH] (for SCP, CFG6), the fault is indicated in the STATUS3[OC_FAULT] (for OCP, STATUS3) or the STATUS3[SC_FAULT] (for SCP, STATUS3), and if unmasked, nFLT1x is pulled low and the driver output goes to the state defined by CFG10[FS_STATE_OCP] (for OCP, CFG10) or CFG10[FS_STATE_SCP] (for SCP, CFG10). The turn-off of the driver output during a OCP or SCP fault is selectable between normal, soft turn-off (STO), or two-level turnoff (2LTO) dictated by the CFG5[2LTOFF_STO_EN] bits (CFG5). See the Soft Turn-off (STO) and Two-Level Turn-Off for additional details on STO and 2LTO, respectively. A blanking time is used for both OCP and SCP to prevent unwanted false protection triggering during transitions and is selectable in CFG6[OC_BLK] (for OCP, CFG6)) or CFG6[SC_BLK] (for SCP, CFG6)). Once the blanking time expires, any SCP/OCP fault must exist for the deglitch time before the fault is registered. Enable/disable which AI* inputs are to be used for SCP/OCP using the DOUTCFG[AI*OCSC_EN] bits (DOUTCFG). The OCP and SCP functions are enabled for the selected AI* inputs using the CFG4[OCP_DIS] (for OCP, CFG4) and CFG4[SCP_DIS] (for SCP, CFG4) bits. Please note that if AI6 is to be used for OCP/SCP, the CFG8[AI_ASC_MUX] bit (CFG8) must be configured as an ADC input. The implementation diagram and timing schemes for the shunt resistor based OCP and SCP are presented in Block diagram of implementation of shunt resistor based OCP and SCP functions and Timing scheme of implementation of shunt resistor based OCP function (safe state is LOW) respectively.

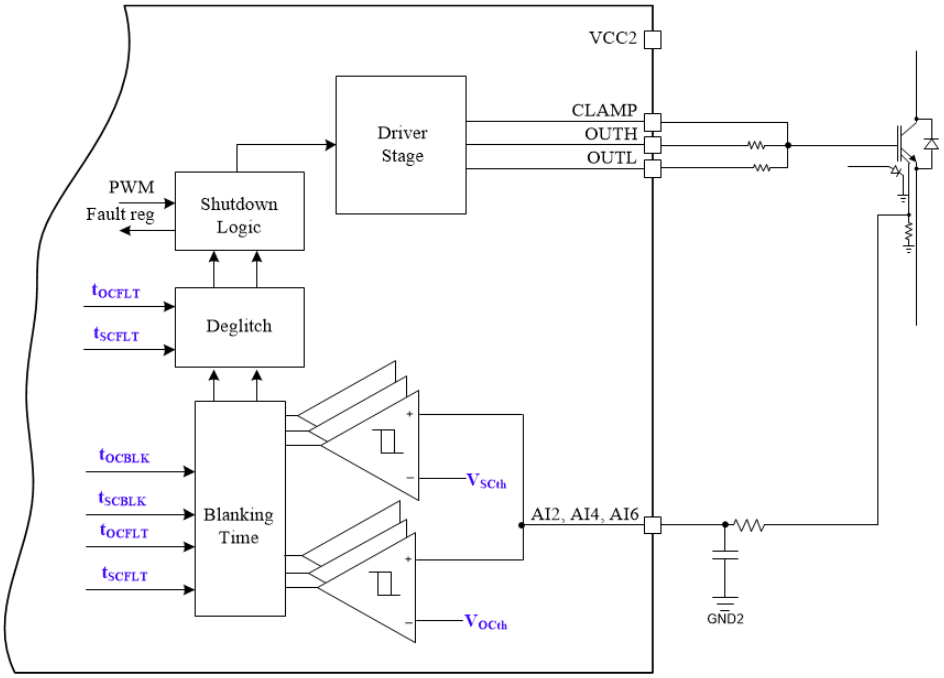


図 7-18. Block diagram of implementation of shunt resistor based OCP and SCP functions.

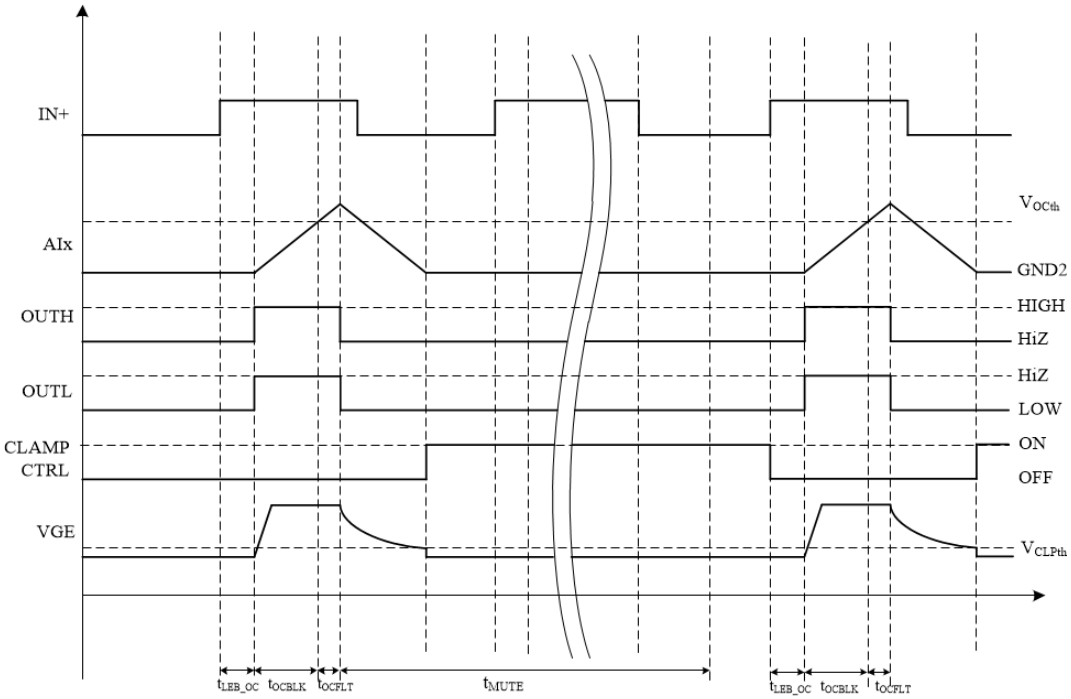


図 7-19. Timing scheme of implementation of shunt resistor based OCP function (safe state is LOW)

Current sources are available for AI2, AI4, and AI6 as open pin diagnosis tools. Enable the current sources using the CFG3[ITO2_EN] bit (CFG3). When enabled, the AI2, AI4, AI6 inputs are pulled high if left unconnected.

7.3.5.6 Temperature Monitoring and Protection for the Power Transistors

The device designates three AI* inputs (AI1, AI3, AI5) to support NTC diode sensing for up to three power transistors in parallel. The temperature protection is intended for power transistors with integrated temperature

sensing diodes. The AI* input provides a zero-TC current that biases the integrated diode, and the voltage is monitored at the AI* input. The bias current is controlled using CFG3[ITO1_EN] (CFG3) as a master enable, and then using CFG3[AI_IZTC_SEL] (CFG3) to select which AI* output is to receive the bias current. Once the voltage at the AI* input falls below the threshold programmed using CFG6[TSD_PS] (CFG6), the fault is indicated in the STATUS3[PS_TSD_FAULT] (STATUS3), and if unmasked, nFLT1 is pulled low and the driver output goes to the state defined by CFG10[FS_STATE_PS_TSD] (CFG10). The turn-off of the driver output during an PS_TSD fault is selectable between normal, soft turn-off (STO), or two-level turnoff (2LTO) dictated by the CFG5[2LTOFF_STO_EN] bits. See the セクション 7.3.5.9 and セクション 7.3.5.8 for additional details on STO and 2LTO, respectively. Any PS_TSD fault must exist for the deglitch time programmed using the CFG4[PS_TSD_DEGLITCH] bits (CFG4) before the fault is registered. Enable/disable which AI* inputs are to be used for PS_TSD using the DOUTCFG[AI*PS_TSD_EN] bits (DOUTCFG). The temperature monitoring function is enabled for the selected AI* inputs using the CFG4[PS_PS_TEMP_EN] bit (CFG4). Please note that if AI5 is to be used for power switch temperature monitoring, the CFG8[AI_ASC_MUX] bit (CFG8) must be configured as an ADC input. The implementation diagram and timing schemes of PS_TSD are presented in 図 7-20 and 図 7-21 respectively.

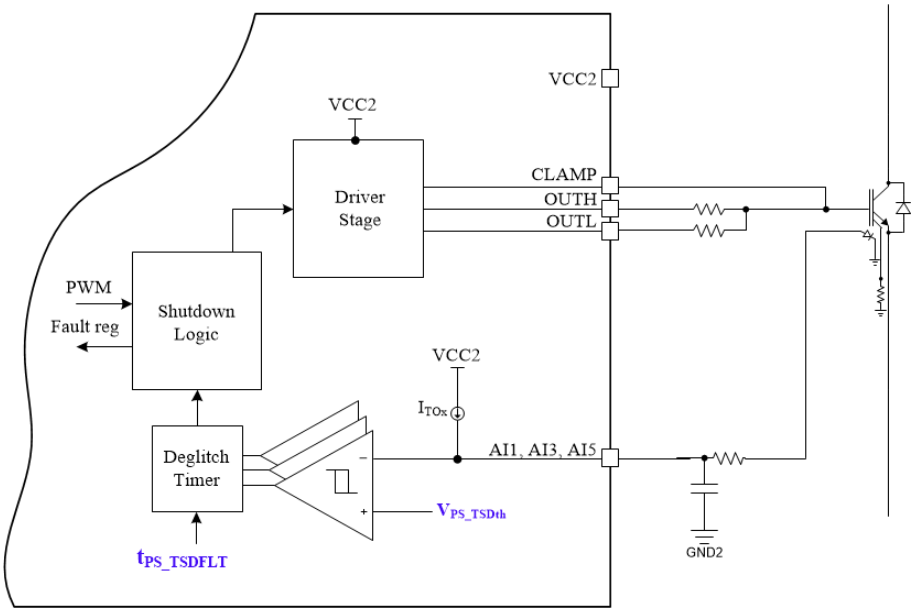


図 7-20. Block diagram of implementation of PS temperature monitoring function.

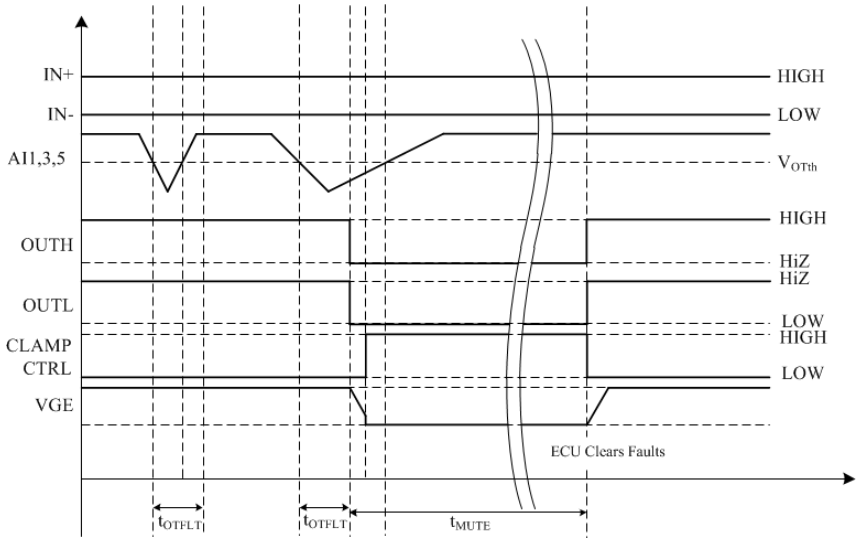


図 7-21. Timing scheme of implementation of PS_TSD function.

7.3.5.7 Active High Voltage Clamping (VCECLP)

The active high voltage clamping feature protects power transistors from over-voltage damage during switching transitions, while reducing the power dissipated in the external TVS clamp diodes protecting the power FET. During turn-off, the VCECLP input is monitored. Once the VCE of the FET increases to turn on the external TVS diode, the RC network on the VCECLP input is charged up. Once the VCECLP input reaches the clamp threshold ($V_{CECLPTH}$), OUTL drive strength changes to the I_{STO} setting in order to slow down the turn off and reduce the overshoot. The high voltage clamping remains active for a predefined time t_{VCECLP_HLD}. The OV condition is reported in STATUS3[VCEOV_FAULT] (STATUS3). The implementation and timing diagrams for the active high voltage clamping are presented in 図 7-22 and 図 7-23, respectively. The VCECLP feature is enabled/disabled using the CFG4[VCECLP_EN] bit (CFG4).

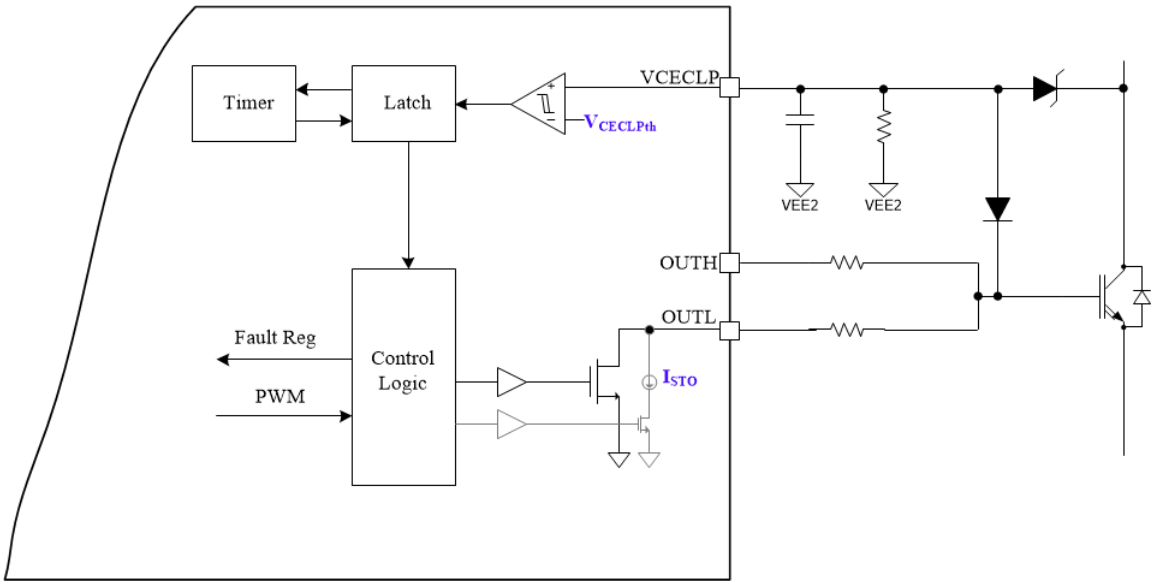


図 7-22. Block diagram of implementation of active high voltage clamping function.

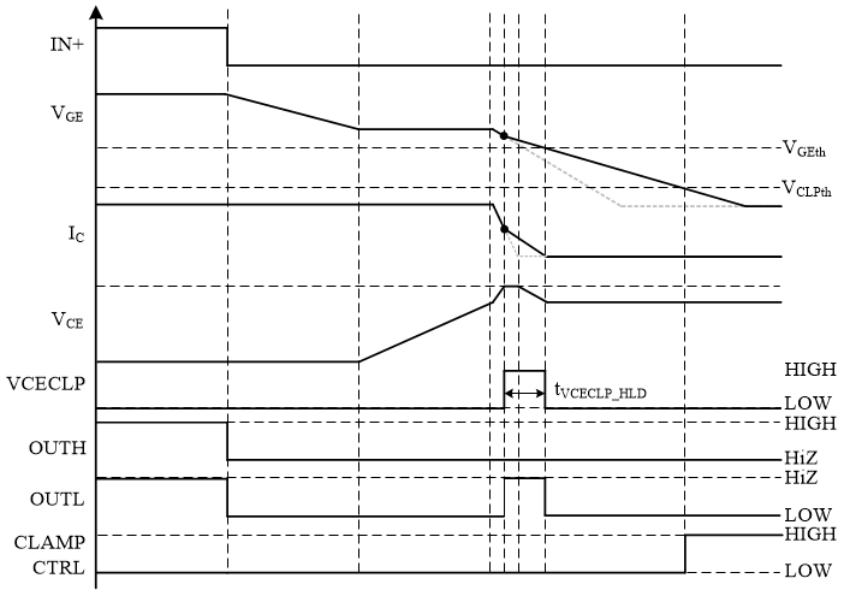


図 7-23. Timing scheme of implementation of active high voltage clamping function.

7.3.5.8 Two-Level Turn-Off

The two-level turn-off (2LTOFF) function limits the transistor current during shutoff during certain fault conditions. The 2LTOFF function is enabled for PS_OC, PS_SC, PS_TSD, and/or DESAT faults using the CF5[2LTOFF_STO_EN] bits (CFG5). When 2LTOFF is triggered, the gate of the power transistor is controlled to operate the transistor in the linear region where the channel current is controlled by the voltage level on the gate terminal. The power transistor current is reduced by controlling the gate voltage to a intermediate voltage, or plateau voltage, (V_{2LOFF}) for t_{2LOFF}, and then ramping the gate down to turn the power transistor off. While 2LTOFF is active, OUTL sinks current to discharge the gate capacitor of the power switch to the plateau voltage. The gate discharge current is programmable using the CFG8[GD_2LOFF_CURR] bits (CFG8). The plateau voltage level and duration are configured using the CFG8[GD_2LOFF_VOLT] and CFG8[GD_2LOFF_TIME] bits (CFG8), respectively. After holding the plateau voltage for the programmed time, the gate is discharged fully using the soft turn-off current or pulled low as normal with the OUTL driver. Enable the soft turn off current using the CFG8[GD_2LOFF_STO_EN] bit (CFG8). The implementation diagram and timing scheme are presented in 図 7-24 and 図 7-25, respectively.

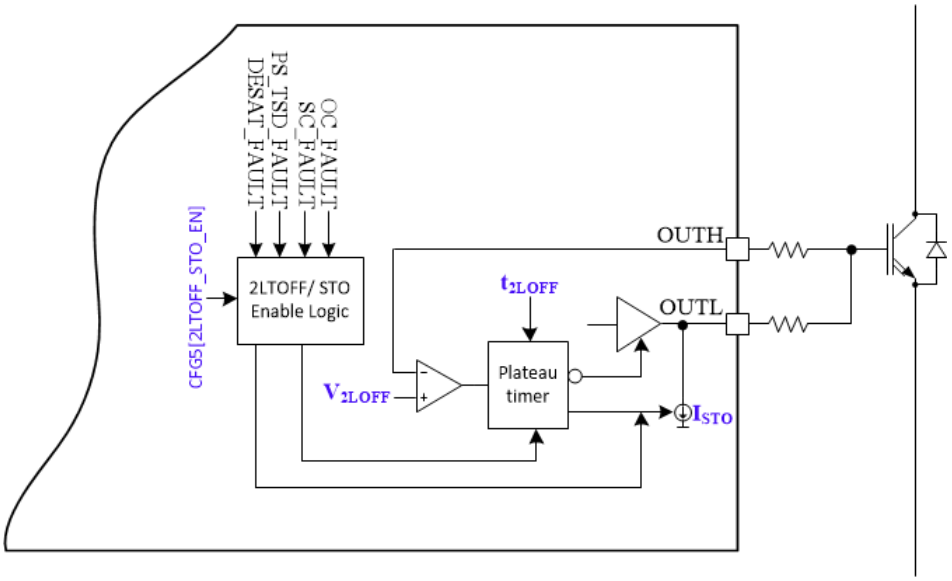


図 7-24. Block diagram of implementation of two-level turn-off function

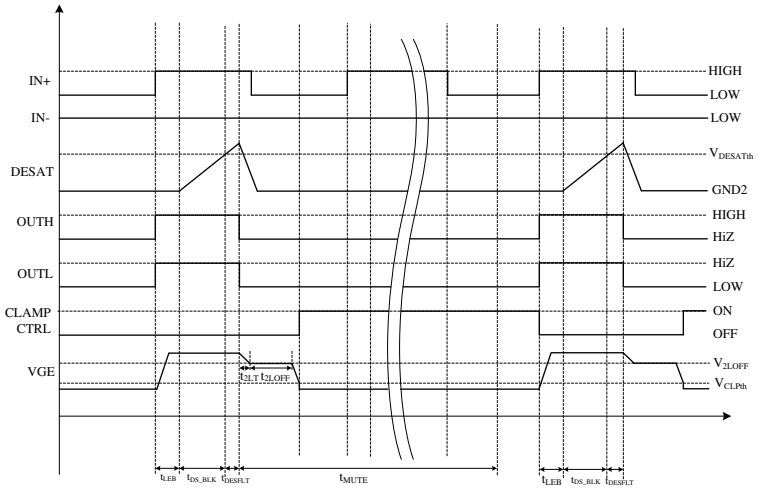


図 7-25. Timing scheme of implementation of two-level turn-off function

7.3.5.9 Soft Turn-Off (STO)

The soft turn-off (STO) function prevents power transistors from OV damage because of parasitic loop inductance induced voltage spikes on V_{CE}. The STO slows down the turn-off process that to limit the di/dt rate, and thus limits the loop inductance induced voltage spikes. During STO, the OUTL drive strength is reduced to the threshold programmed using the CFG5[STO_CURR] bits (CFG5). The STO function is enabled for PS_OC, PS_SC, PS_TSD, and/or DESAT faults using the CF5[2LTOFF_STO_EN] bits (CFG5).

7.3.5.10 Thermal Shutdown (TSD) and Temperature Warning (TWN) of Driver IC

Gate driver temperature monitoring prevents driver IC from damage during overheating conditions. Both the primary and secondary sides of the driver utilize thermal warning and shutdown comparators to help prevent damage due to high temperatures. When a thermal warning is detected on the primary side, the STATUS1[GD_TWN_PRI_FAULT] (STATUS1) is set and, if unmasked, the nFLT2 output is pulled low. If over temperature event is detected on the primary side, the device transitions to the RESET state where the driver output is held low. Once the device cools, the device must be reconfigured as described in the Programming section before enabling the driver output.

When a thermal warning is detected on the secondary side, the STATUS4[GD_TWN_SEC_FAULT](STATUS4) is set and, if unmasked, the nFLT2 output is pulled low. When a thermal shutdown is detected on the secondary side, the driver is disabled, , the STATUS4[GD_TSD_SEC_FAULT] (STATUS4), is set and, if unmasked, the nFLT1 output is pulled low. The status register flag for TSD may not be set depending on the timing of the thermal event, however the nFLT1 indicator will be pulled low. In the case of the secondary thermal shutdown event, the clock monitor and inter-die communication faults will likely be indicated. This is expected behavior due to the secondary side being shutdown and not communicating to the primary side. Once the driver cools and communication is reestablished, the device must be reconfigured as described in the Programming section before turning on the driver output. A blanking time is inserted to prevent unwanted false triggering of the protection circuits.

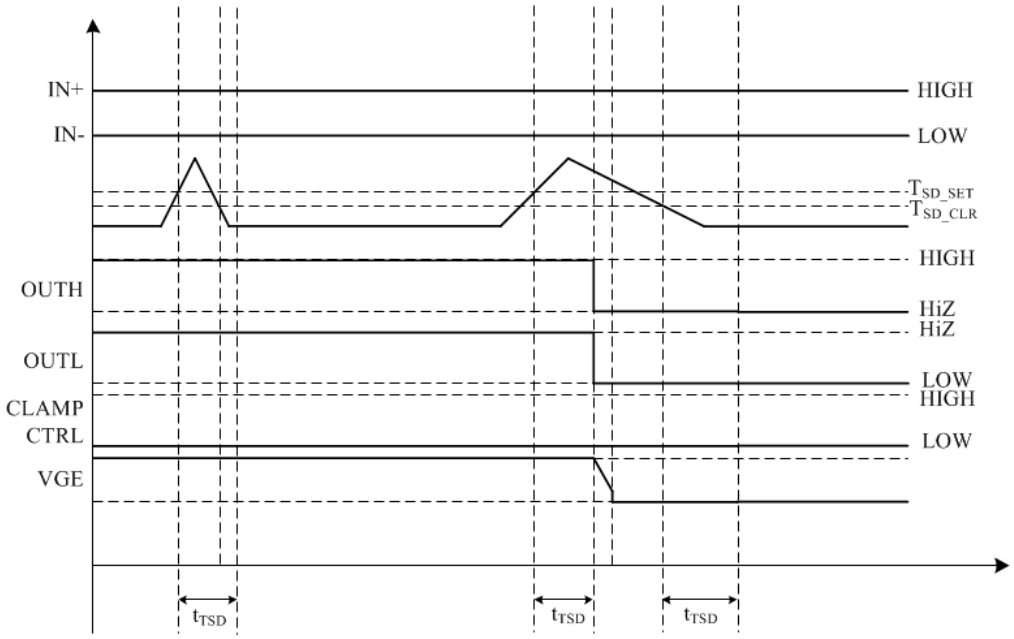


図 7-26. Timing scheme of implementation of driver IC TSD function.

7.3.5.11 Active Short Circuit Support (ASC)

The active short circuit (ASC) function allows the system to force the state of the power transistor regardless of the PWM input. For cases where the main MCU is not available due to fault or otherwise, a secondary control circuit drives the ASC_EN input high to force the output of the device to the state defined by the ASC input. For the primary side, two dedicated inputs are available for the ASC control. The ASC control is also available on the secondary side using the AI5 and AI6 inputs. To configure the device with the secondary ASC function, the CFG8[AI_ASC_MUX] bit (CFG8) must be configured in ASC mode. In this configuration, AI5 is ASC_EN and AI6 is the ASC input. The operation is identical to what is described for the primary side. Please note that if AI5/AI6 are to be used for the ASC function they are unavailable for OCP/SCP and PS temperature monitoring. When using the secondary side ASC, it is possible that the GM_FAULT will be set (when enabled) if the IN+ state is different than the ASC state. There will be no fault action taken, but the STATUS3[GM_FAULT] will be set. The implementation flow of ASC function is presented in 図 7-27. This implementation assumes both primary and secondary ASC are used. The secondary ASC covers the failure mode where VCC1 power is down. The primary and secondary ASC functions can be used independently. If both ASC functions are enabled, the secondary ASC has highest priority. The ASC functions are available in all operation states, assuming there is a valid power supply (VCC1 and VCC2 for ASC/ASC_EN or VCC2 for AI5/AI6).

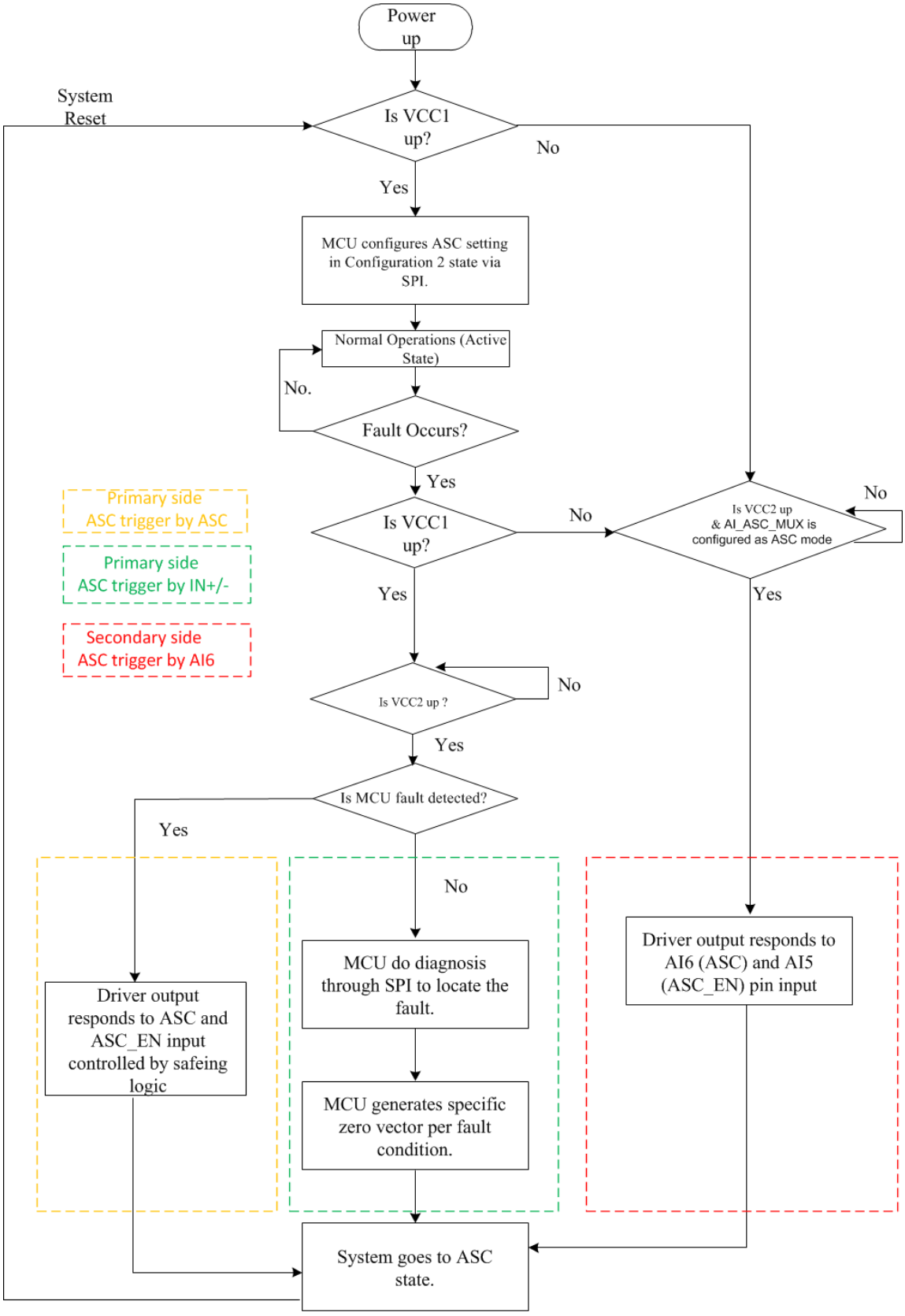


図 7-27. ASC implementation Flowchart

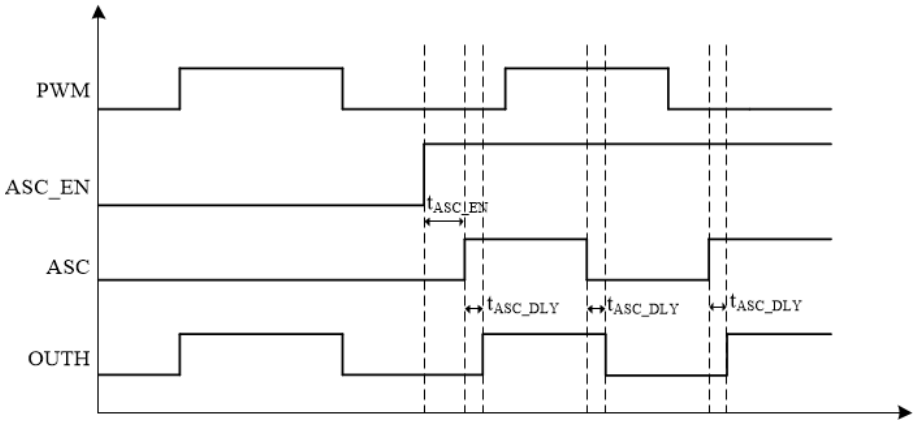


図 7-28. ASC implementation logic.

7.3.5.12 Shoot-Through Protection (STP)

The shoot through protection function (STP) provides an additional layer of protection from shoot through conditions due to incorrect PWM commands from MCU. The output of the driver uses IN+ and the complementary PWM signal provided to the IN- input to set the output state of the driver. Both the IN+ and IN- inputs are deglitched by t_{GLITCH}, which is programmable using CFG1[IO_DEGLITCH] bits (CFG1). There are two available version of STP, IN+/IN- safety interlock and automatic dead-time. The safety interlock function is enabled by setting the CFG1[TDEAD] bits (CFG1) to 0b000000 (t_{DEAD} = 0). When using the safety interlock STP, if IN+ and IN- are both high at the same time, a shoot-through condition (STP fault) is detected. During an STP fault, the STATUS2[STP_FAULT] bit (STATUS2) is set, and, if unmasked, the nFLT1 output pulls low. The output of the driver is forced to the state defined by CFG3[FS_STATE_STP_FAULT] (CFG3). When the t_{DEAD} is non-zero (CFG1[TDEAD] ≠ 0b000000, dead time is added to the falling edge of IN- by the device. In these cases, when IN+ goes high, the device waits until the deglitched falling edge of IN-, then OUTH pulls high t_{DEAD} after the deglitched IN- is low. The implementation diagram and timing schemes are presented in 図 7-29 and 図 7-30 respectively.

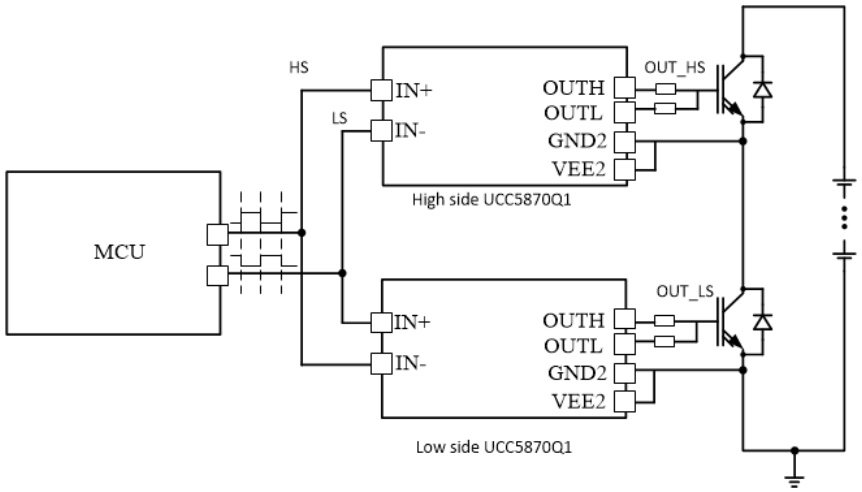


図 7-29. Block diagram of implementation of STP function.

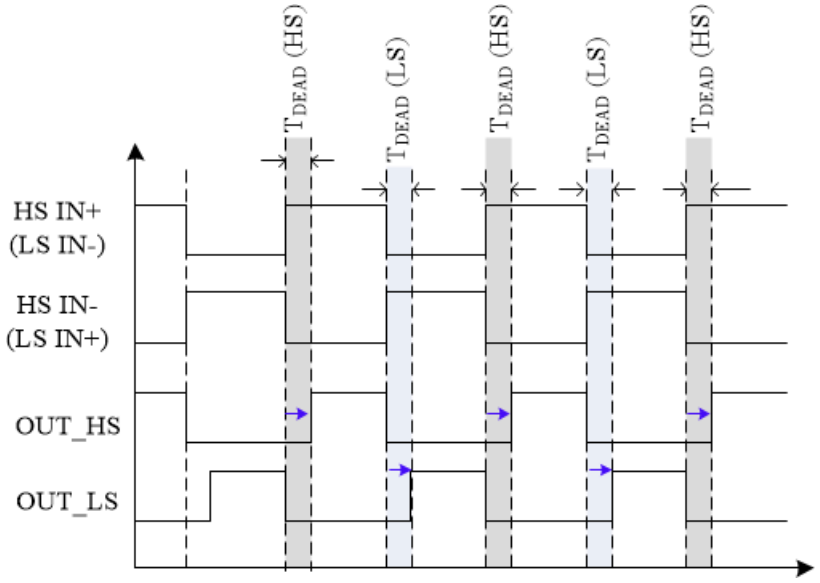


図 7-30. Timing scheme of implementation of STP function.

7.3.5.13 Gate Voltage Monitoring and Status Feedback

The integrity of the PWM channel is monitored end to end using two checks. The first check monitors the communication across the isolation channel. The received state on the secondary side is communicated back o the primary side to ensure the two match. If there is a mismatch between the IN+ state and the received IN+ state, the STATUS1[PWM_COMP_CHK_FAULT] bit (STATUS1) is set, if unmasked, nFLT1 pulls low, and the driver output is forced ot the state defined by CFG3[FS_STATE_PWM_CHK] (CFG3). The second check monitors the actual gate voltage of the power transistor to ensure the gate is in the correct state. The monitored gate voltage is first converted to logic state and indicated in the STATUS3[GM_STATE] bit (STATUS3). The converted gate voltage logic state is then compared with the input PWM (IN+) signal. The mismatch of the two signals causes a gate voltage monitor fault condition where the STATUS3[GM_FAULT] bit (STATUS3) is set, the driver output is forced to the state defined by CFG10[FS_STATE_GM] (CFG10), and, if unmasked, nFLT1 pulls low. Blanking time relative to the driver outputs is used to prevent false reporting of the gate voltage monitor error during driver transitions. During 2LTOFF transitions, the blanking time starts after the 2LTOFF plateau timer expires in order to prevent false GM faults during the transition. Alternatively, the GM fault may be disabled during STO and 2LTOFF using the CFG5[GM_STO2LTO_DIS] bit (CFG5). The blanking time is adjustable using the CFG4[GM_BLK] bits (CFG4). Additionally, the gate monitoring function may be disabled entirely using the CFG4[GM_EN] bit (CFG4). The implementation block diagram and timing schemes are presented in 図 7-31 and 図 7-32.

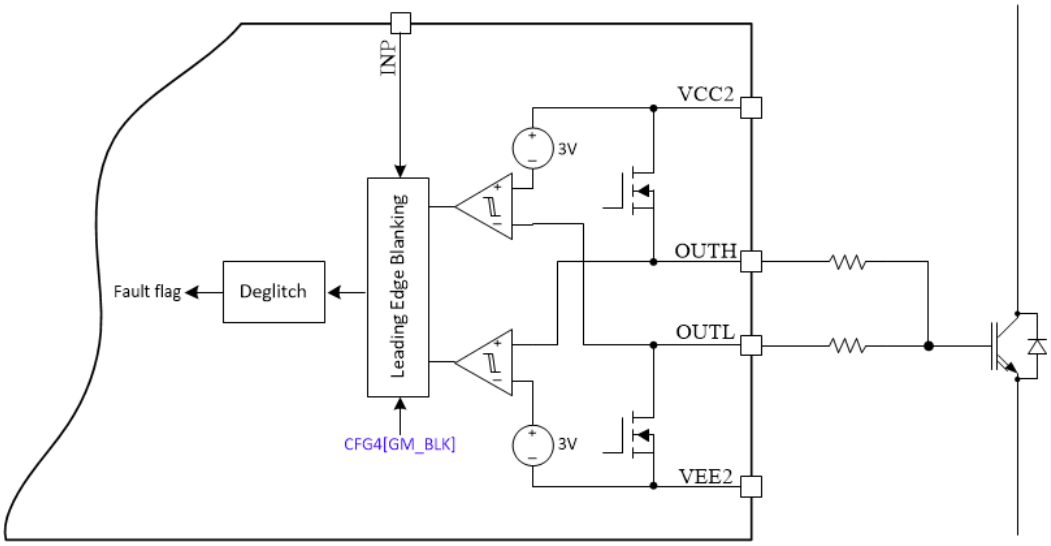


図 7-31. Block diagram of implementation of gate voltage monitor function.

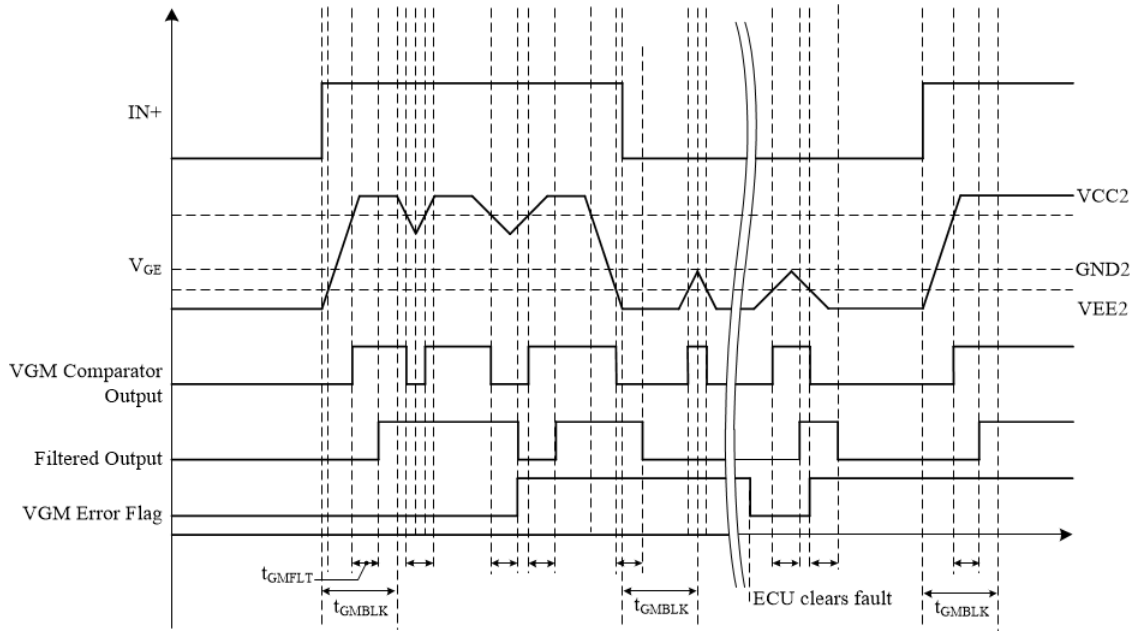


図 7-32. Timing scheme of implementation of gate voltage monitor function.

7.3.5.14 V_{GTH} Monitor

The V_{GTH} Monitor function is used to measure the gate threshold voltage of the power transistor during power up. When enabled using the CONTROL2[VGTH_MEAS] bit (CONTROL2), the switch between DESAT and OUTH is turned on. A constant current source charges the gate capacitance of the power transistor and the gate voltage ramps up gradually. Once the channel starts to conduct, the gate voltage is naturally held at the threshold voltage level as the power transistor in a diode configuration. After the blanking time, t_{dVGTHM}, the integrated ADC samples the gate voltage, and reports the measurement in register ADCDATA8. The measurement is actually a divided down version (divided by 8) of the gate voltage. The actual threshold voltage is calculated as:

$$V_{GTH} = V_{ADCDATA8} \times 8 \quad (3)$$

This measurement is then used by the MCU to judge the health of the power transistor.

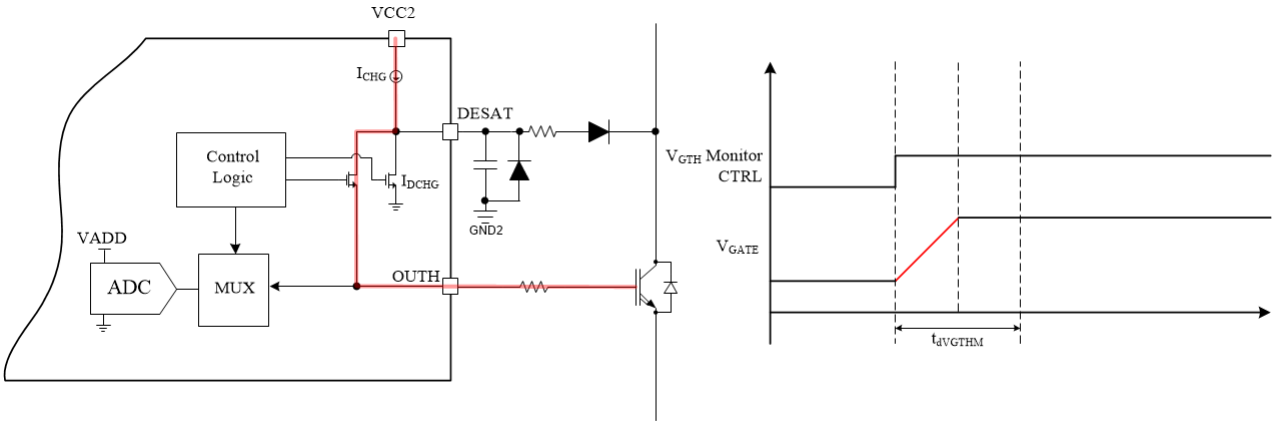


図 7-33. V_{GTH} monitoring circuit current flow while charging the gate capacitance

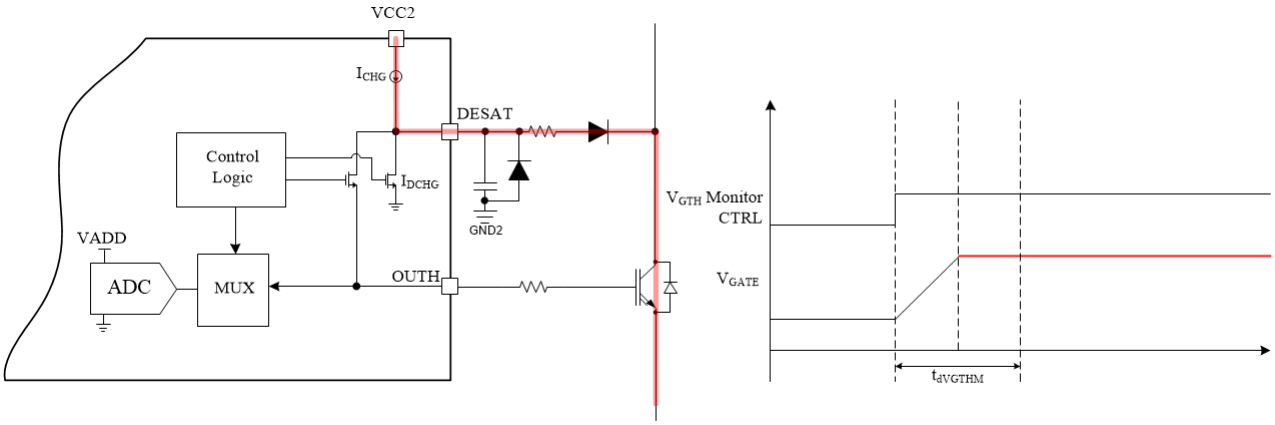


図 7-34. V_{GTH} monitoring circuit current flow while the power transistor is in diode configuration

7.3.5.15 Cyclic Redundancy Check (CRC)

the device uses a cyclic redundancy check (CRC) to ensure data integrity for the configuration of the device while the driver output is active, the SPI communications (both transmitted and received), and the internal non-volatile memory that store the trim information that ensures the performance of the device. The CRC represents the remainder of a process analogous to polynomial long division, where the protected data is divided by the polynomial. The device uses the CRC8 polynomial $X^8 + X^2 + X + 1$ with a 0xFF initialization (to catch leading 0 errors) for its calculations.

7.3.5.15.1 Calculating CRC

The calculation process begins by initializing the command frame by XORing it with the current CRC (0xFF for the very first command frame). Next, the XOR'd value is divided by the polynomial. The result is used as the CRC for the next frame. Repeat the process until all of the frames are run through the calculation. Note that the CRC is updated internal with every 16-bits, so the actual read/write command byte must be included in the calculation. See 図 7-36 for an example calculation.

7.3.5.16 Configuration Data CRC

When the device transitions to the ACTIVE state, the contents of configuration and control registers are protected by CRC engine. The configuration CRC is enabled using the CFG8[CRC_DIS] bit (CFG8). The registers protected by the CRC include:

- CFG1 - CFG11
- ADCCFG
- DOUTCFG

- GD_ADDRESS[GD_ADDR] (no MSB)
- SPITEST
- CONTROL1
- CONTROL2, excluding the MSB (CONTROL2[CLR_STAT_REG])

The CRC fault detection is performed every t_{CRCCFG} (typically 2 ms). If the calculated CRC8 checksum for the configuration registers does not match the CRC8 checksum calculated upon entering the Active state, the STATUS2[CFG_CRC_PRI_FAULT] (for a primary side CRC fail, STATUS2) or the STATUS4[CFG_CRC_SEC_FAULT] (for a secondary side CRC fail, STATUS4) bit is set and, if unmasked, the nFLT1 output goes low. Additionally, for the secondary side CRC failure, the driver output is forced to the state defined by CFG11[FS_STATE_CFG_CRC_SEC_FAULT] (CFG11).

Diagnostics for the CRC check are available. Use the CONTROL1[CFG_CRC_CHK_PRI] (CONTROL1) to induce a CRC error on the primary side. CONTROL2[CFG_CRC_CHK_SEC] (CONTROL2) to induce a CRC error on the secondary side. Writing to any of the "RESERVED" bits in the configuration registers also induces a CRC fault.

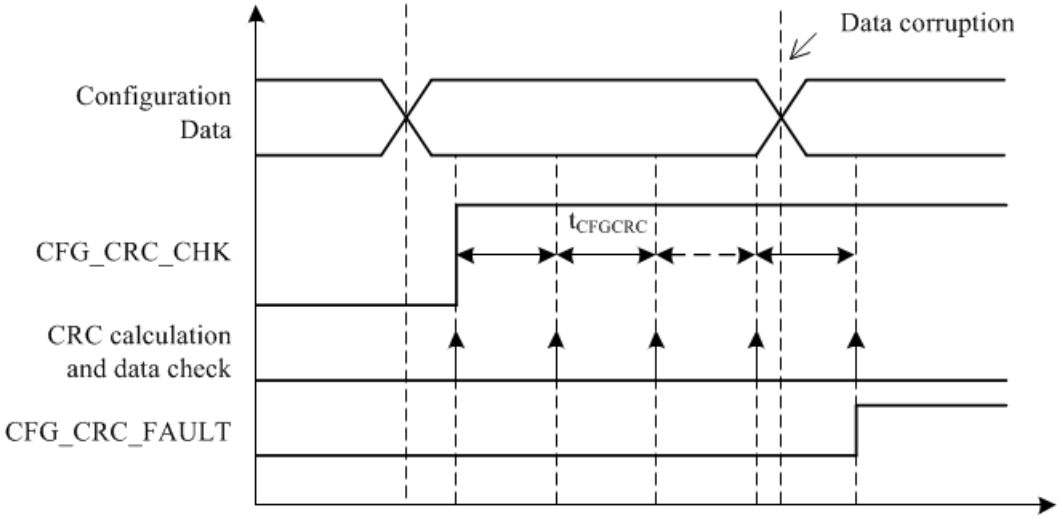


図 7-35. Configuration Data CRC Check Timing

7.3.5.17 SPI Transfer Write/Read CRC

The CRC checks for SPI transfer are continuously updated as SPI traffic is received/ sent. The CRC is updated with every 16-bits that are received. An example of calculating the SPI CRC for a sent command is given in 図 7-36. In this set of commands, we are updating the configuration for CFG1 and then doing a CRC comparison on that command.

表 7-2. Example of CRC Calculation While Updating CFG1

Command	Purpose	CRC Before	CRC_After
0xFC00	Change the SPI address pointer to CFG1 register	0xFF (Initialized)	0x3F
0xFA58	Update the high byte with 0x58 configuration	0x3F	0x23
0xFB2A	Update the low byte with 0x2A configuration	0x23	0xC4
0xFC13	Change the SPI address point to CRCDATA register	0xC4	0x28
0xFA30	Update the CRC_TX bits with the calculated CRC	0x28	0x30 (written to the CRC_TX bits)

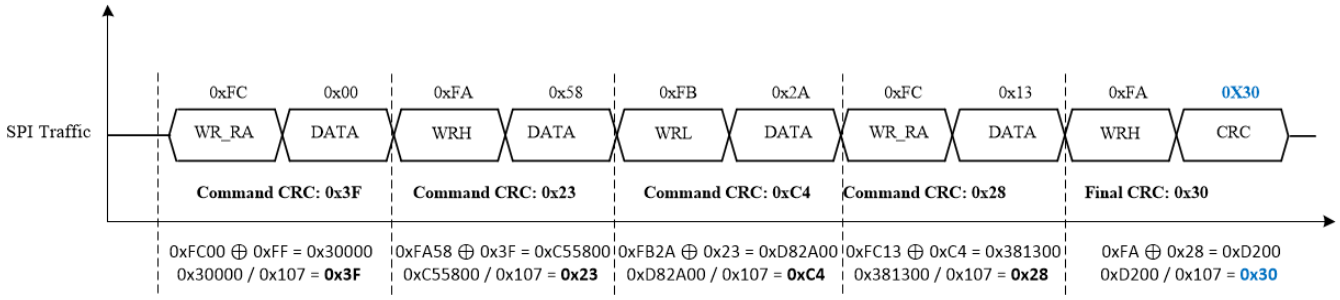


図 7-36. Calculating CRC for a Set of Commands

7.3.5.17.1 SDI CRC Check

The SDI CRC checksum data is continuously calculated as SPI data frames are received. Once the MCU writes to the to CRCDATA[CRC_TX] bits (CRCDATA). The write to these bits triggers a comparison of the data in the CRC_TX bits with the internally calculated CRC. Once the comparison is complete, the CRC calculation logic is reset (reset value = 0xFF). When there is a mismatch between CRC_TX data and CRC calculated internally, the STATUS2[SPI_FAULT] bit (STATUS2) is and, if unmasked, the nFLT1 output pulls low. Additionally, the output of the driver is forced to the state programmed in CFG3[FS_STATE_SPI_FAULT] (CFG3).

7.3.5.17.2 SDO CRC Check

The SDO CRC checksum is continuously calculated as data is clocked out of SDO. The resulting CRC is stored in the CRCDATA[CRC_RX] bits. The bits are updated whenever nCS transitions from low to high. The CRC calculation logic is reset (reset value = 0xFF) when the CRC_RX bits are read or when the CONTROL1[CLR_SPI_CRC] bit is written. Note that the CRC_RX bits are reset immediately with the read, and the next CRC_RX value begins its calculation while clocking out of the CRC_RX bits. This means the received CRC_RX must be included in the next CRC calculation (i.e. the received CRC_RX is the first byte to be xor'd with the 0xFF reset value).

7.3.5.18 TRIM CRC Check

After each power up, the device performs a TRIM CRC check on the internal non-volatile memory on both the primary and secondary sides. If the calculated CRC8 checksum does not match the CRC8 checksum stored in the internal TRIM memory, the STATUS2[TRIM_CRC_PRI_FAULT] (for a primary side CRC fail, STATUS2) or the STATUS4[TRIM_CRC_SEC_FAULT] (for a secondary side CRC fail, STATUS4) bit is set and, if unmasked, the nFLT1 output goes low. Additionally for the secondary side CRC failure, the driver output is forced to the state defined by CFG11[FS_STATE_TRIM_CRC_SEC_FAULT] (CFG11).

7.4 Device Functional Modes

The overall operation mode transition diagram is presented in 図 7-37. The current state of the device is read in the STATUS1[OPM] bits (STATUS1). Note that these bits are only readable in the Configuration 2 and Active states.

- State 1: RESET
- State 2: Configuration 1
- State 3: Configuration 2
- State 4: Active

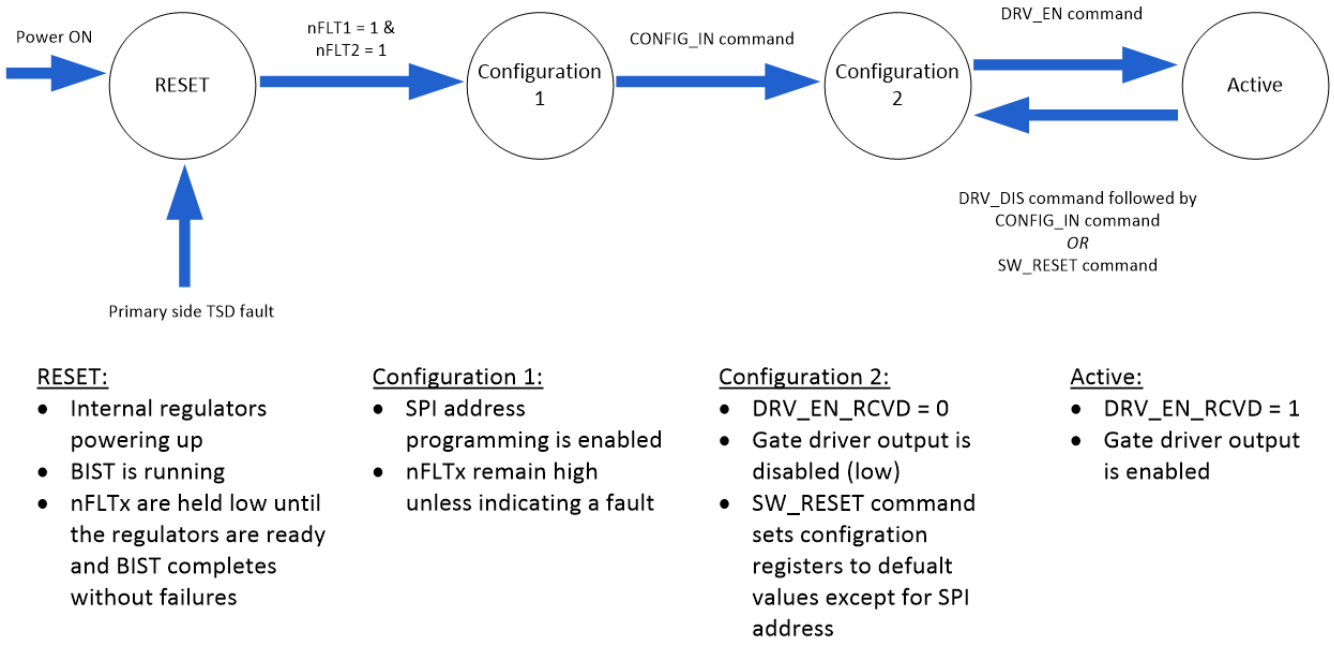


図 7-37. Operation mode diagram during normal operation

7.4.1 State 1: RESET

When a valid power supply is first applied to VCC1, the device enters the RESET state. In the RESET state, the device does not respond to commands from MCU, the driver outputs (OUTL and OUTH) are both high impedance, the registers are reset to the default values, and all of the built In Self Tests (BIST) run. The nFLTx outputs are held low until a power source is connected to VCC2, all of the automatic BISTs complete, and the device transitions to the Configuration 1 state. After transitioning from Reset, the device only returns to the Reset state if the power is cycled, or if the primary side over temperature is detected. The secondary over temperature event does not cause the state transition to RESET unless the primary side also detects the over temperature event.

7.4.2 State 2: Configuration 1

Once all of the BIST complete, and communication is established from the primary to the secondary side, the device transitions to the Configuration 1 state. This is indicated when the nFLT* outputs are pulled high. In this state, the address for the device is programmable by the MCU. See the Device Addressing section for details on how to program the SPI address for the device. The driver output (OUTL) is pulled low in this state. Once the address is programmed, the CONFIG_IN command (see 表 7-3) must be sent to transition to the Configuration 2 state. Note that in Daisy Chain configurations, the CFG_IN must be sent to the devices one-by-one because the SDO output is not enabled until a valid addressed command is sent. This can be done by sending a full frame of 6 CFG_IN commands six times or, alternatively, send a CFG_IN to the first device as a single command followed by CFG_IN, NOP as the second frame, followed by CFG_IN, NOP, NOP as the third frame, and so on to enable the SDO output on all devices and send them to Configuration 2. This process only needs to be done once per power cycle unless an invalid address (non-0x0) is sent.

7.4.3 State 3: Configuration 2

When a valid CONFIG_IN command (see 表 7-3) is received, the device transitions to the Configuration 2 state. In this state, the device configuration is programmable by the MCU via the SPI interface. All of the configuration registers are available for write. The STATUS registers are updated with the status of the device and the nFLT* outputs will indicate any unmasked faults. The ADC does not operate in the Configuration 2 state. The driver output (OUTL) is pulled low in this state. Send a DRV_EN command (see 表 7-3) to transition to the Active state and enable the driver output.

7.4.4 State 4: Active

Upon receiving a valid DRV_EN command, the device transitions to the Active state. In this state, the STATUS2[DRV_EN_RCVD] bit (STATUS2) is set to '1', the CRC for the configuration registers is calculated and stored, SPI writes to most registers are disabled, and the driver outputs are enabled to follow the IN+/IN- inputs, assuming there is no fault condition. All of the registers are Read Only, with the exception of CONTROL2[CLR_STAT_REG], CFG8[IOUT_SEL], and CFG8[CRC_DIS]. Any writes to any other registers/ bits are ignored. The device remains in Active mode until the SW_RESET command is sent, a DRV_DIS command followed by a CONFIG_IN is sent, or a primary side thermal shutdown fault occurs. The SW_RESET command disables the driver and resets all registers except for the driver address, while the DRV_DIS command disables the driver while leaving the register contents intact.

7.5 Programming

7.5.1 SPI Communication

Programming of the device is done through the SPI serial communication slave interface by an external MCU. The SPI communication follows a 16-bit protocol, utilizing specific command data frames, and uses an active-low chip select input (nCS) and communicates at rates up to 4MHz. The communication frame starts with the nCS falling edge and ends with nCS rising edge. While nCS is high, the SPI interface is held in reset, and the SDO output is high impedance. The SPI clock idles at 0 (CPOL=0) and clocks the SDI/SDO data (CPHA=1) on the falling edge. The device supports three SPI bus configurations: independent slave configuration, daisy chain configuration, and a new address oriented configuration.

7.5.1.1 System Configuration of SPI Communication

The system is configured in one of the three SPI modes: Regular SPI configuration (図 7-38), Daisy Chain configuration (図 7-40), and Address-based onfiguration (図 7-42).

7.5.1.1.1 Independent Slave Configuration

The Independent Slave configuration is shown in 図 7-38. In this mode, the CLK input, SDI input, and SDO outputs for all devices on the SPI bus are shared. The MCU drives the nCS input for the device that is to be addressed. The drawback to this approach is that a separate GPIO for each driver in the system (up to 12 for dual inverter systems) is required of the MCU, but it does allow random access to any device in the system. The message frame is shown in 図 7-39

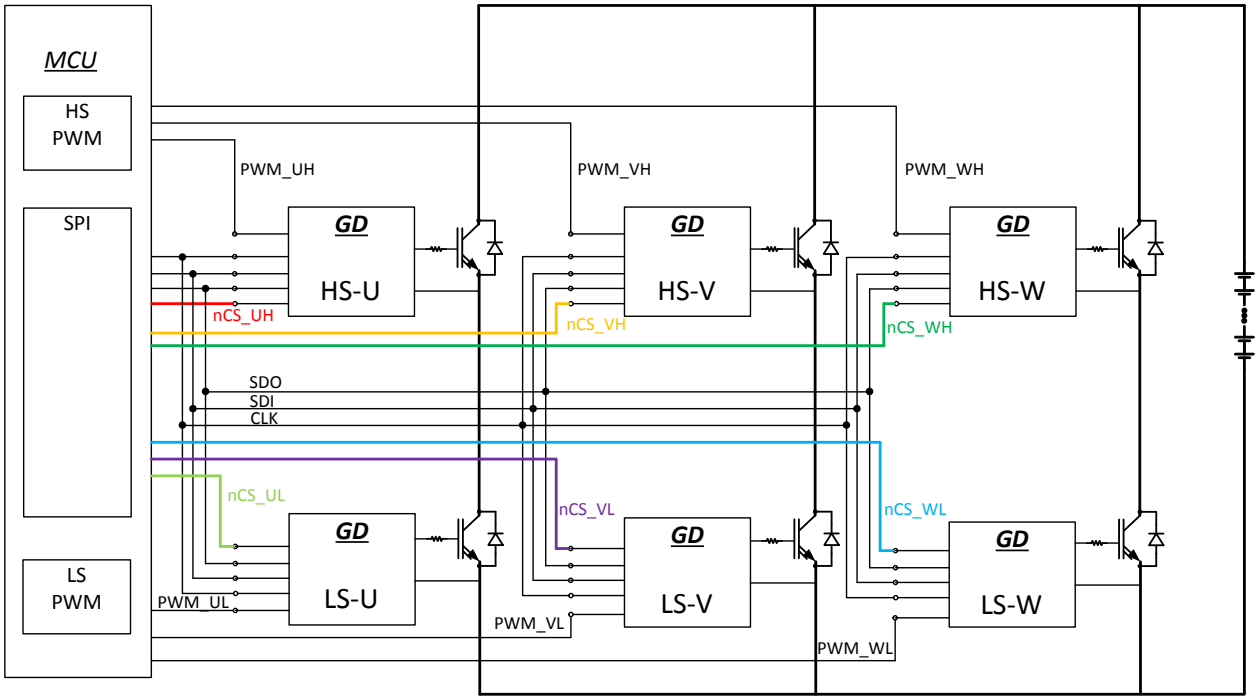


図 7-38. System configuration of regular SPI configuration

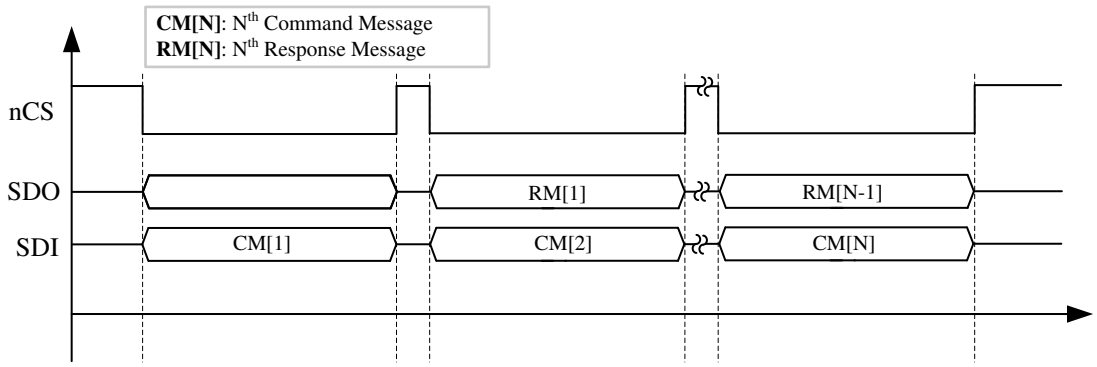


図 7-39. SPI message frame for Independent Slave and Address-based configurations

7.5.1.1.2 Daisy Chain Configuration

The Daisy Chain configuration is shown in 図 7-40. In this configuration, the MCU MOSI connects to the SDI of the first device and the MISO connects to the SDO of the last device. The SDO of each of the device connects to the SDI of the next device in the system (excluding the last device). The system effectively becomes a communication shift register. During communication, the host continuously clocks in data for all the devices in the system while holding the nCS pin low. While the nCS input is low, the SDO shifts data out as the data is clocked into the SDI shift register as shown in 図 7-41. Once nCS is pulled high, the 16-bits in the SDI register are latched and acted upon by the device. This configuration drastically reduces the number of GPIOs required, but it does not allow random access to the devices.

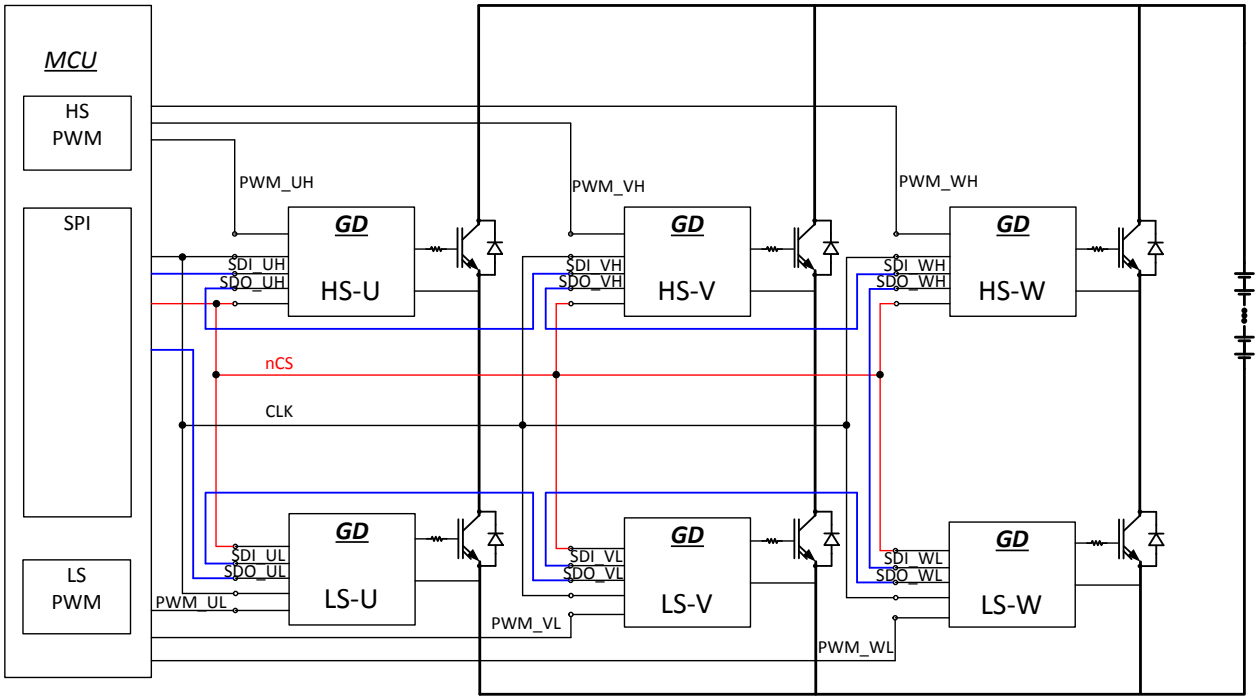


図 7-40. System configuration of daisy chain SPI configuration

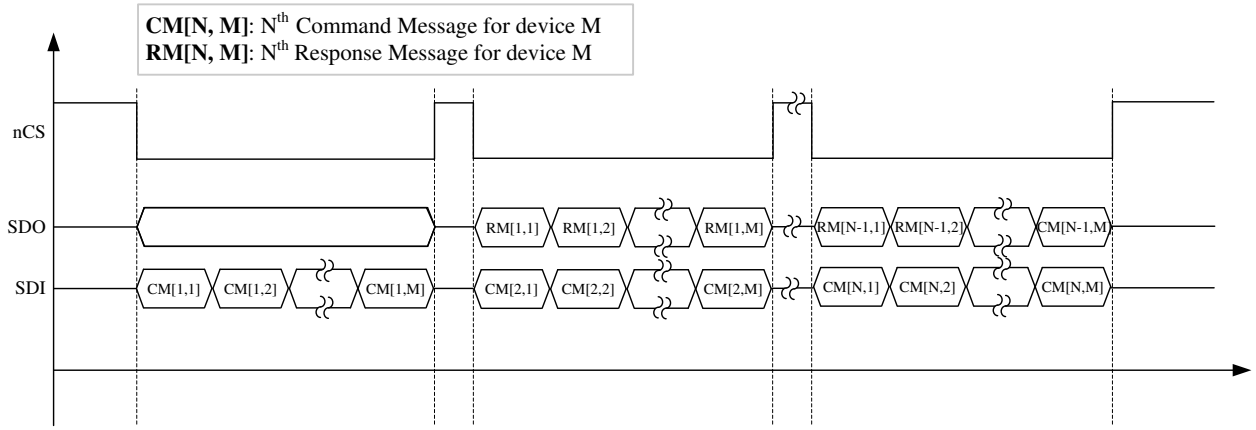


図 7-41. SPI message frame daisy chain SPI configuration

7.5.1.1.3 Address-based Configuration

The Address-based configuration provides significant flexibility to the system design. This configuration is similar to the Independent Slave configuration in that all of the CLK, SDO, and SDI connections are shared between all devices (shown in 図 7-42). Additionally, the nCS input is also shared. This reduces the GPIO requirement on the MCU to one, similar to Daisy Chain, but also allows random access like the Independent Slave configuration. The Address-based configuration is done by defining each device in the system with a unique address. See the Device Addressing section for details on how to address the devices in the system. The message frame is shown in 図 7-39

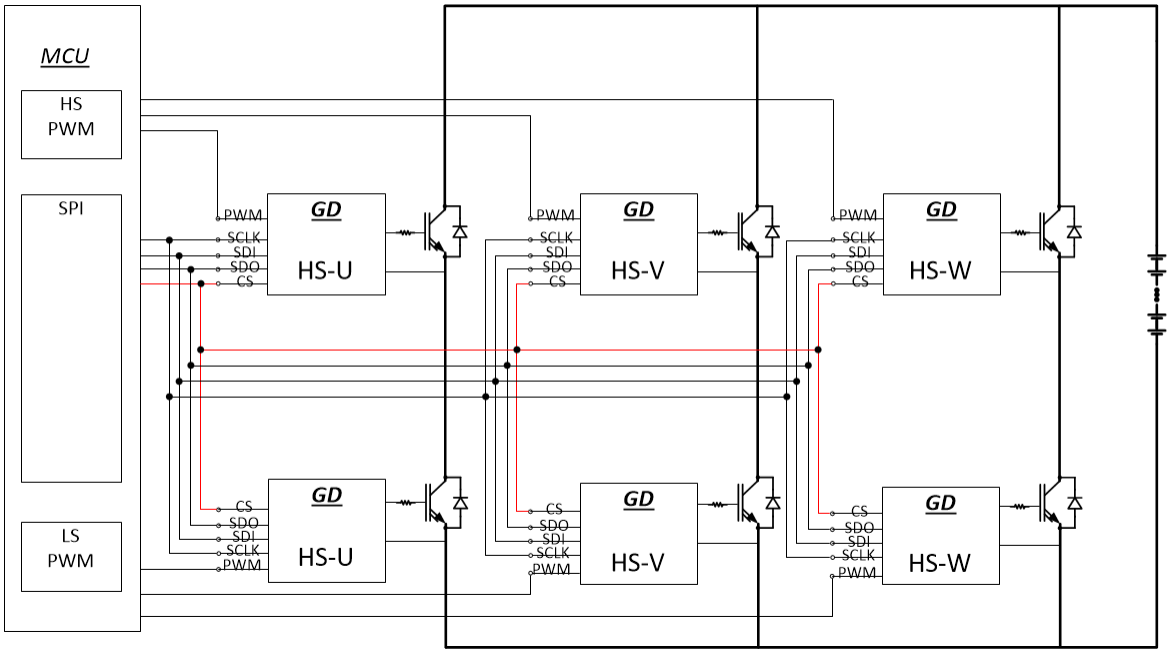


図 7-42. System configuration for Address-based SPI Communication Scheme

7.5.1.2 SPI Data Frame

The SPI data frame is composed of 16bits. The timing scheme and format of a data frame is shown in 図 7-43 and 図 7-44.

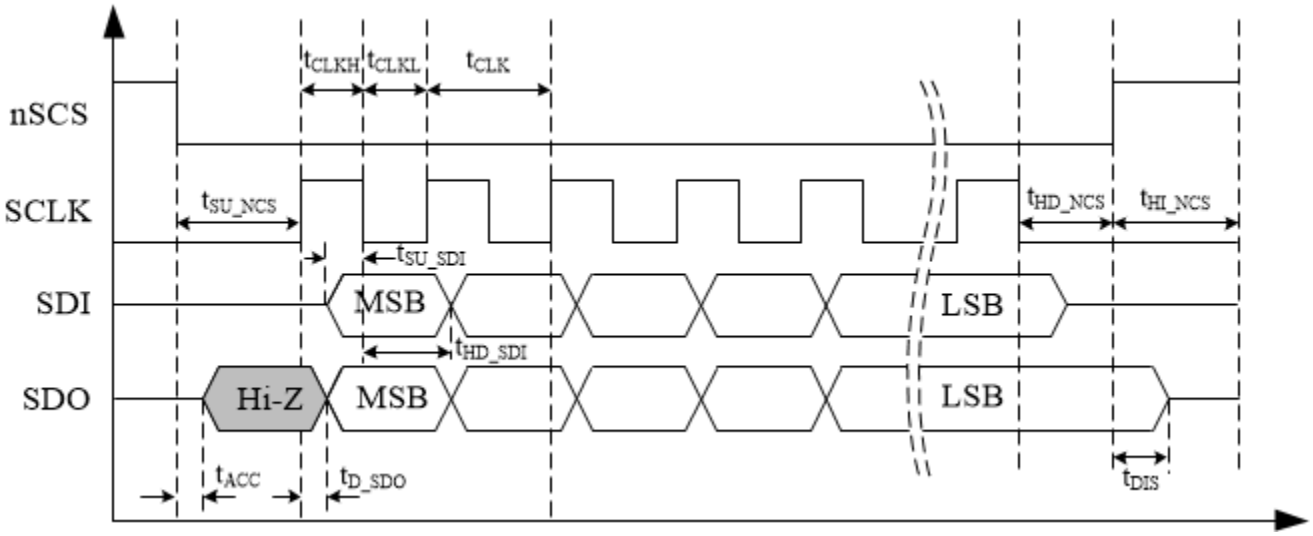


図 7-43. Timing scheme of SPI communication

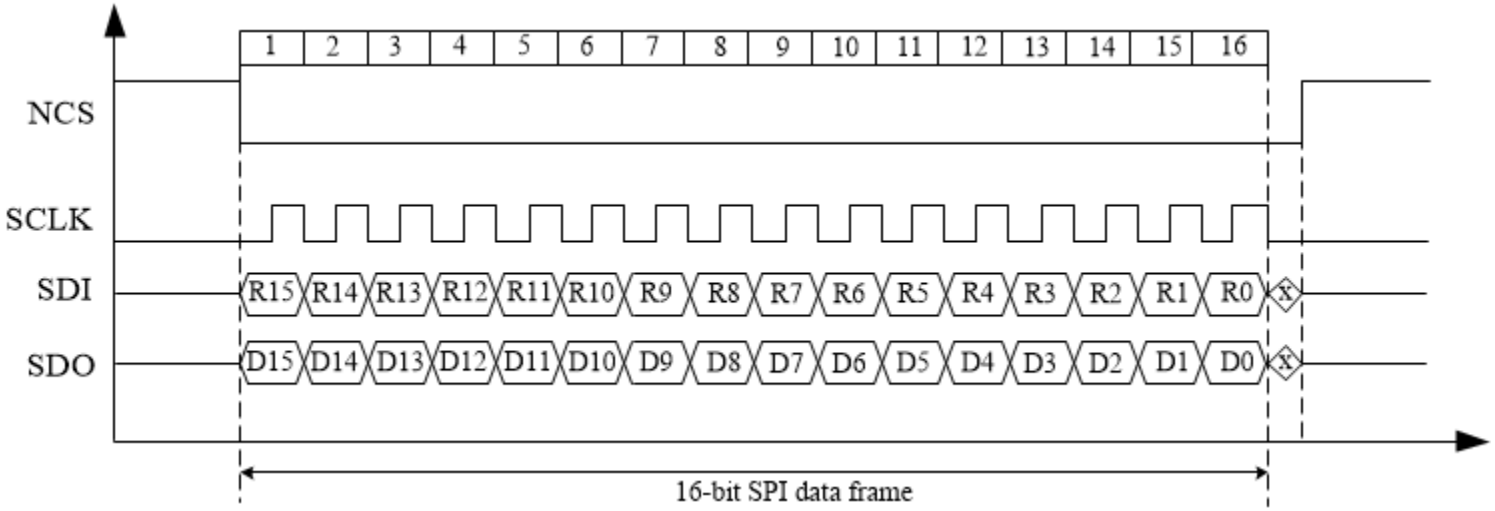


図 7-44. 16-bit of SPI data frame.

The 16-bit data frame includes three data fields: chip address (CHIP_ADDR), command type (CMD), and an 8-bit data (DATA). The chip address (CHIP_ADDR) bits are used, regardless of the system configuration. However, when using the Daisy Chain or Independent Slave configurations, 0x0 or 0xF is used for all of the devices in the system. In Address-based configuration, the devices are individually addressed, and all devices respond to 0x0 and 0xF. Note that SDO is high impedance until it receives a command with the programmed device address. Once receiving the valid addressed command, the SDO is driven to send out data. When an invalid addressed command or 0xF (broadcast address) is received, the SDO returns to high impedance, thereby allowing other devices to take control of the shared MISO (SDO) bus. There are 10 command types used by the device, defined in 表 7-3.

表 7-3. SPI message commands

		16-BIT DATA FRAME															
		BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Command Name	Command Description	CHIP_ADDR				CMD + DATA											
DRV_EN	Driver output enable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	0	1
DRV_DIS	Driver output disable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	1	0
RD_DATA	Read data from register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	1	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
CFG_IN	Enter configuration state	CA[3]	CA[2]	CA[1]	CA[0]	0	0	1	0	0	0	1	0	0	0	1	0
NOP	No operation	CA[3]	CA[2]	CA[1]	CA[0]	0	1	0	1	0	1	0	0	0	0	1	0
SW_RESET	Software RESET (Reinitialize the configurable registers)	CA[3]	CA[2]	CA[1]	CA[0]	0	1	1	1	0	0	0	0	1	0	0	0
WRH	Write D[15:8] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	0	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
WRL	Write D[7:0] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
WR_RA	Write register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	1	0	0	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
WR_CA(1)	Write chip address CA[3:0]	1	1	1	1	1	1	0	1	1	0	1	0	CA[3]	CA[2]	CA[1]	CA[0]

(1) IN+ must be high to program CHIP address

7.5.1.2.1 Writing a Register

The register configuration for the device uses 16-bit registers. The SPI engine utilizes three separate commands in order to program these registers. The process involves first setting the register to be written to by using the WR_RA command. All subsequent writes will go to this register address until the WR_RA command is sent again, or the device is reset. Use the WRH command to write the "high" byte of the register (bits 15:8) and use

the WRL command to write the "low" byte of the register (bits 7:0). The WRH and WRL commands can be sent in any order. Additionally, it is not necessary to write both bytes of the register. If only the "low" byte needs modification, a WRL write is all that is required. It is not necessary to send a WRH command as well.

7.5.1.2.2 Reading a Register

The process for reading a register is less steps than that of a write command. To read a register, simply use the RD_DATA command to program the device with the register to be read. The full 16-bit data is clocked out during the next SPI transaction. The next SPI transaction could be another command (RD_DATA or WR_RA, for example), or simply a NOP (no operation command). Never send a RD_DATA command to the broadcast address (0xF) while in the Address-based configuration. This will cause all devices on the bus to responds simultaneously and the data will be corrupted. It is ok to use 0xF in the other modes as the traffic is handled by another mechanism.

7.6 Register Maps

7.6.1 UCC5870 Registers

表 7-4 lists the memory-mapped registers for the device registers. All register offset addresses not listed in 表 7-4 should be considered as reserved locations and the register contents should not be modified.

表 7-4. UCC5870 Registers

Offset	Acronym	Register Name: description	SPI write access enabled state	Section	Covered by Configuration Data CRC?
0x0	CFG1	Configuration register 1: Primary side device configuration. VCC1 UVLO and OVLO, IO deglitch timer, Over temperature, nFLT2 pin function, and dead time setting.	Configuration 2	Go	Yes
0x1	CFG2	Configuration register 2: nFLT1,2 pin function setting.	Configuration 2	Go	Yes
0x2	CFG3	Configuration register 3: Gate driver output fault reaction setting	Configuration 2	Go	Yes
0x3	CFG4	Configuration register 4: Protection and monitoring function setting. Enabling or disabling of the functions.	Configuration 2	Go	Yes
0x4	CFG5	Configuration register 5: Protection and monitoring function setting. Enabling or disabling of the functions. Threshold setting.	Configuration 2	Go	Yes
0x5	CFG6	Configuration Registers 6: Protection and monitoring function setting. Enabling or disabling of the functions. Threshold and timer setting.	Configuration 2	Go	Yes
0x6	CFG7	Configuration Registers 7: Protection and monitoring function setting. Enabling or disabling of the functions. Threshold and timer setting.	Configuration 2	Go	Yes
0x7	CFG8	Configuration register 8: Protection and monitoring function setting. Enabling or disabling of the functions. Threshold and timer setting.	Bit15-7,5-3: Configuration 2;Bit6,2-0,: Configuration 2; Active	Go	Yes
0x8	CFG9	Configuration register 9: nFLT1,2 pin function setting.	Configuration 2	Go	Yes
0x9	CFG10	Configuration register 10: Gate driver output fault reaction setting.	Configuration 2	Go	Yes
0xA	CFG11	Configuration register 11: Gate driver output fault reaction setting	Configuration 2	Go	Yes
0xB	ADCDATA1	ADC data register 1: Digital representation of sampled AI1 voltage		Go	No

表 7-4. UCC5870 Registers (continued)

Offset	Acronym	Register Name: description	SPI write access enabled state	Section	Covered by Configuration Data CRC?
0xC	ADCDATA2	ADC data register 2: Digital representation of sampled AI3 voltage		Go	No
0xD	ADCDATA3	ADC data register 3: Digital representation of sampled AI5 voltage		Go	No
0xE	ADCDATA4	ADC data register 4: Digital representation of sampled AI2 voltage		Go	No
0xF	ADCDATA5	ADC data register 5: Digital representation of sampled AI4 voltage		Go	No
0x10	ADCDATA6	ADC data register 6: Digital representation of sampled AI6 voltage		Go	No
0x11	ADCDATA7	ADC data register 7: Digital representation of sampled internal die temperature		Go	No
0x12	ADCDATA8	ADC data register 8: Digital representation of sampled divided OUTH voltage for VGTH monitor		Go	No
0x13	CRCDATA	SPI CRC Data Register	Configuration 2	Go	Yes
0x14	SPITEST	SPI read/write test Register	Configuration 2, Active	Go	Yes
0x15	GDADDRESS	Driver address register	Configuration 1	Go	Yes
0x16	STATUS1	Status register 1: Fault status.		Go	No
0x17	STATUS2	Status register 2: Fault and pin status.		Go	No
0x18	STATUS3	Status register 3: Fault status.		Go	No
0x19	STATUS4	Status register 4: Fault status.		Go	No
0x1A	STATUS5	Status register 5: Fault status.		Go	No
0x1B	CONTROL1	Control register 1: Diagnostic commands.	Configuration 2, Active	Go	Yes
0x1C	CONTROL2	Control register 2: Diagnostic commands.	Configuration 2, Active	Go	Yes
0x1D	ADCCFG	ADC setting	Configuration 2	Go	Yes
0x1E	DOUTCFG	DOUT function setting	Configuration 2	Go	Yes

Complex bit access types are encoded to fit into small table cells. 表 7-5 shows the codes that are used for access types in this section.

表 7-5. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 CFG1 Register

CFG1 is shown in 図 7-45 and described in 表 7-6.

Return to Summary Table.

図 7-45. CFG1 Register

15	14	13	12	11	10	9	8
UV1_DIS	UVLO1_LEVEL	OVLO1_LEVEL	IO_DEGLITCH		GD_TWN_PRI_EN	Reserved	OV1_DIS
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1		R/W-0x1	R/W-0x0	RW-0x0
7	6	5	4	3	2	1	0
RESERVED	NFLT2_DOUT_MUX	TDEAD					
RW-0x0	R/W-0x0	R/W-0x0					

表 7-6. CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UV1_DIS	R/W	0x0	VCC1 UVLO disable: 0x0 = Enabled 0x1 = Disabled
14	UVLO1_LEVEL	R/W	0x0	VCC1 UVLO setting: 0x0 = 2.45V (3.3V logic rail) 0x1 = 4.35V (5V logic rail)
13	OVLO1_LEVEL	R/W	0x0	VCC1 OVLO setting: 0x0 = 5.65V (5V logic rail) 0x1 = 4.15V (3.3V logic rail)
12-11	IO_DEGLITCH	R/W	0x1	IO deglitch (INP and INN) filter time: 0x0 = Deglitch filter bypassed 0x1 = 70ns setting 0x2 = 140ns setting 0x3 = 210ns setting
10	GD_TWN_PRI_DIS	R/W	0x1	Over temperature warning of gate driver VCC1 side enable: 0x0 = Enabled 0x1 = Disabled
9	RESERVED	R/W	0x0	This bit field is reserved.
8	OV1_DIS	R/W	0x0	VCC1 OVLO disable: 0x0 = Enabled 0x1 = Disabled
7	RESERVED	R/W	0x0	This bit field is reserved.
6	NFLT2_DOUT_MUX	R/W	0x0	nFLT2/DOUT pin function selection: 0x0 = nFLT2 0x1 = DOUT. When this setting is selected, all warnings selected to output to nFLT2 are output on nFLT1.

表 7-6. CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	TDEAD	R/W	0x0	Shoot-through protection dead time: 0x0 = No added deadtime (Interlock function enabled) 0x1 - 0x3F = 105ns to 4445ns with 70ns resolution Deadtime = code(decimal) x 70ns + 105ns

7.6.1.2 CFG2 Register

CFG2 is shown in 図 7-46 and described in 表 7-7.

Return to Summary Table.

図 7-46. CFG2 Register

15	14	13	12	11	10	9	8
INT_COMM_PRI_FAULT_P	OVLO1_FAULT_P	UVLO1_FAULT_P	STP_FAULT_P	CLK_MON_PRI_FAULT_P	SPI_FAULT_P		CFG_CRC_PRI_FAULT_P
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1		R/W-0x0
7	6	5	4	3	2	1	0
INT_REG_PRI_FAULT_P	TRIM_CRC_PRI_FAULT _P	BIST_PRI_FAULT_P	RESERVED	RESERVED	GD_TWN_PRI_FAULT_P	VREG1_ILIMIT_FAULT_P	PWM_CHK_FAULT_P
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	RW-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-7. CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INT_COMM_PRI_FAULT_P	R/W	0x0	Report inter-die communication failure to nFLT1 output: 0x0 = No 0x1 = Yes
14	OVLO1_FAULT_P	R/W	0x0	Report VCC1 OVLO fault to nFLT1 output: 0x0 = Yes 0x1 = No
13	UVLO1_FAULT_P	R/W	0x0	Report VCC1 UVLO fault to nFLT1 output: 0x0 = Yes 0x1 = No
12	STP_FAULT_P	R/W	0x0	Report STP fault to nFLT1 output: 0x0 = Yes 0x1 = No
11	CLK_MON_PRI_FAULT_P	R/W	0x0	Report clock monitor fault to nFLT1 output: 0x0 = Yes 0x1 = No

表 7-7. CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	SPI_FAULT_P	R/W	0x1	Report SPI fault to nFLT* outputs: 0x0 = nFLT1 0x1 = nFLT2 0x2 = No report 0x3 = RESERVED
8	CFG_CRC_PRI_FAULT_P	R/W	0x0	Report configuration register CRC fault to nFLT1 output: 0x0 = Yes 0x1 = No
7	INT_REG_PRI_FAULT_P	R/W	0x0	Report internal regulator fault to nFLT1 output: 0x0 = Yes 0x1 = No
6	TRIM_CRC_PRI_FAULT_P	R/W	0x0	Report TRIM CRC fault to nFLT* outputs: 0x0 = Yes 0x1 = No
5	BIST_PRI_FAULT_P	R/W	0x0	Report analog BIST fault to nFLT* outputs: 0x0 = Yes 0x1 = No
4-3	RESERVED	R/W	0x0	These bits are reserved. Writing to these bits sets the CFG_CRC_PRI_FAULT.
2	GD_TWN_PRI_FAULT_P	R/W	0x0	Report gate driver temp warning to nFLT* outputs: 0x0 = No 0x1 = Yes
1	VREG1_ILIMIT_FAULT_P	R/W	0x0	Report VREG1 ILIMIT fault to nFLT1 output: 0x0 = Yes 0x1 = No
0	PWM_CHK_FAULT_P	R/W	0x0	Report PWM check fault to nFLT1 output: 0x0 = Yes 0x1 = No

7.6.1.3 CFG3 Register

CFG3 is shown in 図 7-47 and described in 表 7-8.

Return to Summary Table.

図 7-47. CFG3 Register

15	14	13	12	11	10	9	8
FS_STATE_UVLO1_FAULT	FS_STATE_OVLO1_FAULT	FS_STATE_PWM_CHK	FS_STATE_STP_FAULT		Reserved	FS_STATE_SPI_FAULT	
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0		R/W-0x0	R/W-0x2	
7	6	5	4	3	2	1	0

図 7-47. CFG3 Register (continued)

FS_STATE_INT_REG_PRI_FAULT	FS_STATE_INT_COMM_PRI_FAULT	ITO1_EN	ITO2_EN	FS_STATE_CFG_CRC_PRI_FAULT	AI_IZTC_SEL
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-8. CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FS_STATE_UVLO1_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked VCC1 UVLO fault: 0x0 = Pulled low 0x1 = No action
14	FS_STATE_OVLO1_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked VCC1 OVLO fault: 0x0 = Pulled low 0x1 = No action
13	FS_STATE_PWM_CHK	R/W	0x0	OUTH/OUTL output state during an unmasked PWM check fault: 0x0 = Pulled low 0x1 = No action
12-11	FS_STATE_STP_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked shoot-through fault: 0x0 = Low 0x1 = High 0x2 = Reserved 0x3 = No action
10	RESERVED	R/W	0x0	Reserved. Writing to these bits sets the CFG_CRC_PRI_FAULT.
9-8	FS_STATE_SPI_FAULT	R/W	0x2	OUTH/OUTL output state during an unmasked SPI communication fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = No action 0x3 = No action
7	FS_STATE_INT_REG_PRI_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked internal regulator fault: 0x0 = Pulled low 0x1 = No action
6	FS_STATE_INT_COMM_PRI_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked internal communication result: 0x0 = Pulled low 0x1 = No action
5	ITO1_EN	R/W	0x0	Current source output at AI1, AI3, and AI5: 0x0 = Disabled 0x1 = Enabled

表 7-8. CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ITO2_EN	R/W	0x0	Current source output at AI2, AI4, and AI6: 0x0 = Disabled 0x1 = Enabled
3	FS_STATE_CFG_CRC_PRI_FAULT	R/W	0x0	Default OUTH/OUTL output state in case of configuration register CRC fault: 0x0 = Pulled low 0x1 = No action
2-0	AI_IZTC_SEL	R/W	0x0	AI1, AI3, AI5 bias current enable. Additionally, ITO1_EN must be set to '1'.: 0x0 = All bias current is OFF 0x1 = AI1 bias current is ON 0x2 = AI3 bias current is ON 0x3 = AI1 and AI3 bias current is ON 0x4 = AI5 bias current is ON 0x5 = AI1 and AI5 bias current is ON 0x6 = AI3 and AI5 bias current is ON 0x7 = All bias current is ON

7.6.1.4 CFG4 Register

CFG4 is shown in 図 7-48 and described in 表 7-9.

Return to Summary Table.

図 7-48. CFG4 Register

15	14	13	12	11	10	9	8
UV2_DIS	PS_TSD_DEGLITCH		DESAT_DEGLITCH	OV2_DIS	MCLP_CFG	GM_BLK	
R/W-0x0	R/W-0x0		R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x1	
7	6	5	4	3	2	1	0
GM_DIS	MCLP_DIS	VCECLP_EN	DESAT_EN	SCP_DIS	OCP_DIS	PS_TSD_EN	UVOV3_EN
R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0

表 7-9. CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UV2_DIS	R/W	0x0	VCC2 UVLO function disable: 0x0 = Enabled 0x1 = Disabled

表 7-9. CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-13	PS_TSD_DEGLITCH	R/W	0x0	Power switch thermal shutdown (TSD) deglitch filter time: 0x0 = 250ns 0x1 = 500ns 0x2 = 750ns 0x3 = 1000ns
12	DESAT_DEGLITCH	R/W	0x0	DESAT deglitch timer option: 0x0 = 158ns 0x1 = 316ns
11	OV2_DIS	R/W	0x1	VCC2 OVLO function disable: 0x0 = Enabled 0x1 = Disabled
10	MCLP_CFG	R/W	0x0	Active Miller clamp option: 0x0 = Internal 0x1 = External
9-8	GM_BLK	R/W	0x1	Gate voltage monitor blanking time: 0x0 = 500ns 0x1 = 1000ns 0x2 = 2500ns 0x3 = 4000ns
7	GM_DIS	R/W	0x0	Gate voltage monitor function enable: 0x0 = Enabled 0x1 = Disabled
6	MCLP_DIS	R/W	0x0	Active Miller clamp enable: 0x0 = Enabled 0x1 = Disabled
5	VCECLP_EN	R/W	0x1	VCE clamp enable: 0x0 = Disabled 0x1 = Enabled
4	DESAT_EN	R/W	0x1	DESAT detection enable: 0x0 = Disabled 0x1 = Enabled
3	SCP_DIS	R/W	0x0	Short circuit protection (SCP) enable: 0x0 = Enabled 0x1 = Disabled

表 7-9. CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OCP_DIS	R/W	0x1	Overcurrent protection (OCP) enable: 0x0 = Enabled 0x1 = Disabled
1	PS_TSD_EN	R/W	0x0	Thermal shutdown protection for IGBT enable: 0x0 = Disabled 0x1 = Enabled
0	UVOV3_EN	R/W	0x0	VEE2 UVLO and OVLO function enable: 0x0 = Disabled 0x1 = Enabled

7.6.1.5 CFG5 Register

CFG5 is shown in 図 7-49 and described in 表 7-10.

Return to Summary Table.

図 7-49. CFG5 Register

15	14	13	12	11	10	9	8
GM_STO2LTO_DIS	DESATTH				DESAT_CHG_CURR		DESAT_DCHG_EN
RW-0x0	R/W-0xE				R/W-0x3		R/W-0x1
7	6	5	4	3	2	1	0
MCLPTH		STO_CURR		2LTOFF_STO_EN			PWM_MUTE_EN
R/W-0x1		R/W-0x0		RW-0x0			R/W-0x1

表 7-10. CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GM_STO2LTO_DIS	R/W	0x0	Disable gate monitor fault detection during STO or 2LTOFF: 0x0 = Gate monitor is enabled during STO or 2LTOFF 0x1 = Gate monitor is disabled during STO or 2LTOFF
14-11	DESATTH	R/W	0xE	DESAT detection threshold value. DESATTH is programmable from 2.5V to 10V with a 500mV resolution. Calculate DESAT with the following equation: V_{DESAT} = 2.5V + $Code_{DESATTH\ (in\ decimal)}$* 500mV
10-9	DESAT_CHG_CURR	R/W	0x3	Blanking cap charging current: 0x0 = 0.6mA 0x1 = 0.7mA 0x2 = 0.8mA 0x3 = 1mA

表 7-10. CFG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DESAT_DCHG_EN	R/W	0x1	DESAT input pull down current enable: 0x0 = disabled 0x1 = enabled
7-6	MCLPTH	R/W	0x1	Active Miller clamp threshold voltage: 0x0 = 1.5V 0x1 = 2V 0x2 = 3V 0x3 = 4V
5-4	STO_CURR	R/W	0x0	Soft turn-off current: 0x0 = 0.3A 0x1 = 0.6A 0x2 = 0.9A 0x3 = 1.2A
3-1	2LTOFF_STO_EN	R/W	0x0	STO/2LTOFF is enabled for: 0x0 = Disabled 0x1 = STO for SC and DESAT 0x2 = STO for SC, DESAT, and OC faults 0x3 = STO for SC, DESAT, OC, and PS_TSD faults 0x4 = Disabled 0x5 = 2LTOFF for SC and DESAT 0x6 = 2LTOFF for SC, DESAT, and OC faults 0x7 = 2LTOFF for SC, DESAT, OC, and PS_TSD faults
0	PWM_MUTE_EN	R/W	0x1	Mute PWM signal in case of SC/OC/OT faults: 0x0 = Muting is Disabled 0x1 = PWM is muted for t_{MUTE}

7.6.1.6 CFG6 Register

CFG6 is shown in 図 7-50 and described in 表 7-11.

Return to Summary Table.

図 7-50. CFG6 Register

15	14	13	12	11	10	9	8
OCTH				SCTH		TEMP_CURR	
R/W-0x0				R/W-0x2		R/W-0x1	
7	6	5	4	3	2	1	0
SC_BLK		OC_BLK			PS_TSDTH		
R/W-0x0		R/W-0x0			R/W-0x2		

表 7-11. CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	OCTH	R/W	0x0	Overcurrent detection threshold value: 0x0 = 200mV 0x1 = 250mV 0x2 = 300mV 0x3 = 350mV 0x4 = 400mV 0x5 = 450mV 0xF = 950mV
11-10	SCTH	R/W	0x2	Short-circuit fault detection threshold value: 0x0 = 500mV 0x1 = 750mV 0x2 = 1000mV 0x3 = 1250mV
9-8	TEMP_CURR	R/W	0x1	Constant current source for temp sensing diodes: 0x0 = 0.1mA 0x1 = 0.3mA 0x2 = 0.6mA 0x3 = 1.0mA
7-6	SC_BLK	R/W	0x0	Short-circuit detection blanking time: 0x0 = 100ns 0x1 = 200ns 0x2 = 400ns 0x3 = 800ns
5-3	OC_BLK	R/W	0x0	Over-current detection blanking time: 0x0 = 500ns 0x1 = 1000ns 0x2 = 1500ns 0x3 = 2000ns 0x4 = 2500ns 0x5 = 3000ns 0x6 = 5000ns 0x7 = 10000ns

表 7-11. CFG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PS_TSDTH	R/W	0x2	Power switch thermal shutdown threshold: 0x0 = 1.00V 0x1 = 1.25V 0x2 = 1.50V 0x3 = 1.75V 0x4 = 2.00V 0x5 = 2.25V 0x6 = 2.50V 0x7 = 2.75V

7.6.1.7 CFG7 Register

CFG7 is shown in 図 7-51 and described in 表 7-12.

Return to Summary Table.

図 7-51. CFG7 Register

15	14	13	12	11	10	9	8
UVLO2TH		OVLO2TH		UVLO3TH		OVLO3TH	
R/W-0x2		R/W-0x2		R/W-0x2		R/W-0x2	
7	6	5	4	3	2	1	0
ADC_EN	ADC_SAMP_MODE		ADC_SAMP_DLY		ADC_FAULT_P	FS_STATE_ADC_FAULT	
R/W-0x1	R/W-0x0		R/W-0x2		R/W-0x0	R/W-0x0	

表 7-12. CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UVLO2TH	R/W	0x2	VCC2 UVLO threshold: 0x0 = 16V (turnon), 15V(turnoff) 0x1 = 14V (turnon), 13V(turnoff) 0x2 = 12V (turnon), 11V(turnoff) 0x3 = 10V (turnon), 9V(turnoff)
13-12	OVLO2TH	R/W	0x2	VCC2 OVLO threshold: 0x0 = 23V (turnon), 24V(turnoff) 0x1 = 21V (turnon), 22V(turnoff) 0x2 = 19V (turnon), 20V(turnoff) 0x3 = 17V (turnon), 18V(turnoff)
11-10	UVLO3TH	R/W	0x2	VEE2 UVLO threshold: 0x0 = -3V (turnon), -2V (turnoff) 0x1 = -5V (turnon), -4V (turnoff) 0x2 = -8V (turnon), -7V (turnoff) 0x3 = -10V (turnon), -9V (turnoff)

表 7-12. CFG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	OVLO3TH	R/W	0x2	VEE2 OVLO threshold: 0x0 = -5V (turnon), -6V(turnoff) 0x1 = -7V (turnon), -8V(turnoff) 0x2 = -10V (turnon), -11V(turnoff) 0x3 = -12V (turnon), -13V(turnoff)
7	ADC_EN	R/W	0x1	ADC sampling enable: 0x0 = Disabled 0x1 = Enabled
6-5	ADC_SAMP_MODE	R/W	0x0	ADC sampling mode: 0x0 = center aligned 0x1 = edge aligned 0x2 = center hybrid mode 0x3 = RESERVED
4-3	ADC_SAMP_DLY	R/W	0x2	ADC sampling point minimum delay setting with reference to PWM rising edge: 0x0 = 280ns 0x1 = 560ns 0x2 = 840ns 0x3 = 1120ns
2	ADC_FAULT_P	R/W	0x0	Report ADC fault to nFLT1 output: 0x0 = Disabled 0x1 = Enabled
1-0	FS_STATE_ADC_FAULT	R/W	0x0	OUTH/OUTL output state during an unmasked ADC fault (VREF OV/UV, VREF ILIM, or ADC buffer overrun): 0x0 = Pulled low 0x1 = Pulled high 0x2 = Hi-Z 0x3 = No action

7.6.1.8 CFG8 Register

CFG8 is shown in 図 7-52 and described in 表 7-13.

Return to Summary Table.

図 7-52. CFG8 Register

15	14	13	12	11	10	9	8
GD_2LOFF_VOLT			GD_2LOFF_TIME			GD_2LOFF_CURR	
R/W-0x0			R/W-0x0			R/W-0x0	
7	6	5	4	3	2	1	0

図 7-52. CFG8 Register (continued)

RESERVED	CRC_DIS	GD_2LOFF_STO_EN	VREF_SEL	AI_ASC_MUX	IOUT_SEL
RW-0x0	R-0x0	R/W-0x1	R/W-0x1	R/W-0x0	R-0x0

表 7-13. CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	GD_2LOFF_VOLT	R/W	0x0	Plateau voltage during two-level turnoff: 0x0 = 6V 0x1 = 7V 0x2 = 8V 0x3 = 9V 0x4 = 10V 0x5 = 11V 0x6 = 12V 0x7 = 13V
12-10	GD_2LOFF_TIME	R/W	0x0	Duration of plateau voltage during two-level turnoff: 0x0 = 150ns 0x1 = 300ns 0x2 = 450ns 0x3 = 600ns 0x4 = 1000ns 0x5 = 1500ns 0x6 = 2000ns 0x7 = 2500ns
9-8	GD_2LOFF_CURR	R/W	0x0	Gate discharge current for transition to plateau voltage level: 0x0 = 0.3A 0x1 = 0.6A 0x2 = 0.9A 0x3 = 1.2A
7	RESERVED	R/W	0x0	This bit field is reserved. Writing to these bits sets the CFG_CRC_SEC_FAULT.
6	CRC_DIS	R/W	0x0	Disable configuration CRC check: 0x0 = Enable 0x1 = Disable
5	GD_2LOFF_STO_EN	R/W	0x1	STO is enabled for the transition from mid voltage level: 0x0 = Disable 0x1 = Enable

表 7-13. CFG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VREF_SEL	R/W	0x1	Selection of VREF voltage: 0x0 = Internal 0x1 = External
3	AI_ASC_MUX	R/W	0x0	AI5/ AI6 function selection: 0x0 = AI5 and AI6 is configured as ASC_EN and ASC input respectively. Current source pull up on AI5 is always off. 0x1 = AI5 and AI6 are configured as ADC inputs. The secondary side ASC function is disabled.
2-0	IOUT_SEL	R/W	0x0	Gate drive strength selection. IOUT_SEL may be changed while in ACTIVE mode, however the configuration CRC check must be disabled first by setting CRC_DIS=1 to avoid a configuration CRC fault 0x0 = Gate drive output stage all segments enabled 0x1 =Gate drive output stage 1/3 of segments enabled 0x2 = Gate drive output stage 1/6 of segments enabled 0x3 = Gate drive output stage 1/6 of segments enabled 0x4 = Gate drive output stage 1/6 of segments enabled 0x5 = Gate drive output stage 1/6 of segments enabled 0x6 = Gate drive output stage 1/6 of segments enabled 0x7 = Gate drive output stage 1/6 of segments enabled

7.6.1.9 CFG9 Register

CFG9 is shown in 図 7-53 and described in 表 7-14.

Return to Summary Table.

図 7-53. CFG9 Register

15	14	13	12	11	10	9	8
SPARE	SC_FAULT_P	OC_FAULT_P	GM_FAULT_P		UVLO23_FAULT_P	OVLO23_FAULT_P	PS_TSD_FAULT_P
R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x1		R/W-0x0	R/W-0x0	R/W-0x1
7	6	5	4	3	2	1	0
GD_TSD_FAULT_P	INT_COMM_SEC_FAULT_P	CFG_CRC_SEC_FAULT_P	TRIM_CRC_SEC_FAULT_P	INT_REG_SEC_FAULT_P	BIST_SEC_FAULT_P	VREG2_ILIMIT_FAULT_P	CLK_MON_SEC_FAULT_P
R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-14. CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPARE	R/W	0x1	This bit field has no effect on the driver functionality. It is covered by the CFG_CRC_SEC and does not cause a CRC automatically when written..
14	SC_FAULT_P	R/W	0x0	Report SC fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)

表 7-14. CFG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	OC_FAULT_P	R/W	0x0	Report OC fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
12-11	GM_FAULT_P	R/W	0x1	Report gate voltage monitor fault: 0x0 = No (fault masked) 0x1 = nFLT1 0x2 = nFLT2 0x3 = Indicate gate voltage state on nFLT2
10	UVLO23_FAULT_P	R/W	0x0	Report VCC2 and VEE2 UVLO faults to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
9	OVLO23_FAULT_P	R/W	0x0	Report VCC2 and VEE2 OVLO faults to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
8	PS_TSD_FAULT_P	R/W	0x1	Report power switch TSD fault to nFLT1 output: 0x0 = No (fault masked) 0x1 = Yes
7	GD_TSD_SEC_FAULT_P	R/W	0x0	Report gate driver TSD fault to nFLT1 output. The thermal shutdown shuts down the secondary side, regardless of the state of this bit: 0x0 = Yes 0x1 = No
6	INT_COMM_SEC_FAULT_P	R/W	0x1	Report internal communication fault to nFLT1 output: 0x0 = No (fault masked) 0x1 = Yes
5	CFG_CRC_SEC_FAULT_P	R/W	0x0	Report configuration register CRC fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
4	TRIM_CRC_SEC_FAULT_P	R/W	0x0	Report TRIM CRC fault to nFLT* output: 0x0 = Yes 0x1 = No (fault masked)
3	INT_REG_SEC_FAULT_P	R/W	0x0	Report internal regulator fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
2	BIST_SEC_FAULT_P	R/W	0x0	Report ABIST fault to nFLT1 and 2 output: 0x0 = Yes 0x1 = No (fault masked)

表 7-14. CFG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VREG2_ILIMIT_FAULT_P	R/W	0x0	Report VREG2 ILIMIT fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)
0	CLK_MON_SEC_FAULT_P	R/W	0x0	Report clock monitor fault to nFLT1 output: 0x0 = Yes 0x1 = No (fault masked)

7.6.1.10 CFG10 Register

CFG10 is shown in 図 7-54 and described in 表 7-15.

Return to Summary Table.

図 7-54. CFG10 Register

15	14	13	12	11	10	9	8
GD_TWN_SEC_EN	SPARE	FS_STATE_DESAT_SCP		FS_STATE_INT_REG_FAULT	RESERVED	FS_STATE_OCP	
R/W-0x1	R/W-0x1	R/W-0x0		R/W-0x0	RW-0x0	R/W-0x0	
7	6	5	4	3	2	1	0
FS_STATE_PS_TSD		SPARE		FS_STATE_GM		FS_STATE_INT_COMM_SEC	
R/W-0x0		R/W-0x0		R/W-0x2		R/W-0x0	

表 7-15. CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GD_TWN_SEC_EN	R/W	0x1	Over temperature warning of gate driver VCC2 side enable: 0x0 = Disabled 0x1 = Enabled
14	SPARE	R/W	0x1	This bit field has no effect on the driver functionality. It is covered by the CFG_CRC_SEC and does not cause a CRC automatically when written.
13-12	FS_STATE_DESAT_SCP	R/W	0x0	Default OUTH/OUTL output state in case of DESAT/SCP fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = Reserved 0x3 = No action
11	FS_STATE_INT_REG_FAULT	R/W	0x0	Default OUTH/OUTL output state in case of internal regulator fault: 0x0 = Pulled low 0x1 = No action
10	RESERVED	R/W	0x0	This bit field is reserved. Writing to these bits sets the CFG_CRC_SEC_FAULT.

表 7-15. CFG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	FS_STATE_OCP	R/W	0x0	Default OUTH/OUTL output state in case of OC fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = Reserved 0x3 = No action
7-6	FS_STATE_PS_TSD	R/W	0x0	Default state in case of IGBT OT fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = Reserved 0x3 = No action
5-4	SPARE	R/W	0x0	This bit field has no effect on the driver functionality. It is covered by the CFG_CRC_SEC and does not cause a CRC automatically when written.
3-2	FS_STATE_GM	R/W	0x2	Default state in case of gate monitor fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = Hi-Z 0x3 = No action
1-0	FS_STATE_INT_COMM_SEC	R/W	0x0	Default state in case of internal communication fault: 0x0 = Pulled low 0x1 = Pulled high 0x2 = Reserved 0x3 = No action

7.6.1.11 CFG11 Register

CFG11 is shown in 図 7-55 and described in 表 7-16.

Return to Summary Table.

図 7-55. CFG11 Register

15	14	13	12	11	10	9	8
FS_STATE_UVLO2		FS_STATE_OVLO2		FS_STATE_UVLO3		FS_STATE_OVLO3	
R/W-0x0		R/W-0x0		R/W-0x0		R/W-0x0	
7	6	5	4	3	2	1	0
FS_STATE_TRIM_CRC_SEC_FAULT		FS_STATE_CFG_CRC_SEC_FAULT		VCE_CLMP_HLD_TIME		FS_STATE_CLK_MON_SEC_FAULT	
R/W-0x0		R/W-0x0		R/W-0x0		R/W-0x0	

表 7-16. CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FS_STATE_UVLO2	R/W	0x0	OUTH/OUTL state during an unmasked VCC2 UVLO fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
13-12	FS_STATE_OVLO2	R/W	0x0	OUTH/OUTL state during an unmasked VCC2 OVLO fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
11-10	FS_STATE_UVLO3	R/W	0x0	OUTH/OUTL state during an unmasked VEE2 UVLO fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
9-8	FS_STATE_OVLO3	R/W	0x0	OUTH/OUTL state during an unmasked VEE2 OVLO fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
7-6	FS_STATE_TRIM_CRC_SEC_FAULT	R/W	0x0	OUTH/OUTL state during an unmasked TRIM CRC fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
5-4	FS_STATE_CFG_CRC_SEC_FAULT	R/W	0x0	OUTH/OUTL state during an unmasked configuration register CRC fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action
3-2	VCE_CLMP_HLD_TIME	R/W	0x0	Hold time for the VCE_CLMP function 0x0 = 100ns 0x1 = 200ns 0x2 = 300ns 0x3 = 400ns

表 7-16. CFG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	FS_STATE_CLK_MON_SEC_FAULT	R/W	0x0	OUTH/OUTL state during an unmasked clock monitor fault: 0x0 = Pulled Low 0x1 = Pulled High 0x2 = Reserved 0x3 = No action

7.6.1.12 ADCDATA1 Register

ADCDATA1 is shown in 図 7-56 and described in 表 7-17. ADCDATA1 holds digital representation of AI1 input voltage.

Return to Summary Table.

図 7-56. ADCDATA1 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-17. ADCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI1 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI1. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI1	R	0x0	DATA_AI1 holds the data from the last AI1 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI1} = DATA_AI1(decimal) × 3.519mV

7.6.1.13 ADCDATA2 Register

ADCDATA2 is shown in 図 7-57 and described in 表 7-18.DCDATA2 holds digital representation of AI3 input voltage.

Return to Summary Table.

図 7-57. ADCDATA2 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

図 7-57. ADCDATA2 Register (continued)

表 7-18. ADCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI3 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI3. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI3	R	0x0	DATA_AI3 holds the data from the last AI3 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI3} = DATA_AI3(decimal) × 3.519mV

7.6.1.14 ADCDATA3 Register

ADCDATA3 is shown in 図 7-58 and described in 表 7-19.DCDATA2 holds digital representation of AI5 input voltage.

Return to Summary Table.

図 7-58. ADCDATA3 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-19. ADCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI5 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI5. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI5	R	0x0	DATA_AI5 holds the data from the last AI5 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI5} = DATA_AI5(decimal) × 3.519mV

7.6.1.15 ADCDATA4 Register

ADCDATA4 is shown in 図 7-59 and described in 表 7-20.DCDATA2 holds digital representation of AI2 input voltage.

Return to Summary Table.

図 7-59. ADCDATA4 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0

図 7-59. ADCDATA4 Register (continued)

DATA
R-0x0

表 7-20. ADCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI2 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI2. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI2	R	0x0	DATA_AI2 holds the data from the last AI2 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI2} = DATA_AI2(decimal) × 3.519mV

7.6.1.16 ADCDATA5 Register

ADCDATA5 is shown in 図 7-60 and described in 表 7-21.Data field of AI4 ADC conversion result

Return to Summary Table.

図 7-60. ADCDATA5 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-21. ADCDATA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI4 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI4. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI4	R	0x0	DATA_AI4 holds the data from the last AI4 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI4} = DATA_AI4(decimal) × 3.519mV

7.6.1.17 ADCDATA6 Register

ADCDATA6 is shown in 図 7-61 and described in 表 7-22.Data field of AI6 ADC conversion result

Return to Summary Table.

図 7-61. ADCDATA6 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	

図 7-61. ADCDATA6 Register (continued)

7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-22. ADCDATA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_AI6 ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on AI6. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_AI6	R	0x0	DATA_AI6 holds the data from the last AI6 ADC measurement. Convert the measurement to a voltage using the following equation: V_{AI6} = DATA_AI6(decimal) × 3.519mV

7.6.1.18 ADCDATA7 Register

ADCDATA7 is shown in 図 7-62 and described in 表 7-23.Data field of internal die temperature ADC conversion result

Return to Summary Table.

図 7-62. ADCDATA7 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-23. ADCDATA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_DTEMP ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on internal die temperature. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_DTEMP	R	0x0	DATA_DTEMP holds the data from the last secondary side junction temperature ADC measurement. Convert the measurement to a temperature using the following equation: T_J = DATA_DTEMP(decimal) × 0.7015°C - 198.36°C Updated equation for PG2.1

7.6.1.19 ADCDATA8 Register

ADCDATA8 is shown in 図 7-63 and described in 表 7-24.Data field of divided OUTH ADC conversion result

Return to Summary Table.

図 7-63. ADCDATA8 Register

15	14	13	12	11	10	9	8
TIME_STAMP						DATA	
R-0x0						R-0x0	
7	6	5	4	3	2	1	0
DATA							
R-0x0							

表 7-24. ADCDATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	TIME_STAMP	R	0x0	TIME_STAMP holds the time stamp for the DATA_OUTH ADC measurement. The time stamp counter is incremented with every transition on INP, but the TIME_STAMP bits are only updated with a valid ADC conversion on VGTH. Once the counter reaches 63, it rolls over to 0 on the next edge.
9-0	DATA_OUTH	R	0x0	DATA_OUTH holds the data from the last power transistor gate threshold ADC measurement. Convert the measurement to a voltage using the following equation: V_{GTH} = DATA_OUTH(decimal) × 3.519mV

7.6.1.20 CRCDATA Register

CRCDATA is shown in 図 7-64 and described in 表 7-25.

Return to Summary Table.

図 7-64. CRCDATA Register

15	14	13	12	11	10	9	8
CRC_TX							
R/W-0xFF							
7	6	5	4	3	2	1	0
CRC_RX							
R-0xFF							

表 7-25. CRCDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CRC_TX	R/W	0xFF	CRC_TX holds the CRC for the received SPI data. The CRC is continuously updated as SPI messages are received. CRC_TX is reset when the bits are written, triggering a comparison. If the comparison fails, the STATUS2[SPI_FAULT] is set.
7-0	CRC_RX	R	0xFF	CRC_RX holds the CRC for the sent SPI data. The CRC is continuously updated as the SPI messages are sent from SDO. CRC_RX is reset when CONTROL1[CLR_SPI_CRC] is written to '1'.

7.6.1.21 SPITEST

SPITEST is shown in 図 7-65 and described in 表 7-26.

Return to Summary Table.

図 7-65. SPITEST Register

15	14	13	12	11	10	9	8
SPI_TEST							
R/W-0x0							
7	6	5	4	3	2	1	0
SPI_TEST						SPI_TEST	
R/W-0x0						R/W-0x0	

表 7-26. SPITEST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SPI_TEST	R/W	0x0	Writing non-zero value to SPI_TEST triggers the STATUS2[CFG_CRC_PRI_FAULT].

7.6.1.22 GDADDRESS Register

GDADDRESS is shown in 図 7-66 and described in 表 7-27.

Return to Summary Table.

図 7-66. GDADDRESS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED				GD_ADDR			
R-0x0				R-0x0			

表 7-27. GDADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0x0	This bit field is reserved.
3-0	GD_ADDR	R	0x0	GD_ADDR stores the chip address. This field is updated during Configuration 1 when using the SPI Addressing mode. See the セクション 8.1.2 section for more details.

7.6.1.23 STATUS1 Register

STATUS1 is shown in 図 7-67 and described in 表 7-28.

Return to Summary Table.

図 7-67. STATUS1 Register

15	14	13	12	11	10	9	8
INP_STATE	INN_STATE	RESERVED		EN_STATE	RESERVED		OPM
R-0x0	R-0x0	R-0x0		R-0x0	R-0x0		R-0x1
7	6	5	4	3	2	1	0
OPM		PWM_COMP_CHK_FAULT	**RESERVED**			GD_TWN_PRI_FAULT	RESERVED
R-0x1		R-0x0	R-0x0			R-0x0	R-0x0

表 7-28. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INP_STATE	R	0x0	Indicates the input signal logic level at IN+: 0x0 = LOW 0x1 = HIGH
14	INN_STATE	R	0x0	Indicates the input signal logic level at IN-: 0x0 = LOW 0x1 = HIGH
13-12	RESERVED	R	0x0	This bit field is reserved.
11	ASC_EN_STATE	R	0x0	Indicates the input signal logic level at pin ASC_EN: 0x0 = LOW 0x1 = HIGH
10-9	RESERVED	R	0x0	This bit field is reserved.
8-6	OPM	R	0x1	Indicates the current operational state of the device: 0x0 = Error 0x1 = Configuration 1 0x2 = Configuration 2 0x3 = Active 0x4 = Error 0x5 = Error 0x6 = Error 0x7 = Error
5	PWM_COMP_CHK_FAULT	R	0x0	PWM comparison function check triggers a fault when the input to the secondary side is not the same as the IN+ input: 0x0 = No fault 0x1 = Fault
4-2	RESERVED	R	0x0	This bit field is reserved.
1	GD_TWN_PRI_FAULT	R	0x0	Gate driver over temperature warning triggers a fault when the temperature of the primary (VCC1)side is greater than the T_{WN_SET} threshold. This bit is cleared when the temperature drops below the threshold, followed by a read of the STATUS1 register: 0x0 = No fault 0x1 = Fault
0	RESERVED	R	0x0	This bit field is reserved.

7.6.1.24 STATUS2 Register

STATUS2 is shown in 図 7-68 and described in 表 7-29.

Return to Summary Table.

図 7-68. STATUS2 Register

15	14	13	12	11	10	9	8
RESERVED	PRI_RDY	UVLO1_FAULT	OVLO1_FAULT	STP_FAULT	VREG1_ILIM_FAULT	SPI_FAULT	INT_REG_PRI_FAULT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
INT_COMM_PRI_FAULT	BIST_PRI_FAULT	CLK_MON_PRI_FAULT	CFG_CRC_PRI_FAULT	TRIM_CRC_PRI_FAULT	DRV_EN_RCVD	OR_NFLT1_PRI	OR_NFLT2_PRI
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

表 7-29. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	This bit field is reserved.
14	PRI_RDY	R	0x0	Primary side is ready for operations: 0x0 = Not ready 0x1 = Ready
13	UVLO1_FAULT	R	0x0	A UVLO1_FAULT fault is triggered when V_{VCC1} < V_{UVLO1_LEVEL}: 0x0 = No fault 0x1 = Fault
12	OVLO1_FAULT	R	0x0	A OVLO1_FAULT fault is triggered when V_{VCC1} > V_{OVLO1_LEVEL}: 0x0 = No fault 0x1 = Fault
11	STP_FAULT	R	0x0	A Shoot-through protection fault is triggered when the IN- and IN+ logic levels are high at the same time: 0x0 = No fault 0x1 = Fault
10	VREG1_ILIMIT_FAULT	R	0x0	A VREG1_ILIMIT_FAULT fault is triggered when the VREG1 current limit is active: 0x0 = No fault 0x1 = Fault
9	SPI_FAULT	R	0x0	A SPI communication fault is triggered when nCS transitions low and high without receiving a proper amount of SCLK pulses (multiple of 16) or mismatch in the CRC_TX data written by the user. This bit is cleared when a valid SPI command is received, followed by a read of the STATUS2 register: 0x0 = No fault 0x1 = Fault
8	INT_REG_PRI_FAULT	R	0x0	A primary side internal regulator fault is triggered when an internal rail on the primary side (including VREG1) experiences an OV or UV event: 0x0 = No fault 0x1 = Fault

表 7-29. STATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INT_COMM_PRI_FAULT	R	0x0	A primary side internal communication fault is triggered when the communication from the secondary to the primary side is disrupted: 0x0 = No fault 0x1 = Fault
6	BIST_PRI_FAULT	R	0x0	A primary side BIST diagnosis fault is triggered when the latent check BIST fails during primary side power-up: 0x0 = No fault 0x1 = Fault
5	CLK_MON_PRI_FAULT	R	0x0	A primary side Clock monitor fault is triggered when the received clock from the secondary side is mismatched from the primary clock: 0x0 = No fault 0x1 = Fault
4	CFG_CRC_PRI_FAULT	R	0x0	A primary side configuration register CRC fault is triggered if a configuration bit for the primary side registers (CFG1, CFG2, CF3) changes while in ACTIVE mode. Additionally, CFG_CRC_PRI_FAULT is set if the SPITEST register or one of the RESERVED bits in the primary side registers is written while in the Configuration 2 state: 0x0 = No fault 0x1 = Fault
3	TRIM_CRC_PRI_FAULT	R	0x0	A primary side internal data CRC fault is triggered if one of the internal bits held in memory changes. The trim register CRC is monitored in Configuration 2 and ACTIVE states: 0x0 = No fault 0x1 = Fault
2	DRV_EN_RCVD	R	0x0	Indicates if a DRV_EN command has been received. 0x0=Driver not enabled 0x1=Driver is enabled
1	OR_NFLT1_PRI	R	0x0	Indicates the logic OR of all primary side faults reporting to pin nFLT1.
0	OR_NFLT2_PRI	R	0x0	Indicates the logic OR of all primary side faults reporting to pin nFLT2.

7.6.1.25 STATUS3 Register

STATUS3 is shown in 図 7-69 and described in 表 7-30.

Return to Summary Table.

図 7-69. STATUS3 Register

15	14	13	12	11	10	9	8
GM_STATE	GM_FAULT	INT_REG_SEC_FAULT	INT_COMM_SEC_FAULT	MCLP_STATE	OVLO3_FAULT	UVLO3_FAULT	OVLO2_FAULT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

図 7-69. STATUS3 Register (continued)

7	6	5	4	3	2	1	0
UVLO2_FAULT	VCEOV_FAULT	PS_TSD_FAULT	RESERVED	VREG2_ILIMIT_FAULT	SC_FAULT	OC_FAULT	DESAT_FAULT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

表 7-30. STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GM_STATE	R	0x0	Indicates the logic state of power transistor gate voltage. The gate is monitored using OUTH or OUTL depending on the expected output state of the driver (OUTL monitored when OUTH is pulled high and vice versa): 0x0 = LOW 0x1 = HIGH
14	GM_FAULT	R	0x0	Gate voltage monitor fault is triggered when the GM_STATE does not match expected output: 0x0 = No fault 0x1 = Fault
13	INT_REG_SEC_FAULT	R	0x0	Internal regulator fault: 0x0 = No fault 0x1 = Fault
12	INT_COMM_SEC_FAULT	R	0x0	A secondary side internal regulator fault is triggered when an internal rail on the secondary side (including VREG2) experiences an OV or UV event: 0x0 = No fault 0x1 = Fault
11	MCLP_STATE	R	0x0	Indicates the Active Miller clamp output state: 0x0 = Active Miller clamp is not active. $V_{OUTH} > V_{CLPTH}$ 0x1 = Active Miller clamp is active. $V_{OUTH} < V_{CLPTH}$
10	OVLO3_FAULT	R	0x0	A OVLO3_FAULT fault is triggered when $V_{VEE2} < V_{OVLO3TH}$. CFG4[UVOV3_EN] must be '1' to enable VEE2 OV and UV faults: 0x0 = No fault 0x1 = Fault
9	UVLO3_FAULT	R	0x0	A UVLO3_FAULT fault is triggered when $V_{VEE2} > V_{UVLO3TH}$. CFG4[UVOV3_EN] must be '1' to enable VEE2 OV and UV faults: 0x0 = No fault 0x1 = Fault
8	OVLO2_FAULT	R	0x0	A OVLO2_FAULT fault is triggered when $V_{VCC2} > V_{OVLO2TH}$. CFG4[OV2_DIS] must be '0' to enable VCC2 OV faults: 0x0 = No fault 0x1 = Fault

表 7-30. STATUS3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	UVLO2_FAULT	R	0x0	A UVLO2_FAULT fault is triggered when V_{VCC2} < $V_{UVLO2TH}$. CFG4[UV2_DIS] must be '0' to enable VCC2 UV faults: 0x0 = No fault 0x1 = Fault
6	VCEOV_FAULT	R	0x0	Indicates that the active VCE clamp function triggered a soft-turn off event. CFG4[VCECLP_EN] must be '1' to enable VCEOV_FAULT: 0x0 = No fault 0x1 = Fault
5	PS_TSD_FAULT	R	0x0	One of the enabled power switch temperature inputs (AI1, AI3, AI5) is above the PS_TSDTH threshold: 0x0 = No fault 0x1 = Fault
4	RESERVED	R	0x0	This bit field is reserved.
3	VREG2_ILIMIT_FAULT	R	0x0	A VREG2_ILIMIT_FAULT fault is triggered when the VREG2 current limit is active: 0x0 = No fault 0x1 = Fault
2	SC_FAULT	R	0x0	One or more of the enabled power switch current inputs (AI2, AI4, AI6) is above the SCTH threshold indicating a short circuit fault: 0x0 = No fault 0x1 = Fault
1	OC_FAULT	R	0x0	One or more of the enabled power switch current inputs (AI2, AI4, AI6) is above the OCTH threshold indicating a, over current fault: 0x0 = No fault 0x1 = Fault
0	DESAT_FAULT	R	0x0	DESAT fault is triggered when V_{DESAT} > $V_{DESATTH}$ indicating an over current fault: 0x0 = No fault 0x1 = Fault

7.6.1.26 STATUS4 Register

STATUS4 is shown in 図 7-70 and described in 表 7-31.

Return to Summary Table.

図 7-70. STATUS4 Register

15	14	13	12	11	10	9	8
RESERVED	VCE_STATE	GD_TWN_SEC_FAULT	GD_TSD_SEC_FAULT	RESERVED	OR_NFLT1_SEC	OR_NFLT2_SEC	BIST_SEC_FAULT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

図 7-70. STATUS4 Register (continued)

7	6	5	4	3	2	1	0
CLK_MON_SEC_FAULT	CFG_CRC_SEC_FAULT	TRIM_CRC_SEC_FAULT	RESERVED				SEC_RDY
R-0x0	R-0x0	R-0x0	R-0x0				R-0x0

表 7-31. STATUS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	This bit field is reserved.
14	VCE_STATE	R	0x0	State of VCE voltage: 0x0 = Low 0x1 = High
13	GD_TWN_SEC_FAULT	R	0x0	Gate driver over temperature warning triggers a fault when the temperature of the secondary (VCC2) side is greater than the T_{WN_SET} threshold. This bit is cleared when the temperature drops below the threshold, followed by a read of the STATUS4 register: 0x0 = No fault 0x1 = Fault
12	GD_TSD_SEC_FAULT	R	0x0	Gate driver thermal shutdown triggers a fault when the temperature of the secondary (VCC2) side is greater than the T_{SD_SET} threshold: 0x0 = No fault 0x1 = Fault
11	RESERVED	R	0x0	This bit field is reserved.
10	OR_NFLT1_SEC	R	0x0	Indicates the logic OR of all secondary side faults reporting to pin nFLT1.
9	OR_NFLT2_SEC	R	0x0	Indicates the logic OR of all secondary side faults reporting to pin nFLT2.
8	BIST_SEC_FAULT	R	0x0	A secondary side BIST diagnosis fault is triggered when the latent check BIST fails during secondary side power-up: 0x0 = No fault 0x1 = Fault
7	CLK_MON_SEC_FAULT	R	0x0	A secondary side clock monitor fault is triggered when the received clock from the primary side is mismatched from the secondary clock: 0x0 = No fault 0x1 = Fault
6	CFG_CRC_SEC_FAULT	R	0x0	A secondary side configuration register CRC fault is triggered if a configuration bit for the secondary side registers (CFG4 - CF11) changes while in ACTIVE mode. Additionally, CFG_CRC_SEC_FAULT is set if the SPITEST register or one of the RESERVED bits in the secondary side registers is written while in the Configuration 2 state: 0x0 = No fault 0x1 = Fault

表 7-31. STATUS4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TRIM_CRC_SEC_FAULT	R	0x0	A secondary side internal data CRC fault is triggered if one of the internal bits held in memory changes. The trim register CRC is monitored in Configuration 2 and ACTIVE states: 0x0 = No fault 0x1 = Fault
4-1	RESERVED	R	0x0	This bit field is reserved
0	SEC_RDY	R	0x0	Secondary side is ready for operations: 0x0 = Not ready 0x1 = Ready

7.6.1.27 STATUS5 Register

STATUS5 is shown in 図 7-71 and described in 表 7-32.

Return to Summary Table.

図 7-71. STATUS5 Register

15	14	13	12	11	10	9	8
ADC_FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESERVED
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

表 7-32. STATUS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ADC_FAULT	R	0x0	ADC_FAULT indicates that a fault has occurred in the VREF or during the ADC data transfer to the primary side. This fault only indicates faults when the ADC is enabled. 0x0 = No fault 0x1 = Fault condition. The VREF supply is out of range (OV, UV, or in current limit), or the IN+ signal is faster than guaranteed operation while ADC is enabled (30kHz).
14-0	RESERVED	R	0x0	This bit field is reserved

7.6.1.28 CONTROL1 Register

CONTROL1 is shown in 図 7-72 and described in 表 7-33. To write data in ACTIVE state, disable the configuration CRC check by setting CRC_DIS=1 before writing the data. The only exception to this is the CLR_SPI_CRC bit. This bit can be written in ACTIVE mode without disabling the CRC.

Return to Summary Table.

図 7-72. CONTROL1 Register

15	14	13	12	11	10	9	8

図 7-72. CONTROL1 Register (continued)

CLR_SPI_CRC	RESERVED						CFG_CRC_CHK_PRI
R/W-0x0	R-0x0						R/W-0x0
7	6	5	4	3	2	1	0
PWM_COMP_CHK	RESERVED	STP_CHK	RESERVED				CLK_MON_CHK_PRI
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0				R/W-0x0

表 7-33. CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR_SPI_CRC	R/W	0x0	Clear SPI CRC code: 0x0 = No 0x1 = Yes
14-9	RESERVED	R	0x0	This bit field is reserved
8	CFG_CRC_CHK_PRI	R/W	0x0	Run CRC check of configuration register bits of primary (VCC1) side: 0x0 = No 0x1 = Yes
7	PWM_COMP_CHK	R/W	0x0	Run PWM signal comparison function check. PWM comparator generates PWM fault to set PWM_COMP_CHK_FAULT. This is only available in Configuration 2: 0x0 = No 0x1 = Yes
6	RESERVED	R/W	0x0	This bit field is reserved
5	STP_CHK	R/W	0x0	Run the check of STP function. shoot through protection generates STP fault to set STP_FAULT: 0x0 = No 0x1 = Yes
4-1	RESERVED	R	0x0	This bit field is reserved
0	CLK_MON_CHK_PRI	R/W	0x0	Run clock monitor check. Primary side clock monitor generates clock monitor fault to set CLK_MON_PRI_FAULT. SPI functions normally during this test: 0x0 = No 0x1 = Yes

7.6.1.29 CONTROL2 Register

CONTROL2 is shown in 図 7-73 and described in 表 7-34. To write data in ACTIVE state, disable the configuration CRC check by setting CRC_DIS=1 before writing the data.

Return to Summary Table.

図 7-73. CONTROL2 Register

15	14	13	12	11	10	9	8

図 7-73. CONTROL2 Register (continued)

CLR_STAT_REG	RESERVED	GATE_OFF_CHK	GATE_ON_CHK	VCECLP_CHK	RESERVED	DESAT_CHK	SCP_CHK
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
OCP_CHK	RESERVED	VGTH_MEAS	RESERVED	CLK_MON_CHK_SEC	CFG_CRC_CHK_SEC	PS_TSD_CHK_SEC	RESERVED
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-34. CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR_STAT_REG	R/W	0x0	Clear status register. This bit is set back 0 once status register is cleared. Reading this bit always returns 0: 0x0 = No 0x1 = Yes
14	RESERVED	R/W	0x0	This bit field is reserved.
13	GATE_OFF_CHK	R/W	0x0	Check the continuity of gate turnoff path. The gate monitor comparator generates off-state fault to test the GM_FAULT while the gate is off. This function is used in ACTIVE mode with the CRC_DIS bit set. The MCU or the external controller controls IN+/IN- to turn off OUTH before sending this command. The gate driver output is pulled low and does not respond to IN+/IN- until GM_FAULT and this bit is cleared. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = OFF 0x1 = ON
12	GATE_ON_CHK	R/W	0x0	Check the continuity of gate turnon path. The gate monitor comparator generates on-state fault to test the GM_FAULT while the gate is on. This function is used in ACTIVE mode with the CRC_DIS bit set. The gate driver output is pulled low. MCU or the external controller controls IN+/IN- to turn on OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = OFF 0x1 = ON
11	VCECLP_CHK	R/W	0x0	Manual VCECLP BIST. The VCECLAMP comparator generates VCE over voltage fault to set VCEOV_FAULT. This function is used in ACTIVE mode with the CRC_DIS bit set. MCU or the external controller controls IN+/IN- to turn off OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = No 0x1 = Yes
10	RESERVED	R/W	0x0	Reserved

表 7-34. CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DESAT_CHK	R/W	0x0	Manual DESAT BIST. The DESAT comparator generates DESAT fault to set DESAT_FAULT. This function is used in ACTIVE mode with the CRC_DIS bit set. MCU or the external controller controls IN+/IN- to turn on OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = No 0x1 = Yes
8	SCP_CHK	R/W	0x0	Manual SCP BIST. The SCP comparator generates short circuit fault to set SC_FAULT. This function is used in ACTIVE mode with the CRC_DIS bit set. MCU or the external controller controls IN+/IN- to turn on OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = No 0x1 = Yes
7	OCP_CHK	R/W	0x0	Manual OCP BIST. The OCP comparator generates over current fault to set OC_FAULT. This function is used in ACTIVE mode with the CRC_DIS bit set. MCU or the external controller controls IN+/IN- to turn on OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = No 0x1 = Yes
6	RESERVED	R/W	0x0	Reserved
5	VGTH_MEAS	R/W	0x0	Run VGTH measurement function. Refer to the セクション 7.3.5.14 section. This is only available in Configuration 2: 0x0 = No 0x1 = Yes
4	RESERVED	R/W	0x0	Reserved
3	CLK_MON_CHK_SEC	R/W	0x0	Manual clock monitor BIST. Secondary side clock monitor generates clock monitor fault to set CLK_MON_SEC_FAULT. SPI function normally during this test: 0x0 = No 0x1 = Yes
2	CFG_CRC_CHK_SEC	R/W	0x0	Run CRC check of configuration bits of VCC2 side, Secondary side configuration CRC generates CRC fault to set CFG_CRC_SEC_FAULT: 0x0 = No 0x1 = Yes

表 7-34. CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PS_TSD_CHK_SEC	R/W	0x0	Check power switch TSD protection function. The Power Switch over temperature protection generates over temperature fault to set PS_TSD_FAULT. This function is used in ACTIVE mode with the CRC_DIS bit set. MCU or the external controller controls IN+/IN- to turn on OUTH before sending this command. Ensure that the CRC_DIS bit is cleared after performing the necessary latent function checks to enable the CRC function: 0x0 = No 0x1 = Yes
0	RESERVED	R/W	0x0	This bit field is reserved.

7.6.1.30 ADCCFG Register

ADCCFG is shown in 図 7-74 and described in 表 7-35.

Return to Summary Table.

図 7-74. ADCCFG Register

15	14	13	12	11	10	9	8
RESERVED	ADC_ON_CH_SEL_7	ADC_ON_CH_SEL_6	ADC_ON_CH_SEL_5	ADC_ON_CH_SEL_4	ADC_ON_CH_SEL_3	ADC_ON_CH_SEL_2	ADC_ON_CH_SEL_1
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RESERVED	ADC_OFF_CH_SEL_7	ADC_OFF_CH_SEL_6	ADC_OFF_CH_SEL_5	ADC_OFF_CH_SEL_4	ADC_OFF_CH_SEL_3	ADC_OFF_CH_SEL_2	ADC_OFF_CH_SEL_1
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R-0x0

表 7-35. ADCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved
14	ADC_ON_CH_SEL_7	R/W	0x0	The die temperature is enabled for sampling during the PWM ON ADC round robin. Die temperature data is returned to ADCDATA7. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
13	ADC_ON_CH_SEL_6	R/W	0x0	The AI6 channel is enabled for sampling during the PWM ON ADC round robin. AI6 data is returned to ADCDATA6. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
12	ADC_ON_CH_SEL_5	R/W	0x0	The AI4 channel is enabled for sampling during the PWM ON ADC round robin. AI4 data is returned to ADCDATA5. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes

表 7-35. ADCCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ADC_ON_CH_SEL_4	R/W	0x0	The AI2 channel is enabled for sampling during the PWM ON ADC round robin. AI2 data is returned to ADCDATA4. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
10	ADC_ON_CH_SEL_3	R/W	0x0	The AI5 channel is enabled for sampling during the PWM ON ADC round robin. AI5 data is returned to ADCDATA3. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
9	ADC_ON_CH_SEL_2	R/W	0x0	The AI3 channel is enabled for sampling during the PWM ON ADC round robin. AI3 data is returned to ADCDATA2. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
8	ADC_ON_CH_SEL_1	R/W	0x0	The AI1 channel is enabled for sampling during the PWM ON ADC round robin. AI1 data is returned to ADCDATA1. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
7	Reserved	R/W	0x0	Reserved
6	ADC_OFF_CH_SEL7	R/W	0x0	The die temperature is enabled for sampling during the PWM OFF ADC round robin. Die temperature data is returned to ADCDATA7. The round robin sampling order is: AI1, AI3, AI5,AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
5	ADC_OFF_CH_SEL6	R/W	0x0	The AI6 channel is enabled for sampling during the PWM OFF ADC round robin. AI6 data is returned to ADCDATA6. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
4	ADC_OFF_CH_SEL5	R/W	0x0	The AI4 channel is enabled for sampling during the PWM OFF ADC round robin. AI4 data is returned to ADCDATA5. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes

表 7-35. ADCCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ADC_OFF_CH_SEL4	R/W	0x0	The AI2 channel is enabled for sampling during the PWM OFF ADC round robin. AI2 data is returned to ADCDATA4. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
2	ADC_OFF_CH_SEL3	R/W	0x0	The AI5 channel is enabled for sampling during the PWM OFF ADC round robin. AI5 data is returned to ADCDATA3. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
1	ADC_OFF_CH_SEL2	R/W	0x0	The AI3 channel is enabled for sampling during the PWM OFF ADC round robin. AI3 data is returned to ADCDATA2. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes
0	ADC_OFF_CH_SEL1	R/W	0x0	The AI1 channel is enabled for sampling during the PWM OFF ADC round robin. AI1 data is returned to ADCDATA1. The round robin sampling order is: AI1, AI3, AI5, AI2, AI4, AI6, Die Temp: 0x0 = No 0x1 = Yes

7.6.1.31 DOUTCFG Register

DOUTCFG is shown in 図 7-75 and described in 表 7-36.

Return to Summary Table.

図 7-75. DOUTCFG Register

15	14	13	12	11	10	9	8
AI1OT_EN	AI3OT_EN	AI5OT_EN	AI2OCSC_EN	AI4OCSC_EN	AI6OCSC_EN	FREQ_DOUT	
RW-0x0	RW-0x0	RW-0x0	RW-0x1	RW-0x1	RW-0x0	R/W-0x0	
7	6	5	4	3	2	1	0
RESERVED	DOUT_TO_TJ	DOUT_TO_AI6	DOUT_TO_AI4	DOUT_TO_AI2	DOUT_TO_AI5	DOUT_TO_AI3	DOUT_TO_AI1
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R-0x0

表 7-36. DOUTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AI1OT_E	R/W	0x0	AI1 Over Temperature protection for power FET: 0x0 = Disabled 0x1 = Enabled
14	AI3OT_EN	R/W	0x0	AI3 Over Temperature protection for power FET: 0x0 = Disabled 0x1 = Enabled

表 7-36. DOUTCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	AI5OT_EN	R/W	0x0	AI5 Over Temperature protection for power FET: 0x0 = Disabled 0x1 = Enabled
12	AI2OCSC_EN	R/W	0x1	AI2 Over Current / Short circuit protection for power FET: 0x0 = Disabled 0x1 = Enabled
11	AI4OCSC_EN	R/W	0x1	AI4 Over Current / Short circuit protection for power FET: 0x0 = Disabled 0x1 = Enabled
10	AI6OCSC_EN	R/W	0x0	AI6 Over Current / Short circuit protection for power FET: 0x0 = Disabled 0x1 = Enabled
9-8	FREQ_DOUT	R/W	0x0	DOUT output frequency: 0x0 = 13.9kHz 0x1 = 27.8kHz 0x2 = 55.7kHz 0x3 = 111.4kHz
7	RESERVED	R/W	0x0	Reserved
6	DOUT_TO_TJ	R/W	0x0	Channel of die temp is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes
5	DOUT_TO_AI6	R/W	0x0	Channel AI6 is selected to output on DOUT. Only one channel can be selected at a time. : 0x0 = No 0x1 = Yes
4	DOUT_TO_AI4	R/W	0x0	Channel AI4 is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes
3	DOUT_TO_AI2	R/W	0x0	Channel AI2 is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes

表 7-36. DOUTCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DOUT_TO_AI5	R/W	0x0	Channel AI5 is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes
1	DOUT_TO_AI3	R/W	0x0	Channel AI3 is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes
0	DOUT_TO_AI1	R/W	0x0	Channel AI1 is selected to output on DOUT. Only one channel can be selected at a time.: 0x0 = No 0x1 = Yes

8 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Power Dissipation Considerations

Proper system design must assure that the device operates within safe thermal limits across the entire load range. The total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. The equation 式 4 shows total device power dissipation.

$$P_{GDL} = \left[Q_g \times f_{PWM} \times (V_{CC2} - V_{EE2}) \right] \times \frac{R_{int}}{R_{int} + R_g} + (V_{CC2} - V_{EE2}) \times I_{QVCC2} \tag{4}$$

where

- Q_g is the gate charge of the power transistor
- f_{PWM} is the PWM frequency
- V_{CC2} is the positive supply voltage
- V_{EE2} is the negative supply voltage
- R_{int} is the gate driver internal gate resistance
- R_g is the external gate resistor
- I_{QVCC2} is the quiescent supply current of VCC2

8.1.2 Device Addressing

When using the Address-based configuration for SPI communication in the system, all devices must be individually addressed. Upon entering the Configuration 1 state (indicated by nFLT* high, assuming no fault during startup), all devices are addressable 0x1 through 0xE (14 unique addresses), with 0xF being a broadcast address to which all devices respond. Addressing is done in the Configuration 1 state. In this state, the IN+ input is pulled high while the WR_CA command is sent with the defined address. The written address is stored in the GDADDRESS[GD_ADDR] bits (GDADDRESS). Once all devices are addressed, send the CFG_IN command with the broadcast device address (0xF) to lock in the device address and move to configuring the devices (Configuration 2 state). The timing diagram for the addressing is shown in Timing diagram for addressing when using the Address-based SPI Communication Scheme..

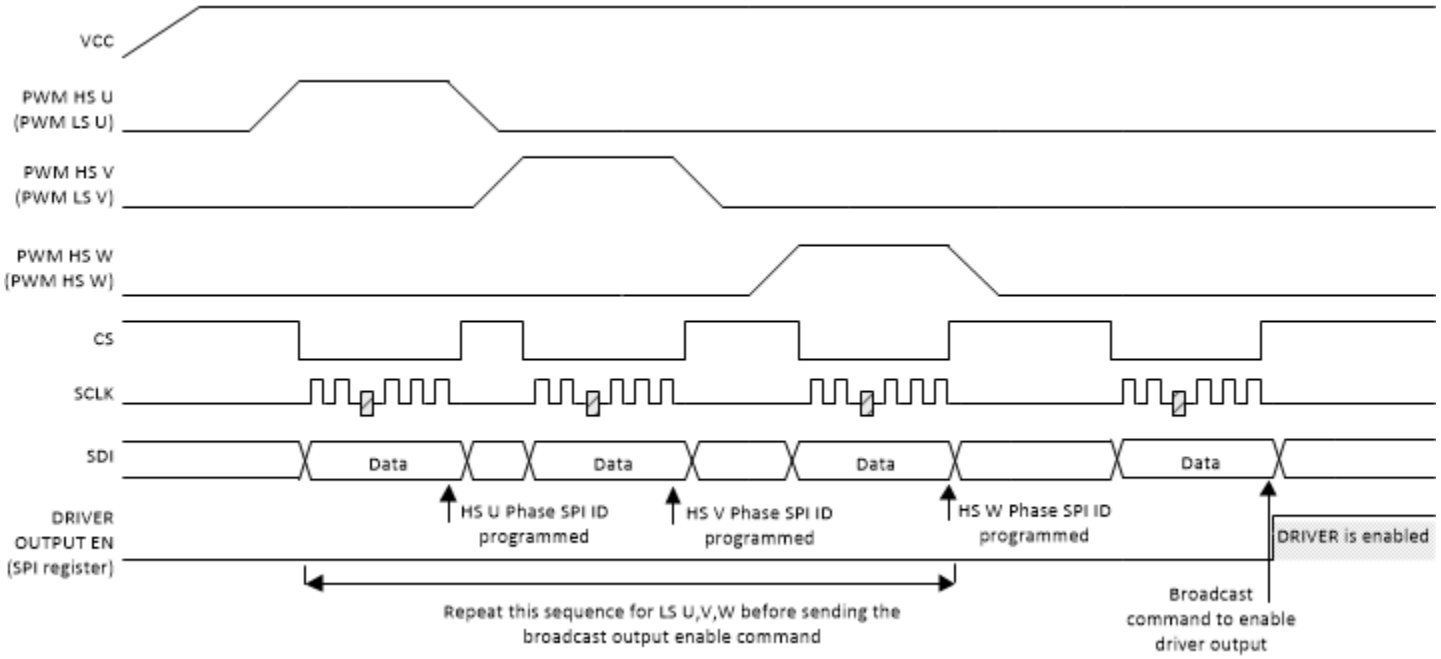


図 8-1. Timing diagram for addressing when using the Address-based SPI Communication Scheme.

8.2 Typical Application Using Internal ADC Reference and Power FET Sense Current Monitoring

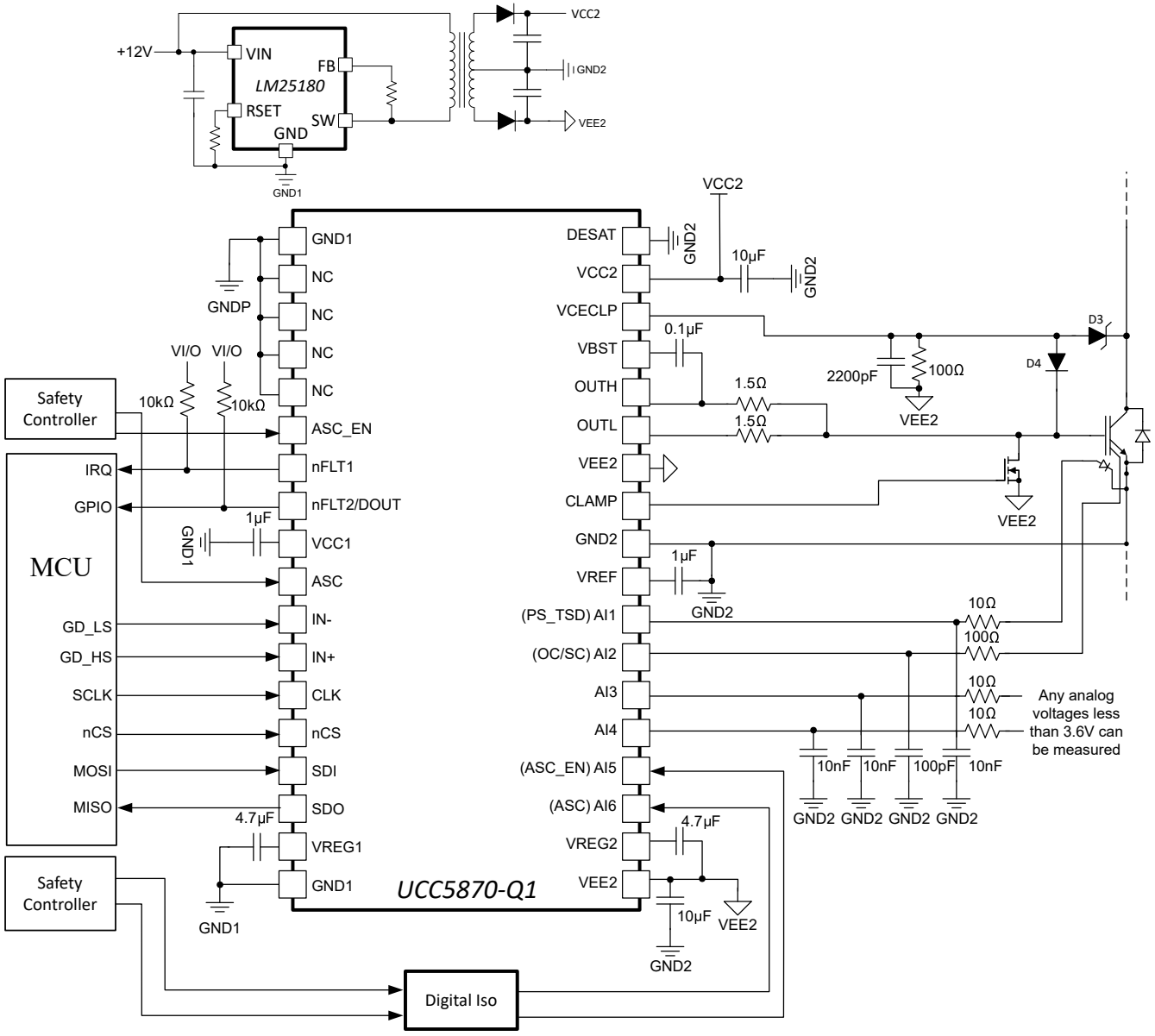


図 8-2. Typical Application Circuit using Sense FET Overcurrent Sensing

8.2.1 Design Requirements

表 8-1 lists reference design parameters for the example application: UCC51870 driving 400V IGBT transistors in a low-side configuration.

表 8-1. Design Requirements

PARAMETER	VALUE	UNITS
DC Bus Voltage	400	V
VCC1	3.3	V
VCC2	15	V
VEE2	-8	V
Switching Frequency	10	kHz

8.2.2 Detailed Design Procedure

8.2.2.1 VCC1, VCC2, and VEE2 Bypass Capacitors

Use ceramic capacitors between VCC1 and GND1, VCC2 and VGND2, and VEE2 and VGND2.

For VCC1, it is recommended to use a 0.1µF capacitor in parallel with a 1µF capacitor. Use at least a 6.3V voltage rating. For VCC2, it is recommended to use a 0.1µF capacitor in parallel with a 1µF capacitor at the pin. Bulk capacitor (>22µF) on the supply rail is required to ensure minimal droop during transitions. Use at least a 50V voltage rating. For VEE2, it is recommended to use a 0.1µF capacitor in parallel with a 1µF capacitor at the pin. Bulk capacitor (>22µF) on the supply rail is required to ensure minimal droop during transitions. Use at least a 25V voltage rating.

8.2.2.2 VREF, VREG1, and VREG2 Bypass Capacitors

Connect a ceramic capacitor between VREG1 and GND1, VREG2 and VEE2, and VREF and GND2. For the VREG1 and VREG2 outputs, it is recommended to use a 0.1µF capacitor in parallel with a 4.7µF capacitor at the pin with at least a 6.3V voltage rating. It is recommended to bypass VREF with a 1µF capacitor at the pin with at least a 6.3V voltage rating.

8.2.2.3 Bootstrap Capacitor (VBST)

Connect a ceramic capacitor between VBST and OUTH. It is recommended to use a 0.1µF capacitor with at least a 6.3V voltage rating.

8.2.2.4 VCECLP Input

The active V_{CE} clamp circuit is used to reduce V_{CE} overshoot voltage during IGBT turn off. The external circuit (図 8-3) uses four components: A high-voltage TVS diode (D1) that turns on (avalanche breakdown) if the V_{CE} overshoot during the IGBT turn-off is greater than the TVS diode avalanche limit, a filter capacitor (C_P) that is charged when D1 conducts, a diode (D2) that conducts some of the avalanche current to the IGBT gate to increase the gate voltage (V_{GE}) in order slow down the turn off transient and reduce the V_{CE} overshoot, and a resistor (R_C) to set the time constant to discharge the VCECLP node when D1 stops conducting. Select the D1 avalanche voltage rating to be the IGBT V_{CE} overshoot voltage control target. During normal operation, the V_{CE} dV/dt couples to VCECLP through junction capacitance of D1. The C_P value is selected to filter this coupled ripple voltage to prevent triggering the V_{CE} clamp function during normal operation. When a V_{CE} over voltage occurs and D1 avalanches, C_P charges to the $V_{CECLPth}$ by avalanche current, then V_{CE} clamp function triggers and OUTL driver is disabled while the STO current is enabled. The R_P value sets the the RC time constant when the C_P voltage drops below $V_{CECLPth}$. The value of R_P depends on the selection of the IGBT, D1, R_{GON}, R_{GOFF}. Typically, the Rp value is between 10 to 100 ohm and C_P value is between 10nF to 100nF. There is not a hard and fast calculation for these components. The best method is experimenting to fine tune the components for best performance in the application. See 図 8-4 for an example of performance with the UCC5870QDWJEVM-026 () EVM.

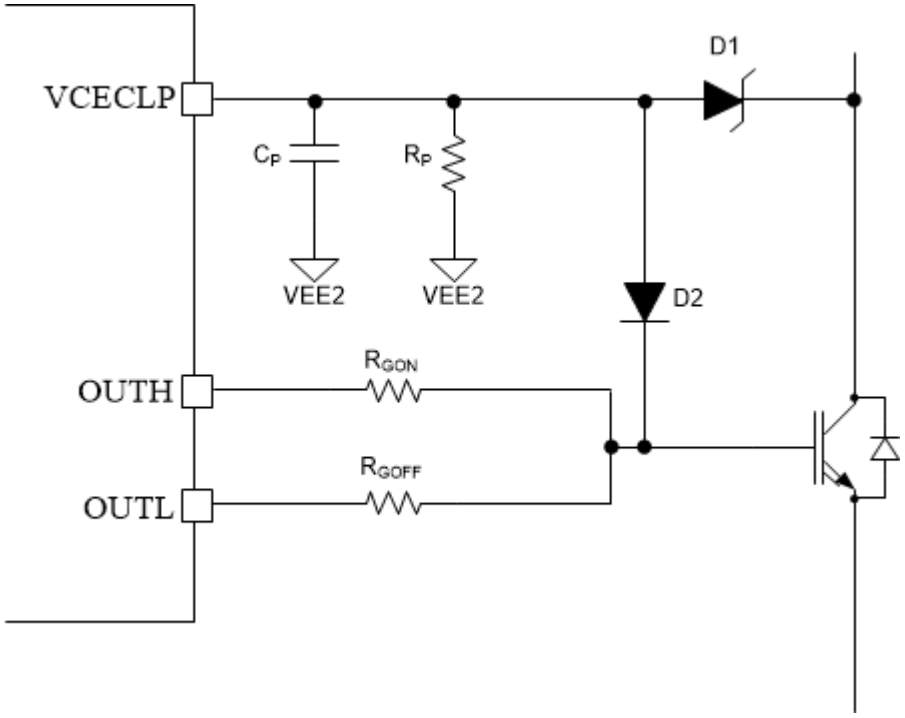


図 8-3. VCECLP External Components

8.2.2.5 External CLAMP Output

When using an external Miller clamp, select a MOSFET with the required RDSON for the desired pulldown strength. Connect CLAMP to the gate of the pulldown transistor, the drain to the gate of the external power FET, and the source to GND2 at the external power FET.

8.2.2.6 AI Inputs*

AI* require a series resistor and bypass capacitor (RC filter) to ensure best results. The values must be selected based on the required corner frequency for the input. A tradeoff must be made between response time, in the case of SCP and OCP monitoring, and the noise during ADC measurements. The DC input impedance of the AI* inputs is very high. However, as the signal frequency goes up, the input impedance decreases. The input impedance can be estimated as:

$$Z_{AI*} = \text{sqrt}(8k\Omega^2 + (1 /(2\pi \times f_S \times 1.5pF))^2) \quad (5)$$

Where f_S is the frequency of the signal. The filter The recommended RC for OCP/SCP monitoring is 100ohm and 100pF. This provides a quicker response with the drawback of more noise in the measurement. The RC chosen for the other inputs used in the application circuits is 10ohm and 10nF. All of the ADC data taken on these inputs in this datasheet are based on those RC values. For best results for ADC accuracy, it is recommended to use these components. If a different corner frequency is required, select a frequency that provides sufficient accuracy with the decreased AI* input impedance. The corner frequency is calculated using the following equation:

$$f_C = 1/ (2\pi RC) \quad (6)$$

8.2.2.7 OUTH/ OUTL Outputs

The OUTH and OUTL outputs provide split gate drive to customize the turn-on and turn-off rates to customize applications for limiting noise and ringing. A resistor from OUTH and from OUTL to the gate of the power transistor set the rise/fall time of the gate drive to the power transistor. To set the rise time, select the resistor (R_G) for OUTH and OUTL to the gate according to the following equation:

$$R_G = \omega L_S / Q \quad (7)$$

Where L_S is the inductance of the gate and Q is the quality factor between 0.5 (critically damped) and 1 (under damped). See SLLA385 () for additional information on gate resistor design. It is required that the value or RG must be greater than 1.5Ω for both OUTH and OUTL.

8.2.2.8 nFLT Outputs*

The nFLT1 and nFLT2 indicators are open-drain outputs, connect a 1k to 100k resistor from nFLT* to VCC1 to set the correct logic level.

8.2.3 Application Curves

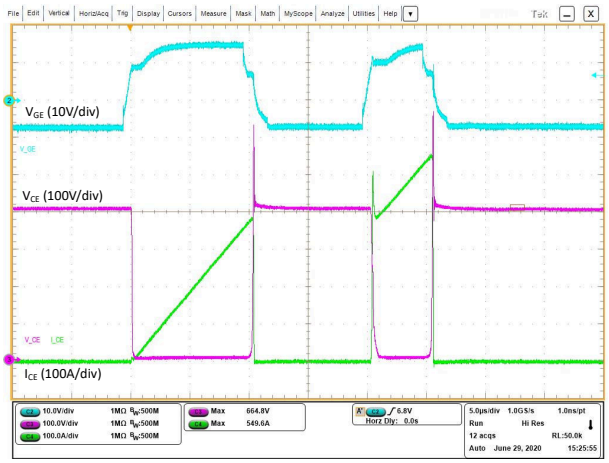


図 8-4. IGBT Double Pulse Waveform

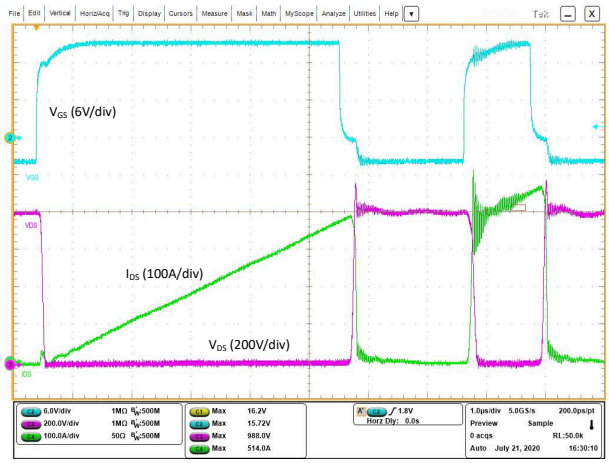


図 8-5. SiC Double Pulse Waveform

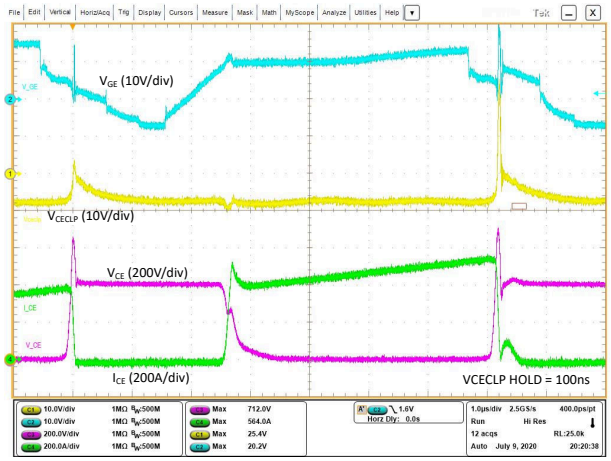


図 8-6. VCE Clamp Response with 100ns Hold Time

8.3 Typical Application Using DESAT Power FET Monitoring

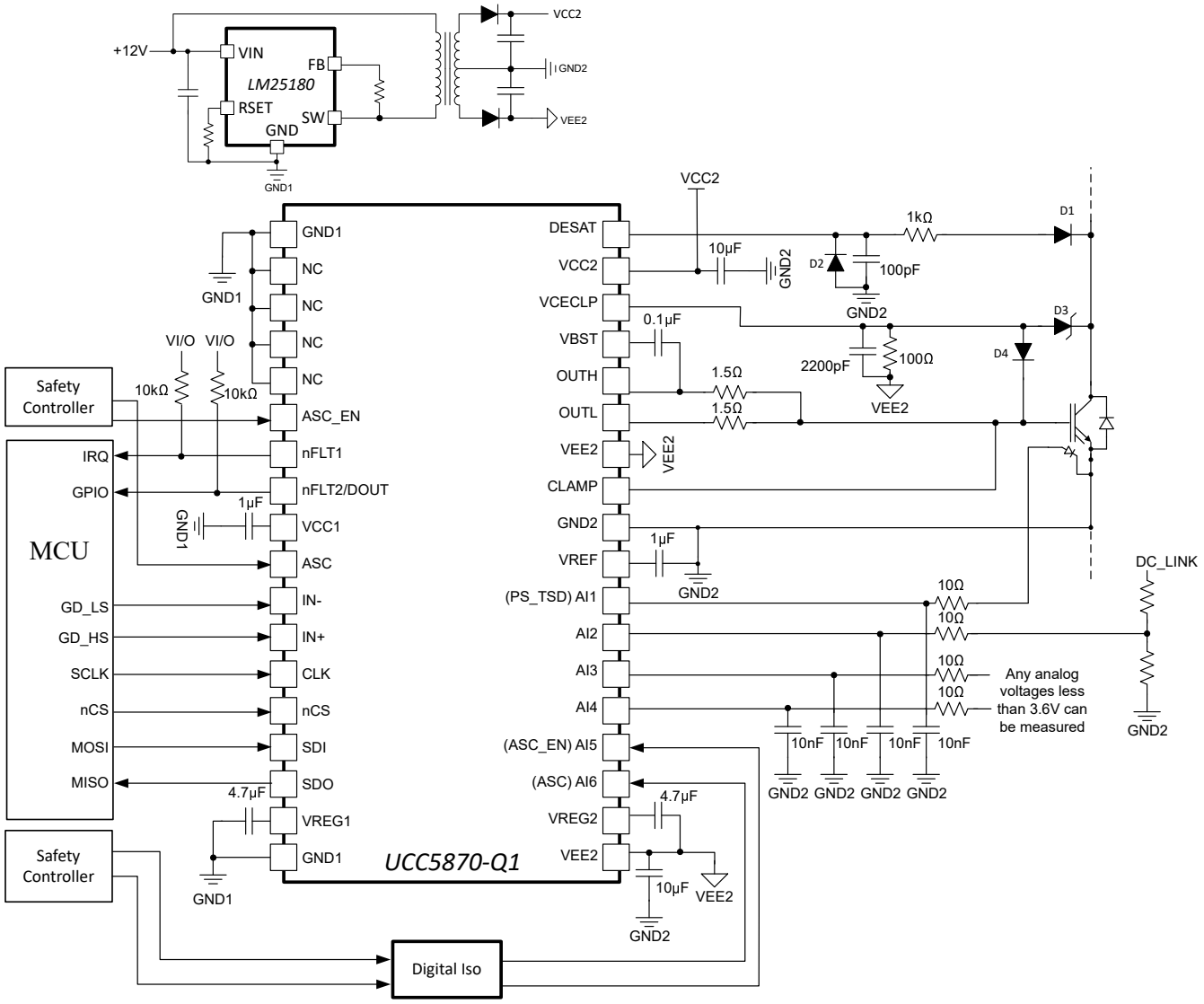


図 8-7. Typical Application Circuit using DESAT Overcurrent Protection

8.3.1 Detailed Design Procedure

See the previous section on details for selection of external components.

8.3.1.1 DESAT Input

The DESAT circuit monitors the power module (IGBT for example) for short circuit or over current protection. The external circuit includes four components (図 8-8): blanking capacitor (C_{BLK}), clamping diode (D_{CLP}), series resistor R_S and high-voltage blocking diode (D_{HV}). C_{BLK} is used to determine the blanking time, t_{BLK}. The time period for t_{BLK} must be long enough to prevent a false trigger when the during the normal operation turn-on cycle. t_{BLK} is calculated as:

$$t_{BLK} = C_{BLK} \times V_{DESATth} / I_{CHG} \quad (8)$$

The high voltage diode D_{HV} blocks the high voltage (V_{CE}) while IGBT is OFF. The voltage rating for D_{HV} must be higher than the DC bus voltage plus any switching transient voltage. It is good practice to choose a voltage rating for D_{HV} to be the same or higher than the IGBT voltage rating. Once the proper voltage rating is

determined, choose a diode with the least amount of junction capacitance to prevent coupling of DESAT with the dV/dt of the V_{CE} switching. Clamping diode, D_{CLP}, provides a current path to for any coupling current due to the aforementioned junction capacitance of D_{HV}. Select a diode large enough to handle any expected coupling current. The series resistor, R_S, dampens any oscillations in the DESAT loop and determines the actual DESAT detection V_{CE} voltage. The actual threshold is calculated as:

$$V_{DESAT,ACTUAL} = V_{DESATth} - I_{CHG} \times R_S - V_{DHV} \quad (9)$$

V_{DHV} is the forward voltage drop of the DHV diode and I_{CHG} is the blanking capacitor charging current selected using the CFG5[DESAT_CHG_CURR] bits.

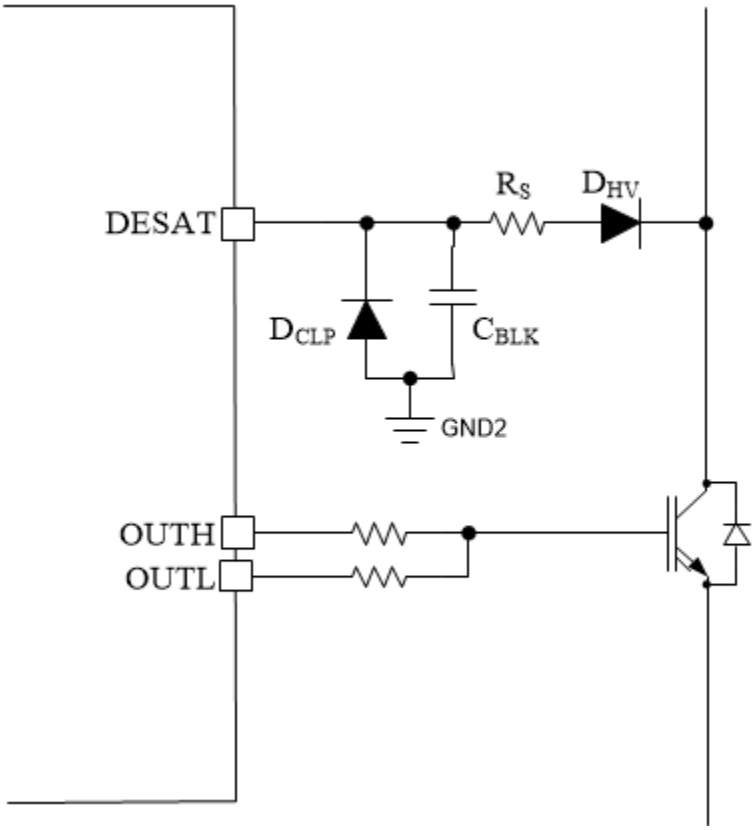


図 8-8. External Components for DESAT

8.3.2 Application Curves

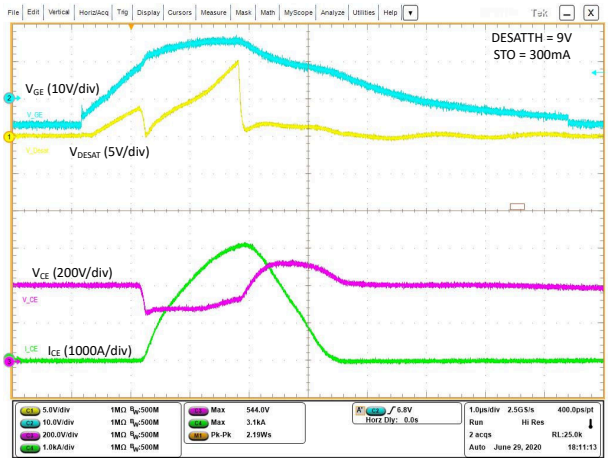


図 8-9. Soft Turn-Off (STO) Shutdown Response to DESAT Event

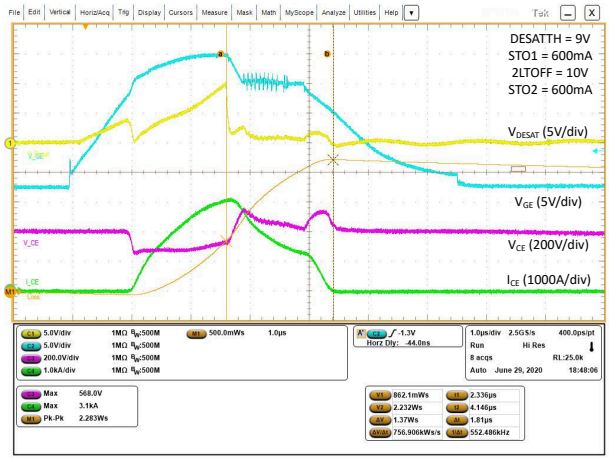


図 8-10. Two-Level Turn Off (2LTOFF) Shutdown Response to DESAT Event

9 Power Supply Recommendations

9.1 VCC1 Power Supply

The VCC1 power supply sets the logic level requirements for the primary side. Connect a 3.3V supply to VCC1 when using 3.3V logic levels, or a 5V supply when using 5V logic levels for the digital IOs.

9.2 VCC2 Power Supply

The VCC2 supply is the positive driver supply for the power transistor. Connect a 15V to 30V supply from VCC2 to GND2, depending on the drive voltage requirement for the selected transistor.

9.3 VEE2 Power Supply

The VEE2 supply is the negative driver supply for the power transistor. Connect a -12V to 0V supply from VEE2 to GND2, depending on the hold off voltage requirement for the selected power transistor.

9.4 VREF Supply (Optional)

When tighter ADC accuracy that achievable with the internal reference is required, and external precision reference may be used. Connect a 4V reference to the VREF output. The accuracy of the reference is directly proportional to the achieved accuracy of the ADC.

10 Layout

10.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the device.

10.1.1 Component Placement

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCC1 and GND1 pins and between the VCC2, VEE2 and GND2 pins to support high peak currents when turning on the external power transistor.
- Place the VBST and VREF caps as close to the device as possible.

10.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This decreases the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the diode by the VCC2 bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

10.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC51870's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the high-side and low-side drivers could operate with a DC-link voltage up to 1000 VDC, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

10.1.4 Thermal Considerations

- The power dissipated by the device is directly proportional to the drive voltage, heavy capacitive loading, and/or high switching frequency (refer to Power Dissipation Considerations section for more details). Proper PCB layout helps dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VCC2 and VEE2 is recommended, with priority on maximizing the connection to VEE2. However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VCC2 and VEE2 to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

10.2 Layout Example

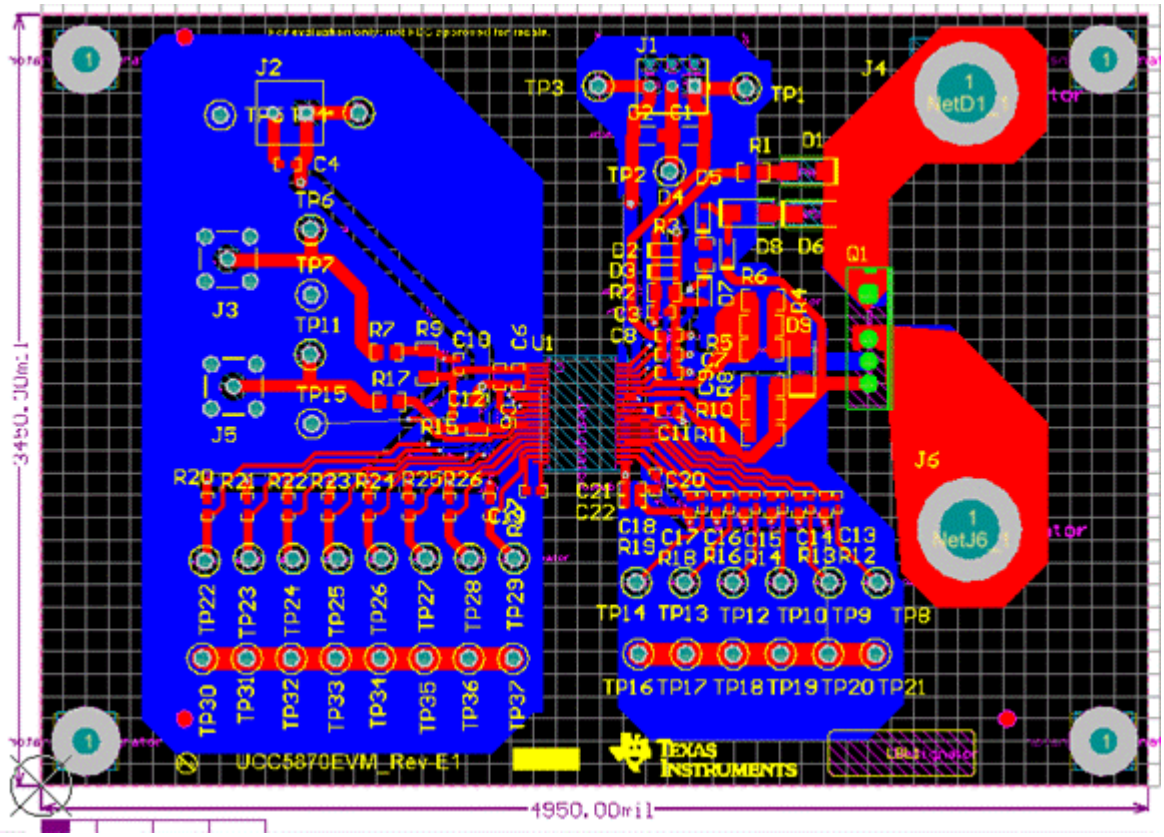


図 10-1. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*
- Documentation available to aid ISO 26262 system design up to ASIL D

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5870QDWJQ1	Obsolete	Production	SSOP (DWJ) | 36	-	-	Call TI	Call TI	-40 to 125	UCC5870Q
UCC5870QDWJRQ1	Active	Production	SSOP (DWJ) | 36	750 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5870Q
UCC5870QDWJRQ1.A	Active	Production	SSOP (DWJ) | 36	750 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5870Q
UCC5870QDWJRQ1.B	Active	Production	SSOP (DWJ) | 36	750 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

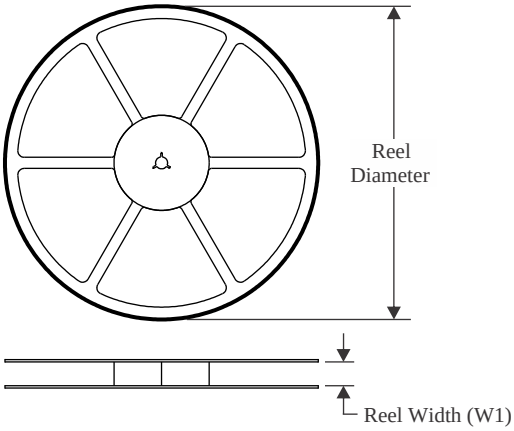
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

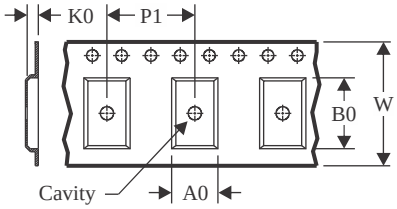
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

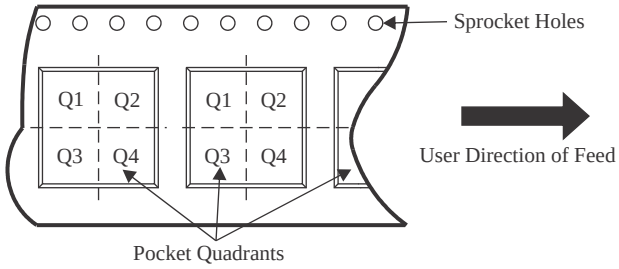


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

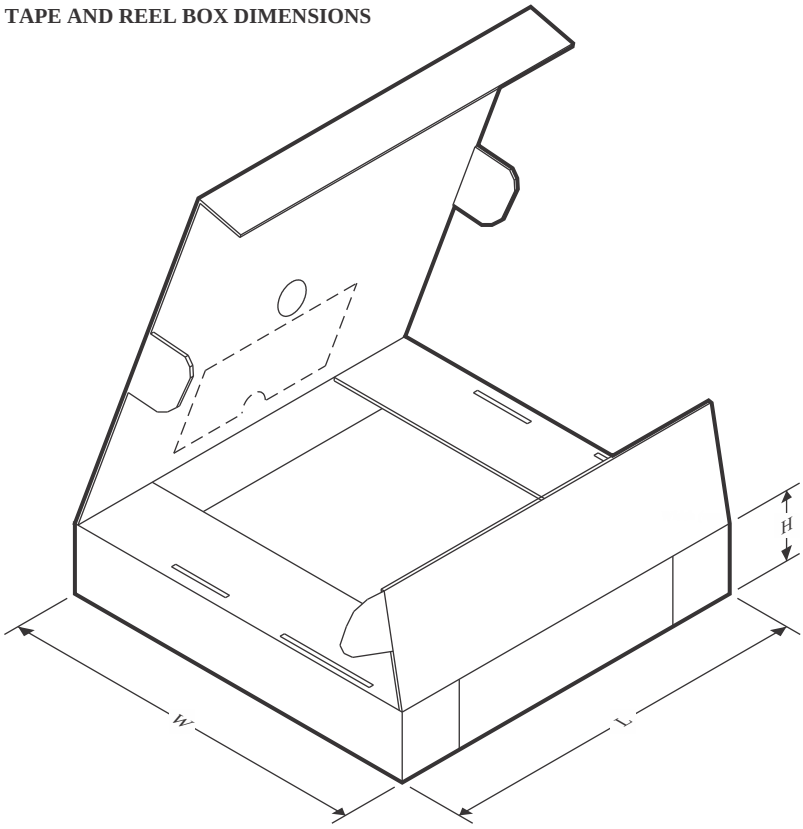
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5870QDWJRQ1	SSOP	DWJ	36	750	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

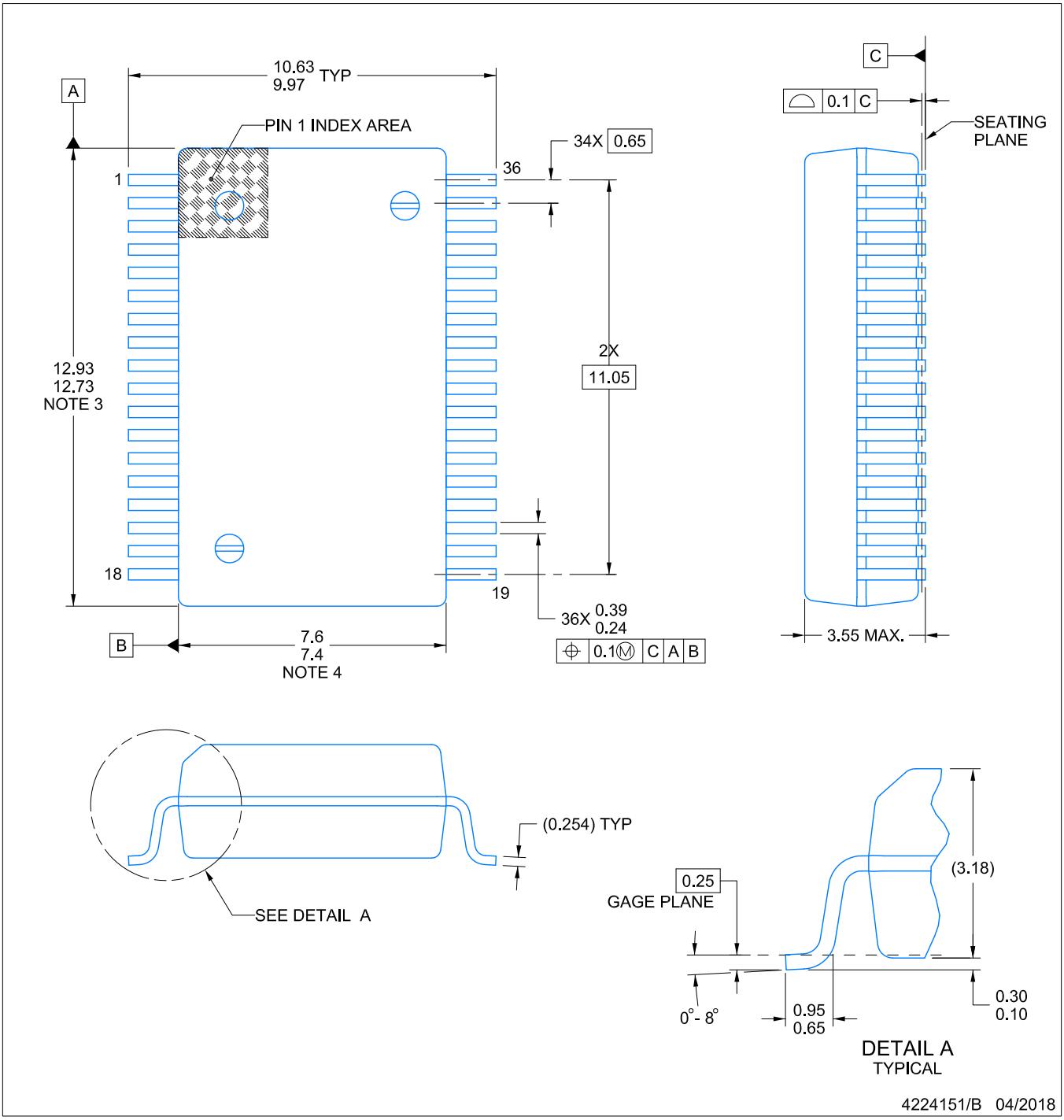
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5870QDWJRQ1	SSOP	DWJ	36	750	350.0	350.0	43.0

PACKAGE OUTLINE

DWJ0036A

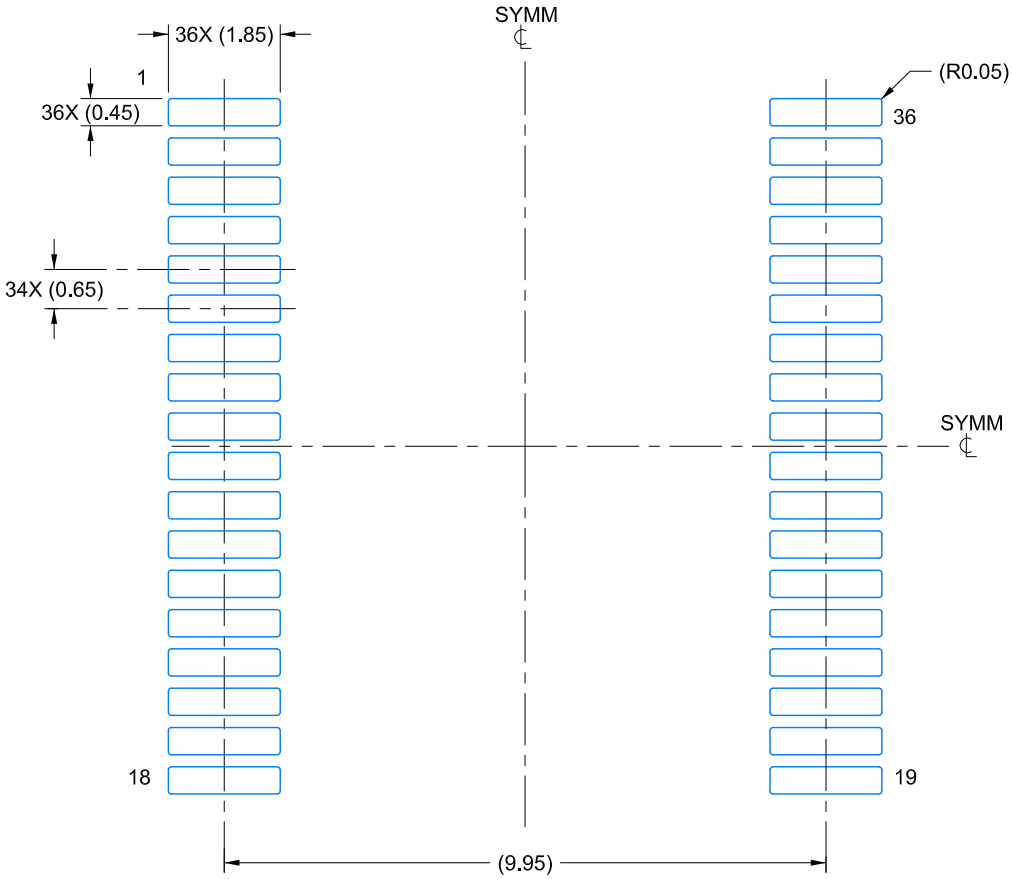
SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE

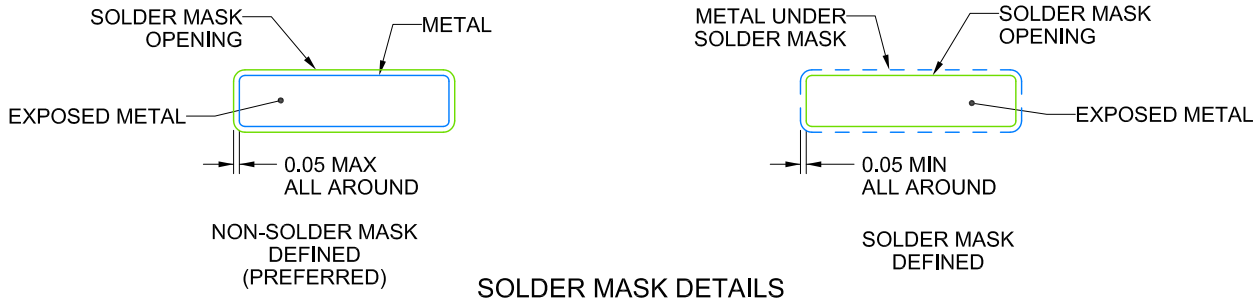


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

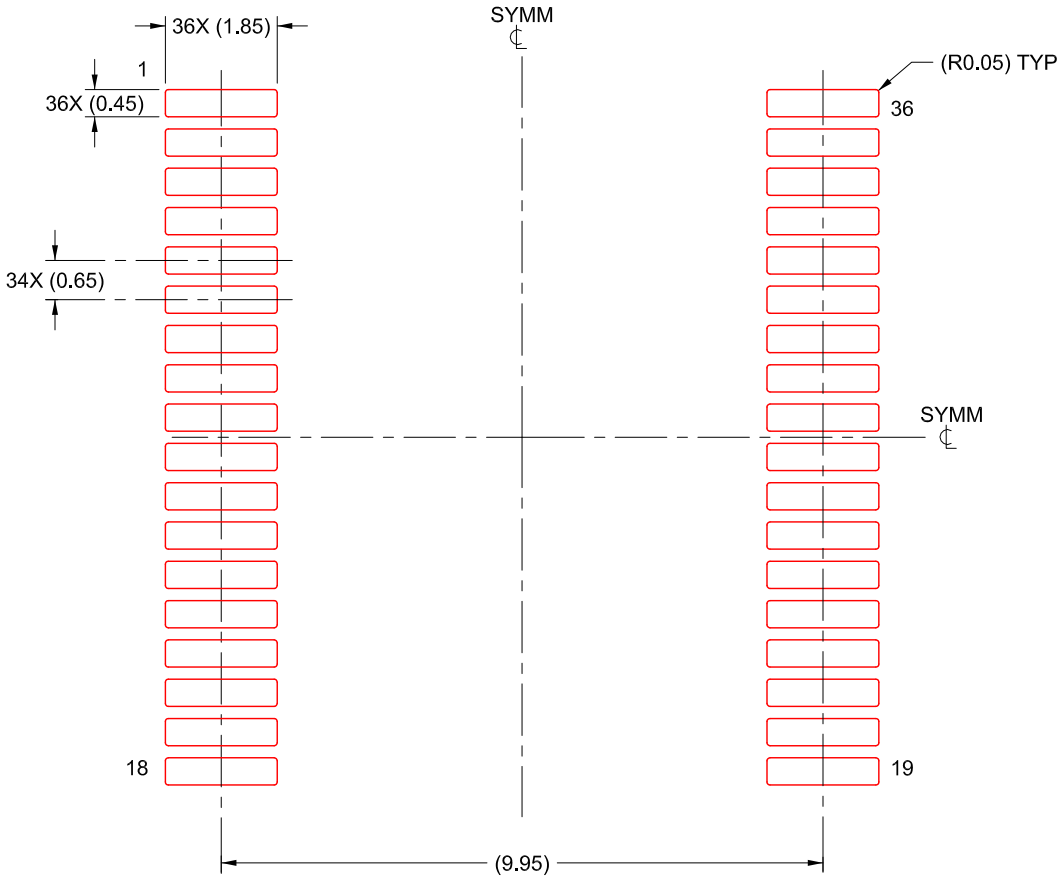


SOLDER MASK DETAILS

4224151/B 04/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4224151/B 04/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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