

UCC57102Z-Q1 高速ローサイド ゲート ドライバ、DESAT 保護付き、車載用アプリケーション向け

1 特長

- 車載アプリケーション認定済み
- AEC-Q100 認定済み
 - デバイス温度グレード 1
- 3A シンク、3A ソース出力電流 (標準値)
- プログラマブル遅延による DESAT 保護
- フォルト発生時のソフト ターンオフ
- VDD 電圧の絶対最大値: 30 V
- -5V まで耐える入力およびイネーブル ピン
- 厳格な UVLO スレッシュホルドによりバイアスの柔軟性を確保
- 伝搬遅延時間: 26ns (標準値)
- サーマル シャットダウン機能を搭載した自己保護ドライバ
- 広いバイアス電圧範囲
- 5mm × 4mm の SOIC-8 パッケージで供給されます
- 動作時の接合部温度範囲: -40°C ~ 150°C

2 アプリケーション

- HEV/EV PTC ヒーター
- トラクション インバータ
- 住宅用 EV チャージャ
- モータドライブ
- HVAC 用コンプレッサ

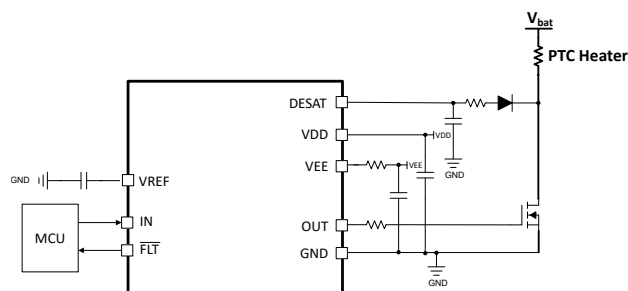
3 概要

UCC57102Z-Q1 は、PTC ヒーター、トラクション インバータのアクティブ放電回路、他の補助サブシステムなどの大電力車載アプリケーションに向けた、シングル チャネルの高性能ローサイド IGBT/SiC ゲートドライバです。このデバイスは、低電圧ロックアウト (UVLO)、脱飽和保護 (DESAT)、異常検出力、サーマルシャットダウン保護などの保護機能を搭載しています。UCC57102Z-Q1 の代表的なピークドライブ能力は 3A です。また、入力で -5V を扱えるため、中程度のグラウンド バウンスが発生するシステムの堅牢性を向上できます。これらの入力は電源電圧の影響を受けず、ほとんどのコントローラ出力に接続できるため、制御の柔軟性を最大限に高めることができます。UCC57102Z-Q1 で供給される広い電圧範囲のバイアス電源は、バイポーラ電圧に対応します。UCC57102Z-Q1 では、正確な 5V 出力 LDO も使用入手できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (公称)
UCC57102Z-Q1	D (SOIC 8)	4.9mm × 6.0mm	4.90mm × 3.91mm

- (1) 供給されているすべてのパッケージについては、[セクション 12](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略図



Table of Contents

1 特長	1	7 Applications and Implementation	19
2 アプリケーション	1	7.1 Application Information.....	19
3 概要	1	7.2 Typical Application.....	20
4 Pin Configuration and Functions	3	8 Power Supply Recommendations	22
5 Specifications	4	9 Layout	23
5.1 Absolute Maximum Ratings.....	4	9.1 Layout Guidelines.....	23
5.2 ESD Ratings.....	4	9.2 Layout Example.....	24
5.3 Recommended Operating Conditions.....	4	10 Device and Documentation Support	25
5.4 Thermal Information.....	4	10.1 サード・パーティ製品に関する免責事項.....	25
5.5 Electrical Characteristics.....	5	10.2 ドキュメントの更新通知を受け取る方法.....	25
5.6 Switching Characteristics.....	6	10.3 サポート・リソース.....	25
5.7 Timing Diagrams.....	7	10.4 Trademarks.....	25
5.8 Typical Characteristics.....	10	10.5 静電気放電に関する注意事項.....	25
6 Detailed Description	14	10.6 用語集.....	25
6.1 Overview.....	14	11 Revision History	25
6.2 Functional Block Diagram.....	14	12 Mechanical, Packaging, and Orderable Information	25
6.3 Feature Description.....	14		
6.4 Device Functional Modes.....	17		

4 Pin Configuration and Functions

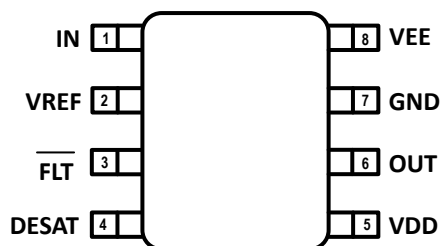


図 4-1. UCC57102Z-Q1 D Package SOIC-8 Top View

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN	1	I	Non-inverting PWM input
VREF	2	O	5V Reference generated within the driver
FLT	3	O	Active low fault reporting
DESAT	4	I	Input for detecting the desaturation fault
VDD	5	P	Driver bias supply
OUT	6	O	Output of the driver
GND	7	G	Driver ground
VEE	8	P	Driver negtive bias supply with respect to GND

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection

5 Specifications

5.1 Absolute Maximum Ratings

All the voltages are with respect to GND. Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDD-GND	Positive power supply	-0.3	30	V
VDD-VEE	Differential Power Supply	-0.3	30	V
VEE-GND	Negative Power Supply	-18	0.3	V
OUT	Output signal DC voltage	GND/VEE-0.3	VDD+0.3	V
	Output signal transient voltage for 200-ns	GND/VEE-2	VDD+3	V
V _{DESAT}	Desat voltage	-0.3	VDD+0.3	V
V _{IN}	IN signal DC voltage	-5	30	V
V _{EN}	EN signal DC voltage (W Version)	-5	30	V
I _{FLT}	FLT current sink		20	mA
V _{FLT}	External pull-up	-0.3	VDD+0.3	V
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

All voltages are with reference to GND. Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD-GND	Positive Power Supply	14.5		26	V
VDD-VEE	Differential Power Supply			26	V
VEE-GND	Negative Power Supply	-15		0	V
V _{OUT}	Output Voltage	GND/VEE		VDD	V
V _{IN}	IN signal DC voltage	-2		26	V
V _{EN}	EN signal DC voltage (W Version)	-2		26	V
T _J	Junction temperature	-40		150	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC57102Z-Q1	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	132.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	74.9	°C/W

5.4 Thermal Information (続き)

THERMAL METRIC ⁽¹⁾		UCC57102Z-Q1	UNIT
		D (SOIC)	
		8 PINS	
R _{θJB}	Junction-to-board thermal resistance	76.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	25.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

VDD = 15 V, VEE = 0 V, 1-μF capacitor from VDD to GND, 1-μF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I _{VDDQ}	VDD quiescent supply current	V _{IN} = 3.3V, EN = 5V, VDD = 6.5V			1.4	mA
I _{VDD}	VDD static supply current	V _{IN} = 3.3 V, EN = 5V		1.1	1.5	mA
I _{VDD}	VDD static supply current	V _{IN} = 0 V, EN = 5V		0.8	1.2	mA
I _{VEEQ}	VEE static supply current	V _{IN} = 0 V, EN = 5V, VEE = -10V			1.1	mA
I _{VDDO}	VDD dynamic operating current	f _{SW} = 1 MHz, EN = 5V, VDD=15 V, C _L =1.8nF			35	mA
I _{DIS}	VDD disable current	V _{IN} = 3.3 V, EN = 0 V		0.8	1.1	mA
VDD UNDERVOLTAGE THRESHOLDS AND DELAY						
t _{UVLO2FLT}	Propagation delay from UVLO shutdown to FLT			8.4		us
V _{VDD_ON}	VDD UVLO Rising Threshold	12.5-V UVLO Option	12.8	13.5	14.2	V
V _{VDD_OFF}	VDD UVLO Falling Threshold	12.5-V UVLO Option	11.8	12.5	13.2	V
V _{VDD_HYS}	VDD UVLO Threshold Hysteresis	12.5-V UVLO Option		1.0		V
VREF						
V _{REF}	Voltage Reference	I _{REF} =10mA		5		V
I _{REF}	Reference output current				20	mA
IN, EN						
V _{INH}	Input High Threshold Voltage		1.8	2.2	2.6	V
V _{INL}	Input Low Threshold Voltage		0.8	1.2	1.6	V
V _{IN_HYS}	Input-threshold Hysteresis			1.0		V
R _{IND}	IN Pin Pull Down Resistance	IN=EN= 3.3V		120		kΩ
V _{ENH}	Enable High Threshold Voltage		1.8	2.2	2.6	V
V _{ENL}	Enable Low Threshold Voltage		0.8	1.2	1.6	V
V _{EN_HYS}	Enable Threshold Hysteresis			1		V
R _{ENU}	EN Pin Pull Up Resistance	EN = 0V		400		kΩ
V _{FLTth}	FLT threshold voltage	I _{FLT-sink} = 15mA		0.43	1	V
DESAT DETECTION						
I _{CHG}	Blanking capacitor charge current	V _{DESAT} = 3.25V	200	250	316	μA
I _{DCHG}	DESAT pin discharge current	V _{DESAT} = 8V		-20		mA
V _{DESATTH}	DESAT Detection Threshold		6.0	6.5	7.0	V
V _{DESLO}	DESAT voltage when OUT=L, referenced to GND				100	mV

5.5 Electrical Characteristics (続き)

VDD = 15 V, VEE = 0 V, 1-μF capacitor from VDD to GND, 1-μF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{DESLEB} ⁽¹⁾	Leading edge blanking time			160		ns
t _{DESFIL} ⁽¹⁾	DESAT deglitch filter			100	150	ns
t _{DES2OUT} ⁽¹⁾	DESAT propagation delay to 90% of OUT	V _{DESAT} >V _{DESATTH}		140	250	ns
t _{MUTE} ⁽¹⁾	DESAT mute time	Output mute time after DESAT fault triggered	15	25	35	us
t _{DES2FLT} ⁽¹⁾	DESAT propagation delay to FLT low	V _{DESATTH} to 90% of FLT		135	250	ns
SOFT TURN OFF						
R _{STO}	Internal Soft turn-off Pulldown Resistance	DESAT triggered, V _{OUT} =5V		35		Ω
OVERTEMPERATURE PROTECTION						
T _{SD} ⁽¹⁾	Overtemperature threshold			180		°C
T _{HYS} ⁽¹⁾	Overtemperature protection hysteresis			30		°C
t _{OTP2FLT} ⁽¹⁾	Propagation delay from overtemperature shutdown to FLT	Over temperature shutdown to 90% of FLT		8		us
OUTPUT DRIVER STAGE						
I _{SRCPK} ⁽¹⁾	Peak Output Source Current	C _{VDD} = 10 μF, C _L = 0.1 μF, f = 1 kHz		-3		A
I _{SNKPK} ⁽¹⁾	Peak Output Sink Current	C _{VDD} = 10 μF, C _L = 0.1 μF, f = 1 kHz		3		A
R _{OH}	Pull up resistance	I _{OUT} = -500mA		5		Ω
R _{OL}	Pull down resistance	I _{OUT} = 500mA		1		Ω

(1) Parameters are not tested in production.

5.6 Switching Characteristics

VDD = 15 V, VEE = 0 V, 1-μF capacitor from VDD to GND, 1-μF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted. ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{RA} , t _{RB}	Output Rise Time	C _L =1.8nF, 10% to 90%, Vin = 0 to 3.3V	8	18	ns
t _{FA} , t _{FB}	Output Fall Time	C _L =1.8nF, 90% to 10%, Vin = 0 to 3.3V	14	32	ns
t _{D2}	Propagation Delay – Input falling to output falling	C _L =1.8nF, from 1V falling on Vin to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle	28	50	ns
t _{D1}	Propagation Delay – Input rising to output rising	C _L =1.8nF, from 2V rising on Vin to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle	26	50	ns
t _{PWmin}	Minimum Input Pulse Width That Passes to Output	C _L =1.8nF, Vin=0 - 3.3V, Fsw=500kHz, Vo > 2V	9	15	ns
t _{PWD}	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz t _{D2} – t _{D1} , C _L =1.8nF	-10	10	ns

(1) Switching parameters are not tested in production.

5.7 Timing Diagrams

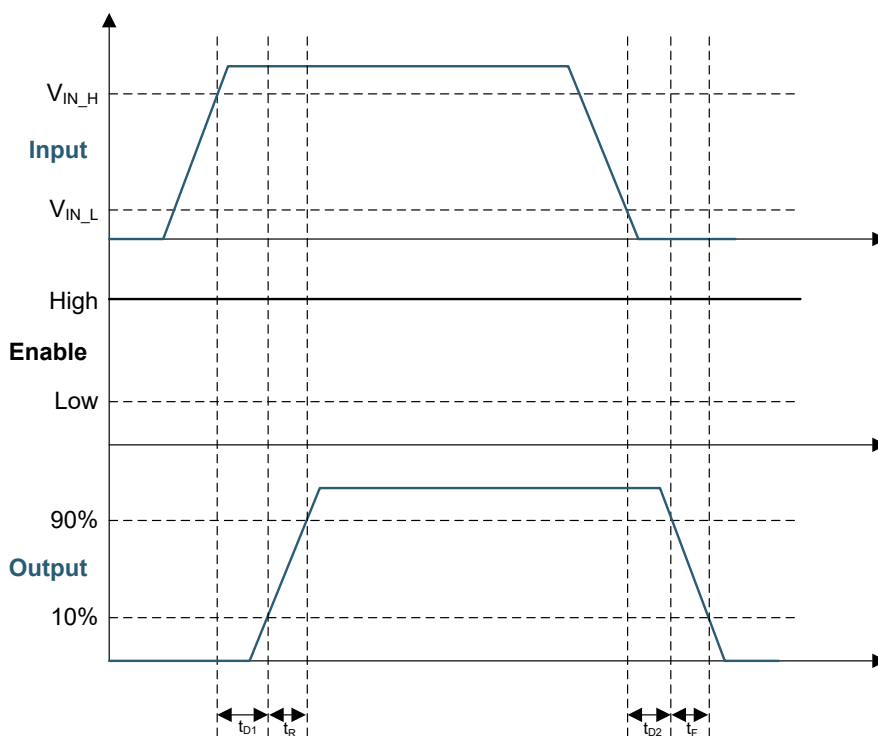


図 5-1. Single Input Version, IN = PWM

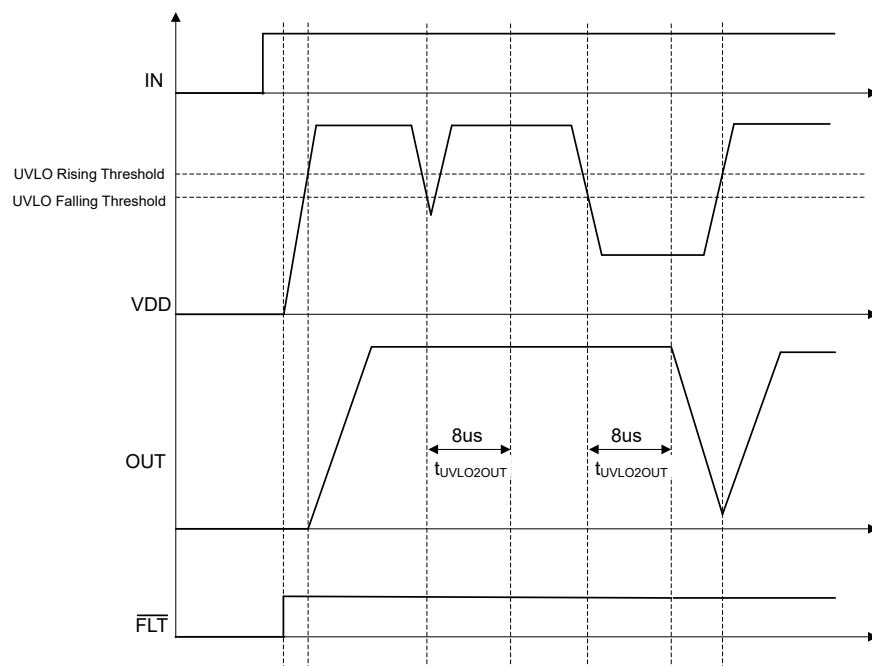


図 5-2. UVLO Protection Timing Diagram

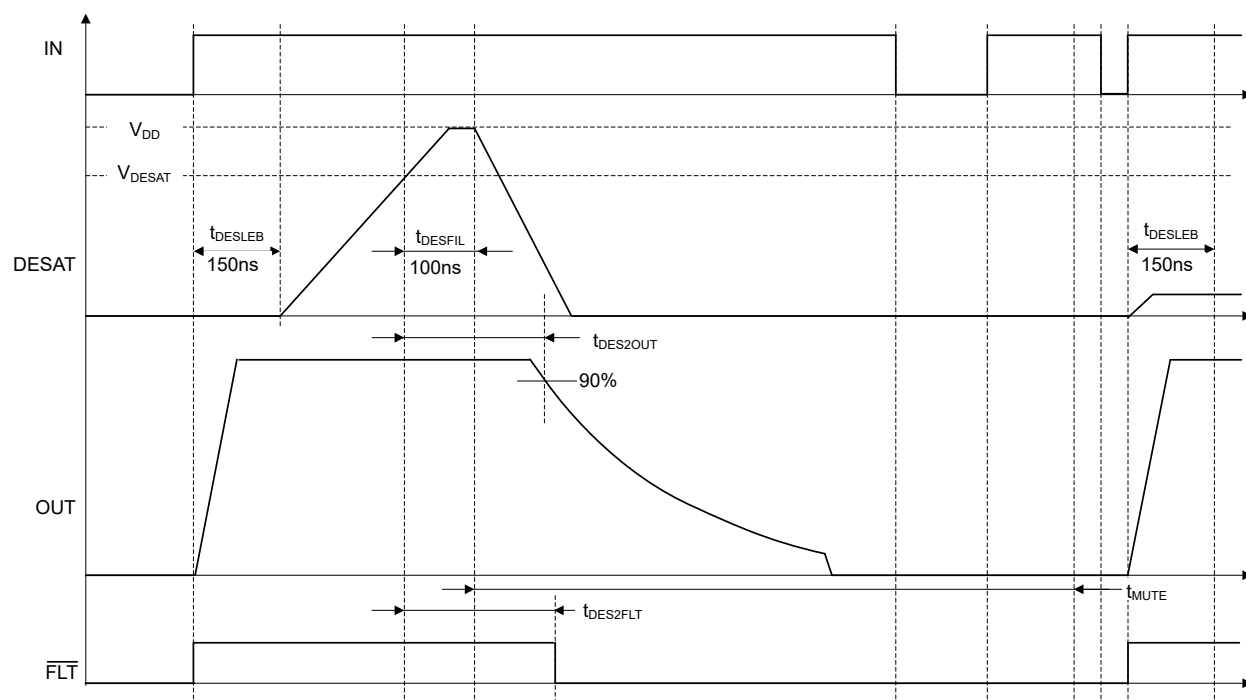


図 5-3. DESAT Protection Timing Diagram

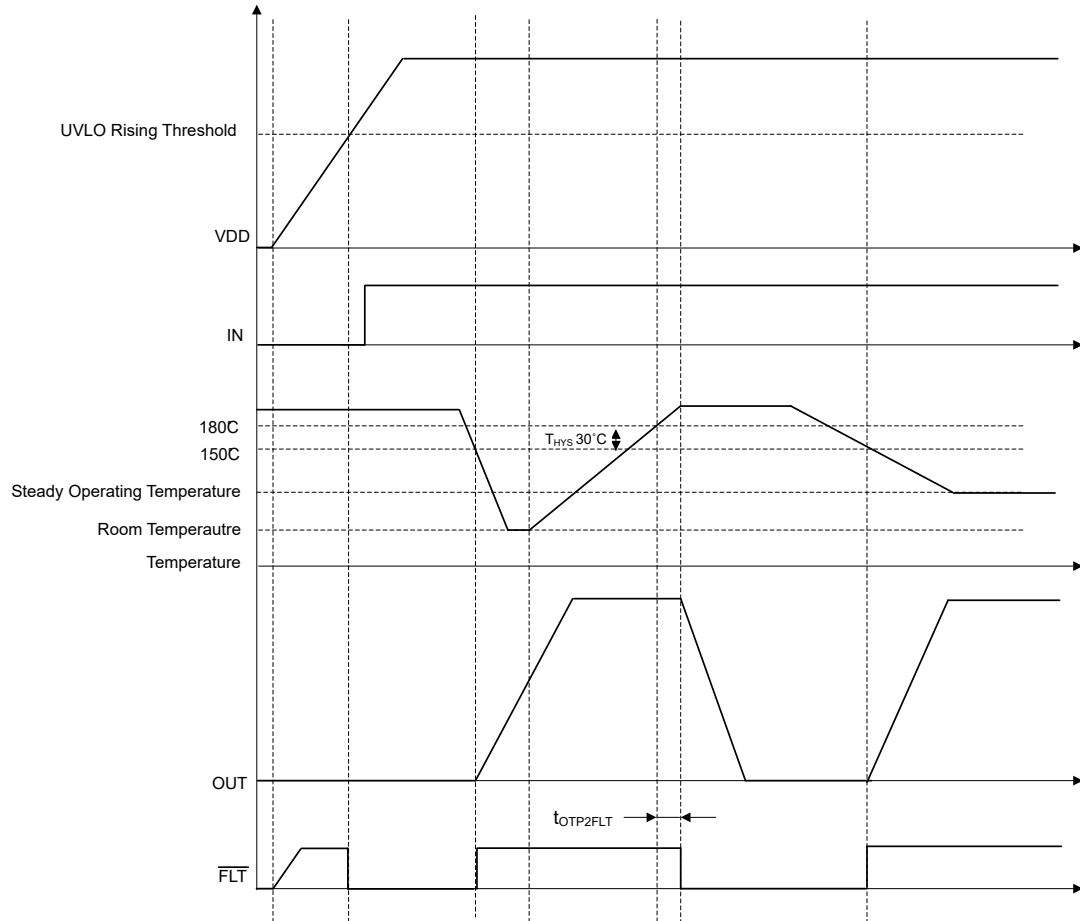


図 5-4. Thermal Shutdown Protection Timing Diagram

5.8 Typical Characteristics

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

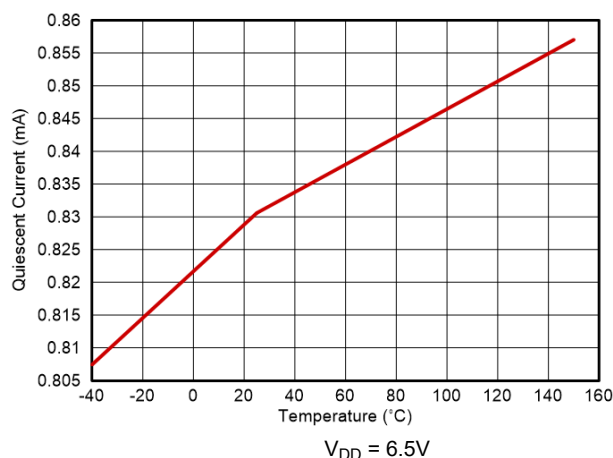


图 5-5. Quiescent Current

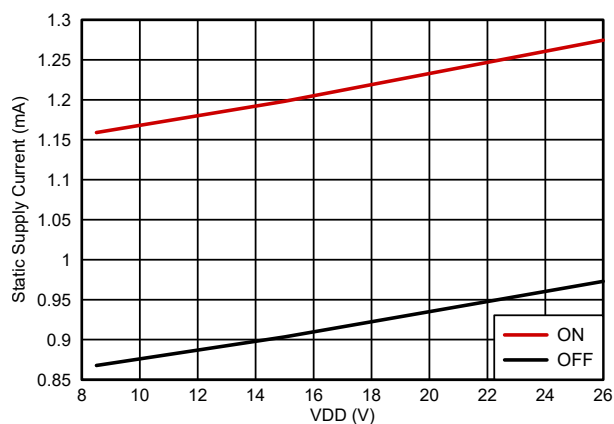


图 5-6. Operating Static Supply Current

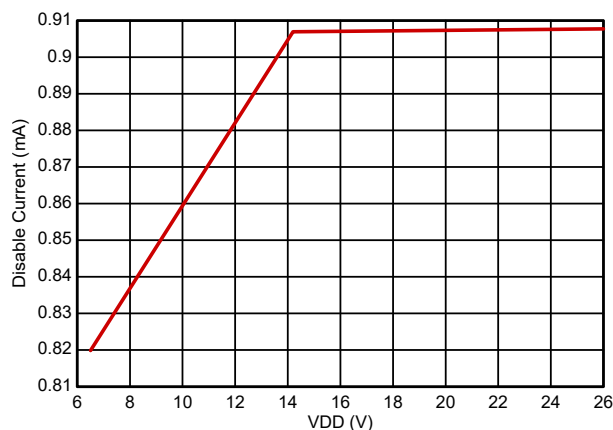


图 5-7. Disable Current

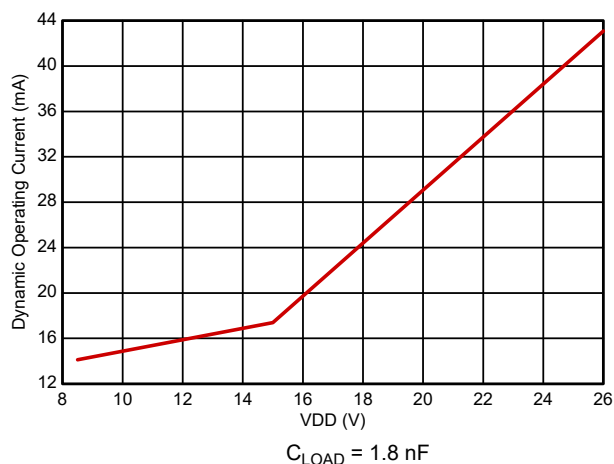


图 5-8. Operating Supply Current

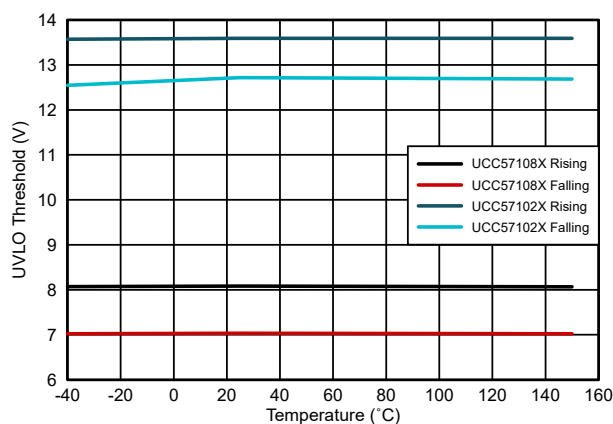


图 5-9. UVLO Threshold

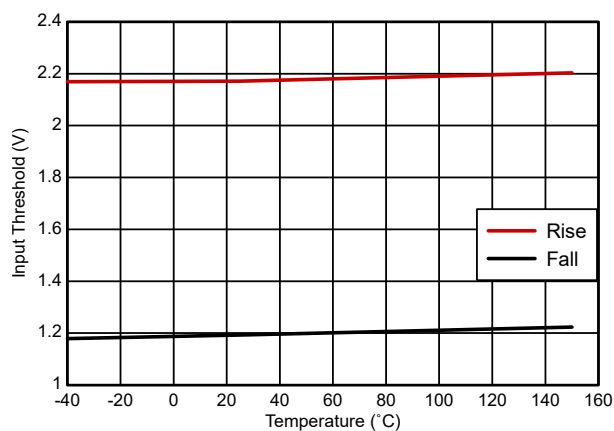


图 5-10. Input Threshold

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

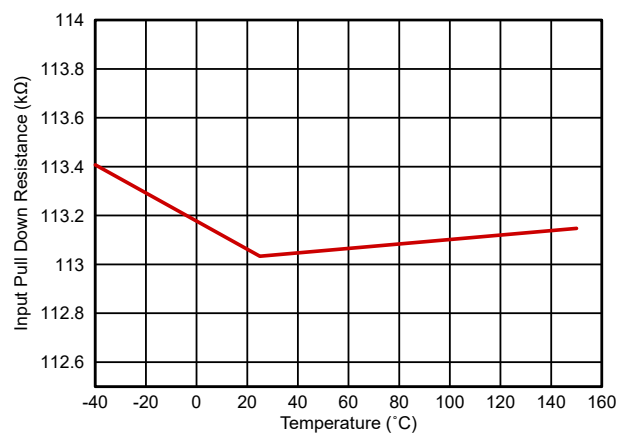


Figure 5-11. Input Pull down Resistance

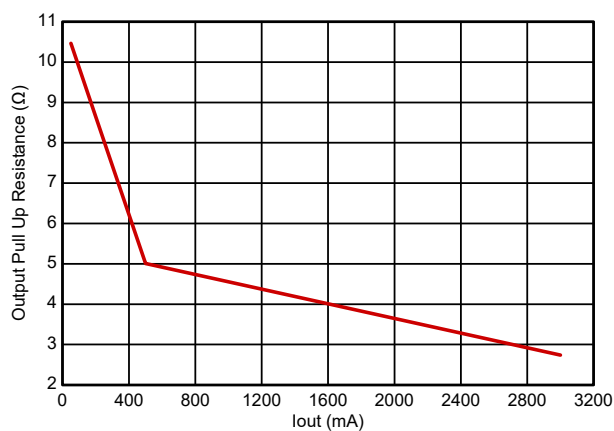


Figure 5-12. Output Pull up Resistance vs VDD

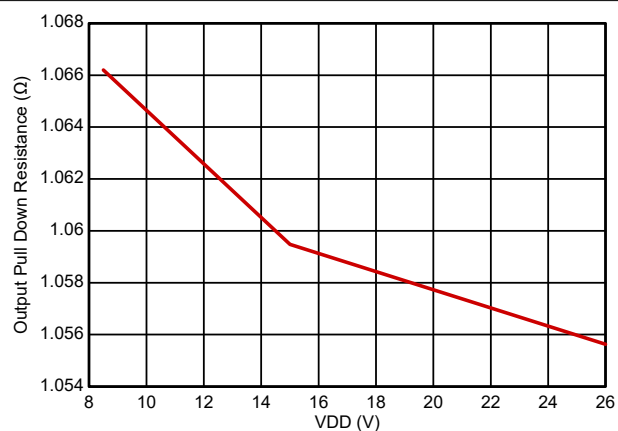


Figure 5-13. Output Pull down Resistance

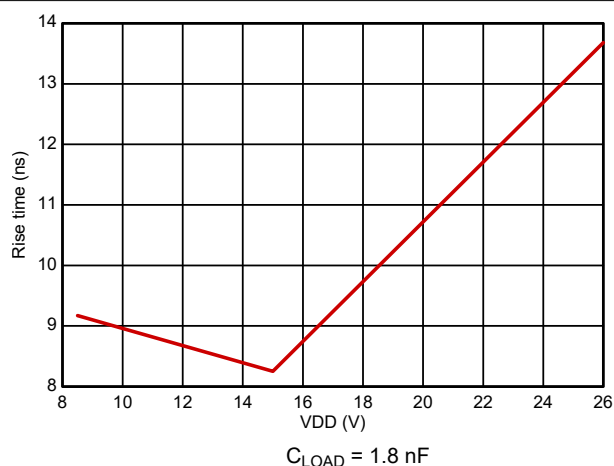


Figure 5-14. Output Rise Time

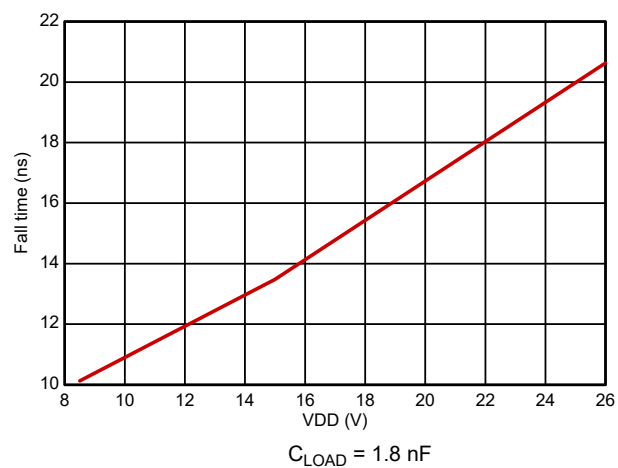


Figure 5-15. Output Fall Time

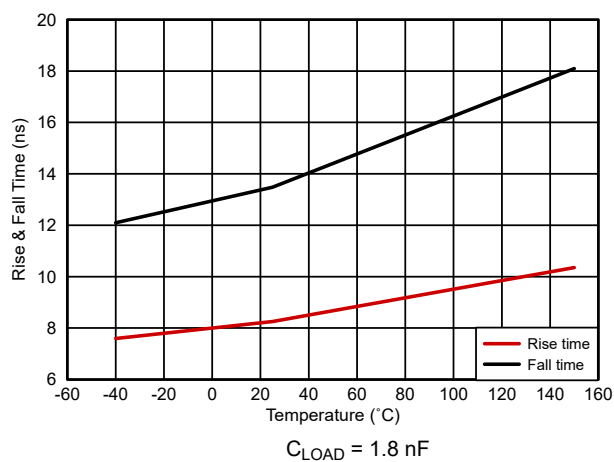


Figure 5-16. Output Rise and Fall Time

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

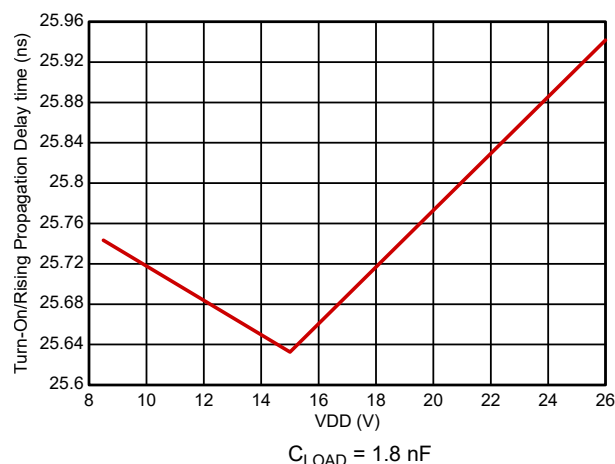


図 5-17. Input to Output Rising (Turnon) Propagation Delay

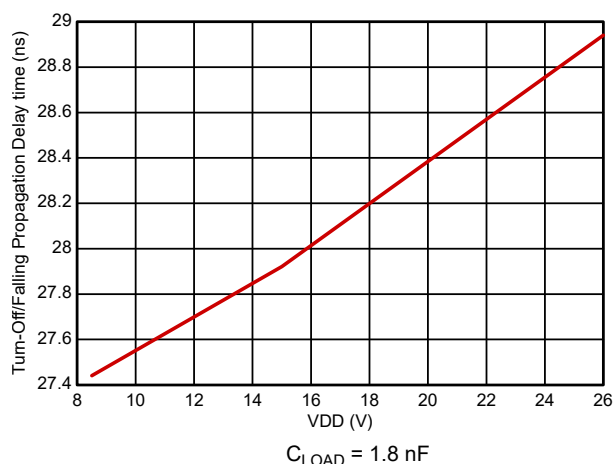


図 5-18. Input to Output Falling (Turnoff) Propagation Delay

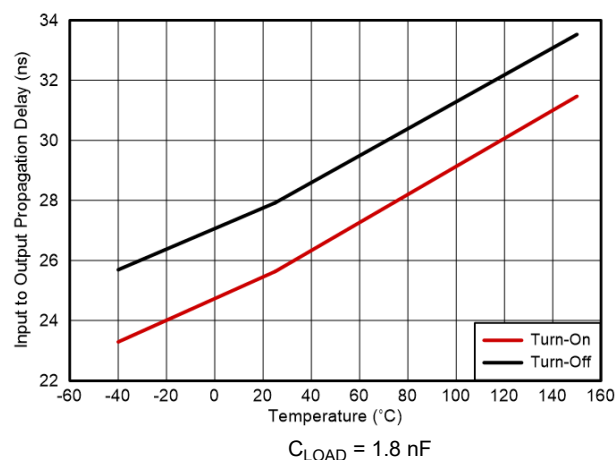


図 5-19. Input Propagation Delay

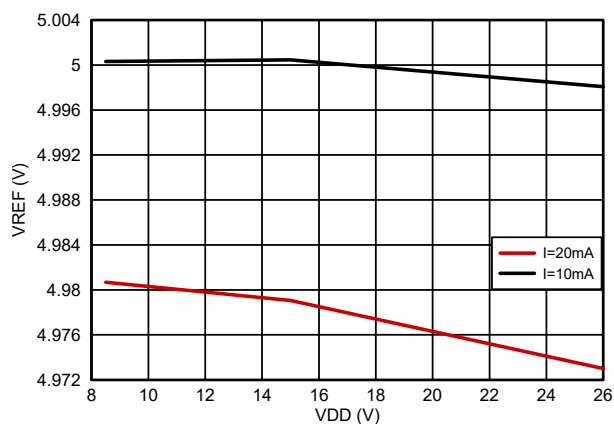


図 5-20. Vref Voltage vs VDD

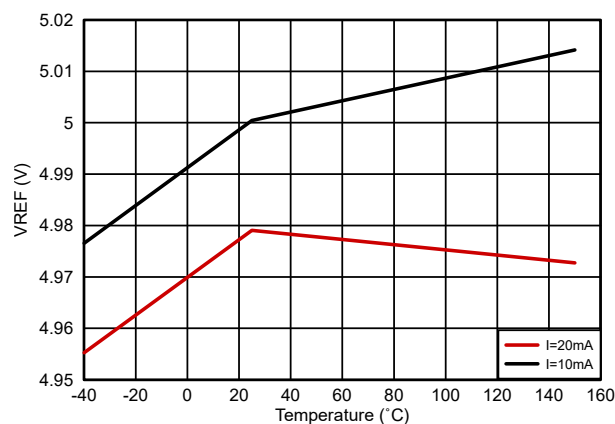


図 5-21. Vref Voltage vs Temperature

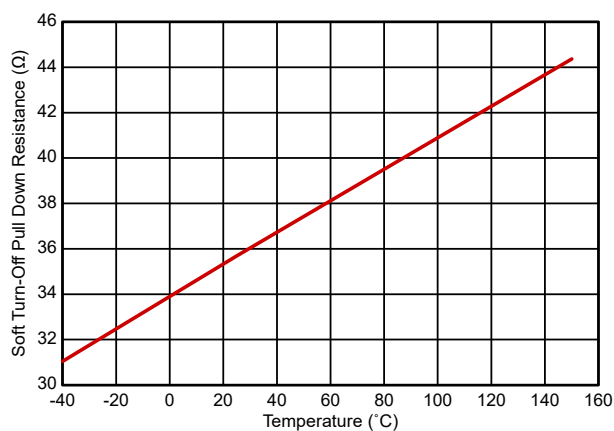


図 5-22. Soft Turn Off Pulldown Resistance vs VDD

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

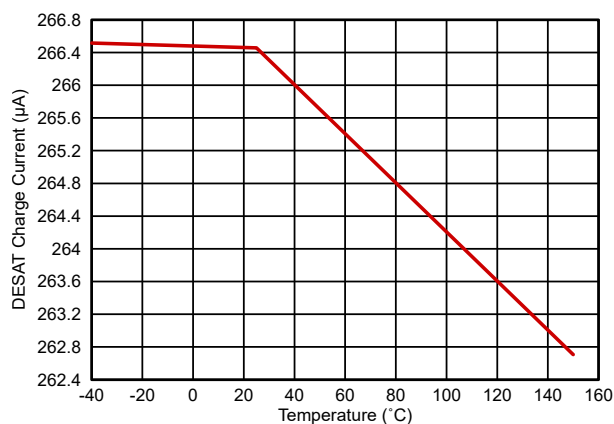


図 5-23. DESAT Charge Current vs Temperature

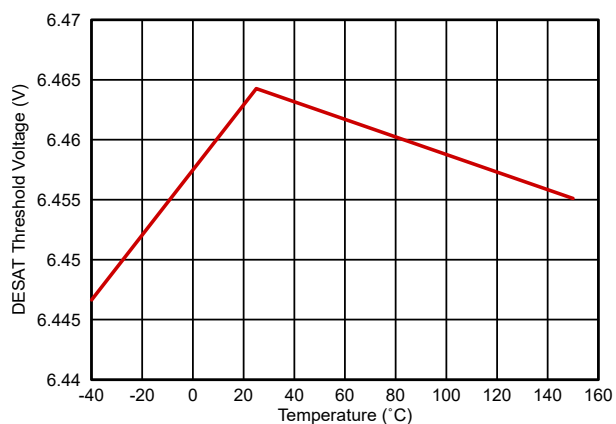


図 5-24. DESAT Threshold vs Temperature

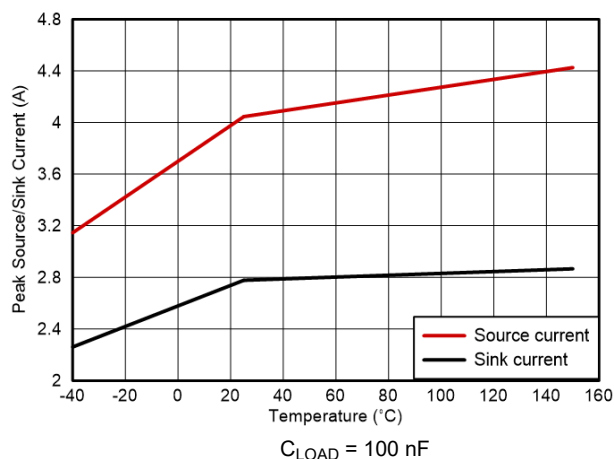


図 5-25. Peak Source and Sink Current

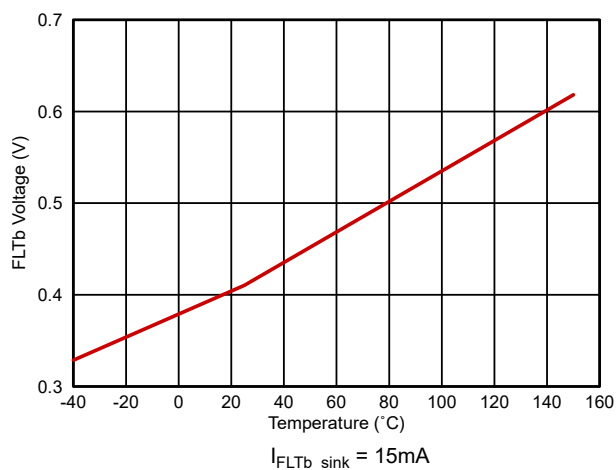


図 5-26. FLTB vs Temperature

6 Detailed Description

6.1 Overview

The UCC57102Z-Q1 device is a single-channel, high-speed, gate driver capable of effectively driving MOSFET, SiC MOSFET, and IGBT power switches with 3-A source and 3-A sink (symmetrical drive) peak current. The driver has a good transient handling capability on its output due to reverse currents, as well as rail-to-rail drive capability and small propagation delay, typically 26ns. The device has the state-of-art DESAT detection time and fault reporting function to the low voltage side DSP/MCU. Soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switch.

The input threshold of the UCC57102Z-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

In the UCC57102Z-Q1 the driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up. Pulling EN low disables the driver, while leaving EN open provides normal operation. The and UCC57102Z-Q1 offer an additional 5V output (VREF) that source up to 20mA function.

6.2 Functional Block Diagram

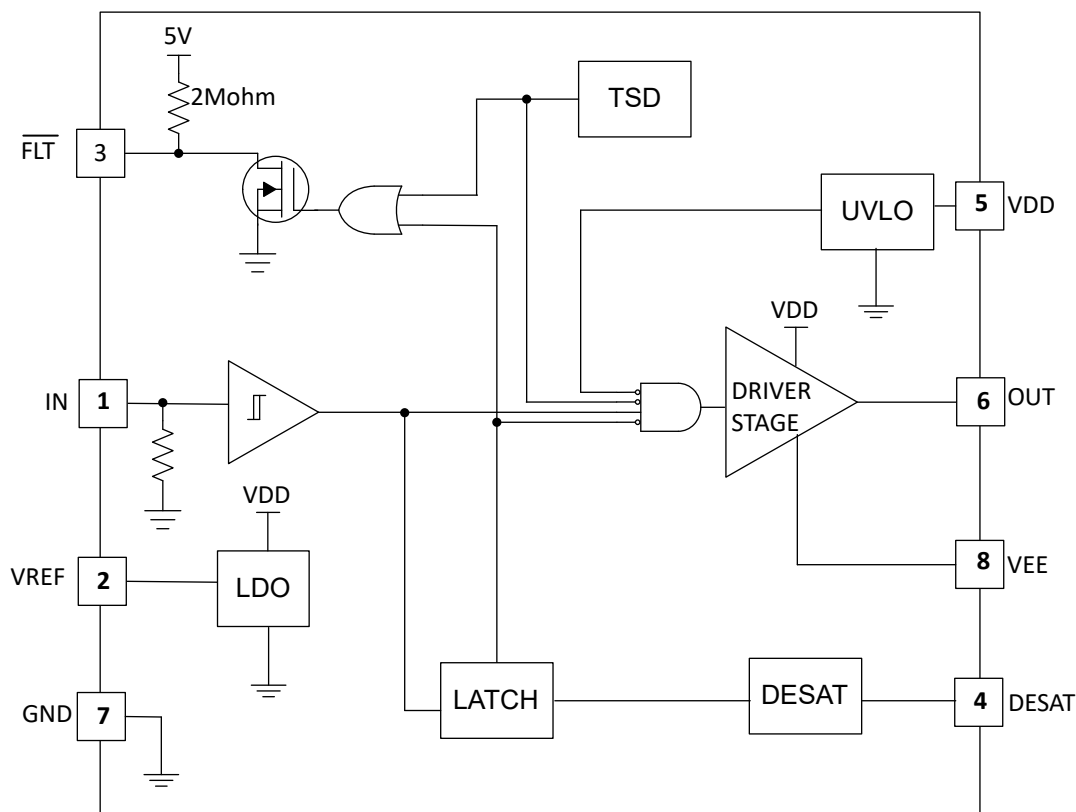


図 6-1. UCC57102Z-Q1 Simplified Functional Block Diagram

6.3 Feature Description

6.3.1 Input Stage

The inputs of the UCC57102Z-Q1 device are compatible with TTL based threshold logic and the inputs are independent of the VDD supply voltage. With typical high threshold of 2.2 V and typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the

input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically less than 8 pF, on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved with internal pullup or pulldown resistors on the input pins as shown in the simplified functional block diagrams. In some applications, due to difference in bias supply sequencing, different ICs power-up at different times. This may cause output of the controller to be in tri-state. This output of the controller is connected to the input of the driver IC. If the driver IC does not have a pulldown resistor then the output of the driver may go high erroneously and damage the switching power device.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located on a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between input pins and GND and trigger an unintended change of output state. Because of a fast 26-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the input and enable pins, caution must be used in the following applications:

- Input or enable pins are switched to amplitude > 15 V.
- Input or enable pins are switched at $dV/dt > 2$ V/ns.

If both of these conditions occur, add a series 150- Ω resistor for the pin(s) being switched to limit the current through the input structure.

6.3.2 Driver Stage

The device has a ± 3 -A peak drive strength and is suitable for driving IGBT/SiC. The driver features an important safety function wherein, when the input pins are in a floating condition, the output is held in the LOW state. The driver has rail-to-rail output by implementing an NMOS pull-up with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the following figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

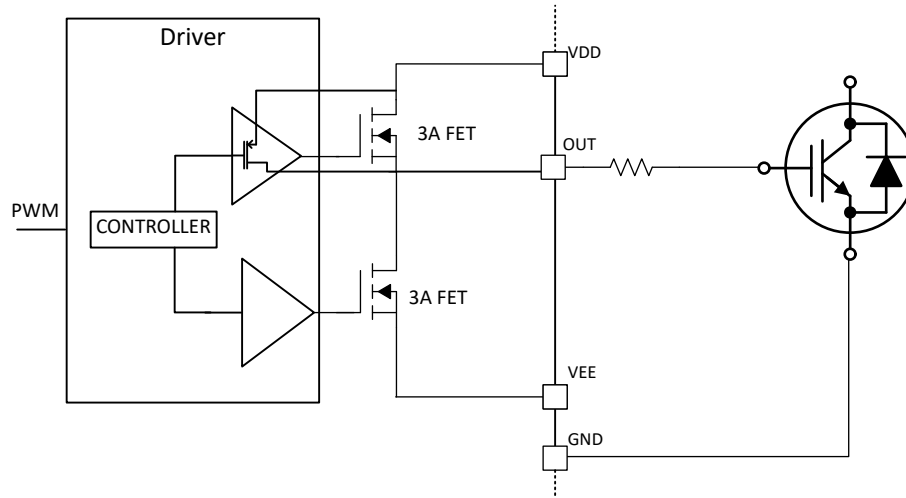


図 6-2. Gate Driver Output Stage

6.3.3 Desaturation (DESAT) Protection

The UCC57102Z-Q1 implements a fast overcurrent and short circuit protection feature to protect the MOSFET/IGBT from catastrophic breakdown during a fault. The DESAT pin has a typical 6.5 V threshold with respect to GND, the source or emitter of the power semiconductor. When the input is in a floating condition or the output is held in the LOW state, the DESAT pin is pulled down by an internal MOSFET and held in the LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in the ON state. The internal pulldown MOSFET helps to discharge the voltage of the DESAT pin when the power semiconductor is turned off. The device features a 150-ns internal leading edge blanking time after OUT switches to the HIGH state. Also, the OUT stay low for 25us T_{mute} time after the DESAT is triggered. The $\overline{\text{FLT}}$ will resume high at the first IN raising edge once the T_{mute} time expired. The UCC57102Z-Q1 internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 250 μA . More details about the DESAT circuit design can be found in [Applications and Benefits of UCC5710x-Q1](#).

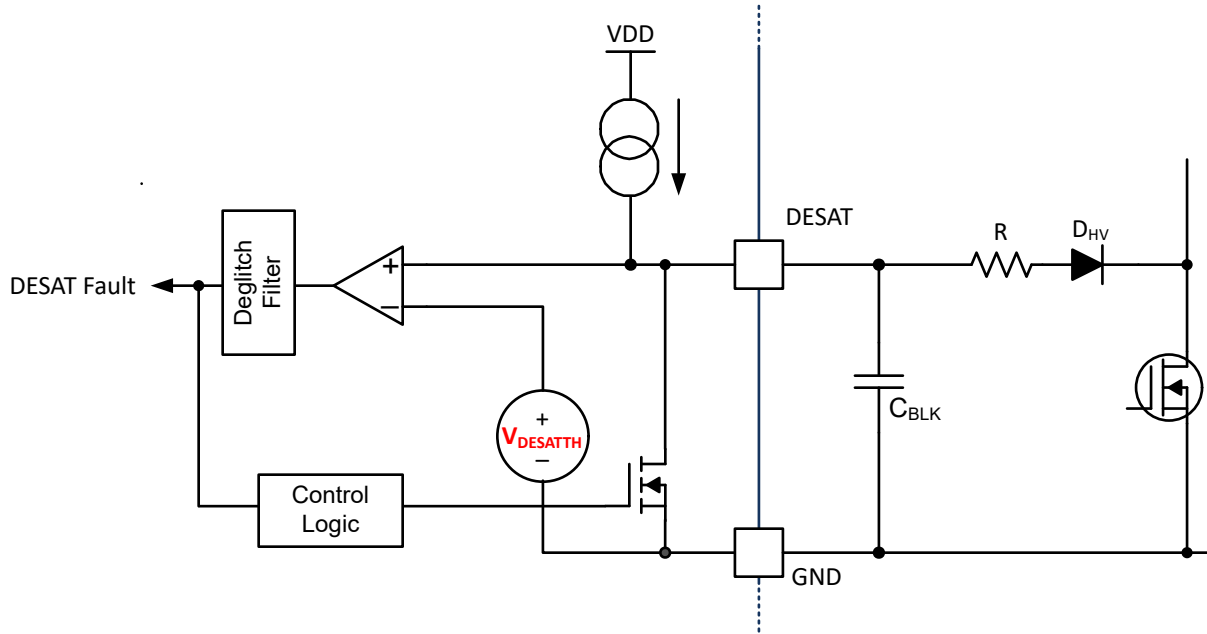


図 6-3. DESAT Protection

6.3.4 Fault (FLT)

The FLT pin of the UCC57102Z-Q1 can report a fault signal to the DSP/MCU when a fault is detected through the DESAT pin and internal TSD. The FLT pin is pulled down to GND after the fault is detected and is held low until the fault is cleared. It can be pull up to external voltage rail up to VDD level with the consideration that the maximum sink current on the FLT is 20mA. Also a 100pF capacitor between FLT and GND is recommended.

6.3.5 VREF

The UCC57102Z-Q1 device provides the 5V bias integrated in to the gate driver. This output is capable of sourcing up to 20mA. for voltage sensing modulators, current-sensing modulators or other external comparator interface. A 100nF bypass capacitor is required on the VREF pin even it is bias any external functions. The detail performance for VREF pin can be found in the [Typical Characteristics](#).

6.3.6 Thermal Shutdown

The UCC57102Z-Q1 device provides the thermal shutdown function that can protect the driver when the internal temperature goes above threshold. When the it excess the overtemperature threshold, the FLT will be pulled low after the 8us propagation delay. The device will active again once the temperature falls below the threshold. More information can be found in the [セクション 5.7](#)

6.4 Device Functional Modes

The UCC57102Z-Q1 device operates in normal mode and UVLO mode (see [セクション 7.2.2.1](#) for information on UVLO operation). In normal mode, the output state is dependent on the states of the device and the input pins.

The UCC57102Z-Q1 features a single, noninverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH enables the noninverting input to output on the IN pin.

表 6-1. UCC57102Z-Q1 Truth Table

IN	DESAT	INTERNAL TSD	FLT	OUT
H	L	L	Open drain	H
L	L	L	Open drain	L
H	H	L	L	L

表 6-1. UCC57102Z-Q1 Truth Table (続き)

IN	DESAT	INTERNAL TSD	FLT	OUT
X	X	H	L	L

7 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation is often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. Level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar (or P- N-channel MOSFET) transistors in a totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive, and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC57102Z-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range of UVLO to 26 V. This allows the driver to be used in 5-V bias logic level very high frequency MOSFET applications, 12-V MOSFET applications, 20-V and -5-V (relative to source) SiC FET applications, 15-V and -8-V (relative to emitter) IGBT applications and many others.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC57102Z-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

7.2 Typical Application

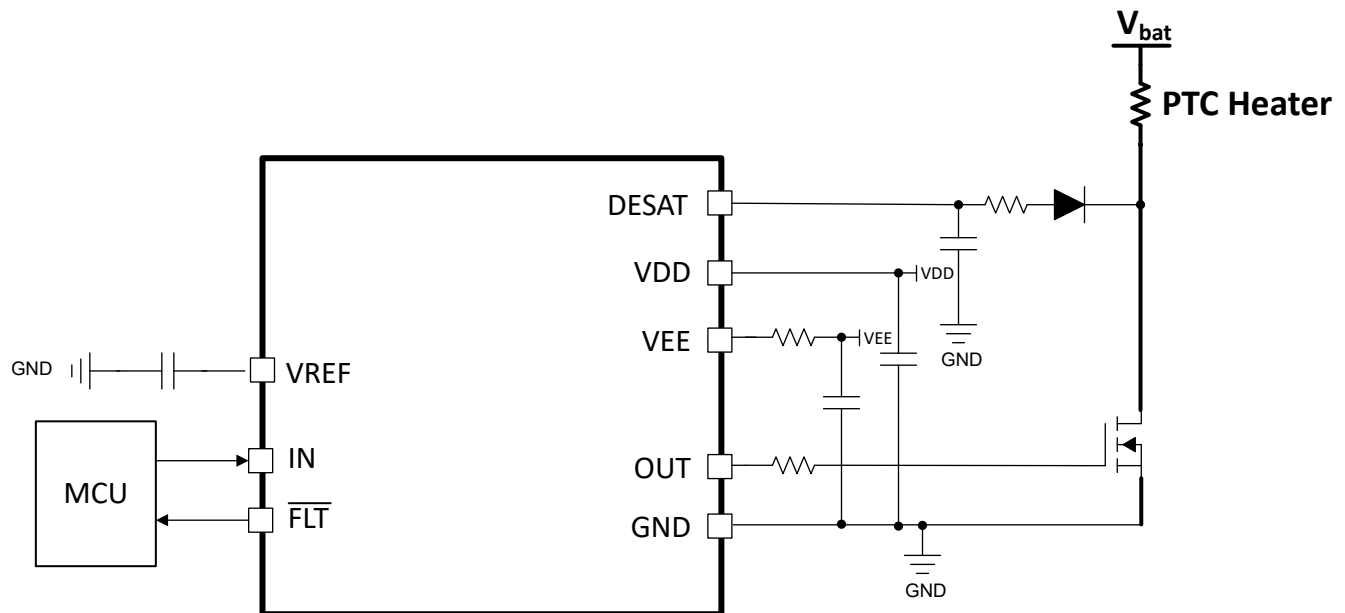


図 7-1. UCC57102Z-Q1 Used in a PTC Heater Application

7.2.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. Example design parameters and requirements are listed in 表 7-1.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input to output logic	Noninverting
Input threshold type	TTL
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dV_{DS}/dt (1)	100 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<1 W
Package type	SON-8 or SOIC-8

(1) dV_{DS}/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in .

7.2.2 Detailed Design Procedure

7.2.2.1 VDD Undervoltage Lockout

The UCC57102Z-Q1 device offers an undervoltage lockout threshold of 8 V and the UCC57102Z-Q1 provides an undervoltage lockout threshold of 12V. The device's hysteresis range helps to avoid any chattering due to the

presence of noise on the bias supply. 1V of typical UVLO hysteresis is expected. There is no significant driver output turnon delay due to the UVLO feature, and 4 μ s of UVLO delay is expected. The UVLO turn-off delay is also minimized as much as possible. The UVLO delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below UVLO thresholds, the outputs are held actively low irrespective of the state of the input pins and enable pin. The device accepts a wide range of slew rates on its VDD pin, and VDD noise within the hysteresis range does not affect the output state of the driver (neither ON nor OFF).

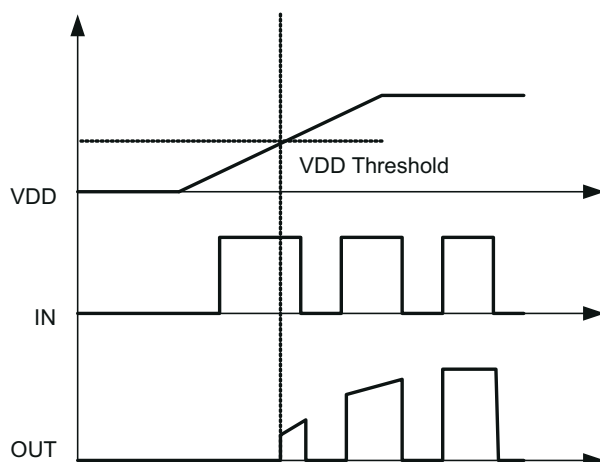


図 7-2. Power Up

7.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC57102Z-Q1 device with a 1nF capacitor load.

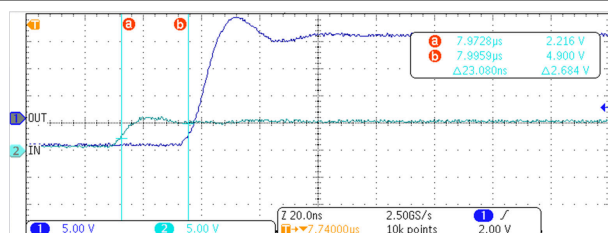


図 7-3. UCC57102Z-Q1 Rising (Turn-On) Propagation Delay

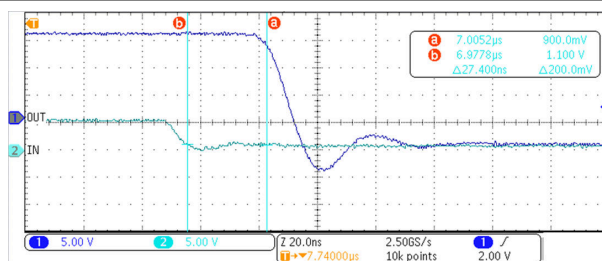


図 7-4. UCC57102Z-Q1 Falling (Turn-Off) Propagation Delay

8 Power Supply Recommendations

The bias supply voltage range for which the UCC57102Z-Q1 device is recommended to operate is from UVLO to 26 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 26-V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 30 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the UVLO range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, device operation continues until the VDD pin voltage has dropped below the VDD UVLO falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded the VDD UVLO rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of a few microfarads added in parallel.

The UCC57102Z-Q1 is a high current gate driver. If the gate driver is placed far from a switching power device such as a MOSFET then that may create a large inductive loop. A large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended ratings. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to high switching currents and board parasitic elements.

9 Layout

9.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC57102Z-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of a power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between the VDD pin and the GND pin and as close to the driver pins as possible to minimize the trace length for improved noise filtering. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of a few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of the power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch, and VDD bypass capacitor) should be minimized as much as possible in order to keep stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as the source of the power switch, the ground of the PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

9.2 Layout Example

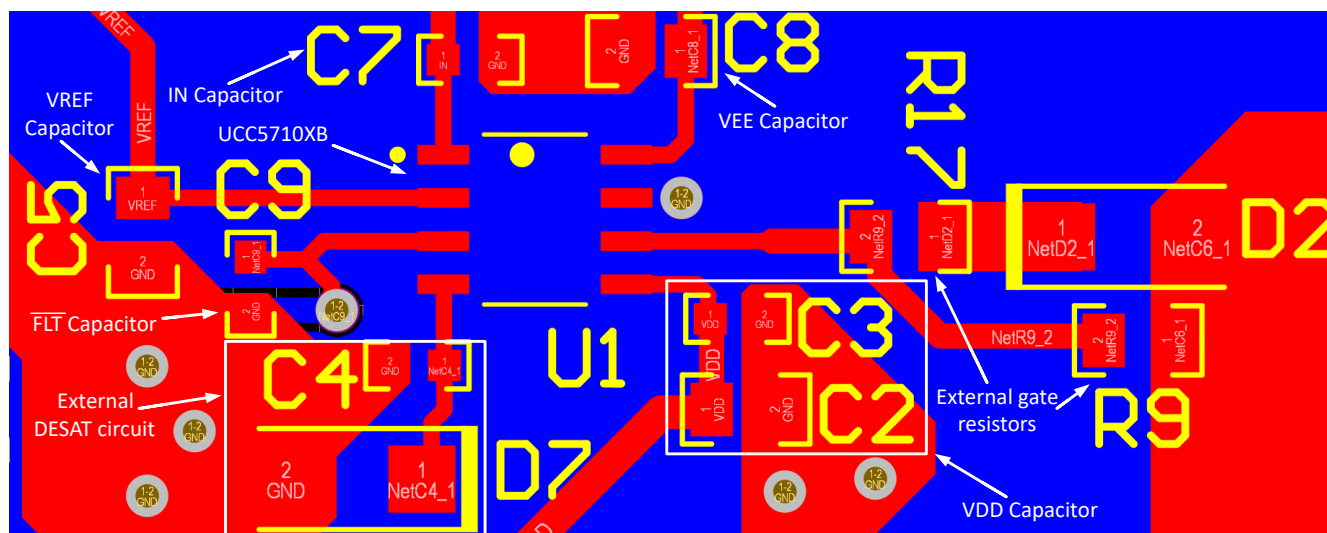


図 9-1. Layout Example: UCC57102Z

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC57102ZQDRQ1	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U102ZQ
UCC57102ZQDRQ1.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U102ZQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC57102Z-Q1 :

- Catalog : [UCC57102Z](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC57102ZQDRQ1	SOIC	D	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC57102ZQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月