UCC53x0 シングル チャネル絶縁ゲート ドライバ

1 特長

- 機能オプション
  - 分割出力 (UCC53x0S)
  - GND2 を基準とする UVLO (UCC53x0E)
  - ミラー クランプ オプション (UCC53x0M)
- 8 ピン D (沿面距離 4mm) および DWV (沿面距離 8.5mm) パッケージ
- 60ns(代表値)の伝搬遅延時間
- 最小 CMTI:100kV/ns
- 絶縁バリアの寿命:>40 年
- 入力電圧範囲:3V～15V
- 最大 33V のドライバ電源電圧
  - 8V および 12V UVLO オプション
- 負の 5V に対応可能な入力ピン
- 安全関連認証:
  - DIN V VDE V 0884-11:2017-01 と DIN EN 61010-1 に準拠した絶縁耐圧:7000V_{PK} (DWV、予定)、4242V_{PK} (D)
  - UL 1577 に準拠した絶縁耐圧定格 (1 分間): 5000V_{RMS} (DWV)、3000V_{RMS} (D)
  - GB4943.1-2011 準拠の CQC 認定: D および DWV (予定)
- CMOS 入力
- 動作温度:-40℃～+125℃

2 アプリケーション

- モータ ドライブ
- 高電圧の DC/DC コンバータ
- UPS および PSU
- HEV および EV 電源モジュール
- 太陽光インバータ

3 概要

UCC53x0 は、MOSFET、IGBT、SiC MOSFET、GaN FET (UCC5350SBD) を駆動するように設計されたシングル チャネル絶縁型ゲート ドライバのファミリです。UCC53x0S には分割出力があり、立ち上がりと立ち下がりの時間を別々に制御できます。UCC53x0M は、トランジスタのゲートを内部的なクランプへ接続することで、ミラー電流により誤って電源オンが発生することを防止します。UCC53x0E には、GND2 を基準とする UVLO2 があり、真の UVLO 読み取り値を得られます。

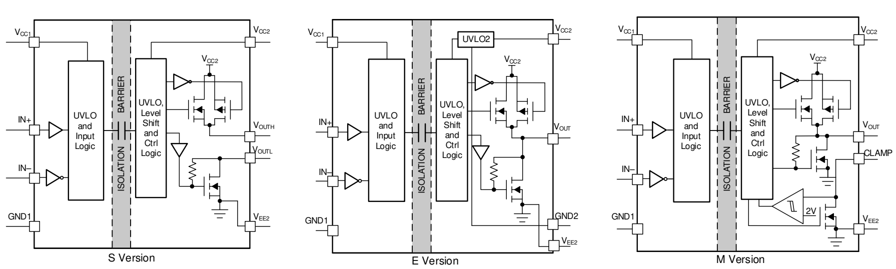
UCC53x0 は、4mm SOIC-8 (D) または 8.5mm SOIC-8 (DWV) パッケージで供給され、それぞれ最大 3kV_{RMS} および 5kV_{RMS} の絶縁電圧をサポートできます。これらの各種のオプションを取りそろえた UCC53x0 ファミリは、モータ ドライブや産業用電源に適しています。

フォトカプラと比較して、UCC53x0 ファミリは部品間スキューが小さく、伝搬遅延時間が短く、より高い温度でも動作し、CMTI が高いという特長があります。

製品情報

発注用製品型番 (1) (2)	最小のソースおよびシンク電流	説明
UCC5310MC	2.4A、1.1A	ミラー クランプ
UCC5320SC	2.4A、2.2A	分割出力
UCC5320EC	2.4A、2.2A	IGBT エミッタを基準とする UVLO
UCC5350MC	5A、5A	ミラー クランプ
UCC5350SB	5A、5A	8V UVLO 付きの分割出力
UCC5390SC	10A、10A	分割出力
UCC5390EC	10A、10A	IGBT エミッタを基準とする UVLO

(1) 供給されているすべてのパッケージについては、セクション 14 を参照してください。
(2) デバイスの詳細な比較については、セクション 4 を参照してください。



機能ブロック図 (S、E、M バージョン)

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4 Device Comparison Table

DEVICE OPTION[(1)]	PACKAGE	MINIMUM SOURCE CURRENT	MINIMUM SINK CURRENT	PIN CONFIGURATION	UVLO	ISOLATION RATING
UCC5310MC	D	2.4 A	1.1 A	Miller clamp	12 V	3-kV_{RMS}
	DWV					5-kV_{RMS}
UCC5320EC	D	2.4 A	2.2 A	UVLO with reference to GND2	12 V	3-kV_{RMS}
UCC5320SC	D	2.4 A	2.2 A	Split output	12 V	3-kV_{RMS}
	DWV					5-kV_{RMS}
UCC5350MC	D	5 A	5 A	Miller clamp	12 V	3-kV_{RMS}
	DWV					5-kV_{RMS}
UCC5350SB	D	5 A	5 A	Split Output	8 V	3-kV_{RMS}
UCC5390EC	D	10 A	10 A	UVLO with reference to GND2	12 V	3-kV_{RMS}
	DWV					5-kV_{RMS}
UCC5390SC	D	10 A	10 A	Split output	12 V	3-kV_{RMS}

(1) The S, E, and M suffixes are part of the orderable part number. See セクション 14 for the full orderable part number.

5 Pin Configuration and Function

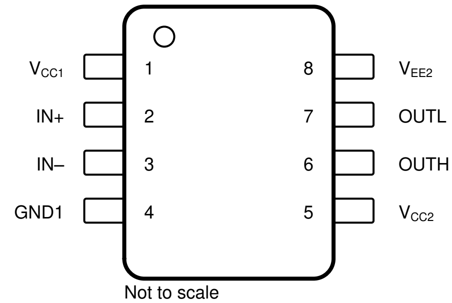


図 5-1. UCC5320S, UCC5350SB, and UCC5390S 8-Pin SOIC Top View

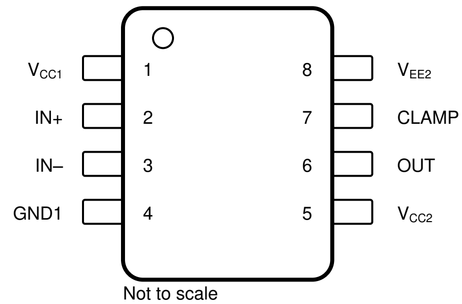


図 5-2. UCC5310M and UCC5350M 8-Pin SOIC Top View

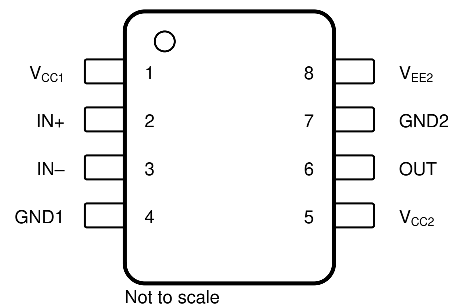


図 5-3. UCC5320E and UCC5390E 8-Pin SOIC Top View

表 5-1. Pin Functions

PIN				TYPE[(1)]	DESCRIPTION
NAME	NO.				
	UCC53x0S	UCC53x0M	UCC53x0E		
CLAMP	—	7	—	I	Active Miller-clamp input found on the UCC53x0M used to prevent false turnon of the power switches.
GND1	4	4	4	G	Input ground. All signals on the input side are referenced to this ground.
GND2	—	—	7	G	Gate-drive common pin. Connect this pin to the IGBT emitter. UVLO referenced to GND2 in the UCC53x0E.
IN+	2	2	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open. Use 表 8-4 to understand the input and output logic of these devices.
IN–	3	3	3	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open. Use 表 8-4 to understand the input and output logic of these devices.
OUT	—	6	6	O	Gate-drive output for UCC53x0E and UCC53x0M versions.

表 5-1. Pin Functions (続き)

PIN				TYPE[(1)]	DESCRIPTION
NAME	NO.				
	UCC53x0S	UCC53x0M	UCC53x0E		
OUTH	6	—	—	O	Gate-drive pull-up output found on the UCC53x0S.
OUTL	7	—	—	O	Gate-drive pull-down output found on the UCC53x0S.
V_{CC1}	1	1	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{CC2}	5	5	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V_{EE2}. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{EE2}	8	8	8	P	Negative output supply rail for E version, and GND for S and M versions. Connect a locally decoupled capacitor to GND2 for E version. Use a low-ESR or ESL capacitor located as close to the device as possible.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input bias pin supply voltage	V_{CC1} – GND1	GND1 – 0.3	18	V
Driver bias supply	V_{CC2} – V_{EE2}	–0.3	35	V
V_{EE2} bipolar supply voltage for E version	V_{EE2} – GND2	–17.5	0.3	V
Output signal voltage	V_{OUTH} – V_{EE2}, V_{OUTL} – V_{EE2}, V_{OUT} – V_{EE2}, V_{CLAMP} – V_{EE2}	V_{EE2} – 0.3	V_{CC2} + 0.3	V
Input signal voltage	V_{IN+} – GND1, $V_{IN–}$ – GND1	GND1 – 5	V_{CC1} + 0.3	V
Junction temperature, T_J [2]		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) To maintain the recommended operating conditions for T_J, see the Thermal Information table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, input side	3		15	V
V_{CC2}	Positive supply voltage output side (V_{CC2} – V_{EE2}), UCC53x0	13.2		33	V
V_{CC2}	Positive supply voltage output side (V_{CC2} – V_{EE2}), UCC5350SBD	9.5		33	V
V_{EE2}	Bipolar supply voltage for E version (V_{EE2} – GND2), UCC53x0	–16		0	V
V_{SUP2}	Total supply voltage output side (V_{CC2} – V_{EE2}), UCC53x0	13.2		33	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		UCC53x0 D (SOIC) 8 PINS	UCC53x0 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction–to-ambient thermal resistance	109.5	119.8	°C/W
$R_{\theta JC(top)}$	Junction–to-case (top) thermal resistance	43.1	64.1	°C/W
$R_{\theta JB}$	Junction–to-board thermal resistance	51.2	65.4	°C/W
Ψ_{JT}	Junction–to-top characterization parameter	18.3	37.6	°C/W
Ψ_{JB}	Junction–to-board characterization parameter	50.7	63.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D Package						
P_D	Maximum power dissipation on input and output	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 2.1-MHz, 50% duty cycle, square wave, 2.2-nF load			1.14	W
P_{D1}	Maximum input power dissipation				0.05	W
P_{D2}	Maximum output power dissipation				1.09	W
DWV Package						
P_D	Maximum power dissipation on input and output	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 1.9-MHz, 50% duty cycle, square wave, 2.2-nF load			1.04	W
P_{D1}	Maximum input power dissipation				0.05	W
P_{D2}	Maximum output power dissipation				0.99	W

6.6 Insulation Specifications for D Package

PARAMETER		TEST CONDITIONS	VALUE D	UNIT
CLR	External Clearance[1]	Shortest pin–to-pin distance through air	≥ 4	mm
CPG	External Creepage[1]	Shortest pin–to-pin distance across the package surface	≥ 4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 400	V
	Material Group	According to IEC 60664–1	II	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 150_{VRMS}	I-IV	
		Rated mains voltage ≤ 300_{VRMS}	I-III	
DIN V VDE 0884–11: 2017–01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990[6]	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	700[6]	V_{RMS}
		DC Voltage	990[6]	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50-µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	4242	V_{PK}
q_{pd}	Apparent charge[4]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output[5]	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.
(6) System isolation working voltages need to be verified according to application parameters.

6.7 Insulation Specifications for DWV Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DWV	
CLR	External Clearance[(1)]	Shortest pin–to-pin distance through air	≥ 8.5	mm
CPG	External Creepage[(1)]	Shortest pin–to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600_{VRMS}	I-III	
		Rated mains voltage ≤ 1000_{VRMS}	I-II	
DIN V VDE 0884–11: 2017–01[(2)]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC Voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) ; $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[(3)]	Test method per IEC 62368-1, 1.2/50-μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge [(4)]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[(5)]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output[(5)]	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^9$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.8 Safety-Related Certifications For D Package

VDE	UL	CQC
Certified according to DIN V VDE V 0884–11:2017–01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1–2011
Basic Insulation Maximum Transient Isolation Overvoltage, 4242 V_{PK}; Maximum Repetitive Peak Voltage, 990 V_{PK}; Maximum Surge Isolation Voltage, 4242 V_{PK}	Single protection, 3000 V_{RMS}	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 700 V_{RMS} Maximum Working Voltage
Certificate Number: 40047657	File Number: E181974	Certification number: CQC18001199354

6.9 Safety-Related Certifications For DWV Package

VDE	UL	CQC
Plan to certify according to DIN V VDE V 0884–11:2017–01 and DIN EN 61010-1	Recognized under UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1–2011
Reinforced Insulation Maximum Transient Isolation Overvoltage, 7000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121 V_{PK}; Maximum Surge Isolation Voltage, 8000 V_{PK}	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate
Certification number: 40047657	File Number: E181974	Certification planned

6.10 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
D PACKAGE							
I_S	Safety output supply current	$R_{\theta JA}$ = 109.5°C/W, V_{CC2} = 15 V, T_J = 150°C, T_A = 25°C, see 図 6-1	Output side			73	mA
		$R_{\theta JA}$ = 109.5°C/W, V_{CC2} = 30 V, T_J = 150°C, T_A = 25°C, see 図 6-1	Output side			36	
P_S	Safety output supply power	$R_{\theta JA}$ = 109.5°C/W, T_J = 150°C, T_A = 25°C, see 図 6-3	Input side			0.05	W
			Output side			1.09	
			Total			1.14	
T_S	Maximum safety temperature(1)					150	°C
DWV PACKAGE							
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 119.8°C/W, V_I = 15 V, T_J = 150°C, T_A = 25°C, see 図 6-2	Output side			66	mA
		$R_{\theta JA}$ = 119.8°C/W, V_I = 30 V, T_J = 150°C, T_A = 25°C, see 図 6-2	Output side			33	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 119.8°C/W, T_J = 150°C, T_A = 25°C, see 図 6-4	Input side			0.05	W
			Output side			0.99	
			Total			1.04	
T_S	Maximum safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.11 Electrical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-μF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-μF capacitor from V_{CC2} to V_{EE2}, C_L = 100-pF, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input supply quiescent current			1.67	2.4	mA
I_{VCC2}	Output supply quiescent current			1.1	1.8	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
$V_{IT+(UVLO1)}$	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
$V_{IT-(UVLO1)}$	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
$V_{hys(UVLO1)}$	VCC1 UVLO threshold hysteresis			0.1		V
UCC5310MC, UCC5320SC,UCC5320EC,UCC5390SC,UCC5390EC, and UCC5350MC UVLO THRESHOLDS (12-V UVLO Version)						
$V_{IT+(UVLO2)}$	VCC2 Positive-going UVLO threshold voltage			12	13	V
$V_{IT-(UVLO2)}$	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
$V_{hys(UVLO2)}$	VCC2 UVLO threshold voltage hysteresis			1		V
UCC5350SB UVLO THRESHOLD (8-V UVLO Version)						
$V_{IT+(UVLO2)}$	VCC2 Positive-going UVLO threshold voltage			8.7	9.4	V
$V_{IT-(UVLO2)}$	VCC2 Negative-going UVLO threshold voltage		7.3	8.0		V
$V_{hys(UVLO2)}$	VCC2 UVLO threshold voltage hysteresis			0.7		V
LOGIC I/O						
$V_{IT+(IN)}$	Positive-going input threshold voltage (IN+, IN–)			0.55 × V_{CC1}	0.7 × V_{CC1}	V
$V_{IT-(IN)}$	Negative-going input threshold voltage (IN+, IN–)		0.3 × V_{CC1}	0.45 × V_{CC1}		V
$V_{hys(IN)}$	Input hysteresis voltage (IN+, IN–)			0.1 × V_{CC1}		V
I_{IH}	High-level input leakage at IN+	IN+ = V_{CC1}		40	240	μA
I_{IL}	Low-level input leakage at IN–	IN– = GND1	–240	–40		μA
		IN– = GND1 – 5 V	–310	–80		
GATE DRIVER STAGE						
V_{OH}	High-level output voltage (VCC2 - OUT) and (VCC2 - OUTH)	I_{OUT} = –20 mA	100	240		mV
V_{OL}	Low level output voltage (OUT and OUTL)	UCC5320SC and UCC5320EC, IN+ = low, IN– = high; I_O = 20 mA	9.4	13		mV
		UCC5310MC, IN+ = low, IN– = high; I_O = 20 mA	17	26		
		UCC5390SC and UCC5390EC, IN+ = low, IN– = high; I_O = 20 mA	2	3		
		UCC5350MC and UCC5350SB, IN+ = low, IN– = high; I_O = 20 mA	5	7		

6.11 Electrical Characteristics (続き)

V_{CC1} = 3.3 V or 5 V, 0.1-μF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-μF capacitor from V_{CC2} to V_{EE2}, C_L = 100-pF, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Peak source current	UCC5320SC and UCC5320EC, IN+ = high, IN– = low	2.4	4.3		A
		UCC5310MC, IN+ = high, IN– = low	2.4	4.3		
		UCC5390SC and UCC5390EC, IN+ = high, IN– = low	10	17		
		UCC5350MC, IN+ = high, IN– = low	5	10		
		UCC5350SB IN+ = high, IN– = low	5	8.5		
I_{OL}	Peak sink current	UCC5320SC and UCC5320EC, IN+ = low, IN– = high	2.2	4.4		A
		UCC5310MC, IN+ = low, IN– = high	1.1	2.2		
		UCC5390SC and UCC5390EC, IN+ = low, IN– = high	10	17		
		UCC5350MC, IN+ = low, IN– = high	5	10		
		UCC5350SB IN+ = low, IN– = high	5	10		
ACTIVE MILLER CLAMP (UCC53xxM only)						
V_{CLAMP}	Low-level clamp voltage	UCC5310MC, I_{CLAMP} = 20 mA		26	50	mV
		UCC5350MC, I_{CLAMP} = 20 mA		7	10	
I_{CLAMP}	Clamp low-level current	UCC5310MC, V_{CLAMP} = V_{EE2} + 15 V	1.1	2.2		A
		UCC5350MC, V_{CLAMP} = V_{EE2} + 15 V	5	10		
$I_{CLAMP(L)}$	Clamp low-level current for low output voltage	UCC5310MC, V_{CLAMP} = V_{EE2} + 2 V	0.7	1.5		A
		UCC5350MC, V_{CLAMP} = V_{EE2} + 2 V	5	10		
$V_{CLAMP-TH}$	Clamp threshold voltage	UCC5310MC and UCC5350MC		2.1	2.3	V
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping voltage ($V_{OUTH} – V_{CC2}$ or $V_{OUT} – V_{CC2}$)	IN+ = high, IN– = low, t_{CLAMP} = 10 μs, I_{OUTH} or I_{OUT}= 500 mA		1	1.3	V
$V_{CLP-OUT}$	Clamping voltage ($V_{EE2} – V_{OUTL}$ or $V_{EE2} – V_{CLAMP}$ or $V_{EE2} – V_{OUT}$)	IN+ = low, IN– = high, t_{CLAMP} = 10 μs, I_{CLAMP} or I_{OUTL} = –500 mA		1.5		V
		IN+ = low, IN– = high, I_{CLAMP} or I_{OUTL} = –20 mA		0.9	1	
ACTIVE PULLDOWN						
V_{OUTSD}	Active pulldown voltage on OUTL, CLAMP, OUT	I_{OUTL} or I_{OUT} = 0.1 × $I_{OUTL(typ)}$, V_{CC2} = open		1.8	2.5	V

6.12 Switching Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output-signal rise time	UCC5320SC, UCC5320EC, and UCC5310MC, C_{LOAD} = 1 nF		12	28	ns
		UCC5390SC, UCC5350SB, UCC5390EC, and UCC5350MC, C_{LOAD} = 1 nF		10	26	ns
t_f	Output-signal fall time	UCC5320SC and UCC5320EC, C_{LOAD} = 1 nF		10	25	ns
		UCC5310MC, C_{LOAD} = 1 nF		10	26	ns
		UCC5390SC, UCC5350SB, UCC5390EC, and UCC5350MC, C_{LOAD} = 1 nF		10	22	ns
t_{PLH}	Propagation delay (default versions), high	UCC5320SC and UCC5320EC, C_{LOAD} = 100 pF		60	72	ns
		UCC5310MC, C_{LOAD} = 100 pF		60	75	ns
		UCC5390SC, UCC5350SB, UCC5390EC, and UCC5350MC, C_{LOAD} = 100 pF		65	100	ns
t_{PHL}	Propagation delay (default versions), low	UCC5320CS and UCC5320EC, C_{LOAD} = 100 pF		60	75	ns
		UCC5310MC, C_{LOAD} = 100 pF		60	75	ns
		UCC5390SC, UCC5350SB, UCC5390EC, and UCC5350MC, C_{LOAD} = 100 pF		65	100	ns
t_{UVLO1_rec}	UVLO recovery delay of V_{CC1}	See 図 8-9		30		µs
t_{UVLO2_rec}	UVLO recovery delay of V_{CC2}	See 図 8-9		50		µs
t_{PWD}	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	UCC5320SC and UCC5320EC, C_{LOAD} = 100 pF		1	20	ns
		UCC5310MC, C_{LOAD} = 100 pF		1	20	ns
		UCC5390SC, UCC5350SB, and UCC5390EC, C_{LOAD} = 100 pF		1	20	ns
		UCC5350MC, C_{LOAD} = 100 pF		1	20	ns
$t_{sk(pp)}$	Part-to-part skew(1)	UCC5320SC and UCC5320EC, C_{LOAD} = 100 pF		1	25	ns
		UCC5310MC, C_{LOAD} = 100 pF		1	25	ns
		UCC5390SC, UCC5350SB, and UCC5390EC, C_{LOAD} = 100 pF		1	25	ns
		UCC5350MC, C_{LOAD} = 100 pF		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or V_{CC1}, V_{CM} = 1200 V	100	120		kV/µs

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

6.13 Insulation Characteristics Curves

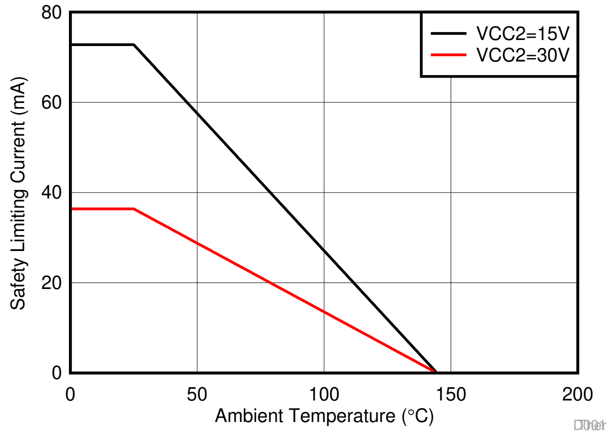


図 6-1. Thermal Derating Curve for Limiting Current per VDE for D Package

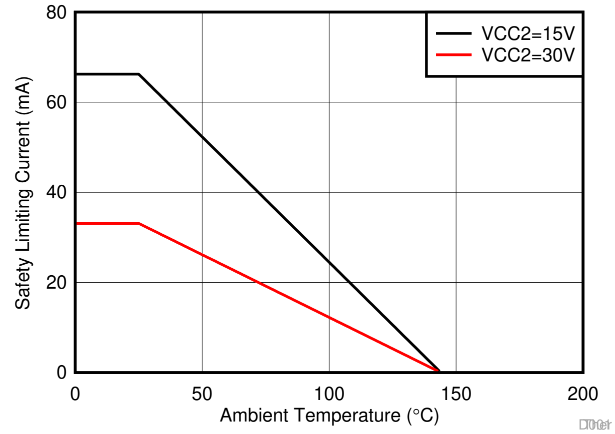


図 6-2. Thermal Derating Curve for Limiting Current per VDE for DWV Package

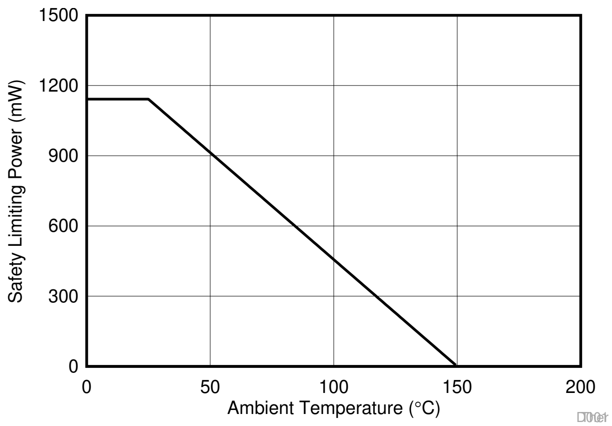


図 6-3. Thermal Derating Curve for Limiting Power per VDE for D Package

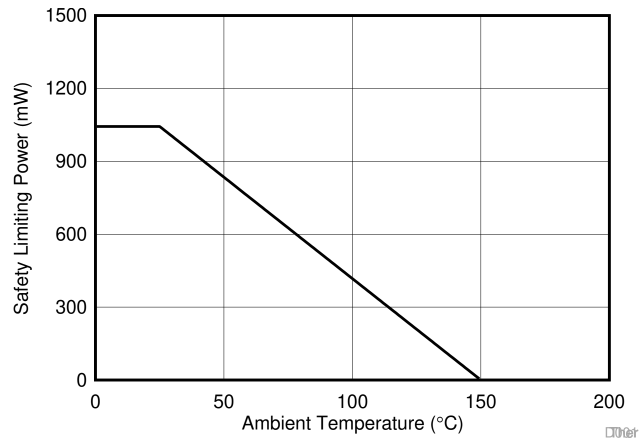
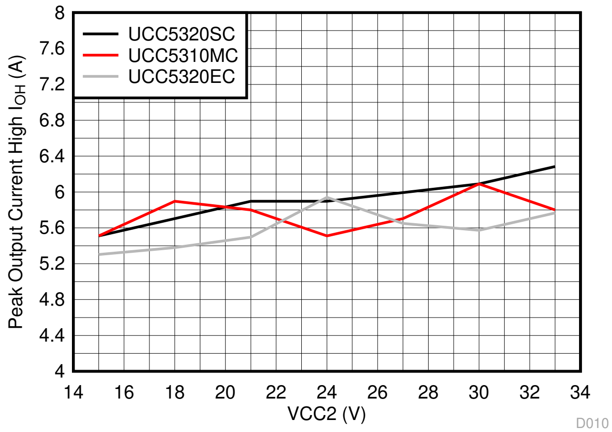


図 6-4. Thermal Derating Curve for Limiting Power per VDE for DWV Package

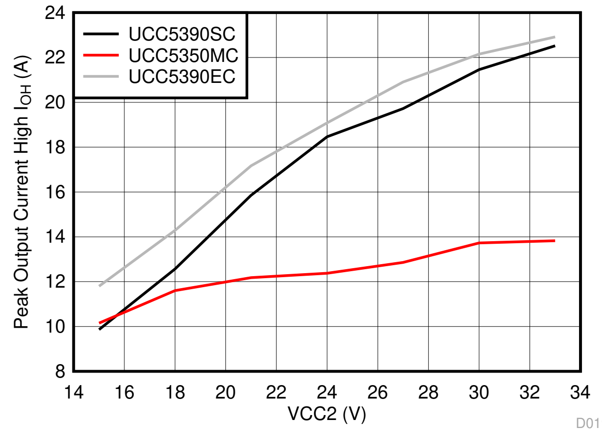
6.14 Typical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



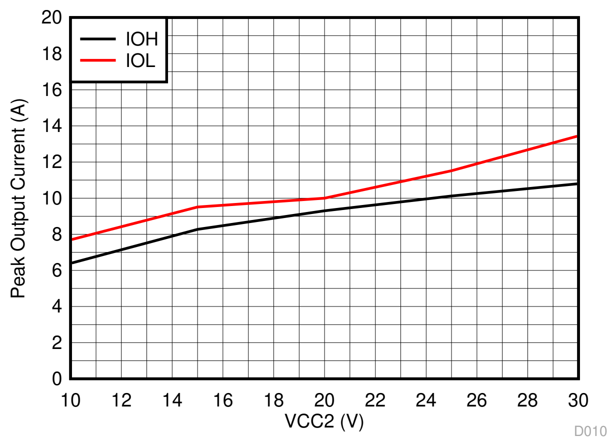
C_{LOAD} = 150 nF

図 6-5. Output-High Drive Current vs Output Voltage



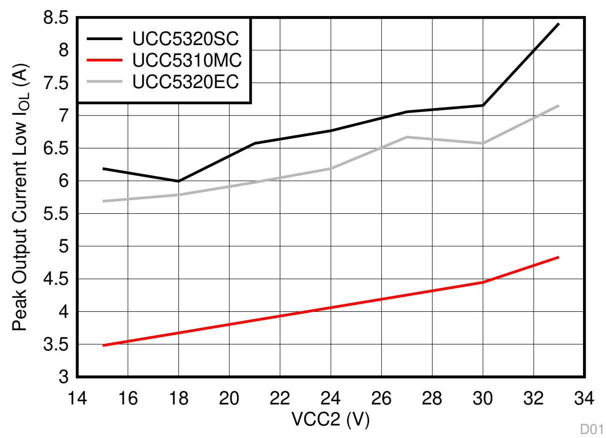
C_{LOAD} = 150 nF

図 6-6. Output-High Drive Current vs Output Voltage



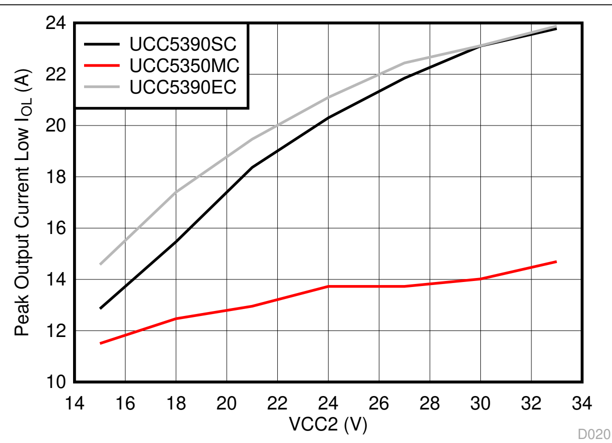
C_{LOAD} = 150 nF

図 6-7. UCC5350SBD Output-High Drive Current vs Output Voltage



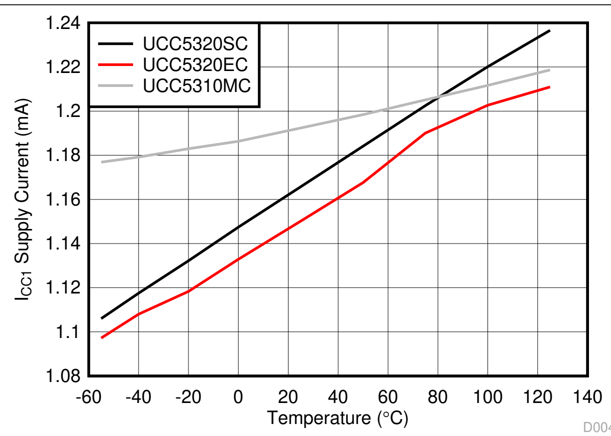
C_{LOAD} = 150 nF

図 6-8. Output-Low Drive Current vs Output Voltage



C_{LOAD} = 150 nF

図 6-9. Output-Low Drive Current vs Output Voltage

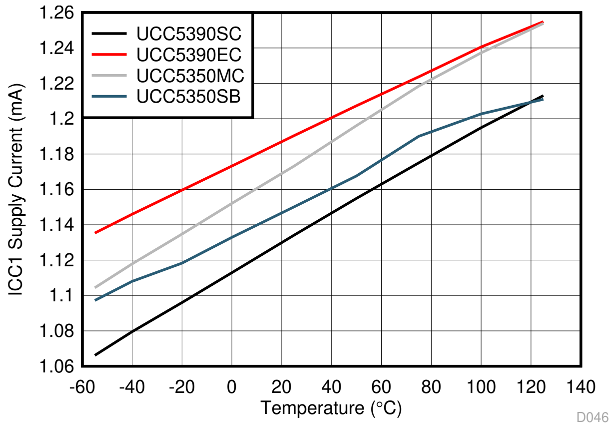


IN+ = L IN– = H

図 6-10. I_{CC1} Supply Current vs Temperature

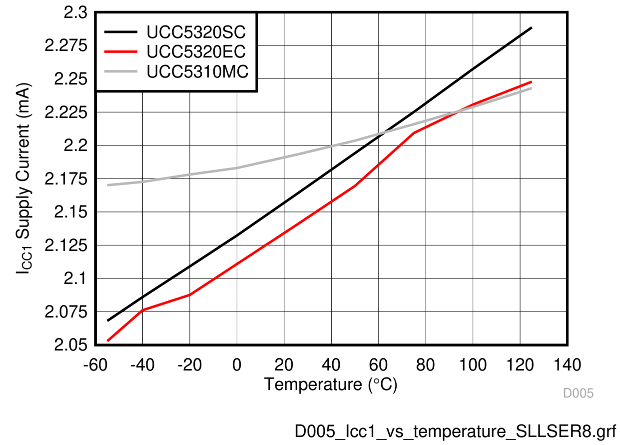
6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



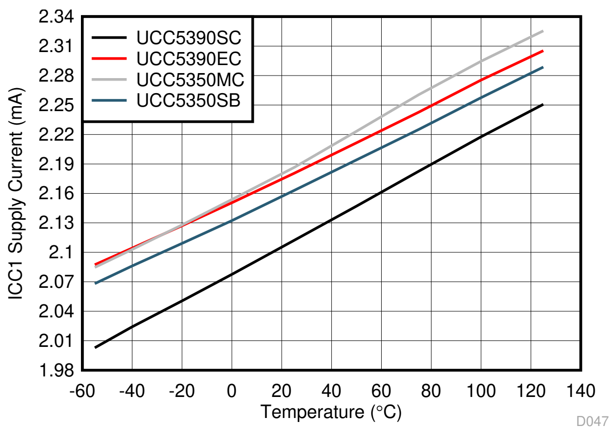
IN+ = L IN– = H

図 6-11. I_{CC1} Supply Current vs Temperature



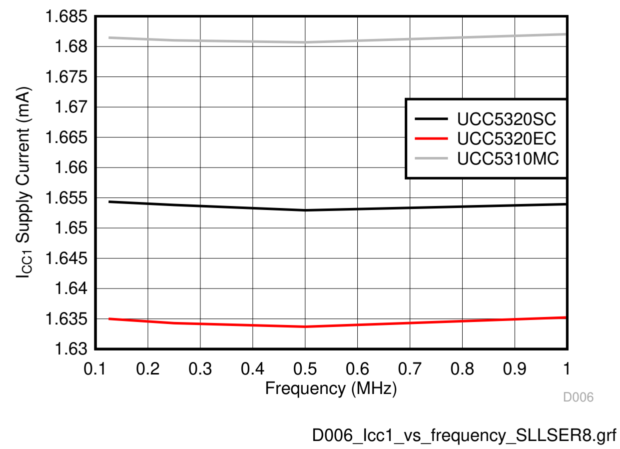
IN+ = H IN– = L

図 6-12. I_{CC1} Supply Current vs Temperature



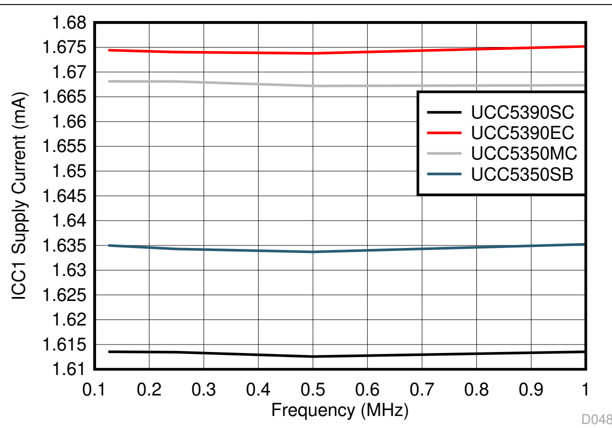
IN+ = H IN– = L

図 6-13. I_{CC1} Supply Current vs Temperature



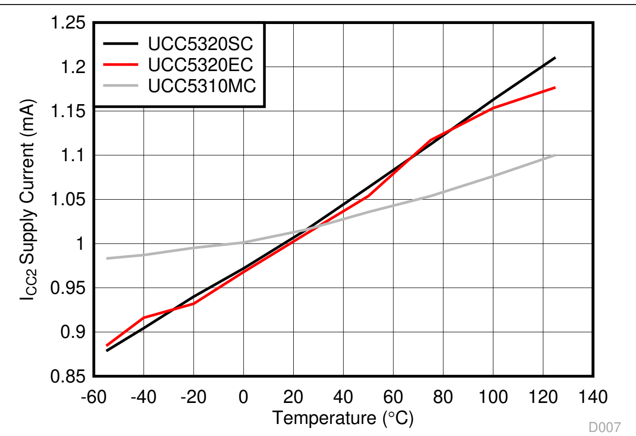
Duty Cycle = 50% T = 25°C

図 6-14. I_{CC1} Supply Current vs Input Frequency



Duty Cycle = 50% T = 25°C

図 6-15. I_{CC1} Supply Current vs Input Frequency

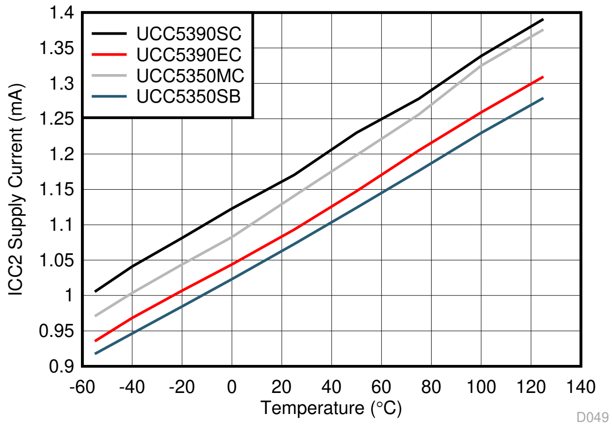


IN+ = L IN– = H

図 6-16. I_{CC2} Supply Current vs Temperature

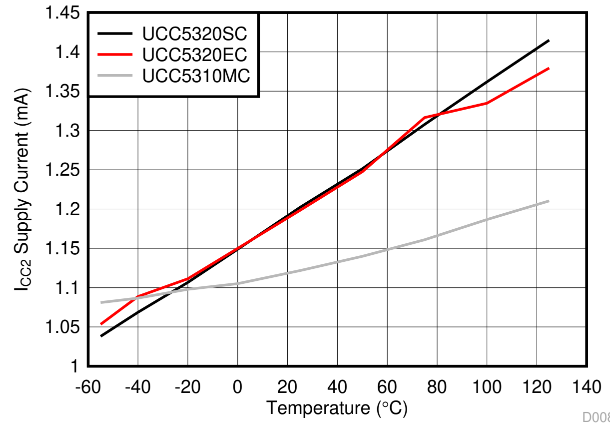
6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



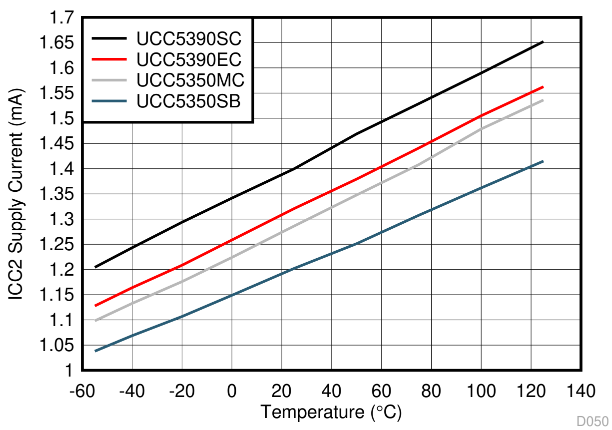
IN+ = L IN– = H

図 6-17. I_{CC2} Supply Current vs Temperature



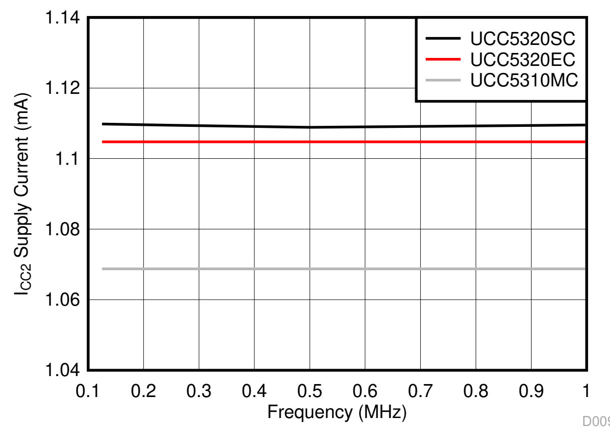
IN+ = H IN– = L

図 6-18. I_{CC2} Supply Current vs Temperature



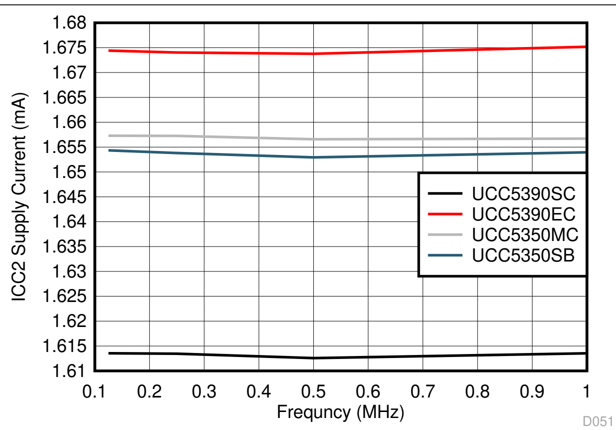
IN+ = H IN– = L

図 6-19. I_{CC2} Supply Current vs Temperature



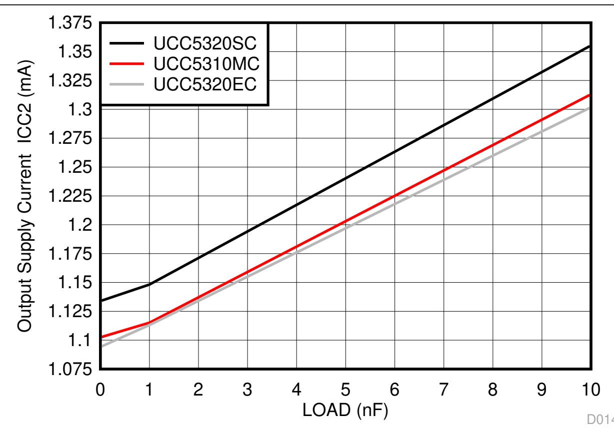
Duty Cycle = 50% T = 25°C

図 6-20. I_{CC2} Supply Current vs Input Frequency



Duty Cycle = 50% T = 25°C

図 6-21. I_{CC2} Supply Current vs Input Frequency

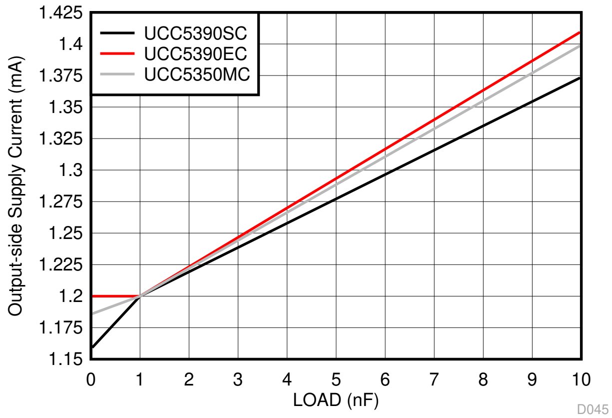


f_{SW} = 1 kHz

図 6-22. I_{CC2} Supply Current vs Load Capacitance

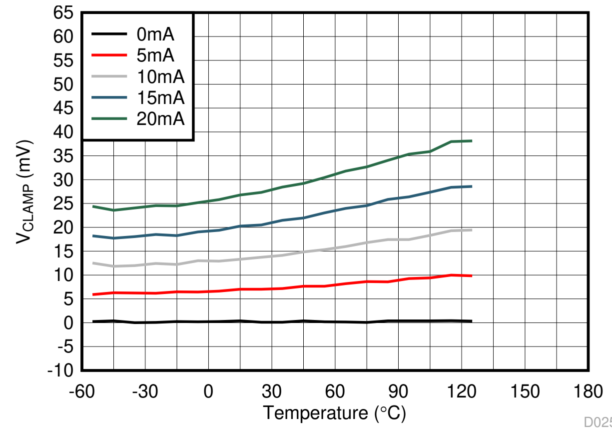
6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



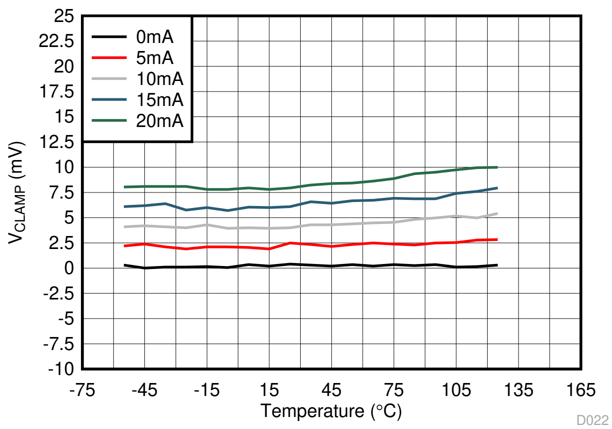
f_{SW} = 1 kHz

図 6-23. I_{CC2} Supply Current vs Load Capacitance



I_{Clamp} = 0mA~20mA

図 6-24. UCC5310M V_{Clamp} vs Temperature



I_{Clamp} = 0mA~20mA

図 6-25. UCC5350M V_{Clamp} vs Temperature

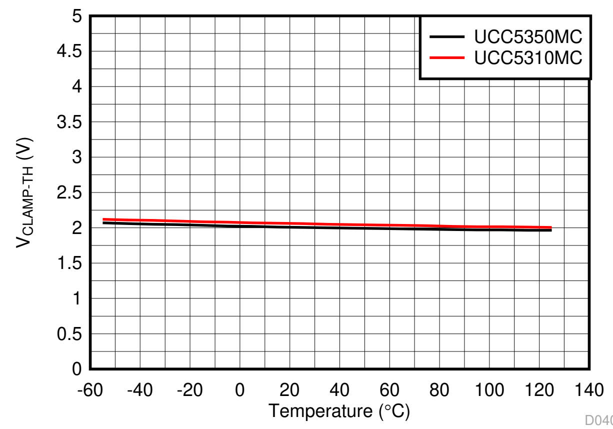


図 6-26. $V_{Clamp\text{-}TH}$ vs Temperature

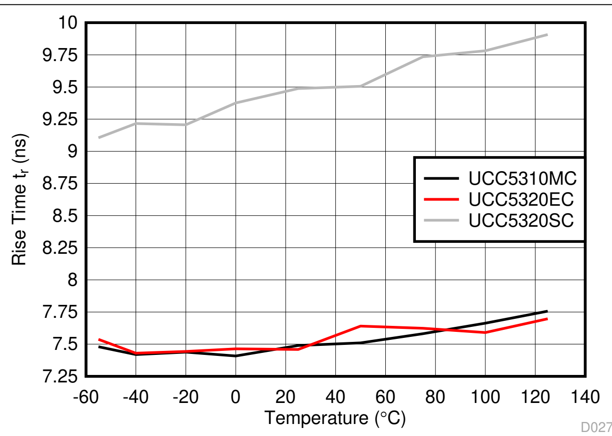


図 6-27. Rise Time vs Temperature

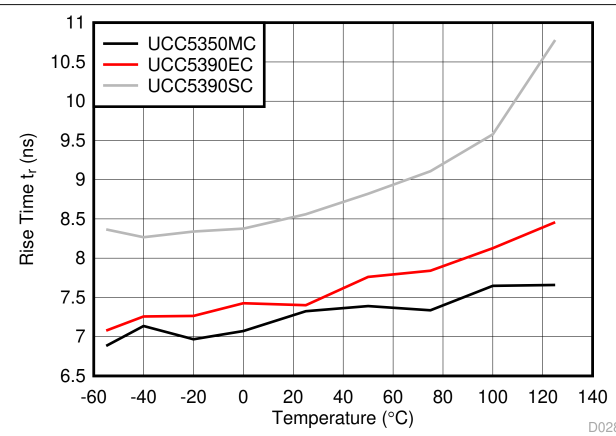


図 6-28. Rise Time vs Temperature

6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)

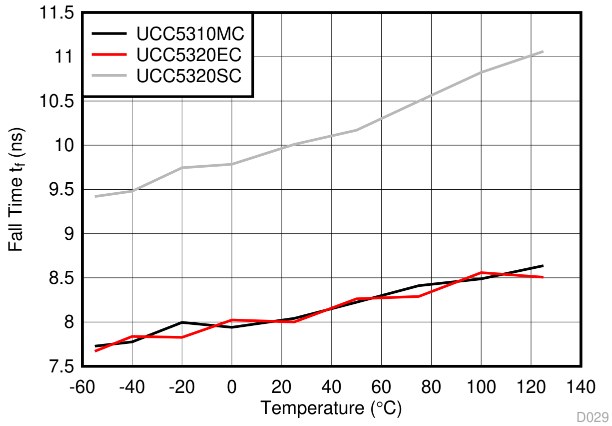


図 6-29. Fall Time Vs Temperature

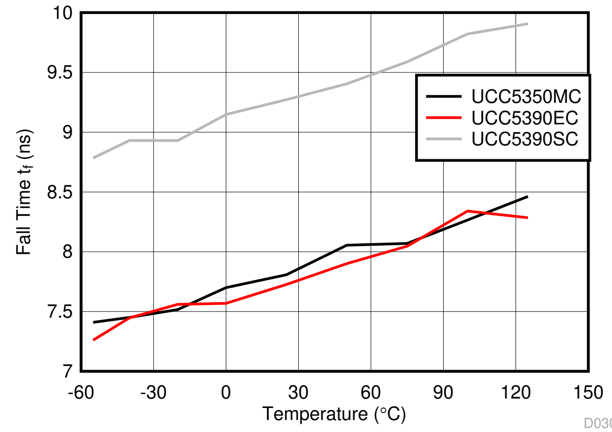


図 6-30. Fall Time vs Temperature

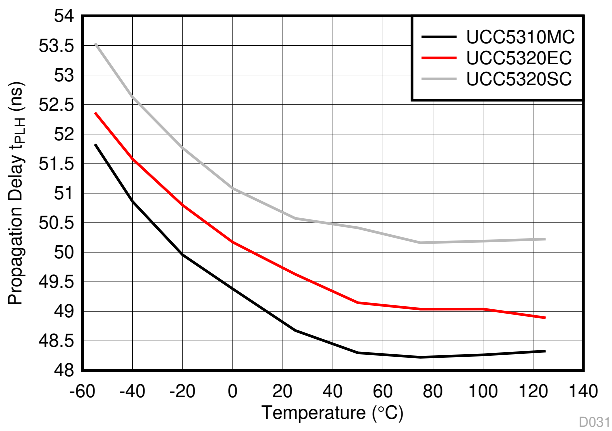


図 6-31. Propagation Delay t_{PLH} vs Temperature

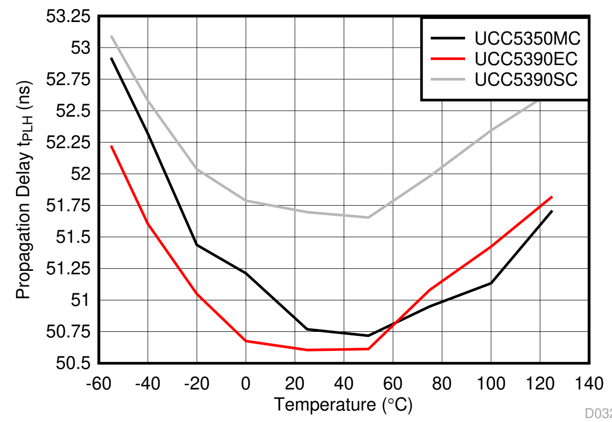


図 6-32. Propagation Delay t_{PLH} vs Temperature

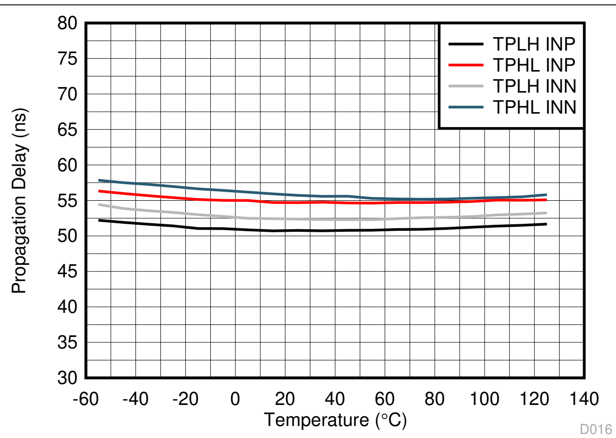


図 6-33. UCC5350SBD Propagation Delay vs Temperature

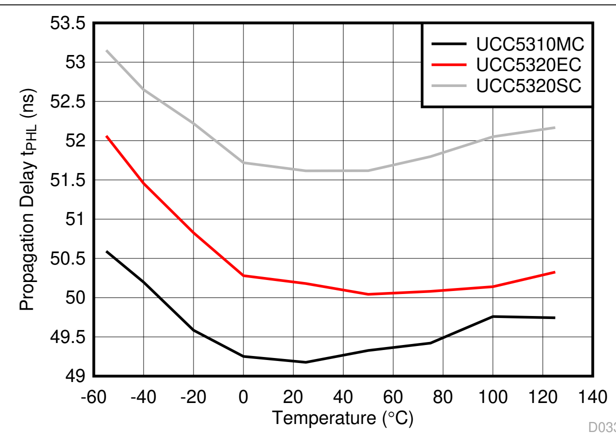


図 6-34. Propagation Delay t_{PHL} vs Temperature

6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)

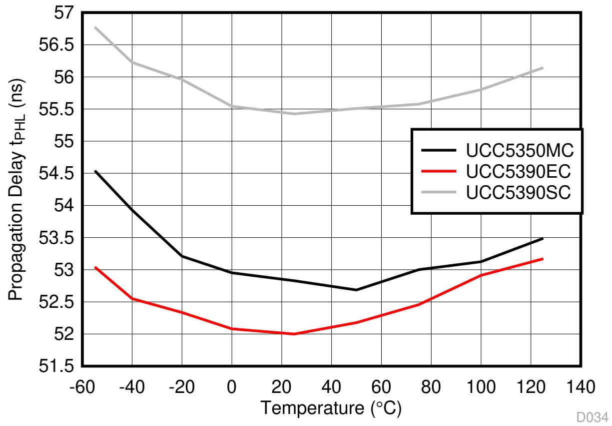
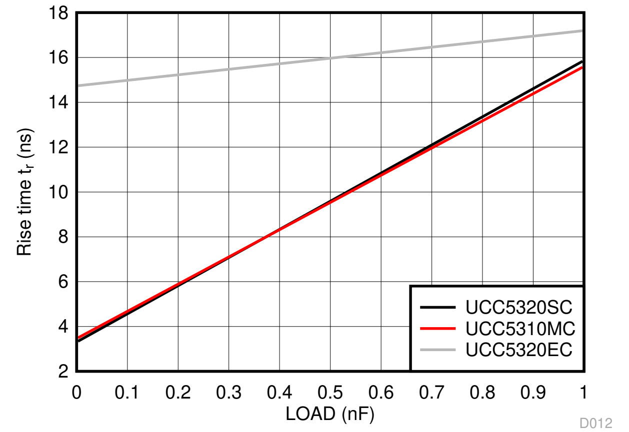
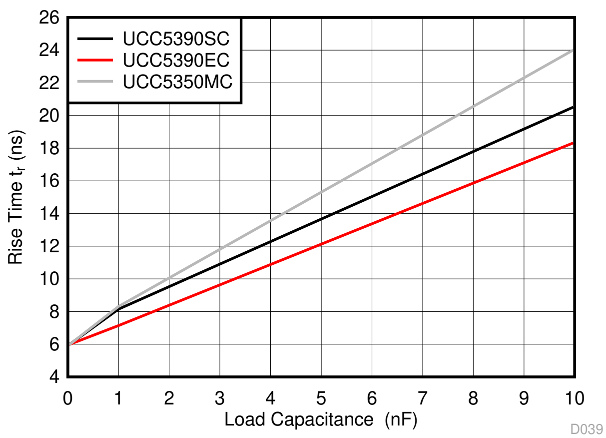


図 6-35. Propagation Delay t_{PHL} vs Temperature



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

図 6-36. Rise Time vs Load Capacitance



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

図 6-37. Rise Time vs Load Capacitance

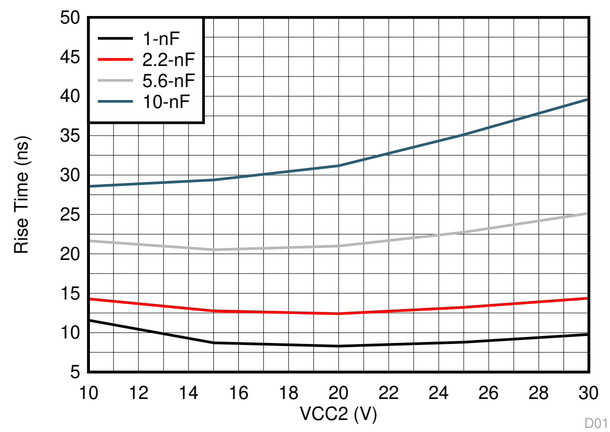
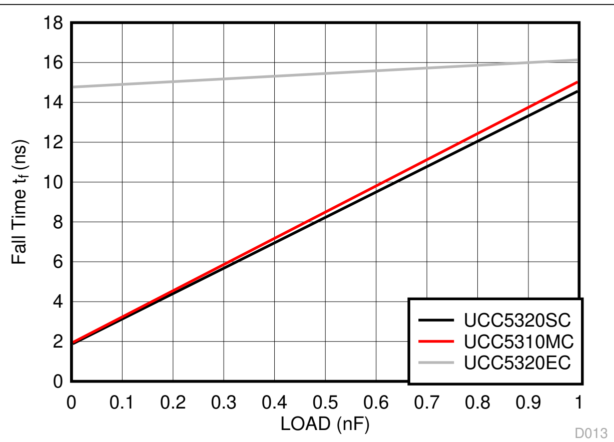
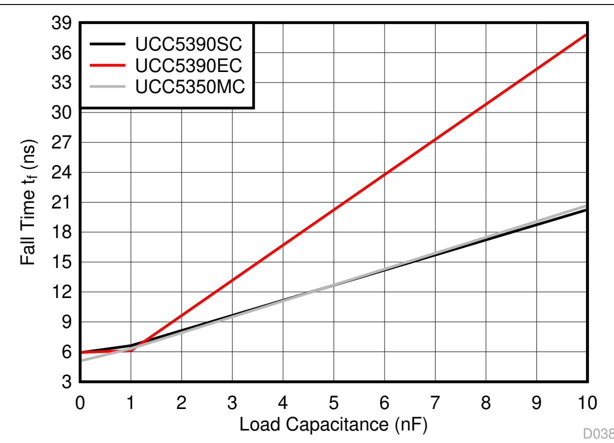


図 6-38. UCC5350SBD Rise Time vs C_L and V_{CC2}



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

図 6-39. Fall Time vs Load Capacitance



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

図 6-40. Fall Time vs Load Capacitance

6.14 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)

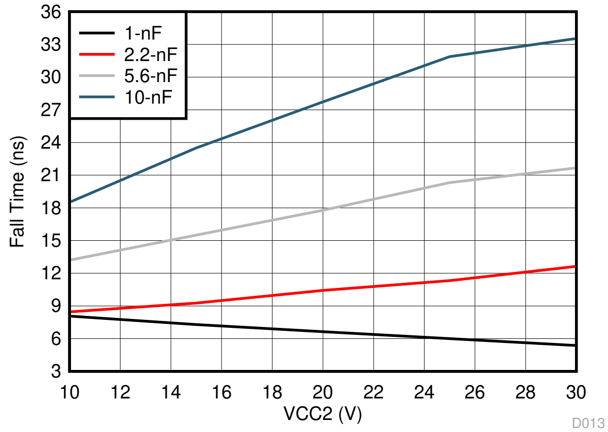


図 6-41. UCC5350SBD Fall Time vs C_L and V_{CC2}

7 Parameter Measurement Information

7.1 Propagation Delay, Inverting, and Noninverting Configuration

図 7-1 shows the propagation delay OUTH and OUTL for noninverting configurations. 図 7-2 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

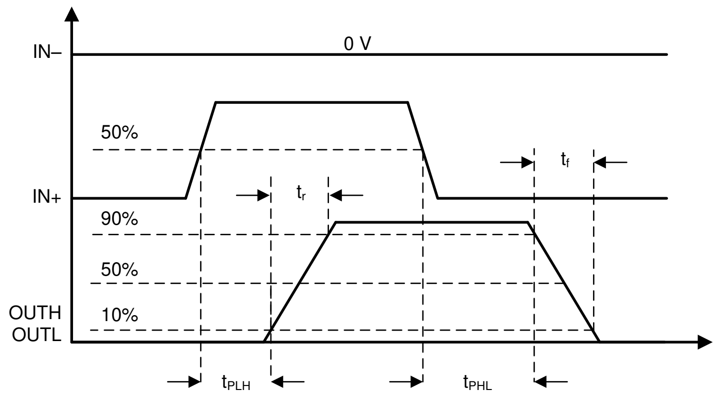


図 7-1. OUTH and OUTL Propagation Delay, Noninverting Configuration

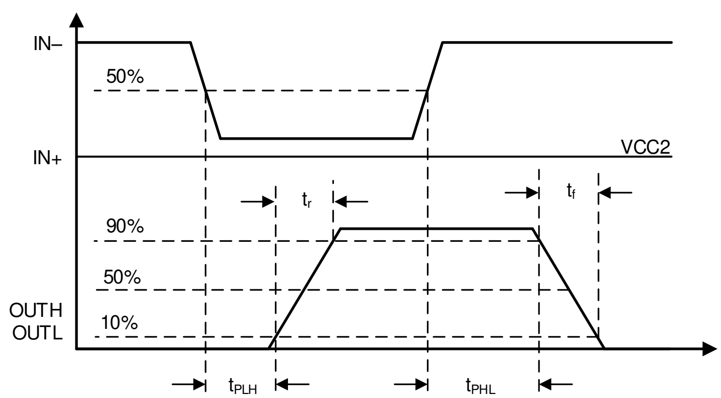


図 7-2. OUTH and OUTL Propagation Delay, Inverting Configuration

7.1.1 CMTI Testing

図 7-3, 図 7-4, and 図 7-5 are simplified diagrams of the CMTI testing configuration used for each device type.

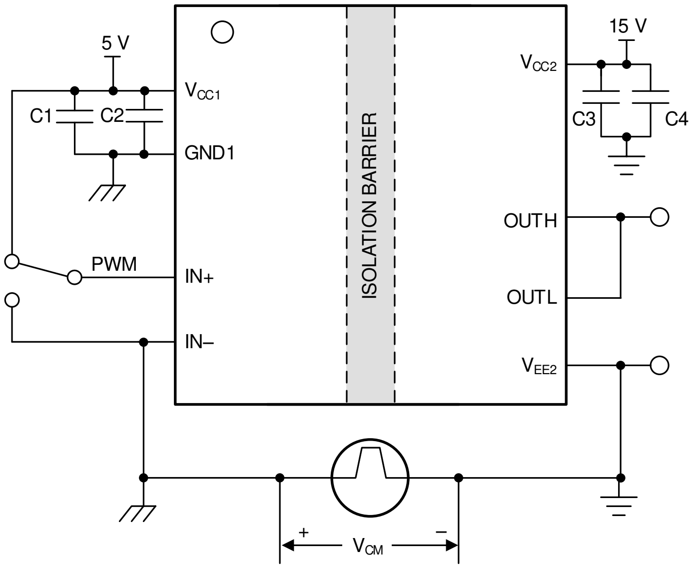


図 7-3. CMTI Test Circuit for Split Output (UCC53x0S)

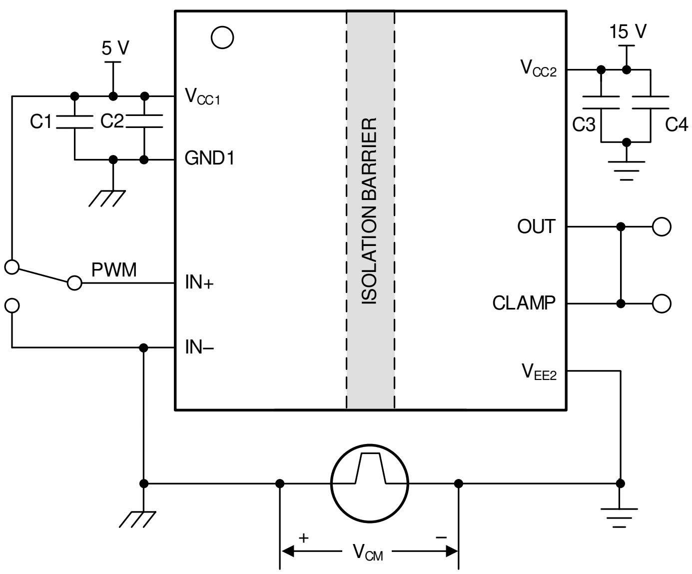


図 7-4. CMTI Test Circuit for Miller Clamp (UCC53x0M)

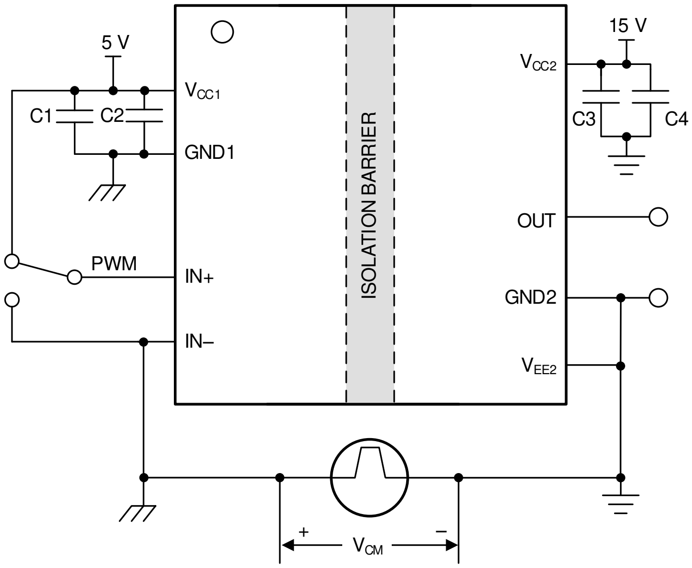


図 7-5. CMTI Test Circuit for UVLO2 with Respect to GND2 (UCC53x0E)

8 Detailed Description

8.1 Overview

The UCC53x0 family of isolated gate drivers has three variations: split output, Miller clamp, and UVLO2 referenced to GND2 (see セクション 4). The isolation inside the UCC53x0 family of devices is implemented with high-voltage SiO_2-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see 図 8-2). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC53x0 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 8-1, shows a functional block diagram of a typical channel. 図 8-2 shows a conceptual detail of how the OOK scheme works.

図 8-1 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

8.2 Functional Block Diagram

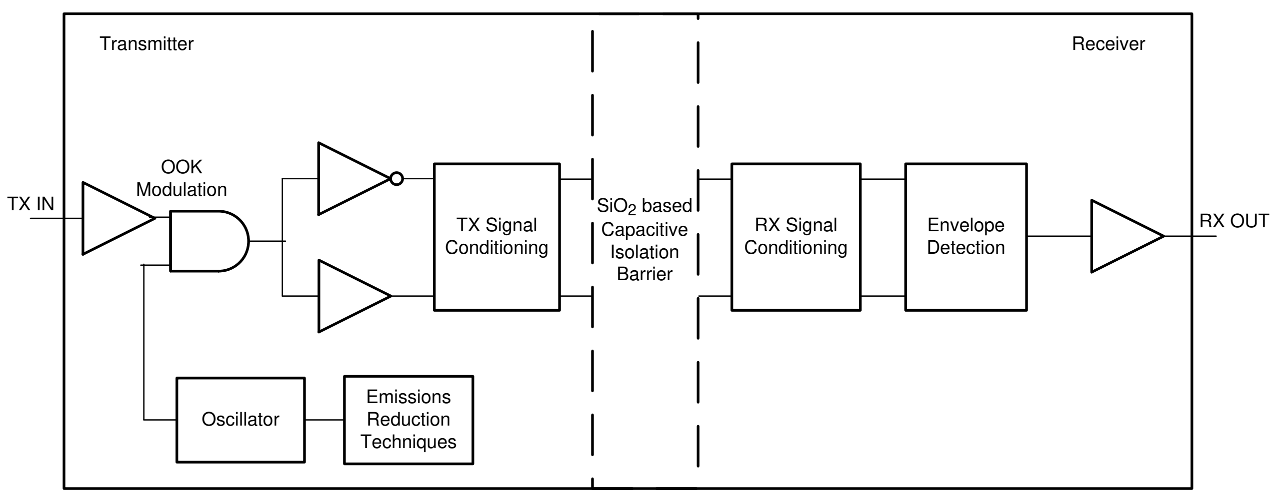


図 8-1. Conceptual Block Diagram of a Capacitive Data Channel

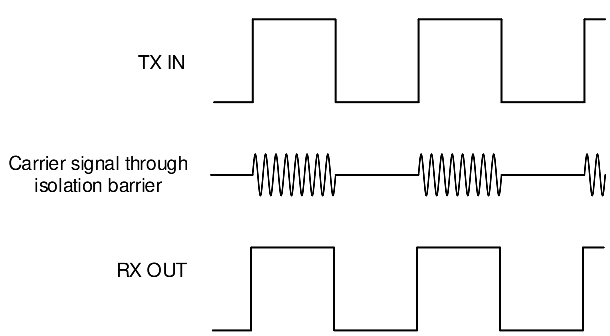


図 8-2. On-Off Keying (OOK) Based Modulation Scheme

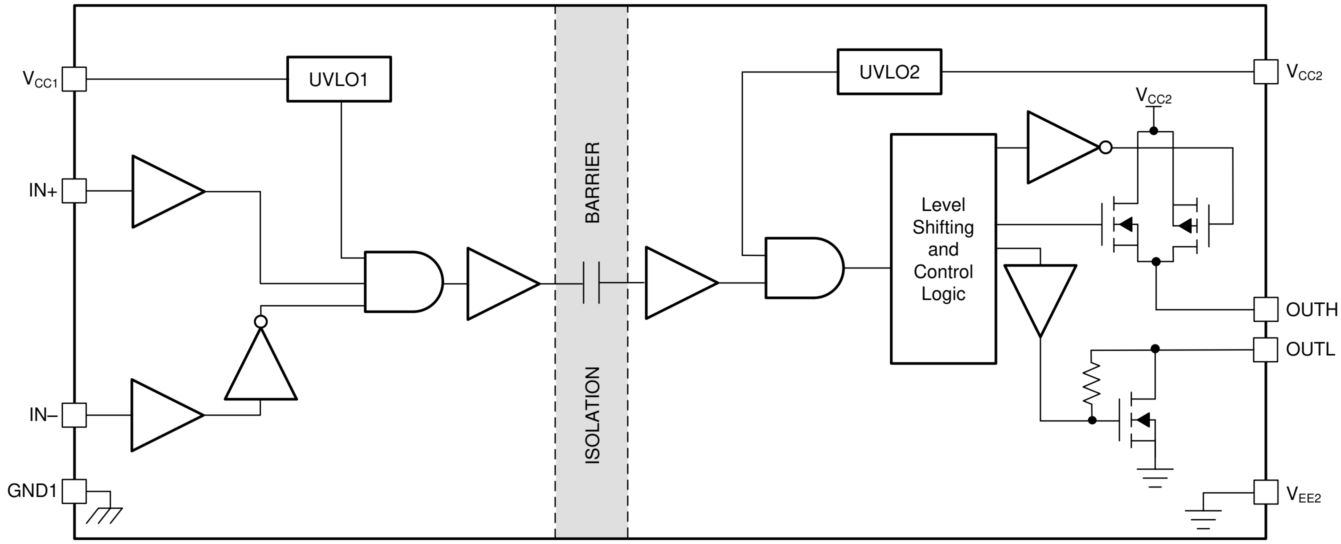


図 8-3. Functional Block Diagram — Split Output (UCC53x0S)

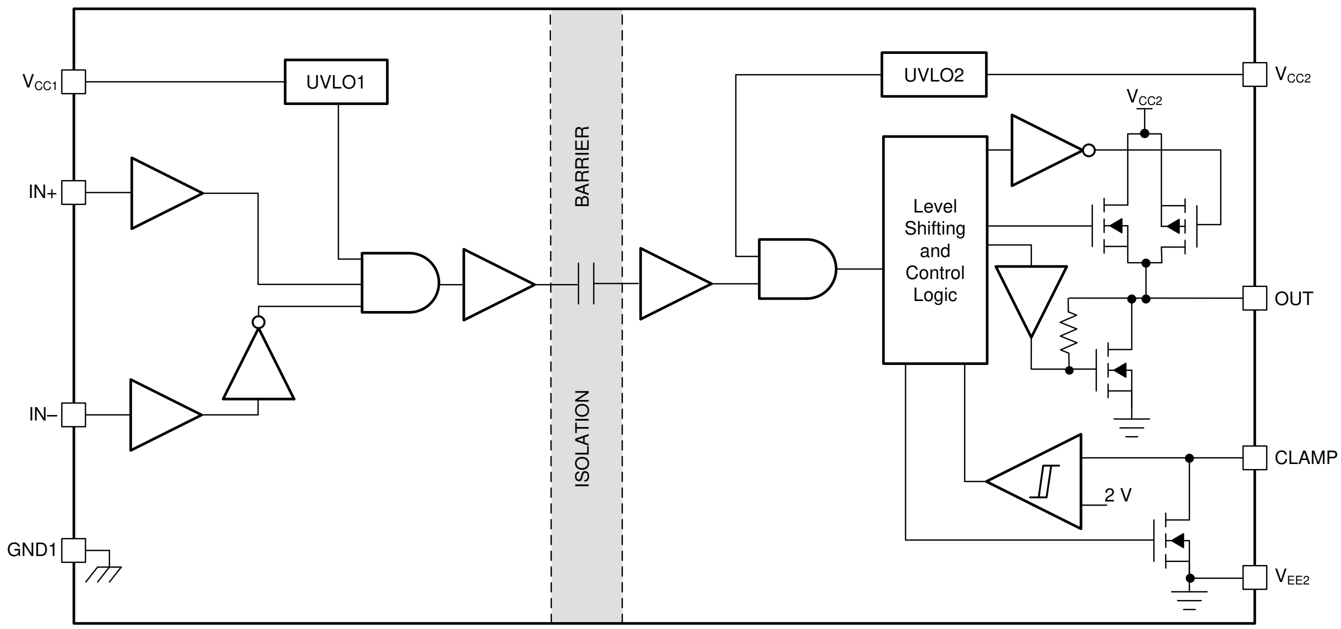


図 8-4. Functional Block Diagram — Miller Clamp (UCC53x0M)

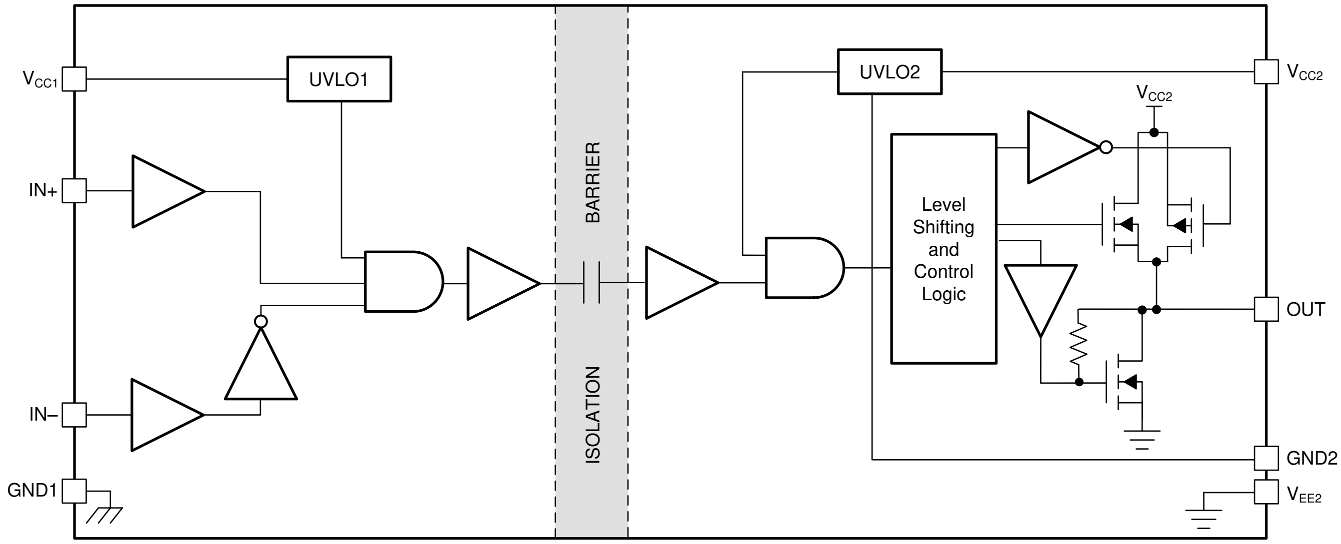


図 8-5. Functional Block Diagram — UVLO With Respect to GND2 (UCC53x0E)

8.3 Feature Description

8.3.1 Power Supply

The V_{CC1} input power supply supports a wide voltage range from 3 V to 15 V and the V_{CC2} output supply supports a voltage range from 9.5 V to 33 V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the V_{CC2} and V_{EE2} output supplies for bipolar operation are 15 V and –8 V with respect to GND2 for IGBTs and 20 V and –5 V for SiC MOSFETs.

For operation with unipolar supply, the V_{CC2} supply is connected to 15 V with respect to VEE2 for IGBTs, and 20 V for SiC MOSFETs. The V_{EE2} supply is connected to 0 V. In this use case, the UCC53x0 device with Miller clamping function (UCC53x0M) can be used . The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the V_{EE2} supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate.

8.3.2 Input Stage

The input pins (IN+ and IN–) of the UCC53x0 family are based on CMOS-compatible input-threshold logic that is completely isolated from the V_{CC2} supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC53x0 family has a typical high threshold ($V_{IT+(IN)}$) of 0.55 × V_{CC1} and a typical low threshold of 0.45 × V_{CC1}. A wide hysteresis ($V_{hys(IN)}$) of 0.1 × V_{CC1} makes for good noise immunity and stable operation. If either of the inputs are left open, 128 kΩ of internal pull-down resistance forces the IN+ pin low and 128 kΩ of internal resistance pulls IN– high. However, TI still recommends grounding an input or tying to VCC1 if it is not being used for improved noise immunity.

Because the input side of the UCC53x0 family is isolated from the output driver, the input signal amplitude can be larger or smaller than V_{CC2} provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient V_{CC2} for any gate. However, the amplitude of any signal applied to IN+ or IN– must never be at a voltage higher than V_{CC1}.

8.3.3 Output Stage

The output stages of the UCC53x0 family feature a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. 表 8-1 lists the typical internal resistance values of the pull-up and pull-down structure.

表 8-1. UCC53x0 On-Resistance

DEVICE OPTION	R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	UNIT
UCC5320SC and UCC5320EC	4.5	12	0.65	Not applicable	Ω
UCC5310MC	4.5	12	1.3	1.3	Ω
UCC5390SC and UCC5390EC	0.76	12	0.13	Not applicable	Ω
UCC5350MC	1.54	12	0.26	0.26	Ω
UCC5350SB	1.54	12	0.26	Not applicable	Ω

The R_{OH} parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pull-up N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC53x0 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter, which yields a faster turn-on. The turn-on-phase output resistance is the parallel combination $R_{OH} \| R_{NMOS}$.

The pull-down structure in the UCC53x0 S and E versions is simply composed of an N-channel MOSFET. For the M version, an additional FET is connected in parallel with the pull-down structure when the CLAMP and OUT pins are connected to the gate of the IGBT or MOSFET. The output voltage swing between V_{CC2} and V_{EE2} provides rail-to-rail operation.

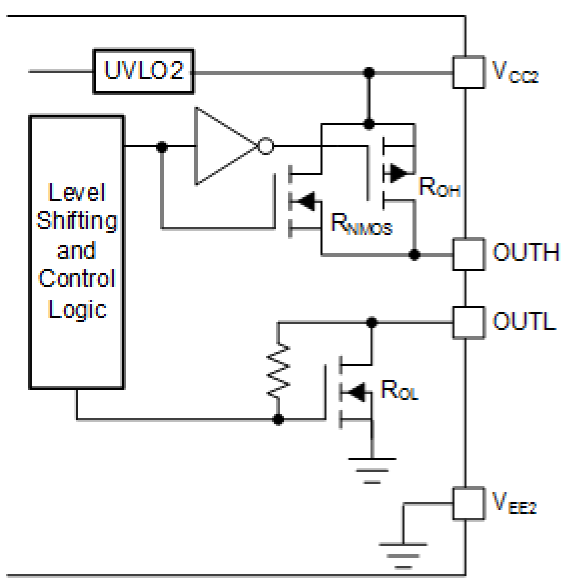


図 8-6. Output Stage—S Version

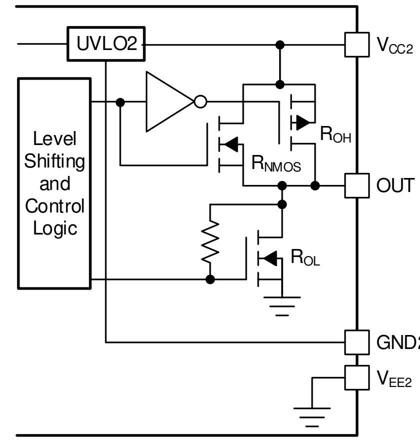


図 8-7. Output Stage—E Version

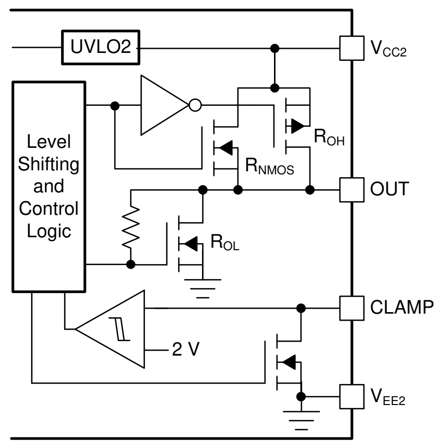


図 8-8. Output Stage—M Version

8.3.4 Protection Features

8.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V_{CC1} and V_{CC2} supplies between the V_{CC1} and GND1, and V_{CC2} and V_{EE2} pins to prevent an underdriven condition on IGBTs and MOSFETs. When V_{CC} is lower than $V_{IT+\ (UVLO)}$ at device start-up or lower than $V_{IT-(UVLO)}$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN–) as shown in 表 8-2. The V_{CC} UVLO protection has a hysteresis feature ($V_{hys(UVLO)}$). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. 図 8-9 shows the UVLO functions.

表 8-2. UCC53x0 V_{CC1} UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUT, OUTL
V_{CC1} – GND1 < $V_{IT+(UVLO1)}$ during device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

表 8-2. UCC53x0 V_{CC1} UVLO Logic (続き)

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUT, OUTL
V_{CC1} – GND1 < $V_{IT–(UVLO1)}$ after device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

表 8-3. UCC53x0 V_{CC2} UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUT, OUTL
V_{CC2} – V_{EE2} < $V_{IT+(UVLO2)}$ during device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L
V_{CC2} – V_{EE2} < $V_{IT–(UVLO2)}$ after device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

When V_{CC1} or V_{CC2} drops below the UVLO1 or UVLO2 threshold, a delay, t_{UVLO1_rec} or t_{UVLO2_rec}, occurs on the output when the supply voltage rises above $V_{IT+(UVLO)}$ or $V_{IT+(UVLO2)}$ again. 図 8-9 shows this delay.

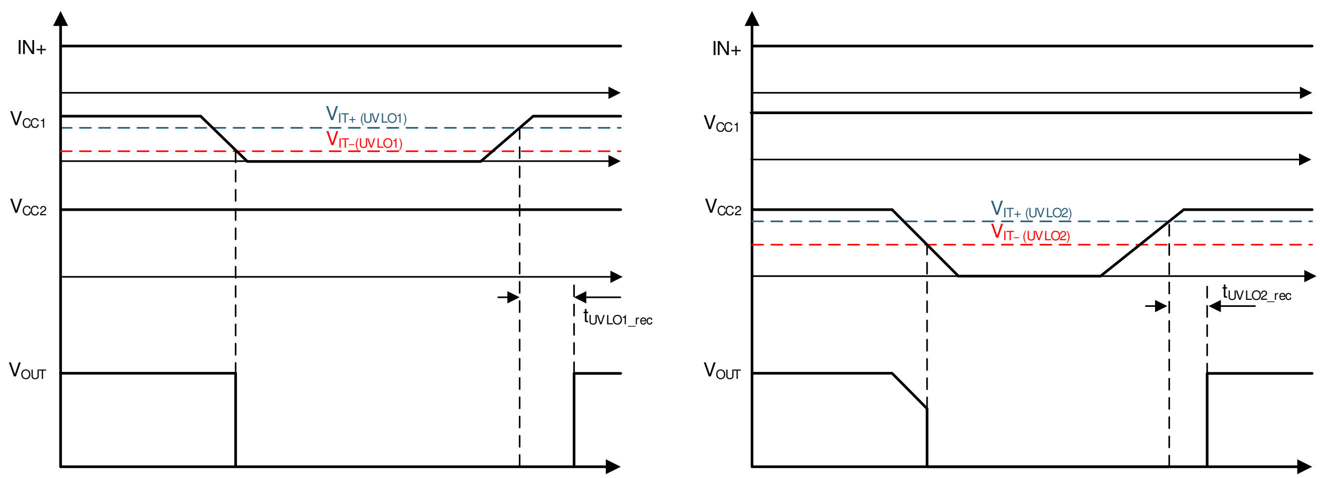


図 8-9. UVLO Functions

8.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the V_{CC2} supply. This feature prevents false IGBT and MOSFET turn-on on the OUT and CLAMP pins by clamping the output to approximately 2 V.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pull-up resistor while the lower NMOS gate is tied to the driver output through a 500-kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

8.3.4.4 Active Miller Clamp (UCC53x0M)

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground (V_{EE2}) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. 図 9-2 shows a typical application circuit of UCC5310M and UCC5350M.

8.4 Device Functional Modes

表 8-4 lists the functional modes for the UCC53x0 devices assuming V_{CC1} and V_{CC2} are in the recommended range.

表 8-4. Function Table for UCC53x0S

IN+	IN–	OUTH	OUTL
Low	X	Hi-Z	Low
X	High	Hi-Z	Low
High	Low	High	High-Z

表 8-5. Function Table for UCC53x0M and UCC53x0E

IN+	IN–	OUT
Low	X	Low
X	High	Low
High	Low	High

8.4.1 ESD Structure

図 8-10 shows the multiple diodes involved in the ESD protection components of the UCC53x0 devices. This provides pictorial representation of the absolute maximum rating for the device.

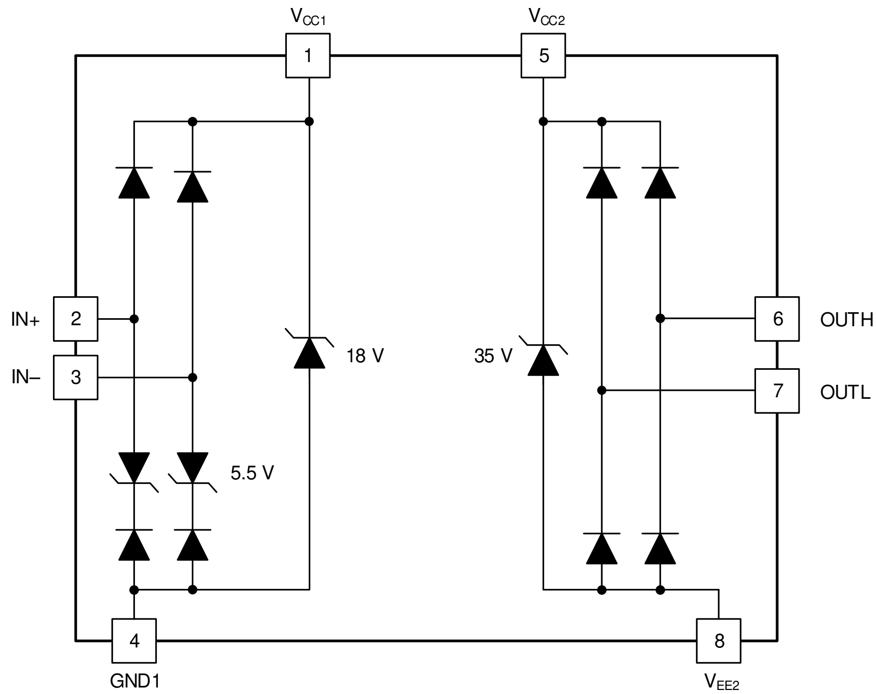


図 8-10. ESD Structure

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The UCC53x0 is a family of simple, isolated gate drivers for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

The UCC53x0 family of devices has three pinout configurations, featuring split outputs, Miller clamp, and UVLO with reference to GND2. The UCC5320SC, UCC5350SB, and UCC5390SC have a split output, OUTH and OUTL. The two pins can be used to separately decouple the power transistor turnon and turnoff commutations. The UCC5310MC and UCC5350MC feature active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The UCC5320EC and UCC5390EC offer true UVLO protection by monitoring the voltage between the V_{CC2} and GND2 pins to prevent the power transistors from operating in a saturation region. The UCC53x0 family of devices comes in an 8-pin D and 8-pin DWV package options and have a creepage, or clearance, of 4 mm and 8.5 mm respectively, which are suitable for applications where basic or reinforced isolation is required. Different drive strengths enable a simple driver platform to be used for applications demanding power transistors with different power ratings. Specifically, the UCC5390 device offers a 10-A minimum drive current which can help remove the external current buffer used to drive high power transistors.

9.2 Typical Application

The circuits in 図 9-1, 図 9-2, and 図 9-3 show a typical application for driving IGBTs.

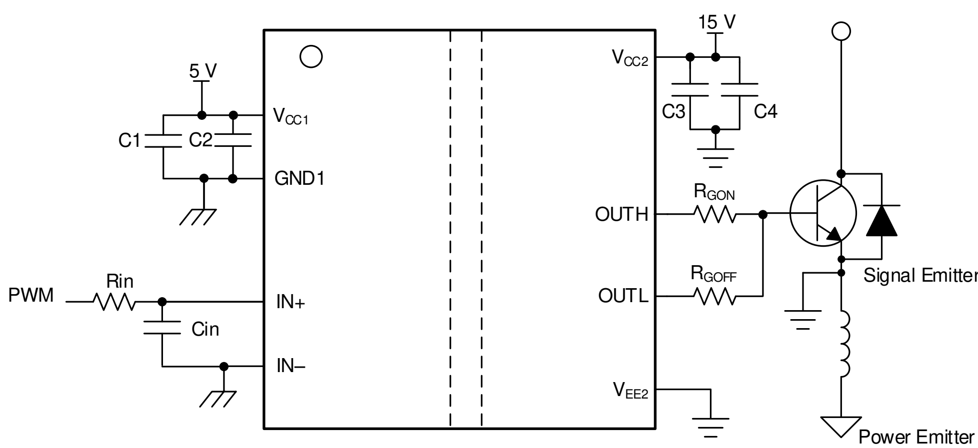


図 9-1. Typical Application Circuit for UCC53x0S to Drive IGBT

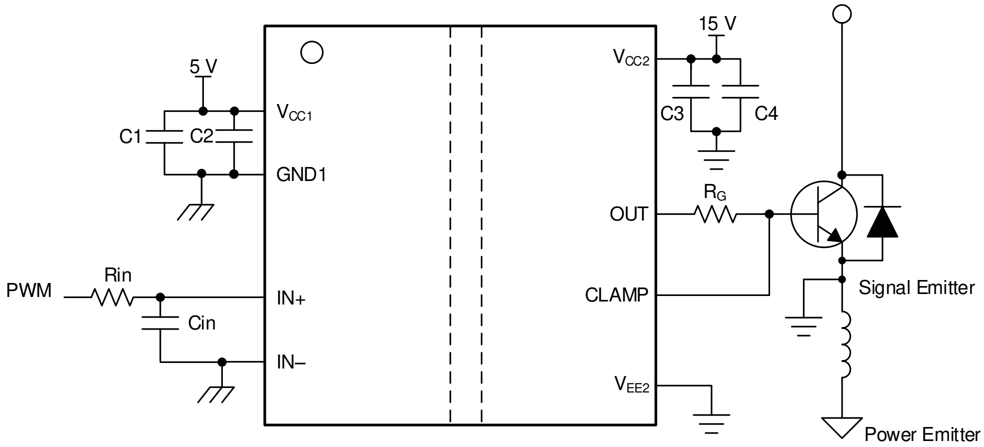


図 9-2. Typical Application Circuit for UCC5310M and UCC5350M to Drive IGBT

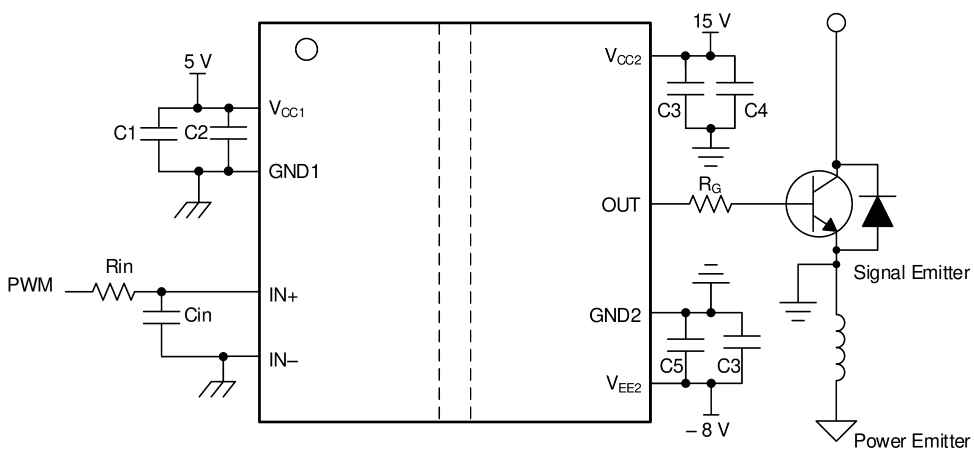


図 9-3. Typical Application Circuit for UCC5320E and UCC5390E to Drive IGBT

9.2.1 Design Requirements

表 9-1 lists the recommended conditions to observe the input and output of the UCC5320S split-output gate driver with the IN– pin tied to the GND1 pin.

表 9-1. UCC5320S Design Requirements

PARAMETER	VALUE	UNIT
V_{CC1}	3.3	V
V_{CC2}	15	V
IN+	3.3	V
IN–	GND1	-
Switching frequency	10	kHz
IGBT	IKW50N65H5	-

9.2.2 Detailed Design Procedure

9.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter, R_{IN}-C_{IN}, can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R_{IN} resistor with a value from 0 Ω to 100 Ω and a C_{IN} capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for R_{IN} is 51 Ω and C_{IN} is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

9.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pull-up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined peak source current is 4.3 A for the UCC5320 family and 17 A for the UCC5390 family and 17 A for the UCC5390 family. Use 式 1 to estimate the peak source current using the UCC5320S as an example.

$$I_{OH} = \min\left(4.3\text{ A}, \frac{V_{CC2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{1}$$

where

- R_{ON} is the external turn-on resistance.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 0Ω for our example.
- I_{OH} is the peak source current which is the minimum value between 4.3 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak source current is approximately 1.8 A as calculated in 式 2.

$$I_{OH} = \frac{V_{CC2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{15\text{ V}}{4.5\ \Omega \,||\, 12\ \Omega + 5.1\ \Omega + 0\ \Omega} \approx 1.8\text{ A} \tag{2}$$

Similarly, use 式 3 to calculate the peak sink current.

$$I_{OL} = \min\left(4.4\text{ A}, \frac{V_{CC2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right) \tag{3}$$

where

- R_{OFF} is the external turn-off resistance.
- I_{OL} is the peak sink current which is the minimum value between 4.4 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum value between 式 4 and 4.4 A.

$$I_{OL} = \frac{V_{CC2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}} = \frac{15\ V}{0.65\ \Omega + 10\ \Omega + 0\ \Omega} \approx 1.4\ A \quad (4)$$

注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

9.2.2.3 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC53x0 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC53x0 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The P_{GDQ} parameter is measured on the bench with no load connected to the OUT or OUTH and OUTL pins at a given V_{CC1}, V_{CC2}, switching frequency, and ambient temperature. In this example, V_{CC1} is 3.3V and V_{CC2} is 15 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 10 kHz, is measured to be I_{CC1} = 1.67 mA and I_{CC2} = 1.11 mA . Therefore, use 式 5 to calculate P_{GDQ}.

$$P_{GDQ} = V_{CC1} \times I_{VCC1} + V_{CC2} \times I_{CC2} \approx 22mW \quad (5)$$

The second component is the switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 式 6 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = V_{CC2} \times Q_G \times f_{SW} \quad (6)$$

where

- Q_G is the gate charge of the power transistor at V_{CC2}.

So, for this example application the total dynamic loss from load switching is approximately 18 mW as calculated in 式 7.

$$P_{GSW} = 15\ V \times 120\ nC \times 10\ kHz = 18\ mW \quad (7)$$

Q_G represents the total gate charge of the power transistor switching 520 V at 50 A, and is subject to change with different testing conditions. The UCC5320S gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC5320S. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4.3 A/4.4 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2}\left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right) \tag{8}$$

In this design example, all the predicted source and sink currents are less than 4.3 A and 4.4 A, therefore, use 式 9 to estimate the UCC53x0 gate-driver loss.

$$P_{GDO} = \frac{18\ \text{mW}}{2}\left(\frac{12\ \Omega \,||\, 4.5\ \Omega}{12\ \Omega \,||\, 4.5\ \Omega + 5.1\ \Omega + 0\ \Omega} + \frac{0.65\ \Omega}{0.65\ \Omega + 10\ \Omega + 0\ \Omega}\right) \approx 4.1\ \text{mW} \tag{9}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = f_{SW} \times \left[4.3\ \text{A} \times \int_0^{T_{R\_Sys}} \left(V_{CC2} - V_{OUTH}(t)\right) dt + 4.4\ \text{A} \times \int_0^{T_{F\_Sys}} V_{OUTL}(t) dt\right] \tag{10}$$

where

- $V_{OUTH/L(t)}$ is the gate-driver OUTH and OUTL pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (4.3 A at turnon and 4.4 A at turnoff) charging or discharging a load capacitor. Then, the $V_{OUTH/L(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} is a combination of case 1 and case 2, and the equations can be easily identified for the pull-up and pull-down based on this discussion.

Use 式 11 to calculate the total gate-driver loss dissipated in the UCC53x0 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 22\text{mW} + 4.1\ \text{mW} = 26.1\ \text{mW} \tag{11}$$

9.2.2.4 Estimating Junction Temperature

Use the equation below to estimate the junction temperature (T_J) of the UCC53x0 family.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{12}$$

where

- T_C is the UCC53x0 case-top temperature measured with a thermocouple or some other instrument.
- Ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The Ψ_{JT} parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

9.2.3 Selecting V_{CC1} and V_{CC2} Capacitors

Bypass capacitors for the V_{CC1} and V_{CC2} supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

9.2.3.1 Selecting a V_{CC1} Capacitor

A bypass capacitor connected to the V_{CC1} pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V_{CC1} pin, a tantalum or electrolytic capacitor with a value greater than 1 µF should be placed in parallel with the MLCC.

9.2.3.2 Selecting a V_{CC2} Capacitor

A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are selected for the C_{VCC2} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC2} pin, a tantalum or electrolytic capacitor with a value greater than 10 µF should be used in parallel with C_{VCC2}.

9.2.3.3 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turn-on and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

図 9-4 shows the first example with negative bias turn-off on the output using a Zener diode on the isolated power-supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply is equal to 20 V, the turn-off voltage is –5.1 V and the turn-on voltage is 20 V – 5.1 V ≈ 15 V.

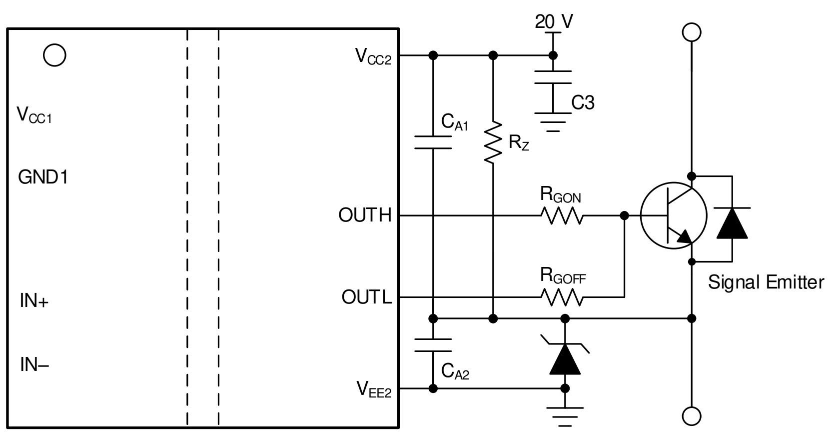


図 9-4. Negative Bias With Zener Diode on Iso-Bias Power-Supply Output

図 9-5 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across V_{CC2} and GND2 determines the positive drive output voltage and the power supply across V_{EE2} and GND2 determines the negative turn-off voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

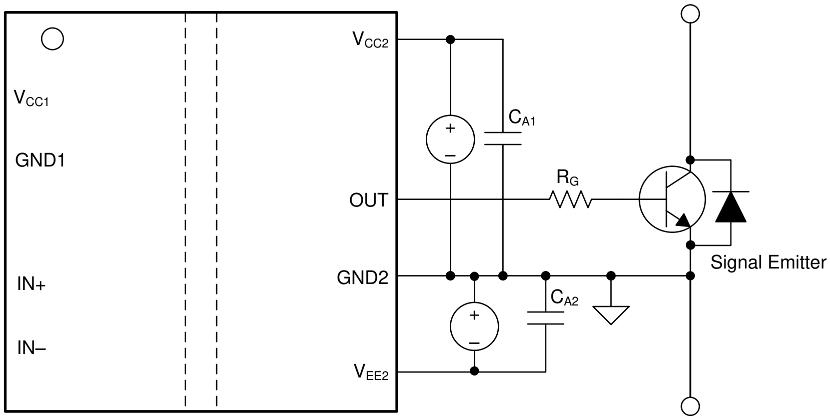
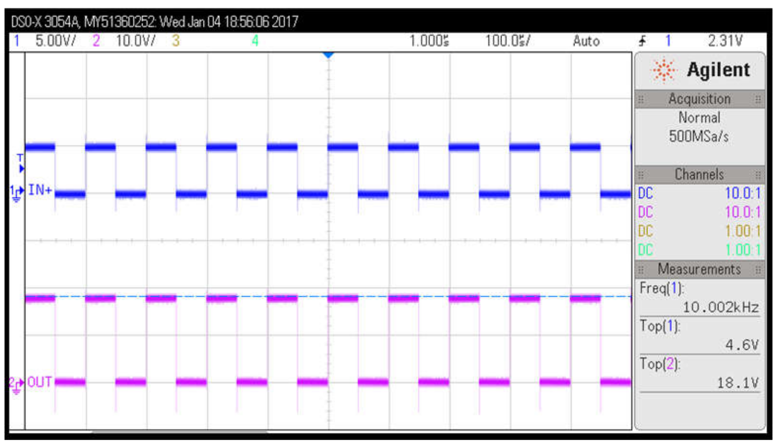


図 9-5. Negative Bias With Two Iso-Bias Power Supplies (UCC5320E and UCC5390E)

9.2.4 Application Curve



V_{CC2} = 20 V V_{EE2} = GND f_{SW} = 10 kHz

図 9-6. PWM Input and Gate Voltage Waveform

10 Power Supply Recommendations

The recommended input supply voltage (V_{CC1}) for the UCC53x0 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage (V_{CC2}) is determined by the internal UVLO protection feature of the device. The V_{CC1} and V_{CC2} voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50 µs by the UVLO protection feature. For more information on UVLO, see セクション 8.3.4.1. The higher limit of the V_{CC2} range depends on the maximum gate voltage of the power device that is driven by the UCC53x0 device, and should not exceed the recommended maximum V_{CC2} of 33 V. A local bypass capacitor should be placed between the V_{CC2} and V_{EE2} pins, with a value of 220-nF to 10-µF for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the V_{CC1} and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC53x0 device, this bypass capacitor has a minimum recommended value of 100 nF.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* data sheet and *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

11 Layout

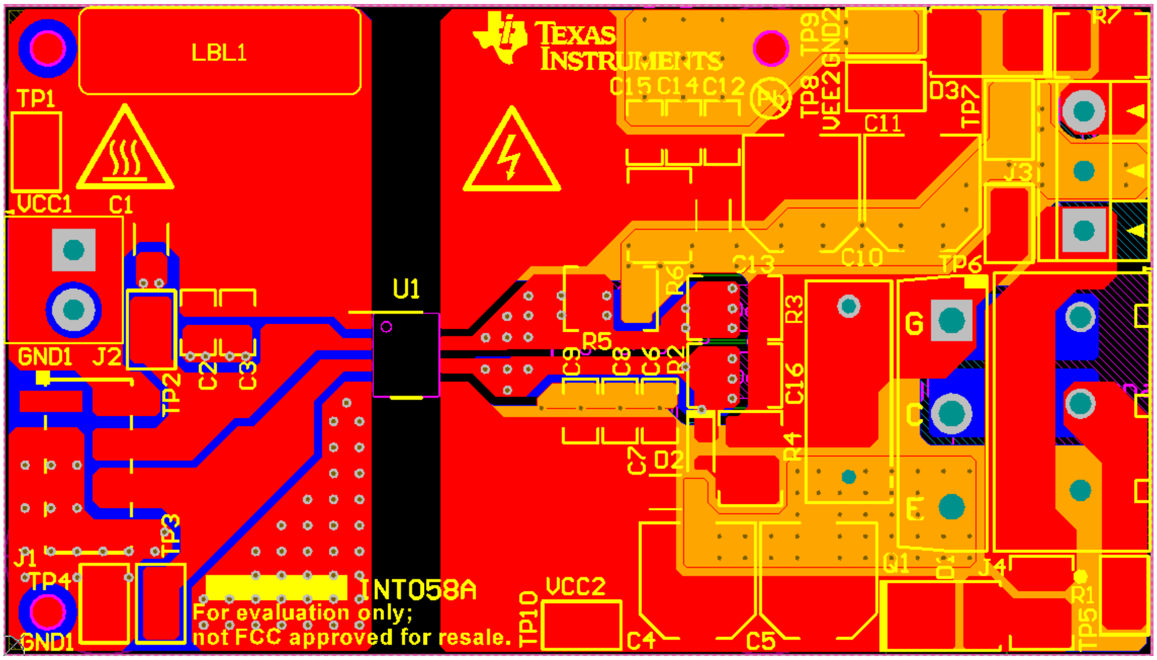
11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC53x0. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CC1} and GND1 pins and between the V_{CC2} and V_{EE2} pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC53x0 if the driving voltage is high, the load is heavy, or the switching frequency is high (for more information, see セクション 9.2.2.3). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - Increasing the PCB copper connecting to the V_{CC2} and V_{EE2} pins is recommended, with priority on maximizing the connection to V_{EE2}. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the V_{CC2} and V_{EE2} pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

11.2 Layout Example

図 11-1 shows a PCB layout example with the signals and key components labeled.



A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

図 11-1. Layout Example

図 11-2 and 図 11-3 show the top and bottom layer traces and copper.

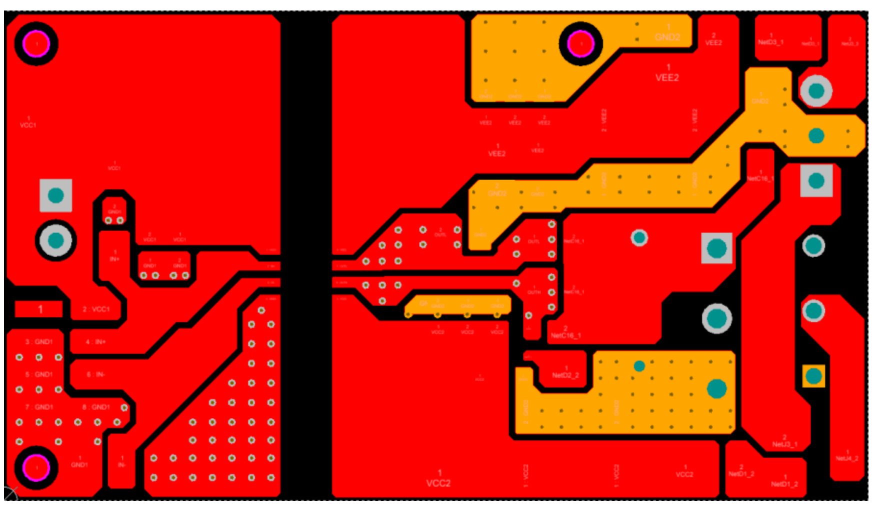


図 11-2. Top-Layer Traces and Copper

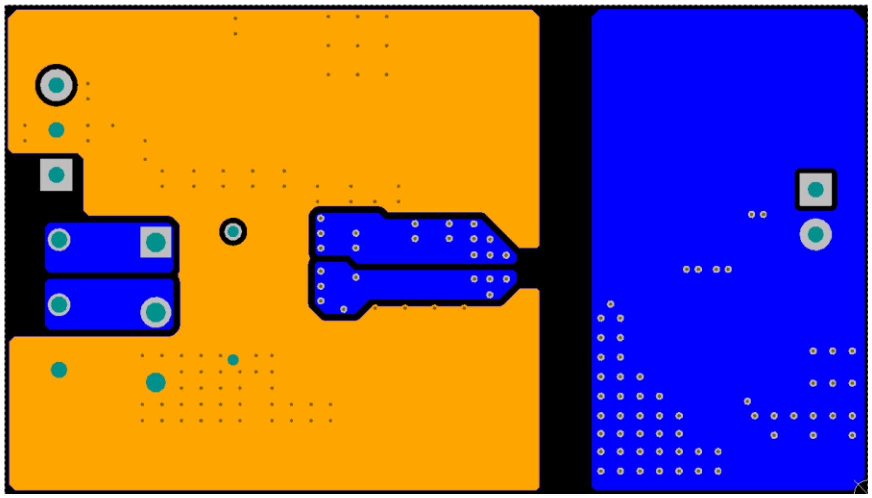
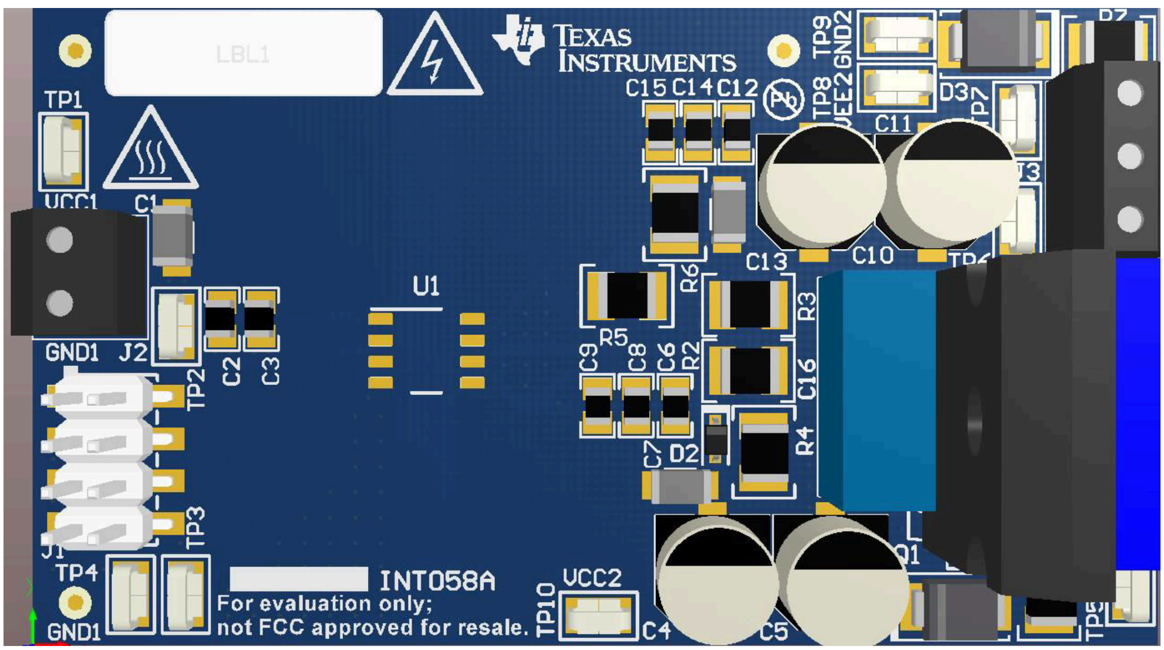


図 11-3. Bottom-Layer Traces and Copper (Flipped)

図 11-4 shows the 3D layout of the top view of the PCB.



A. The location of the PCB cutout between primary side and secondary sides ensures isolation performance.

図 11-4. 3-D PCB View

11.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

図 11-5 shows the recommended layer stack.

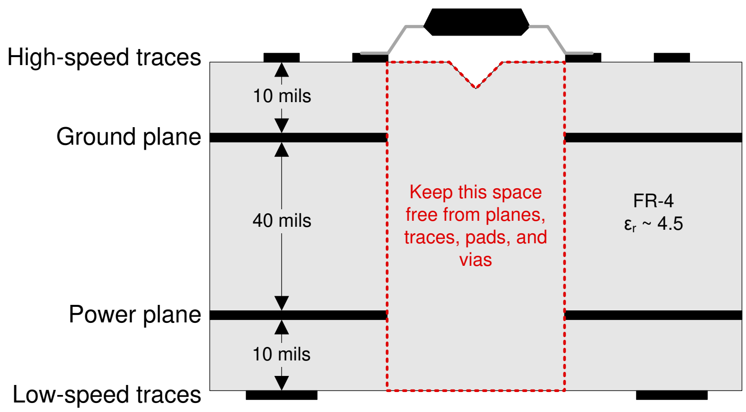


図 11-5. Recommended Layer Stack

12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *UCC5390ECDWV Isolated Gate Driver Evaluation Module* user's guide
- Texas Instruments, *UCC53x0xD Evaluation Module* user's guide

12.3 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20170718-E181974,

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 サポート・リソース

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12.8 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (February 2024) to Revision I (March 2024)	Page
• Changed Certification Planned to Certification number: 40047657 in Safety-Related Certifications For DWV Package section	10

Changes from Revision G (December 2023) to Revision H (February 2024)	Page
• Changed CTI and Material Group values in insulation specifications and added table note	8

Changes from Revision F (January 2019) to Revision G (December 2023)	Page
• Added UCC5350MC DWV package	3

Changes from Revision E (October 2018) to Revision F (January 2019)	Page
• 2 番目の項目から (UCC5390EC) を削除(現在 3 つの幅広デバイスがリリースされているので)	1
• 安全関連認証に DIN EN 61010-1 を追加	1
• 「安全関連の認定」の箇条書き項目全体にわたって「(予定)」を追加	1
• 「概要」の「ピン配置構成と駆動力のバリアント」とスイッチ タイプの情報を変更	1
• Changed creepage and clearance from 9 mm to 8.5 mm in Insulation Specifications and throughout datasheet	9
• Added VDE and CQC certification for D package and UL file number for DWV package	10
• Changed test condition for V_{OH}	11
• Changed a minor detail to the UCC53x0M figures	28
• Changed typical application circuit for E Version to include capacitors on negative bias	33

Changes from Revision D (May 2018) to Revision E (October 2018)	Page
• Changed UCC5310 DWV package from Preview to Final	3
• Changed UCC5320 DWV package from Preview to Final	3

Changes from Revision C (February 2018) to Revision D (May 2018)	Page
• UCC5390EC のマーケティング ステータスをプレビューから量産に変更	1

Changes from Revision B (August 2017) to Revision C (February 2018)	Page
• UCC5350SBD、UCC5320SCDWV、UCC5310MCDWV、UCC5390ECDWV デバイスをデータシートに追加	1
• E および M バージョンと DWV パッケージの情報を含むように「特長」、「アプリケーション」、「概要」、「機能ブロック図」を変更	1
• Added UCC5350SB to the pin configuration and function	4
• Added minimum storage temperature	6
• Changed from VDE V 0884-10 to VDE V 0884-11 in insulation specifications and safety-related certification table	8
• Changed safety limiting values	10
• Deleted test conditions for Supply Currents	11
• Added Typical Curves and Test Conditions to include UCC5390 and UCC5350 information	15
• Deleted device I/O figure	31

- Changed ESD figure 31
- Added UL online certification directory to the certification section.................... 44

Changes from Revision A (June 2017) to Revision B (August 2017) **Page**

- 動作時の周囲温度の最低値を –55℃から –40℃に変更.................... 1

Changes from Revision * (June 2017) to Revision A (June 2017) **Page**

- 将来の 10A デバイスにも利用可能な 17A をタイトルから削除....................1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5310MCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	5310M
UCC5310MCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310M
UCC5310MCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310M
UCC5310MCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5310MCDWV	Obsolete	Production	SOIC (DWV) | 8	-	-	Call TI	Call TI	-40 to 125	5310MC
UCC5310MCDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310MC
UCC5310MCDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310MC
UCC5310MCDWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5320ECD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	5320E
UCC5320ECDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320E
UCC5320ECDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320E
UCC5320ECDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5320SCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	5320S
UCC5320SCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320S
UCC5320SCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320S
UCC5320SCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5320SCDWV	Obsolete	Production	SOIC (DWV) | 8	-	-	Call TI	Call TI	-40 to 125	5320SC
UCC5320SCDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320SC
UCC5320SCDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320SC
UCC5320SCDWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5350MCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350M
UCC5350MCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350M
UCC5350MCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5350MCDWV	Obsolete	Production	SOIC (DWV) | 8	-	-	Call TI	Call TI	-40 to 125	5350MC
UCC5350MCDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350MC
UCC5350MCDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350MC
UCC5350MCDWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5350SBD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	5350SB
UCC5350SBDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350SB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5350SBDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350SB
UCC5350SBDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5390ECD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	53X0E
UCC5390ECDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0E
UCC5390ECDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0E
UCC5390ECDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5390ECDWV	Obsolete	Production	SOIC (DWV) | 8	-	-	Call TI	Call TI	-40 to 125	5390EC
UCC5390ECDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5390EC
UCC5390ECDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5390EC
UCC5390ECDWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5390SCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	53X0S
UCC5390SCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S
UCC5390SCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S
UCC5390SCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC5390SCDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S
UCC5390SCDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S
UCC5390SCDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC5350, UCC5390 :

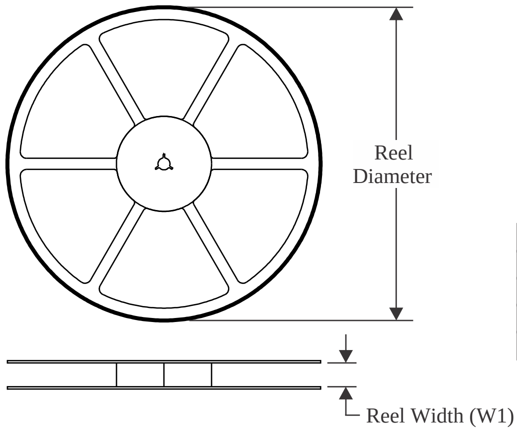
- Automotive : UCC5350-Q1, UCC5390-Q1

NOTE: Qualified Version Definitions:

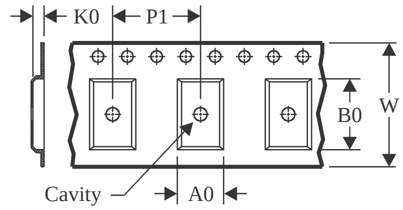
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

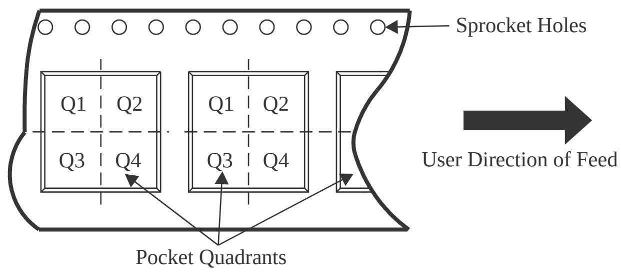


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

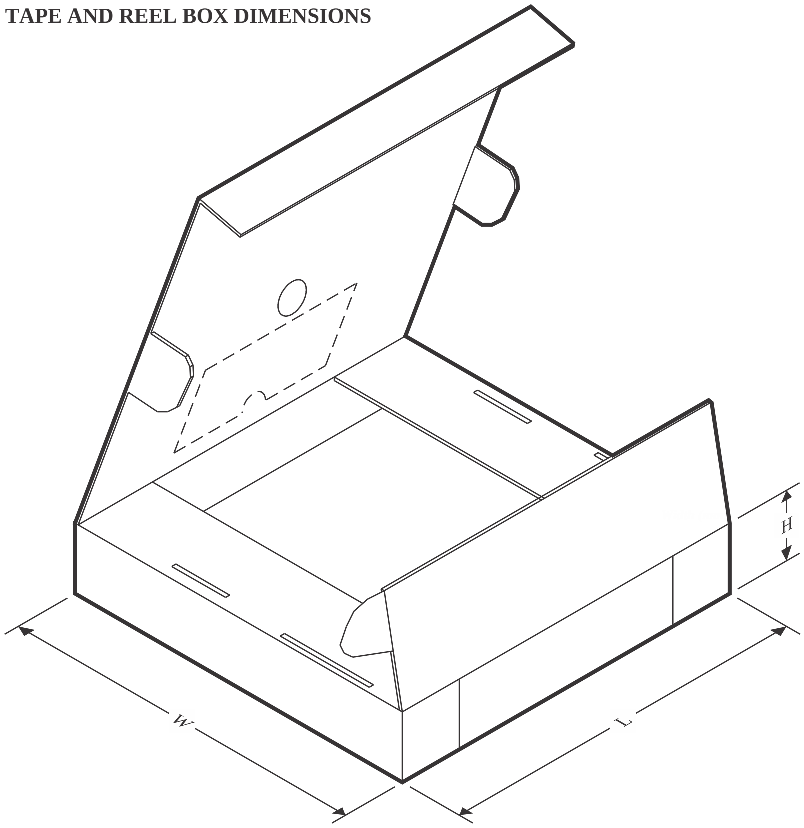
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

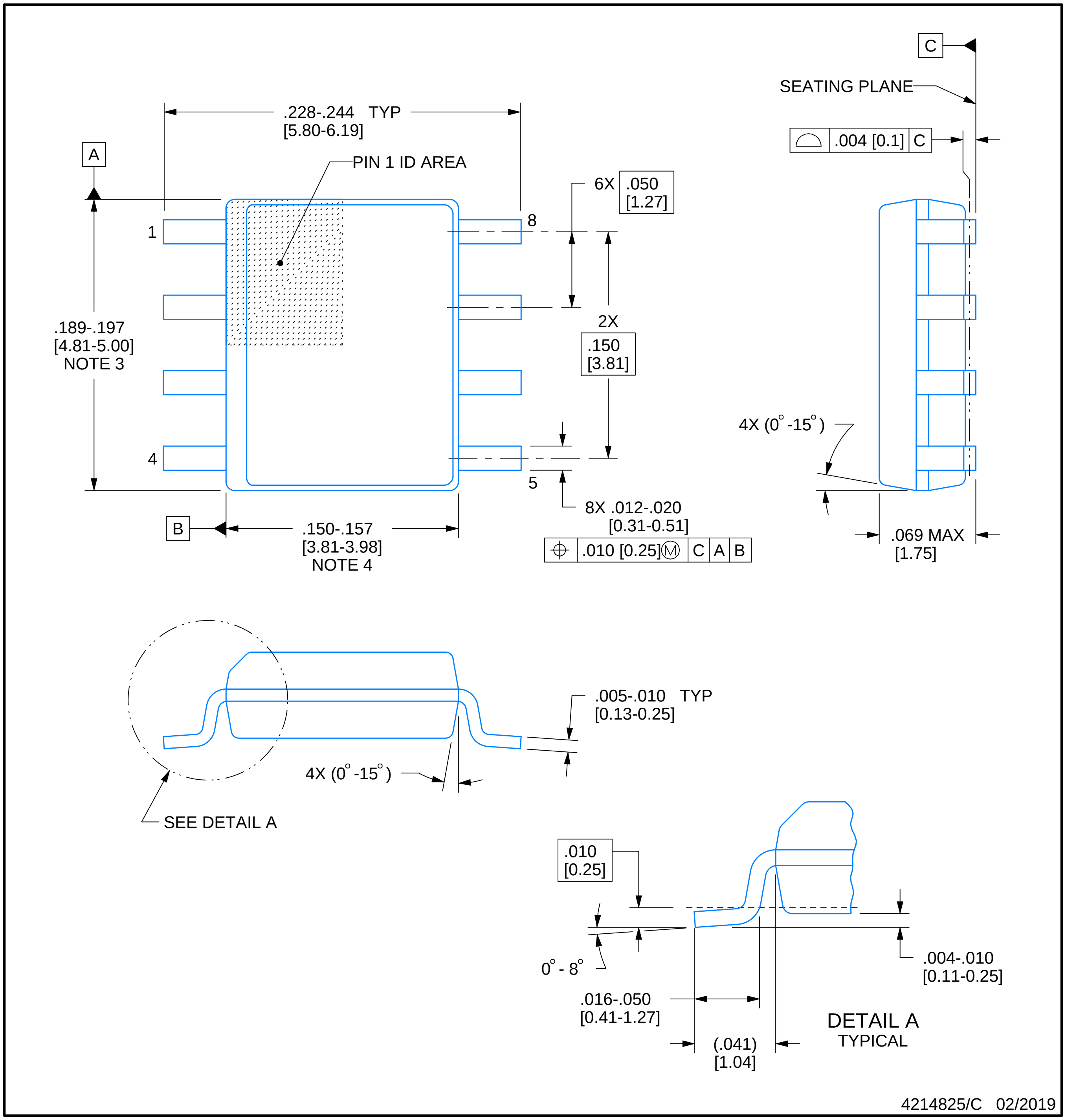
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5310MCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5310MCDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5320ECDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5320SCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5320SCDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5350MCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5350MCDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5350SBDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5390ECDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5390ECDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5390SCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5390SCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



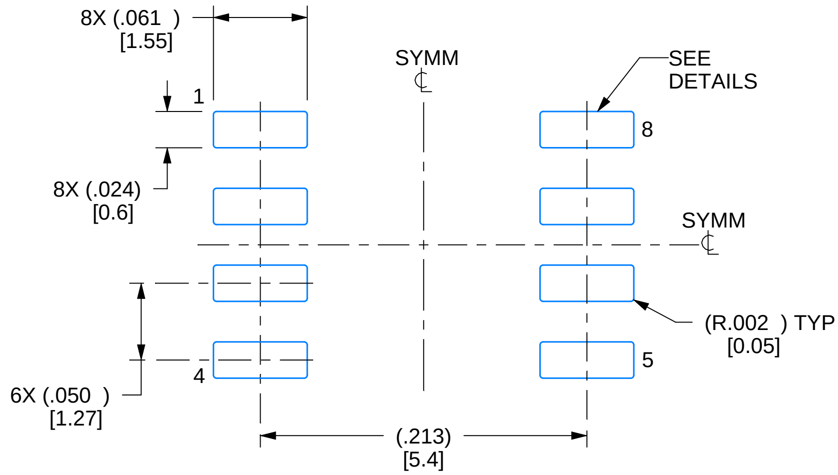
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5310MCDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC5310MCDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5320ECDR	SOIC	D	8	2500	350.0	350.0	43.0
UCC5320SCDR	SOIC	D	8	2500	350.0	350.0	43.0
UCC5320SCDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5350MCDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC5350MCDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5350SBDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC5390ECDR	SOIC	D	8	2500	350.0	350.0	43.0
UCC5390ECDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5390SCDR	SOIC	D	8	2500	350.0	350.0	43.0
UCC5390SCDRG4	SOIC	D	8	2500	350.0	350.0	43.0

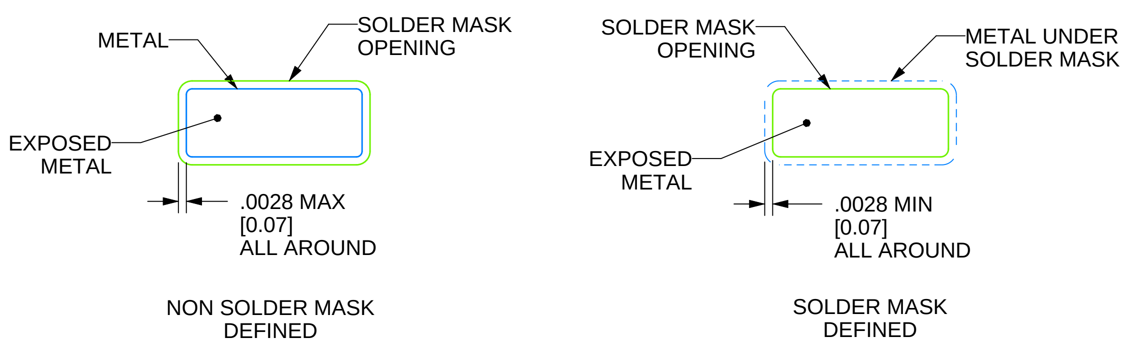


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

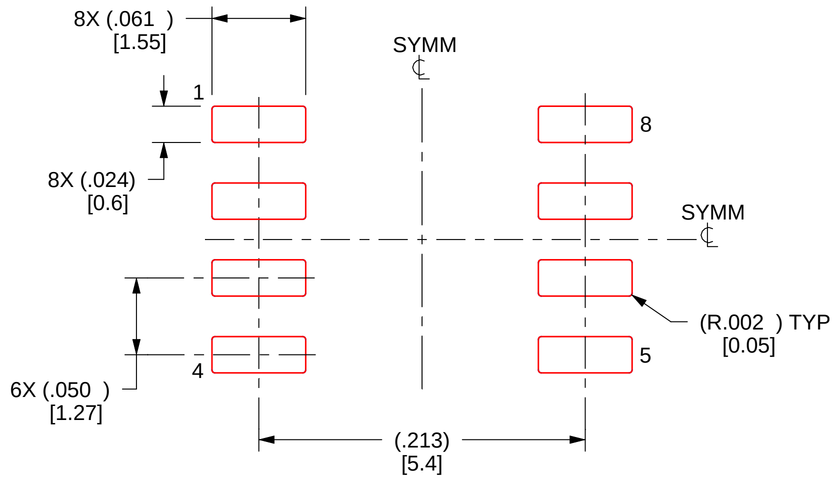


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

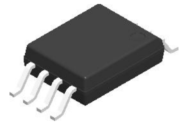


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

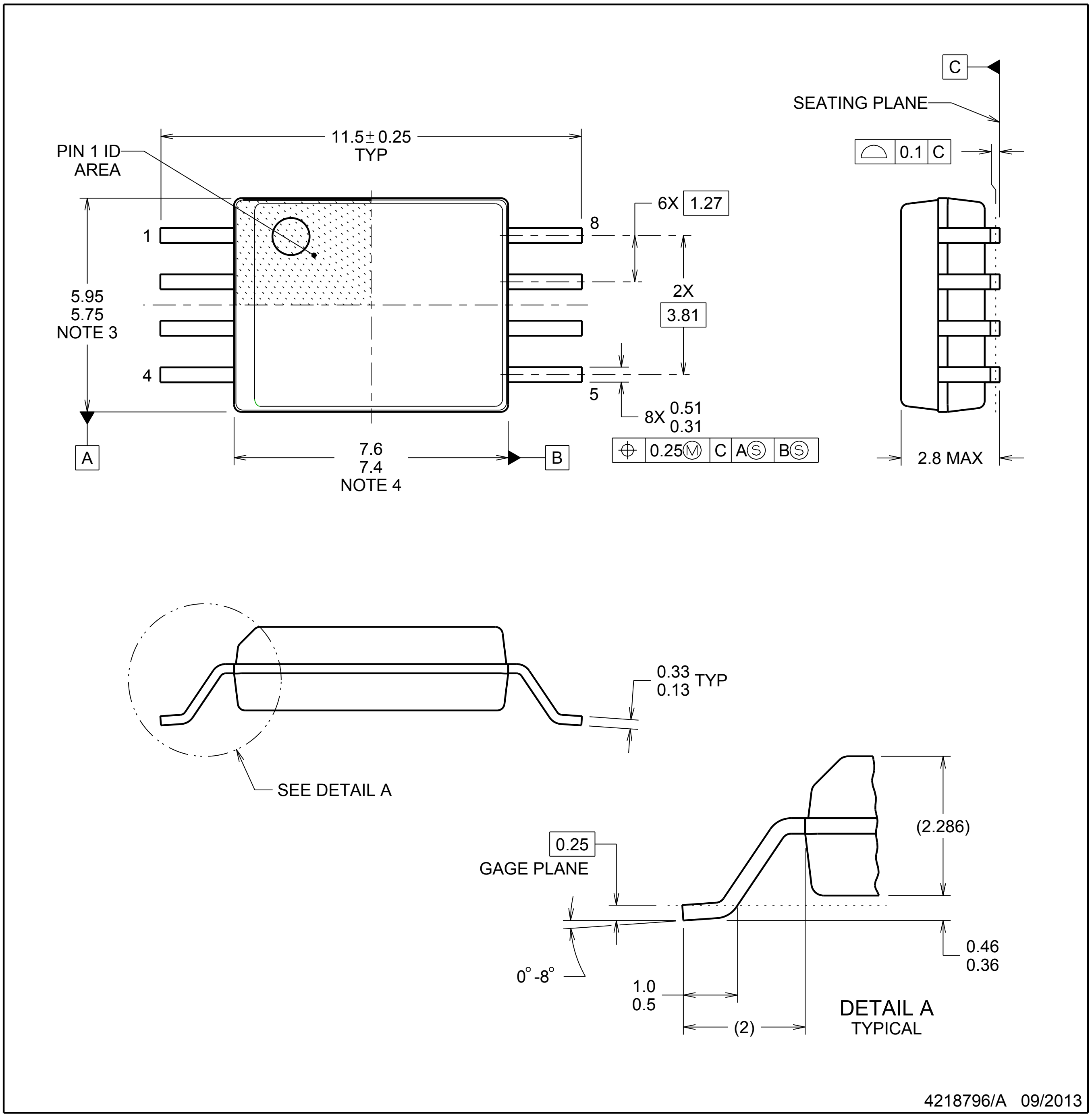
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DWV0008A

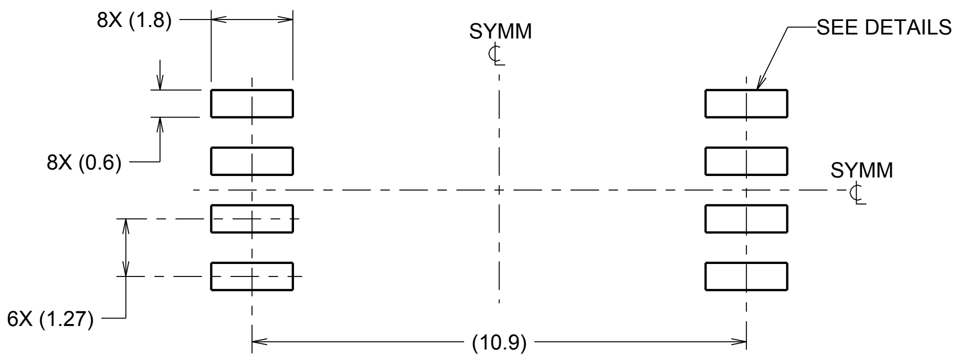
SOIC - 2.8 mm max height

SOIC

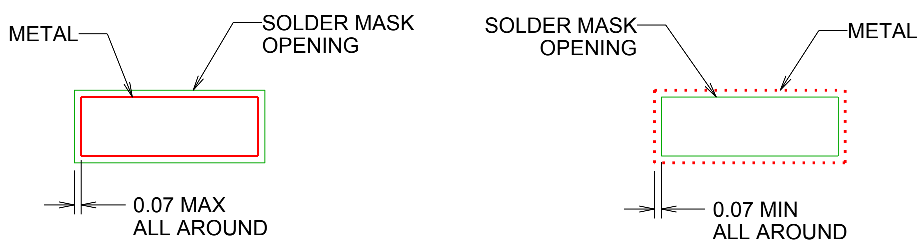


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



NON SOLDER MASK DEFINED

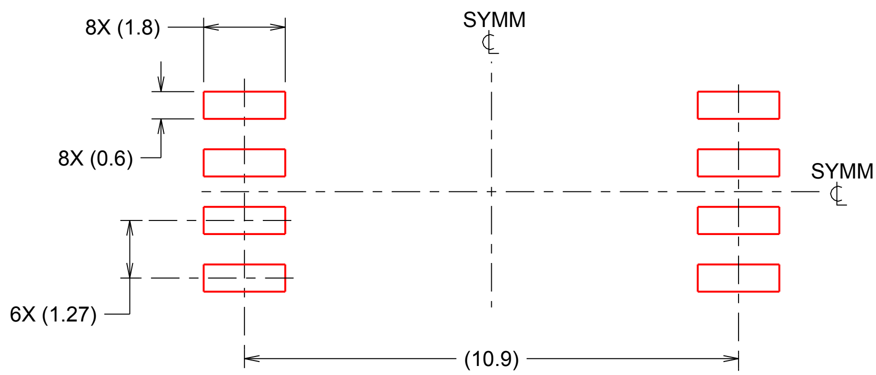
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.