

UCCx8C5x BiCMOS 低消費電力、電流モード PWM コントローラ Si および SiC MOSFET 用

1 特長

- Si および SiC の両方の MOSFET アプリケーションをサポートする低電圧誤動作防止オプション
- 30V の絶対最大定格電圧
- 最大 1MHz の固定周波数動作
- スタートアップ電流: 50 μ A (標準値)、75 μ A (最大値)
- 小さい動作電流: 1.3mA ($f_{OSC} = 52$ kHz 時)
- 高速な 35ns のサイクルごとの過電流制限
- ± 1 A のピーク駆動電流
- レール・ツー・レール出力
 - 25ns の立ち上がり時間
 - 20ns の立ち下がり時間
- $\pm 1\%$ 精度、2.5V の誤差増幅器基準電圧
- UCCx8C4x のピン互換およびドロップイン代替品
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能

2 アプリケーション

- 汎用シングルエンド DC/DC またはオフライン絶縁型電源コンバータ
- 太陽光発電用電力インバータ、モーター駆動、エネルギー貯蔵システム用の補助電源
- EV 充電ステーション向け絶縁型電源

3 概要

UCCx8C5x デバイス・ファミリは、各種アプリケーションの Si と SiC の両方の MOSFET を駆動できる高性能電流モード PWM コントローラです。UCCx8C5x ファミリは、UCCx8C4x に対して効率と信頼性を高めたバージョンです。

UCCx8C5x ファミリは、Si MOSFET を引き続きサポートするための既存の UVLO スレッショルド (UCCx8C50～55) に加えて、SiC MOSFET を確実に動作させることができる新しい UVLO スレッショルド (UCC28C56～59) を備えています。

VDD の絶対最大定格電圧は 20V から 30V に拡張されており、20V_{gs}、18V_{gs}、または 15V_{gs} の SiC MOSFET ゲートを最適に駆動すると共に、外部の LDO は不要となります。

デバイスの性能の向上

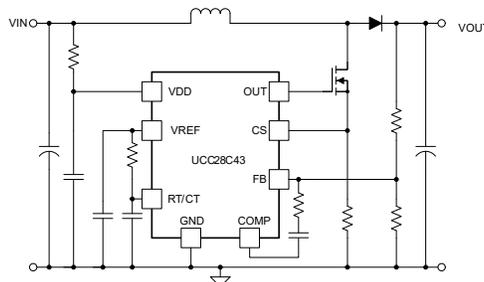
パラメータ	UCCx8C4x	UCCx8C5x
52kHz 時の消費電流	2.3mA	1.3mA
スタートアップ電流 (最大値)	100 μ A	75 μ A
VDD 絶対最大定格	20V	30V
基準電圧精度	$\pm 2\%$	$\pm 1\%$
Si FET の UVLO および D _{MAX}	6 つのオプション	6 つのオプション
SiC FET の UVLO および D _{MAX}	なし	6 つのオプション
最小パッケージ・オプション	VSSOP (8)	VSSOP (8)

UCCx8C5x ファミリは、8 ピン VSSOP (DGK) および 8 ピン SOIC (D) パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
UCC28C50, UCC28C51 UCC28C52, UCC28C53, UCC28C54, UCC28C55, UCC38C50, UCC38C51 UCC38C52, UCC38C53 UCC38C54, UCC38C55	SOIC (8) VSSOP (8)	3.91mm × 4.90mm 3.00mm × 3.00mm
UCC28C56H, UCC28C56L UCC28C57H, UCC28C57L, UCC28C58, UCC28C59	SOIC (8)	3.91mm × 4.90mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略化されたアプリケーション



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2023) to Revision C (March 2023)	Page
• UCC28C56L、UCC38C53、UCC38C55 デバイスの初版リリース.....	1

Changes from Revision A (October 2022) to Revision B (February 2023)	Page
• UCC28C50、UCC28C51、UCC28C52、UCC28C53、UCC28C54、UCC28C55、UCC28C57H、UCC28C57L、UCC38C50、UCC38C51、UCC38C52、UCC38C54 デバイスの初版リリース.....	1
• Corrected Figure 8-5 Oscillator Synchronization Circuit	21

5 Device Comparison Table

UVLO			Junction Temperature (T _J) (°C)	Maximum duty cycle
Turn on at 14.5 V Turn off at 9 V for off-line applications	Turn on at 8.4 V Turn off at 7.6 V for dc/dc applications	Turn on at 7 V Turn off at 6.6 V for battery applications		
UCC28C52	UCC28C53	UCC28C50	–40 to 125	100%
UCC38C52	UCC38C53	UCC38C50	0 to 85	
UCC28C54	UCC28C55	UCC28C51	–40 to 125	50%
UCC38C54	UCC38C55	UCC38C51	0 to 85	

UVLO			Junction Temperature (T _J) (°C)	Maximum duty cycle
Turn on at 18.8 V Turn off at 15.5 V Suitable for HV applications using GEN-I SiC MOSFET	Turn on at 18.8 V Turn off at 14.5 V Suitable for HV applications using GEN-II SiC MOSFET	Turn on at 16 V Turn off at 12.5 V Suitable for HV applications using GEN-III SiC MOSFET		
UCC28C56H	UCC28C56L	UCC28C58	–40 to 125	100%
UCC28C57H	UCC28C57L	UCC28C59	–40 to 125	50%

6 Pin Configuration and Functions

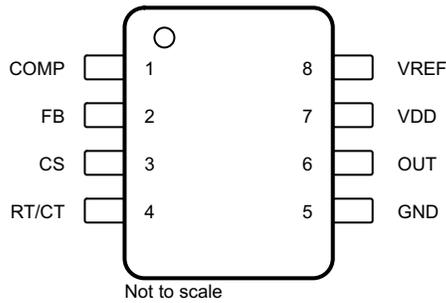


图 6-1. D Package 8-Pin SOIC (Top View)

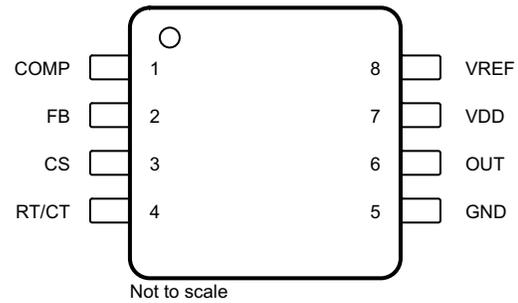


图 6-2. DGK Package, 8-Pin VSSOP (Top View)

表 6-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
COMP	1	O	This pin provides the output of the error amplifier for compensation. In addition, the COMP pin is frequently used as a control port, by utilizing a secondary-side error amplifier to send an error signal across the secondary-primary isolation boundary through an opto-isolator. The error amplifier is internally current limited so the user can command zero duty cycle by externally forcing COMP to GND.
CS	3	I	Primary-side current sense pin. The current sense pin is the noninverting input to the PWM comparator. Connect to current sensing resistor. This signal is compared to a signal proportional to the error amplifier output voltage. The PWM uses this to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration.
FB	2	I	This pin is the inverting input to the error amplifier. FB is used to control the power converter voltage-feedback loop for stability. The noninverting input to the error amplifier is internally trimmed to $2.5\text{ V} \pm 1\%$.
GND	5	—	Ground return pin for the output driver stage and the logic level controller section.
OUT	6	O	The output of the on-chip drive stage. OUT is intended to directly drive a MOSFET. The OUT pin in the UCCx8C50, UCCx8C52, UCCx8C53, UCC28C56H/L and UCC28C58 is the same frequency as the oscillator, and can operate near 100% duty cycle. In the UCCx8C51, UCCx8C54, and UCCx8C55, UCC28C57H/L and UCC28C59, the frequency of OUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle to $< 50\%$. Peak currents of up to 1 A are sourced and sunk by this pin. OUT is actively held low when VDD is below the turn-on threshold.
RT/CT	4	I/O	Fixed frequency oscillator set point. Connect timing resistor (R_{RT}) to VREF and timing capacitor (C_{CT}) to GND from this pin to set the switching frequency. For best performance, keep the timing capacitor lead to the device GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions. The switching frequency (f_{SW}) of the UCCx8C50, UCCx8C52, UCCx8C53, UCC28C56H/L and UCC28C58 gate drive is equal to f_{OSC} ; the switching frequency of the UCCx8C51, UCCx8C54, and UCCx8C55, UCC28C57H/L and UCC28C59 is equal to half of the f_{OSC} .
VDD	7	I	Analog controller bias input that provides power to the device. Total VDD current is the sum of the quiescent VDD current and the average OUT current. A bypass capacitor, typically $0.1\ \mu\text{F}$, connected directly to GND with minimal trace length, is required on this pin. Additional capacitance at least 10 times greater than the gate capacitance of the main switching FET used in the design and at least 10 times greater than the capacitance on the VREF pin used in the design are also required on VDD.
VREF	8	O	5-V reference voltage. VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor. It is important for reference stability that VREF is bypassed to GND with a ceramic capacitor connected as close to the pin as possible. A minimum value of $0.1\ \mu\text{F}$ ceramic is required. Additional VREF bypassing is required for external loads on VREF. No external voltage higher than specified VREF is allowed to superimposed to VREF pin since VREF is an output.

(1) I = input, O = output, G = ground

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
Input voltage	VDD		30	V
Input current	IVDD		30	mA
Output drive current (peak)			±1	A
Output energy (capacitive load), E _{OUT}			5	μJ
Analog input voltage	COMP, CS, FB, RT/CT	-0.3	6.3	V
Output driver voltage	OUT	-0.3	30	
Reference voltage	VREF		7	
Error amplifier output sink current	COMP		10	mA
Total power dissipation at T _A = 25°C	D package		72.3	°C/W
	DGK package		98.1	
Lead temperature (soldering, 10 s), T _{LEAD}			300	°C
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND pin. Currents are positive into and negative out of the specified terminals.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{VDD}	Input voltage		28	V
V _{OUT}	Output driver voltage		28	V
I _{OUT}	Average output driver current ⁽¹⁾		200	mA
I _{OUT(VREF)}	Reference output current ⁽¹⁾		-20	mA
T _J	Operating junction temperature ⁽¹⁾	UCC28C5x	-40	125
		UCC38C5x	0	85

- (1) TI recommends against operating the device under conditions beyond those specified in this table for extended periods of time.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	UCC28C5x, UCC38C5x		UNIT	
	D (SOIC)	DGK (VSSOP)		
	8 PINS	8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	128.9	176.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	71.7	67.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	72.3	98.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	23.4	11.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	71.5	91.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

$V_{VDD} = 20V$ for UCC28C56H/L, UCC28C57H/L, and UCC28C58/9, $V_{VDD} = 15V$ for all other device options, $R_{RT} = 10\text{ k}\Omega$, $C_{CT} = 3.3\text{ nF}$, $C_{VDD} = 0.1\text{ }\mu\text{F}$ and no load on the outputs, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ for the UCC28C5x, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$, for the UCC38C5x (unless otherwise noted).

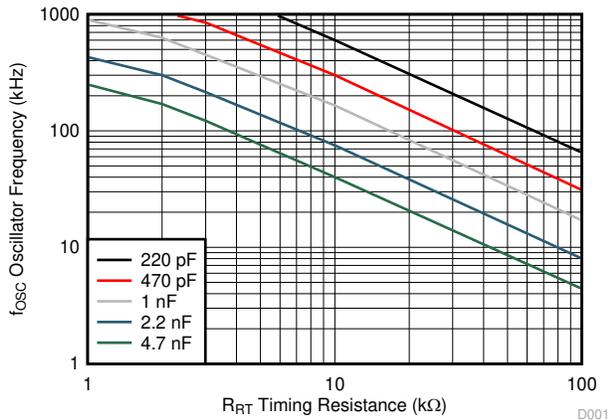
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{VREF}	VREF voltage, initial accuracy	$T_J = 25^\circ\text{C}$, $I_{OUT} = 1\text{ mA}$	4.95	5	5.05	V
	Line regulation	$12\text{ V} \leq V_{VDD} \leq 25\text{ V}$		0.2	20	mV
	Load regulation	1 mA to 20 mA		3	25	mV
	Temperature stability ⁽²⁾			0.2	0.4	mV/°C
	Total output variation ⁽²⁾		4.85		5.15	V
	VREF noise voltage ⁽²⁾	10 Hz to 10 kHz, $T_J = 25^\circ\text{C}$		50		μV
	Long term stability ⁽²⁾	1000 hours, $T_J = 125^\circ\text{C}$		5	25	mV
I_{VREF}	Output short circuit (source current)		30	45	55	mA
OSCILLATOR						
f_{OSC}	Initial accuracy ⁽³⁾	$T_J = 25^\circ\text{C}$	50.5	53	55	kHz
	Voltage stability	$12\text{ V} \leq V_{VDD} \leq 25\text{ V}$		0.2%	1%	
	Temperature stability ⁽²⁾	$T_{J(MIN)}$ to $T_{J(MAX)}$		1%	2.5%	
	Amplitude	RT/CT pin peak-to-peak voltage		1.9		V
	Discharge current ⁽⁴⁾	$T_J = 25^\circ\text{C}$, $V_{RT/CT} = 2\text{ V}$	7.7	8.4	9	mA
		$V_{RT/CT} = 2\text{ V}$	7.2	8.4	9.5	
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage, initial accuracy	$V_{COMP} = 2.5\text{ V}$, $T_J = 25^\circ\text{C}$	2.475	2.5	2.525	V
	Feedback input voltage, total variation	$V_{COMP} = 2.5\text{ V}$	2.45	2.5	2.55	V
I_{FB}	Input bias current (source current)	$V_{FB} = 5\text{ V}$		0.1	2	μA
A_{VOL}	Open-loop voltage gain	$2\text{ V} \leq V_{OUT} \leq 4\text{ V}$	65	90		dB
	Unity gain bandwidth ⁽²⁾		1	1.5		MHz
PSRR	Power supply rejection ratio	$12\text{ V} \leq V_{VDD} \leq 25\text{ V}$	60			dB
	Output sink current	$V_{FB} = 2.7\text{ V}$, $V_{COMP} = 1.1\text{ V}$	2	14		mA
	Output source current	$V_{FB} = 2.3\text{ V}$, $V_{COMP} = 5\text{ V}$	0.5	1		mA
VOH	High-level COMP voltage	$V_{FB} = 2.7\text{ V}$, $R_{COMP} = 15\text{ k}\Omega$ COMP to GND		$V_{REF} - 0.2$		V
VOL	Low-level COMP voltage	$V_{FB} = 2.7\text{ V}$, $R_{COMP} = 15\text{ k}\Omega$ COMP to VREF		0.1	1.1	V
CURRENT SENSE						
A_{CS}	Gain ^{(5) (1)}		2.85	3	3.15	V/V
V_{CS}	Maximum input signal	$V_{FB} < 2.4\text{ V}$	0.9	1	1.1	V
PSRR	Power supply rejection ratio ^{(2) (5)}	$12\text{ V} \leq V_{VDD} \leq 25\text{ V}$		70		dB
I_{CS}	Input bias current (source current)			0.1	2	μA
t_D	CS to output delay			35	70	ns
	COMP to CS offset	$V_{CS} = 0\text{ V}$		1.15		V
OUTPUT						
$V_{OUT(low)}$	$R_{DS(on)}$ pulldown	$I_{SINK} = 200\text{ mA}$		5.5	15	Ω
$V_{OUT(high)}$	$R_{DS(on)}$ pullup	$I_{SOURCE} = 200\text{ mA}$		10	25	Ω
t_{RISE}	Rise time	$T_J = 25^\circ\text{C}$, $C_{OUT} = 1\text{ nF}$		25	50	ns
t_{FALL}	Fall time	$T_J = 25^\circ\text{C}$, $C_{OUT} = 1\text{ nF}$		20	40	ns
UNDERVOLTAGE LOCKOUT						

$V_{VDD} = 20V$ for UCC28C56H/L, UCC28C57H/L, and UCC28C58/9, $V_{VDD} = 15V$ for all other device options, $R_{RT} = 10\text{ k}\Omega$, $C_{CT} = 3.3\text{ nF}$, $C_{VDD} = 0.1\text{ }\mu\text{F}$ and no load on the outputs, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ for the UCC28C5x, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$, for the UCC38C5x (unless otherwise noted).

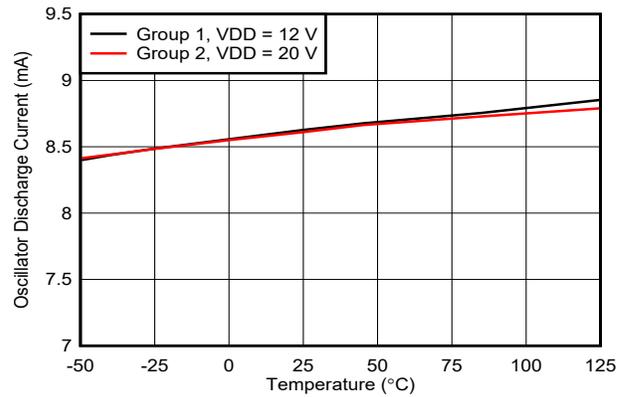
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD _{ON}	Start threshold ⁽⁶⁾	UCCx8C52, UCCx8C54	13.5	14.5	15.5	V
		UCCx8C53, UCCx8C55	7.8	8.4	9	
		UCCx8C50, UCCx8C51	6.5	7	7.5	
		UCC28C56H, UCC28C57H	17.6	18.8	20	
		UCC28C56L, UCC28C57L	17.6	18.8	20	
		UCC28C58, UCC28C59	14.8	16	17.2	
VDD _{OFF}	Minimum operating voltage ⁽⁶⁾	UCCx8C52, UCCx8C54	8	9	10	V
		UCCx8C53, UCCx8C55	7	7.6	8.2	
		UCCx8C50, UCCx8C51	6.1	6.6	7.1	
		UCC28C56H, UCC28C57H	15	15.5	16	
		UCC28C56L, UCC28C57L	13.95	14.5	15	
		UCC28C58, UCC28C59	12	12.5	13	
VDD _{Hyst}	VDD _{ON} - VDD _{OFF}	UCCx8C52, UCCx8C54	5.4	5.5		V
		UCCx8C53, UCCx8C55	0.8	0.9		
		UCCx8C50, UCCx8C51	0.4	0.5		
		UCC28C56H, UCC28C57H	2.6	3.3		
		UCC28C56L, UCC28C57L	3.65	4.3		
		UCC28C58, UCC28C59	2.8	3.5		
PWM						
D _{MAX}	Maximum duty cycle	UCCx8C52, UCCx8C53, UCCx8C50, V _{FB} < 2.4 V	94%	96%		
		UCC28C56H, UCC28C56L, UCC28C58, V _{FB} < 2.4 V	94%	96%		
		UCCx8C54, UCCx8C55, UCCx8C51, V _{FB} < 2.4 V	47%	48%		
		UCC28C57H, UCC28C57L, UCC28C59, V _{FB} < 2.4 V	47%	48%		
D _{MIN}	Minimum duty cycle	V _{FB} > 2.6 V			0%	
CURRENT SUPPLY						
I _{START-UP}	Start-up current	V _{VDD} = VDD _{ON} - 0.5 V		50	75	μA
I _{VDD}	Operating supply current	V _{FB} = V _{CS} = 0 V		1.3	2	mA

- (1) For UCC28C56H/L, UCC28C57H/L and UCC28C58/9 adjust V_{VDD} to a value above the start threshold before setting it to 20 V. For all other device options, adjust V_{VDD} to a value above the start threshold before setting it to 15.5 V
- (2) Specified by design. Not production tested.
- (3) Output frequencies of the UCCx8C51, UCCx8C54, and the UCCx8C55, UCC28C57H/L and the UCC28C59 are half the oscillator frequency.
- (4) Oscillator discharge current is measured with $R_{RT} = 10\text{ k}\Omega$ to VREF.
- (5) Parameter measured at trip point of latch with $V_{FB} = 0\text{ V}$. Gain is defined as $A_{CS} = \Delta V_{COMP} / \Delta V_{CS}$, $0\text{ V} \leq V_{CS} \leq 900\text{ mV}$.
- (6) VDD_{ON}, VDD_{OFF} and VREF are tracking each other in the same direction. (Minimum VDD_{OFF} is due to minimum VDD_{ON}.)

7.6 Typical Characteristics

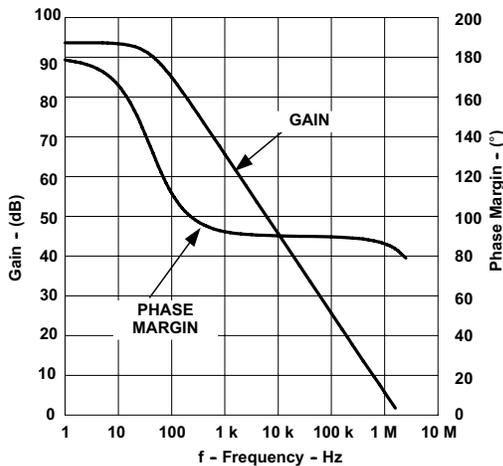


7-1. Oscillator Frequency vs Timing Resistance and Capacitance

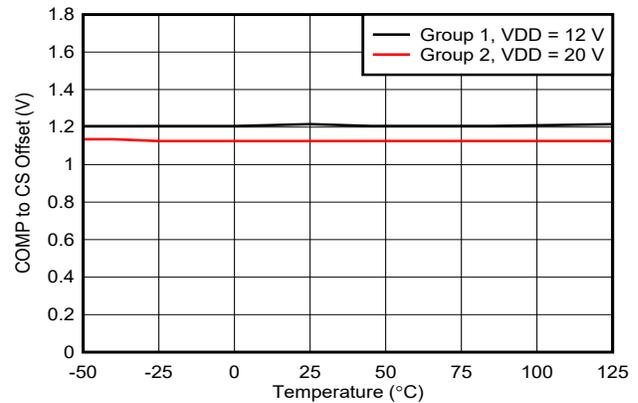


Group 1: UCCx8C50 to UCCx8C55
Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-2. Oscillator Discharge Current vs Temperature



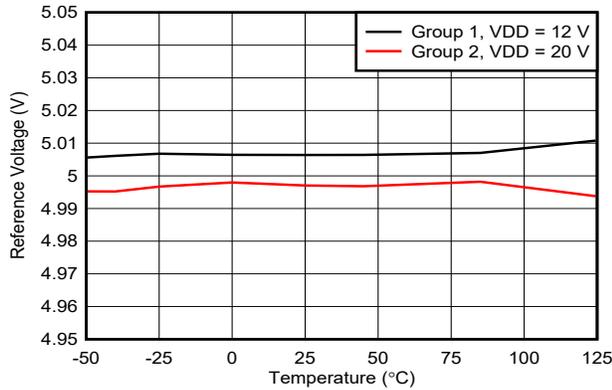
7-3. Error Amplifier Frequency Response



$V_{CS} = 0\text{ V}$

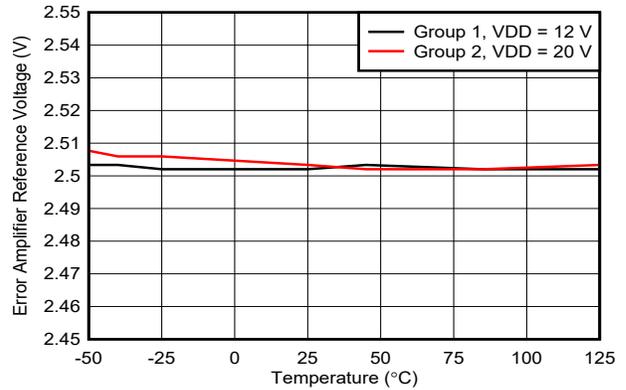
Group 1: UCCx8C50 to UCCx8C55
Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-4. COMP to CS Offset Voltage vs Temperature



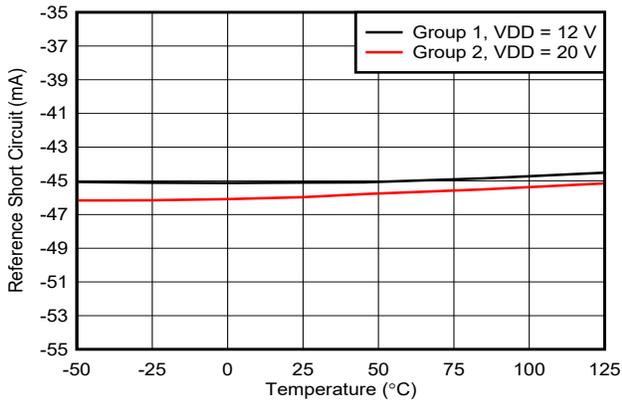
Group 1: UCCx8C50 to UCCx8C55
 Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-5. Reference Voltage vs Temperature



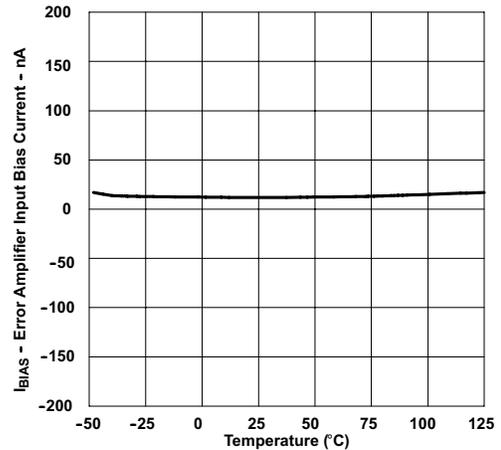
Group 1: UCCx8C50 to UCCx8C55
 Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-6. Error Amplifier Reference Voltage vs Temperature

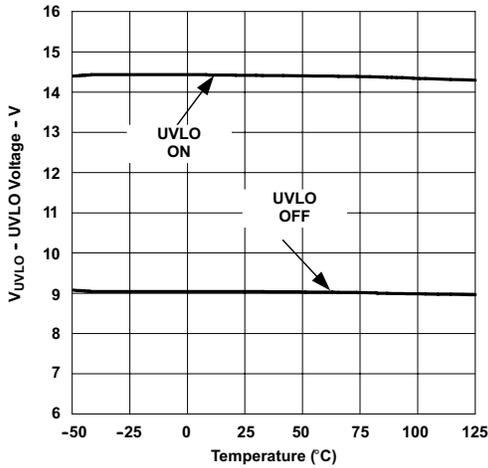


Group 1: UCCx8C50 to UCCx8C55
 Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-7. Reference Short-Circuit Current vs Temperature

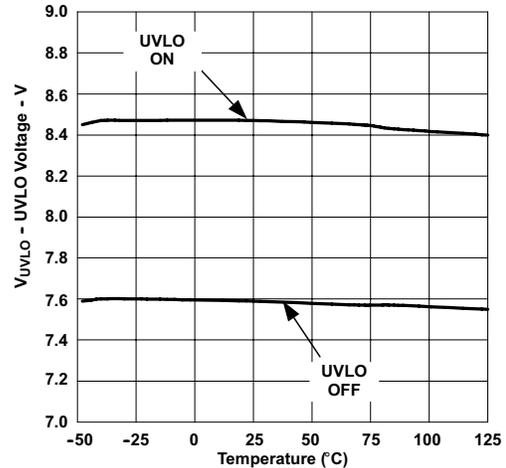


7-8. Error Amplifier Input Bias Current vs Temperature



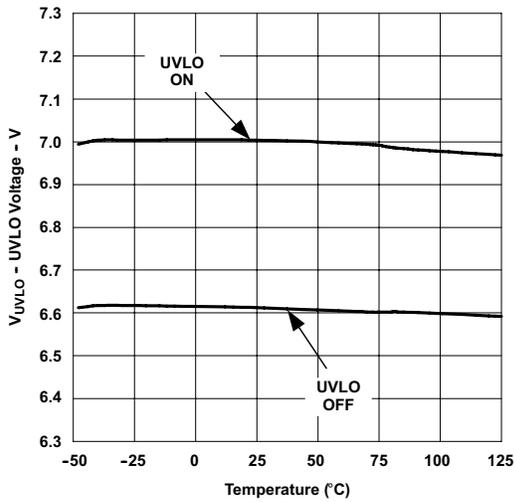
UCCx8C52 and UCCx8C54

7-9. Undervoltage Lockout vs Temperature



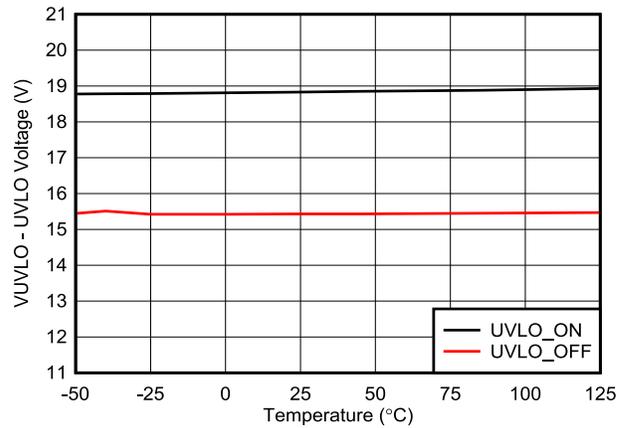
UCCx8C53 and UCCx8C55

7-10. Undervoltage Lockout vs Temperature



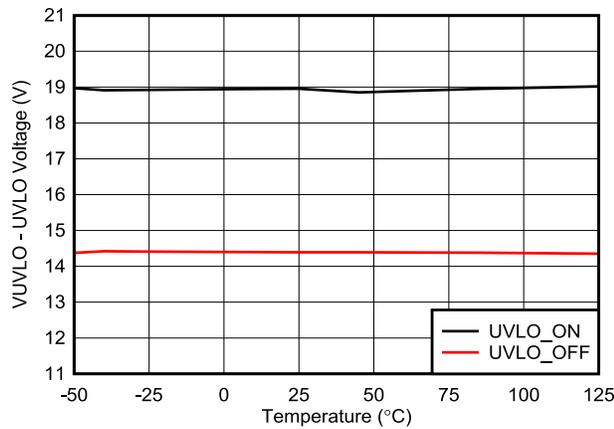
UCCx8C50 and UCCx8C51

7-11. Undervoltage Lockout vs Temperature



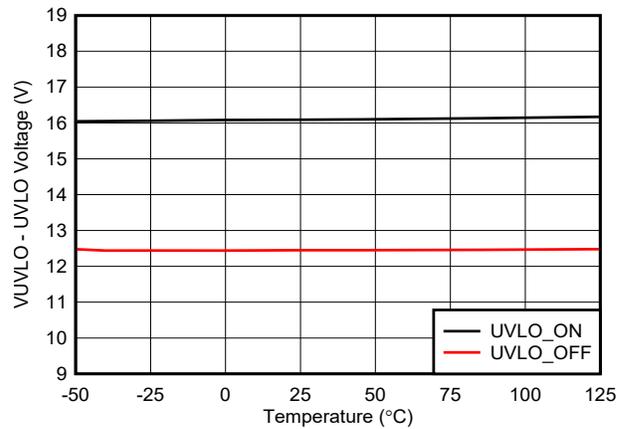
UCC28C56H and UCC28C57H

7-12. Undervoltage Lockout vs Temperature



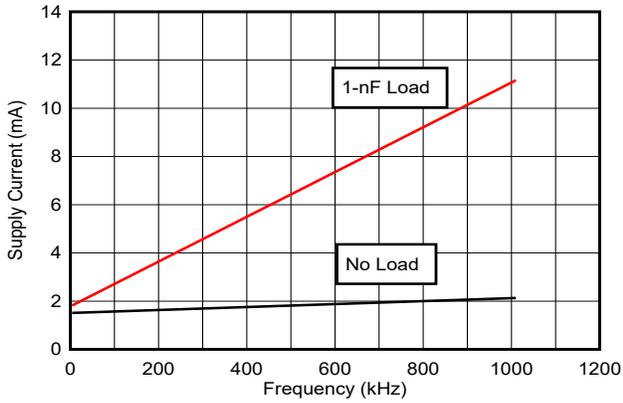
UCC28C56L and UCC28C57L

7-13. Undervoltage Lockout vs Temperature

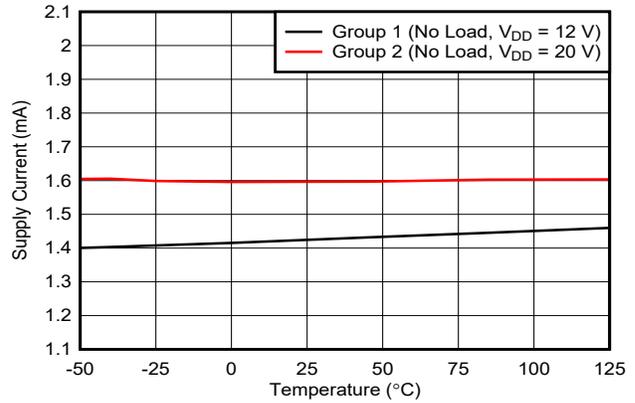


UCC28C58 and UCC28C59

7-14. Undervoltage Lockout vs Temperature

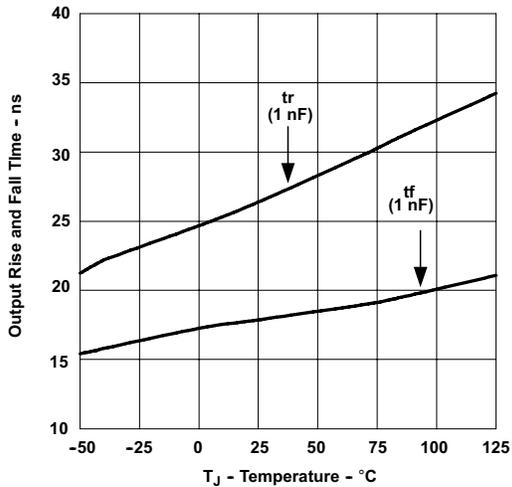


7-15. Supply Current vs Oscillator Frequency

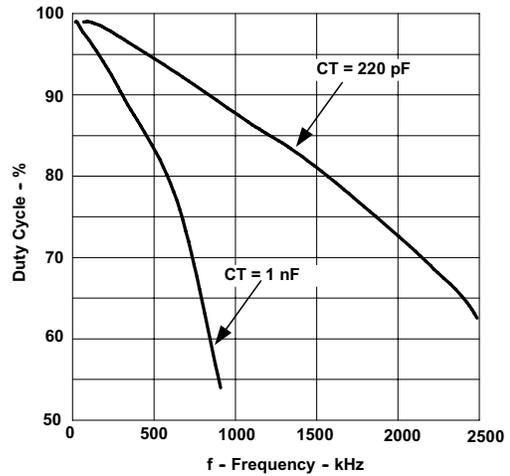


Group 1: UCCx8C50 to UCCx8C55
Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

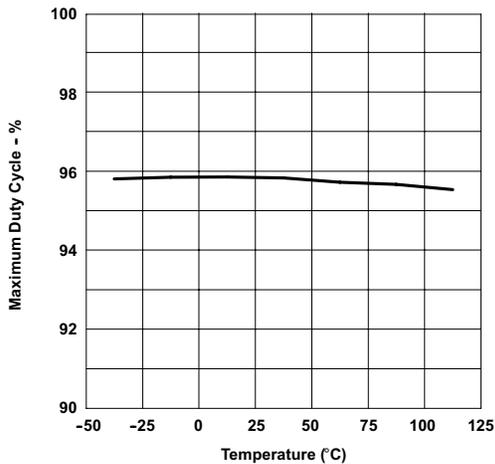
7-16. Supply Current vs Temperature



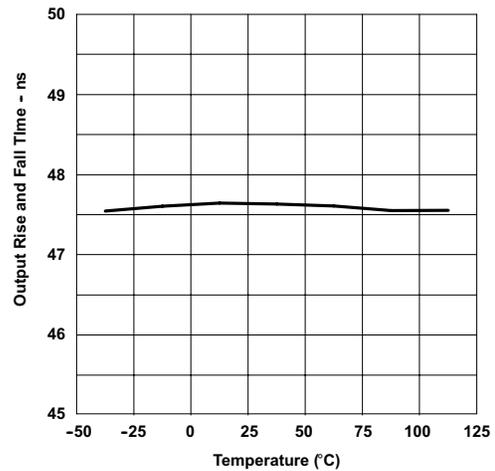
7-17. Output Rise Time and Fall Time vs Temperature



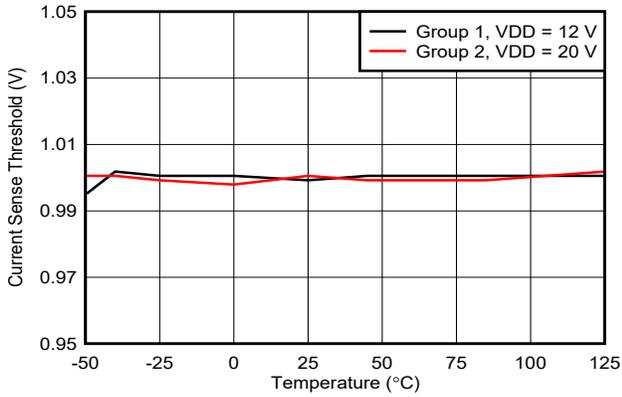
7-18. Maximum Duty Cycle vs Oscillator Frequency



7-19. Maximum Duty Cycle vs Temperature

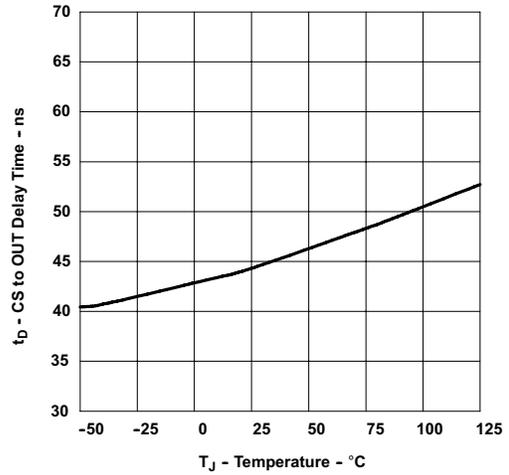


7-20. Maximum Duty Cycle vs Temperature



Group 1: UCCx8C50 to UCCx8C55
 Group 2: UCC28C56H/L, UCC28C57H/L, and UCC28C58/9

7-21. Current Sense Threshold Voltage vs Temperature



7-22. Current Sense to Output Delay Time vs Temperature

8 Detailed Description

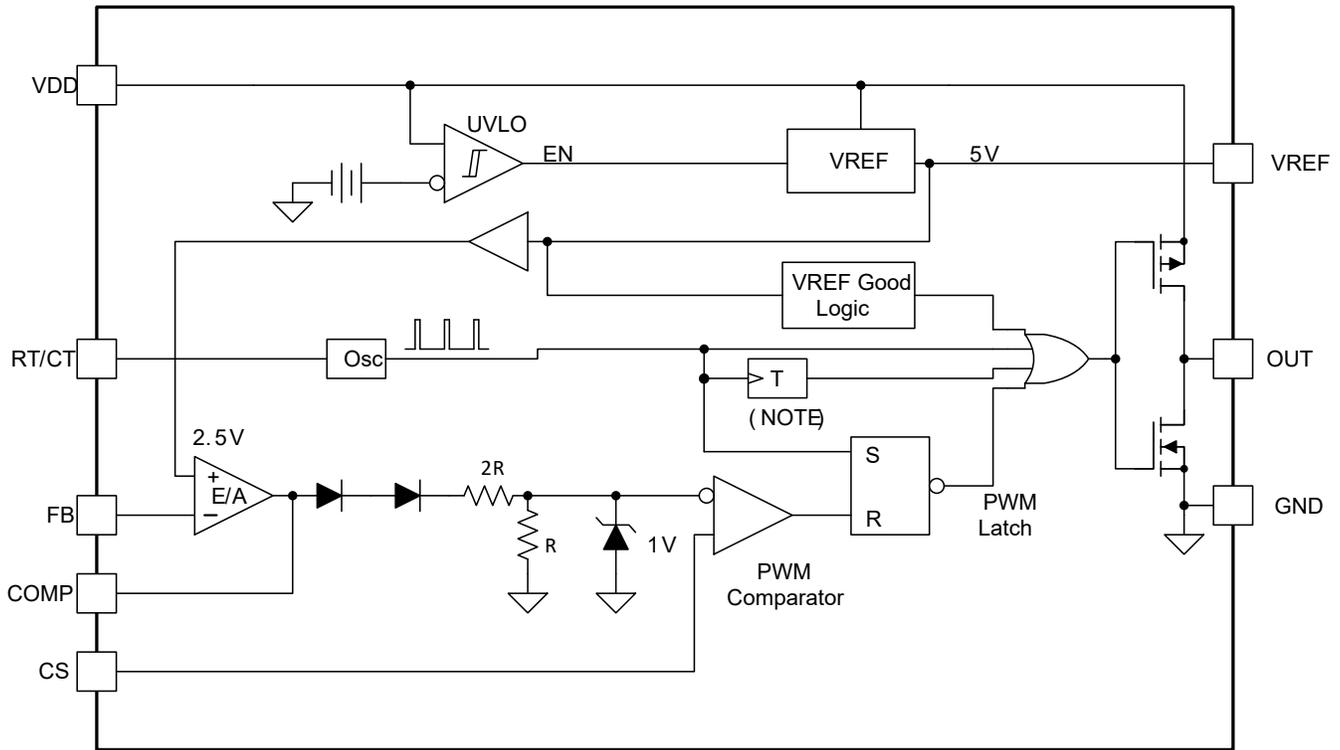
8.1 Overview

The UCCx8C5x series of control integrated circuits provide the features necessary to implement AC-DC or DC-to-DC fixed-frequency current-mode control schemes with a minimum number of external components. Protection circuitry includes undervoltage lockout (UVLO) and current limiting. Internally implemented circuits include a start-up current of less than 75 μ A, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and an output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the OFF state. The oscillator contains a trimmed discharge current that enables accurate programming of the maximum duty cycle and dead time limit, making this device suitable for high-speed applications.

Major differences between members of this series are the UVLO thresholds, acceptable ambient temperature range, maximum duty cycle and frequency. Typical UVLO thresholds of 14.5 V (ON) and 9 V (OFF) on the UCCx8C52 and UCCx8C54 devices make them ideally suited to off-line AC-DC applications. The corresponding typical thresholds for the UCCx8C53 and UCCx8C55 devices are 8.4 V (ON) and 7.6 V (OFF), making them ideal for use with regulated input voltages used in DC-DC applications. The UCCx8C50 and UCCx8C51 feature a start-up threshold of 7 V and a turnoff threshold of 6.6 V (OFF), which makes them suitable for battery-powered applications. The UCC28C56H/L, UCC28C57H/L, UCC28C58 and UCC28C59 can operate with higher UVLO thresholds to reliably drive SiC MOSFETs in high-voltage applications. The UCC28C56H and UCC28C57H operate with start threshold of 18.8 V (ON) and stop threshold of 15.5 V (OFF). The UCC28C56L and UCC28C57L operate with start threshold of 18.8V (ON) and stop threshold of 14.5 V (OFF). The UCC28C58 and UCC28C59 operate with start threshold of 16 V (ON) and stop threshold of 12.5 V (OFF). The UCCx8C50, UCCx8C52, UCCx8C53, UCC28C56H/L and UCC28C58 devices can operate with duty cycles approaching 100%. The UCCx8C51, UCCx8C54, UCCx8C55, UCC28C57H/L and UCC28C59 devices can operate from 0% to 50% duty cycle, by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle. The UCC28C5x series is specified for operation from -40°C to 125°C , and the UCC38C5x series is specified for operation from 0°C to 85°C . The switching frequency (f_{SW}) of the UCCx8C50, UCCx8C52, UCCx8C53, UCC28C56H/L and UCC28C58 gate drive is equal to f_{OSC}; the switching frequency of the UCCx8C51, UCCx8C54, UCCx8C55, UCC28C57H/L and UCC28C59 is equal to half of the f_{OSC}.

The UCC28C5x and UCC38C5x series devices are drop-in replacement for BiCMOS UCCx8C4x family and pin-to-pin compatible with the bipolar UC284x, UC384x, UC284xA, and UC384xA families. The new series offers improved performance when compared to older bipolar devices and other competitive BiCMOS devices with similar functionality. These improvements generally consist of tighter specification limits that are a subset of the older product ratings. In new designs, these improvements can reduce the component count or enhance circuit performance when compared to the older generation devices.

8.2 Functional Block Diagram



Toggle flip-flop used only in UCCx8C51, UCCx8C54, UCCx8C55, UCC28C57H/L, and UCC28C59

8.3 Feature Description

The BiCMOS design allows operation at high frequencies that were not feasible in the predecessor bipolar devices. First, the output stage has been redesigned to drive the external power switch in approximately half the time of the earlier devices. Second, the internal oscillator is more robust, with less variation as frequency increases. This faster oscillator makes this device suitable for high speed applications and the trimmed discharge current enables precise programming of the maximum duty cycle and dead-time limit. In addition, the current sense to output delay is kept the same 45 ns (typical) as UCCx8C4x. Such a delay time in the current sense results in superior overload protection at the power switch. The reduced start-up current of this device minimizes steady state power dissipation in the startup resistor, and the low operating current maximizes efficiency while running, increasing the total circuit efficiency, whether operating off-line, DC input, or battery operated circuits. These features combine to provide a device capable of reliable, high-frequency operation.

表 8-1. Improved Key Parameters

PARAMETER	UCCx8C4x	UCCx8C5x
Supply current at 52 kHz	2.3 mA	1.3 mA
Start-up current, maximum	100 μ A	75 μ A
V_{DD} absolute maximum	20 V	30 V
Reference voltage accuracy	$\pm 1\%$	$\pm 2\%$
UVLO and Dmax for Si FETs	6 options	6 options
UVLO and Dmax for SiC FETs	No options	6 options
Smallest package option	VSSOP (8)	VSSOP (8)

8.3.1 Detailed Pin Description

8.3.1.1 COMP

The error amplifier in the UCC28C5x family has a unity-gain bandwidth of 1 MHz. The COMP terminal can both source and sink current. The error amplifier is internally current-limited, so that one can command zero duty cycle by externally forcing COMP to GND.

8.3.1.2 FB

FB is the inverting input of the error amplifier. The noninverting input to the error amplifier is internally trimmed to $2.5\text{ V} \pm 1\%$. FB is used to control the power converter voltage-feedback loop for stability. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

8.3.1.3 CS

The UCC28C5x current sense input connects directly to the PWM comparator. Connect CS to the MOSFET source current sense resistor. The PWM uses this signal to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration or to add slope compensation. To prevent false triggering due to leading edge noises, an RC current sense filter may be required. The gain of the current sense amplifier is typically 3 V/V.

8.3.1.4 RT/CT

The internal oscillator uses a timing capacitor (C_{CT}) and a timing resistor (R_{RT}) to program the oscillator frequency and maximum duty cycle. The operating frequency can be programmed based the curves in [Figure 7-1](#), where the timing resistor can be found once the timing capacitor is selected. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 15.4 k Ω and 1000 pF were selected for R_{RT} and C_{CT} to operate at 110-kHz switching.

8.3.1.5 GND

GND is the signal and power returning ground. TI recommends separating the signal return path and the high current gate driver path so that the signal is not affected by the switching current.

8.3.1.6 OUT

The high-current output stage of the UCCx8C5x to drive the external power switch has been kept the same as the earlier devices UCC28C4x. To drive a power MOSFET directly, the totem-pole OUT driver sinks or source up to 1 A peak of current. The OUT of the UCCx8C50, UCCx8C52, UCCx8C53, UCC28C56H/L and UCC28C58 devices switch at the same frequency as the oscillator and can operate near 100% duty cycle. In the UCCx8C51, UCCx8C54, and UCCx8C55, UCC28C57H/L and UCC28C59, the switching frequency of OUT is one-half that of the oscillator due to an internal T flip-flop. This limits the maximum duty cycle in the UCCx8C51, UCCx8C54, and UCCx8C55, UCC28C57H/L and UCC28C59 to < 50%.

The UCCx8C5x family houses unique totem pole drivers exhibiting a 10- Ω impedance to the upper rail and a 5.5- Ω impedance to ground, typically. This reduced impedance on the low-side switch helps minimize turn-off losses at the power MOSFET, whereas the higher turnon impedance of the high-side is intended to better match the reverse recovery characteristics of many high-speed output rectifiers. Transition times, rising and falling edges, are typically 25 nanoseconds and 20 nanoseconds, respectively, for a 10% to 90% change in voltage.

A low impedance MOS structure in parallel with a bipolar transistor, or BiCMOS construction, comprises the totem-pole output structure. This more efficient utilization of silicon delivers the high peak current required along with sharp transitions and full rail-to-rail voltage swings. Furthermore, the output stage is self-biasing, active low during under-voltage lockout type. With no VDD supply voltage present, the output actively pulls low if an attempt is made to pull the output high. This condition frequently occurs at initial power-up with a power MOSFET as the driver load.

8.3.1.7 VDD

VDD is the power input connection for this device. In normal operation, power VDD through a current limiting resistor. The absolute maximum supply voltage is 30 V (extended from 20 V of UCCx8C4x) to facilitate more designs and applications. The voltage level of 30 V, including any transients that may be present, cannot be exceeded, device damage is likely if otherwise. Because of this limitation, the UCCx8C5x devices match the predecessor bipolar devices, which could survive up to 30 V on the input bias pin. Because no internal clamp is included in the device, the VDD pin must be protected from external sources which could exceed the 30 V level. If containing the start-up and bootstrap supply voltage from the auxiliary winding N_A below 30 V under all line and load conditions can not be achieved, use a zener protection diode from VDD to GND. Depending on the impedance and arrangement of the bootstrap supply, this may require adding a resistor, R_{VDD} , in series with the auxiliary winding to limit the current into the zener as shown in [Figure 8-1](#). Ensure that over all tolerances and temperatures, the minimum zener voltage is higher than the highest UVLO upper turn-on threshold. To prevent noise related problems, filter VDD with a ceramic bypass capacitor to GND. The VDD pin must be decoupled as close to the GND pin as possible.

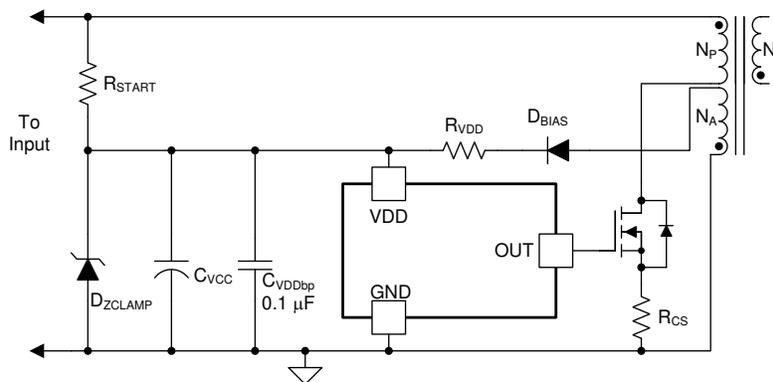


Figure 8-1. VDD Protection

Although nominal VDD operating current is only 1.3 mA, the total supply current is higher, depending on the OUT current. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from [Equation 1](#).

$$I_{OUT} = Q_g \times f_{SW} \quad (1)$$

8.3.1.8 VREF

VREF is the voltage reference for the error amplifier and also for many other internal circuits in the IC. The 5-V reference tolerance is $\pm 1\%$ for the UCC28C5x family. The high-speed switching logic uses VREF as the logic power supply. The reference voltage is divided down internally to 2.5 V $\pm 1\%$ and connected to the error amplifier's noninverting input for accurate output voltage regulation. The reference voltage sets the internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. The output short-circuit current is 55 mA (maximum). To avoid device over-heating and damage, do not pull VREF to ground as a means to terminate switching. For reference stability and to prevent noise problems with high-speed switching transients, bypass VREF to GND with a ceramic capacitor close to the IC package. A ceramic capacitor with a minimum value of 0.1 μ F is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

8.3.2 Undervoltage Lockout

Six sets of UVLO thresholds are available with turn-on and turnoff thresholds of: (14.5 V and 9 V), (8.4 V and 7.6 V), (7 V and 6.6 V), (18.8 V and 15.5 V), (18.8 V and 14.5V) and (16 V and 12.5V), respectively. The first set is primarily intended for off-line and 48-V distributed power applications, where the wider hysteresis allows for lower frequency operation and longer soft-starting time of the converter. The second set of UVLO option is ideal for high frequency DC-DC converters typically running from a 12-VDC input. The third set is for battery powered and portable applications. The fourth to sixth UVLO sets are suitable to drive SiC MOSFETs in high voltage applications. 表 8-2 shows the maximum duty cycle and UVLO thresholds by device.

表 8-2. UVLO Options

MAXIMUM DUTY CYCLE (%)	UVLO ON (V)	UVLO OFF (V)	DEVICE NUMBER
100	14.5	9	UCCx8C52
100	8.4	7.6	UCCx8C53
100	7	6.6	UCCx8C50
100	18.8	15.5	UCC28C56H
100	18.8	14.5	UCC28C56L
100	16	12.5	UCC28C58
50	14.5	9	UCCx8C54
50	8.4	7.6	UCCx8C55
50	7	6.6	UCCx8C51
50	18.8	15.5	UCC28C57H
50	18.8	14.5	UCC28C57L
50	16	12.5	UCC28C59

During UVLO the IC draws less than 75 μ A of supply current. Once crossing the turnon threshold the IC supply current increases to a maximum of 2mA, typically 1.3 mA. This low start-up current allows the power supply designer to optimize the selection of the startup resistor value to provide a more efficient design. In applications where low component cost overrides maximum efficiency, the low run current of 1.3 mA (typical) allows the control device to run directly through the single resistor to (+) rail, rather than requiring a bootstrap winding on the power transformer, along with a rectifier. The start and run resistor for this case must also pass enough current to allow driving the primary switching MOSFET, which may be a few milliamps in small devices.

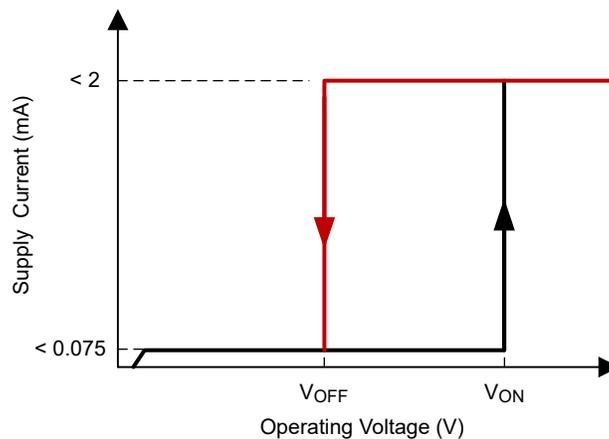


图 8-2. UVLO ON and OFF Profile

8.3.3 $\pm 1\%$ Internal Reference Voltage

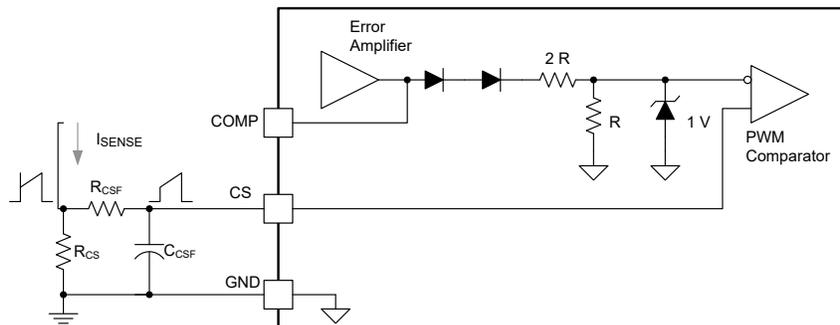
The BiCMOS internal reference of 2.5 V has an enhanced design, and uses production trim to allow initial accuracy of $\pm 1\%$ at room temperature and $\pm 2\%$ over the full temperature range. This reference voltage can be used to eliminate an external reference in applications that do not require the extreme accuracy afforded by the additional device. This reference voltage is useful for non-isolated DC-DC applications, where the control device is referenced to the same common as the output. It is also applicable in off-line designs that regulate on the primary side of the isolation boundary by looking at a primary bias winding, or from a winding on the output inductor of a buck-derived circuit.

8.3.4 Current Sense and Overcurrent Limit

An external series resistor (R_{CS}) senses the current and converts this current into a voltage that becomes the input to the CS pin. The CS pin is the noninverting input to the PWM comparator. The device compares the CS input with a signal proportional to the error amplifier output voltage. The gain of the current sense amplifier is typically 3 V/V. The peak I_{SENSE} current is determined using 式 2

$$I_{SENSE} = \frac{V_{CS}}{R_{CS}} \quad (2)$$

The typical value for V_{CS} is 1 V. A small RC filter (R_{CSF} and C_{CSF}) may be required to suppress switch transients caused by the reverse recovery of a secondary side diode or equivalent capacitive loading in addition to parasitic circuit impedances. The time constant of this filter should be considerably less than the switching period of the converter.



8-3. Current-Sense Circuit Schematic

Cycle-by-cycle pulse width modulation performed at the PWM comparator essentially compares the error amplifier output to the current sense input. This is not a direct volt-to-volt comparison, as the error amplifier output network incorporates two diodes in series with a resistive divider network before connecting to the PWM comparator. The two-diode drop adds an offset voltage that enables zero duty cycle to be achieved with a low amplifier output. The $2R/R$ resistive divider facilitates the use of a wider error amplifier output swing that can be more symmetrically centered on the 2.5-V noninverting input voltage.

The 1-V Zener diode associated with the PWM comparator input from the error amplifier is not an actual diode in the device design, but an indication that the maximum current sense input amplitude is 1 V (typical). When this threshold is reached, regardless of the error amplifier output voltage, cycle-by-cycle current limiting occurs, and the output pulse width is terminated within 35 ns (typical). The minimum value for this current limit threshold is 0.9 V with a 1.1-V maximum. In addition to the tolerance of this parameter, the accuracy of the current sense resistor, or current sense circuitry, must be taken into account. It is advised to factor in the worst case of primary and secondary currents when sizing the ratings and worst-case conditions in all power semiconductors and magnetic components.

8.3.5 Reduced-Discharge Current Variation

The oscillator design for the UCC28C5x controllers incorporates a trimmed discharge current to accurately program maximum duty cycle and operating frequency. In its basic operation, a timing capacitor (C_{CT}) is charged by a current source, formed by the timing resistor (R_{RT}) connected to the device reference voltage (V_{REF}). The oscillator design incorporates comparators to monitor the amplitude of the timing capacitor voltage. The exponentially shaped waveform charges up to a specific amplitude representing the oscillator upper threshold of 3 V. After the controller reaches this level, an internal current sink to ground turns on and the capacitor begins to discharge. This discharge continues until the oscillator lower threshold has reached 0.7 V at which point the current sink is turned off. Next, the timing capacitor starts charging again and a new switching cycle begins.

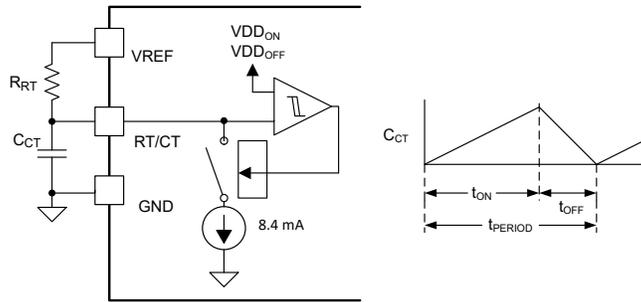
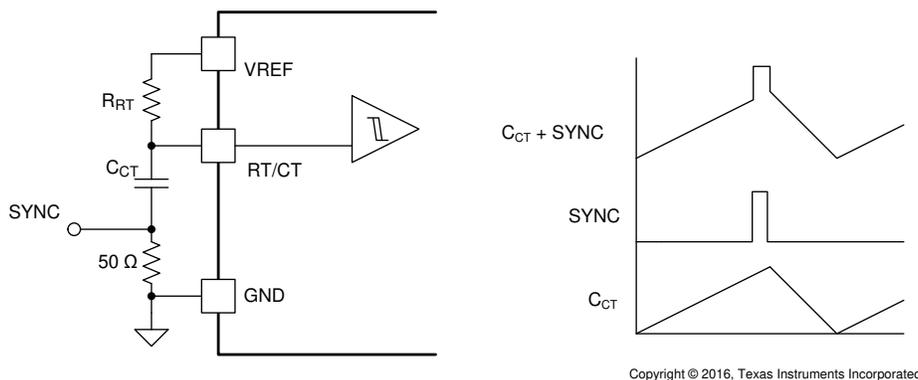


图 8-4. Oscillator Circuit

While the device discharges the timing capacitor, resistor R_{RT} continues attempting to charge C_{CT} . It is the exact ratio of these two currents, the discharging versus the charging current, which specifies the maximum duty cycle. During the discharge time of C_{CT} , the device output is always off. This represents an ensured minimum off time of the switch, commonly referred to as dead-time. To program an accurate maximum duty cycle, use the information provided in Maximum Duty Cycle vs Oscillator Frequency for maximum duty cycle versus oscillator frequency. Any number of maximum duty cycles can be programmed for a given frequency by adjusting the values of R_{RT} and C_{CT} . After selecting the value of R_{RT} , find the oscillator timing capacitance using the curves in Oscillator Frequency vs Timing Resistance and Capacitance. However, because resistors are available in more precise increments, typically 1%, and capacitors are only available in 5% accuracy, it might be more practical to select the closest capacitor value first and then calculate the timing resistor value.

8.3.6 Oscillator Synchronization

Synchronization is best achieved by forcing the timing capacitor voltage above the oscillator internal upper threshold. A small resistor is placed in series with C_{CT} to GND. This resistor serves as the input for the sync pulse which raises the C_{CT} voltage above the oscillator internal upper threshold. The PWM is allowed to run at the frequency set by R_{RT} and C_{CT} until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UCC28C5x oscillator must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5-V pulse applied across the resistor.



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图 8-5. Oscillator Synchronization Circuit

8.3.7 Soft-Start Timing

The soft-start timing is the technique to gradually power up the converter in a well-controlled fashion by slowly increasing the effective duty cycle starting at zero and gradually rising. Following start-up of the PWM, the error amplifier inverting input is low, commanding the error amplifier's output to go high. The output stage of the amplifier can source 1 mA typically, which is enough to drive most high impedance compensation networks, but not enough for driving large loads quickly. Soft-start timing is achieved by charging a fairly large value, $>1\text{-}\mu\text{F}$, capacitor (C_{SS}) connected to the error amplifier output through a PNP transistor as shown in [Figure 8-6](#)

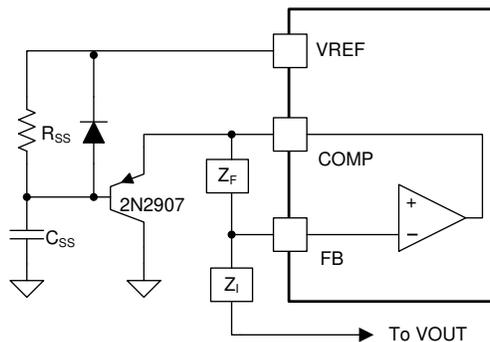


Figure 8-6. Soft-Start Implementation

The limited charging current of the amplifier into the capacitor translates into a dv/dt limitation on the error amplifier output. This directly corresponds to some maximum rate of change of primary current in a current mode controlled system as one of the PWM comparator inputs gradually rises. The values of R_{SS} and C_{SS} must be selected to bring the COMP pin up at a controlled rate, limiting the peak current supplied by the power stage. After the soft-start interval is complete, the capacitor continues to charge to V_{REF} , effectively removing the PNP transistor from the circuit consideration. Soft-start timing offers a different, frequently preferred function in current mode controlled systems than it does in voltage mode control. In current mode, soft start controls the rising of the peak switch current. In voltage mode control, soft start gradually widens the duty cycle, regardless of the primary current or rate of ramp-up.

The purpose of resistor R_{SS} and the diode is to remove the soft-start capacitor from the error amplifier path during normal operation, after the soft-start period completes and the capacitor charges fully. The optional diode in parallel with the resistor forces a soft-start period each time the PWM goes through UVLO condition that forces V_{REF} to go low. Without the diode, the capacitor remains charged during a brief loss of supply or brown-out, and the device does not enable a soft-start function upon re-application of V_{DD} .

8.3.8 Enable and Disable

There are several ways to enable or disable the UCC28C5x devices, depending on which type of restart is required. The two basic techniques use external transistors to either pull the error amplifier output low ($< 2 V_{BE}$) or pull the current sense input high ($> 1.1\text{ V}$). Application of the disable signal causes the output of the PWM comparator to be high. The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or CS pin is removed. Another choice for restart without a soft-start period is to pull the current sense input above the cycle-by-cycle current limiting threshold. A logic level P-channel FET from the reference voltage to the current sense input can be used.

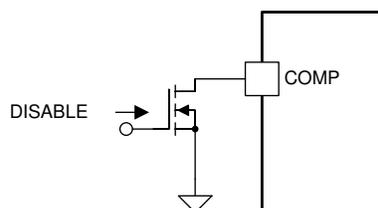


Figure 8-7. Disable Circuit

8.3.9 Slope Compensation

With current mode control, slope compensation is required to stabilize the overall loop with duty cycles exceeding 50%. Although not required, slope compensation also improves stability in applications using below a 50% maximum duty cycle. Slope compensation is introduced by injecting a portion of the oscillator waveform to the actual sensed primary current. The two signals are summed together at the current sense input (CS) connection at the filter capacitor. To minimize loading on the oscillator, it is best to buffer the timing capacitor waveform with a small transistor whose collector is connected to the reference voltage.

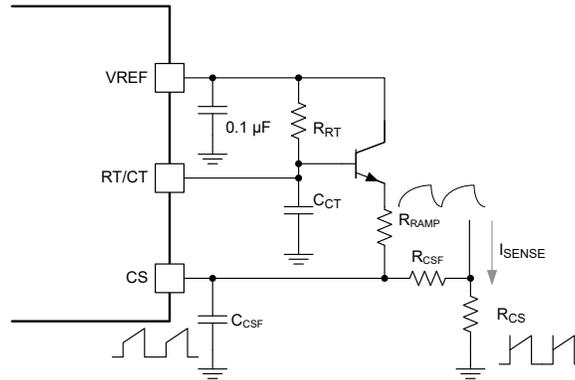


Figure 8-8. Slope Compensation Circuit

8.3.10 Voltage Mode

In certain applications, voltage mode control may be a preferred control strategy for a variety of reasons. Voltage mode control is easily executable with any current mode controller, especially the UCC28C5x family members. Implementation requires generating a 0-V to 0.9-V sawtooth shaped signal to input to the current sense pin (CS) which is also one input to the PWM comparator. This is compared to the divided down error amplifier output voltage at the other input of the PWM comparator. As the error amplifier output is varied, it intersects the sawtooth waveform at different points in time, thereby generating different pulse widths. This is a straightforward method of linearly generating a pulse whose width is proportional to the error voltage.

Implementation of voltage mode control is possible by using a fraction of the oscillator timing capacitor (C_{CT}) waveform. This value can be divided down and fed to the current sense pin as shown in [Figure 8-9](#). The oscillator timing components must be selected to approximate as close to a linear sawtooth waveform as possible. Although exponentially charged, large values of timing resistance and small values of timing capacitance help approximate a more linear shaped waveform. A small transistor is used to buffer the oscillator timing components from the loading of the resistive divider network. Due to the offset of the oscillator's lower timing threshold, a DC blocking capacitor is added.

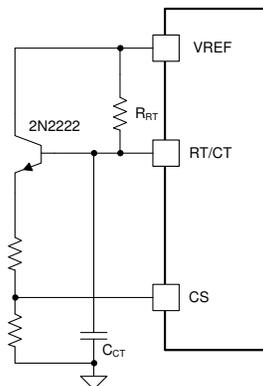


Figure 8-9. Current Mode PWM Used as a Voltage Mode PWM

8.4 Device Functional Modes

8.4.1 Normal Operation

During normal operating mode, the controller can be used in peak current mode or voltage mode control. When the converter is operating in peak current mode, the controller regulates the converter's peak current and duty cycle. When used in voltage mode control, the controller regulates the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

8.4.2 UVLO Mode

During the system start-up, VDD voltage starts to rise from 0 V. Before the VDD voltage reaches its corresponding turn-on threshold, the IC is operating in UVLO mode. During UVLO mode operation, the VREF pin voltage is not generated. When VDD is above 1 V and below the turn-on threshold, the VREF pin is actively pulled low. This behavior allows VREF to be used as a logic signal to indicate UVLO mode. If the bias voltage to VDD drops below the UVLO-OFF threshold, the PWM switching stops and VREF returns to 0 V. The device can be restarted by applying a voltage greater than the UVLO-ON threshold to the VDD pin.

9 Application and Implementation

注

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9.1 Application Information

The UCC28C5x controllers are peak current mode pulse width modulators. These controllers have an onboard amplifier and can be used in isolated and nonisolated power supply designs. The onboard totem pole gate driver is capable of delivering 1 A of peak current. This high-speed PWM is capable of operating at switching frequencies up to 1 MHz. Since UCCx8C5x can be used to directly substitute UCCx8C4x by drop-in, the design steps are the same as those for UCCx8C4x. The same design example, including the layout, of UCCx8C4x is re-used for UCCx8C5x as shown below. [図 9-1](#) shows a typical off-line application using UCC38C44.

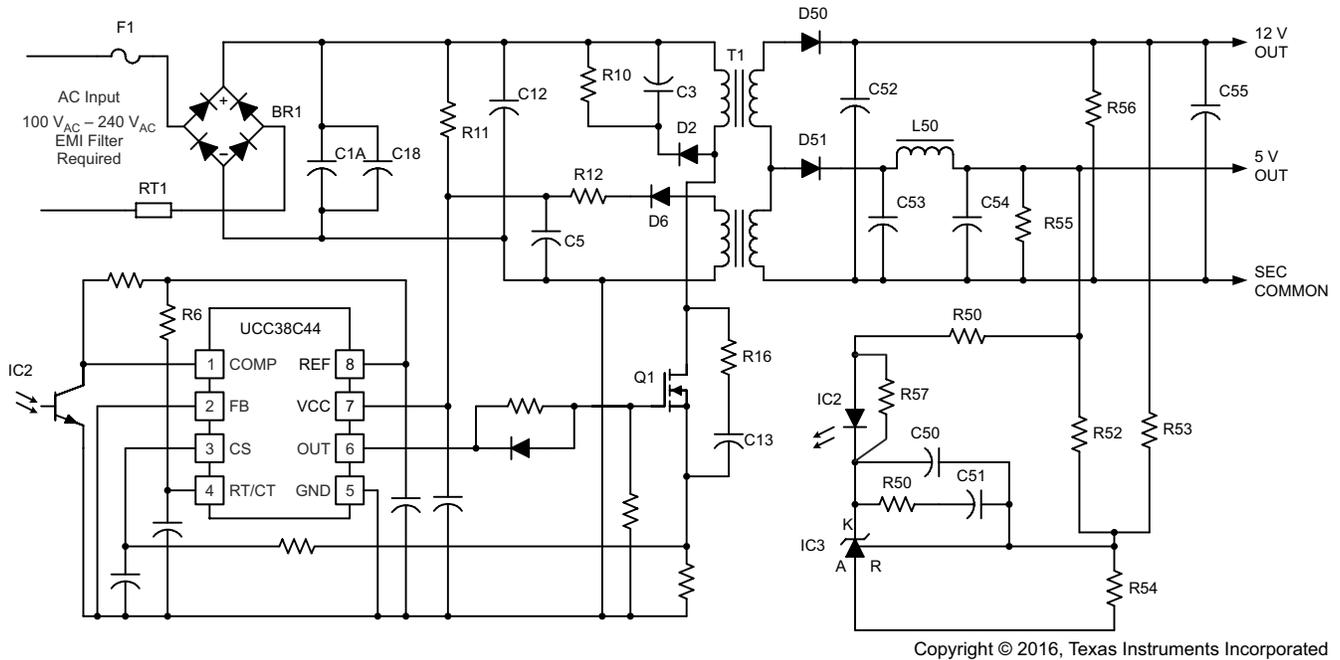
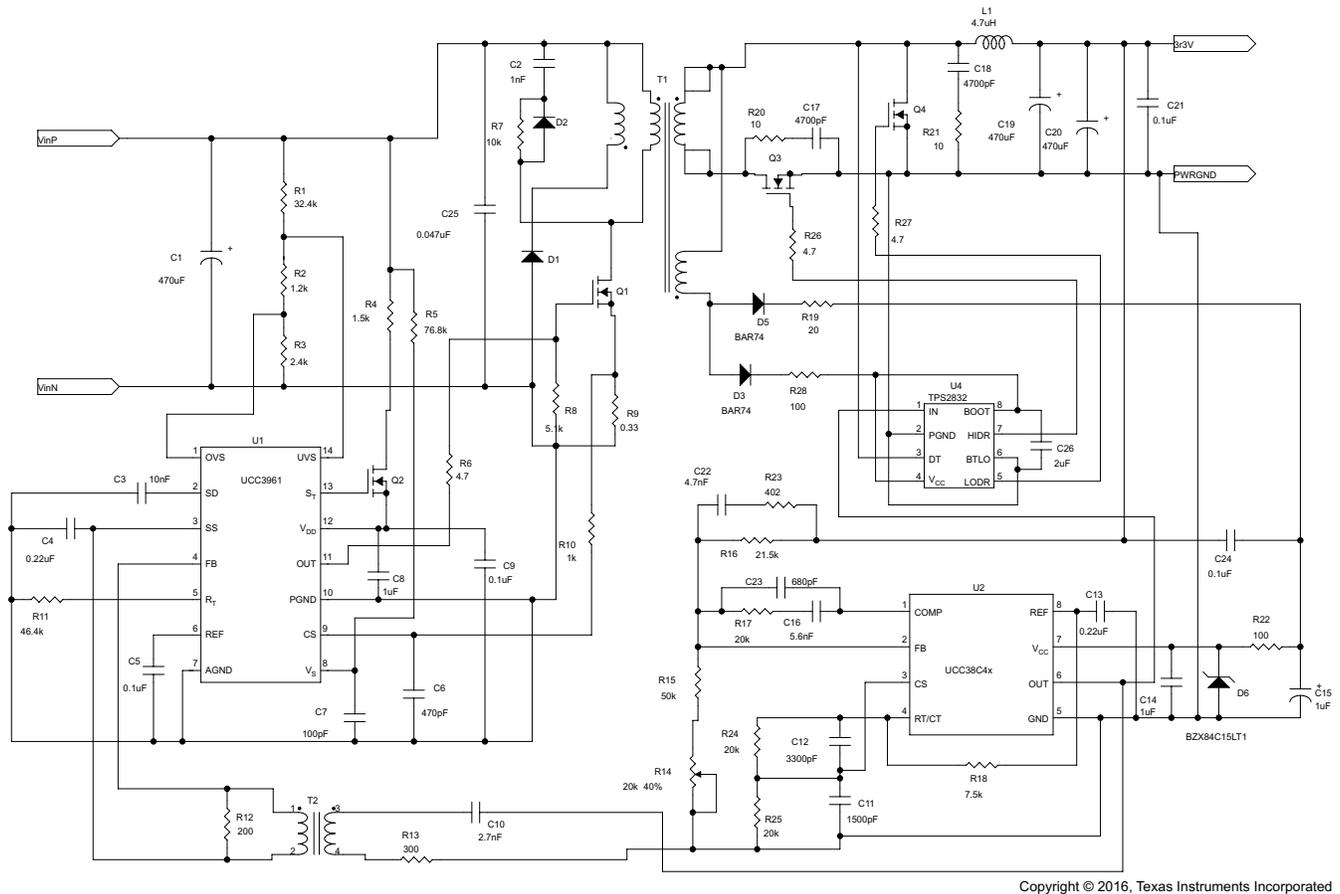


図 9-1. Typical Off-Line Application

9-2 shows a forward converter with synchronous rectification. This application provides 48 V to 3.3 V at 10 A with over 85% efficiency, and uses the UCC38C42 as the secondary-side controller and UCC3961 as the primary-side startup control device.

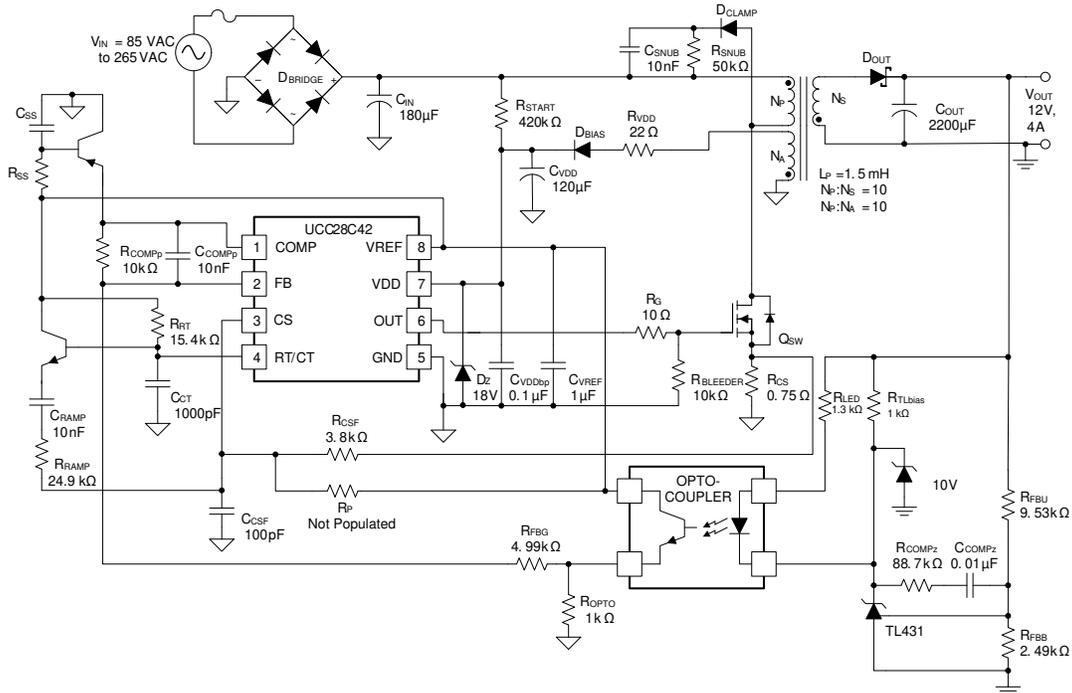


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9-2. Forward Converter with Synchronous Rectification Using the UCC38C42 as the Secondary-Side Controller

9.2 Typical Application

A typical application for the UCC28C42 controller in an off-line flyback converter is shown in [Figure 9-3](#). The UCC28C52 controller can be used as drop-in replacement for UCC28C42. The controller uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.



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Figure 9-3. Typical Application Design Schematic

9.2.1 Design Requirements

Table 9-1 shows a typical set of performance requirements for an off-line flyback converter capable of providing 48 W at 12-V output voltage from a universal AC input. The design uses peak primary current control in a continuous current mode PWM converter.

Table 9-1. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V _{IN}	Input Voltage	85	115/230	265	V _{RMS}
f _{LINE}	Line Frequency	47	50/60	63	Hz
V _{OUT}	Output Voltage	11.75	12	12.25	V
V _{RIPPLE}	Output Ripple Voltage			100	mVpp
I _{VOUT}	Output Current	0	4		A
f _{SW}	Switching Frequency		110		kHz

表 9-1. Design Parameters (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
η	Efficiency			85%		

9.2.2 Detailed Design Procedure

This procedure outlines the steps to design an off-line universal input continuous current mode (CCM) flyback converter. See [Figure 9-3](#) for component names referred to in the design procedure.

9.2.2.1 Input Bulk Capacitor and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. The value of the input capacitor sets the minimum bulk voltage;. Setting the bulk voltage lower by using minimal input capacitance results in higher peak primary currents leading to more stress on the MOSFET switch, the transformer, and the output capacitors. Setting the bulk voltage higher by using a larger input capacitor results in higher peak current from the input source and the capacitor itself is physically larger. Compromising between size and component stresses determines the acceptable minimum input voltage. The total required value for the primary-side bulk capacitance (C_{IN}) is selected based upon the power level of the converter (P_{OUT}), the efficiency target (η), the minimum input voltage ($V_{IN(min)}$), and is chosen to maintain an acceptable minimum bulk voltage level ($V_{BULK(min)}$), using [Equation 3](#).

$$C_{IN} = \frac{2 \times P_{IN} \times \left(0.25 + \frac{1}{\pi} \times \arcsin \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE(min)}} \quad (3)$$

where

- $V_{IN(min)}$ is the RMS value of the minimum AC input voltage (85 VRMS) whose minimum line frequency is denoted as $f_{LINE(min)}$, equal to 47 Hz

Based on [Equation 3](#), to achieve a minimum bulk voltage of 75 V, assuming 85% converter efficiency, the bulk capacitor must be larger than 126 μ F. this design uses a value of 180 μ F, with consideration for component tolerances and efficiency estimation.

9.2.2.2 Transformer Turns Ratio and Maximum Duty Cycle

The transformer design begins with selecting a suitable switching frequency for the given application. The UCC28C42 is capable of switching up to 1 MHz but considerations such as overall converter size, switching losses, core loss, system compatibility, and interference with communication frequency bands generally determine an optimum frequency that should be used. For this off-line converter, the switching frequency (f_{SW}) is selected to be 110 kHz as a compromise to minimize the transformer size and the EMI filter size, and still have acceptable losses.

The transformer primary to secondary turns ratio (N_{PS}) can be selected based on the desired MOSFET voltage rating and the secondary diode voltage rating. Because the maximum input voltage is 265 VRMS, the peak bulk input voltage can be calculated as shown in [Equation 4](#).

$$V_{BULK(max)} = \sqrt{2} \times V_{IN(max)} \approx 375 \text{ V} \quad (4)$$

To minimize the cost of the system, a readily available 650-V MOSFET is selected. Derating the maximum voltage stress on the drain to 80% of its rated value and allowing for a leakage inductance voltage spike of up to 30% of the maximum bulk input voltage, the reflected output voltage must be less than 130 V as shown in [Equation 5](#).

$$V_{REFLECTED} = 0.8 \times \left(V_{DS(rated)} - 1.3 \times V_{BULK(max)} \right) = 130.2 \text{ V} \quad (5)$$

The maximum primary to secondary transformer turns ratio (N_{PS}) for a 12 V output can be selected as

$$N_{PS} = \frac{V_{REFLECTED}}{V_{OUT}} = 10.85 \quad (6)$$

A turns ratio of $N_{PS} = 10$ is used in the design example.

The auxiliary winding is used to supply bias voltage to the controller. Maintaining the bias voltage above the VDD minimum operating voltage after turnon is required for stable operation. The minimum VDD operating voltage for the controller selected for this design is 10 V. The auxiliary winding is selected to support a 12 V bias voltage so that it is above the minimum operating level but maintains a low level of losses in the IC. The primary to auxiliary turns ratio (N_{PA}) can be calculated from 式 7:

$$N_{PA} = N_{PS} \times \frac{V_{OUT}}{V_{BIAS}} = 10 \quad (7)$$

The output diode experiences a voltage stress that is equal to the output voltage plus the reflected input voltage:

$$V_{DIODE} = \frac{V_{BULK(max)}}{N_{PS}} + V_{OUT} = 49.5 \text{ V} \quad (8)$$

TI recommends a Schottky diode with a rated blocking voltage greater than 60 V to allow for voltage spikes due to ringing. The forward voltage drop (V_F) of this diode is estimated to be equal to 0.6 V

To avoid high peak currents, the flyback converter in this design operates in continuous conduction mode. Once N_{PS} is determined, the maximum duty cycle (D_{MAX}) can be calculated using the transfer function for a CCM flyback converter:

$$\frac{V_{OUT} + V_F}{V_{BULK(min)}} = \left(\frac{1}{N_{PS}}\right) \times \left(\frac{D_{MAX}}{1 - D_{MAX}}\right) \quad (9)$$

$$D_{MAX} = \frac{N_{PS} \times (V_{OUT} + V_F)}{V_{BULK(min)} + N_{PS} \times (V_{OUT} + V_F)} = 0.627 \quad (10)$$

Because the maximum duty cycle exceeds 50%, and the design is an off-line (AC-input) application, the UCC28C42 is best suited for this application.

9.2.2.3 Transformer Inductance and Peak Currents

For this design example, the transformer magnetizing inductance is selected based upon the CCM condition. An inductance value that allows the converter to stay in CCM over a wider operating range before transitioning into discontinuous current mode is used to minimize losses due to otherwise high currents and also to decrease the output ripple. The design of the transformer in this example sizes the inductance so the converter enters CCM operation at approximately 10% load and minimum bulk voltage to minimize output ripple.

The inductor (L_P) for a CCM flyback can be calculated using 式 11.

$$L_P = \frac{1}{2} \times \frac{(V_{BULK(min)})^2 \times \left(\frac{N_{PS} \times V_{OUT}}{V_{BULK(min)} + N_{PS} \times V_{OUT}}\right)^2}{0.1 \times P_{IN} \times f_{SW}} \quad (11)$$

where

- P_{IN} is estimated by dividing the maximum output power (P_{OUT}) by the target efficiency (η)
- f_{SW} is the switching frequency of the converter

For the UCC28C42 the switching frequency is equal to the oscillator frequency and is set to 110 kHz. Selecting f_{SW} to be 110 kHz provides a good compromise between size of magnetics, switching losses, and places the first harmonic below the 150-kHz lower limit of EN55022. Therefore, the transformer inductance must be approximately 1.8 mH. A 1.5 mH inductance is chosen as the magnetizing inductance, L_P , value for this design.

Based on calculated inductor value and the switching frequency, the current stress of the MOSFET and output diode can be calculated.

The peak current in the primary-side MOSFET of a CCM flyback can be calculated as shown in 式 12.

$$I_{PK_MOSFET} = \frac{P_{IN}}{V_{BULK (min)} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK (min)} + (N_{PS} \times V_{OUT})}} + \left(\frac{V_{BULK (min)}}{2 \times L_m} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK (min)} + (N_{PS} \times V_{OUT})} \right) \quad (12)$$

The MOSFET peak current is 1.36 A. The RMS current of the MOSFET is calculated to be 0.97 A as shown in 式 13. Therefore, IRFB9N65A is selected to be used as the primary-side switch.

$$I_{RMS_MOSFET} = \sqrt{\frac{D_{MAX}^3}{3} \times \left(\frac{V_{BULK (min)}}{L_p \times f_{SW}} \right)^2 - \left(\frac{D_{MAX}^2 \times I_{PK_MOSFET} \times V_{BULK (min)}}{L_p \times f_{SW}} \right) + (D_{MAX} \times I_{PK_MOSFET}^2)} \quad (13)$$

The output diode peak current is equal to the MOSFET peak current reflected to the secondary side.

$$I_{PK_DIODE} = N_{PS} \times I_{PK_MOSFET} = 13.634 \text{ A} \quad (14)$$

The diode average current is equal to the total output current (4 A) combined with a required 60-V rating and 13.6-A peak current requirement, a 48CTQ060-1 is selected for the output diode.

9.2.2.4 Output Capacitor

The total output capacitance is selected based upon the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected using 式 15.

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK (min)} + N_{PS} \times V_{OUT}}}{0.001 \times V_{OUT} \times f_{SW}} = 1865 \mu\text{F} \quad (15)$$

To design for device tolerances, a 2200-μF capacitor was selected.

9.2.2.5 Current Sensing Network

The current sensing network consists of the primary-side current sensing resistor (R_{CS}), filtering components R_{CSF} and C_{CSF} , and optional R_P . Typically, the direct current sense signal contains a large amplitude leading edge spike associated with the turnon of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. Therefore, C_{CSF} and R_{CSF} form a low-pass filter that provides immunity to suppress the leading edge spike. For this converter, C_{CSF} is chosen to be 100 pF.

Without R_P , R_{CS} sets the maximum peak current in the transformer primary based on the maximum amplitude of the CS pin, which is specified to be 1 V. To achieve 1.36-A primary side peak current, a 0.75- Ω resistor is chosen for R_{CS} .

The high current sense threshold of CS helps to provide better noise immunity to the system but also results in higher losses in the current sense resistor. These current sense losses can be minimized by injecting an offset voltage into the current sense signal using R_P . R_P and R_{CSF} form a resistor divider network from the current sense signal to the reference voltage of the controller (V_{VREF}) which adds an offset to the current sense voltage. This technique still achieves current mode control with cycle-by-cycle over-current protection. To calculate required offset value (V_{OFFSET}), use 式 16.

$$V_{OFFSET} = \frac{R_{CSF}}{R_{CSF} + R_P} \times V_{REF} \quad (16)$$

After adding the R_P resistance, adjust the R_{CS} value accordingly.

9.2.2.6 Gate Drive Resistor

R_G is the gate driver resistor for the power switch (Q_{SW}). The selection of this resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Using a larger resistor value for R_G slows down the turnon and turnoff of the MOSFET. A slower switching speed reduces EMI but also increases the switching loss. A tradeoff between switching loss and EMI performance must be carefully performed. For this design, a 10- Ω resistor was chosen for the gate drive resistor.

9.2.2.7 VREF Capacitor

A precision 5-V reference voltage performs several important functions. The reference voltage is divided down internally to 2.5 V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds. Therefore, the reference voltage must be bypassed with a ceramic capacitor. A 1- μ F, 16-V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective VREF and GND pins.

9.2.2.8 RT/CT

RT/CT is the oscillator timing pin. For fixed frequency operation, set the timing capacitor charging current by connecting a resistor from VREF to RT/CT. Set the frequency by connecting timing capacitor from RT/CT to GND. For the best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The controller's oscillator allows for operation to 1 MHz. The device uses an external resistor to set the charging current for the external capacitor, which determines the oscillator frequency. TI recommends timing resistor values from 1 k Ω to 100 k Ω and timing capacitor values from 220 pF to 4.7 nF. The UCCx8C5x oscillator is true to the curves of the original BiCMOS devices at lower frequencies, yet extends the frequency programmability range to at least 1 MHz. This programmability allows the device to offer pin-to-pin capability where required, yet capable of extending the operational range to the higher frequencies.

See [图 7-1](#) for component values for setting the oscillator frequency.

9.2.2.9 Start-Up Circuit

At start-up, the IC gets its power directly from the high-voltage bulk, through a high-voltage resistor (R_{START}). The selection of the start-up resistor is the tradeoff between power loss and start-up time. The current flowing through R_{START} at the minimum input voltage must be higher than the VDD current under UVLO conditions (100 μ A at its maximum value). A resistance of 420-k Ω was chosen for R_{START} , providing 250 μ A of start-up current at low-line conditions. The start-up resistor is physically comprised of two 210-k Ω resistors in series to meet the high voltage requirements and power rating at high-line.

After VDD is charged up above the UVLO-ON threshold, the UCC28C42 starts to consume full operating current. The VDD capacitor is required to provide enough energy to prevent its voltage from dropping below the UVLO-OFF threshold during start-up, before the output is able to reach its regulated level. A large bulk capacitance would hold more energy but would result in slower start-up time. In this design, a 120- μ F capacitor is chosen to provide enough energy and maintain a start-up time of approximately 7 seconds. For faster start-up, the bulk capacitor value may be decreased or the R_{START} resistor modified to a lower value.

9.2.2.10 Voltage Feedback Compensation

Feedback compensation, also called closed-loop control, can reduce or eliminate steady state error, reduce the sensitivity of the system to parametric changes, change the gain or phase of a system over some desired frequency range, reduce the effects of small signal load disturbances and noise on system performance, and create a stable system from an unstable system. A system is stable if its response to a perturbation is that the perturbation eventually dies out. A peak current mode flyback uses an outer voltage feedback loop to stabilize the converter. To adequately compensate the voltage loop, the open-loop parameters of the power stage must be determined.

9.2.2.10.1 Power Stage Poles and Zeroes

The first step in compensating a fixed frequency flyback is to verify if the converter is continuous conduction mode (CCM) or discontinuous conduction mode (DCM). If the primary inductance (L_P) is greater than the inductance for DCM or CCM boundary mode operation, called the critical inductance (L_{Pcrit}), then the converter operates in CCM:

$$L_P > L_{Pcrit}, \text{ then CCM} \quad (17)$$

$$L_{Pcrit} = \frac{R_{OUT} \times (N_{PS})^2}{2 \times f_{SW}} \times \left(\frac{V_{IN}}{V_{IN} + V_{OUT} \times N_{PS}} \right)^2 \quad (18)$$

For the entire input voltage range, the selected inductor has a value larger than the critical inductor. Therefore, the converter operates in CCM and the compensation loop requires design based on CCM flyback equations.

The current-to-voltage conversion is done externally with the ground-referenced R_{CS} and the internal 2R/R resistor divider which sets up the internal current sense gain, $A_{CS} = 3$. The exact value of these internal resistors is not critical but the IC provides tight control of the resistor divider ratio, so regardless of the actual resistor value variations their relative value to each other is maintained.

The DC open-loop gain (G_O) of the fixed-frequency voltage control loop of a peak current mode control CCM flyback converter shown in 式 19 is approximated by first using the output load (R_{OUT}), the primary to secondary turns ratio (N_{PS}), and the maximum duty cycle (D) as calculated in 式 20.

$$G_O = \frac{R_{OUT} \times N_{PS}}{R_{CS} \times A_{CS}} \times \frac{1}{\frac{(1-D)^2}{\tau_L} + (2 \times M) + 1} \quad (19)$$

In 式 19, D is calculated with 式 20, τ_L is calculated with 式 21, and M is calculated with 式 22.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULKmin} + (N_{PS} \times V_{OUT})} \quad (20)$$

$$\tau_L = \frac{2 \times L_P \times f_{SW}}{R_{OUT} \times (N_{PS})^2} \quad (21)$$

$$M = \frac{V_{OUT} \times N_{PS}}{V_{BULKmin}} \quad (22)$$

For this design, a converter with an output voltage (V_{OUT}) of 12 V, and 48 W relates to an output load (R_{OUT}) equal to 3 Ω at full load. With a maximum duty cycle of 0.627, a current sense resistance of 0.75 Ω , and a primary to secondary turns-ratio of 10, the open-loop gain calculates to 3.082 or 9.776 dB.

A CCM flyback has two zeroes that are of interest. The ESR and the output capacitance contribute a left-half plane zero (ω_{ESRz}) to the power stage, and the frequency of this zero (f_{ESRz}), are calculated with 式 23 and 式 24.

$$\omega_{ESRz} = \frac{1}{R_{ESR} \times C_{OUT}} \quad (23)$$

$$f_{ESRz} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (24)$$

The f_{ESRz} zero for an output capacitance of 2200 μF and a total ESR of 43 m Ω is located at 1.682 kHz.

CCM flyback converters have a zero in the right-half plane (RHP) in their transfer function. A RHP zero has the same 20 dB per decade rising gain magnitude with increasing frequency just like a left-half plane zero, but it adds a 90° phase lag instead of lead. This phase lag tends to limit the overall loop bandwidth. The frequency location (f_{RHPz}) of the RHP zero (ω_{RHPz}) is a function of the output load, the duty cycle, the primary inductance (L_P), and the primary to secondary side turns ratio (N_{PS}).

$$\omega_{RHPz} = \frac{R_{OUT} \times (1 - D)^2 \times (N_{PS})^2}{L_P \times D} \quad (25)$$

$$f_{RHPz} = \frac{R_{OUT} \times (1 - D)^2 \times (N_{PS})^2}{2 \times \pi \times L_P \times D} \quad (26)$$

The right-half plane zero frequency increases with higher input voltage and lighter load. Generally, the design requires consideration of the worst case of the lowest right-half plane zero frequency and the converter must be compensated at the minimum input and maximum load condition. With a primary inductance of 1.5 mH, at 75-V DC input, the RHP zero frequency (f_{RHPz}) is equal to 7.07 kHz at maximum duty cycle, full load.

The power stage has one dominate pole (ω_{p1}) which is in the region of interest, located at a lower frequency (f_{p1}); which is related to the duty cycle, the output load, and the output capacitance, and calculated with 式 28. There is also a double pole placed at half the switching frequency of the converter (f_{p2}) calculated with 式 30. For this example, pole f_{p1} is located at 40.37 Hz and f_{p2} is at 55 kHz.

$$\omega_{p1} = \frac{\frac{(1 - D)^3}{\tau_L} + 1 + D}{R_{OUT} \times C_{OUT}} \quad (27)$$

$$f_{P1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2 \times \pi \times R_{OUT} \times C_{OUT}} \quad (28)$$

$$\omega_{P2} = \pi \times f_{SW} \quad (29)$$

$$f_{P2} = \frac{f_{SW}}{2} \quad (30)$$

9.2.2.10.2 Slope Compensation

Slope compensation is the large signal subharmonic instability that can occur with duty cycles that may extend beyond 50% where the rising primary side inductor current slope may not match the falling secondary side current slope. The subharmonic oscillation would result in an increase in the output voltage ripple and may even limit the power handling capability of the converter.

The target of slope compensation is to achieve an ideal quality coefficient (Q_P), equal to 1 at half of the switching frequency. The Q_P is calculated with 式 31.

$$Q_P = \frac{1}{\pi \times [M_C \times (1 - D) - 0.5]} \quad (31)$$

where

- D is the primary side switch duty cycle
- M_C is the slope compensation factor, which is defined with 式 32

$$M_C = \frac{S_e}{S_n} + 1 \quad (32)$$

where

- S_e is the compensation ramp slope
- S_n is the inductor rising slope

The optimal goal of the slope compensation is to achieve $Q_P = 1$; upon rearranging 式 32 the ideal value of slope compensation factor is determined:

$$M_{ideal} = \frac{\frac{1}{\pi} + 0.5}{1 - D} \quad (33)$$

For this design to have adequate slope compensation, M_C must be 2.193 when D reaches its maximum value of 0.627.

The inductor rising slope (S_n) at the CS pin is calculated with 式 34.

$$S_n = \frac{V_{INmin} \times R_{CS}}{L_p} = 0.038 \frac{V}{\mu s} \quad (34)$$

The compensation slope (S_e) is calculated with 式 35.

$$S_e = (M_C - 1) \times S_n = 44.74 \frac{mV}{\mu s} \quad (35)$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF} . The C_{RAMP} is an AC-coupling capacitor that allows the voltage ramp of the oscillator to be used without adding an offset to the current sense; select a value to approximate a high-frequency short circuit, such as 10 nF, as a starting point and make adjustments if required. The R_{RAMP} and R_{CSF} resistors form a voltage divider from the oscillator charge slope and this proportional ramp is injected into the CS pin to add slope compensation. Choose the value of R_{RAMP} to be much larger than the R_{RT} resistor so that it does not load down the internal oscillator and result in a frequency shift. The oscillator charge slope is calculated using the peak-to-peak voltage of the RT/CT sawtooth waveform ($V_{OSC_{pp}}$) equal to 1.9 V, and the minimum ON time, as shown in 式 37.

$$t_{ONmin} = \frac{D}{f_{SW}} \quad (36)$$

$$S_{OSC} = \frac{V_{OSC_{pp}}}{t_{ONmin}} = \frac{1.9 \text{ V}}{5.7 \mu\text{s}} = 333 \frac{\text{mV}}{\mu\text{s}} \quad (37)$$

To achieve a 44.74-mV/ μs compensation slope, R_{CSF} is calculated with 式 38. In this design, R_{RAMP} is selected as 24.9 k Ω , a 3.8-k Ω resistor was selected for R_{CSF} .

$$R_{CSF} = \frac{R_{RAMP}}{\frac{S_{OSC}}{S_e} - 1} \quad (38)$$

9.2.2.10.3 Open-Loop Gain

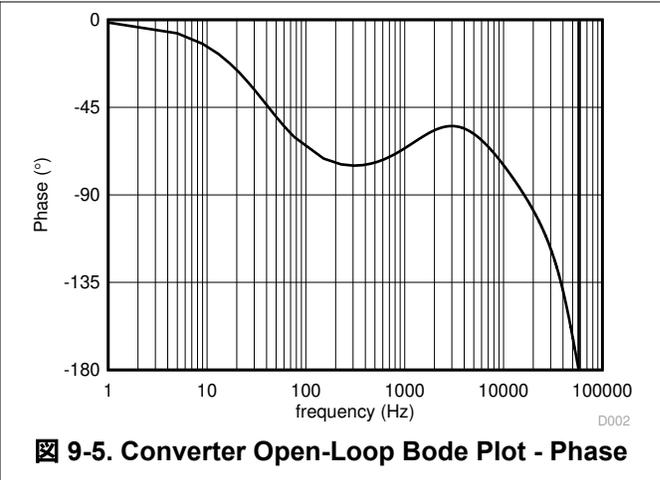
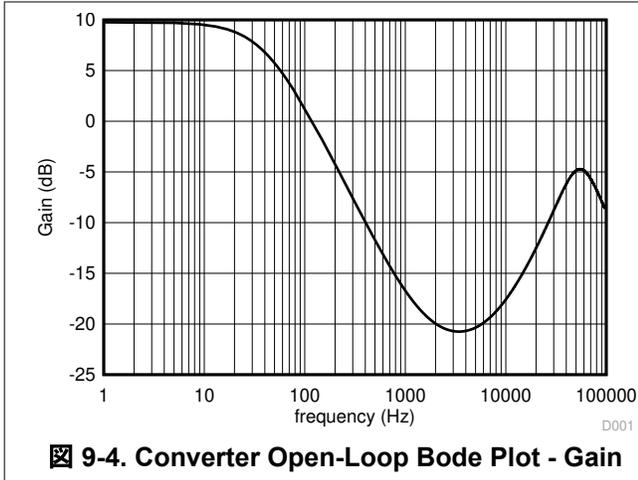
Once the power stage poles and zeros are calculated and the slope compensation is determined, the power stage open-loop gain and phase of the CCM flyback converter can be plotted as a function of frequency. The power stage transfer function can be characterized with 式 39.

$$H_{OPEN}(s) = G_0 \times \frac{\left(1 + \frac{s(f)}{\omega_{ESRz}}\right) \times \left(1 - \frac{s(f)}{\omega_{RHPz}}\right)}{1 + \frac{s(f)}{\omega_{P1}}} \times \frac{1}{1 + \frac{s(f)}{\omega_{P2} \times Q_P} + \frac{s(f)^2}{(\omega_{P2})^2}} \quad (39)$$

The bode for the open-loop gain and phase can be plotted by using 式 40.

$$\text{Gain}_{OPEN}(s) = 20 \times \log(|H_{OPEN}(s)|) \quad (40)$$

See [图 9-4](#) and [图 9-5](#).



9.2.2.10.4 Compensation Loop

The design of the compensation loop involves selecting the appropriate components so that the required gain, poles, and zeros can be designed to result in a stable system over the entire operating range. There are three distinct portions of the loop: the TL431, the opto-coupler, and the error amplifier. Each of these stages combines with the power stage to result in a stable robust system.

For good transient response, the bandwidth of the finalized design must be as large as possible. The bandwidth of a CCM flyback, f_{BW} , is limited to $\frac{1}{4}$ of the RHP zero frequency, or approximately 1.77 kHz using 式 41.

$$f_{BW} = \frac{f_{RHPz}}{4} \quad (41)$$

The gain of the open-loop power stage at f_{BW} can be calculated using 式 40 or can be observed on the Bode plot (9-4) and is equal to -19.55 dB and the phase at f_{BW} is equal to -58° .

The secondary side portion of the compensation loop begins with establishing the regulated steady state output voltage. To set the regulated output voltage, a TL431 adjustable precision shunt regulator is ideally suited for use on the secondary side of isolated converters due to its accurate voltage reference and internal op-amp. The resistors used in the divider from the output terminals of the converter to the TL431 REF pin are selected based upon the desired power consumption. Because the REF input current for the TL431 is only $2 \mu\text{A}$, selecting the resistors for a divider current (I_{FB_REF}) of 1 mA results in minimal error. The top divider resistor (R_{FBU}) is calculated:

$$R_{FBU} = \frac{V_{OUT} - REF_{TL431}}{I_{FB_REF}} \quad (42)$$

The TL431 reference voltage (REF_{TL431}) has a typical value of 2.495 V. A 9.53-k Ω resistor is chosen for R_{FBU} . To set the output voltage to 12 V, 2.49 k Ω is used for R_{FBB} .

$$R_{FBB} = \frac{REF_{TL431}}{V_{OUT} - REF_{TL431}} \times R_{FBU} \quad (43)$$

For good phase margin, a compensator zero (f_{COMPz}) is required and should be placed at 1/10th the desired bandwidth:

$$f_{COMPz} = \frac{f_{BW}}{10} \quad (44)$$

$$\omega_{\text{COMPz}} = 2 \times \pi \times f_{\text{COMPz}} \quad (45)$$

With this converter, f_{COMPz} should be set at approximately 177 Hz. A series resistor (R_{COMPz}) and capacitor (C_{COMPz}) placed across the TL431 cathode to REF sets the compensator zero location. Setting C_{COMPz} to 0.01 μF , R_{COMPz} is calculated:

$$R_{\text{COMPz}} = \frac{1}{\omega_{\text{COMPz}} \times C_{\text{COMPz}}} \quad (46)$$

Using a standard value of 88.7 k Ω for R_z and a 0.01 μF for C_z results in a zero placed at 179 Hz.

In [Figure 9-3](#), R_{TLbias} provides cathode current to the TL431 from the regulated voltage provided from the Zener diode (D_{REG}). For robust performance, 10 mA is provided to bias the TL431 by way of the 10-V Zener and a 1-k Ω resistor is used for R_{TLbias} .

The gain of the TL431 portion of the compensation loop is calculated with [Equation 47](#).

$$G_{\text{TL431}}(s) = \left(R_{\text{COMPz}} + \frac{1}{s(f) \times C_{\text{ZCOMPz}}} \right) \times \frac{1}{R_{\text{FBU}}} \quad (47)$$

A compensation pole is required at the frequency of right half plane zero or the ESR zero, whichever is lowest. Based previous the analysis, the right half plane zero (f_{RHPz}) is located at 7.07 kHz and the ESR zero (f_{ESRz}) is at 1.68 kHz; therefore, for this design, the compensation pole must be put at 1.68 kHz. The opto-coupler contains a parasitic pole that is difficult to characterize over frequency so the opto-coupler is set up with a pull-down resistor (R_{OPTO}) equal to 1 k Ω , which moves the parasitic opto-coupler pole further out and beyond the range of interest for this design.

The required compensation pole can be added to the primary side error amplifier using R_{COMPp} and C_{COMPp} . Choosing R_{COMPp} as 10 k Ω , the required value of C_{COMPp} is determined using [Equation 48](#).

$$C_{\text{COMPp}} = \frac{1}{2 \times \pi \times f_{\text{ESRz}} \times R_{\text{COMPp}}} = 9.46 \text{ nF} \quad (48)$$

A 10-nF capacitor is used for C_{COMPp} setting the compensation pole at 1.59 kHz.

Adding a DC gain to the primary-side error amplifier may be required to obtain the required bandwidth and helps to adjust the loop gain as needed. Using 4.99 k Ω for R_{FBG} sets the DC gain on the error amplifier to 2. At this point the gain transfer function of the error amplifier stage ($G_{\text{EA}}(s)$) of the compensation loop can be characterized using [Equation 49](#).

$$G_{\text{EA}}(s) = \left(\frac{R_{\text{COMPp}}}{R_{\text{FBG}}} \right) \times \left(\frac{1}{1 + s(f) \times C_{\text{COMPp}} \times R_{\text{COMPp}}} \right) \quad (49)$$

Using an opto-coupler whose current transfer ratio (CTR) is typically at 100% in the frequency range of interest so that $\text{CTR} = 1$, the transfer function of the opto-coupler stage ($G_{\text{OPTO}}(s)$) is found using [Equation 50](#).

$$G_{\text{OPTO}}(s) = \frac{\text{CTR} \times R_{\text{OPTO}}}{R_{\text{LED}}} \quad (50)$$

The bias resistor (R_{LED}) to the internal diode of the opto-coupler and the pull-down resistor on the opto emitter (R_{OPTO}) sets the gain across the isolation boundary. R_{OPTO} has already been set to 1 k Ω but the value of R_{LED} has not yet been determined.

The total closed loop gain ($G_{TOTAL}(s)$) is the combination of the open-loop power stage ($H_o(s)$), the opto gain ($G_{OPTO}(s)$), the error amplifier gain ($G_{EA}(s)$), and the gain of the TL431 stage ($G_{TL431}(s)$), as shown in 式 51.

$$G_{TOTAL}(s) = |H_{OPEN}(s)| \times |G_{OPTO}(s)| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (51)$$

The required value for R_{LED} can be selected to achieve the desired crossover frequency (f_{BW}). By setting the total loop gain equal to 1 at the desired crossover frequency and rearranging 式 51, the optimal value for R_{LED} can be determined, as shown in 式 52.

$$R_{LED} \leq |H_{OPEN}(s)| \times |CTR \times C_{OPTO}| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (52)$$

A 1.3-kΩ resistor suits the requirement for R_{LED} .

Based on the compensation loop structure, the entire compensation loop transfer function is written as 式 53.

$$G_{CLOSED}(s) = H_{OPEN}(s) \times \left(\frac{CTR \times R_{OPTO}}{R_{LED}} \right) \times \left(\frac{R_{COMPp}}{R_{FBG}} \right) \times \left(\frac{1}{1 + (s \times C_{COMPp} \times R_{COMPp})} \right) \times \left(\frac{R_{COMPz} + \left(\frac{1}{s \times C_{COMPz}} \right)}{R_{FBU}} \right) \quad (53)$$

The final closed-loop bode plots are shown in 图 9-6 and 图 9-7. The converter achieves a crossover frequency of approximately 1.8 kHz and has a phase margin of approximately 67°.

TI recommends checking the loop stability across all the corner cases including component tolerances to ensure system stability.

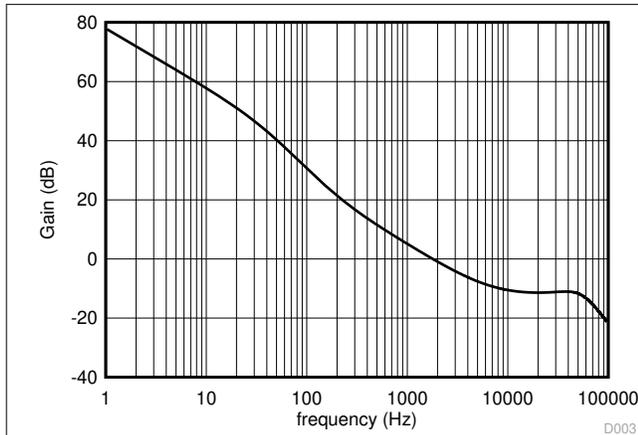


图 9-6. Converter Closed-Loop Bode Plot – Gain

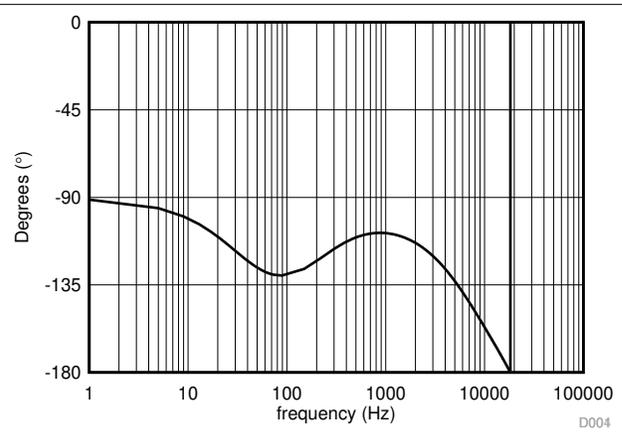
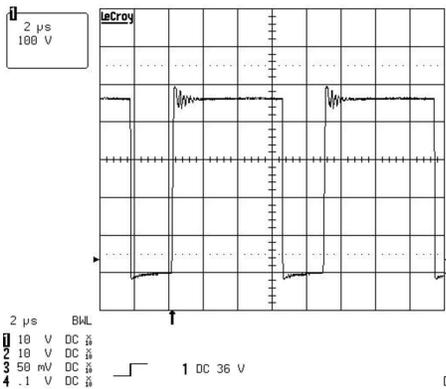
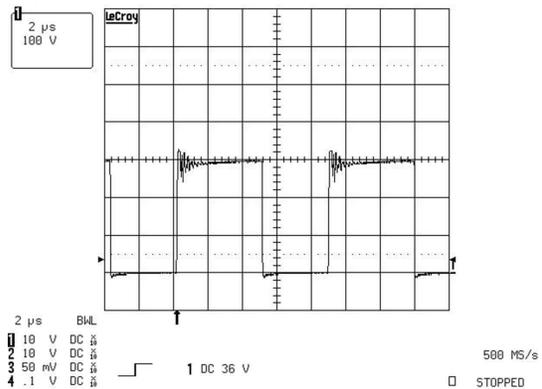


图 9-7. Converter Closed-Loop Bode Plot – Phase

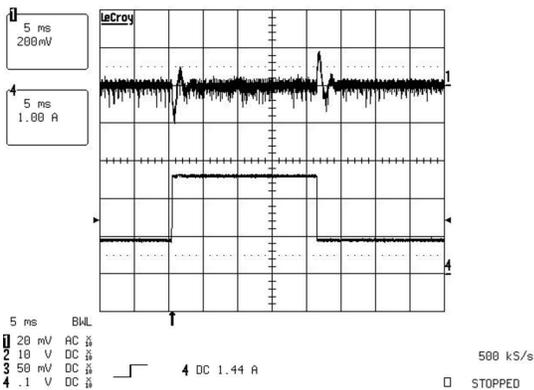
9.2.3 Application Curves



9-8. Primary Side MOSFET Drain to Source Voltage at 240-V AC Input (100 V/div)

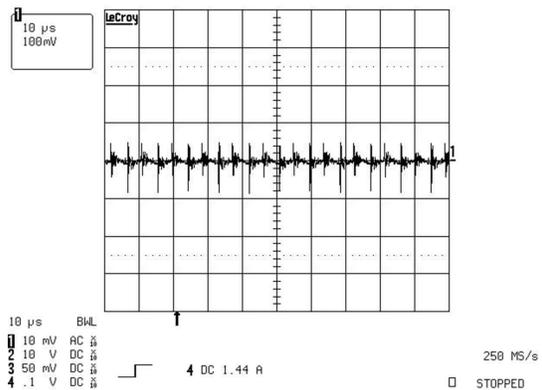


9-9. Primary Side MOSFET Drain to Source Voltage at 120-V AC Input (100 V/div)

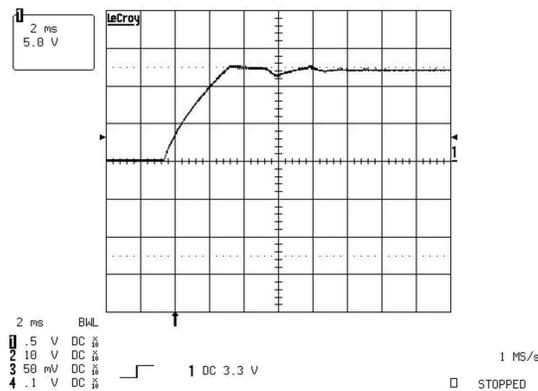


CH1: Output Voltage AC Coupled, 200 mV/div
CH4: Output Current, 1 A/div

9-10. Output Voltage During 0.9-A to 2.7-A Load Transient



9-11. Output Voltage Ripple at Full Load (100 mV/div)



9-12. Output Voltage Behavior at Full Load Start-up (5 V/div)

9.3 Power Supply Recommendations

The absolute maximum supply voltage is 30 V for UCC28C52, including any transients that may be present. If this voltage is exceeded, device damage is likely.

Because no clamp is included in the device, the supply pin must be protected from external sources which could exceed the 30-V level.

To prevent false triggering due to leading edge noises, an RC current sense filter may be required on CS. Keep the time constant of the RC filter well below the minimum on-time pulse width.

To prevent noise problems with high-speed switching transients, bypass VREF to ground with a ceramic capacitor close to the IC package. A minimum of 0.1- μ F ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Precautions

Careful layout of the printed board is a necessity for high-frequency power supplies. As the device-switching speeds and operating frequencies increase, the layout of the converter becomes increasingly important.

This 8-pin device has only a single ground for the logic and power connections. This forces the gate-drive current pulses to flow through the same ground that the control circuit uses for reference. Thus, the interconnect inductance must be minimized as much as possible. One implication is to place the device (gate driver) circuitry close to the MOSFET it is driving. This can conflict with the need for the error amplifier and the feedback path to be away from the noise generating components.

The single most critical item in a PWM controlled printed-circuit board layout is the placement of the timing capacitor. While both the supply and reference bypass capacitor locations are important, the timing capacitor placement is far more critical. Any noise spikes on the C_{CT} waveform due to lengthy printed circuit trace inductance or pick-up noise from being in proximity to high power switching noise causes a variety of operational problems. Dilemmas vary from incorrect operating frequency caused by pre-triggering the oscillator due to noise spikes to frequency jumping with varying duty cycles, also caused by noise spikes. The placement of the timing capacitor must be treated as the most important layout consideration. Keep PC traces as short as possible to minimize added series inductance.

9.4.1.2 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from EMI and other noise sources is the more critical of the two. If possible, run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

9.4.1.3 Bypass Capacitors

When using a low value ceramic bypass capacitor, it must be placed as close to the VDD pin of the device as possible. This eliminates as much trace inductance effects as possible and give the internal device rail a cleaner voltage supply. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

9.4.1.4 Compensation Components

For best stability, external compensation components must be placed close to the IC. Keep FB lead length as short as possible and FB stray capacitance as small as possible. TI recommends surface mount components here as well for the same reasons discussed for the filter capacitors. These must not be placed very close to traces with high switching noise.

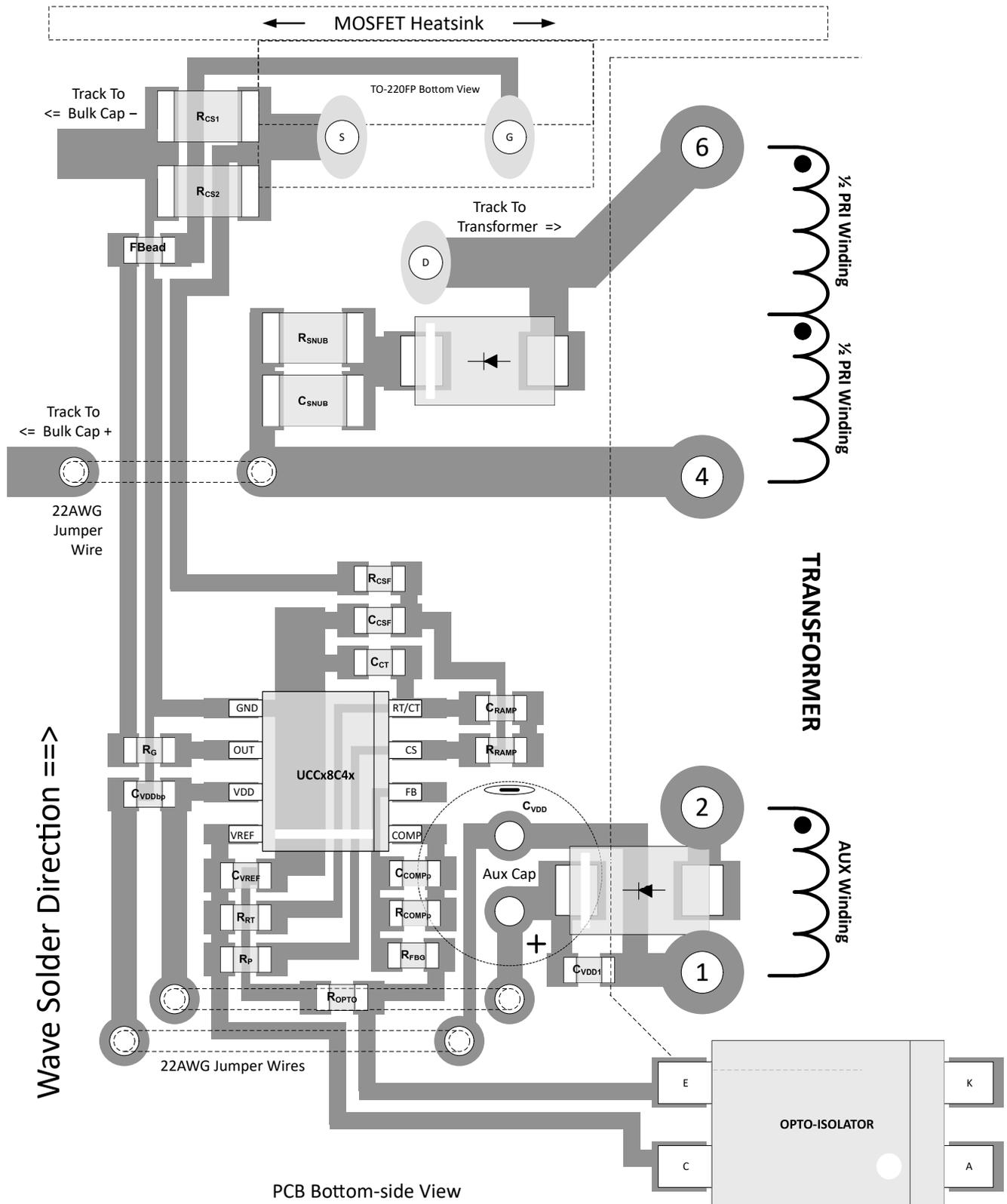
9.4.1.5 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode must be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This also reduces lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode, if applicable, must be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane, where the power traces and components are, and the signal plane, where the feedback and compensation and components are, for improved performance. On multi-layer boards the use of vias is required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace conducts a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is ON and one when the switch is OFF. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

9.4.2 Layout Example



9-13. UCCx8C4x Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

[UC384x Provides Low-Cost Current-Mode Control \(SLUA143\)](#)

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28C50DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C50
UCC28C50DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C50
UCC28C50DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C50
UCC28C50DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C50
UCC28C51DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C51
UCC28C51DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C51
UCC28C51DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C51
UCC28C51DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C51
UCC28C52DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C52
UCC28C52DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C52
UCC28C52DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C52
UCC28C52DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C52
UCC28C53DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C53
UCC28C53DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C53
UCC28C53DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C53
UCC28C53DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C53
UCC28C54DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C54
UCC28C54DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C54
UCC28C54DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C54
UCC28C54DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C54
UCC28C55DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C55
UCC28C55DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C55
UCC28C55DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C55
UCC28C55DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C55
UCC28C56HDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C56H
UCC28C56HDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C56H
UCC28C56LDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C56L
UCC28C56LDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C56L
UCC28C57HDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C57H

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28C57HDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C57H
UCC28C57LDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C57L
UCC28C57LDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C57L
UCC28C58DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C58
UCC28C58DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C58
UCC28C59DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C59
UCC28C59DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C59
UCC38C50DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C50
UCC38C50DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C50
UCC38C51DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C51
UCC38C51DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C51
UCC38C52DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C52
UCC38C52DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C52
UCC38C53DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	3C53
UCC38C53DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	3C53
UCC38C53DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C53
UCC38C53DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C53
UCC38C54DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C54
UCC38C54DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C54
UCC38C55DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C55
UCC38C55DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C55

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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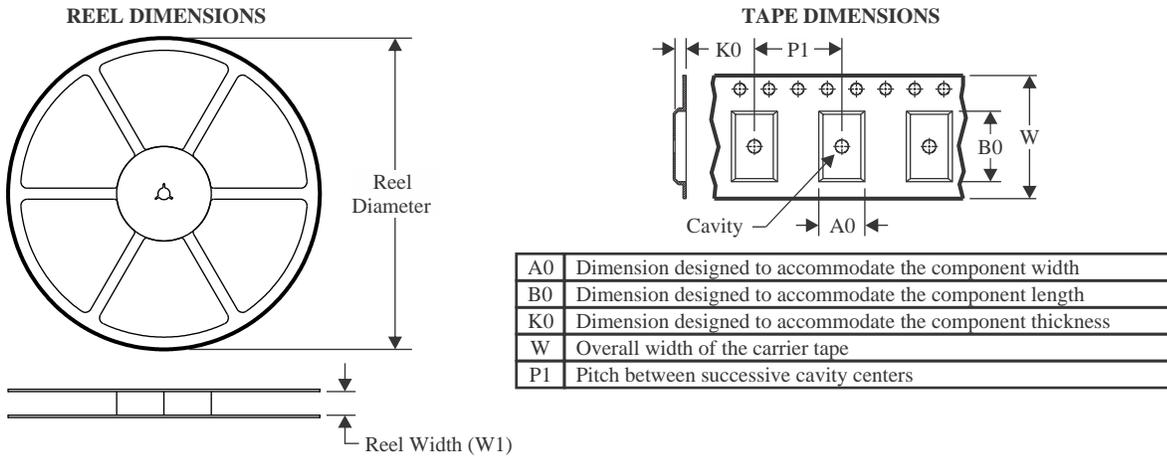
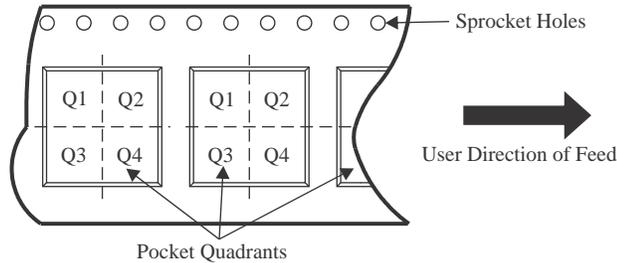
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC28C50, UCC28C51, UCC28C52, UCC28C53, UCC28C54, UCC28C55, UCC28C56H, UCC28C56L, UCC28C57H, UCC28C57L, UCC28C58, UCC28C59 :

- Automotive : [UCC28C50-Q1](#), [UCC28C51-Q1](#), [UCC28C52-Q1](#), [UCC28C53-Q1](#), [UCC28C54-Q1](#), [UCC28C55-Q1](#), [UCC28C56H-Q1](#), [UCC28C56L-Q1](#), [UCC28C57H-Q1](#), [UCC28C57L-Q1](#), [UCC28C58-Q1](#), [UCC28C59-Q1](#)

NOTE: Qualified Version Definitions:

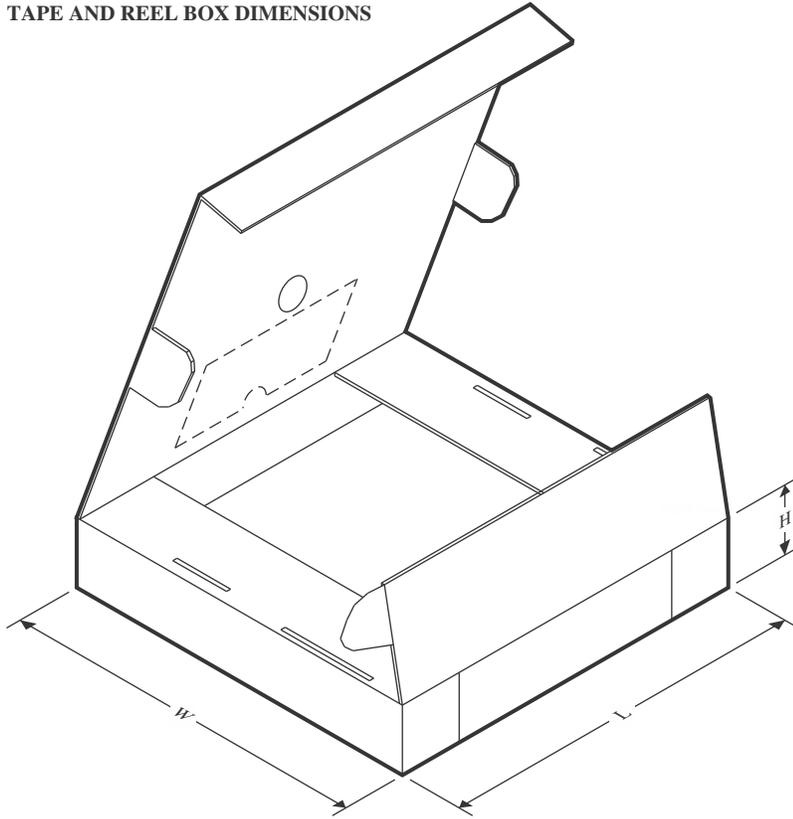
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28C50DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C51DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C51DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C52DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C52DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C53DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C53DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C54DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C54DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C55DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C55DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C56HDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C56LDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C57HDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C57LDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

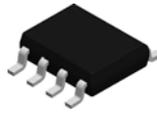
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28C58DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C59DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C51DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C52DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C53DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C53DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C54DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C55DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28C50DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C50DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C51DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C51DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C52DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C52DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C53DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C53DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C54DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C54DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C55DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C55DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C56HDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C56LDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C57HDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C57LDR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C58DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C59DR	SOIC	D	8	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC38C50DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C51DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C52DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C53DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC38C53DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C54DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C55DR	SOIC	D	8	2500	353.0	353.0	32.0

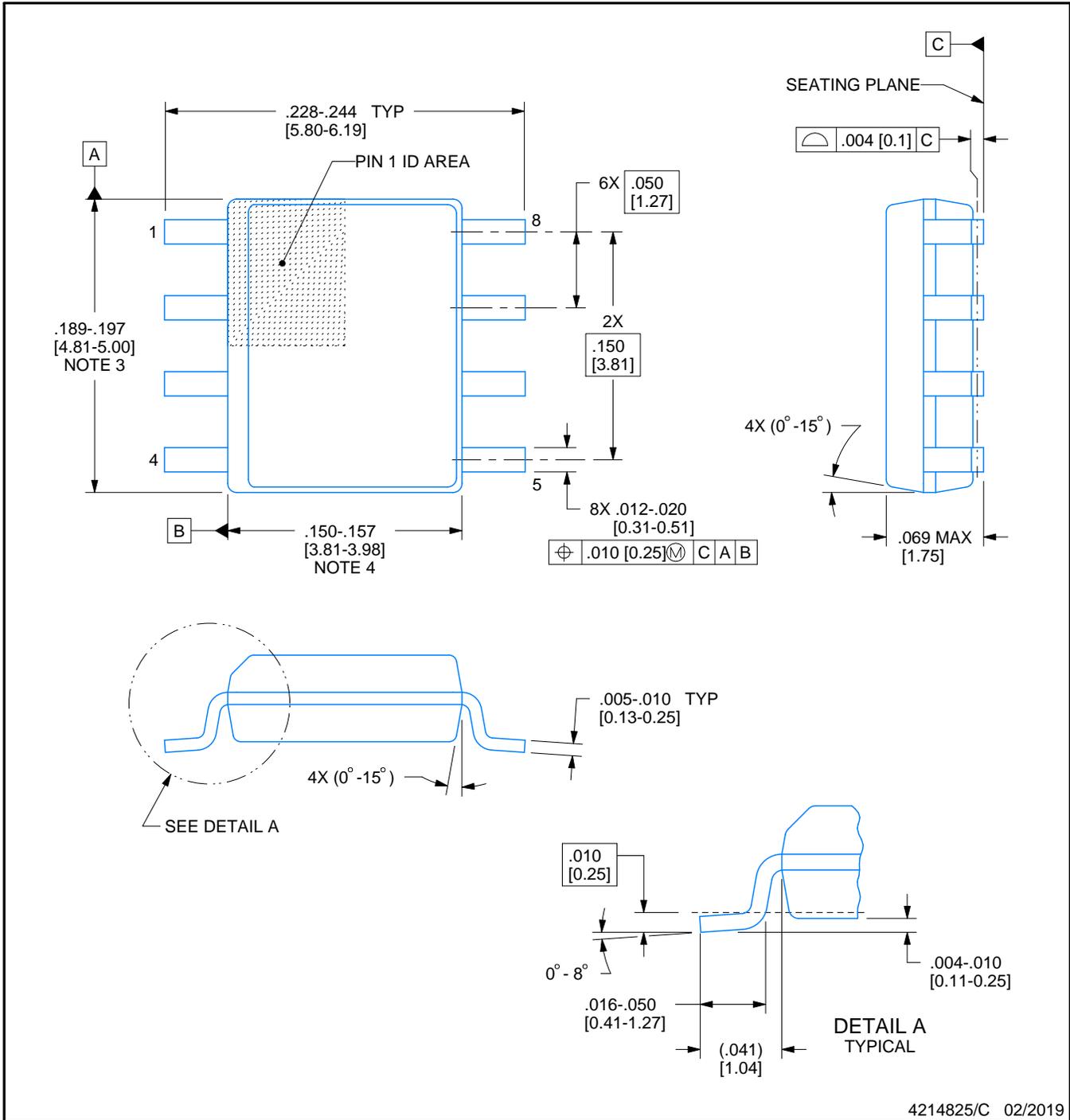


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

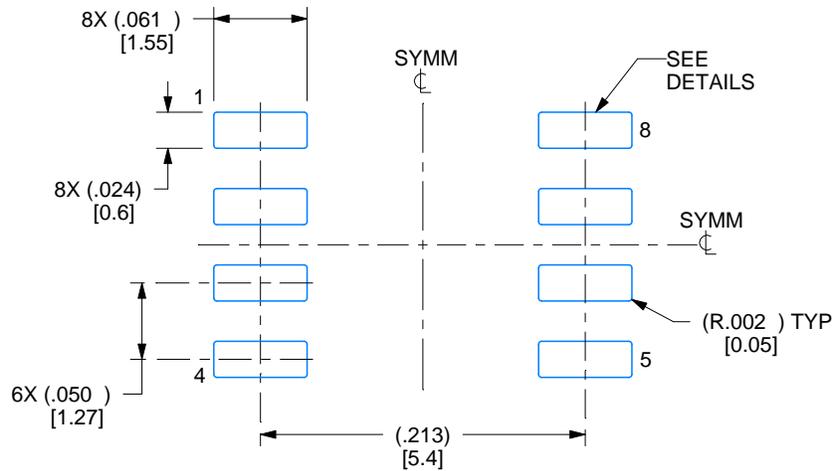
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

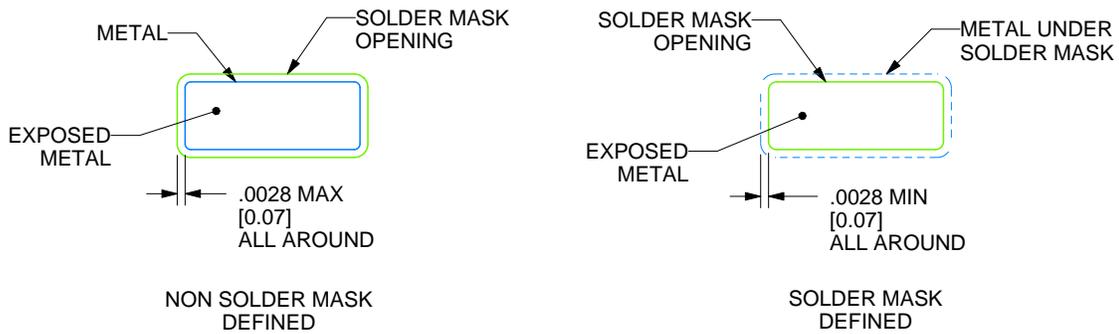
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

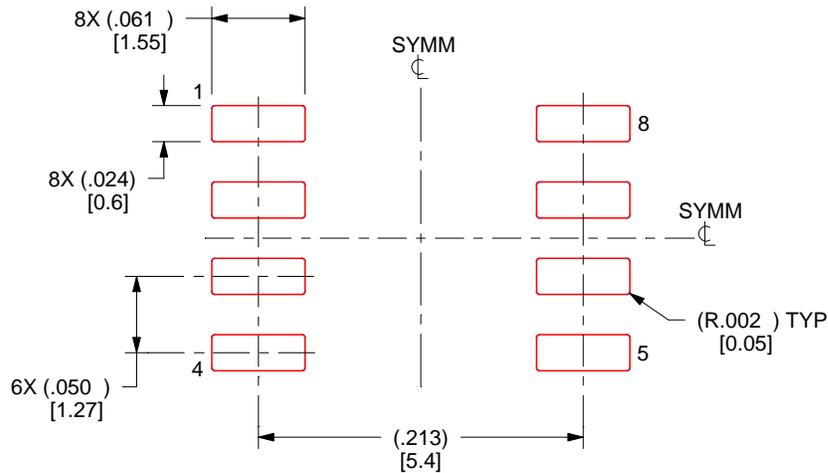
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

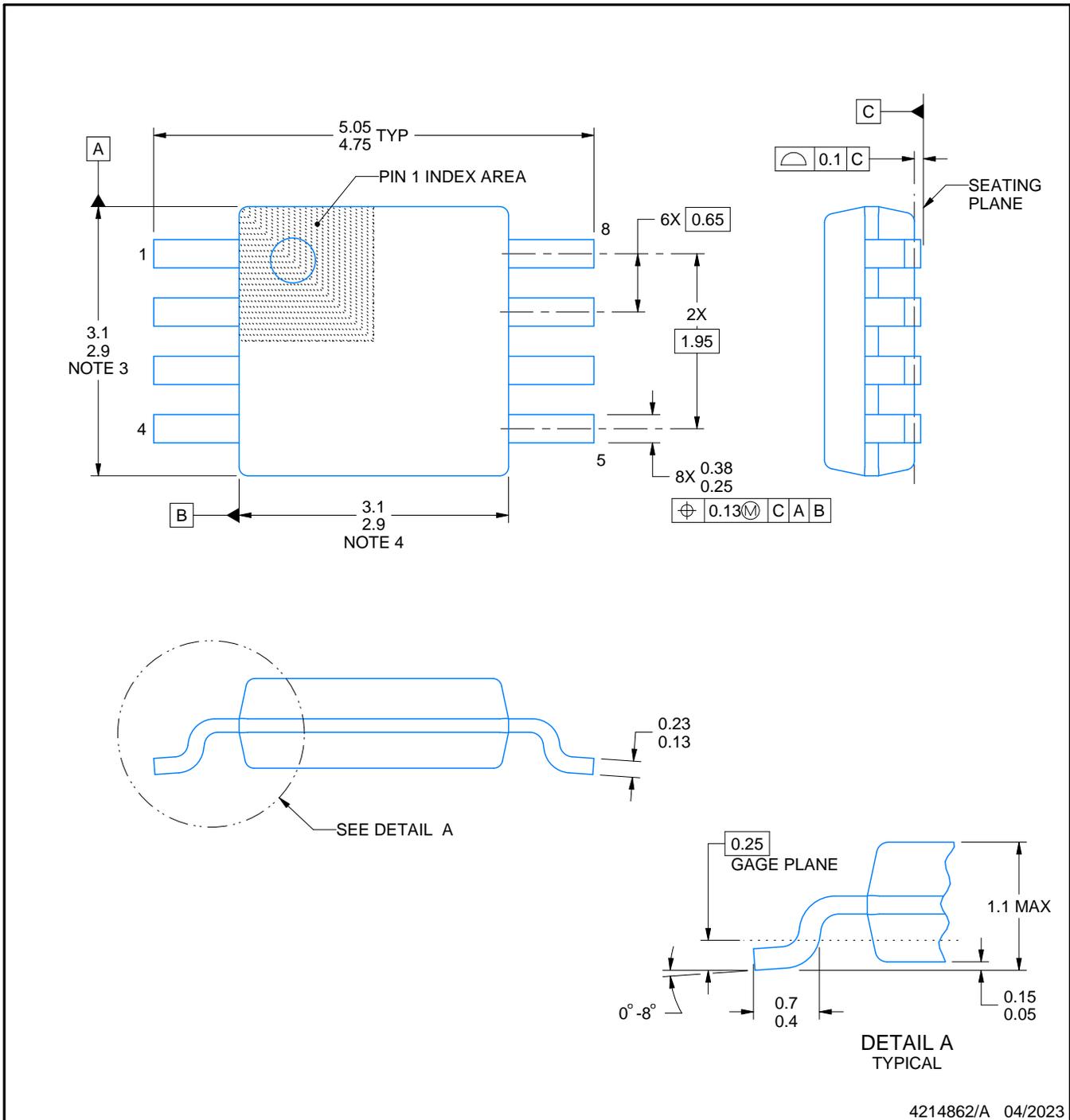
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

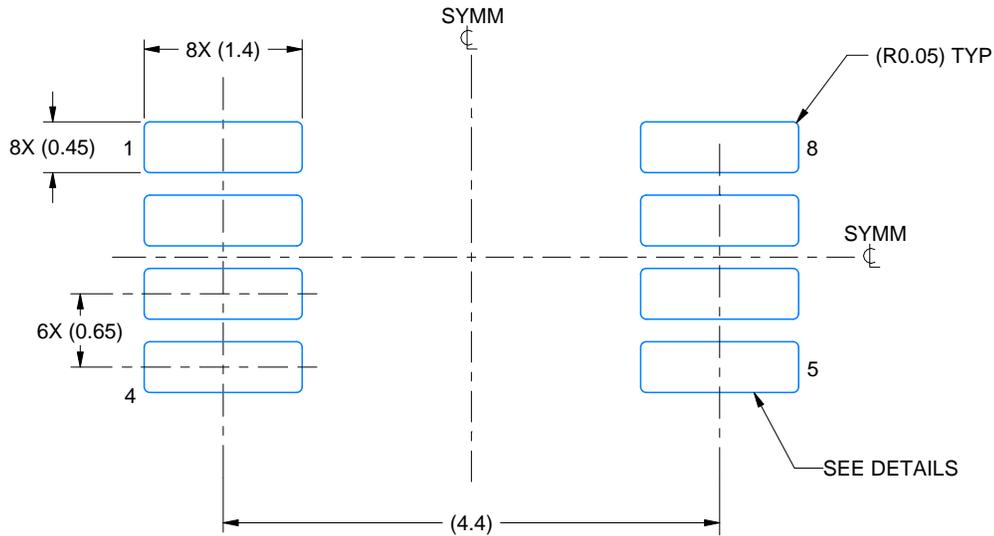
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

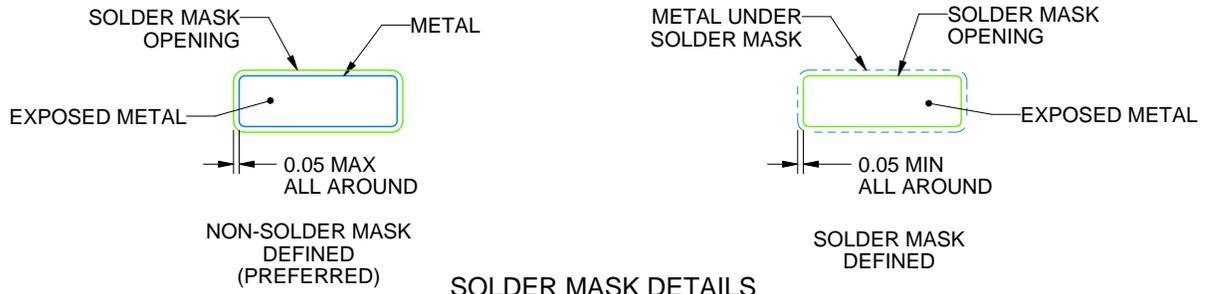
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

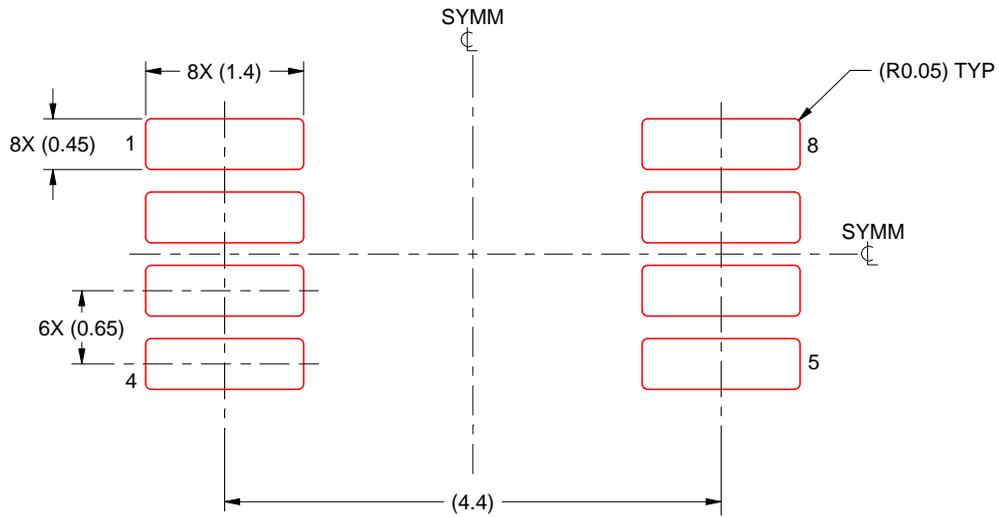
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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