UCC2897A Advanced Current-Mode Active-Clamp PWM Controller

1 Features

- Low-output jitter
- Soft-stop shutdown of MAIN and AUX
- 110-V input startup function
- Ideal for active-clamp, reset-forward, flyback and synchronous rectifier uses
- Provides complementary auxiliary driver with programmable dead time (Turn-On Delay) between AUX and MAIN switches
- Peak current-mode control with 0.5-V cycle-by-cycle current limiting
- TrueDrive™ 2-A Sink, 2-A source outputs
- Trimmed internal-bandgap reference for accurate line UV and line OV threshold
- Programmable slope compensation
- High-performance 1-MHz synchronizable oscillator with internal timing capacitor
- Precise programmable maximum duty cycle
- PB-free lead finish package

2 Applications

- High-efficiency DC-to-DC power supplies
- Server power, 48-V telecom, datacom, and 42-V automotive applications

3 Description

The UCC2897A PWM controller simplifies implementation of the various active clamp or reset and synchronous rectifier switching power topologies.

The UCC2897A is a peak current-mode fixed-frequency high-performance pulse-width modulator. The controller includes the logic and the drive capability for the P-channel auxiliary switch along with a simple method of programming the critical delays for proper active-clamp operation.

Features include an internal programmable slope compensation circuit, precise D_{MAX} limit, and a synchronizable oscillator with an internal-timing capacitor. An accurate line-monitoring function also programs the ON and OFF transitions of the converter with regard to the bulk input voltage, VIN.

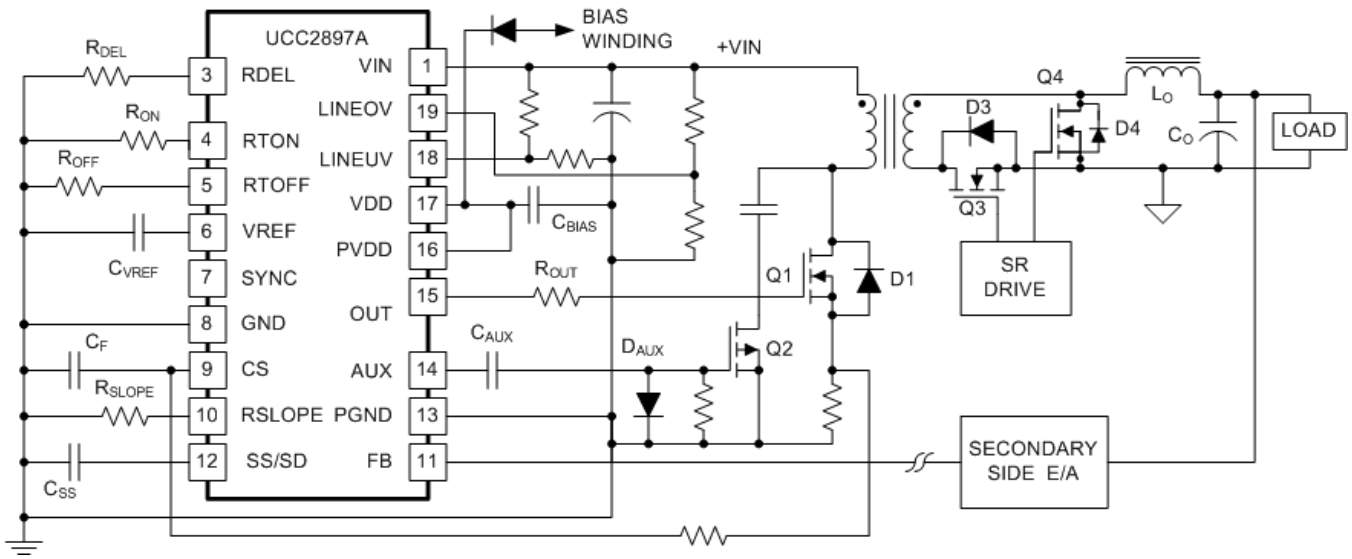
The UCC2897A adds a second-level hiccup-mode current-sense threshold, bi-directional synchronization and input-overvoltage protection functionalities. The UCC2897A is offered in 20-pin TSSOP (PW) and 20-pin QFN (RGP) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2897A	TSSOP (20)	6.60 mm x 6.60 mm
	VQFN (20)	4.15 mm x 4.15 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2017) to Revision G — **Page**

- Changed Modified Typical Application diagram ... 1
- Changed Updated the RDEL1 calculation ... 31
- Changed Updated the RDEL2 calculation ... 31

Changes from Revision E (April 2015) to Revision F — **Page**

- Changed Equation 1 From; $t_{DEL2} = 11.1 \times 10^{-2}$ To: $t_{DEL2} = 11.1 \times 10^{-12}$ ... 13
- Changed Equation 15 From: $Q_{G(main)} \times Q_{G(aux)}$ To: $Q_{G(main)} + Q_{G(aux)}$ ... 31

Changes from Revision D (July 2009) to Revision E — **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Changed *Thermal Resistance Information* table to new Thermal Information layout and updated PW and RGP package data ... 3
- Added R_{ON} and R_{OFF}, R_{DEL} test conditions to D_{MAX} parameter in the PWM section of the *Electrical Characteristics* table ... 7
- Changed Oscillator equations in Step 1 for R_{ON} and R_{OFF} ... 30

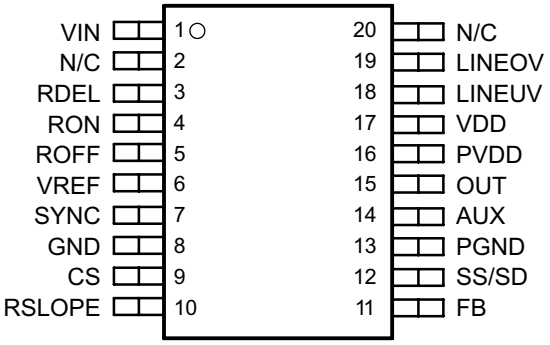
5 Device Options

APPLICATION	AUX OUTPUT POLARITY	CYCLE-BY-CYCLE CS THRESHOLD	HICCUP MODE CS THRESHOLD	110-V HV JFET START-UP CIRCUIT	PART NUMBER	
					TSSOP-20 (PW)(1)	QFN-20 (RGP)(2)
DC/DC	P-Channel	0.5 V	0.75 V	Yes	UCC2897APW	UCC2897ARGP

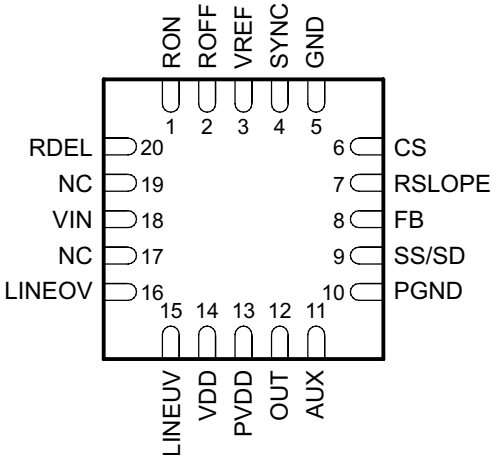
(1) The PW package is available taped and reeled. Add R suffix to the device type (for example: UCC2897APWR) to order quantities of 2,000 devices per reel. Bulk quantities are 70 units per tube. The RGP package is available in two options of tape and reel. The RGPT is orderable in small reels of 250 (for example: UCC2897ARGPT); the RGPR contains 3000 pieces per reel (for example: UCC2897ARGPR).
(2) The TSSOP-20 (PW) and QFN-20 (RGP) package uses Pb-free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature and compatible with either lead-free, tin, or lead soldering operations.

6 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



RGP Package
20-Pin VQFN
Bottom View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	VQFN		
AUX	14	11	O	This output drives the auxiliary-clamp MOSFET which turns on when the main PWM-switching device turns off. The AUX pin directly drives the auxiliary switch with a 2-A source turn-on current and a 2-A sink turn-off current.
CS	9	6	I	This pin senses the peak current utilized for current-mode control and for current-limiting functions. The peak signal is applied to this pin before pulse-by-pulse current limiting activates and is approximately 0.5 V.
FB	11	8	I	This pin brings the error signal from an external optocoupler or error amplifier into the PWM-control circuitry. Often, there is a resistor tied from FB to VREF, and an optocoupler pulls the control pin closer to GND to reduce the pulse width of the OUT output driving the main-power switch of the converter.
GND	8	5		This pin serves as the fundamental-analog ground for the PWM-control circuitry. This pin is connected to PGND directly at the device.
LINEOV	19	16	I	The LINEOV pin is an input pin of voltage comparator with programmable hysteresis and 1.27-V threshold, providing LINE overvoltage or other functions.
LINEUV	18	15	I	This pin provides a means to accurately enable/disable the power converter stage by monitoring the bulk input voltage or another parameter. When the circuit initially starts (or restarts from a disabled condition), a rising input on LINEUV enables the outputs when the threshold of 1.27 V is crossed. After the circuit is enabled, a falling LINEUV signal disables the outputs when the same threshold is reached. The hysteresis between the two levels is programmed using an internal current source.
OUT	15	12	O	This output pin drives the main PWM switching element MOSFET in an active-clamp controller. The OUT pin directly drives an N-channel device with a 2-A source turnon-current and a 2-A sink turnoff-current. TI recommends connecting a 10-kΩ resistor from this pin to PGND pin.
PGND	13	10		The PGND should serve as the current return for the high-current output drivers OUT and AUX. Ideally, the current path from the outputs to the switching devices, and back would be as short as possible, and enclose a minimal-loop area.
PVDD	16	13	I	The PVDD pin is the supply pin for the power devices. It is separated internally from the VDD pin.
RSLOPE	10	7	I	A resistor connected from this pin to GND programs an internal current source that sets the slope-compensation ramp for the current-mode control-circuitry.
RTDEL	3	20	I	A resistor from this pin to GND programs the turn-on delay of the two gate-drive outputs to accommodate the resonant transitions of the active-clamp power converter.
ROFF	5	2	I	A resistor connected from this pin to GND programs an internal-current source that discharges the internal timing-capacitor.
RON	4	1	I	A resistor connected from this pin to GND programs an internal-current source that charges the internal timing-capacitor.
SS/SD	12	9	I	A capacitor from SS/SD to ground is charged by an internal-current source of IRON to program the soft-start interval for the controller. During a fault condition this capacitor is discharged by a current source equal to I_{RON}.
SYNC	7	4	I	The SYNC pin serves as a bidirectional-synchronization input for the internal oscillator. The synchronization function is implemented such that the user-programmable maximum duty-cycle (set by RON and ROFF) remains accurate during synchronized operation. This pin is left open when not in use. The external capacitance is minimized. No capacitors are connected to this pin.
VDD	17	14	I	The VDD pin is the power supply for the device. There should be a 1-μF capacitor directly from VDD to PGND. The capacitor value should be at least 10-times larger than that on VREF. PGND and GND are connected externally and directly from PGND pin to GND pin. (To make a full design of capacitance on VDD pin, please refer to, Application Note: *Understanding and Designing an Active Clamp Current Mode Controlled Converter* (SLUA535), section 7.3)
VIN	1	18	I	This pin is connected to the input-power rail directly. Inside the device, a high-voltage start-up device is utilized to provide the start-up current for the controller until a bootstrap-type bias rail becomes available.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	VQFN		
VREF	6	3	O	The VREF pin is the 5-V reference voltage that is used for an external load of up to 5 mA. Since this reference provides the supply rail for internal logic, VREF is bypassed to AGND as close as possible to the device. The VREF bias profile is not always monotonic before VDD reaches 5 V.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Line input voltage		120	V
V_{DD}	Supply voltage		16.5	
	Analog inputs, FB, CS, SYNC, LINEOV, LINEUV	–0.3	(V_{REF}+ 0.3)	
I_{O_SOURCE}	Output source current (peak) OUT AUX		2.5	A
I_{O_SINK}	Output sink current (peak) OUT AUX		–2.5	
T_J	Operating junction temperature range	–55	150	°C
T_{sol}	Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds		300	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Line input voltage	18		110	V
V_{DD}	Supply voltage	8.5	12	16	V
V_{DD}	Supply bypass capacitance	1			µF
R_{ON} = R_{OFF}	Timing resistance (for 250-kHz operation)		75		kΩ
T_J	Operating junction temperature	–40		125	°C
C_{REF}	Reference bypass capacitance	0.1			µF

7.4 Thermal Information

THERMAL METRIC(1)		UCC2897A		UNIT
		QFN (RGP)	TSSOP (PW)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	91.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.3	26.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.2	42.6	
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.1	
ψ_{JB}	Junction-to-board characterization parameter	9.1	42.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{DD} = 12 V(1), 1-µF capacitor for VDD to GND, 0.01-µF capacitor from VREF to GND, R_{ON} = R_{OFF} = 75 kΩ, R_{SLOPE} = 50 kΩ, –40°C ≤ T_A = T_J ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
$I_{STARTUP}$	Start-up current	V_{DD} < V_{UVLO}		300	500	µA
I_{DD}	Operating supply current(1)(2)	V_{FB} = 0 V, V_{CS} = 0V, Outputs not switching		2	3	mA
HIGH-VOLTAGE BIAS						
I_{DD-ST}	VDD startup current	Current available from VDD during startup, T_A = –40°C to +85°C, V_{IN} = 36 V(3)	4	11		mA
I_{VIN}	JFET leakage current	VIN = 120 V; VDD = 14 V			75	µA
UNDERVOLTAGE LOCKOUT						
UVLO	Start threshold voltage		12.2	12.7	13.2	V
	Minimum operating voltage after start		7.6	8	8.4	
	Hysteresis		4.4	4.7	5	
LINE MONITOR						
V_{LINEUV}	Line UV voltage threshold		1.243	1.268	1.294	V
$I_{LINEUVHYS}$	Line UV hysteresis current		–11.5	–13	–14.5	µA
V_{LINEOV}	Line OV voltage threshold		1.243	1.268	1.294	V
$I_{LINEOVHYS}$	Line OV hysteresis current		–11.5	–13	–14.5	µA
Soft-Start						
I_{SSC}	SS charge current	R_{ON} = 75 kΩ(4)	–10.5	–14.5	–18.5	µA
I_{SSD}	SS discharge current	R_{ON} = 75 kΩ(4)	10.5	14.5	18.5	
$V_{SS/SD}$	Discharge/shutdown threshold voltage		0.4	0.5	0.6	V
VOLTAGE REFERENCE						
V_{REF}	Reference voltage	T_J = 25°C	4.85	5	5.15	V
V_{REF}	Reference voltage	0 A < I_{REF} < 5 mA, over temperature	4.75	5	5.25	
I_{SC}	Short circuit current	REF = 0 V, T_J = 25°C	–20	–11	–8	mA
INTERNAL SLOPE COMPENSATION						

(1) Set VDD above the start threshold before setting at 12 V.
(2) Does not include current of the external oscillator network.
(3) The power supply starts with $I_{DD–ST}$ load on VDD, the part starts up with no load up to 125°C. For more information see the section for VIN and VDD
(4) I_{SSC} and $I_{SS/SD}$ are directly proportional to I_{RON}. See Equation 8.

Electrical Characteristics (continued)

V_{DD} = 12 V(1), 1-µF capacitor for VDD to GND, 0.01-µF capacitor from VREF to GND, R_{ON} = R_{OFF} = 75 kΩ, R_{SLOPE} = 50 kΩ, –40°C ≤ T_A = T_J ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
m	Slope	FB = High	–10%	R_{CS} / R_{SLOPE}	+10%	
OSCILLATOR						
f_{OSC}	Oscillator frequency	T_J = 25°C	237	250	265	kHZ
		–40°C < T_J < 125°C; 8.5 V < V_{DD} < 14.5 V	225		270	
V_{P_P}	Oscillator amplitude (peak-to-peak)			2		V
SYNCHRONIZATION						
	SYNC input high voltage		3			V
	SYNC input low voltage				1.6	
	SYNC pull down output current			600		µA
	SYNC pull up output current			–600		
	SYNC output pulse width			150		ns
t_{DEL}	SYNC-to-output delay			50		
PWM(5)						
D_{MAX}	Maximum duty cycle	R_{ON} = R_{OFF} = 75 kΩ, R_{DEL} = 10 kΩ	66%	70%	74%	
	Minimum duty cycle				0%	
	PWM offset	CS = 0 V	0.43	0.5	0.61	V
CURRENT SENSE						
V_{LVL}	Current sense level shift voltage		0.4	0.5	0.6	V
$V_{ERR(max)}$	Maximum voltage error (clamped)			5		
V_{CS}	Current sense threshold cycle-by-cycle		0.43	0.48	0.53	
OUTPUT (OUT AND AUX)						
$I_{OUT(src)}$	Output source current			–2		A
$I_{OUT(sink)}$	Output sink current			2		
$V_{OUT(low)}$	Low-level output voltage	I_{OUT} = 150 mA		0.4		V
$V_{OUT(high)}$	High-level output voltage	I_{OUT} = –150 mA		11.1		

(5) Maximum pulse width needs to be less than D_{MAX}, which is a function of RON and R_{OFF}. For more information on D_{MAX}, see detailed description for R_{OFF} in .

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
OUTPUT (OUT AND AUX)						
t_R	Rise time	C_{LOAD} = 2 nF		19	28	ns
t_F	Fall time	C_{LOAD} = 2 nF		14	23	
t_{DEL1}	Delay time (AUX to OUT)	C_{LOAD} = 2 nF, R_{DEL} = 10 kΩ		110		
t_{DEL2}	Delay time (OUT to AUX)	C_{LOAD} = 2 nF, R_{DEL} = 10 kΩ		115		

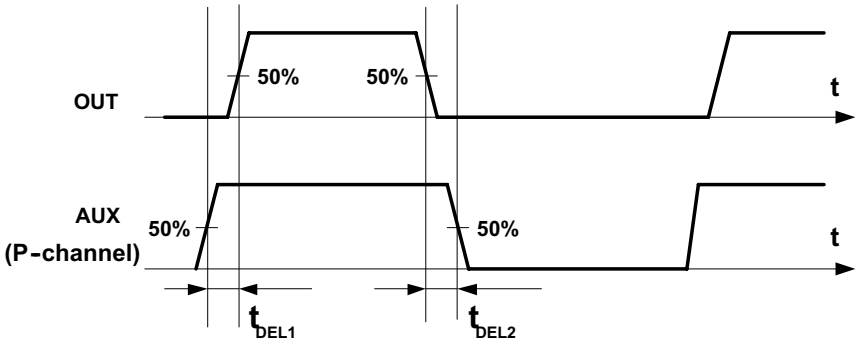


Figure 1. Output Timing Diagram

7.7 Typical Characteristics

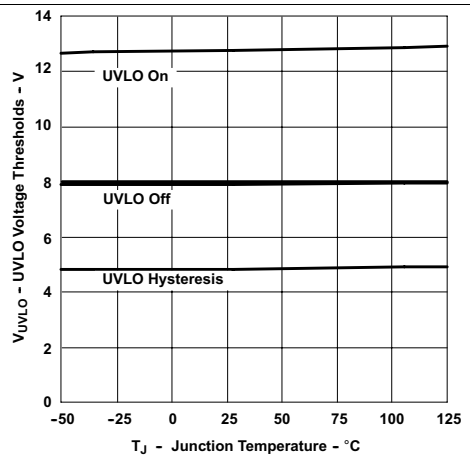


Figure 2. UVLO Voltage Thresholds vs. Junction Temperature

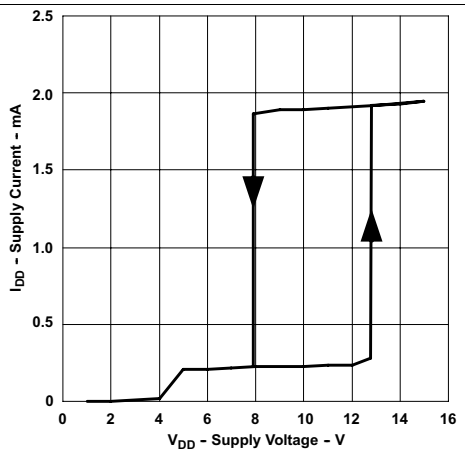


Figure 3. Quiescent Current vs. Supply Voltage

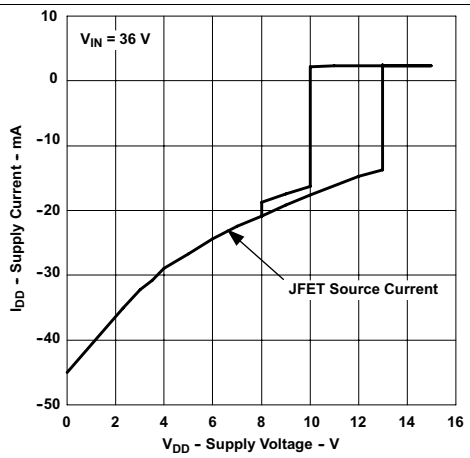


Figure 4. Supply Current vs. Supply Voltage

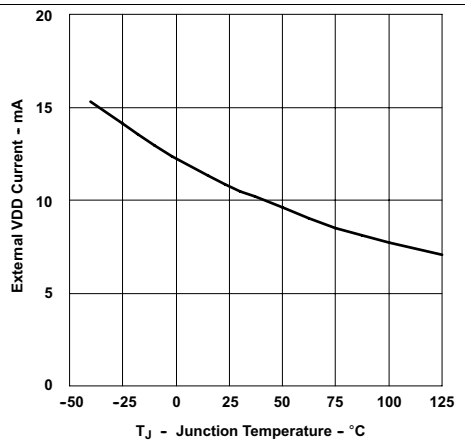


Figure 5. Typical Startup Current Available From VDD vs. Temperature

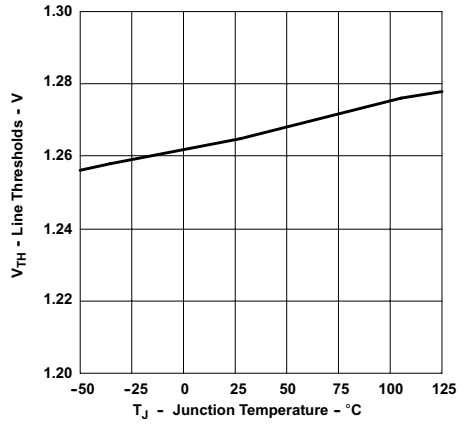


Figure 6. Line UV/OV Voltage Threshold vs. Junction Temperature

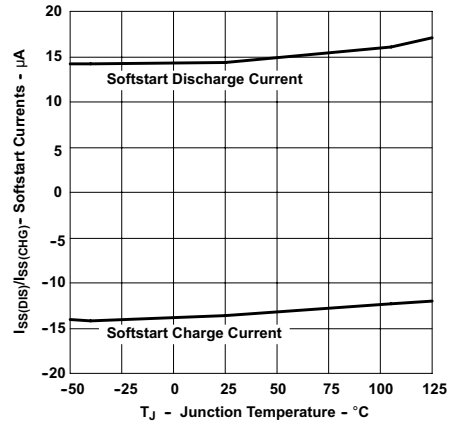


Figure 7. Softstart Currents vs. Temperature

Typical Characteristics (continued)

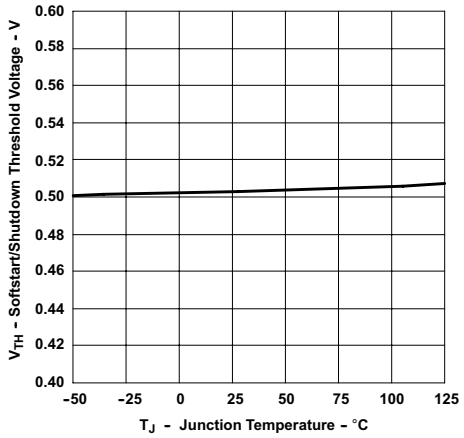


Figure 8. Soft Start/Shutdown Threshold Voltage vs. Junction Temperature

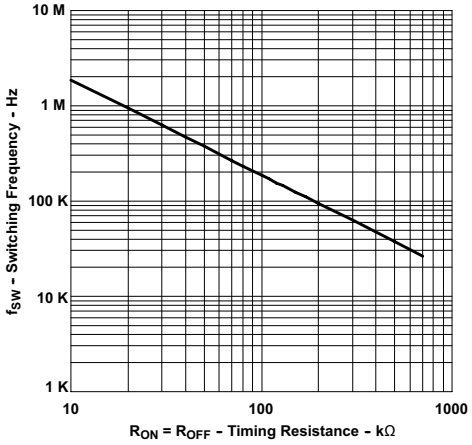


Figure 9. Switching Frequency vs. Programming Resistance

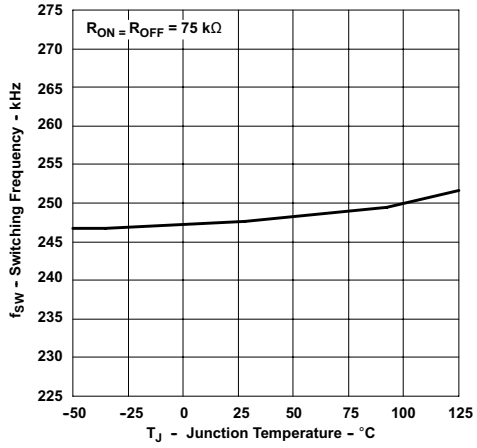


Figure 10. Oscillator Frequency vs. Junction Temperature

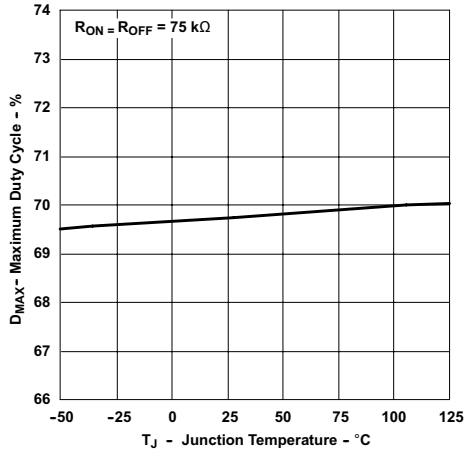


Figure 11. Maximum Duty Cycle vs. Junction Temperature

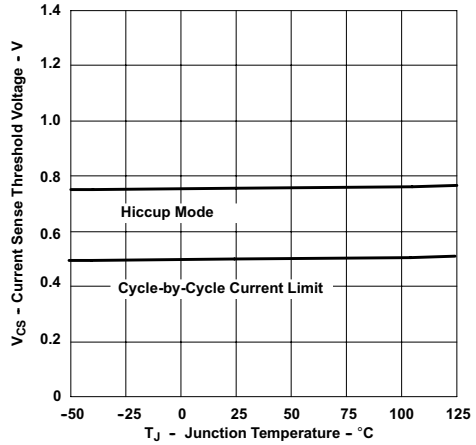


Figure 12. Current Sense Threshold Voltage vs. Junction Temperature

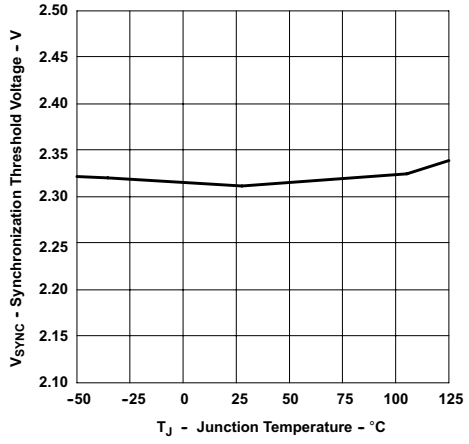


Figure 13. Synchronization Threshold Voltage vs. Junction Temperature

Typical Characteristics (continued)

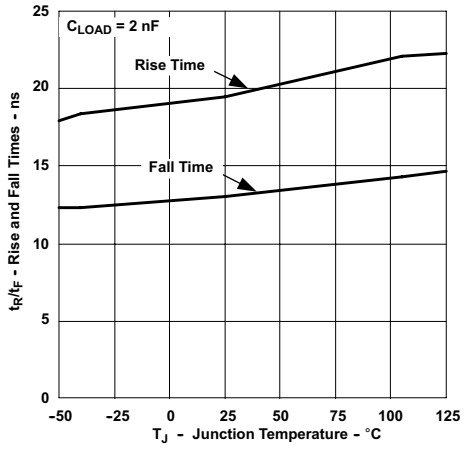


Figure 14. Out And AUX Rise And Fall Time vs. Junction Temperature

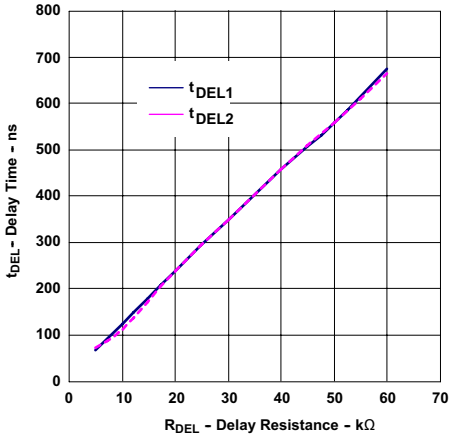


Figure 15. Delay Time vs. Delay Resistance

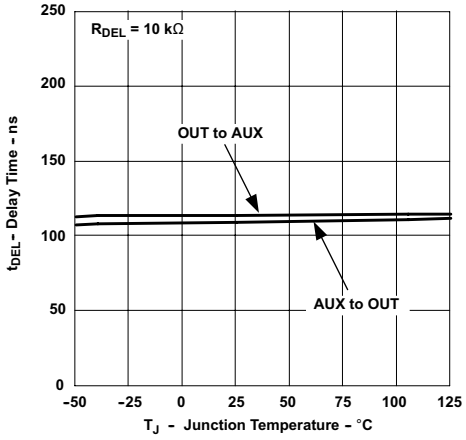


Figure 16. Delay Time vs. Junction Temperature

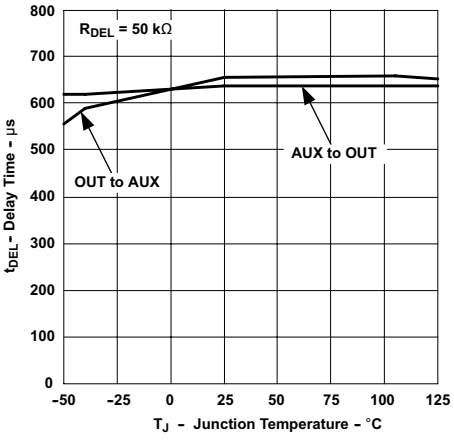


Figure 17. Delay Time vs. Junction Temperature

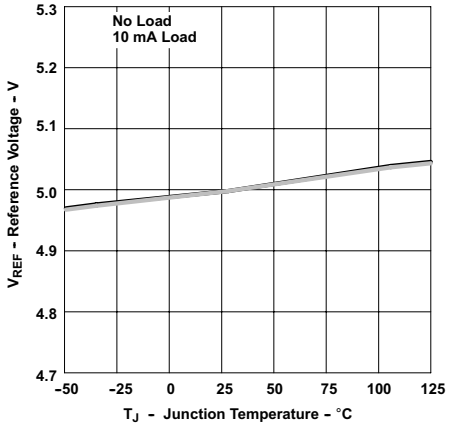


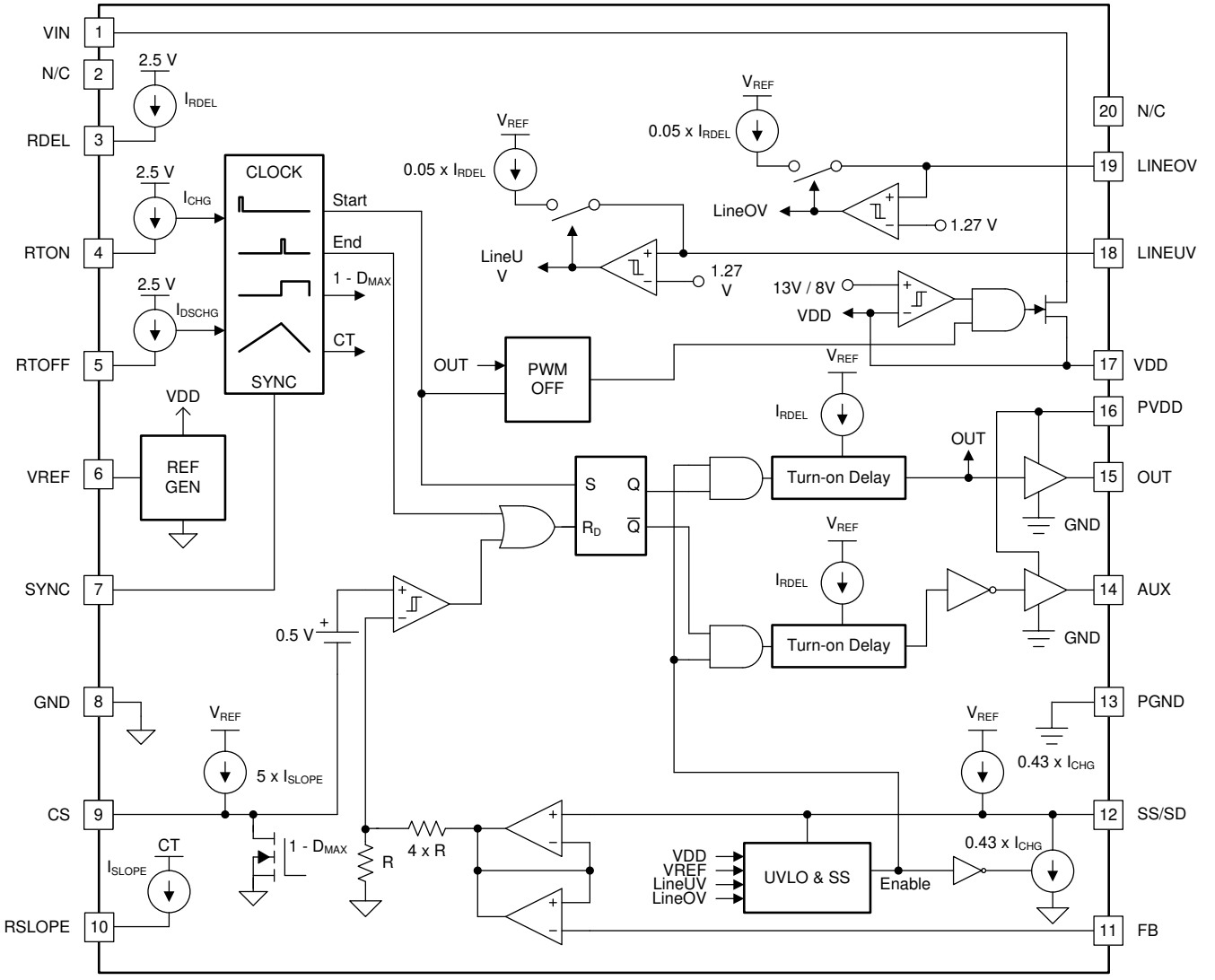
Figure 18. Reference Voltage vs. Temperature

8 Detailed Description

8.1 Overview

The UCC2897A is a peak current mode active clamp PWM controller. It provides simple interface to program the critical timings such as soft start, gate turn on delay, switching period, maximum operating duty cycle, and slope compensation. Features includes a high voltage JFET circuit, UVLO protection, line under/over voltage protection, pulse skipping, and synchronization. The UCC2897A also has the logic and the drive capability for a P-channel auxiliary switch. The VDD supply is generated from a bootstrap circuit connected to a bias winding.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Detailed Pin Descriptions

8.3.1.1 RDEL

This pin is internally connected to an approximately 2.5-V DC source. A resistor (RDEL) to GND sets the turn-on delay for both gate drive signals of the UCC2987A controller. The delay time is identical for both switching transitions between OUT turning off and AUX turning on, as well as when AUX is turning off and OUT is turning on. The delay time is defined in Equation 1.

$$t_{DEL1} = t_{DEL2} = 11.1 \times 10^{-12} \times R_{DEL} + 15 \times 10^{-9} \text{ seconds} \quad (1)$$

For proper selection of the delay time refer to the various references describing the design of active-clamp power-converters.

8.3.1.2 RON

This pin is internally connected to an approximately 2.5-V DC source. A resistor (R_{ON}) to GND (pin 6) sets the charge current of the internal-timing capacitor. The RON pin, in conjunction with the ROFF pin (pin 3), sets the operating frequency and maximum-operating duty cycle.

8.3.1.3 ROFF

This pin is internally connected to an approximately 2.5-V DC source. A resistor (R_{OFF}) to GND (pin 6) sets the discharge current of the internal-timing capacitor. The RON and ROFF pins set the switching period (T_{SW}) and maximum-operating duty cycle (D_{MAX}) according to the following equations:

$$t_{ON} = 36.1 \times 10^{-12} \times R_{ON} \times \left(\frac{S}{\Omega}\right) - t_{DEL}(s) \text{ seconds} \quad (2)$$

$$t_{OFF} = 15 \times 10^{-12} \times R_{OFF} \times \left(\frac{S}{\Omega}\right) + t_{DEL}(s) + 170 \times 10^{-9} \times (s) \text{ seconds} \quad (3)$$

$$T_{SW} = t_{ON} + t_{OFF} \quad (4)$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (5)$$

8.3.1.4 VREF

The internal 5-V bias rail of the controller is connected to this pin. The internal bias-regulator requires a high-quality ceramic-bypass capacitor (C_{VREF}) to GND for noise filtering and to provide compensation to the regulator circuitry. The recommended C_{VREF} value is 0.22 μF and X7R capacitors are recommended. The minimum-bypass capacitor value is 0.022 μF limited by stability considerations of the bias regulator, while the maximum is approximately 22 μF. The capacitance on VREF and VDD should be in a minimum ratio of 1:10.

The VREF pin is internally current-limited and supplies approximately 5 mA to external circuits. The 5-V bias is available only when the undervoltage lock-out (UVLO) circuit enables the operation of UCC2897A controller. The VREF-bias profile may not be monotonic before VDD reaches 5 V.

For the detailed functional description of the undervoltage lock-out (UVLO) circuit refer to the section of this datasheet.

Feature Description (continued)

8.3.1.5 SYNC

This pin is a bi-directional synchronization terminal. This pin should be left open if not used.

This pin provides an input for an external-clock signal which synchronizes the internal oscillator of the UCC2897A controller. The synchronizing frequency must be higher than the free-running frequency of the onboard oscillator (T_{SYNC} < T_{SW}). The acceptable minimum pulse-width of the synchronization signal is approximately 50 ns (positive logic), and should remain shorter than Equation 6.

$$(1 – D_{MAX}) \times T_{SYNC} \quad (6)$$

where

- D_{MAX} is set by R_{ON} and R_{OFF}

If the pulse-width of the synchronization signal stays within these limits, the maximum-operating duty ratio remains valid as defined by the ratio of RON and ROFF, and DMAX is the same in free-running and in synchronized modes of operation. If the pulse width of the synchronization signal would exceed the $(1 – D_{MAX}) \times T_{SYNC}$ limit, the maximum-operating duty cycle is defined by the synchronization pulse width.

In the stand-alone mode, the sync pin is driven by the internal oscillator which provides output pulses. The pulse width from SYNC output does not vary with the duty cycle. That signal synchronizes other PWM controllers or circuits requiring a constant-frequency time base.

External capacitance should be minimized on this pin layout. Capacitors are not connected between SYNC and GND or PGND. For more information on synchronization of the UCC2897A refer to the section of this datasheet.

8.3.1.6 GND

This pin provides a reference potential for all small-signal control and programming circuitry inside the UCC2897A. Ground layout is critical for correct operation. High-current surges from the MOSFET drivers conduct through PVDD, OUT, AUX, and PGND. To localize these surges, PVDD must bypass directly to PGND. PGND current must be electrically, capacitively, and inductively isolated from GND with only one short trace connecting PGND to GND, located to best minimize noise into GND.

8.3.1.7 CS

CS is a direct input to the PWM and current-limit comparators of the UCC2897A controller. The CS pin never connects directly across the current-sense resistor (R_{CS}) of the power converter. A small, customary R-C filter between the current-sense resistor and the CS pin is necessary to accommodate the proper operation of the onboard slope-compensation circuit and in order to protect the interna- discharge transistor connected to the CS pin (R_{F1}, C_F).

Slope compensation is achieved across RF by a linearly-increasing current flowing out of the CS pin. The slop-compensation current is only present during the on-time of the gate-drive signal of the main-power switch (OUT) of the converter. The internal-pulldown transistor of the CS pin is activated during the discharge time of the timing capacitor. This time interval is $(1 – D_{MAX}) \times T_{SW}$ long and represents the specified off-time of the main-power switch.

Feature Description (continued)

8.3.1.8 RSLOPE

A resistor (R_{SLOPE}) connected between this pin and GND (pin 6) sets the amplitude of the slope-compensation current. During the on time of the main gate-drive output (OUT) the voltage across R_{SLOPE} is a representation of the internal-timing-capacitor waveform. As the timing capacitor is being charged, the voltage across R_{SLOPE} also increases, generating a linearly-increasing current waveform. The current provided at the CS pin for slope compensation is proportional to this current flowing through R_{SLOPE}.

Due to the high speed, AC-voltage waveform present at the RSLOPE pin, the parasitic capacitance and inductance of the external-circuit components connected to the RSLOPE pin should be carefully minimized.

For more information on how to program the internal-slope compensation refer to the section of this datasheet.

8.3.1.9 FB

FB and SS/SD interact. The one with the lower-voltage value takes control on the duty cycle, refer to SS/SD description. This pin is an input for the control voltage of the pulse-width modulator of the UCC2897A.The control voltage is generated by an external-error amplifier by comparing the output voltage of the converter to a voltage reference and employing the compensation for the voltage-regulation loop. Usually, the error amplifier is located on the secondary side of the isolated-power converter and the output voltage is sent across the isolation boundary by an optocoupler. Thus, the FB pin is usually driven by the optocoupler. An external-pullup resistor to the VREF pin (pin 4) is also required for proper operation as part of the feedback circuitry.

The control voltage is internally buffered and connected to the PWM comparator through a voltage divider to make it compatible to the signal level of the current-sense circuit. The useful voltage range of the FB pin is between approximately 2.5 V and 4.5 V. Control voltages below the 2.5-V threshold result in zero-duty cycle (pulse skipping) while voltages above 4.5 V result in full-duty-cycle (D_{MAX}) operation.

8.3.1.10 SS/SD

A capacitor (C_{SS}) connected between this pin and GND (pin 6) programs the soft-start time of the power converter. The soft-start capacitor is charged by a precise, internal DC-current source which is programmed by the R_{ON} resistor connected to pin 2. The soft-start current is defined in Equation 7.

$$I_{SS} = 0.43 \times I_{RON} = 0.43 \times \frac{V_{REF}}{2} \times \frac{1}{R_{ON}} \quad (7)$$

This DC current charges C_{SS} from 0 V to approximately 5 V. Internal to the UCC2897A, the soft-start capacitor voltage is buffered and ORed with the control voltage present at the FB pin (pin 9). The lower of the two voltages manipulates the PWM engine of the controller through the voltage divider described with regards to the FB pin. Accordingly, the useful control range on the SS pin is similar to the control range of the FB pin and it is between 2.5 V and 4.5 V approximately. During line-undervoltage protection, the PWM follows this pin-capacitor discharge to achieve soft-stop function

Feature Description (continued)

8.3.1.11 PGND

This pin serves as a dedicated connection to all high-current circuits inside the UCC2897A. The high-current portion of the controller consists of the two high-current gate drivers, and the various bias connections except VREF (pin 4). The PGND (pin 11) and GND (pin 6) pins are not connected internally, a low-impedance external connection between the two ground pins is also required. TI recommends to form a separate ground plane for the low-current setup components (R_{DEL}, R_{ON}, R_{OFF}, C_{VREF}, C_F, R_{SLOPE}, C_{SS} and the emitter of the optocoupler in the feedback circuit). This separate ground plane (GND) should have a single connection to the rest of the ground of the power converter (PGND) and this connection should be between pin 6 and pin 11 of the controller.

8.3.1.12 AUX

AUX is a high-current gate-drive output for the auxiliary switch to implement the active-clamp operation for the power stage. The auxiliary output (AUX) of the UCC2897A drives a P-channel device as the clamp switch therefore it requires an active-low operation (the switch is ON when the output is low).

8.3.1.13 OUT

This high-current output drives an external N-channel MOSFET. The UCC2897A controller uses an active-high drive signal for the main switch of the converter.

Due to the high-speed and high-drive current capability of these outputs (AUX, OUT) the parasitic inductance of the external-circuit components connected to these pins should be carefully minimized. A potential way of avoiding unnecessary parasitic inductances in the gate-drive circuit is to place the controller in close proximity to the MOSFETs and by ensuring that the outputs (AUX, OUT) and the gates of the MOSFET devices are connected by wide overlapping traces. TI recommends connecting a 10-kΩ resistor from this pin to PGND pin to reduce a possible parasitic effect from layout.

8.3.1.14 VDD

The VDD rail is the primary bias for the internal high-current gate drivers, the internal 5-V bias regulator and for parts of the undervoltage-lockout circuit. To reduce switching noise on the bias rail, a good-quality ceramic capacitor (C_{HF}) must be placed very closely between the VDD pin and PGND (pin 11) to provide adequate filtering. The recommended C_{HF} value is 1-µF for most applications but the value might be affected by the properties of the external-MOSFET transistors used in the power stage.

In addition to the low-impedance high-frequency filtering, the bias rail of the controller requires a larger value energy-storage capacitor (C_{BIAS}) connected parallel to C_{HF}. The energy-storage capacitor must provide the hold-up time to operate the UCC2897A (including gate-drive power requirements) during start up. In steady-state operation the controller must be powered from a bootstrap winding off the power transformer or by an auxiliary-bias supply. In case of an independent-auxiliary-bias supply, the energy storage is provided by the output capacitance of the bias supply. The capacitor values are also determined by the capacitor values connected to VREF. The capacitance on VREF and VDD should be in a minimum ratio of 1:10.

Feature Description (continued)

8.3.1.15 LINEUV

This input monitors the incoming-power source to provide an accurate undervoltage-lockout function with user-programmable hysteresis for the power supply controlled by the UCC2897A. The unique property of the UCC2897A is to use only one pin to implement these functions without sacrificing on performance. The input voltage of the power supply is scaled to the precise 1.27-V threshold of the undervoltage-lockout comparator by an external-resistor divider (R_{IN1}, R_{IN2} in). Once the input threshold of the line monitor is exceeded, an internal-current source gets connected to the LINEUV pin. The current generator is programmed by the R_{DEL} resistor connected to pin 1 of the controller. The actual current level is given in Equation 8.

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \quad (8)$$

As this current flows through R_{IN2} of the input divider, the undervoltage-lockout hysteresis is a function of I_{HYST} and R_{IN2} allowing accurate programming of the hysteresis of the line-monitoring circuit. When LINEUV is detected, PWM follows VSS capacitor discharge and soft-stop function is provided. The soft-start capacitor starts discharging when the soft-start capacitor voltage reaches 2.5 V. Both OUT and AUX stop switching while the soft-start capacitor continues discharging until the voltage reaches 0.5 V when the soft start is resumed on the assumption of all other soft-start conditions are met.

For more information on how to program the line-monitoring function refer to the of this datasheet.

8.3.1.16 VIN

The UCC2897A controller is equipped with a high-voltage N-channel-JFET startup device to initiate operation from the input-power source of the converter in applications where the input voltage does not exceed the 110-V maximum rating of the startup transistor. In these applications, the VIN pin connects directly to the positive terminal of the input-power source. The internal-JFET startup transistor provides charge-current for the energy-storage capacitor (C_{BIAS}) connected across the VDD (pin 14) and PGND (pin 11) terminals. Note that the startup device turns off immediately when the voltage on the VDD pin exceeds approximately 12.7 V, the undervoltage-lockout threshold of the controller for turn-on. The JFET is also disabled at all times when the high-current gate drivers are switching to protect against excessive-power dissipation and current through the device. For dependable start-up, VDD must not be loaded by more than 4 mA.

For more information on biasing the UCC2897A, refer to the and sections of this datasheet.

8.3.1.17 LINEOV

This input monitors the incoming-power source to provide an accurate-overvoltage protection with user-programmable hysteresis for the power supply controlled by the controller. The circuit implementation of the overvoltage-protection function is identical to the technique used for monitoring the input-power rail for undervoltage lockout. The circuit implements an accurate threshold and hysteresis using only one pin. The input voltage of the power supply is scaled to the precise 1.27-V threshold of the overvoltage-protection comparator by an external-resistor divider (R_{IN3}, R_{IN4} in). Once the input threshold of the line monitor is exceeded, an internal-current source gets connected to the LINEOV pin. The current generator is programmed by the R_{DEL} resistor connected to pin 1 of the controller. The actual current level is given in Equation 9.

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \quad (9)$$

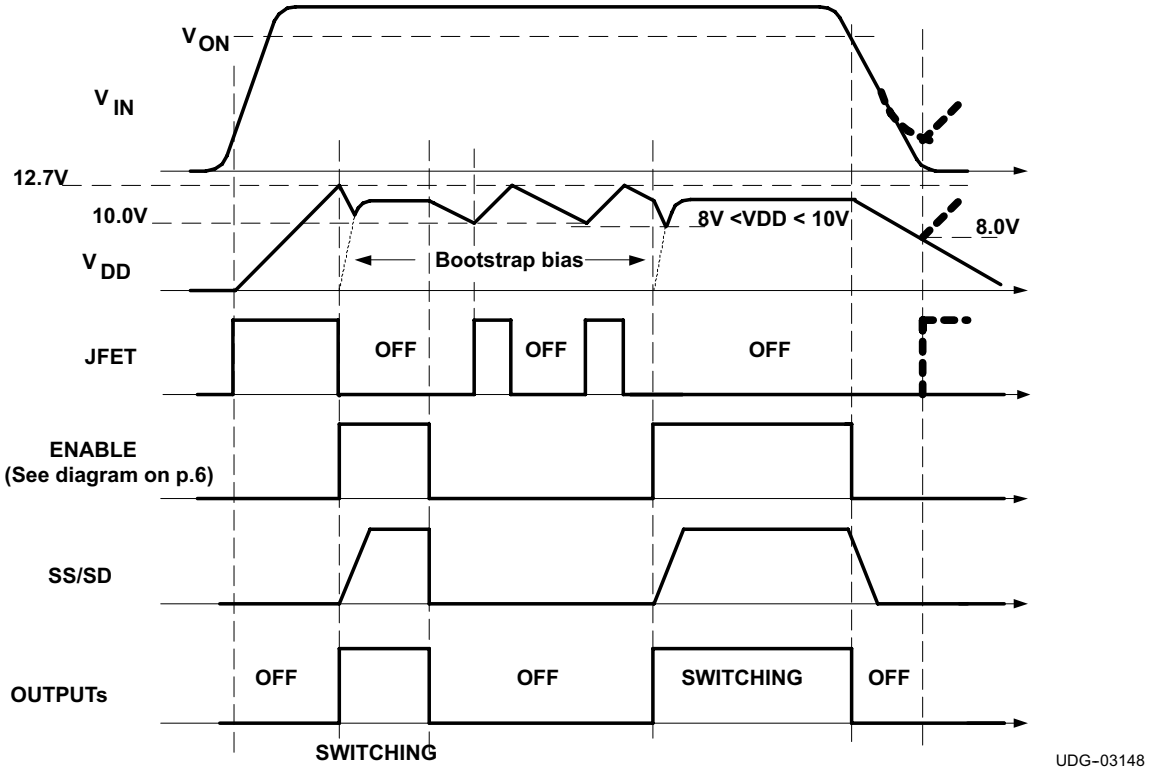
As this current flows through RIN4 of the input divider, the overvoltage-protection hysteresis is a function of I_{HYST} and R_{IN4} allowing accurate programming of the hysteresis of the line-monitoring circuit.

For more information on how to program the overvoltage protection, refer to the of this datasheet.

Feature Description (continued)

8.3.2 JFET Control and UVLO

The UCC2897A controller includes a high-voltage JFET startup-transistor. The steady-state power-consumption of the of the control circuit which also includes the gate-drive power-loss of the two power switches of an active-clamp converter exceeds the current and thermal capabilities of the device. Thus the JFET should only be used for initial start-up of the control circuitry and to provide keep-alive power during stand-by mode when the gate-drive outputs are not switching. Accordingly, the startup device is managed by the control algorithm implemented on board the UCC2897A. The following timing diagram in Figure 19 illustrates the operation of the JFET startup device.



Values are typical in the drawing.

Figure 19. JFET Control Startup and Shutdown

During initial power-up the JFET is on and charges the C_{BIAS} and C_{HF} capacitors connected to the VDD pin. The undervoltage lockout-circuit of the controller monitors the VDD pin to ensure proper biasing before the operation is enabled. When the VDD voltage reaches approximately 12.7 V (UVLO turnon threshold) the UVLO circuit enables the rest of the controller. At that time, the JFET turns off and 5 V appears on the VREF terminal. Switching waveforms might not appear at the gate-drive outputs unless all other conditions of proper operation are met. These conditions are:

- The voltage on the CS pin is below the current limit threshold
- The control voltage is above the zero duty-cycle boundary (V_{FB} > 2.5 V).
- The input voltage is in the valid operating range (V_{VON} < V_{VIN} < V_{VOFF}.
  - The line under or overvoltage protections are not activated.

Feature Description (continued)

As the controller starts operation it draws bias power from the C_{BIAS} capacitor until the bootstrap winding takes over (referring to Figure 25 and Figure 26). During this time, VDD voltage is falling rapidly as the JFET is off but the bootstrap voltage is still not sufficient to power the control circuits. It is imperative to store enough energy in C_{BIAS} to prevent the bias voltage from dipping below the turnoff threshold of the UVLO circuit during the startup-time interval. Otherwise the power supply goes through several cycles of retry attempts before steady-state operation is established.

During normal operation the bias voltage is determined by the bootstrap bias design. The UCC2897A tolerates a wide range of bias voltages between the minimum-operating voltage (UVLO turn-off threshold) and the maximum-operating voltage as defined in the .

In applications where the power supply enters standby in response to an external command, the bias voltage of the controller must be kept alive to react intelligently to the control signal. In standby mode, switching action is suspended for an undefined period of time and the bootstrap power is unavailable to bias the controller. Without an alternate power source the bias voltage collapses and the controller initiates a re-start sequence. To avoid this situation, the onboard JFET of the UCC2897A controller keeps the VDD bias alive as long as the gate-drive outputs remain inactive. As shown in the timing diagram in Figure 19, the JFET turns on when VDD = 10 V and charges the C_{BIAS} capacitor to approximately 12.7 V. At that time the JFET turns off and VDD gradually decreases to 10 V then the procedure repeats. When the power supply is enabled again, the controller is fully biased and ready to initiate the soft-start sequence. As soon as the gate-drive pulses appear the JFET turn off and bias is provided by the bootstrap bias generator.

During power down the situation is different as the switching action continues until the VDD bias voltage drops below the UVLO turn-off threshold of the controller (approximately 8 V). At that time the UCC2897A shuts down and turns off the 5-V bias rail and returning to startup state when the JFET device is turned on and the C_{BIAS} capacitor starts charging again. In case the input voltage of the converter is re-established, the UCC2897A attempts to restart the converter.

Feature Description (continued)

8.3.3 Line Undervoltage Protection

As shown in Figure 20, when the input power-source is removed, the power supply is turned off by the line-undervoltage protection because the bootstrap winding keeps the VDD bias up as long as switching takes place in the power stage. As the input voltage of the power supply decreases gradually toward the line-cutoff voltage, the operating duty cycle of the converter must compensate for the lower input voltage. At minimum input-voltage the duty cycle nears the maximum value (D_{MAX}). Under these conditions the voltage across the clamp capacitor approaches the highest value since the transformer must be reset in a relatively short time. The timing diagram in Figure 20 highlights that in the instance when the converter stops switching the clamp-capacitor voltage might be at the maximum level. Since the only load of the clamp capacitor is the power transformer, this high voltage could linger across the clamp capacitor for a long time when the converter is off. With this high voltage present across the clamp capacitor a soft start would be very dangerous, due to the narrow duty cycle of the main switch and the long on-time of the clamp switch. This could cause the power transformer to saturate during the next soft-start cycle.

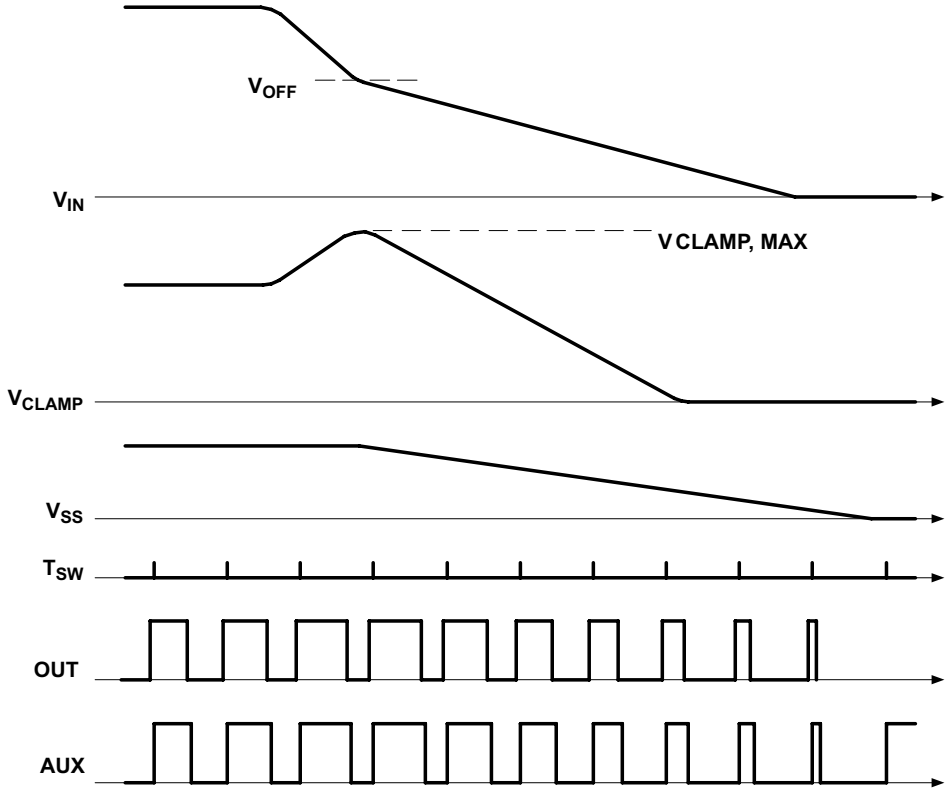


Figure 20. Line Undervoltage Shutdown Waveforms, P-Channel

To eliminate this potential hazard the UCC2897A controller, discharge the clamp capacitor during power down safely. The OUT and the AUX output continues switching while the soft-start capacitor C_{SS} is being slowly discharged. the function of soft stop is achieved because the AUX pulse-width gradually increases as the clamp voltage decreases, while never applying the high voltage across the transformer for extended period of time.

Feature Description (continued)

8.3.4 Line Overvoltage Protection

When the line-overvoltage protection is triggered in the UCC2897A controller, the gate-drive signals are immediately disabled. At the same time, the slow discharge of C_{SS} initiates. While the soft-start capacitor discharges the gate-drive signals remain disabled. Once V_{SS} = 0.5 V and the overvoltage disappears from the input of the power supply, operation resumes through a regular soft start of the converter as it is demonstrated in Figure 21. The pulses of OUT and AUX stop if one of three conditions is met:

1. VDD reaches UVLO off
2. VSS reaches below 2.5 V
3. FB voltage is below 2.5 V

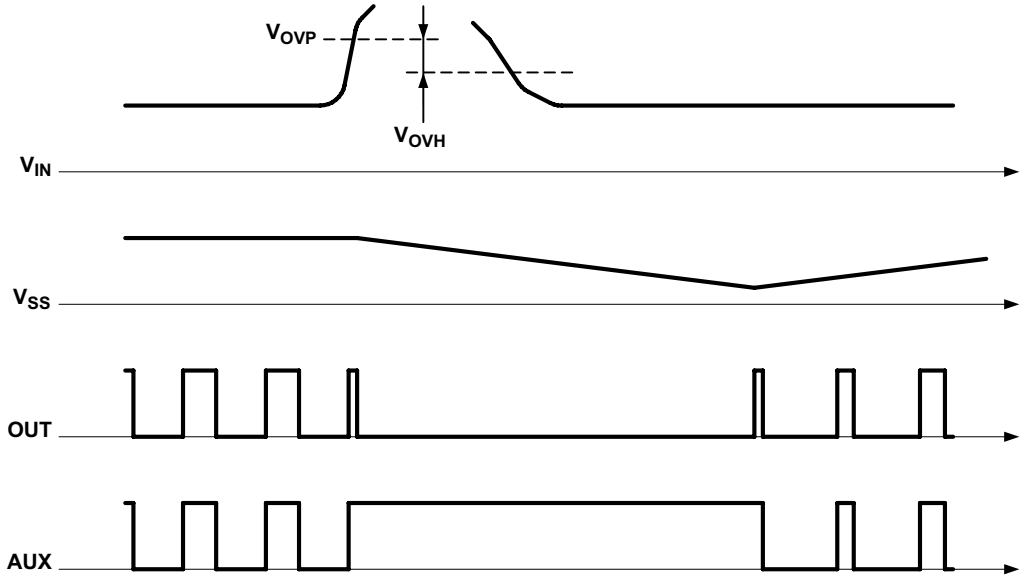


Figure 21. Line Overvoltage Sequence, P-Channel

Feature Description (continued)

8.3.5 Pulse Skipping

During output-load current-transients or light-load conditions most PWM controllers must be able to skip some number of PWM pulses. In an active-clamp topology where the clamp switch is driven complementary to the main switch, the skipping of pulses applies the clamp voltage across the transformer continuously. Since operating conditions might require skipping several switching-cycles on the main transistor, saturating the transformer is very likely if the AUX output remains on.

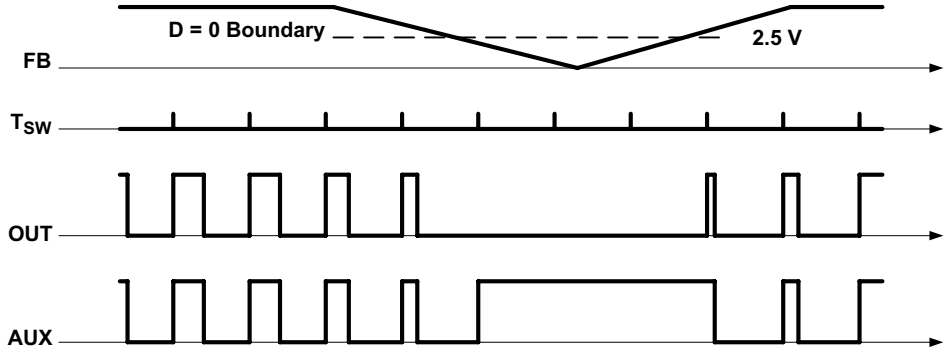


Figure 22. Pulse Skipping Operation, P-Channel

To overcome this problem, the UCC2897A family incorporates pulse skipping for both outputs in the controller. As shown in Figure 22, when a pulse is skipped at the main output (OUT) because the feedback signal demands zero duty-ratio, the corresponding output pulse on the AUX output is omitted as well. This operation prevents reverse saturation of the power transformer and preserves the clamp-capacitor voltage level during pulse-skipping operation.

Feature Description (continued)

8.3.6 Synchronization

The UCC2897A has a bi-directional synchronization pin. In the stand-alone operation the SYNC pin is driven by the internal oscillator of the UCC2897A which provides an approximately 5-V amplitude square-wave output. This signal synchronizes other PWM controllers or circuits requiring a constant frequency time-base. The synchronization output of the UCC2897A is generated when the internal-timing capacitor reaches the peak value. Therefore, the synchronization waveform does not coincide with the turnon of the main gate-driver output as it is usually implemented in PWM controllers.

The operation of the oscillator and other relevant waveforms in free-running and synchronized mode are shown in Figure 23.

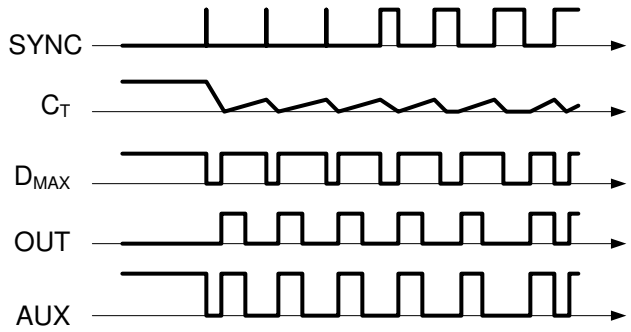


Figure 23. A Synchronization Waveform for SYNC Input, P-Channel

The most critical and unique feature of the oscillator is to limit the maximum-operating duty-cycle of the converter, which is achieved by accurately controlling the charge and discharge intervals of the on-board timing capacitor. The maximum on-time of the OUT pin, which is also the maximum duty-cycle of the active-clamp converter, is limited by the charging-interval of the timing capacitor. While the capacitor is reset to the initial voltage level, OUT is ensured to be off.

When synchronization is used, the rising edge of the signal terminates the charging period and initiates the discharge of the timing capacitor. Once the timing-capacitor voltage reaches the predefined valley-voltage, a new charge period starts automatically. This method of synchronization leaves the charge and discharge slopes of the timing-waveform unaffected thus maintains the maximum duty-cycle of the converter, independent of the operation mode.

Although the synchronization circuit is level sensitive, the actual synchronization event occurs at the rising-edge of the waveform, allowing the synchronizing pulse-width to vary significantly while certain limitations are observed. The minimum pulse-width should be sufficient to ensure reliable triggering of the internal-oscillator circuitry, therefore it is greater than approximately 50 nanoseconds. The other limiting factor is to keep it shorter than Equation 10.

$$(1 - D_{MAX}) \times T_{SYNC} \quad (10)$$

where

- T_{SYNC} is the period of the synchronization frequency

When a pulse wider than that of Equation 10 is connected to the SYNC input, the oscillator is unable to maintain the maximum duty-cycle, originally set by the timing-resistor ratio (R_{ON}, R_{OFF}). Furthermore, the timing-capacitor waveform has a flat portion as highlighted by the vertical marker in the timing diagram. During this flat portion of the waveform, both outputs are off, but this state is not compatible with the operation of active-clamp power converters. Therefore, this operating mode is not recommended.

Note that both outputs of the UCC2897A controller are off if the synchronization signal stays continuously high.

When both UCC2897A outputs are synchronized by tying their SYNC pins together, they operate in-phase. It is possible to set different maximum duty-cycle limits for both UCC2897A outputs and still synchronize them by a simple connection between their respective SYNC terminals.

Feature Description (continued)

8.3.7 Gate Drive Connection

The low-side P-channel gate-drive circuit involves a level shifter using a capacitor and a diode which ensures that the gate-drive amplitude of the auxiliary switch is independent of the actual duty-cycle of the converter.

Detailed analysis and design examples of these and many similar gate-drive solutions are given in *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SLUP169.

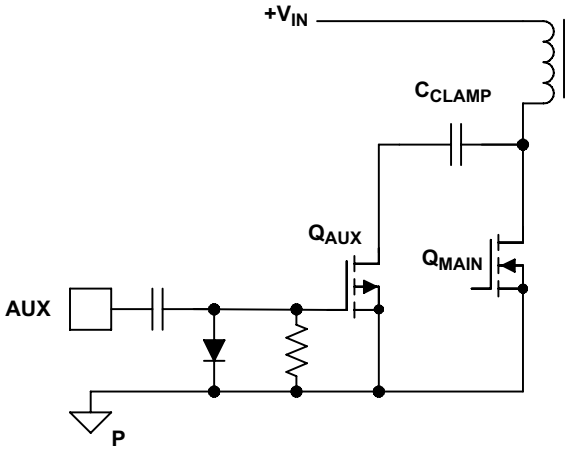


Figure 24. Low-Side P-Channel

Feature Description (continued)

8.3.8 Bootstrap Biasing

Many converters use a bootstrap circuit to generate bias power during steady-state operation. The popularity of this solution is justified by the simplicity and high-efficiency of the circuit. Usually, bias power is derived from the main transformer by adding an additional dedicated winding to the structure. Using a flyback converter as shown in Figure 25, a bootstrap winding provides a quasi-regulated bias voltage for the primary-side control circuits. The voltage on the VDD pin is equal to the output voltage times the turns-ratio between the output and the bootstrap-winding in the transformer. Because the output is regulated, the bias rail is regulated as well.

While the same arrangement is used in a forward-type converter, the bootstrap winding off the main-power transformer is unable to provide a quasi-regulated voltage. In the forward converter, the voltage across the bootstrap-winding equals the input voltage times the turns-ratio. Accordingly the bias voltage would vary with the input voltage and exceeds the maximum-operating voltage of the control circuits at high line. A linear regulator limits and regulates the bias voltage if the power dissipation is acceptable. Another possible solution for the forward converter is to generate the bias voltage from the output inductor as shown in Figure 26.

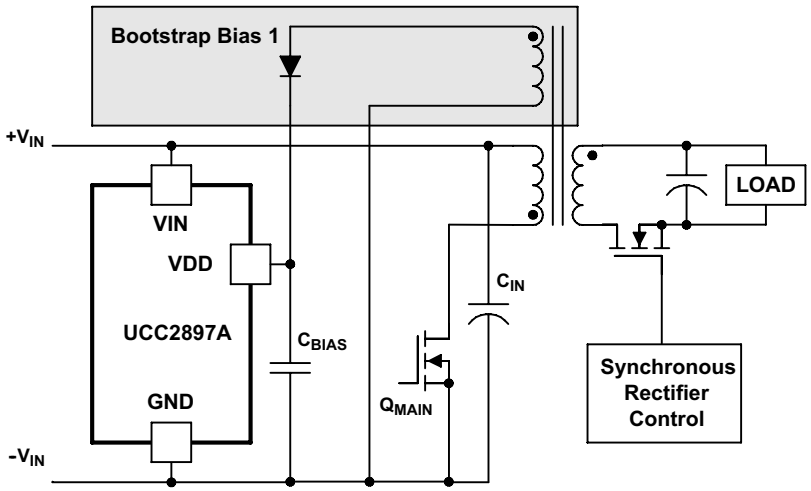


Figure 25. Bootstrap Bias 1, Flyback Example

Feature Description (continued)

This solution uses the regulated output voltage across the output inductor during the freewheeling period to generate a quasi-regulated bias for the control circuits.

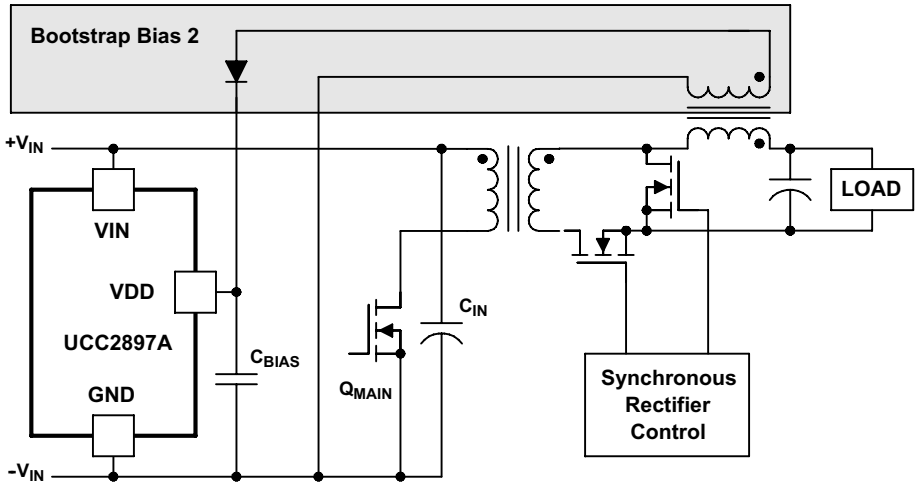


Figure 26. Bootstrap Bias 2, Forward Example

This solution uses the regulated output voltage across the output inductor during the freewheeling period to generate a quasi-regulated bias for the control circuits.

Both of the illustrated solutions provide reliable bias-power during normal operation. Note that in both cases, the bias voltages are proportional to the output voltage. This nature of the bootstrap bias-supply causes the converter to operate in a hiccup mode under significant overload or under short-circuit conditions as the bootstrap winding is not able to hold the bias rail above the undervoltage lockout-threshold of the controller.

Another biasing solution, based on the active circuit, is shown on the previous page with components Q10, C18, R19, D10 and D12. Such a circuit is used in the applications where the allowed biasing-capacitor size is limited to optimize the board space utilization.

8.4 Device Functional Modes

The UCC2897A uses a high voltage JFET to provide the start-up current for the controller until a bootstrap-type rail becomes available on VDD pin. The JFET will be turned off after the VDD pin voltage exceeds the UVLO threshold. Then the device enters normal operation mode. If the line voltage is abnormal, the device enters line under voltage or line over voltage mode. During light load or load transient, the device may enter pulse skipping mode if the feedback voltage FB is less than a certain threshold. Figure 27 shows the mode transition diagram.

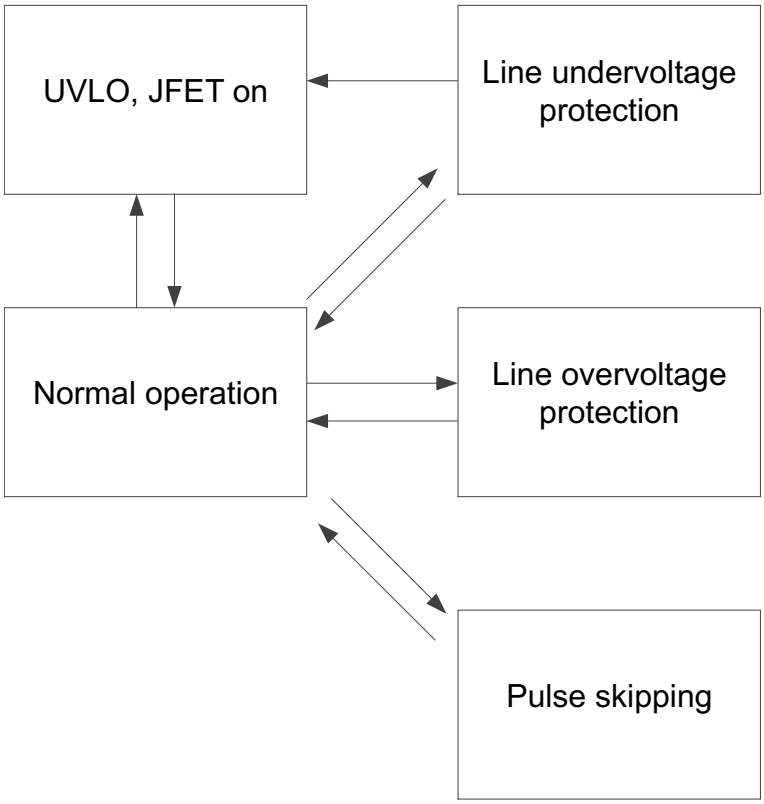


Figure 27. Mode Transition Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC2897A offers a highly integrated solution for active clamp PWM converters. In order to make the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device.

The UCC2897A family offers a highly integrated feature-set and excellent accuracy to control an active-clamp forward or active-clamp flyback power-converter.

9.2 Typical Application

In order to take advantage of all the benefits integrated in these controllers, the following procedure simplifies the setup to avoid unnecessary iterations in the design procedure. Refer to Figure 28 setup diagrams for component names.

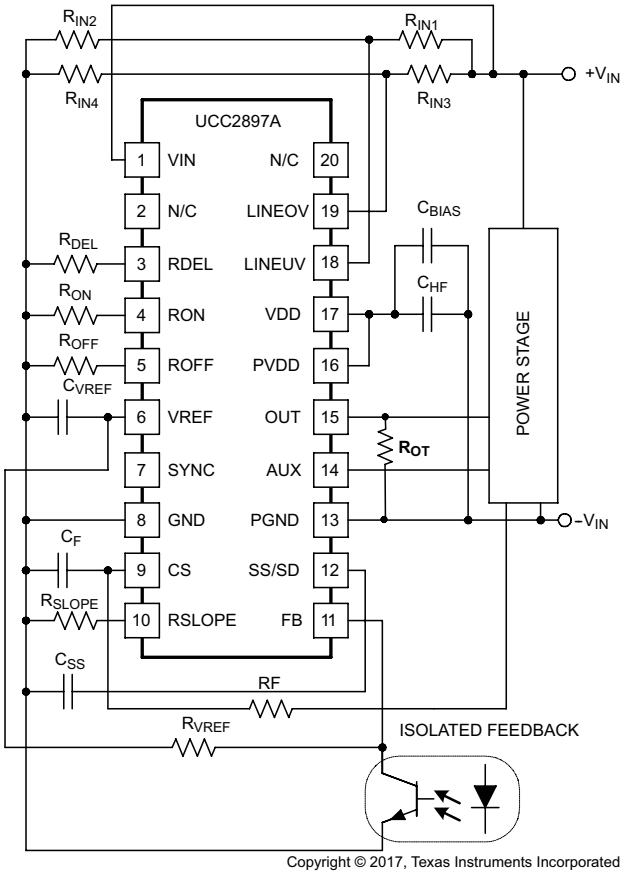


Figure 28. UCC2897A Typical Application

Typical Application (continued)

9.2.1 Design Requirements

The required design is an active clamp reset forward converter providing a 3.3-V regulated output at 30 A of load current, operating from a 48-V input. The design operates over the full 36-V to 72-V telecom input range, and is able to fully regulate down to zero load current.

Table 1. Design Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics					
Input voltage range		36	48	72	V
No load input current	V_{IN} = 36 V, I_{OUT} = 0 A		75	100	mA
Input undervoltage limit			35		V
Input overvoltage limit			73		V
Max input current	V_{IN} = 36 V, I_{OUT} = 30 A		3	3.25	A
Input voltage ripple	V_{IN} = 72 V, I_{OUT} = 30 A		1.5	1.75	V_{PP}
Output Characteristics					
Output voltage	36 V < V_{IN} < 72 V, 0 A < I_{OUT} < 30 A	3.25	3.3	3.35	V
Output voltage regulation	Line reg (36 V < V_{IN} < 72 V, I_{OUT} = 0 A)		0.00%	0.01%	
	Load reg (0 A < I_{OUT} < 30 A, V_{IN} = 48 V)		0.06%	0.10%	
Output voltage ripple	V_{IN} = 48 V, I_{OUT} = 30 A		30	35	mV_{PP}
Output load current	36 V < V_{IN} < 72 V	0		30	A
Output current limit		32			A
Short circuit protection	Not provided				
Systems Characteristics					
Switching frequency		225	250	265	kHz
Control loop bandwidth	36 V < V_{IN} < 72 V, I_{OUT} = 10 A	5		7	kHz
Phase margin		50		60	degrees
Peak efficiency	V_{IN} = 36 V		93%		
Full load efficiency	V_{IN} = 48 V, I_{OUT} = 30 A		91%		

9.2.2 Detailed Design Procedure

Before the controller design begins, the power-stage design must be completed. From the power-stage design the following operating parameters are required to complete the setup procedure of the controller:

- Switching frequency (f_{SW})
- Maximum operating duty cycle (D_{MAX})
- Soft-start duration (t_{SS})
- Gate-drive power requirements of the external-power MOSFETs ($Q_{G(main)}$, $Q_{G(aux)}$)
- Bias method and voltage for steady-state operation (bootstrap or bias supply)
- Gate-drive turn-on delay (t_{DEL})
- Turnon input-voltage threshold (V_{ON})
- Minimum-operating input voltage (V_{OFF} where $V_{IN(OFF)} < V_{IN(on)}$
- Maximum-operating input voltage (V_{OVP})
- Overvoltage-protection hysteresis (V_{OVH})
- The down slope of the output-inductor current-waveform reflected across the primary-side current-sense resistor (dV_L / dt)

9.2.2.1 Oscillator

The two timing elements of the oscillator are calculated from f_{SW} and D_{MAX} by the Equation 11 and Equation 12.

$$R_{ON} = \frac{t_{ON} + t_{DEL}}{36.1 \times 10^{-12} \times \left(\frac{s}{\Omega}\right)} \tag{11}$$

$$R_{OFF} = \frac{t_{OFF} - t_{DEL} - 170 \times 10^{-9} \times (s)}{15 \times 10^{-12} \times \left(\frac{s}{\Omega}\right)}$$

where

- D_{MAX} is a dimensionless number between 0 and 1. (12)

9.2.2.2 Soft Start

Once R_{ON} is defined, the charge current of the soft-start capacitor is calculated with Equation 13.

$$I_{SS} = 0.43 \times \frac{V_{REF}}{2} \times \frac{1}{R_{ON}} \tag{13}$$

During soft start, C_{SS} charges from 0 to 5 V by the calculated I_{SS} current. The actual control range of the soft-start capacitor voltage is between 2.5 and 4.5 V. Therefore, the soft-start capacitor value must be based on this narrower control range and the required startup time (t_{SS}) according to Equation 14.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{4.5\ V - 2.5\ V} \tag{14}$$

Note that t_{SS} defines a time interval to reach the maximum-current capability of the converter and not the time required to ramp the output voltage from 0 V to the nominal regulated level. Using an open-loop start-up scheme does not allow accurate control over the ramp-up time of the output voltage. In addition to the I_{SS} and C_{SS} values, the time required to reach the nominal output voltage of the converter is a function of the maximum-output current (current limit), the output capacitance of the converter and the actual load conditions. If it is critical to implement a tightly-controlled ramp-up time at the output of the converter, the soft start must be implemented using a closed-loop technique. Closed-loop soft-start implements with the error amplifier of the voltage regulation loop when the voltage reference is ramped from 0 V to the final steady-state value during the required t_{SS} startup-time interval.

9.2.2.3 VDD Bypass Requirements

First, the high-frequency filter capacitor is calculated based on the gate-charge parameters of the external MOSFETs. If the basic switching-frequency ripple is kept below 0.1-V across C_{HF}, this value is approximated with Equation 15.

$$C_{HF} = \frac{Q_{G(main)} + Q_{G(aux)}}{0.1\,V} \tag{15}$$

The energy storage requirements are defined primarily by the startup-time (t_{SS}), turnon (approximately 12.7 V), and turnoff (approximately 8 V) thresholds of the undervoltage-lockout circuit-monitoring of the controller for the VDD pin. In addition, the bias-current consumption of the entire primary-side control circuit (I_{DD} + I_{EXT}) must be known. This power consumption is estimated with Equation 16.

$$P_{BIAS} = [I_{DD} + I_{EXT} + (Q_{G(main)} + Q_{G(aux)} \times f_{SW})] \times V_{DD} \tag{16}$$

During start-up (t_{SS}), this power is provided by C_{BIAS} while the voltage must remain above the UVLO turn-off threshold. This relationship is expressed with Equation 17.

$$P_{BIAS} \times t_{SS} < ½ \times C_{BIAS} \times (12.7^2 - 8^2) \tag{17}$$

Rearranging the equation yields the minimum value for CBIAS as shown in Equation 18.

$$C_{BIAS} > \frac{2 \times P_{BIAS} \times t_{SS}}{\left(12.7^2 - 8^2\right)} \tag{18}$$

Equation 19 may yield a big capacitance value that is not feasible in some applications, such as an additional energy-storage circuit. A smaller footprint is designed to ease the space demand. Refer to the Application Note for such a design.

9.2.2.4 Delay Programming

From the power-stage design, the required turn-on delay (t_{DEL}) of the gate-drive signals is defined. The corresponding R_{DEL} resistor value to implement this delay is given by Equation 19 and Equation 20.

$$R_{DEL} = \left(t_{DEL1} - 15 \times 10^{-9}\right) 9.01 \times 10^{10} \tag{19}$$

or

$$R_{DEL} = \left(t_{DEL2} - 15 \times 10^{-9}\right) 9.01 \times 10^{10} \tag{20}$$

9.2.2.5 Input Voltage Monitoring

The input-voltage monitoring functions is governed by the following two expressions (see Equation 21 and Equation 22) of the voltage at the LINEUV pi.

$$V_{LINEUV} = V_{ON} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}} \text{ at turn on, and} \tag{21}$$

$$V_{LINEUV} = V_{OFF} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}} + I_{HYST} \times \frac{R_{IN1} \times R_{IN2}}{R_{IN1} + R_{IN2}} \text{ at turn off.} \tag{22}$$

Since V_{ON} and V_{OFF} are given by the power-supply specification, V_{LINEUV} equals the 1.27-V threshold of the line monitor and I_{HYST} is already defined in Equation 23.

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \tag{23}$$

The two unknown, R_{IN1} and R_{IN2} are fully determined (see Equation 24 and Equation 25).

$$R_{IN1} = \frac{V_{ON} - V_{OFF}}{I_{HYST}} \tag{24}$$

$$R_{IN2} = \frac{1.27\ V}{V_{ON} - 1.27\ V} \times R_{IN1} \tag{25}$$

9.2.2.6 Current Sense and Slope Compensation

The UCC2897A offers onboard user-programmable slope-compensation. The programming of the correct amount of slope compensation is accomplished by the appropriate selection of two external resistors, R_F and R_{SLOPE}.

First, the current-sense filter-resistor value (RF) must be calculated based on the desired filtering of the current-sense signal. The filter consists of two components, C_F and R_F. The C_F filter capacitor is connected between the CS pin and the GND pin. While the value of CF is selected freely as the first step of the filter design, the value of CF is minimized to avoid filtering the slope compensation current exiting the CS pin. The recommended range for the filter capacitance is between 50 pF and 270 pF. The value of the filter resistor is calculated from the filter capacitance and the desired filter corner frequency f_F.

$$R_F = \frac{1}{2\pi \times f_F \times C_F} \tag{26}$$

After RF is defined, RSLOPE is calculated. The amount of slope compensation is defined by the stability requirements of the inner-peak current-loop of the control algorithm and is measured by the number *m*. When the slope of the applied compensation ramp equals the down-slope of the output-inductor current waveform reflected across the primary-side current-sense resistor (dV_L / dt), *m* = 1. The minimum value of *m* is 0.5 to prevent current-loop instability. The best current-mode performance is achieved around *m* = 1. The increase of *m* moves the control closer to the voltage-mode control operation.

In the UCC2897A controllers, slope compensation is implemented by sourcing a linearly-increasing current at the CS pin. When this current passes through the current-sense filter resistor (RF), the current converts to a slope-compensation ramp which is characterized by (dV_S / dt). The (dV_S / dt) of the slope-compensation current is defined by R_{SLOPE} according to Equation 27.

$$\frac{dI_S}{dt} = \frac{5 \times 2\ V}{t_{ON} \times R_{SLOPE}}$$

where

- 2 V is the peak-to-peak ramp amplitude of the internal oscillator waveform
- 5 is the multiplication factor of the internal current mirror

(27)

The voltage equivalent of the compensation ramp (dV_S / dt) is obtained easily by multiplying with R_F. After introducing the application specific *m* and (dV_L / dt) values, Equation 28 is rearranged for R_{SLOPE}.

$$R_{SLOPE} = \frac{5 \times 2\ V \times R_F}{t_{ON} \times m \times \left(\frac{dV_L}{dt}\right)} \tag{28}$$

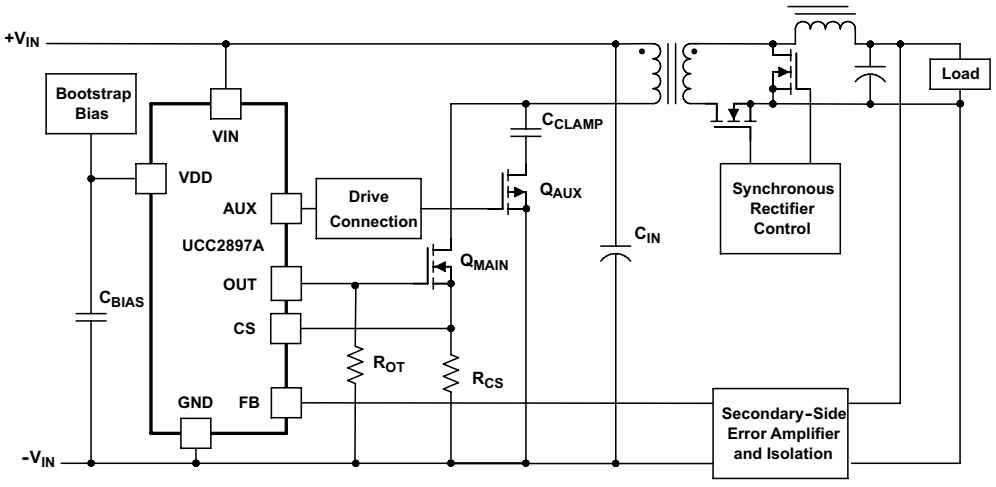


Figure 29. Active Clamp Forward Converter

9.2.3 Application Curves

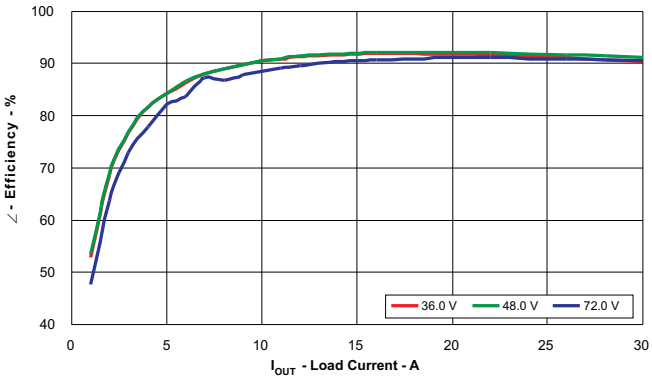


Figure 30. UCC2897A-EVM Efficiency

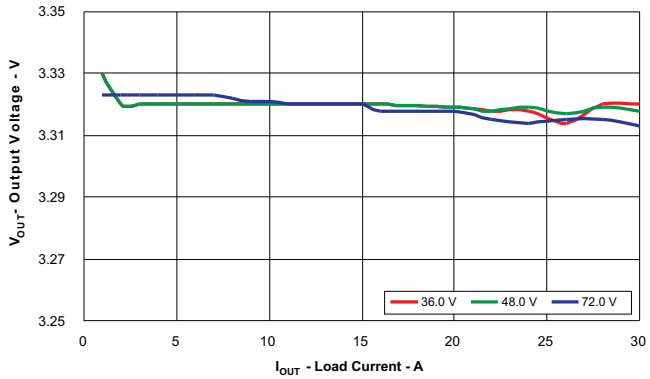


Figure 31. Line and Load Regulation

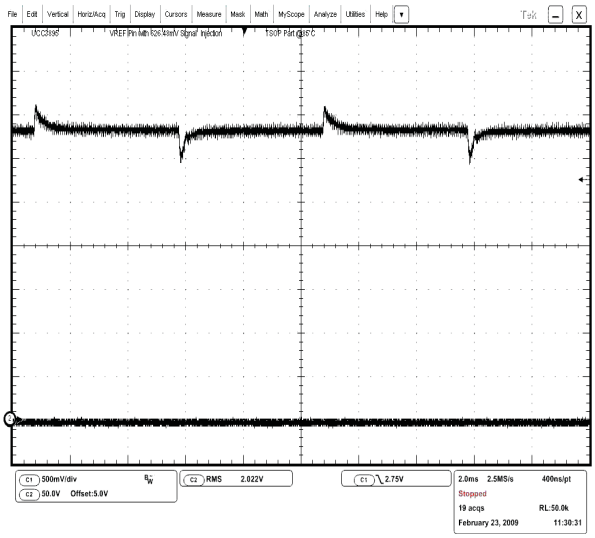


Figure 32. 10-A Load with 5-A Transient

10 Power Supply Recommendations

VDD pin is the power supply for the device. There should be a 1-µF capacitor directly from VDD to PGND. VREF pin provides the supply rail for internal logic, it should be by-passed to GND as close as possible to the device using a 0.1-µF capacitor. PVDD pin is the supply pin for the power devices, it should be by-passed to PGND using a 10-µF capacitor.

11 Layout

11.1 Layout Guidelines

- Connection of Two Grounds: GND (analog ground) and PGND (power ground). Two grounds should be connected using a net tie right between GND pin and PGND pin at IC, and there should be only this connection between two grounds.
- The bypass capacitors to the VDD pin and VREF pin should be as close as possible to the device GND.
- The timing configuration pins RDEL, RTON, RTOFF, and RSLOPE are connected to the device GND as close as possible.
- PGND should serve as the current return for the high current output drivers OUT and AUX. The current path should be as short as possible.
- Connect PVDD and VDD using a 0ohm resistor right at IC of these two pins.

11.2 Layout Example

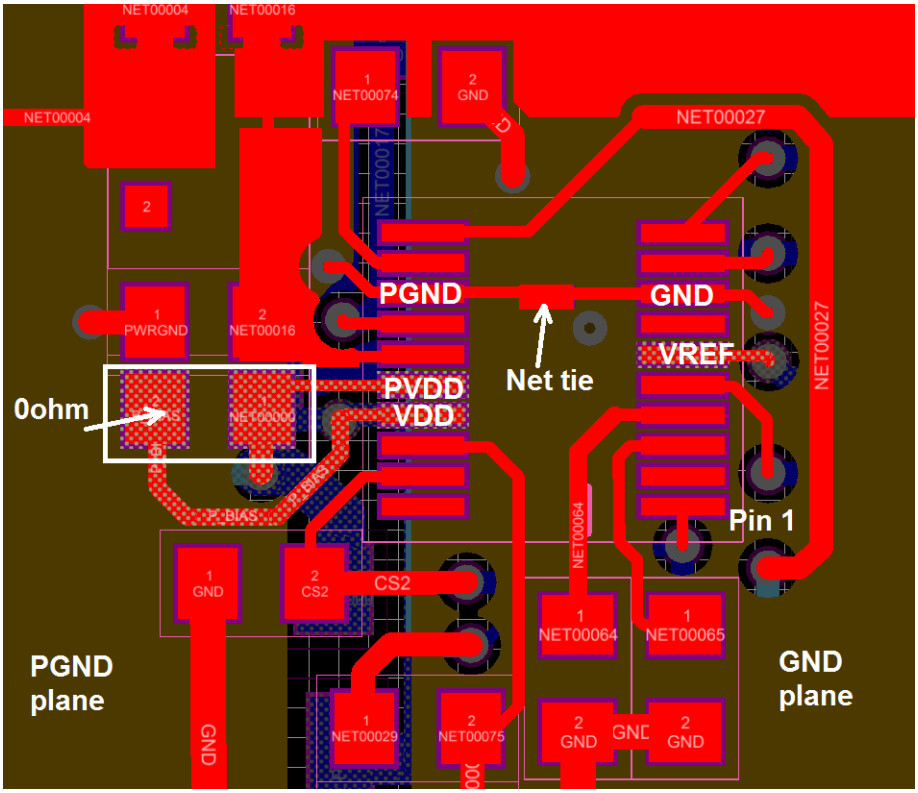


Figure 33. Layout Example Top Layer

Layout Example (continued)

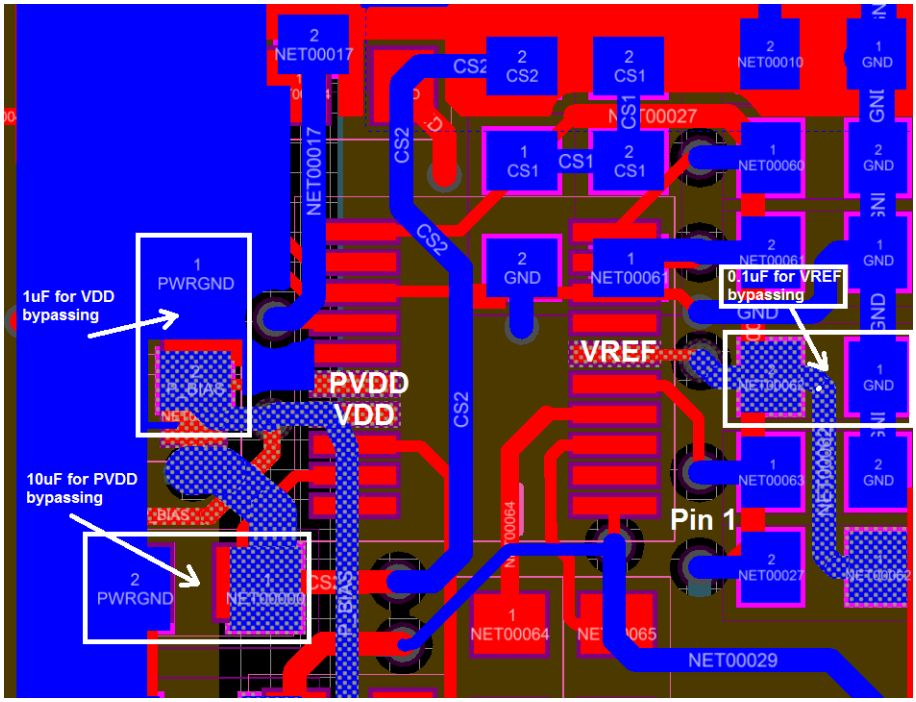


Figure 34. Layout Example Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

1. Evaluation Module: *UCC2891EVM, 48-V to 3.3-V, 30-A Forward Converter with Active Clamp Reset*. (SLUU407).
2. User's Guide: *Using the UCC2897AEVM, 48-V to 3.3-V Forward Converter with Active Clamp Reset* (SLUU357).
3. Application Note: *Understanding and Designing an Active Clamp Current Mode Controlled Converter* (SLUA535).
4. Power Supply Design Seminar Topic: *Design Considerations for Active Clamp and Reset Technique,* D. Dalal, SEM1100-Topic 3 (SLUP112).
5. Power Supply Design Seminar Topic: *Active Clamp and Reset Technique Enhances Forward Converter Performance*, B. Andreycak, SEM1000-Topic 3 (SLUP108).
6. Power Supply Design Seminar Topic: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, L. Balogh, SEM1400-Topic 2 (SLUP169).
7. Datasheet: *UCC3580, Single Ended Active-Clamp/Reset PWM Controller* (SLUS292).
8. Evaluation Module: *UCC3580EVM, Flyback Converters, Active Clamp vs. Hard-Switched* (SLUU085).
9. Reference Designs: Highly Efficient 100W Isolated Power Supply Reference Design Using UCC3580-1. Texas Instruments Hardware Reference Design Number PMP206.
10. Reference Designs: *Active Clamp Forward Reference Design using UCC3580-1*. Texas Instruments Hardware Reference Design Number PMP368
11. Application Note: *Method of Providing Hiccup Operation for UCC2897AEVM* (SLUA532)
12. Application Note: *External Slope Compensation for UCC2897A in Some Special Applications* (SLUA548)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TrueDrive, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2897APW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2897A
UCC2897APW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2897A
UCC2897APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2897A
UCC2897APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2897A
UCC2897ARGPR	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2897A
UCC2897ARGPR.B	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2897A
UCC2897ARGPT	Active	Production	QFN (RGP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2897A
UCC2897ARGPT.B	Active	Production	QFN (RGP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2897A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

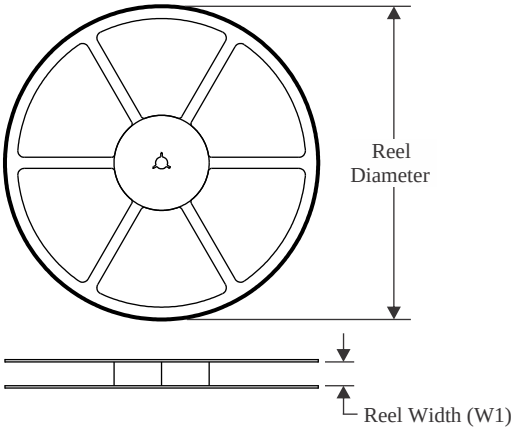
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

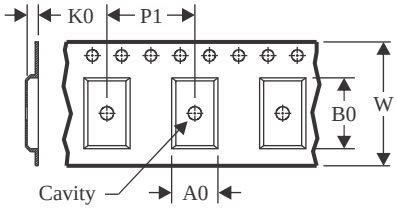
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

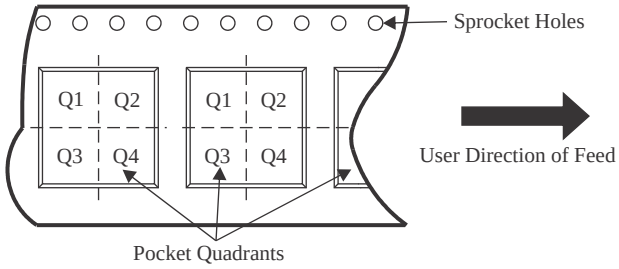


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

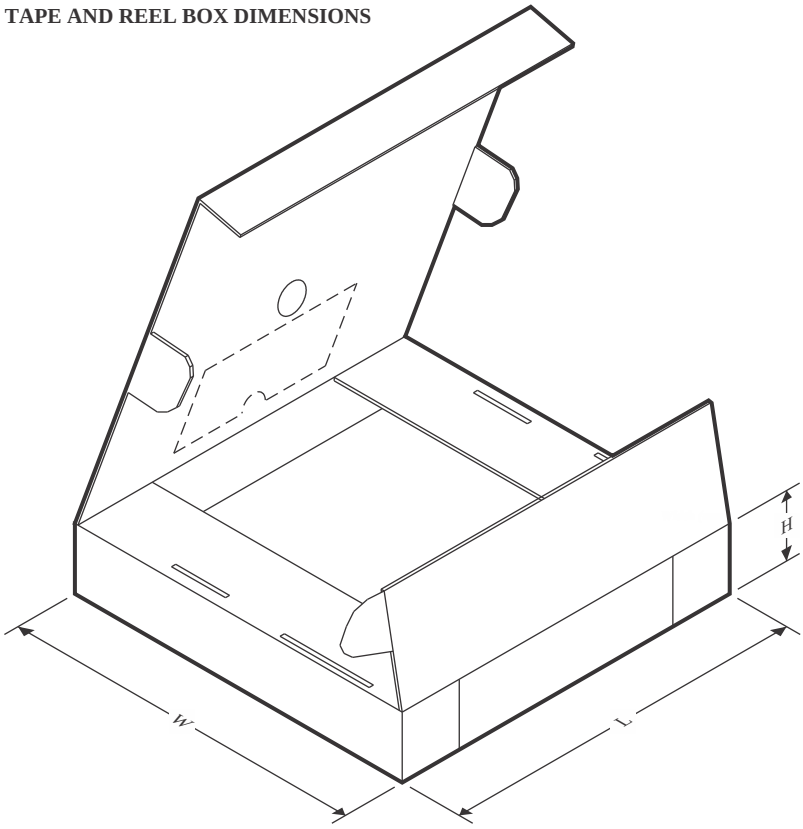
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2897APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
UCC2897ARGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC2897ARGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

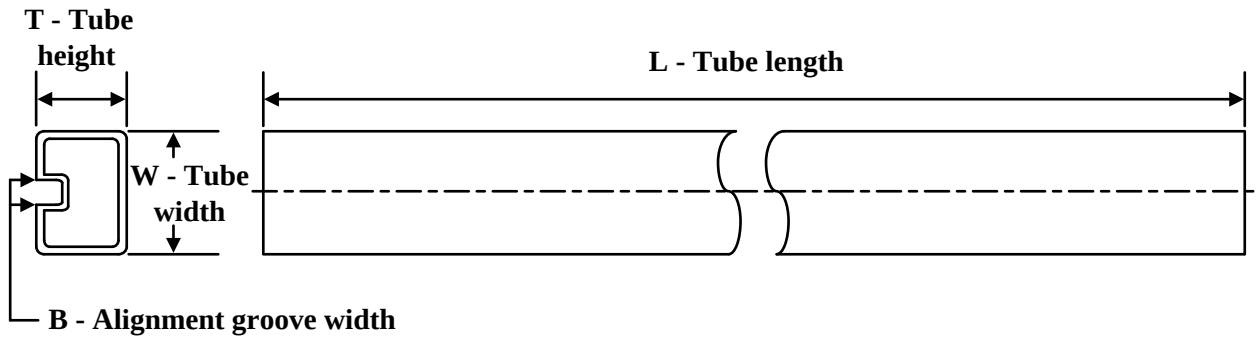
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2897APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
UCC2897ARGPR	QFN	RGP	20	3000	353.0	353.0	32.0
UCC2897ARGPT	QFN	RGP	20	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2897APW	PW	TSSOP	20	70	530	10.2	3600	3.5
UCC2897APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5

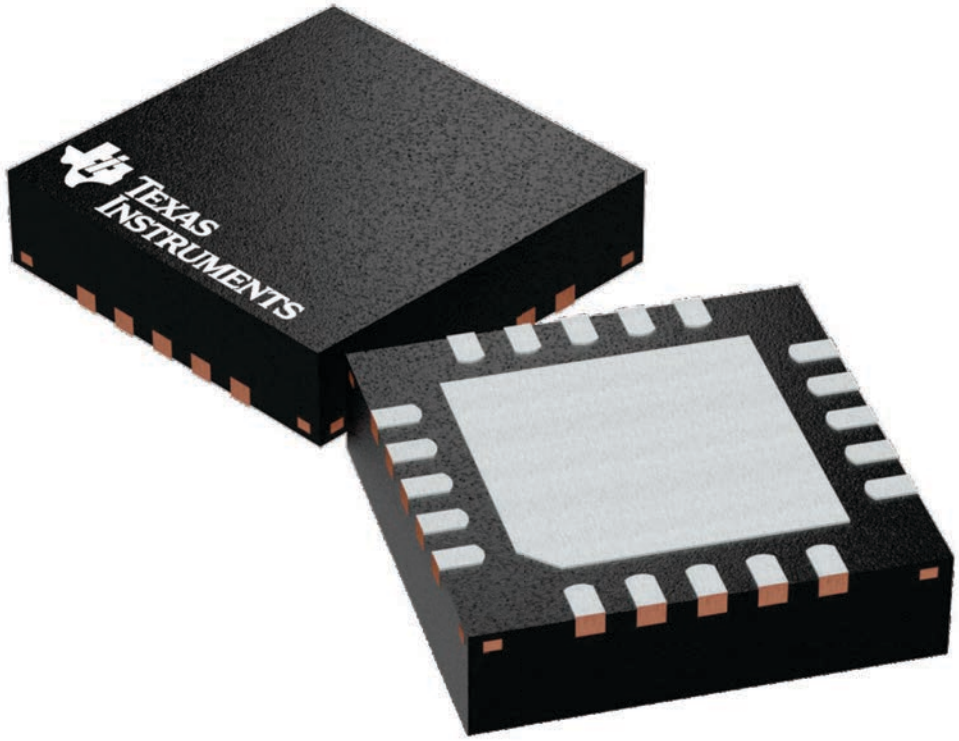
GENERIC PACKAGE VIEW

RGP 20

VQFN - 1 mm max height

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

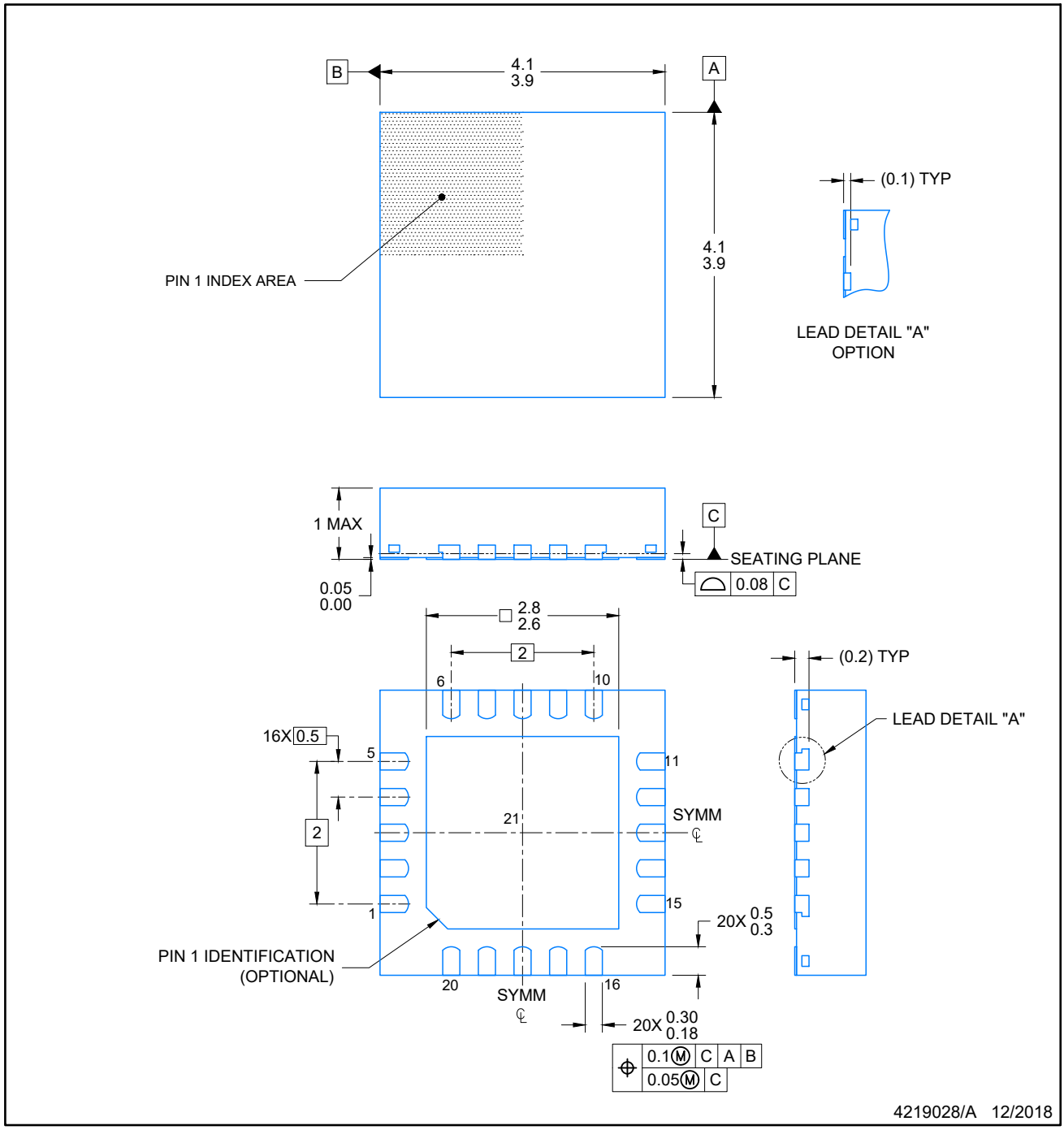
4224735/A

PACKAGE OUTLINE

RGP0020D

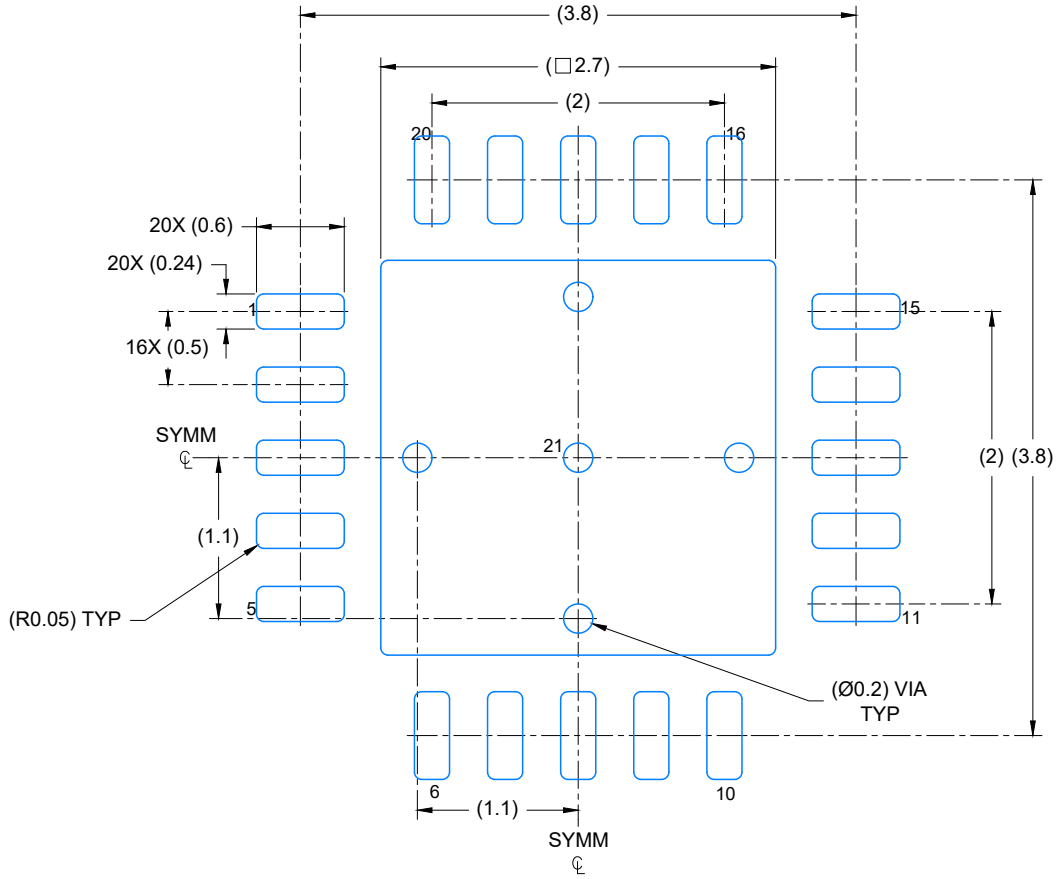
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

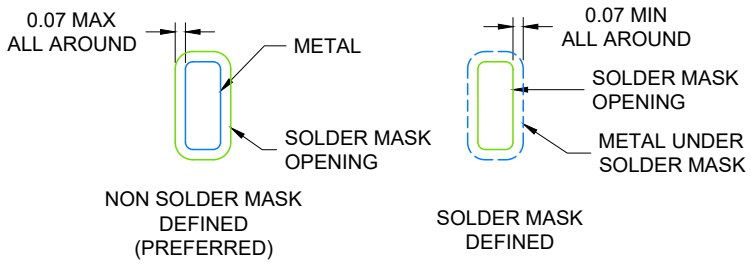


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

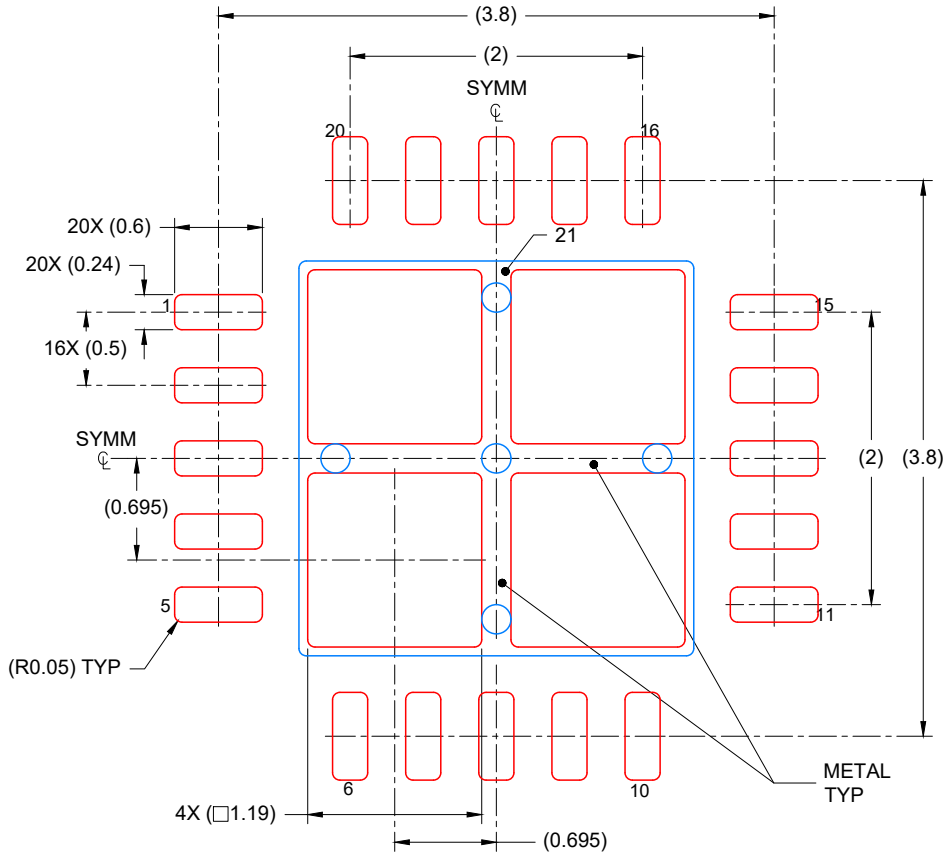


SOLDER MASK DETAILS

4219028/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED COVERAGE BY AREA
SCALE: 20X

4219028/A 12/2018

NOTES: (continued)

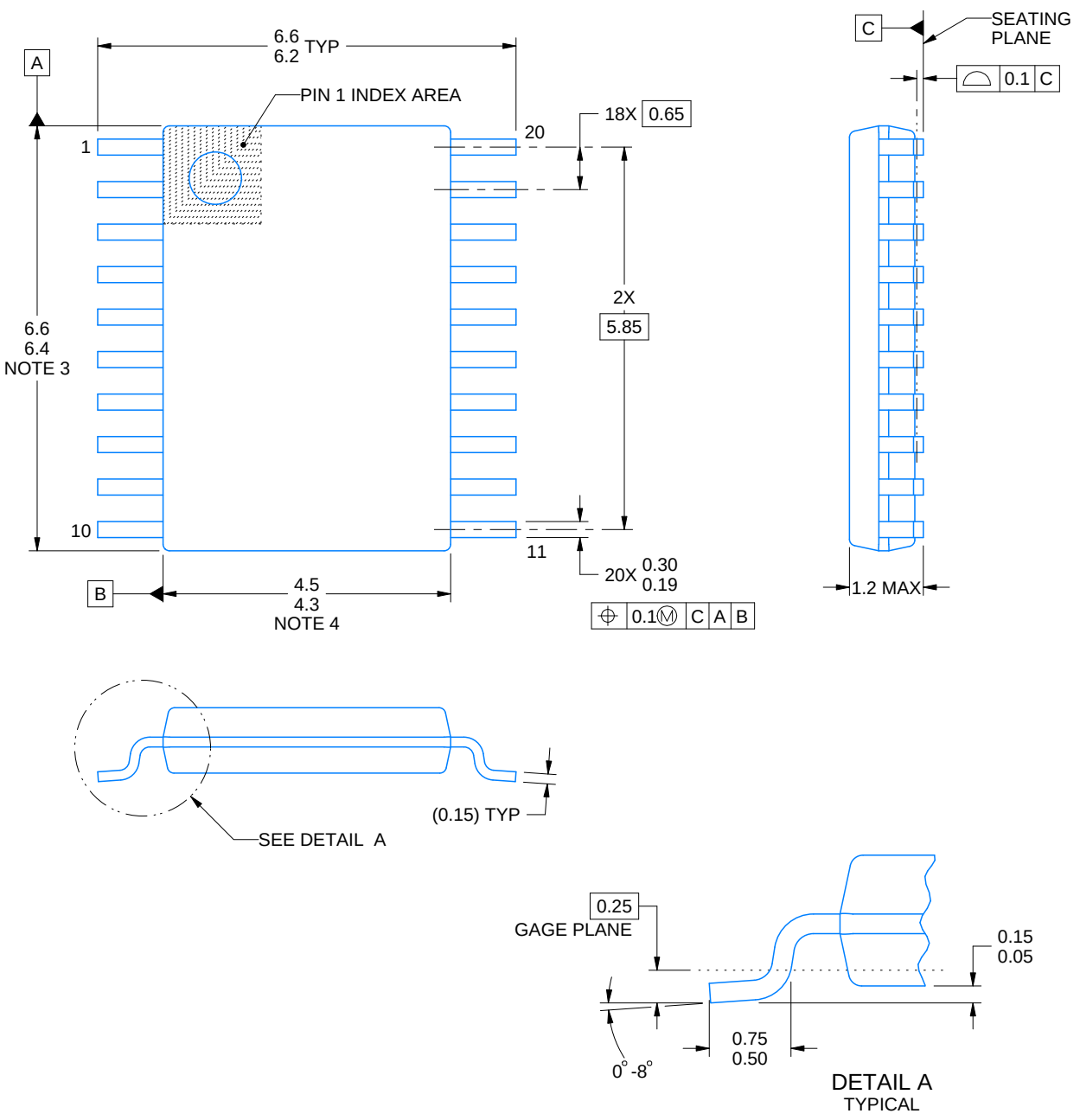
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0020A

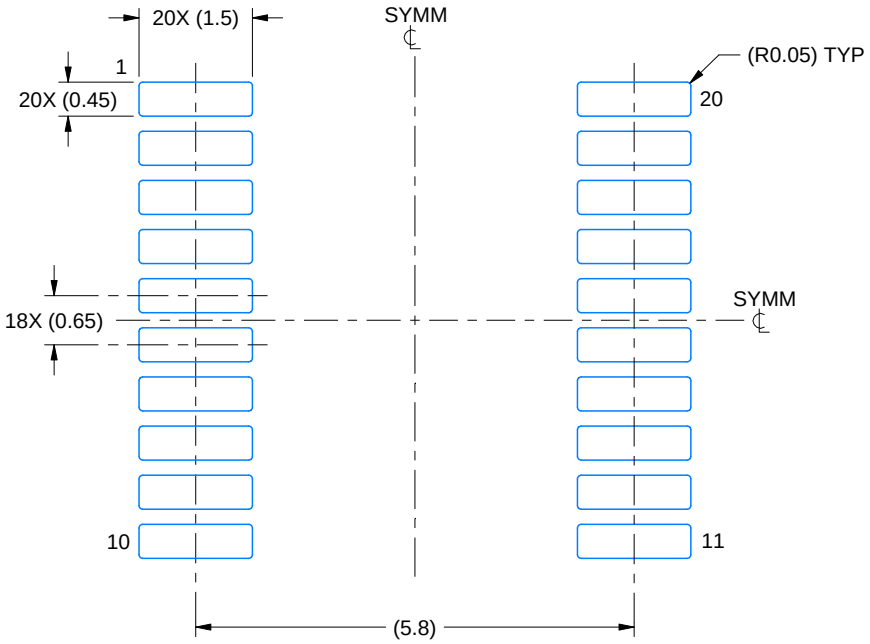
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



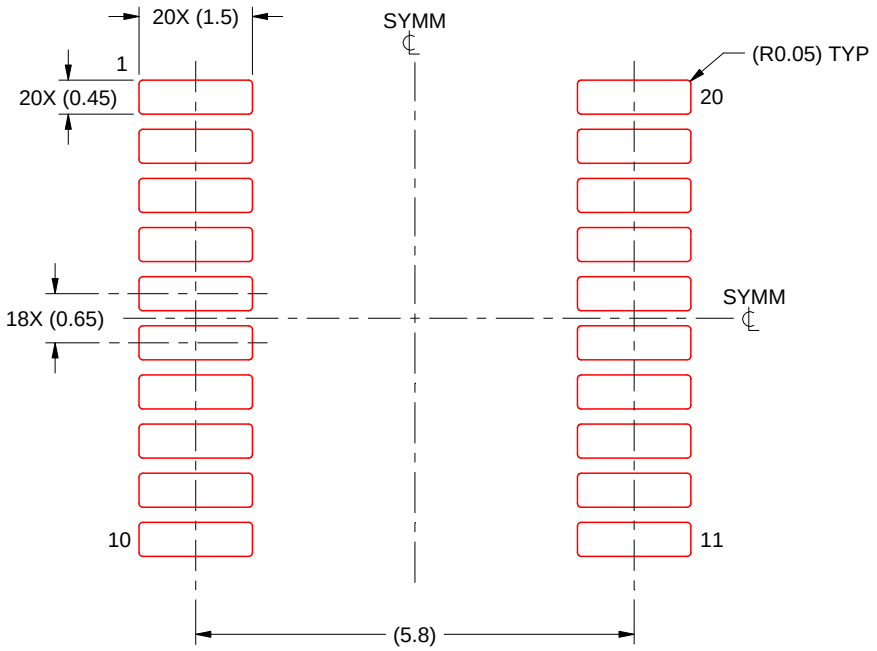
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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