TEXAS INSTRUMENTS
UCC28730-Q1
JAJSDB5 – JUNE 2017

UCC28730-Q1 *Zero-Power*車載用スタンバイPSR フライバック・コントローラ

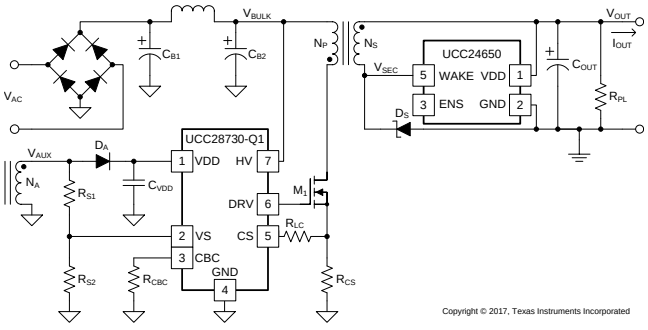
1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード1: -40℃～+125℃
  - デバイスHBM分類レベル2: ±2kV
  - デバイスCDM分類レベルC4B: ±750V
- *Zero-Power*: 5mW未満の待機電力を実現
- 1次側レギュレーション(PSR)によりオプトカプラが不要
- ラインおよび負荷範囲全体にわたる±5%の電圧レギュレーションおよび電流レギュレーション
- 700Vのスタートアップ・スイッチ
- 83kHzの最大スイッチング周波数により低待機電力の充電器を設計可能
- 共振リング・バレー・スイッチング動作により全体効率を最大化
- EMI準拠を容易にする周波数ディザリング
- クランプされたMOSFETゲート駆動出力
- 過電圧、低ライン、および過電流保護機能
- プログラミング可能なケーブル補償
- SOIC-7パッケージ

2 アプリケーション

- 車載用電源
- ハイブリッドおよび電気自動車
- 家電および産業用オートメーション向けSMPS
- スタンバイ電源、補助電源

概略回路図



3 概要

UCC28730-Q1絶縁フライバック電源コントローラは、オプトカプラを使用せず、定電圧(CV)および定電流(CC)出力レギュレーションを行います。30Hzの最小スイッチング周波数により、5mW未満の無負荷時消費電力を容易に実現できます。1次側電源スイッチおよび補助フライバック巻線からの情報を処理することで、出力電圧および電流を精密に制御します。

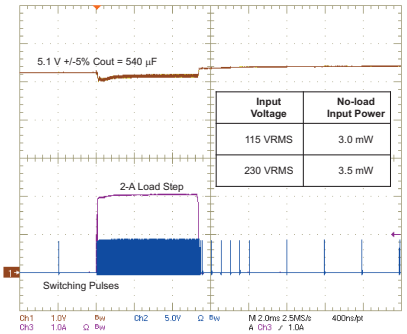
内部の700Vスタートアップ・スイッチ、動的に制御される動作状態、および適切に調整された変調プロファイルにより、スタートアップ時間や出力過渡応答を犠牲にすることなく、非常に低い待機電力を実現します。UCC28730-Q1の制御アルゴリズムによって、適用される規格に準拠またはそれを上回る動作効率を実現できます。バレー・スイッチングによる不連続導通モード(DCM)動作でスイッチング損失が低減されます。スイッチング周波数の変調(FM)および1次側電流のピーク振幅の変調(AM)により、負荷およびライン範囲の全体にわたって高い変換効率を保持します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
UCC28730-Q1	SOIC (7)	4.90mm×3.90mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

*Zero-Power*入力消費電力(無負荷時)



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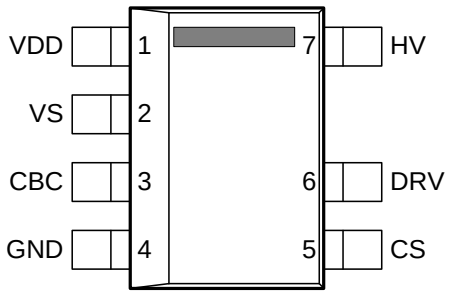
4 改訂履歴

日付	改訂内容	注
2017年6月	*	初版

5 Pin Configuration and Functions

D Package
7-Pin SOIC
Top View



Pin Functions(1)

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	P	VDD is the bias supply input pin to the controller. A carefully-placed by-pass capacitor to GND is required on this pin.
VS	2	I	Voltage Sense is an input used to provide voltage feed-back and demagnetization timing to the controller for output voltage regulation, frequency limiting, constant-current control, line voltage detection, and output over-voltage detection. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin. This input also detects a qualified *wake-up* signal when operating in the Wait state.
CBC	3	I	CaBle Compensation is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.
GND	4	G	The GrouND pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with power and signal return paths.
CS	5	I	Current Sense input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the rectified bulk voltage varies.
DRV	6	O	DRiVe is an output used to drive the gate of an external high-voltage MOSFET switching transistor.
HV	7	I	The High Voltage pin connects directly to the rectified bulk voltage and provides charge to the VDD capacitor for start-up of the power supply.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	HV		700	V
	VDD		38	V
	VS	–0.75	7	V
	CS, CBC	–0.5	5	V
	DRV	–0.5	Self-limiting	V
Current	DRV, continuous sink		50	mA
	DRV, source		Self-limiting	mA
	VS, peak, 1% duty-cycle		–1.2	mA
Lead temperature 0.6 mm from case for 10 seconds		–65	150	°C
Storage temperature, T_{stg}			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	9		35	V
C_{VDD}	VDD by-pass capacitor	0.047			µF
R_{CBC}	Cable-compensation resistance	10			kΩ
I_{VS}	VS pin current, out of pin			1	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28730-Q1 D (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, R_{CBC} = open, T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
HIGH-VOLTAGE START-UP						
I_{HV}	Start-up current out of VDD	V_{HV} = 100 V, V_{VDD} = 0 V, start state	100	250	500	µA
$I_{HVLKG25}$	Leakage current into HV	V_{HV} = 400 V, run state, T_J = 25°C		0.01	0.5	µA
BIAS SUPPLY INPUT CURRENT						
I_{RUN}	Supply current, run	Run state, I_{DRV} = 0 A		2.1	2.65	mA
I_{WAIT}	Supply current, wait	Wait state, I_{DRV} = 0 A, V_{VDD} = 20 V		52	75	µA
I_{START}	Supply current, start	Start state, I_{DRV} = 0 A, V_{VDD} = 18 V, I_{HV} = 0 A		18	30	µA
I_{FAULT}	Supply current, fault	Fault state, I_{DRV} = 0 A		54	75	µA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	17.5	21	23	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.3	7.7	8.1	V
VS Input and *Wake-Up* Monitor						
V_{VSR}	Regulating level(1)	Measured at no-load condition, T_J = 25°C	4.00	4.04	4.08	V(1)
V_{VSNC}	Negative clamp level below GND	I_{VSLS} = –300 µA	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
$V_{WU(high)}$	*Wake-up* threshold at VS, high(2)	VS pin rising		2		V(2)
$V_{WU(low)}$	*Wake-up* threshold at VS, low	VS pin rising	15	57	105	mV
CS INPUT						
$V_{CST(max)}$	CS maximum threshold voltage(3)	V_{VS} = 3.7 V	710	740	770	mV(3)
$V_{CST(min)}$	CS minimum threshold voltage	V_{VS} = 4.35 V	230	249	270	mV
K_{AM}	AM control ratio, $V_{CST(max)}$ / $V_{CST(min)}$		2.75	2.99	3.20	V/V
V_{CCR}	Constant-current regulation factor		310	319	329	mV
K_{LC}	Line compensation current ratio, I_{VSLS} / current out of CS pin	I_{VSLS} = –300 µA	24	25.3	28	A/A
DRIVER						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	29	35	mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V	13	14.5	16	V
R_{DRVSS}	DRV pull-down in start state		150	190	230	kΩ

(1) The regulating level and OV threshold at VS decrease with increasing temperature by 1 mV/°C. This compensation over temperature is included to reduce the variances in power supply output regulation and over-voltage detection with respect to the external output rectifier.
(2) Designed for accuracy within ±10% of typical value.
(3) These threshold voltages represent average levels. This device automatically varies the current sense thresholds to improve EMI performance.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, R_{CBC} = open, T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVP}	Over-voltage threshold(1)	At VS input, T_J = 25°C	4.52	4.62	4.71	V(1)
V_{OCP}	Over-current threshold	At CS input	1.4	1.5	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	190	225	275	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	µA
K_{VSL}	VS line-sense ratio, $I_{VSL(run)}$ / $I_{VSL(stop)}$		2.45	2.8	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature		165		°C
CABLE COMPENSATION						
$V_{CBC(max)}$	Cable compensation output maximum voltage	Voltage at CBC at full load	2.9	3.13	3.5	V
$V_{CVS(min)}$	Minimum compensation at VS	V_{CBC} = open, change in VS regulating level from no load to full load	–50	–15	20	mV
$V_{CVS(max)}$	Maximum compensation at VS	V_{CBC} = 0 V, change in VS regulating level from no load to full load	275	325	375	mV

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{WUDLY}	*Wake-up* qualification delay, V_{VS} = 0 V	7.0	8.5	11.0	µs
t_{CSLEB}	Leading-edge blanking time , DRV output duration, V_{CS} = 1 V	170	225	280	ns
t_{ZTO}	Zero-crossing timeout delay, no zero-crossing detected	1.6	2.2	2.9	µs

6.7 Switching Characteristics

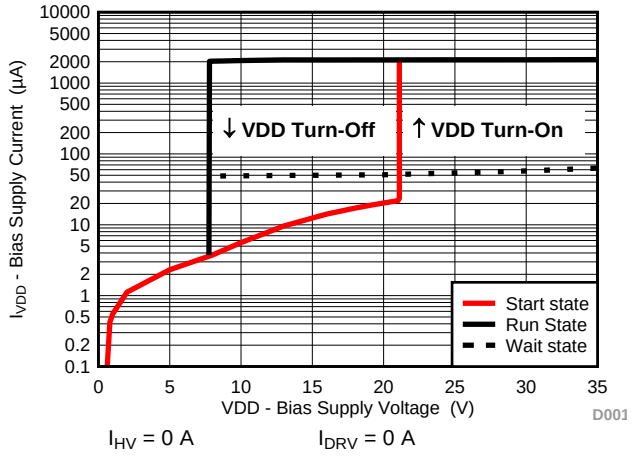
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency(1)	V_{VS} = 3.7 V	76.0	83.3	90.0	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.35 V	25	32	37	Hz

(1) These frequency limits represent average levels. This device automatically varies the switching frequency to improve EMI performance.

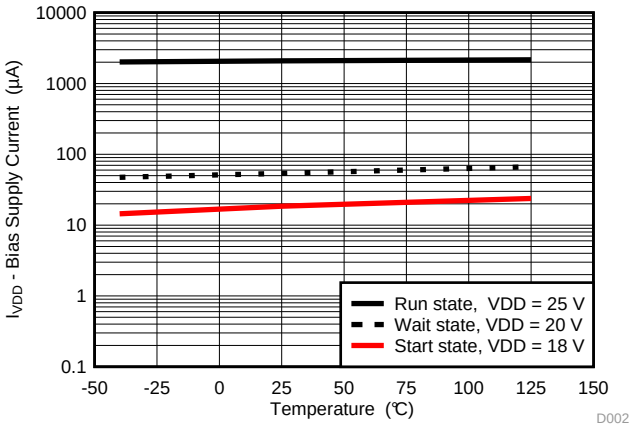
6.8 Typical Characteristics

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.



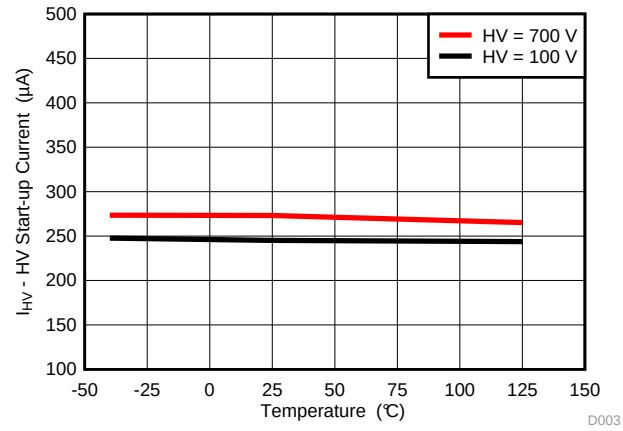
I_{HV} = 0 A I_{DRV} = 0 A

図 1. Bias Supply Current vs. Bias Supply Voltage



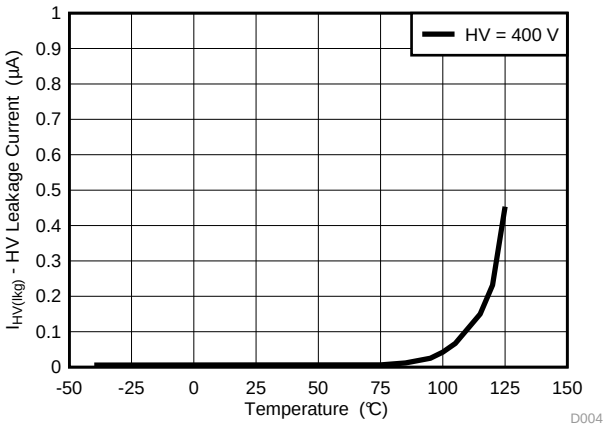
I_{HV} = 0 A I_{DRV} = 0 A

図 2. Bias Supply Current vs. Temperature



V_{VDD} = 0 V

図 3. HV Start-up Current vs. Temperature



V_{VDD} = 25 V

図 4. HV Leakage Current vs. Temperature

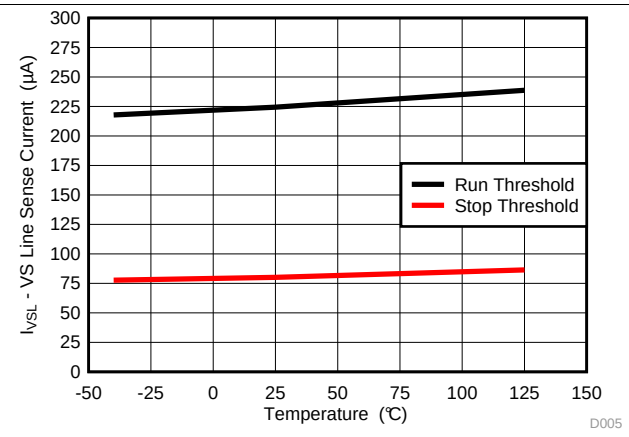


図 5. VS Line-Sense Current vs. Temperature

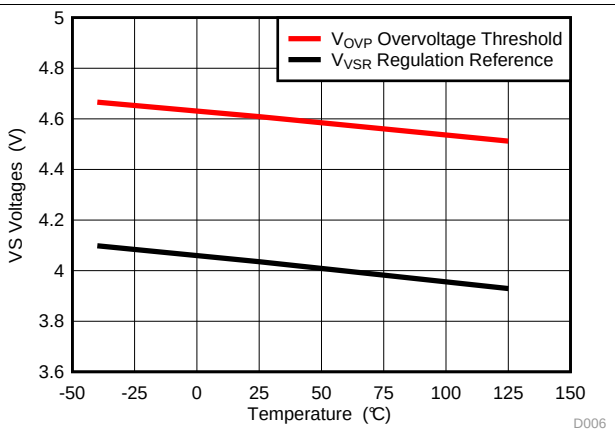


図 6. VS Voltages vs. Temperature

Typical Characteristics (continued)

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.

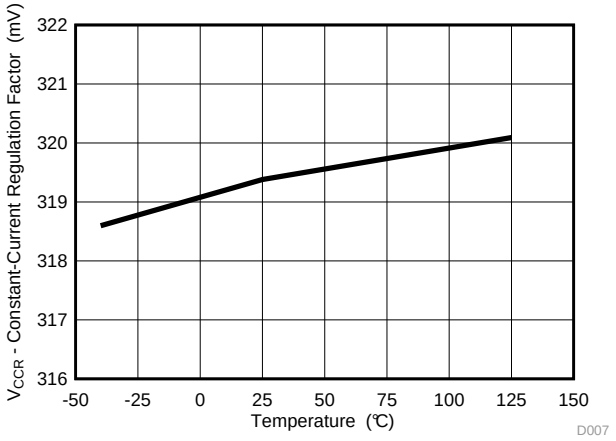


図 7. Constant-Current Regulation Factor vs. Temperature

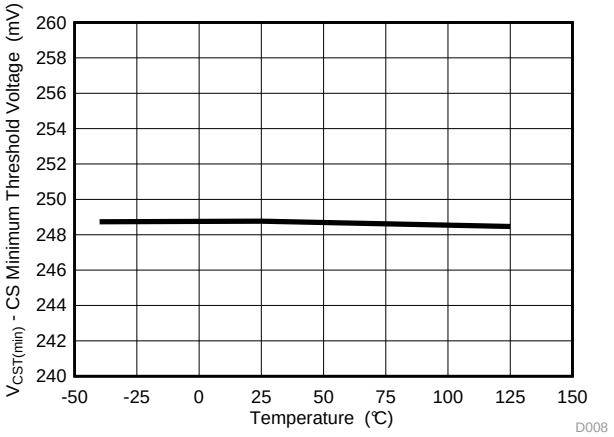
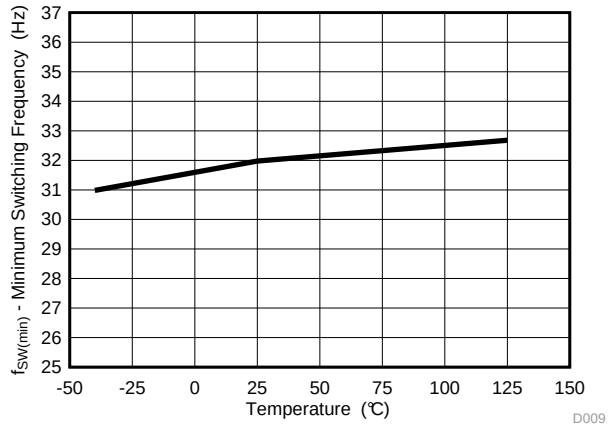
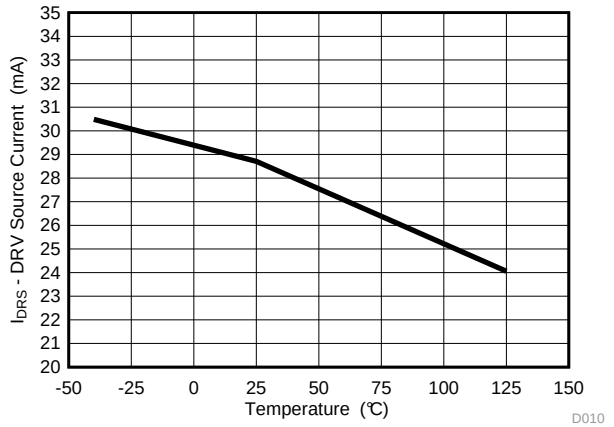


図 8. CS Minimum Threshold Voltage vs. Temperature



V_{VS} = 4.35 V

図 9. Minimum Switching Frequency vs. Temperature



V_{VDD} = 9 V V_{DRV} = 8 V

図 10. DRV Source Current vs. Temperature

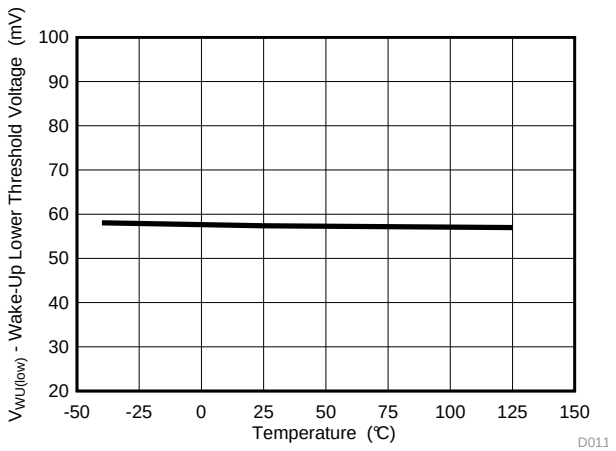
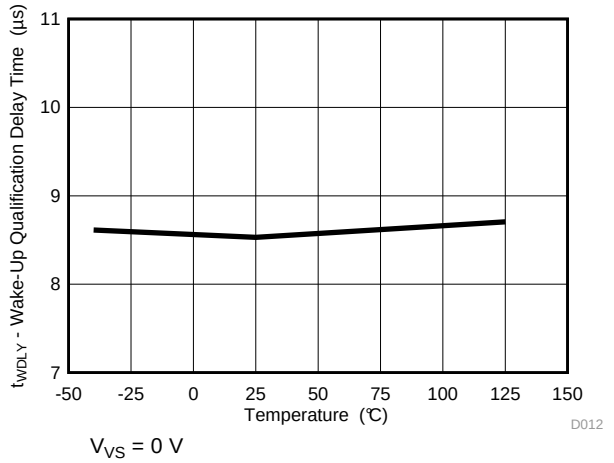


図 11. *Wake-Up* Lower Threshold Voltage vs. Temperature



V_{VS} = 0 V

図 12. *Wake-Up* Qualification Delay Time vs. Temperature

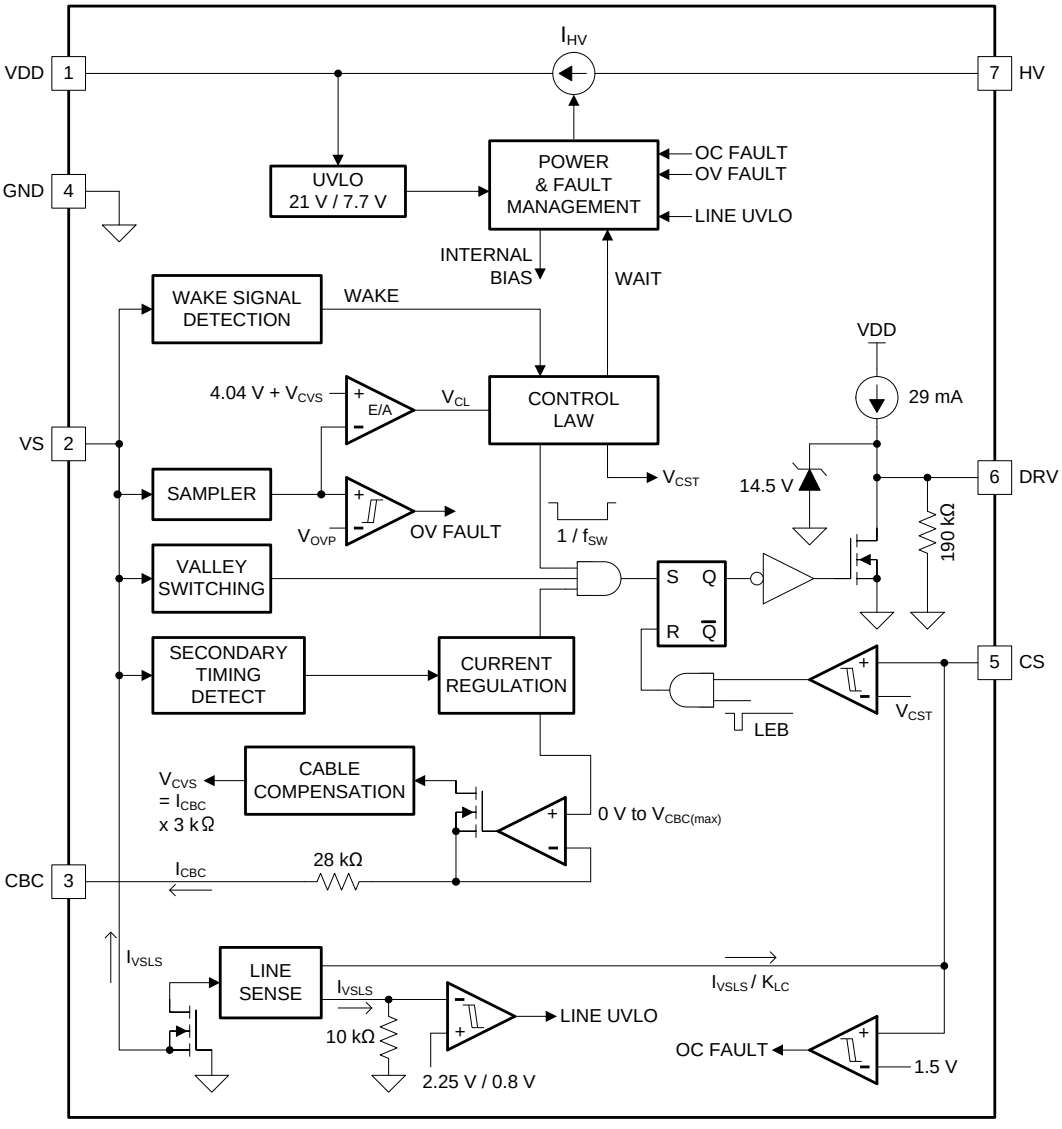
7 Detailed Description

7.1 Overview

The UCC28730-Q1 is an isolated-flyback power supply controller which provides accurate voltage and constant current regulation using primary-side winding sensing, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency modulation and primary peak-current modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which facilitates the achievement of <5-mW stand-by power.

During low-power operating levels the device has power management features to reduce the device operating current at switching frequencies less than 28 kHz. The UCC28730-Q1 includes features in the pulse-width modulator to reduce the EMI peak energy at the fundamental switching frequency and its harmonics. Accurate voltage and current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost, and low component-count.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Pin Description

7.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin connects to a by-pass capacitor to ground. The turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 7.7 V with an available operating range up to 35 V on VDD. The typical USB charging specification requires the output current to operate in Constant-Current mode from 5 V down to at least 2 V, which is easily achieved with a nominal V_{VDD} of approximately 20 V. The additional VDD headroom up to 35 V allows for V_{VDD} to rise due to the leakage energy delivered to the VDD capacitor during high-load conditions.

7.3.1.2 GND (Ground)

UCC28730-Q1 has a single ground reference external to the device for the gate-drive current and analog signal reference. Place the VDD-bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

7.3.1.3 HV (High Voltage Startup)

The HV pin connects directly to the bulk capacitor to provide startup current to the VDD capacitor. The typical startup current is approximately 250 µA which provides fast charging of the VDD capacitor. The internal HV startup device is active until V_{VDD} exceeds the turn-on UVLO threshold of 21 V at which time the HV startup device turns off. In the off state the HV leakage current is very low to minimize stand-by losses of the controller. When V_{VDD} falls below the 7.7-V UVLO turn-off threshold the HV startup device turns on.

7.3.1.4 DRV (Gate Drive)

The DRV pin connects to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turn-on characteristic of the driver is a 29-mA current source which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, while still providing a gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the $R_{DS(on)}$ of the low-side driver and any external gate drive resistance. Adding external gate resistance reduces the MOSFET drain turn-off dv/dt, if necessary. Such resistance value is generally higher than the typical 10 Ω commonly used to damp resonance. However, calculation of the external resistance value to achieve a specific dv/dt involves MOSFET parameters beyond the scope of this datasheet.

7.3.1.5 CBC (Cable Compensation)

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation needed to offset cable resistance. The cable compensation circuit generates a 0 to 3.13-V voltage level on the CBC pin corresponding to 0 A to I_{OCC} maximum output current. The resistance selected on the CBC pin programs a current mirror that is summed into the VS feedback divider therefore increasing the regulation voltage as I_{OUT} increases. There is an internal series resistance of 28 kΩ to the CBC pin which sets a maximum cable compensation for a 5-V output to approximately 400 mV when CBC is shorted to ground. The CBC resistance value can be determined using 式 1.

$$R_{CBC} = \frac{V_{CBC\,(max)} \times (V_{OCV} + V_F) \times 3\ k\Omega}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \quad (1)$$

where

- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see Electrical Characteristics),
- V_{OCV} is the regulated output voltage,
- V_F is the diode forward voltage,
- V_{VSR} is the CV regulating level at the VS input (see Electrical Characteristics),
- V_{OCBC} is the target cable compensation voltage at the output terminals.

Note that the cable compensation does not change the overvoltage protection (OVP) threshold, V_{OVP} (see Electrical Characteristics), so the operating margin to OVP is less when cable compensation is used.

Feature Description (continued)

7.3.1.6 VS (Voltage Sense)

The VS pin connects to a resistor-divider from the auxiliary winding to ground and is used to sense input voltage, output voltage, event timing, and Wait-state *wake-up* signaling. The auxiliary voltage waveform is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. The waveform on the VS pin determines the timing information to achieve valley-switching, and the timing to control the duty-cycle of the transformer secondary current when in Constant-Current Mode. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.

During the MOSFET on-time, this pin also senses VS current generated through R_{S1} by the reflected bulk-capacitor voltage to provide for AC-input Run and Stop thresholds, and to compensate the current-sense threshold across the AC-input range. For the AC-input Run/Stop function, the Run threshold on VS is 225 µA and the Stop threshold is 80 µA.

At the end of off-time demagnetization, the reflected output voltage is sampled at this pin to provide regulation and overvoltage protection. The values for the auxiliary voltage-divider upper-resistor, R_{S1}, and lower-resistor, R_{S2}, are determined by 式 2 and 式 3.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \quad (2)$$

where

- $V_{IN(run)}$ is the target AC RMS voltage to enable turn-on of the controller (Run) (in case of DC input, leave out the √2 term in the equation),
- $I_{VSL(run)}$ is the Run-threshold for the current pulled out of the VS pin during the switch on-time (see Electrical Characteristics),
- N_{PA} is the transformer primary-to-auxiliary turns-ratio.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (3)$$

where

- V_{OCV} is the converter regulated output voltage,
- V_F is the output rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary-to-secondary turns-ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{VSR} is the CV regulating level at the VS input (see Electrical Characteristics).

When the UCC28730-Q1 is operating in the Wait state, the VS input is receptive to a *wake-up* signal superimposed upon the auxiliary winding waveform after the waveform meets either of two qualifying conditions. A high-level *wake-up* signal is considered to be detected if the amplitude at the VS input exceeds $V_{WU(high)}$ (2 V) provided that any voltage at VS has been continuously below $V_{WU(high)}$ for the *wake-up* qualification delay t_{WDLY} (8.5 us) after the demagnetization interval. A low-level *wake-up* signal is considered to be detected if the amplitude at the VS input exceeds $V_{WU(low)}$ (57 mV) provided that any voltage at VS has been continuously below $V_{WU(low)}$ for the *wake-up* qualification delay t_{WDLY} (8.5 us) after the demagnetization interval. The high-level threshold accommodates signals generated by a low-impedance secondary-side driver while the low-level threshold detects signals generated by a high-impedance driver.

Feature Description (continued)

7.3.1.7 CS (Current Sense)

The current-sense pin connects to a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The maximum current-sense threshold ($V_{CST(max)}$) is approximately 0.74 V for $I_{PP(max)}$ and minimum current-sense threshold ($V_{CST(min)}$) is approximately 0.25 V for $I_{PP(min)}$. R_{LC} provides the function of feed-forward line compensation to eliminate changes in I_{PP} with input voltage due to the propagation delay of the internal comparator and MOSFET turn-off time. An internal leading-edge blanking time of 225 ns eliminates sensitivity to the MOSFET turn-on current spike. It should not be necessary to place a bypass capacitor on the CS pin. The target output current in constant-current (CC) regulation determines the value of R_{CS}. The values of R_{CS} and R_{LC} are calculated by 式 4 and 式 5. The term V_{CCR} is the product of the demagnetization constant, 0.432, and $V_{CST(max)}$. V_{CCR} is held to a tighter accuracy than either of its constituent terms. The term η_{XFMR} accounts for the energy stored in the transformer but not delivered to the secondary. This term includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example: With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias-power to output-power ratio of 0.5%, the η_{XFMR} value at full-power is: 1 - 0.05 - 0.035 - 0.005 = 0.91.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}}$$

where

- V_{CCR} is a constant-current regulation factor (see Electrical Characteristics),
- N_{PS} is the transformer primary-to-secondary turns-ratio, (a ratio of 13 to 15 is typical for a 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency at full-power output. (4)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times N_{PA} \times t_D}{L_P}$$

where

- K_{LC} is a current-scaling constant for line compensation (see Electrical Characteristics),
- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- t_D is the total current-sense delay consisting of MOSFET turn-off delay, plus approximately 50-ns internal delay,
- L_P is the transformer primary inductance. (5)

7.3.2 Primary-Side Regulation (PSR)

図 13 illustrates a simplified isolated-flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control. The output voltage is sensed as a reflected voltage during the transformer demagnetization time using a divider network at the VS input. The primary winding current is sensed at the CS input using a current-sense resistor, R_{CS}.

Feature Description (continued)

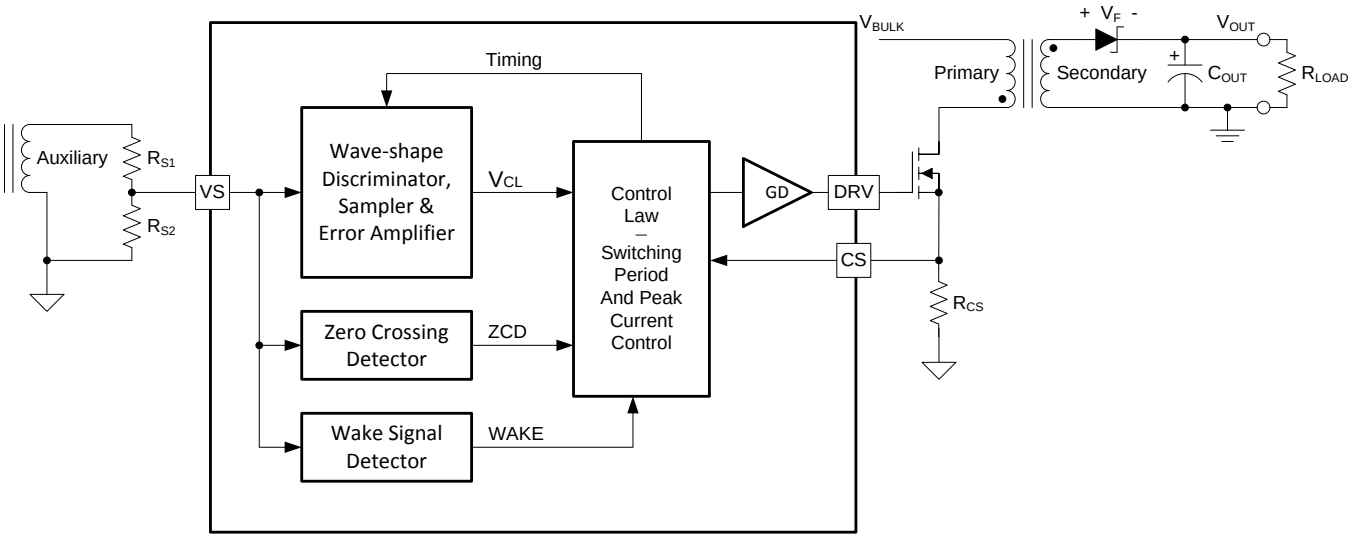


図 13. Simplified Flyback Convertor (with the main voltage regulation blocks)

In primary-side control, the output voltage is indirectly sensed on the auxiliary winding at the end of the transfer of stored transformer energy to the secondary. As shown in 図 14 it is clear there is a down slope representing a decreasing total rectifier V_F and resistance voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.04 V. Temperature compensation on the VS reference voltage of -1 mV/°C offsets the change in the forward voltage of the output rectifier with temperature. The resistor divider is selected as outlined in the VS pin description.

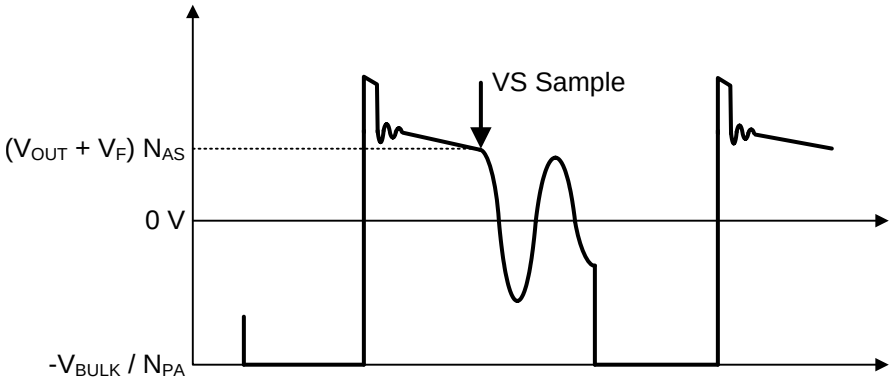


図 14. Auxiliary Winding Voltage

The UCC28730-Q1 VS-signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are, however, some details of the auxiliary winding signal which require attention to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to 図 15 below for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin.

Feature Description (continued)

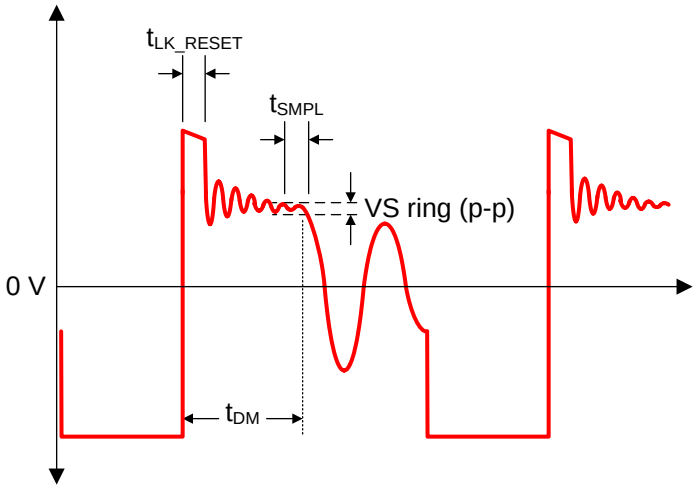


図 15. Auxiliary Waveform Details

The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET} in 図 15. Since this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time to less than 750 ns for I_{PRI} minimum, and to less than 2.25 µs for I_{PRI} maximum.

The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than 125 mV for at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light-load or no-load conditions, when t_{DM} is at the minimum. To avoid distorting the signal waveform at VS with oscilloscope probe capacitance, it is recommended to probe the auxiliary winding to view the VS waveform characteristics. The tolerable ripple on VS is scaled up to the auxiliary-winding voltage by R_{S1} and R_{S2}, and is equal to 125 mV x (R_{S1} + R_{S2}) / R_{S2}.

Feature Description (continued)

7.3.3 Primary-Side Constant Voltage Regulation

During voltage regulation, the controller operates in frequency modulation and amplitude modulation modes according to the control law as illustrated in 図 16 below. The control law voltage V_{CL} reflects the internal operating level based on the voltage-error amplifier output signal. Neither of these signals is accessible to the user, however the approximate V_{CL} may be inferred from the frequency and amplitude of the current sense signal at the CS input. As the line and load conditions vary, V_{CL} adjusts the operating frequency and amplitude as required to maintain regulation of the output voltage. Because the UCC28730-Q1 incorporates internal loop compensation, no external stability compensation is required.

The internal operating frequency limits of the device are $f_{SW(max)}$ and $f_{SW(min)}$, typically 83.3 kHz and 32 Hz, respectively. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{SW(max)}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switched-node capacitance losses, other switching and conduction losses, and bias-supply requirements. In any case, the minimum steady-state frequency of the converter must always exceed $f_{SW(min)}$ or the output voltage may rise to the overvoltage protection level (OVP) and the controller responds as described in the Fault Protection Section.

The steady-state Control-Law voltage, V_{CL}, ranges between 1.3 to 4.85 V, depending on load, but may occasionally move below 0.75 V or above 4.85 V on load transients. Dropping below 0.75 V shifts the switching frequency to a lower range at light loads, while exceeding 4.85 V enters the constant-current mode of operation. There are 3 lower operating frequency ranges for progressively lighter loads, each overlapping the previous range to some extent, to provide stable regulation at very low frequencies. Peak-primary current is always maintained at $I_{PP(max)}/3$ in these lower frequency levels. Transitions between levels is automatically accomplished by the controller depending on the internal control-law voltage, V_{CL}.

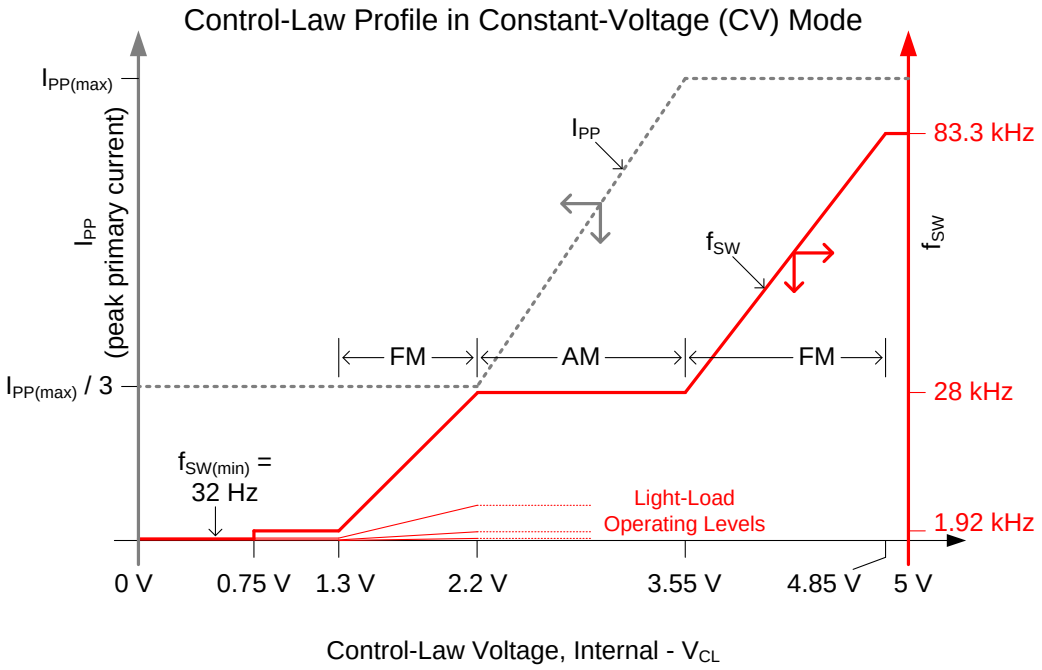


図 16. Frequency and Amplitude Modulation Modes (during voltage regulation)

Feature Description (continued)

7.3.4 Primary-Side Constant Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current will be at $I_{PP(max)}$. Referring to 図 17 below, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by 式 6.

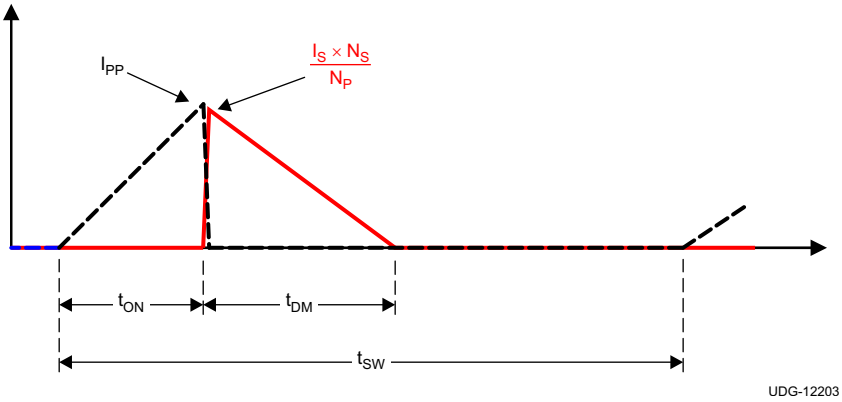


図 17. Transformer Currents Relationship

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (6)$$

When the average output current reaches the CC regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current, I_{OCC}, at any output voltage down to or below the minimum operating voltage target, V_{OCC} (as seen in 図 18), as long as the auxiliary winding can keep VDD voltage above the UVLO turn-off threshold. When V_O falls so low that VDD cannot be sustained above UVLO, the device shuts down.

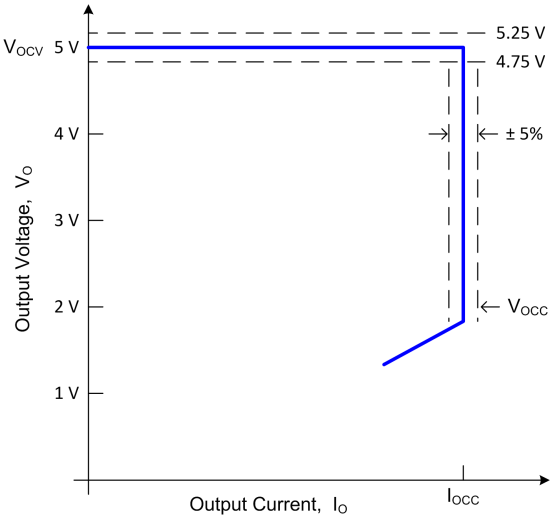


図 18. Typical Output V-I Target Characteristic

Feature Description (continued)

7.3.5 *Wake-Up* Detection and Function

A major feature available at the VS pin is the *wake-up* function which operates in conjunction with a companion secondary-side *wake-up* device, such as the UCC24650. This feature allows light-load and no-load switching frequencies to approach 32 Hz to minimize losses, yet wake the UCC28730-Q1 from its wait state (sleep mode) in the event of a significant load step between power cycles. Despite the low frequencies, excessive output capacitance is not required to maintain reasonable transient response. While in the wait state, the UCC28730-Q1 continually monitors the VS input for a *wake-up* signal, and when detected, responds immediately with several high-frequency power cycles and resumes operation as required by the control law to recover from the load-step transient and restore output voltage regulation.

Because the *wake-up* feature interrupts the wait state between very low frequency switching cycles, it allows the use of a much lower output capacitance value than would be required to hold up the voltage without the *wake-up* function. It also allows the controller to drop to extremely low switching frequencies at no-load conditions to minimize switching losses. This facilitates the achievement of less than 5 mW of input power to meet *zero-power* stand-by requirements. Use of the UCC28730-Q1 controller alone cannot ensure *zero-power* operation since other system-level limitations are also imposed, however, the UCC28730-Q1 and UCC24650 combination goes a long way to reaching this goal.

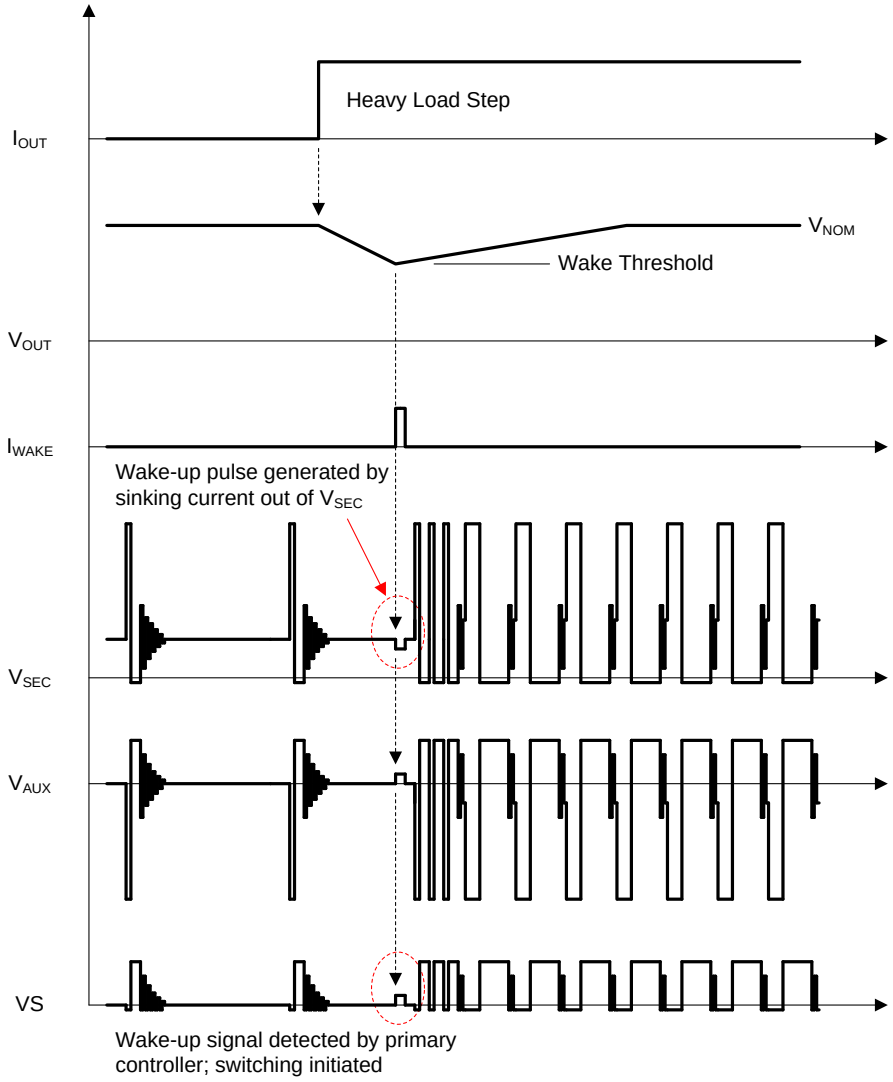


図 19. Simplified *Wake-Up* Operation and Waveforms

Feature Description (continued)

The signals illustrated in 図 19 refer to circuit nodes located on the 概略回路図 diagram on the first page of this datasheet. The *wake-up* signal, which is provided by a secondary-side driver, must meet certain criteria to be considered valid and recognized by the UCC28730-Q1 at the VS input. To distinguish the signal from the residual resonant ringing that follows a switching power cycle, the resonant ringing amplitude must diminish and remain below the *wake-up* signal detection threshold, V_{WU}, for a fixed qualification time, t_{WUDLY}.

The UCC28730-Q1 has two such thresholds; one at $V_{WU(low)}$ and one at $V_{WU(high)}$. The lower $V_{WU(low)}$ threshold is used by converters which incorporate a relatively high-impedance driver for the *wake-up* signal, while the upper $V_{WU(high)}$ threshold may be used in converters with a low-impedance *wake-up* driver. Both thresholds work exactly the same way. The advantage of the upper threshold is that the UCC28730-Q1 is qualified to accept a strong *wake-up* signal without waiting additional time for the resonant ringing to diminish below the lower threshold.

図 20 illustrates the qualification delay period and *wake-up* response to a low-level *wake-up* signal. 図 21 illustrates the qualification delay period and *wake-up* response to a high-level *wake-up* signal.

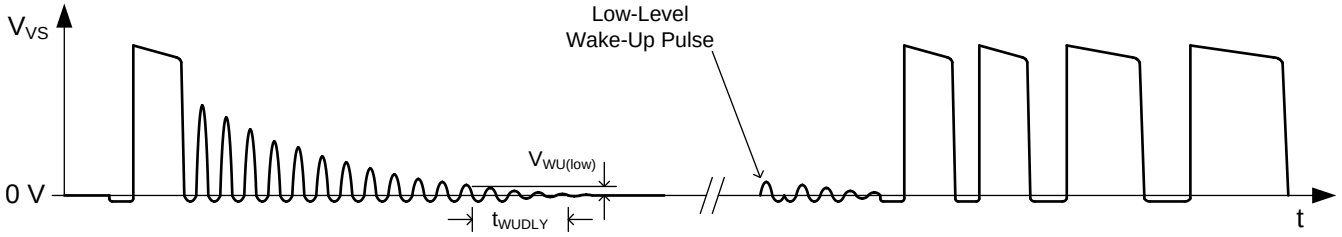


図 20. *Wake-Up* Qualification Criteria and *Wake-Up* Response with Low *Wake-Up* Signal

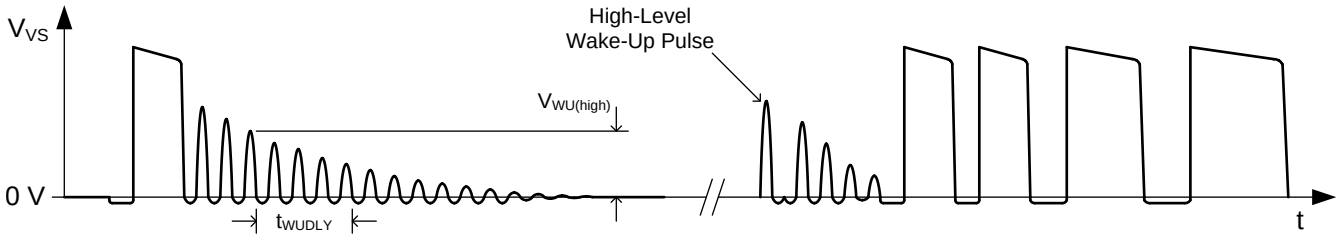


図 21. *Wake-Up* Qualification Criteria and *Wake-Up* Response with High *Wake-Up* Signal

Feature Description (continued)

7.3.6 Valley-Switching and Valley-Skipping

The UCC28730-Q1 utilizes valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turn-on current spike at the current-sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing is diminished to the point where valleys are no longer detectable.

As shown in 図 22, the UCC28730-Q1 operates in a valley-skipping mode (also known as valley-hopping) in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

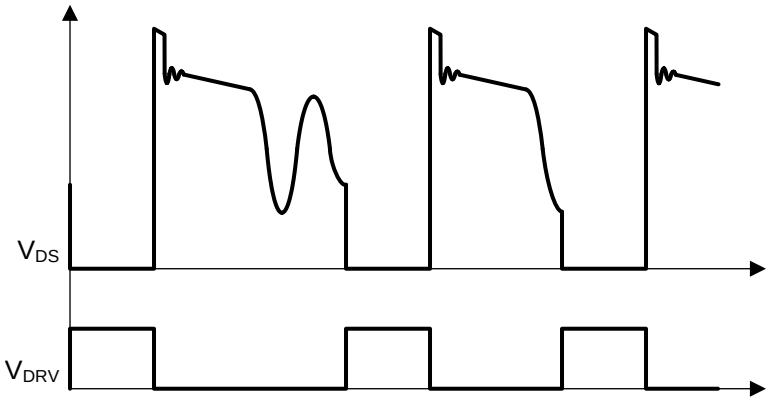


図 22. Valley-Skipping Mode

Valley-skipping modulates each switching cycle into discrete period durations. During FM operation, the switching cycles are periods when energy is delivered to the output in fixed packets, and the power delivered varies inversely with the switching period. During operating conditions when the switching period is relatively short, such as at high-load and low-line, the average power delivered per cycle varies significantly based on the number of valleys skipped between cycles. As a consequence, valley-skipping adds additional low-amplitude ripple voltage to the output with a frequency dependent upon the rate of change of the bulk voltage. For a load with an average power level between that of cycles with fewer valleys skipped and cycles with more valleys skipped, the voltage-control loop modulates the control law voltage and toggles between longer and shorter switching periods to match the required average output power.

7.3.7 Startup Operation

An internal high-voltage startup switch, connected to the bulk capacitor voltage (V_{BULK}) through the HV pin, charges the VDD capacitor. This startup switch functions similarly to a current source providing typically 250 µA to charge the VDD capacitor. When V_{VDD} reaches the 21-V UVLO turn-on threshold, the controller is enabled, the converter starts switching, and the startup switch turns off.

At initial turn-on, the output capacitor is often in a fully-discharged state. The first 4 switching-cycle current peaks are limited to $I_{PP(min)}$ to monitor for any initial input or output faults with limited power delivery. After these 4 cycles, if the sampled voltage at VS is less than 1.32 V, the controller operates in a special startup mode. In this mode, the primary-current-peak amplitude of each switching cycle is limited to approximately 0.67 x $I_{PP(max)}$ and D_{MAGCC} increases from 0.432 to 0.650. These modifications to $I_{PP(max)}$ and D_{MAGCC} during startup allow high-frequency charge-up of the output capacitor to avoid audible noise while the demagnetization voltage is low. Once the sampled VS voltage exceeds 1.36 V, D_{MAGCC} is restored to 0.432 and the primary-current peak resumes as $I_{PP(max)}$. While the output capacitor charges, the converter operates in CC mode to maintain a constant output current until the output voltage enters regulation. Thereafter, the controller responds to conditions as dictated by the control law. The time to reach output regulation consists of the time the VDD capacitor charges to $V_{VDD(on)}$ plus the time the output capacitor charges.

Feature Description (continued)

7.3.8 Fault Protection

The UCC28730-Q1 provides comprehensive fault protection. The protection functions include:

1. Output Overvoltage
2. Input Undervoltage
3. Internal Overtemperature
4. Primary Overcurrent fault
5. CS-pin Fault
6. VS-pin Fault

A UVLO reset and restart sequence applies to all fault-protection events.

The output-overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample of VS exceeds 4.6 V for three consecutive switching cycles, the device stops switching and the internal current consumption becomes I_{FAULT} which discharges the VDD capacitor to the UVLO-turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

Current into the VS pin during the MOSFET on time determines the line-input run and stop voltages. While the VS pin clamps close to GND during the MOSFET on time, the current through R_{S1} is monitored to determine a sample of V_{BULK}. A wide separation of the run and stop thresholds allows clean start-up and shut-down of the power supply with line voltage. The run-current threshold is 225 µA and the Stop-current threshold is 80 µA. The input AC voltage to run at start-up always corresponds to the peak voltage of the rectified line, because there is no loading on C_{BULK} before start-up. The AC input voltage to stop varies with load since the minimum V_{BULK} depends on the loading and the value of C_{BULK}. At maximum load, the stop voltage is close to the run voltage, but at no-load condition the stop voltage can be approximately 1/3 of the run voltage.

The UCC28730-Q1 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.74 to 0.249 V. An additional protection occurs if the CS pin reaches 1.5 V after the leading-edge blanking interval for three consecutive cycles, which results in a UVLO reset and restart sequence.

Normally at initial start-up, the peak level of the primary current of the first four power cycles is limited to the minimum $V_{CST(min)}$. If the CS input is shorted or held low such that the $V_{CST(min)}$ level is not reached within 4 µs on the first cycle, the CS input is presumed to be shorted to GND and the fault protection function results in a UVLO reset and restart sequence. Similarly, if the CS input is open, the internal voltage is pulled up to 1.5 V for three consecutive switching cycles and the fault protection function results in a UVLO reset and restart sequence.

The internal overtemperature-protection threshold is 165°C. If the junction temperature reaches this threshold, the device initiates a UVLO-reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

7.4 Device Functional Modes

According to the input voltage, the VDD voltage, and the output load conditions, the device can operate in different modes:

1. At start-up, when VDD is less than the $V_{VDD(on)}$ turn-on threshold, the HV internal current source is on and charging the VDD capacitor at a ($I_{HV} – I_{START}$) rate.
2. When VDD exceeds $V_{VDD(on)}$, the HV source is turned Off and the device starts switching to deliver power to the converter output. Depending on the load conditions, the converter operates in CC mode or CV mode.
   (a) CC mode means that the converter keeps the output current constant. When the output voltage is below the regulation level, the converter operates in CC mode to restore the output to the regulation voltage.
   (b) CV mode means that the converter keeps the output voltage constant. When the load current is less than the current limit level, the converter operates in CV mode to keep the output voltage at the regulation level over the full load and input line ranges.
3. When operating in CV or CC mode where I_{PP} is greater than 0.55 X $I_{PP(max)}$, the UCC28730-Q1 operates continuously in the run state. In this state, the VDD bias current is always at I_{RUN} plus the average gate-drive current.
4. When operating in CV mode where I_{PP} is less than 0.55 X $I_{PP(max)}$, the UCC28730-Q1 operates in the Wait state between switching cycles and in the run state during a switching cycle. In the Wait state, the VDD bias current is reduced to I_{WAIT} after each switching cycle to improve efficiency at light loads.
5. The device operation can be stopped by the events listed below:
   (a) If VDD drops below the $V_{VDD(off)}$ threshold, the device stops switching, its bias current consumption is lowered to I_{START} and the internal HV current source is turned on until VDD rises above the $V_{VDD(on)}$ threshold. The device then resumes switching.
   (b) If a fault condition is detected, the device stops switching and its bias current consumption is lowered to I_{FAULT}. This current level slowly the discharges VDD to $V_{VDD(off)}$ where the bias current changes from I_{FAULT} to I_{START} and the internal HV current source is turned on until VDD rises above the $V_{VDD(on)}$ threshold.
6. If a fault condition persists, the operation sequence described above in repeats until the fault condition or the input voltage is removed.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28730-Q1 device is a PSR controller optimized for isolated-flyback AC-to-DC single-output supply applications in the 5-W to 25-W range, providing constant-voltage (CV) mode control and constant current (CC) mode control for precise output regulation. Higher-power, multiple-output applications and other variations may also be supported. It is capable of switching at a very low frequency to facilitate achieving stand-by input power consumption of less than 5 mW.

To maintain fast transient response at such low-switching frequencies, the device recognizes a *wake-up* signal at the VS input generated by a companion device, the secondary-side voltage monitor UCC24650.

8.2 Typical Application

A typical application for the UCC28730-Q1 includes the compatible UCC24650 *Wake-Up* Monitor device to regulate an isolated low-voltage DC output with low output capacitance. When the UCC28730-Q1 is operating in the low-frequency Wait state, the UCC24650 alerts the UCC28730-Q1 to a sudden load increase, avoiding the need for extremely high output capacitance to hold up between power cycles. As shown in 図 23, the output rectification uses a ground-referenced diode to facilitate application of the UCC24650. A ground-referenced synchronous rectifier may also be used.

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This figure is simplified to illustrate the basic application of the UCC28730-Q1 and does not show all of the components and networks needed for an actual converter design, nor all of the possible circuit variations.

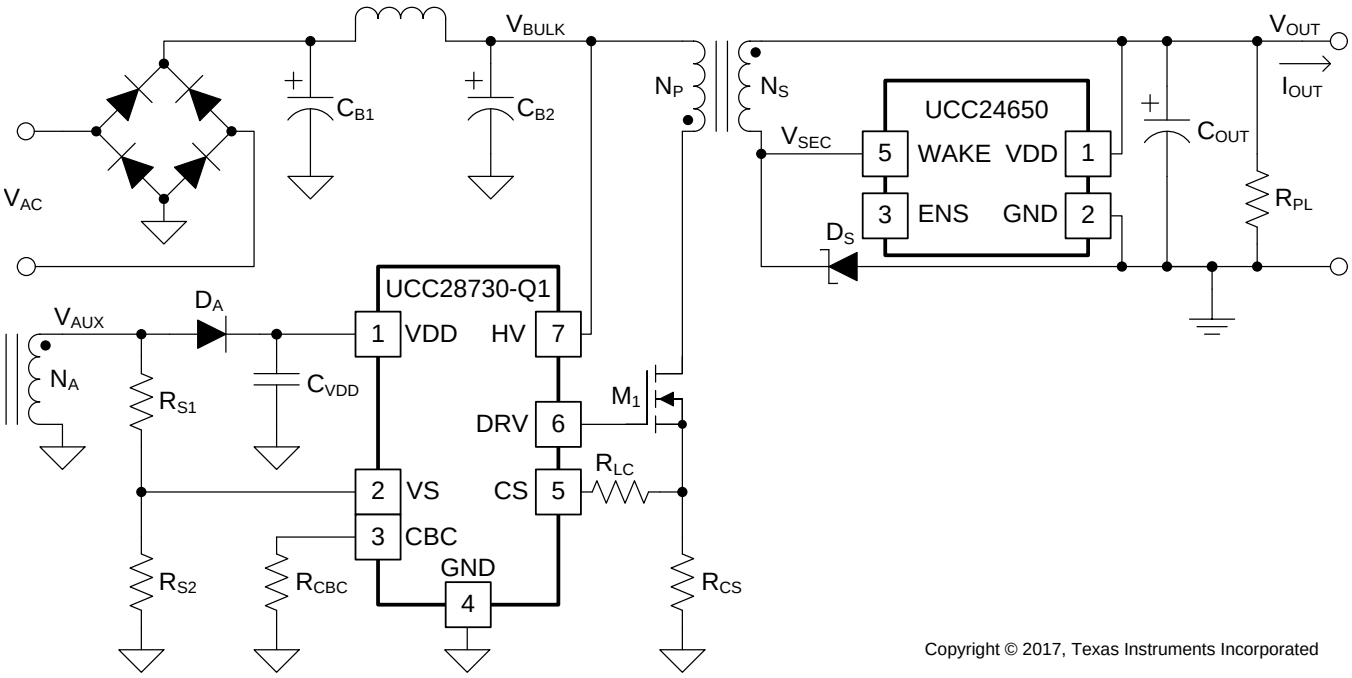

図 23. Simplified Application With Ground-Referenced Diode

Typical Application (continued)

8.2.1 Design Requirements

The following table illustrates a typical subset of high-level design requirements for a particular converter, of which many of the parameter values are used in the various design equations in this section.

表 1. Design Example Performance Requirements

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
V_{IN}	AC-Line Input Voltage		85	115 / 230	264	V_{RMS}
f_{LINE}	Line Frequency		47	50 / 60	63	Hz
V_{OCV}	Output Voltage, CV Mode	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} \le I_{OCC}$	4.75	5.0	5.25	V
I_{OCC}	Output Current, CC Mode	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} = I_{OCC}$	2.0	2.1	2.2	A
V_{RIPPLE}	Output Voltage Ripple	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} \le I_{OCC}$			80	mV_{pp}
	Output Over-Voltage Limit			5.6		V
	Output Over-Current Limit			2.1		A
$V_{IN(run)}$	Start-Up Input Voltage	$I_{OUT} = I_{OCC}$		72		V_{RMS}
V_{OCC}	Minimum Output Voltage, CC Mode	$I_{OUT} = I_{OCC}$			2	V
η_{AVG}	Average Efficiency	Average of 25%, 50%, 75% 100% Load, at V_{IN} = 115 V_{RMS} and 230 V_{RMS}	80%			
η_{10}	Light-Load Efficiency	At 10 % Load, at V_{IN} = 115 V_{RMS} and 230 V_{RMS}	75%			
P_{STBY}	Stand-by Input Power Consumption	At V_{IN} = 115 V_{RMS} and 230 V_{RMS}			4.5	mW

Many other necessary design parameters, such as f_{MAX} and $V_{BULK(min)}$ for example, may not be listed in such a table. These values may be selected based on design experience or other considerations, and may be iterated to obtain optimal results.

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28730-Q1 controller. Refer to 図 23 for component names and network locations. The design procedure equations use terms that are defined below. The primary-side and secondary-side snubbers or clamps are not designed in this procedure.

8.2.2.1 Stand-By Power Estimate

The extra-low operating frequency capability and minimal bias power of the UCC28730-Q1, in conjunction with its companion micro-power *wake-up* device UCC24650, allow for the achievement of less than 5-mW input stand-by power consumption under no-load conditions. This is often referred to as *zero-power* stand-by.

Assuming that no-load stand-by power is a critical design parameter, determine the estimated no-load input power based on the target maximum switching frequency and the maximum output power. The following equation estimates the stand-by power of the converter.

$$P_{STBY} = \frac{V_{OCV} \times I_{OCC} \times f_{MIN}}{\eta_{SB} \times K_{AM}{}^2 \times f_{MAX}} \quad (7)$$

For a typical flyback converter, η_{SB} may range between 0.5 and 0.7, but the lower factor should be used for an initial estimate. Also, f_{MIN} should be estimated at 3x to 4x $f_{SW(min)}$ to allow for possible parameter adjustment.

If the P_{STBY} calculation result is well below 5 mW, there is an excellent chance of achieving *zero-power* stand-by in the actual converter. If the result is near 5 mW, some design adjustment to f_{MAX}, f_{MIN}, and η_{SB} may be needed to achieve *zero-power*. If the result is well above 5 mW, there is little chance to achieve *zero-power* at the target power level unless additional special circuitry and design effort is applied.

8.2.2.2 Input Bulk Capacitance and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. EMI filter design is beyond the scope of this procedure.

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum N_P to N_S turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance value.

Maximum input power is used in the C_{BULK} calculation and is determined by the V_{OCV}, I_{OCC}, and full-load efficiency targets.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \quad (8)$$

The below equation provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target $V_{BULK(min)}$, accounting for hold-up during any loss of AC power for a certain number of half-cycles, N_{HC}, by an AC-line drop-out condition. Alternatively, if a given input capacitance value is prescribed, iterate the $V_{BULK(min)}$ value until that target capacitance is obtained, which determines the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} \geq \frac{2P_{IN} \times \left(0.25 + 0.5\, N_{HC} + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK\,(min)}}{\sqrt{2} \times V_{IN\,(min)}}\right)\right)}{\left(2\, V_{IN\,(min)}^2 - V_{BULK\,(min)}^2\right) \times f_{LINE}} \quad (9)$$

8.2.2.3 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

First, determine the maximum duty cycle of the MOSFET based on the target maximum switching frequency, f_{MAX}, the secondary conduction duty cycle, D_{MAGCC}, and the DCM resonant period, t_R. For t_R, assume 2 µs (500-kHz resonant frequency), if you do not have an estimate from experience or previous designs. For the transition mode operation limit, the time interval from the end of the secondary current conduction to the first resonant valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500 kHz. Actual designs vary. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) \quad (10)$$

D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant current, CC, operation. In the UCC28730-Q1, it is fixed internally at 0.432. Once D_{MAX} is known, the ideal turns ratio of the primary-to-secondary windings can be determined with the equation below. The total voltage on the secondary winding needs to be determined, which is the total of V_{OCV}, the secondary rectifier drop V_F, and cable compensation voltage V_{OCBC}, if used. For 5-V USB charger applications, for example, a turns ratio in the range of 13 to 15 is typically used.

$$N_{PS\,(ideal)} = \frac{D_{MAX} \times V_{BULK\,(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (11)$$

The actual turns ratio depends on the actual number of turns on each of the transformer windings. Choosing $N_{PS} > N_{PS(ideal)}$ results in an output power limit lower than (V_{OCV} x I_{OCC}) when operating at $V_{IN(min)}$, and line-frequency ripple may appear on V_{OUT}. Choosing $N_{PS} < N_{PS(ideal)}$ allows full-power regulation down to $V_{IN(min)}$, but increases conduction losses and the reverse voltage stress on the output rectifier.

Once the actual turns ratio is determined from a detailed transformer design, use this ratio for the following parameter calculations.

The UCC28730-Q1 constant-current regulation is achieved by maintaining a maximum D_{MAGCC} duty cycle of 0.432 at the maximum primary current setting. The transformer turns ratio and constant-current regulating factor determine the current-sense resistor, R_{CS}, for a regulated constant-current target, I_{OCC}. Actual implementation of R_{CS} may consist of multiple parallel resistors to meet power rating and accuracy requirements.

Since not all of the energy stored in the transformer is transferred to the secondary output, a transformer efficiency term, η_{XFMR}, is used to account for the core and winding loss ratio, leakage inductance loss ratio, and primary bias power ratio with respect to the rated output power. At full load, an overall transformer efficiency estimate of 0.91, for example, includes ~3% leakage inductance loss, ~5% core and winding loss, and ~1% bias power. Actual loss ratios may vary from this example.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (12)$$

The primary-transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below.

Initially, determine the transformer peak primary current, $I_{PP(max)}$.

Peak-primary current is simply the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (13)$$

Then, calculate the primary inductance of the transformer, L_P.

$$L_P = \frac{2 \times (V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{I_{PP(max)}^2 \times f_{MAX} \times \eta_{XFMR}} \quad (14)$$

The auxiliary winding to secondary winding turns ratio, N_{AS}, is determined by the lowest target operating output voltage in constant current regulation, the VDD turn-off threshold of the UCC28730-Q1, and the forward diode drops in the respective winding networks.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (15)$$

There is additional energy supplied to VDD from the transformer leakage inductance energy which may allow a lower turns ratio to be used in many designs.

8.2.2.4 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage V_{REV}, these should be reviewed.

The secondary rectifier reverse voltage stress is determined by the equation below. A snubber around the rectifier may be necessary to suppress any voltage spike, due to secondary leakage inductance, which adds to V_{REV}.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (16)$$

For the MOSFET V_{DS} peak stress, an estimated leakage inductance voltage spike, V_{LK}, should to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + (V_{OCV} + V_F + V_{OCBC}) \times N_{PS} + V_{LK} \quad (17)$$

In the high-line, minimum-load condition, the UCC28730-Q1 requires a minimum on-time of the MOSFET ($t_{ON(min)}$) and minimum demagnetization time of the secondary rectifier ($t_{DMAG(min)}$). The selection of f_{MAX}, L_P and R_{CS} affects the actual minimum t_{ON} and t_{DMAG} achieved. The following equations are used to determine if the minimum t_{ON} is greater than t_{CSLEB} and minimum t_{DMAG} target of >1.2 µs is achieved.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (18)$$

$$t_{DMAG(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (19)$$

8.2.2.5 Output Capacitance

With ordinary flyback converters, the output capacitance value is typically determined by the transient response requirement for a specific load step, I_{TRAN}, sometimes from a no-load condition. For example, in some USB charger applications, there is requirement to maintain a transient minimum V_O of 4.1 V with a load-step of 0 mA to 500 mA. 式 20 below assumes that the switching frequency can be at the UCC28730-Q1 minimum of $f_{SW(min)}$.

$$C_{OUT\,(No\_Wake\,)} \geq \frac{I_{TRAN}\left(\frac{1}{f_{SW\,(min\,)}} + 150\ \mu s\right)}{V_{O\Delta}} \tag{20}$$

This results in a C_{OUT} value of over 17,000 µF, unless a substantial pre-load is used to raise the minimum switching frequency. However, the *wake-up* feature allows the use of a much smaller value for C_{OUT} because the *wake-up* response immediately cancels the Wait state and provides high-frequency power cycles to recover the output voltage from the load transient. The secondary-side voltage monitor UCC24650 provides the UCC28730-Q1 with a *wake-up* signal when it detects a -3% droop in output voltage.

$$C_{OUT} \geq \frac{1.2 \times I_{TRAN}}{(dV_{OUT}/dt)}$$

where

- (dV_{OUT}/dt) is the slope at which the UCC24650 must detect the V_{OUT} droop. Use a slope factor of 3700 V/s or lower for this calculation. (21)

The UCC28730-Q1 incorporates internal voltage-loop compensation circuits so that external compensation is not necessary, provided that the value of C_{OUT} is high enough. The following equation determines a minimum value of C_{OUT} necessary to maintain a phase margin of about 40 degrees over the full-load range. K_{Co} is a dimensionless factor which has a value of 100.

$$C_{OUT} \geq K_{Co} \times \frac{I_{OCC}}{V_{OCV} \times f_{MAX}} \tag{22}$$

Another consideration for selecting the output capacitor(s) is the maximum ripple voltage requirement, $V_{RIPPLE(max)}$, which is reviewed based on the maximum output load, the secondary-peak current, and the equivalent series resistance (ESR) of the capacitor. The two major contributors to the output ripple voltage are the change in V_{OUT} due to the charge and discharge of C_{OUT} between each switching cycle and the step in V_{OUT} due to the ESR of C_{OUT}. TI recommends an initial allocation of 33% of $V_{RIPPLE(max)}$ to ESR, 33% to C_{OUT}, and the remaining 33% to account for additional low-level ripple from EMI-dithering, valley-hopping, sampling noise and other random contributors. In 式 23, a margin of 50% is applied to the capacitor ESR requirement to allow for aging. In 式 24, set ΔV_{CQ} = 0.33 x $V_{RIPPLE(max)}$ to determine the minimum value of C_{OUT} with regard to ripple voltage limitation. If other allocations of the allowable ripple voltage are desired, these equations may be adjusted accordingly.

$$ESR \leq \frac{0.33 \times V_{RIPPLE\,(max\,)}}{I_{PP\,(max\,)} \times N_{PS}} \times 0.50 \tag{23}$$

$$C_{OUT} \geq \frac{I_{OCC}}{\Delta V_{CQ} \times f_{MAX}} \tag{24}$$

Choose the largest value of the previous C_{OUT} calculations for the minimum output capacitance. If the value of C_{OUT} becomes excessive to meet a stringent ripple limitation, a C-L-C pi-filter arrangement can be considered to as an alternative to a simple capacitor-only filter. This arrangement is beyond the scope of this datasheet.

8.2.2.6 VDD Capacitance, C_{VDD}

A capacitor is required on VDD to provide:

1. Run-state bias current during start-up while VDD falls toward UVLO, until V_{OCC} is reached,
2. Wait-state bias current between steady-state low-frequency power cycles and
3. Wait-state bias current between minimum-frequency power cycles while V_{OUT} recovers from a transient overshoot.

Generally, the value to satisfy (3) also satisfies (2) and (1), however the value for (1) may be the largest if the converter must provide high output current at a voltage below V_{OCC} during power up.

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation, V_{OCC}. At that point, the auxiliary winding can sustain the bias voltage to the UCC28730-Q1 above the UVLO shutdown threshold. The total current available to charge the output capacitors and supply an output load and is the constant-current regulation target, I_{OCC}.

式 25 assumes that all of the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. For margin, there is an estimated 1 mA of average gate-drive current added to the run current and 1 V added to the minimum VDD.

$$C_{VDD} \geq \frac{(I_{RUN} + 1\ mA) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{VDD\,(on)} - (V_{VDD\,(off)} + 1\ V)} \tag{25}$$

At light loads, the UCC28730-Q1 enters a Wait-state between power cycles to minimize bias power and improve efficiency. 式 26 estimates the minimum capacitance needed to obtain a target maximum ripple voltage on VDD ($V_{VDD(max\Delta)}$ < 1 V, for example) during the Wait state, which occurs at the lowest possible switching frequency.

$$C_{VDD} \geq \frac{I_{WAIT}}{V_{VDD\,(max\,\Delta)} \times f_{SW\,(min)}} \tag{26}$$

Choose the largest value of the previous C_{VDD} calculations for the minimum VDD capacitance.

8.2.2.7 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter. Also, the high-side divider resistor, R_{S1}, determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer primary to auxiliary turns ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \tag{27}$$

The low-side VS divider resistor, R_{S2}, is selected based on the desired constant-voltage output regulation target, V_{OCV}.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \tag{28}$$

The UCC28730-Q1 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor value, R_{LC}, is determined by various system parameters and the combined gate-drive turn-off and MOSFET turn-off delays, t_D. Assume a 50-ns internal propagation delay in the UCC28730-Q1.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times N_{PA} \times t_D}{L_P} \tag{29}$$

The UCC28730-Q1 provides adjustable cable compensation of up to approximately +8% of V_{OCV} by connecting a resistor between the CBC terminal and GND. This compensation voltage, V_{OCBC}, represents the incremental increase in voltage, above the nominal no-load output voltage, needed to cancel or reduce the incremental decrease in voltage at the end of a cable due to its resistance. The programming resistance required for the desired cable compensation level at the converter output terminals can be determined using the equation below. As the load current changes, the cable compensation voltage also changes slowly to avoid disrupting control of the main output voltage. A sudden change in load current will induce a step change of output voltage at the end of the cable until the compensation voltage adjusts to the required level. Note that the cable compensation does not change the overvoltage protection (OVP) threshold,V_{OVP} (see Electrical Characteristics), so the operating margin to OVP is less when cable compensation is used. If cable compensation is not required, CBC may remain unconnected.

$$R_{CBC} = \frac{V_{CBC(max)}}{V_{OCBC} \times \frac{V_{VSR}}{(V_{OCV} + V_F)}} \times 3\ k\Omega - 28\ k\Omega \tag{30}$$

8.2.2.8 VS Wake-Up Detection

The amplitude of the *wake-up* signal at the VS input must be high enough to be detected. This signal, which originates on the secondary winding, is limited by the impedances of the *wake-up* signal driver and the L-C resonant tank of the transformer windings. The signal is further attenuated by the VS divider resistors. To maximize the *wake-up* signal amplitude, the pulse width, t_{WAKE}, of the *wake-up* signal should be at least 1/4-wavelength of the switched-node resonant frequency, f_{RES}. The resonant frequency depends on the primary magnetizing inductance and the total equivalent capacitance at the switching node, that is, the primary-side MOSFET drain node. The switched-node capacitance, C_{SWN}, includes the MOSFET C_{OSS}, the transformer winding capacitance, and all other stray circuit capacitance attached to the MOSFET drain. Use 式 31 to determine f_{RES}. Conversely, if f_{RES} is known by experience or measurement, C_{SWN} can be derived from 式 31.

$$f_{RES} = \frac{1}{2\pi\sqrt{L_P \times C_{SWN}}} \tag{31}$$

Since the *wake-up* pulse width is typically fixed by the driver device, such as the UCC24650, maximum signal strength is obtained when 式 32 is true. Since L_P is generally fixed by other system requirements, only C_{SWN} can be reduced to increase f_{RES}, if necessary.

$$f_{RES} \geq \frac{1}{4 \times t_{WAKE}} \tag{32}$$

式 33 is used to ensure that there is sufficient amplitude at the VS input to reliably trigger the *wake-up* function, where R_{WAKE_TOT} is the total secondary-side resistance of the wake-up signal driver and any series resistance. An over-drive of 15 mV is added to the *wake-up* threshold level for margin.

$$\sqrt{\frac{L_P}{C_{SWN}}} \geq \frac{R_{WAKE\_TOT} \times N_{PS}^2}{\left[\frac{V_{OUT} \times N_{AS}}{\left(V_{WU\,(low)} + 15mV\right) \times \left(\frac{R_{S1}}{R_{S2}} + 1\right)} - 1\right]} \tag{33}$$

8.2.3 Application Curves

The following figures indicate the transient response of a 5-V, 10-W flyback converter which receives a pulsed step-load of 2 A while operating in the no-load stand-by condition. 図 27 indicates the no-load stand-by input power consumption achieved by this converter over the full AC input range. *Zero-Power* operation is achieved while retaining fast transient response to a full load step.

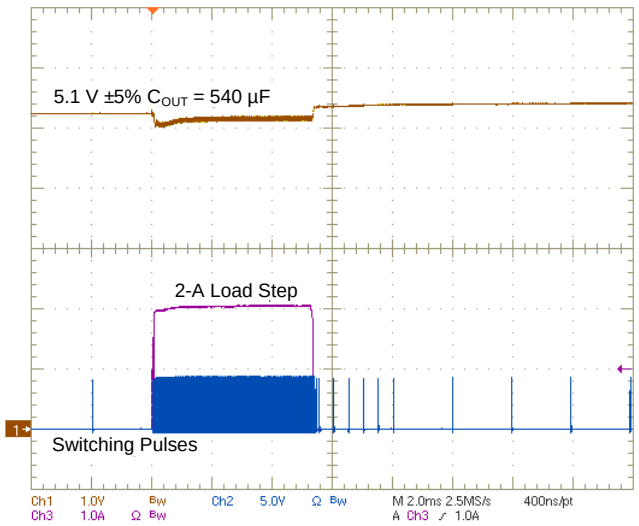

図 24. 2-A Load Step During Stand-by Operation

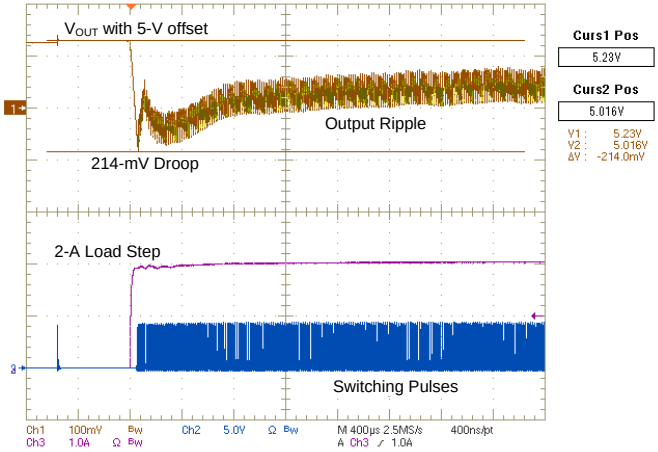

図 25. Transient Response Detail for 2-A Load Step

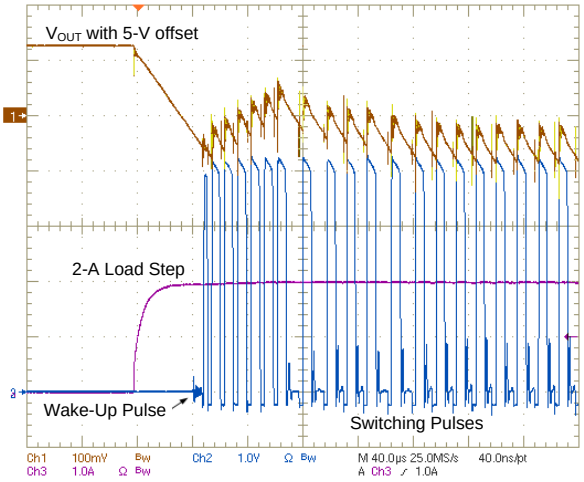

図 26. *Wake-Up* Pulse Triggering Response from UCC28730-Q1 Primary-Side Controller

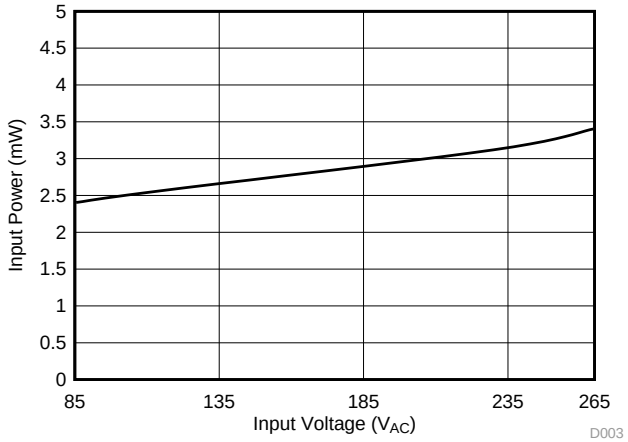

図 27. No-Load Input Power Consumption for a 5-V, 10-W Converter

8.3 Do's and Don'ts

- During no-load operation, do allow sufficient margin for variations in VDD level to avoid the UVLO shutdown threshold. Also, at no-load, keep the average switching frequency, $<f_{SW}>$, greater than 2 x $f_{SW(min)}$ to avoid a rise in output voltage.
- Do clean flux residue and contaminants from the PCB after assembly. Uncontrolled leakage current from VS to GND causes the output voltage to increase, while leakage current from HV or VDD to VS causes output voltage to decrease.
- If ceramic capacitors are used for VDD, do use quality parts with X7R or X5R dielectric rated 50 V or higher to minimize reduction of capacitance due to dc-bias voltage and temperature variation.
- Do not use leaky components if less than 5-mW stand-by input power consumption is a design requirement.
- Do not probe the VS node with an ordinary oscilloscope probe; the probe capacitance can alter the signal and disrupt regulation. Do observe VS indirectly by probing the auxiliary winding voltage at R_{S1} and scaling the waveform by the VS divider ratio.

9 Power Supply Recommendations

The UCC28730-Q1 is intended for AC-to-DC adapters and chargers with input voltage range of 85 $V_{AC(rms)}$ to 265 $V_{AC(rms)}$ using flyback topology. It can also be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

The DRV output normally begins PWM pulses approximately 55 µs after VDD exceeds the turn-on threshold $V_{VDD(on)}$. Avoid excessive dv/dt on VDD. Positive dv/dt greater than 1 V/µs may delay the start of PWM . Negative dv/dt greater than 1 V/µs on VDD which does not fall below the UVLO turn-off threshold $V_{VDD(off)}$ may result in a temporary dip in the output voltage.

10 Layout

10.1 Layout Guidelines

In order to increase the reliability and feasibility of the project it is recommended to adhere to the following guidelines for PCB layout.

1. Minimize stray capacitance on the VS node. Place the voltage sense resistors (R_{S1} and R_{S2} in 図 24 through 図 27) close to the VS pin.
2. TI recommends to connect the HV input to a non-switching source of high voltage, not to the MOSFET drain, to avoid injecting high-frequency capacitive current pulses into the device.
3. Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop, the MOSFET gate-drive loop, the primary snubber loop, the auxiliary winding loop and the secondary output current loop.

10.2 Layout Example

The partial layout example of 図 28 demonstrates an effective component and track arrangement for low-noise operation on a single-layer printed circuit board. Actual board layout must conform to the constraints on a specific design, so many variations are possible.

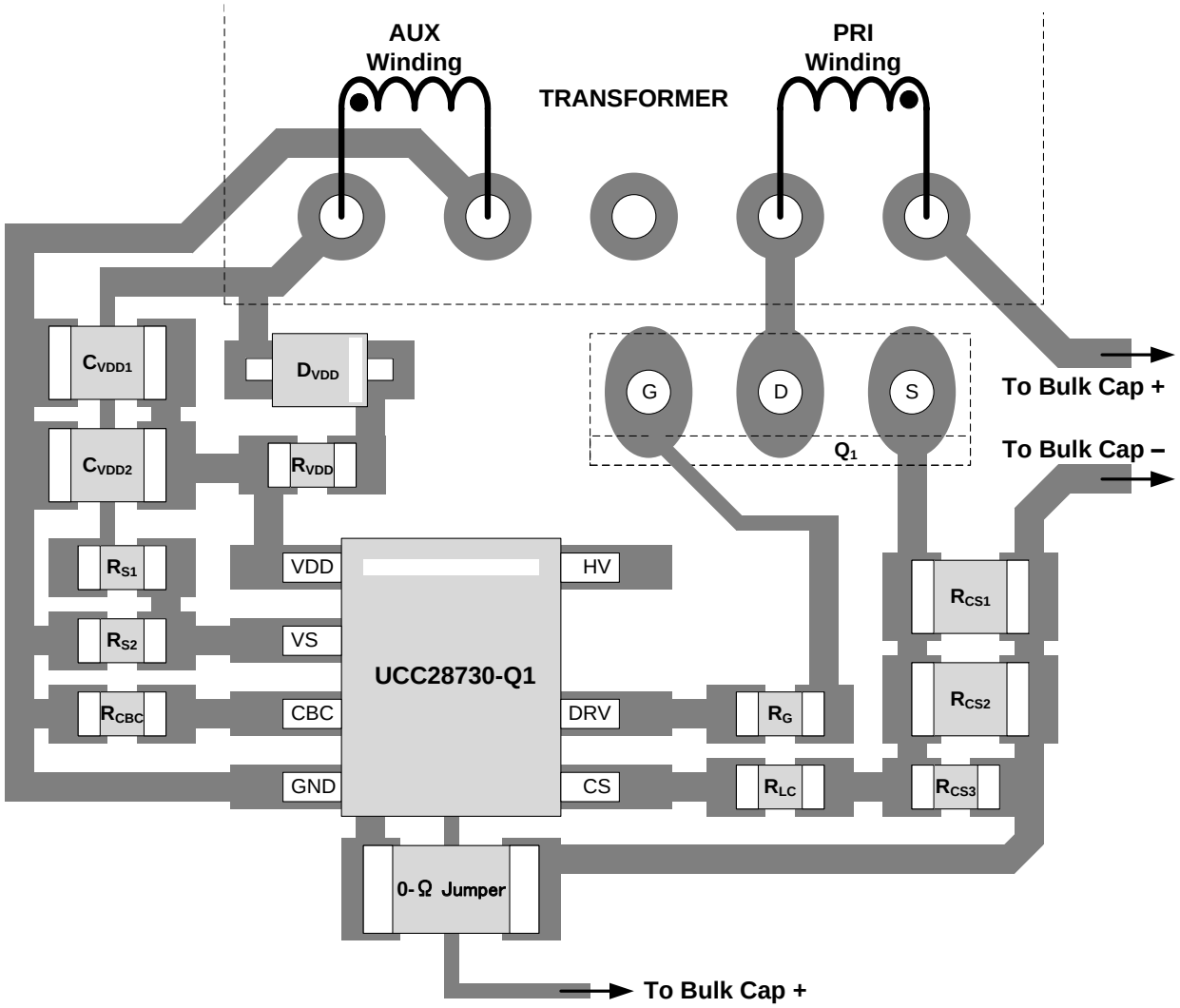

図 28. UCC28730-Q1 Partial Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの項目表記

11.1.1.1 容量項(ファラッド単位)

- C_{BULK}: C_{B1}とC_{B2}の合計入力容量
- C_{VDD}: VDDピンに必要な最小容量
- C_{OUT}: 必要な最小出力容量

11.1.1.2 デューティ・サイクル項

- D_{MAGCC}: CCモード中の2次側ダイオード導通デューティ・サイクル定数 = 0.432
- D_{MAX}: 許容される最大のMOSFETオン時間デューティ・サイクル
- N_{HC}: ライン・ドロップアウト中のACライン周波数の半サイクル数

11.1.1.3 周波数項(ヘルツ単位)

- f_{LINE}: 最小ライン周波数
- f_{MAX}: コンバータの目標全負荷最大スイッチング周波数
- f_{MIN}: コンバータの実際の最小スイッチング周波数
- $f_{SW(max)}$: コントローラの最大スイッチング周波数能力(「Electrical Characteristics」を参照)
- $f_{SW(min)}$: コントローラの最小スイッチング周波数能力(「Electrical Characteristics」を参照)

11.1.1.4 電流項(アンペア単位)

- I_{OCC}: コンバータの出力定電流目標
- $I_{PP(max)}$: トランスの最大1次側ピーク電流
- I_{START}: スタートアップ前のVDDバイアス電流(「Electrical Characteristics」を参照)
- I_{TRAN}: 必要な正の負荷ステップ電流
- I_{WAIT}: ウェイト状態時のVDDバイアス電流(「Electrical Characteristics」を参照)
- $I_{VSL(run)}$: VSピンの動作電流(「Electrical Characteristics」を参照)

11.1.1.5 電流および電圧のスケーリング項

- K_{AM}: 1次側電流ピーク振幅の最大値と最小値の比(「Electrical Characteristics」を参照)
- K_{LC}: ライン補償の電流スケーリング定数(「Electrical Characteristics」を参照)
- K_{Co}: C_{OUT}の計算に使用する安定性係数 = 100

11.1.1.6 トランスの項

- L_P: トランスの1次側インダクタンス
- N_{AS}: トランスの補助/2次巻線比
- N_{PA}: トランスの1次/補助巻線比
- N_{PS}: トランスの1次/2次巻線比

11.1.1.7 電力項(ワット単位)

- P_{IN}: 全負荷時のコンバータの最大入力電力
- P_{OUT}: 全負荷時のコンバータの出力電力
- P_{STBY}: 待機状態でのコンバータの合計入力電力

デバイス・サポート (continued)

11.1.1.8 抵抗項(オーム単位)

- R_{CS}: 1次電流プログラミング抵抗
- R_{ESR}: 出力コンデンサの合計ESR
- R_{PL}: コンバータの出力のプリロード抵抗
- R_{S1}: VS入力のハイサイド抵抗
- R_{S2}: VS入力のローサイド抵抗

11.1.1.9 タイミング項(秒単位)

- t_D: MOSFETのターンオフ遅延を含む合計電流センス遅延時間、MOSFET遅延に50nsを加算
- $t_{DMAG(min)}$: 2次側整流器の最小導通時間(トランスの消磁時間)
- $t_{ON(min)}$: 最小MOSFETオン時間
- t_R: t_{DMAG}後の共振リンギング期間

11.1.1.10 DC電圧項(ボルト単位)

- V_{BULK}: 待機電力測定用の最大バルク・コンデンサ電圧
- $V_{BULK(min)}$: フルパワー時のバルク・コンデンサ上の最小バレー電圧
- V_{OCBC}: 出力端子の目標ケーブル補償電圧
- $V_{CBC(max)}$: 最大出力電流時のCBCピン上の最大電圧(「Electrical Characteristics」を参照)
- V_{CCR}: 定電流レギュレート係数電圧(「Electrical Characteristics」を参照)
- $V_{CST(max)}$: CSピンの最大電流センシング・スレッショルド(「Electrical Characteristics」を参照)
- $V_{CST(min)}$: CSピンの最小電流センシング・スレッショルド(「Electrical Characteristics」を参照)
- $V_{VDD(off)}$: UVLO電源オフ・スレッショルド電圧(「Electrical Characteristics」を参照)
- $V_{VDD(on)}$: UVLO電源オン・スレッショルド電圧(「Electrical Characteristics」を参照)
- $V_{VDD(max\Delta)}$: ウェイト状態中のスイッチング・サイクル間でのVDD電圧の最大降下
- $V_{O\Delta}$: 出力の負荷過渡中に許容される出力電圧降下
- V_{DSPK}: 高ラインでのピークMOSFETドレイン-ソース電圧
- V_F: ゼロに近い電流での2次側整流器の順方向電圧降下
- V_{FA}: 補助整流器の順方向電圧降下
- V_{LK}: 1次側リーク・インダクタンス・エネルギーの推定リセット電圧
- V_{OCV}: コンバータのレギュレーション出力電圧
- V_{OCC}: 定電流レギュレーション時の目標最低出力電圧
- V_{REV}: 2次側整流器でのピーク逆方向電圧
- V_{RIPPLE}: 全負荷時の出力ピーク・ツー・ピーク・リップル電圧
- V_{VSR}: VS入力での定電圧レギュレーション・レベル(「Electrical Characteristics」を参照)
- ΔV_{CQ}: スイッチング・サイクル間の負荷放電によってC_{OUT}電圧に許容される変化

11.1.1.11 AC電圧項(ボルト単位)

- $V_{IN(max)}$: コンバータへの最大AC入力電圧
- $V_{IN(min)}$: コンバータへの最小AC入力電圧
- $V_{IN(run)}$: コンバータのスタートアップ(動作)入力電圧

11.1.1.12 効率項

- η_{SB}: フライバック・コンバータの、出力電力が0であるときの推定内部プリロード電力効率。この効率は、R_{PL}で消費されるコンバータの内部プリロード電力を、待機状態のコンバータの合計入力電力P_{STBY}で除算して計算されます。設計の開始時には推定値として50%を使用できます。
- η: 最大定格出力電力でのコンバータの全体効率
- η_{XFMR}: トランスの電力伝送効率

11.2 ドキュメントのサポート

11.2.1 関連資料

- 『UCC24650 高速過渡PSR用の200Vウェイクアップ・モニタ』、SLUSBL6
- 『UCC28730 ゼロパワー・スタンバイ、PSRフライバック・コントローラ、CVCCおよびウェイクアップ監視付き』、SLUSBL5
- UCC28730EVM-552 EVMユーザー・ガイド『*UCC28730EVM-552の使用法*』、SLUUB75

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.5 商標

E2E is a trademark of Texas Instruments.

11.6 静電気放電に関する注意事項

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28730QDRQ1	Active	Production	SOIC (D) | 7	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28730Q
UCC28730QDRQ1.B	Active	Production	SOIC (D) | 7	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

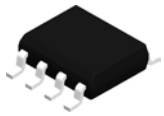
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC28730-Q1 :

- Catalog : UCC28730

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

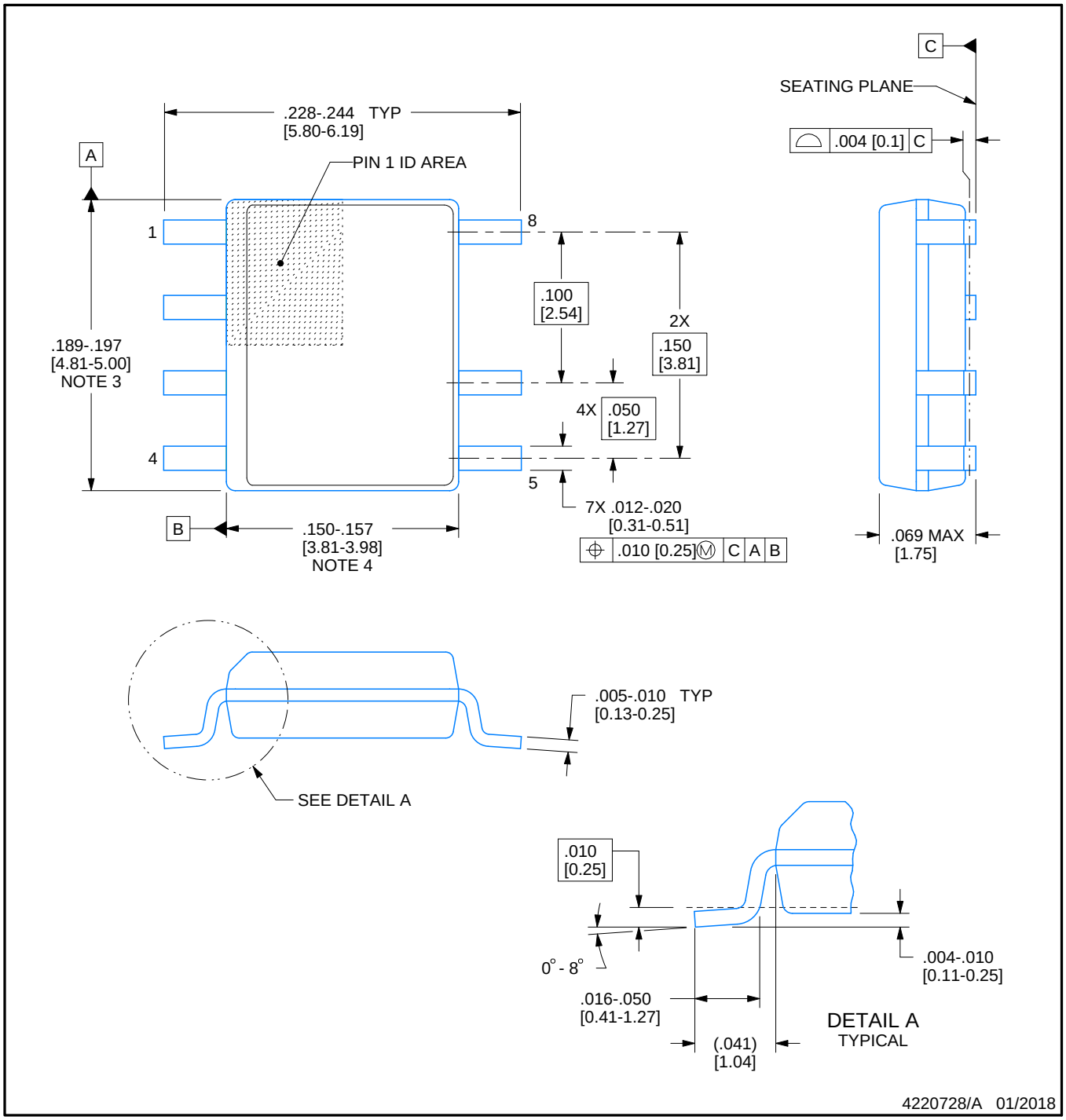


PACKAGE OUTLINE

D0007A

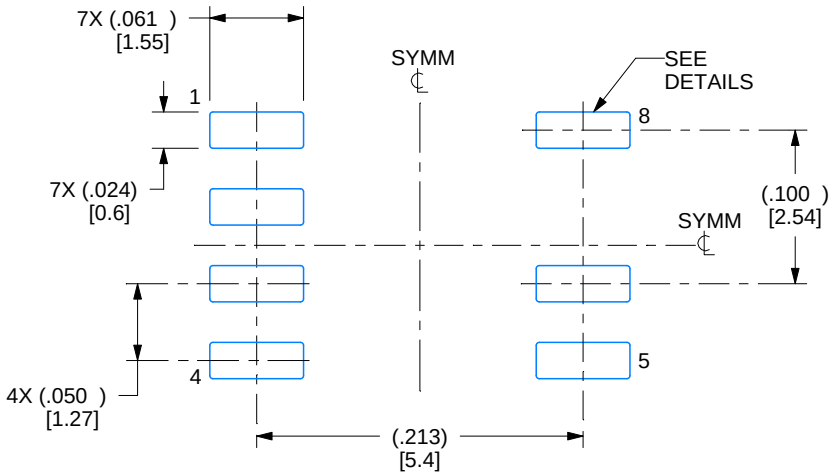
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

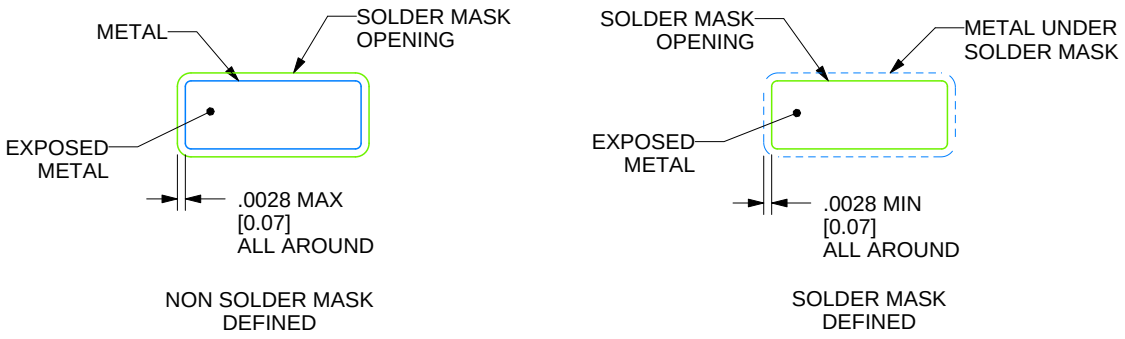


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

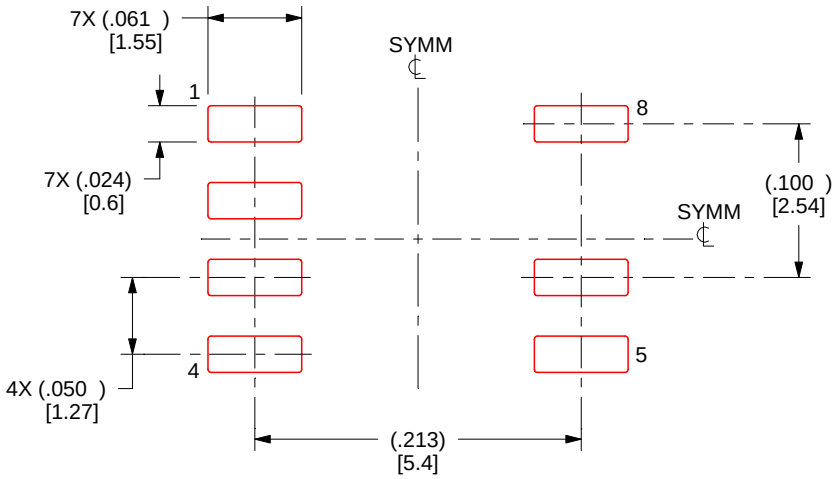
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月