UCC27532-Q1 2.5A および 5A、35V$_{MAX}$ VDD、FET および IGBT シングル ゲート ドライバ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1
- 低コストのゲートドライバ (FET と IGBT の駆動に最適なソリューションを提供)
- ディスクリートトランジスタ ペアによる駆動の代替として最適 (コントローラとのインターフェイスが容易)
- CMOS 互換の入力ロジック スレッショルド (VDD が 18V を超えた場合は固定)
- 分割出力により、ターンオンとターンオフを個別に調整可能
- TTL 互換の固定スレッショルドによるイネーブル
- 高いピーク駆動電流:ソース 2.5A、シンク 5A (VDD 18V 時)
- 広い VDD 範囲:10V～35V
- グランドより低い電圧 (DC -5V) にも耐える入力ピン
- 入力がフローティング時または VDD UVLO 時は出力を Low に保持
- 高速伝搬遅延時間:17ns (標準値)
- 高速な立ち上がり / 立ち下がり時間:
  15ns/7ns (標準値、1800pF 負荷)
- 低電圧誤動作防止 (UVLO)
- ハイサイドまたはローサイドドライバとして使用可能 (適切にバイアスを印加し信号を分離して設計した場合)
- 低コストで省スペースの 6 ピン DBV (SOT-23) パッケージ
- 動作温度範囲:–40℃～140℃

2 アプリケーション

- 車載用
- スイッチ モード電源
- DC/DC コンバータ
- ソーラー インバータ、モーター制御、UPS
- HEV および EV 用充電器
- 家電製品
- 再生可能エネルギーの電力変換
- SiC FET コンバータ

3 概要

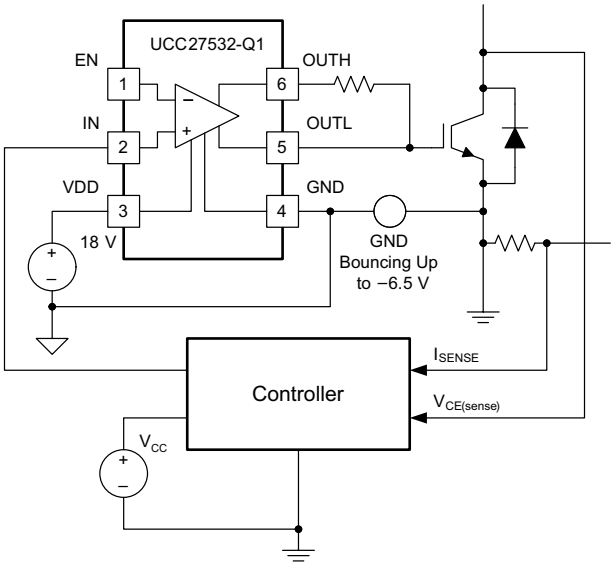
UCC27532-Q1 デバイスは、最大 2.5A のソース電流と最大 5A のシンク電流 (非対称駆動) で MOSFET および IGBT パワー スイッチを効率的に駆動できるシングル チャネル高速ゲートドライバです。非対称駆動の強力なシンク能力により、寄生素子によるミラー ターンオン効果に対する耐性を高めています。また、UCC27532-Q1 デバイスは分割出力構成を実装し、ゲート駆動電流は OUTH ピンからソース、OUTL ピンからシンクされます。このピン配置により、ユーザーは OUTH および OUTL ピンに対してそれぞれ独立したオン / オフ抵抗を使用でき、スイッチングのスルーレートを簡単に制御できます。

また、レール ツー レールの駆動能力と、17ns (標準値) の非常に小さな伝搬遅延を特長としています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
UCC27532-Q1	DBV (SOT-23、6)	2.90mm × 1.60mm

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



負バイアスを使用しない IGBT 駆動

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4 概要 (続き)

UCC27532-Q1 デバイスは、18V 以下の VDD において、VDD 電圧の 55% (立ち上がり時) と VDD 電圧の 45% (立ち下がり時) に設定された CMOS 入力スレッショルドを持っています。VDD が 18V より高い場合、入力スレッショルドはその最大レベルに固定されたままになります。

このドライバには、TTL 互換の固定スレッショルドを持つ EN ピンが搭載されています。EN は内部でプルアップされているため、EN を Low にするとドライバがディスエーブルになり、オープンにすると通常動作が可能になります。EN ピンは、IN ピンと同じ性能を持つ追加の入力としても使用できます。

ドライバの入力ピンをオープンにすると、出力が Low に保持されます。本ドライバの論理動作を「タイミング図」、「入力 / 出力ロジックの真理値表」、セクション 8.2 に示します。

VDD ピンの内部回路は、VDD 電源電圧が動作範囲内になるまで出力を Low に保持する低電圧誤動作防止機能を備えています。

UCC27532-Q1 ドライバは、6 ピンの標準 SOT-23（DBV）パッケージで供給されます。このデバイスは、広い温度範囲 (-40℃～140℃) で動作します。

5 Pin Configuration and Functions

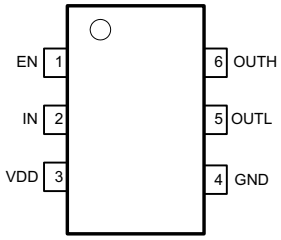


図 5-1. DBV Package 6-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable (Pull EN to GND to disable output, pull it high or leave it open to enable the output)
GND	4	—	Ground (all signals are referenced to this node)
IN	2	I	Driver noninverting input (CMOS threshold)
OUTL	5	O	5-A sink current output of driver
OUTH	6	O	2.5-A source current output of driver
VDD	3	I	Bias supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			MIN	MAX	UNIT
Supply voltage range	VDD		–0.3	35	V
	Continuous	OUTH, OUTL	–0.3	VDD +0.3	
		IN, EN	–2	VDD +0.3	
	Pulse	OUTH, OUTL (200 ns)	–5	27	V
		IN, EN (1.5 µs)	–6.5	27	
Operating virtual junction temperature range, T_J			–40	150	°C
Lead temperature	Soldering, 10 seconds			300	
	Reflow			260	
Storage temperature range, T_{stg}			–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the data sheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	–40		140	°C
Input voltage, IN	–5		25	V
Enable, EN	–5		25	

6.4 Thermal Information

THERMAL METRIC(1)		UCC27532-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = –40°C to 140°C, IN switching from 0 V to VDD, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into and negative out of the specified terminal. OUTH and OUTL are tied together. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{DDoff}	Startup current, VDD = 7	IN, EN = VDD	100	240	350	µA
		IN, EN = GND	100	250	350	
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{ON}	Supply start threshold		8	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	V
V_{DD_H}	Supply voltage hysteresis			0.7		V
INPUT (IN)						
V_{IN_H}	Input signal high threshold	VDD = 16V, Output high	8.8	9.4	10	V
V_{IN_L}	Input signal low threshold	VDD = 16V, Output low	6.7	7.3	7.9	V
V_{IN_HYS}	Input signal hysteresis	VDD = 16V		2.1		V
ENABLE (EN)						
V_{EN_H}	Enable signal high threshold	VDD = 16V, Output high	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	VDD = 16V, Output low	0.8	1	1.2	V
V_{EN_HYS}	Enable signal hysteresis	VDD = 16V		0.9		V
OUTPUTS (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(1)	C_{LOAD} = 0.22 µF, f = 1 kHz		–2.5 / 5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = –10 mA	VDD –0.2	VDD –0.12	VDD –0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	V
R_{OH}	OUTH, pullup resistance(1)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = –40°C to 140°C, I_{OUT} = -10 mA	7	12	20	
R_{OL}	OUTL, pulldown resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	Ω
		T_A = –40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	

(1) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure. The effective dynamic pullup resistance is 3 × R_{OL}.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		ns
t_{D1}	Turnon propagation delay	C_{LOAD} = 1.8 nF, IN = 0 V to VDD		17	26	ns
t_{D2}	Turnoff propagation delay	C_{LOAD} = 1.8 nF, IN = VDD to 0 V		17	26	ns

(1) Ensured by design and tested during characterization. Not production tested.
(2) See 図 6-1.

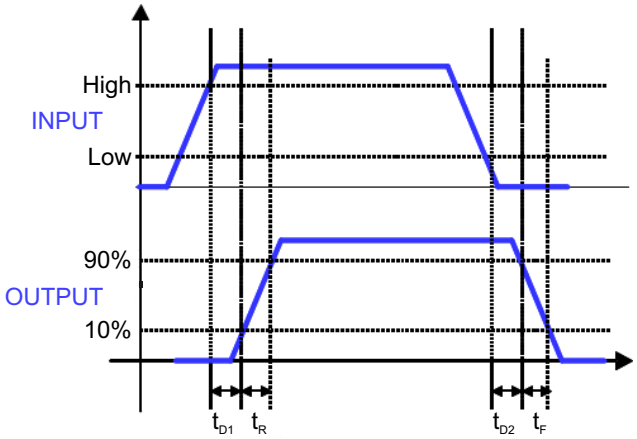


図 6-1. Timing Diagram: (OUTH Tied To OUTL) Input = IN, Output = OUT (EN = VDD) Or Input = EN, Output = OUT (IN = VDD)

6.7 Typical Characteristics

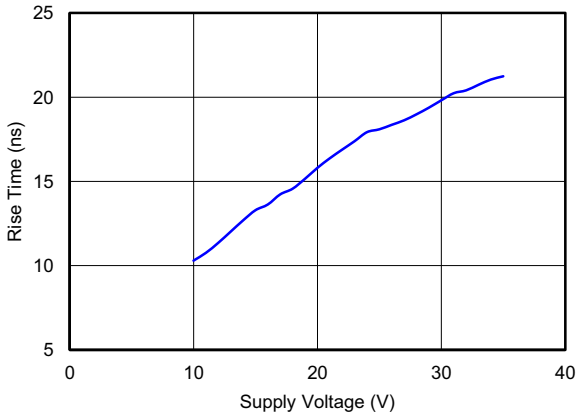


図 6-2. Rise Time vs Supply Voltage

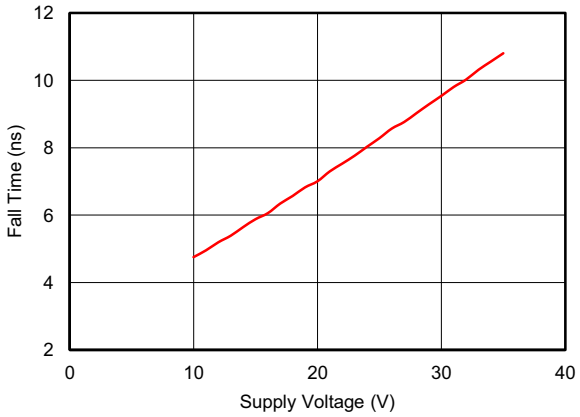


図 6-3. Fall Time vs Supply Voltage

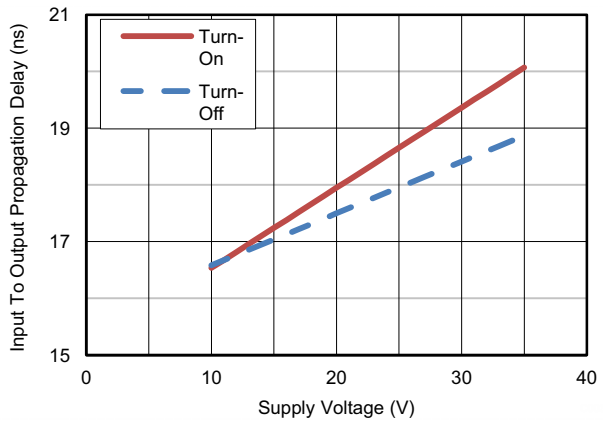


図 6-4. Propagation Delay vs Supply Voltage

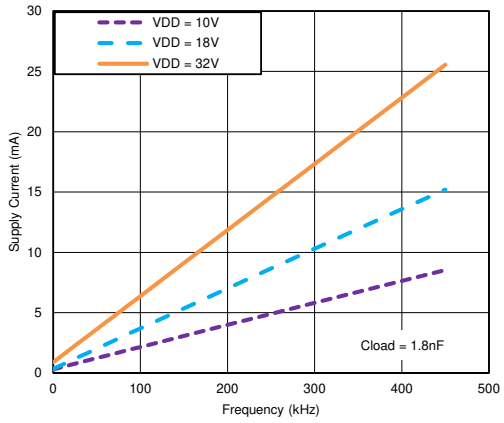


図 6-5. Operating Supply Current vs Frequency

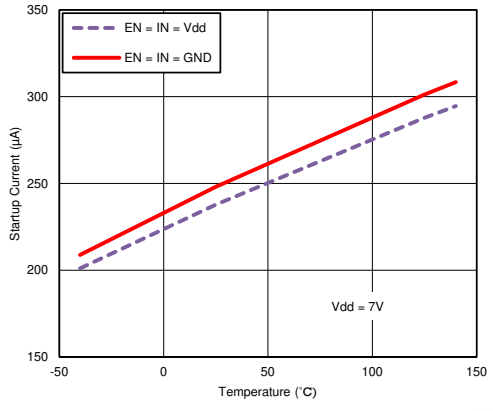


図 6-6. Start-Up Current vs Temperature

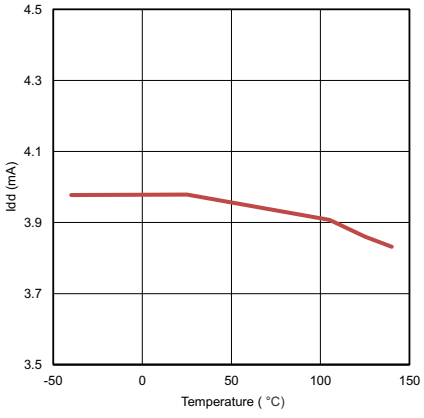


図 6-7. Operating Supply Current vs Temperature (Output Switching)

6.7 Typical Characteristics (continued)

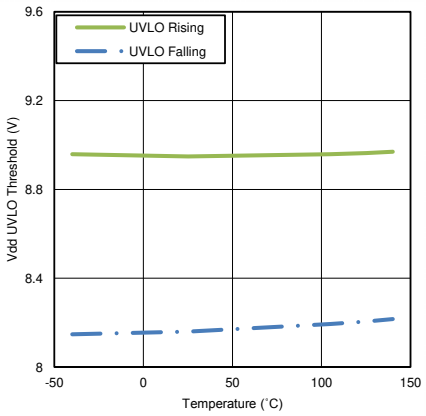


図 6-8. UVLO Threshold Voltage vs Temperature

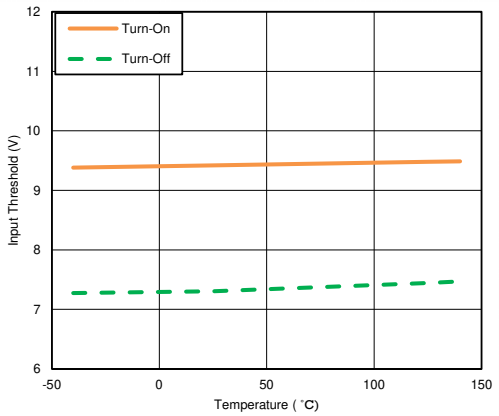


図 6-9. Input Threshold vs Temperature

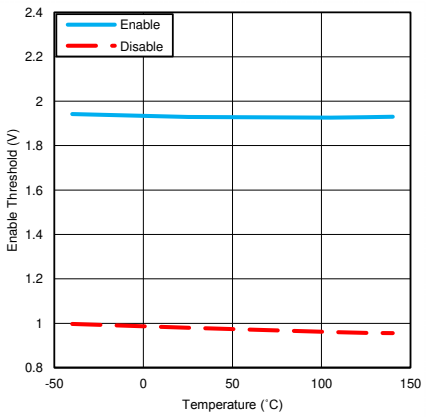


図 6-10. Enable Threshold vs Temperature

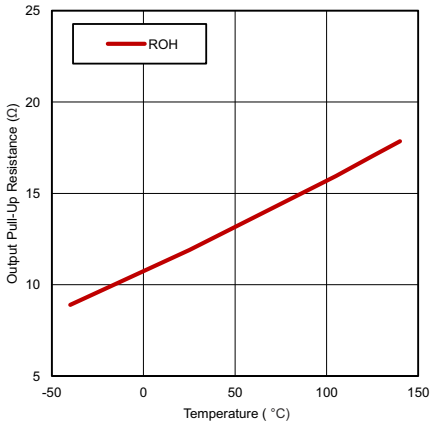


図 6-11. Output Pullup Resistance vs Temperature

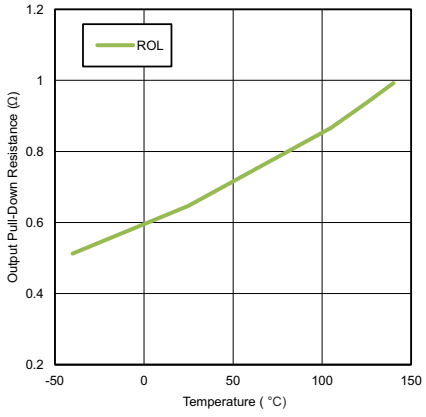


図 6-12. Output Pulldown Resistance vs Temperature

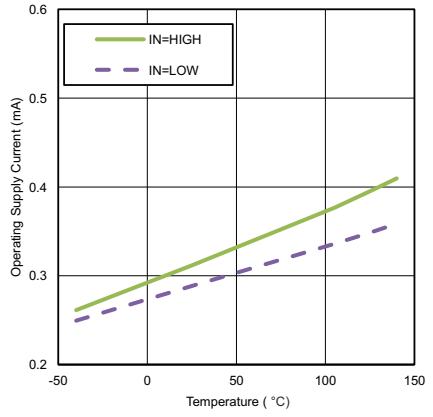


図 6-13. Operating Supply Current vs Temperature (Output In DC ON and OFF Condition)

6.7 Typical Characteristics (continued)

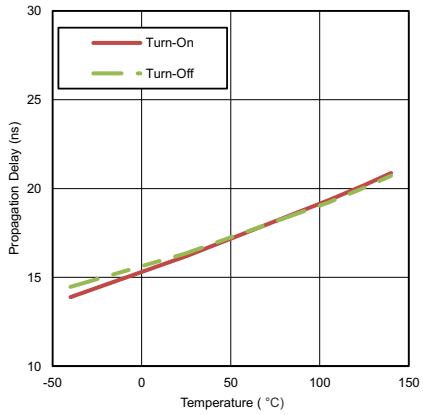


図 6-14. Input-to-Output Propagation Delay vs Temperature

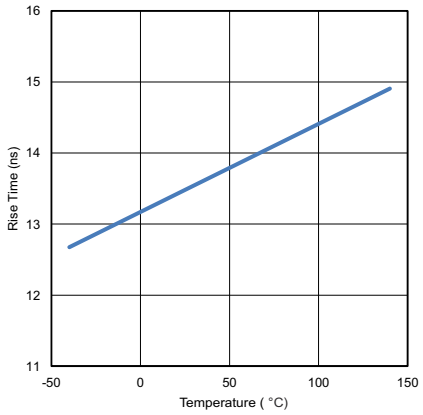


図 6-15. Rise Time vs Temperature

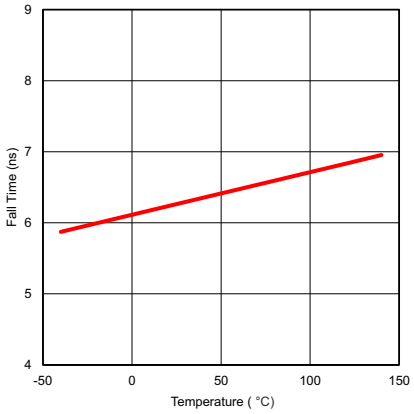


図 6-16. Fall Time vs Temperature

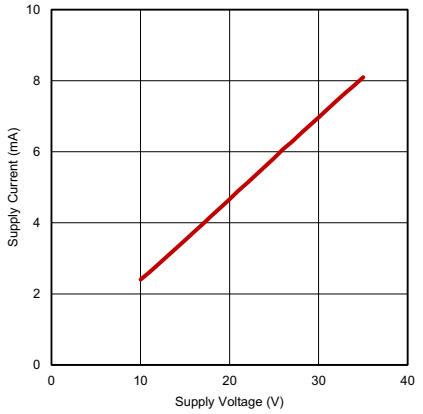


図 6-17. Operating Supply Current vs Supply Voltage (Output Switching)

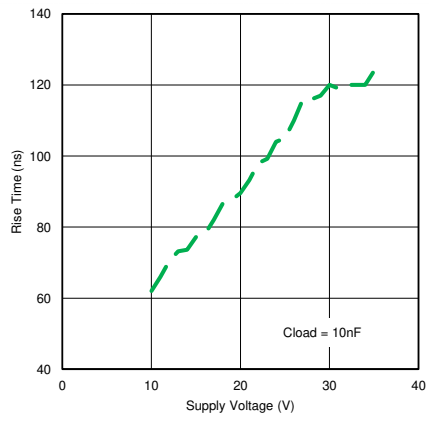


図 6-18. Rise Time vs Supply Voltage

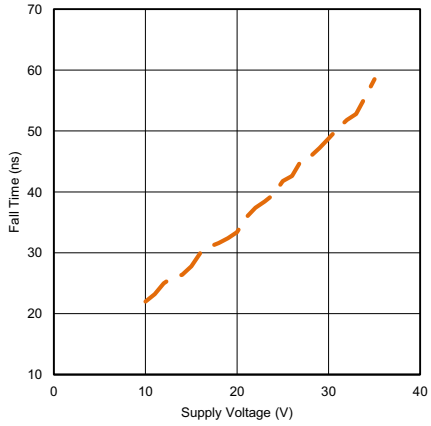


図 6-19. Fall Time vs Supply Voltage

7 Detailed Description

7.1 Overview

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be used between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when having the PWM controller directly drive the gates of the switching devices is not feasible. This situation is often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is required to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar (or P-channel and N-channel MOSFET) transistors in totem-pole arrangement, being emitter-follower configurations, prove inadequate for this function because these circuits lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive, and UVLO functions. Gate drivers have other uses such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, controlling floating power device gates, and reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27532-Q1 device is very flexible in this role with a strong current-drive capability and wide supply-voltage range up to 35 V. These features allow the driver to be used in 12-V Si MOSFET applications, 20-V and –5-V (relative to source) SiC FET applications, 15-V and –15-V (relative to emitter) IGBT applications, and many others. As a single-channel driver, the UCC27532-Q1 device can be used as a low-side or high-side driver. To use the device as a low-side driver, the switch ground is typically the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node, however, signal isolation is required from the controller as well as an isolated bias to the UCC27532-Q1 device. Alternatively, in a high-side drive configuration the UCC27532-Q1 device can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC27532-Q1 device must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turnon and turnoff speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27532-Q1 device extremely important components in switching power combining benefits of high-performance, low cost, component count and board-space reduction, and simplified system design.

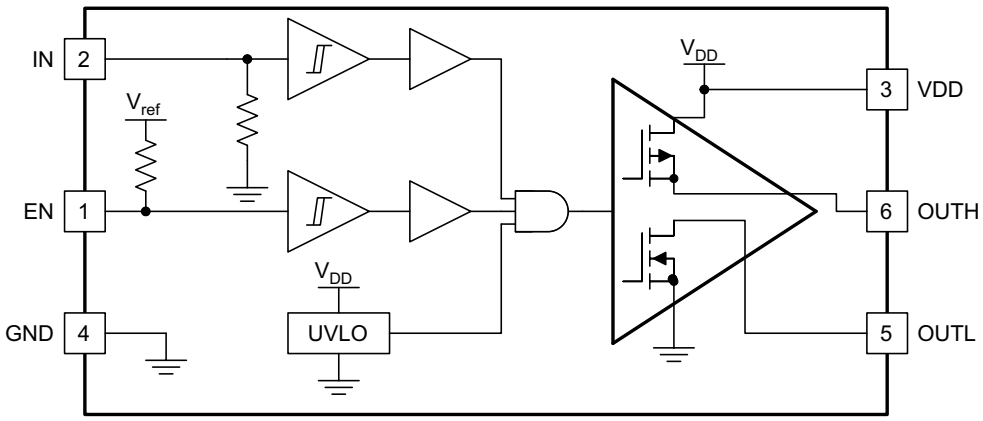
表 7-1. UCC27532-Q1 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC27532-Q1 device device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative (relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down.
	High UVLO of 8.9 V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (IN) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure (OUTH, OUTL).	Allows independent optimization of turnon and turnoff speeds using series gate resistors.
Strong sink current (5 A) and low pulldown impedance (0.65 Ω).	High immunity to high dV/dt Miller turnon events.
CMOS compatible input threshold logic with wide 2.1-V hysteresis.	Excellent noise immunity.

表 7-1. UCC27532-Q1 Features and Benefits (続き)

FEATURE	BENEFIT
Input capable of withstanding –6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

7.2 Functional Block Diagram



NOTE: EN Pullup Resistance to V_{ref} = 500 kΩ, V_{ref} = 5.8 V, In Pulldown Resistance to GND = 230 kΩ

7.3 Feature Description

7.3.1 VDD Undervoltage Lockout

The UCC27532-Q1 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD-pin supply-circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when the VDD voltage less than V_{ON} during power up and when the VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with a 700-mV typical hysteresis. This hysteresis helps prevent chatter when low-VDD supply voltages have noise from the power supply. This hysteresis also prevents chatter when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

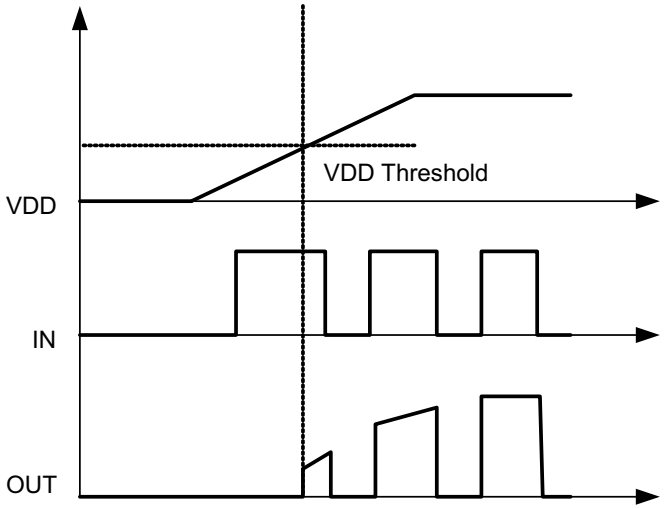


図 7-1. Power Up

7.3.2 Input Stage

The input pin of UCC27532-Q1 device is based on a standard CMOS-compatible input-threshold logic that is dependent on the VDD supply voltage. The input threshold is approximately 55% of VDD for rise and 45% of VDD for fall. With 18-V VDD, the typical high threshold is 9.4 V and the typical low threshold is 7.3 V. The 2.1-V hysteresis offers excellent noise immunity compared to traditional TTL logic implementations where the hysteresis is typically less than 0.5 V. For proper operation using CMOS input, the input signal level must be at a voltage equal to VDD. Using an input signal slightly larger than the threshold but less than VDD for the CMOS input can result in slower propagation delay from input to output (for example). This device also features tight control of the input-pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function where the output is held in the low state whenever the input pin is in a floating condition. This function is achieved using GND pulldown resistors on the noninverting input pin (IN pin), as shown in the .

The input stage of the driver is best driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input-connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which can be referenced to the power ground, this can interfere with the differential voltage between input pins and GND and can trigger an unintended change of output state. Because of the fast 17-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses a risk of damage
- 2.1-V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate-charge-related power dissipation in the gate-driver device package and transferring the dissipation into the external resistor itself.

7.3.3 Enable Function

The enable (EN) pin of the UCC27532-Q1 device has an internal pullup resistor to an internal reference voltage. Therefore, leaving the EN pin floating turns on the driver and allows it to send output signals properly. If desired, the EN pin can also be driven by low-voltage logic to enable and disable the driver.

7.3.4 Output Stage

図 7-2 shows the output stage of the UCC27532-Q1 device. The UCC27532-Q1 device features a unique architecture on the output stage which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turnon.

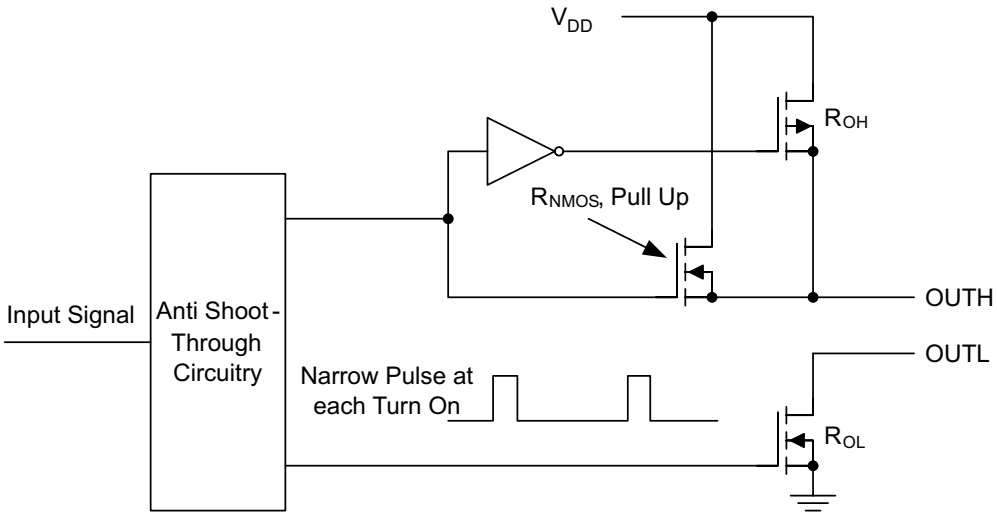


図 7-2. UCC27532-Q1 Gate-Driver Output Stage

The R_{OH} parameter (see セクション 6.5) is a DC measurement and is representative of the on-resistance of the P-Channel device only because the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see セクション 6.5), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In UCC27532-Q1 device, the effective resistance of the hybrid pullup structure is approximately 3 × R_{OL}.

The UCC27532-Q1 device is capable of delivering 2.5-A source, 5-A Sink (asymmetrical drive) at VDD = 18 V. Strong sink capability in asymmetrical drive results in a very low pulldown impedance in the driver output stage which boosts immunity against the parasitic Miller turnon (high slew-rate dV/dt turnon) effect that is seen in both IGBT and FET power switches.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in the off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in 図 7-3.

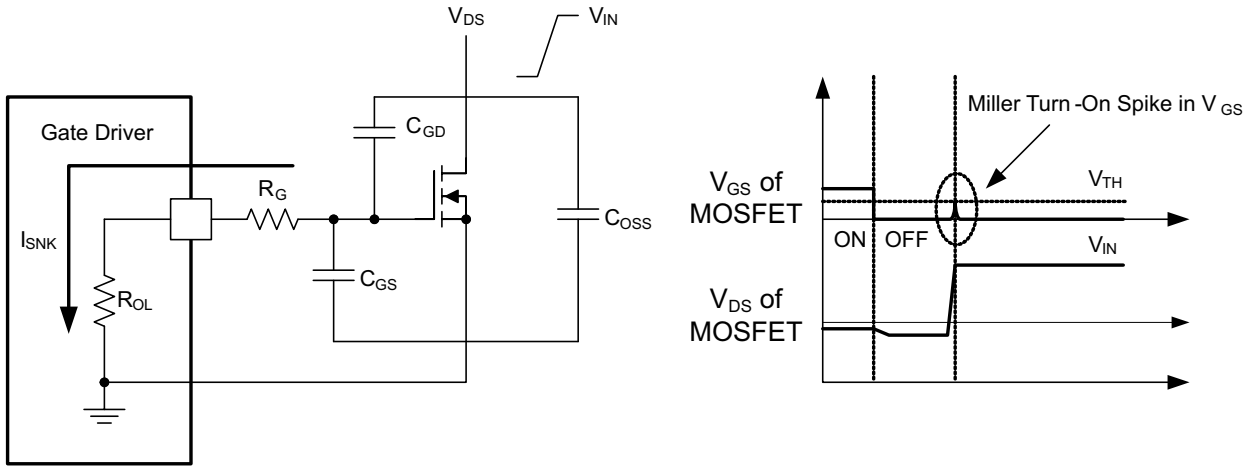


図 7-3. Low Pulldown Impedance in the UCC27532-Q1 Device (Output Stage Mitigates Miller Turnon Effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation because of the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky diode clamps can be eliminated.

7.4 Device Functional Modes

表 7-2. Input and Output Logic Truth Table

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27532-Q1 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V (relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC27532-Q1 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC27532-Q1. Alternatively, in a high-side drive configuration the UCC27532-Q1 can be tied directly to the controller signal and biased with a nonisolated supply. However, in this configuration the outputs of the UCC27532-Q1 must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turnon and turnoff speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27532-Q1 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

8.2 Typical Applications

8.2.1 Driving IGBT Without Negative Bias

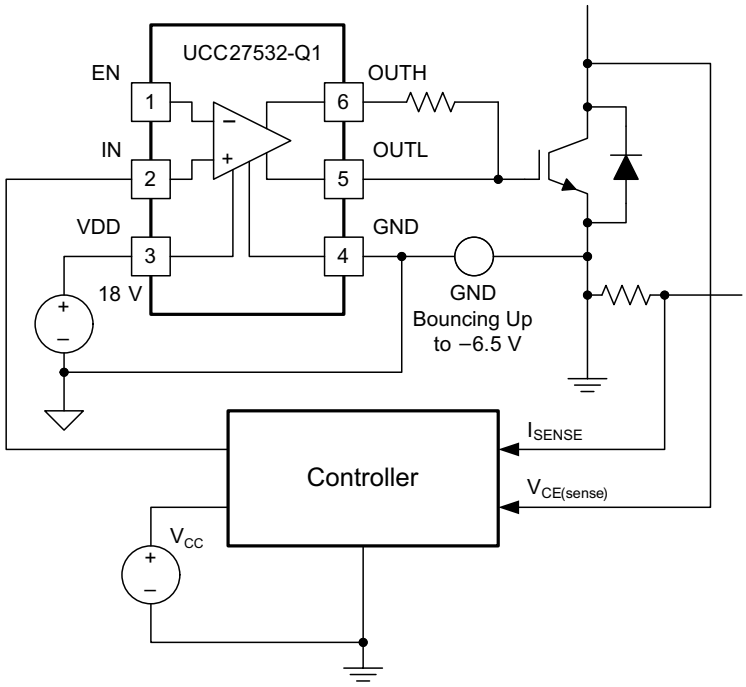


図 8-1. Driving IGBT Without Negative Bias Schematic

8.2.1.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
IN-OUT configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	18 V
Negative output low voltage	N/A
dVDS/dt(1)	20 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<0.25 W
Package type	DBV

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in セクション 8.2.1.2.4.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input-to-Output Configuration

The design should specify which type of input-to-output configuration should be used. See 表 7-2 for UCC27532-Q1 device functionality.

8.2.1.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. See the table for the actual input threshold voltage levels and hysteresis specifications for the UCC27532-Q1 devices.

8.2.1.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With an operating range from 10 V to 32 V, the UCC27532-Q1 devices can be used to drive a power switches such as power MOSFETS and IGBTs (VGE = 15 V, 18 V).

8.2.1.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dV_{DS}/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to VDS(on) in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $VGS_{(TH)}$.

To achieve the targeted dVDS/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27532-Q1 series of gate drivers can provide 2.5-A peak sourcing current, and 5A peak sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 1.5x sourcing, and 3x sinking overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ ×IPEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET data sheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power

MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

8.2.1.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers an enable and disable function achieves this requirement.

8.2.1.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. See セクション 6.6 for the propagation and switching characteristics of the UCC27532-Q1 devices.

8.2.1.2.7 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27532-Q1 features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. During turnoff the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} \tag{3}$$

where

- f_{SW} is the switching frequency

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches

between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD}V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD}V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \quad (5)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pullup structure) = 3 x R_{OL}

8.2.1.3 Application Curves

The following application curves were observed using the UCC27531 on the UCC27531EVM-184.

注

Legend: Green: EVM PWM Input, Blue: UCC27531 IN, Red: EVM GATE Output

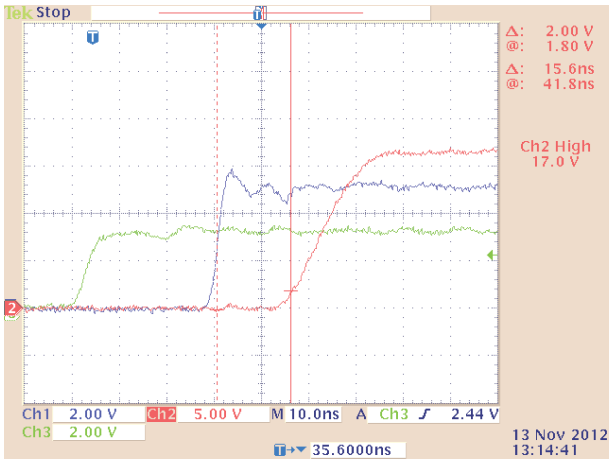


図 8-2. UCC27531DBV Input vs Output PWM Propagation Delay (high)

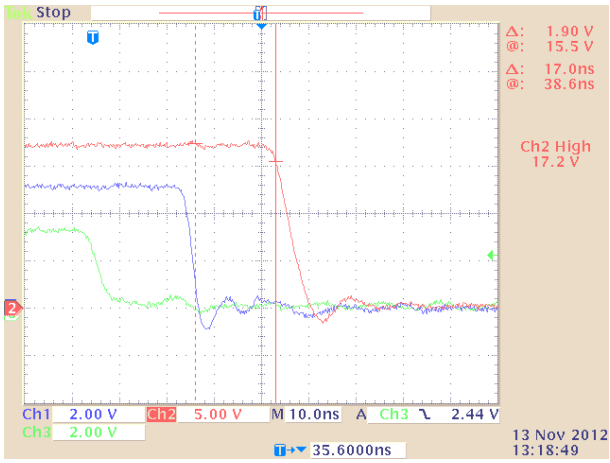


図 8-3. UCC27531DBV Input vs Output PWM Propagation Delay (low)

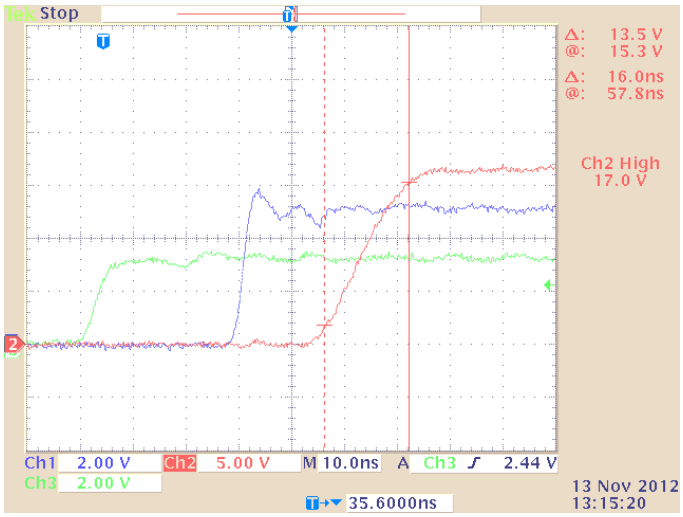


図 8-4. UCC27531DBV Input vs Output PWM Rise Time

8.2.2 Driving IGBT With 13-V Negative Turnoff Bias

The circuit configuration in 図 8-5 includes an addition 13-V supply, which is configured to bias the gate of the IGBT at 13-V negative with respect to its emitter. The negative voltage on the gate terminal ensures safe turn off of the IGBT and ensures that the IGBT remains in the blocking state in the presence of high dv/dt voltages on the collector terminal.

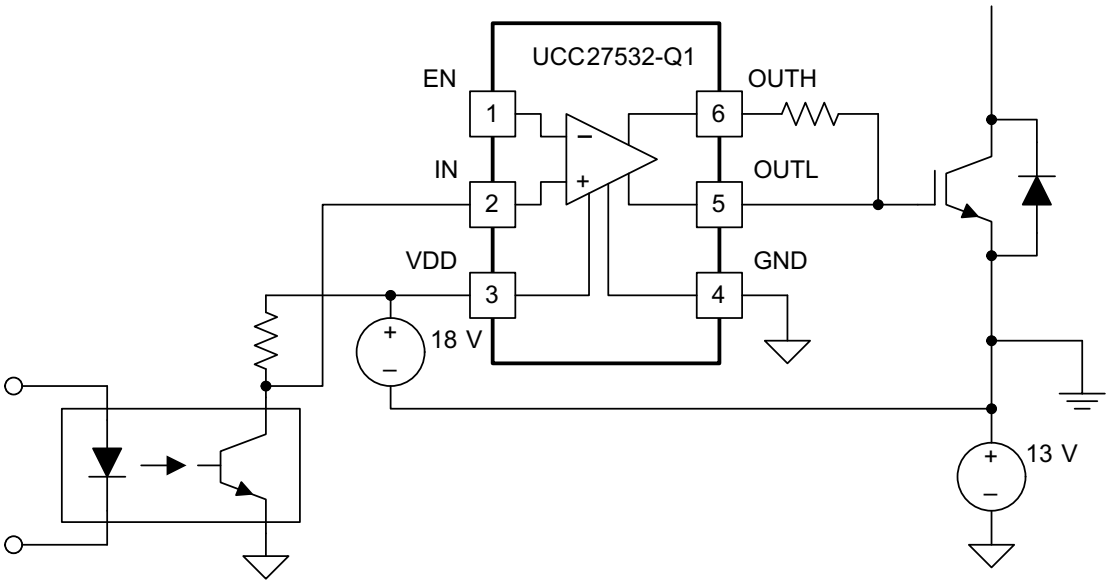


図 8-5. Driving IGBT With 13-V Negative Turnoff Bias Schematic

8.2.3 Using UCC27532-Q1 Drivers in an Inverter

In the inverter circuit shown in 図 8-6, the UCC27532-Q1 drivers for the IGBTs will require the drivers to be supplied by individually isolated power supplies to enable them to drive the floating IGBT devices in the power stage.

In addition the gate drive signals from the micro-controller to the UCC27532-Q1 will also must level shifted through isolation devices.

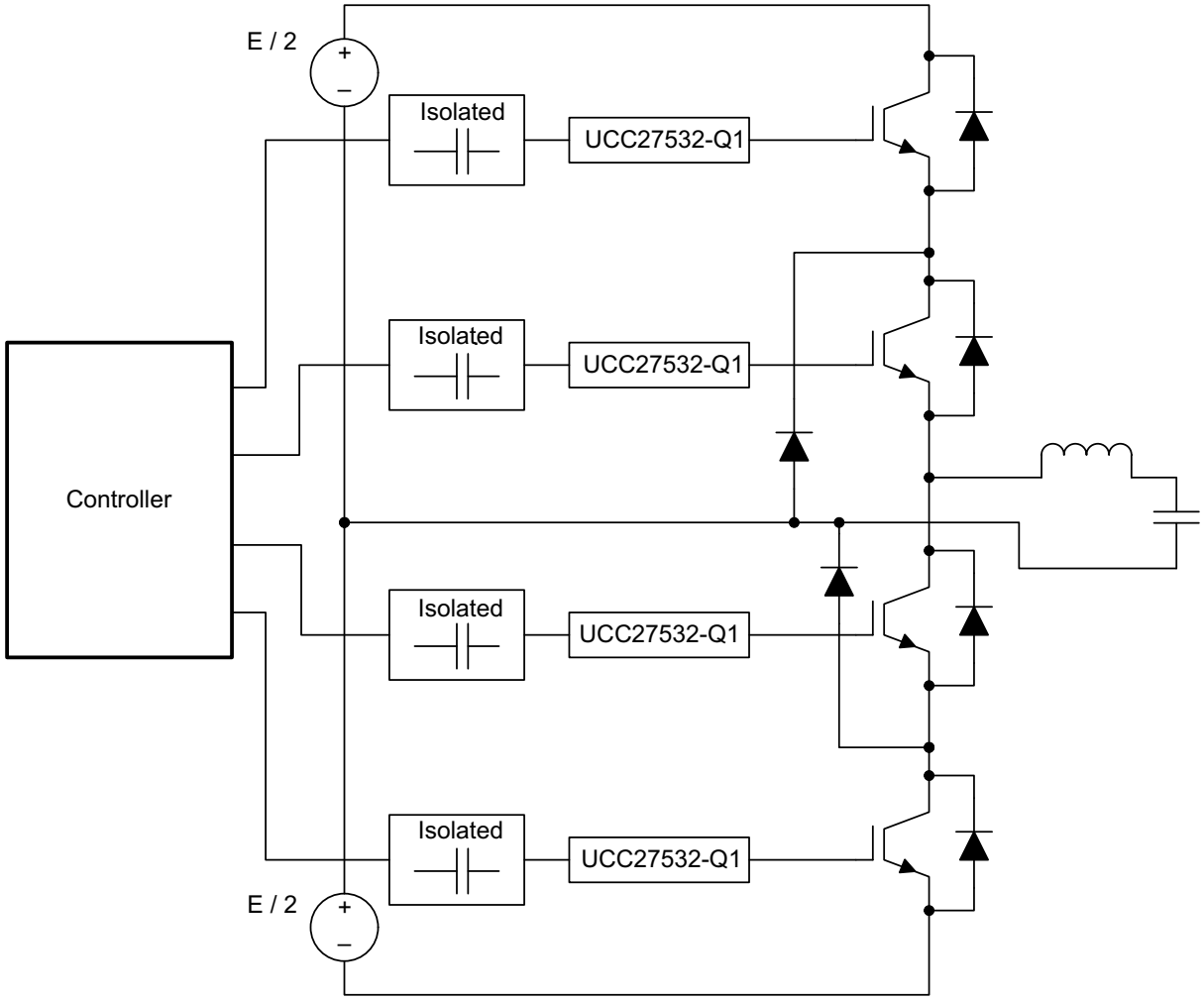


図 8-6. Using UCC27532-Q1 Drivers in an Inverter

9 Power Supply Recommendations

The bias supply voltage range for which the UCC27532-Q1 devices are rated to operate is from 10 V to 32 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 35-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 32 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys). Therefore, ensuring that, while operating at or near the 9.8 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is mandatory.

10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27532-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. TI strongly recommends adhering to the following circuit layout guidelines when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device to minimize the length of high-current traces between the driver output pins and the gate of the power-switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turnon of power switch. TI highly recommends using low-inductance SMD components such as chip resistors and chip capacitors.
- The turnon and turnoff current-loop paths (driver device, power switch, and VDD bypass capacitor) must be minimized as much as possible to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances — during turnon and turnoff transients — which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop which takes advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver must be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and others at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT can corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

10.2 Layout Example

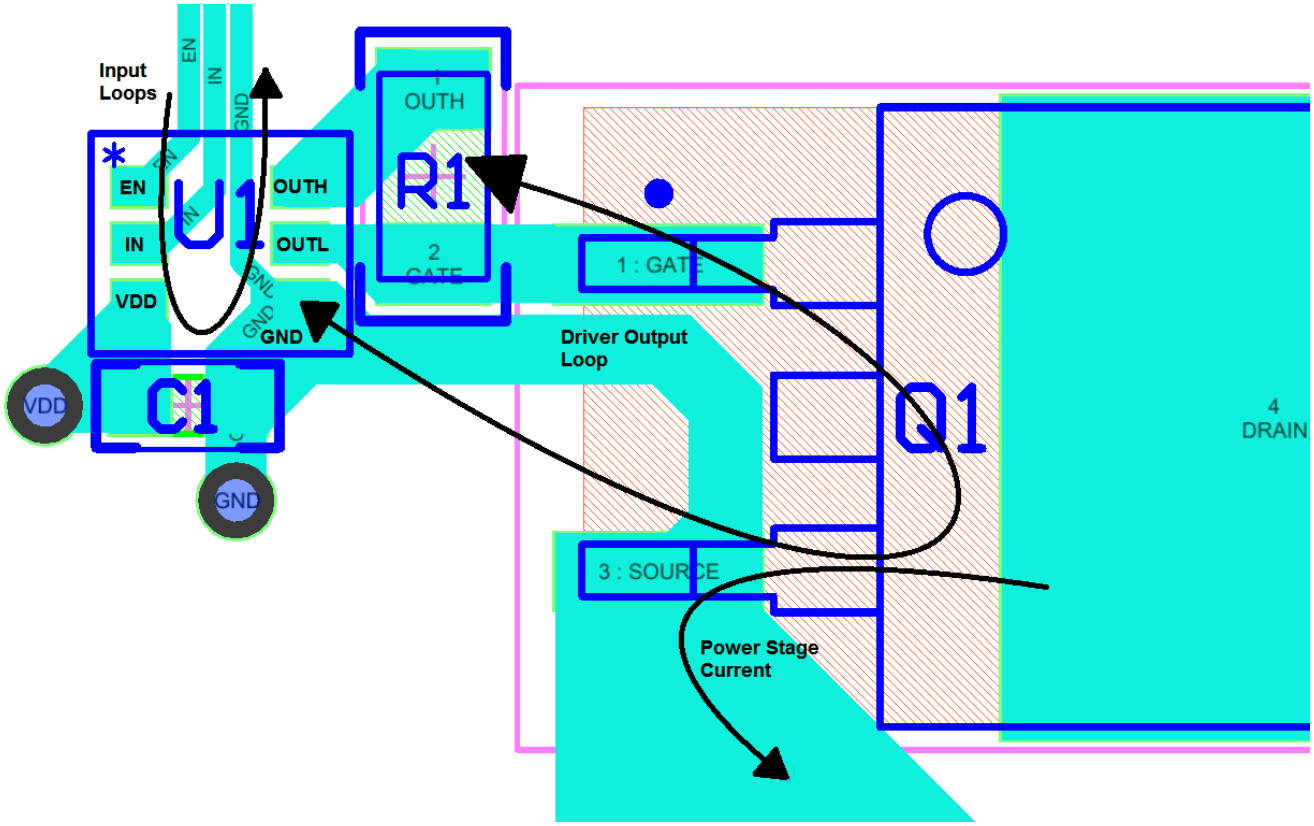


図 10-1. Layout Example: UCC27531DBV

10.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the セクション 6.4 table. For detailed information regarding the thermal information table, see SPRA953.

11 Device and Documentation Support

11.1 サード・パーティ製品に関する免責事項

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Using the UCC27531EVM-184*, SLUUA70
- *UCC27531-Q1 2.5-A and 5-A, 35-VMAX VDD FET and IGBT Single-Gate Driver*, SLVSC82

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2015) to Revision C (September 2024) **Page**

- 「特長」の HBM および CDM ESD 分類レベルを更新 1
- 「アプリケーション」のリンクを更新 1
- Added VDD = 16V to *INPUT (IN)* and *ENABLE (EN)* test conditions 6

Changes from Revision A (January 2014) to Revision B (August 2015) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1

Changes from Revision * (December 2013) to Revision A (January 2014) **Page**

- ドキュメントのステータスを製品プレビューから量産データへ変更 3

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27532QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	EAIQ
UCC27532QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	EAIQ
UCC27532QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	EAIQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC27532-Q1 :

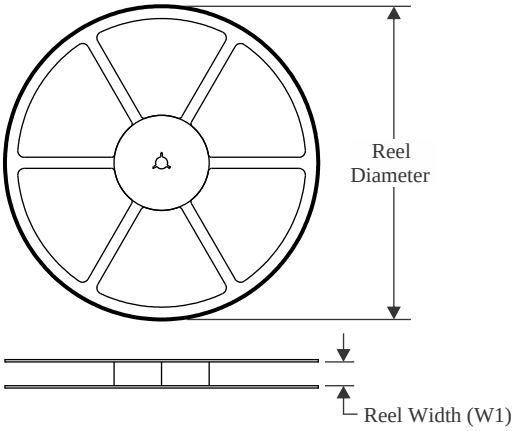
- Catalog : UCC27532

NOTE: Qualified Version Definitions:

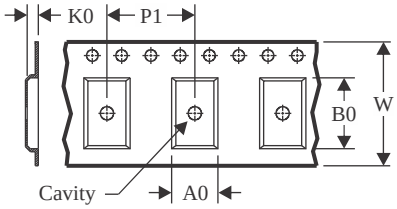
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

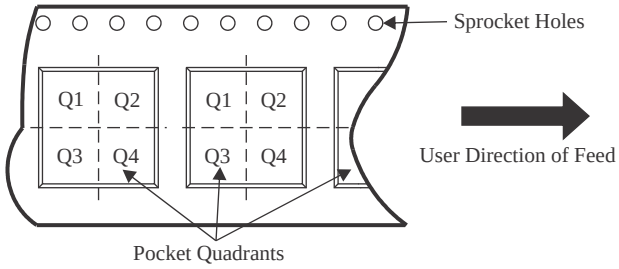


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

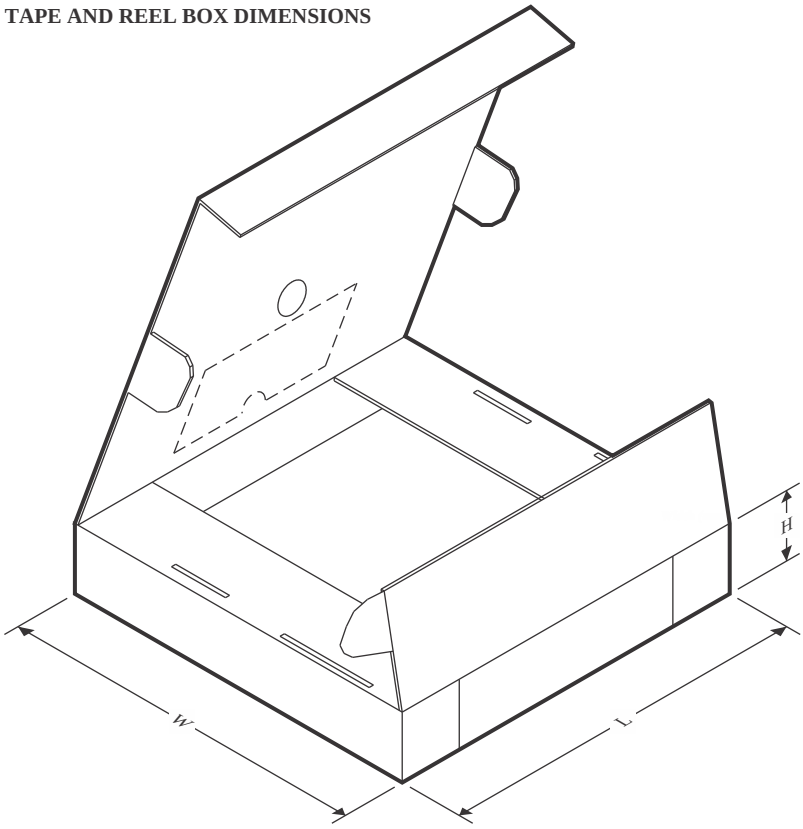
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27532QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

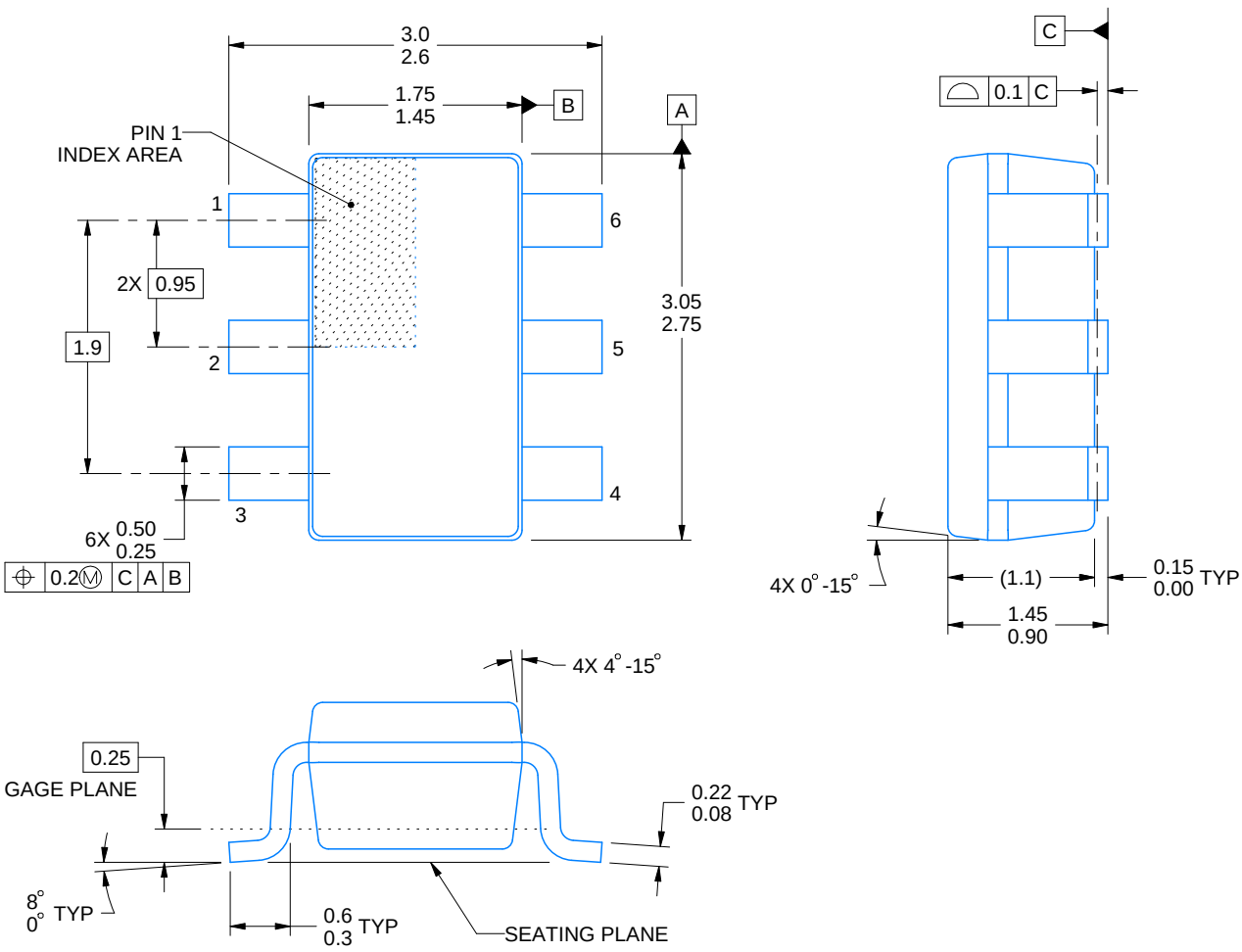
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27532QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

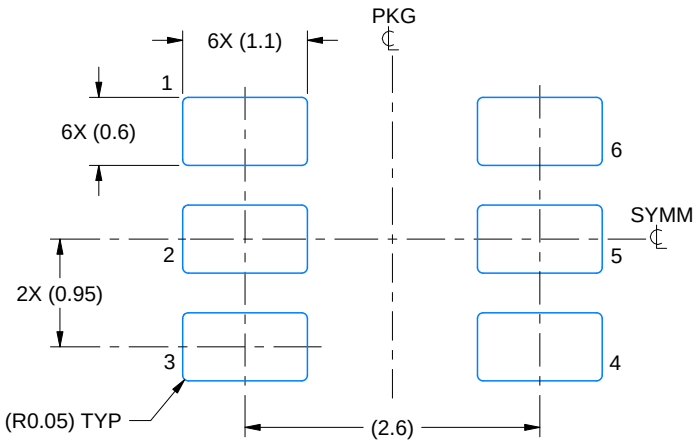
SMALL OUTLINE TRANSISTOR



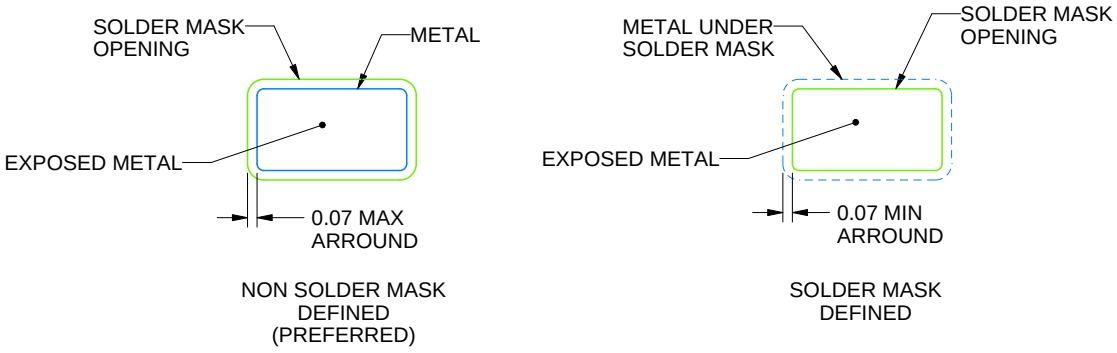
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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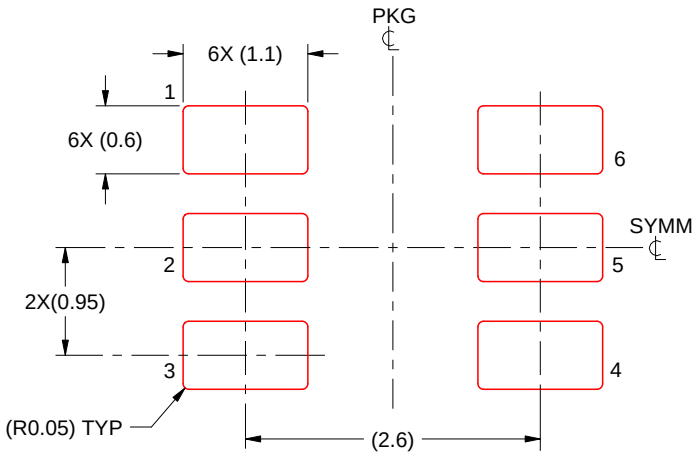
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月