UCC27524 デュアル 5A、高速ローサイド ゲート ドライバ、負入力電圧機能付

1 特長

- 業界標準のピン配置
- 2 つの独立したゲート駆動チャネル
- ソースおよびシンク駆動ピーク電流：5A
- 出力ごとに独立したイネーブル機能
- TTL および CMOS 互換のロジック スレッショルド (電源電圧に無関係)
- ヒステリシス付きのロジック スレッショルドによる高いノイズ耐性
- 負入力電圧 (-5V) に対応
- 入力およびイネーブル ピンの電圧レベルが VDD ピンのバイアス電源電圧に制限されない
- 4.5V～18V の単一電源電圧範囲
- VDD UVLO 時に出力を Low に保持 (パワーアップ / パワーダウン時のグリッチを防止)
- 高速伝搬遅延時間：17ns (標準値)
- 高速立ち上がり / 立ち下がり時間：6ns/10ns (標準値)
- 2 チャネル間遅延マッチング：1ns (代表値)
- 2 出力の並列による高駆動電流
- 入力フローティング時に出力を Low に保持
- SOIC-8、HVSSOP-8 PowerPAD™ パッケージ オプション
- 動作時の接合部温度範囲：–40～150°C

2 アプリケーション

- スイッチ モード電源
- DC/DC コンバータ
- モータ制御、太陽光発電
- 最新の広バンドギャップ パワー デバイス (GaN など) 用ゲート駆動

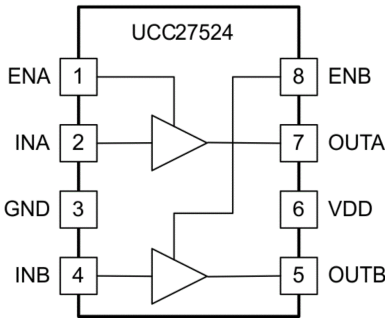
3 概要

UCC27524 デバイスは、デュアル チャネルで高速な、ローサイドのゲート ドライバ デバイスで、MOSFET および IGBT 電源スイッチを効果的に駆動できます。UCC27524 には、入力ピンで -5V を直接扱う機能があるため、堅牢性が向上しています。UCC27524 はデュアル非反転ドライバです。本質的に貫通電流を最小限に抑える設計により、UCC27524 は、容量性負荷に対してソース / シンクともに最大 5A の高いピーク電流パルスを供給できます。また、レール ツー レールの駆動能力を持ち、伝搬遅延は標準 17ns と非常に小さくなっています。さらに、2 つのチャネル間で内部伝搬遅延がマッチングされるため、同期整流器などタイミング条件の厳しいデュアル ゲート ドライバを必要とするアプリケーションに最適です。また、2 つのチャネルを並列接続して実質的な電流駆動能力を高めることも、1 つの入力信号で 2 つのスイッチを並行して駆動することも可能です。入力ピンのスレッショルドは、TTL および CMOS 互換の低電圧ロジックに基づき、VDD 電源電圧に依存しない固定値となっています。上限と下限のスレッショルド間に幅広いヒステリシスが設けられているため、優れたノイズ耐性が得られます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
UCC27524	D (SOIC 8)	4.90mm × 3.91mm
	DGN (HVSSOP 8)	3.00mm × 3.00mm
	DSD (WSON 8)	

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



デュアル非反転入力

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4 概要 (続き)

安全な動作のために、UCC27524 の入力ピンに内部プルアップおよびプルダウン抵抗により、入力ピンがフローティング状態のときには出力が Low に保持されます。UCC27524 は、イネーブル ピン (ENA および ENB) を搭載し、ドライバ アプリケーションの動作をよりきめ細かく制御できます。これらのピンは、アクティブ ハイ ロジックでは内部で VDD にプルアップされ、標準動作時にはオープンになります。

UCC27524 ファミリ デバイスは、SOIC-8 (D)、露出したパッド (DGN) パッケージ付きの VSSOP-8、および露出したパッド (DSD) パッケージ付きの 3mm × 3mm WSON-8 パッケージで供給されます。

5 Pin Configuration and Functions

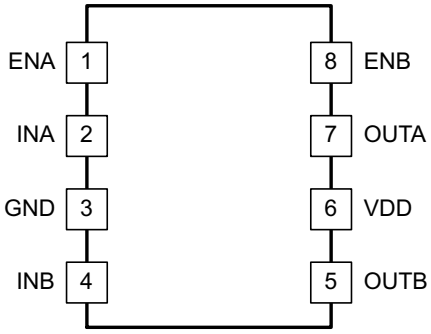


図 5-1. D and DGN Packages 8-Pin SOIC and HVSSOP Top View

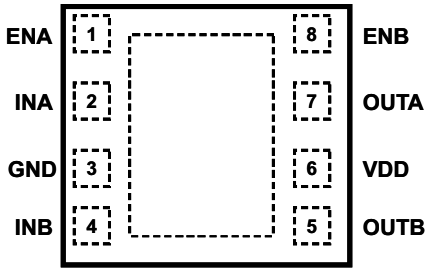


図 5-2. DSD Package 8-Pin WSON Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the UCC27324 N/C pin.
ENB	8	I	Enable input for Channel B: ENB is biased LOW to disables the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable Channel B output. ENB is allowed to float hence; the pin-to-pin compatibility with the UCC27324 N/C pin.
GND	3	-	Ground: All signals are referenced to this pin.
INA	2	I	Input to Channel A: INA is the non-inverting input in the UCC27524 device. OUTA is held LOW if INA is unbiased or floating.
INB	4	I	Input to Channel B: INB is the non-inverting input in the UCC27524 device. OUTB is held LOW if INB is unbiased or floating.
OUTA	7	O	Output of Channel A
OUTB	5	O	Output of Channel B
VDD	6	I	Bias supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
OUTA, OUTB voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns(4)	–2	VDD + 0.3	V
Output continuous source/sink current	I_{OUT_DC}		0.3	A
Output pulsed source/sink current (0.5 µs)	I_{OUT_pulsed}		5	A
INA, INB, ENA, ENB voltage(3)	D and DGN package	–5	20	V
	DSD package	-0.3	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.
(4) Values are verified by characterization on bench.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	D, DGN Package	±2000	V
			DSD package	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4.5	12	18	V
Operating junction temperature		–40		140	°C
Input voltage, INA, INB	D and DGN package	–2		18	V
Input voltage, INA, INB	DSD package	0		18	
Enable voltage, ENA and ENB		–2		18	V

6.4 Thermal Information

THERMAL METRIC (1)		UCC27524			Unit
		DGN	D	DSD	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	126.4	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.8	67.0	46.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	69.9	22.4	
ψ_{JT}	Junction-to-top characterization parameter	2.6	19.2	0.7	
ψ_{JB}	Junction-to-board characterization parameter	22.3	69.1	22.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	n/a	9.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, VDD = 12 V, $T_A = T_J$ = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS (D, DGN)						
I_{VDDq}	VDD quiescent supply current	V_{INx} = 3.3 V, VDD = 3.4 V, ENx = VDD		300	450	µA
I_{VDD}	VDD static supply current	V_{INx} = 3.3 V, ENx = VDD		0.6	1.0	mA
I_{VDD}	VDD static supply current	V_{INx} = 0 V, ENx = VDD		0.7	1.0	mA
I_{VDDO}	VDD operating current	f_{SW} = 1000 kHz, ENx = VDD, V_{INx} = 0 V – 3.3 V PWM		3.2	3.8	mA
I_{DIS}	VDD disable current	V_{INx} = 3.3 V, ENx = 0 V		0.8	1.1	mA
BIAS CURRENTS (DSD)						
$I_{DD(off)}$	Start-up current	V_{DD} = 3.4 V, INA = V_{DD}, INB = V_{DD}	55	110	175	µA
		V_{DD} = 3.4 V, INA = GND, INB = GND	25	75	145	
UNDERVOLTAGE LOCKOUT (UVLO) (D, DGN)						
V_{VDD_ON}	VDD UVLO rising threshold		3.8	4.1	4.4	V
V_{VDD_OFF}	VDD UVLO falling threshold		3.5	3.8	4.1	V
V_{VDD_HYS}	VDD UVLO hysteresis			0.3		V
UNDERVOLTAGE LOCKOUT (UVLO) (DSD)						
V_{ON}	Supply start threshold	T_J = 25°C	3.91	4.2	4.5	V
		T_J = –40°C to 140°C	3.7	4.2	4.65	
V_{OFF}	Minimum operating voltage after supply start		3.4	3.9	4.4	
VDD_H	Supply voltage hysteresis		0.2	0.3	0.5	
INPUT (INA, INB) (D, DGN)						
V_{INx_H}	Input signal high threshold	Output High, ENx = HIGH	1.8	2	2.3	V
V_{INx_L}	Input signal low threshold	Output Low, ENx = HIGH	0.8	1	1.2	V
V_{INx_HYS}	Input signal hysteresis			1		V
R_{INx}	INx pin pulldown resistor	INx = 3.3 V		120		kΩ
INPUT (INA, INB) (DSD)						

6.5 Electrical Characteristics (続き)

Unless otherwise noted, VDD = 12 V, $T_A = T_J$ = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins	1.9	2.1	2.3	V
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	1	1.2	1.4	
V_{IN_HYS}	Input hysteresis		0.7	0.9	1.1	
ENABLE (ENA, ENB) (D, DGN)						
V_{ENx_H}	Enable signal high threshold	Output High, INx = HIGH	1.8	2	2.3	V
V_{ENx_L}	Enable signal low threshold	Output Low, INx = HIGH	0.8	1	1.2	V
V_{ENx_HYS}	Enable signal hysteresis			1		V
R_{ENx}	EN pin pullup resistance	ENx = 0 V		200		kΩ
ENABLE (ENA, ENB) (DSD)						
V_{EN_H}	Enable signal high threshold	Output enabled	1.9	2.1	2.3	V
V_{EN_L}	Enable signal low threshold	Output disabled	0.95	1.15	1.35	
V_{EN_HYS}	Enable hysteresis		0.7	0.95	1.1	
OUTPUTS (OUTA, OUTB) (D, DGN)						
I_{SRC} (1)	Peak output source current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
I_{SNK} (1)	Peak output sink current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–5		A
R_{OH} (2)	Pullup resistance	I_{OUT} = –50 mA, See セクション 7.3.4.		5	8.5	Ω
R_{OL}	Pulldown resistance	I_{OUT} = 50 mA		0.6	1.1	Ω
OUTPUTS (OUTA, OUTB) (DSD)						
$I_{SNK/SRC}$ (1)	Sink/source peak current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
V_{DD}-V_{OH}	High output voltage	I_{OUT} = –10 mA			0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA			0.01	
R_{OH} (2)	Output pullup resistance	I_{OUT} = –10 mA	2.5	5	7.5	Ω
R_{OL}	Output pulldown resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

6.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 12 V, T_A = T_J = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D, DGN package						
t_{Rx}	Rise time	C_{LOAD} = 1.8 nF, 20% to 80%, Vin = 0 V – 3.3 V		6	10	ns
t_{Fx}	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, Vin = 0 V – 3.3 V		10	14	ns
t_{D1x}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D2x}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D3x}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D4x}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_M	Delay matching between two channels	C_{LOAD} = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, INA = INB, $\lvert t_{RA} - t_{RB} \rvert$, $\lvert t_{FA} - t_{FB} \rvert$		1	2	ns
t_{PWmin}	Minimum input pulse width	C_L = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, Vo > 1.5 V		10	15	ns
DSD package						
t_R	Rise time	C_{LOAD} = 1.8 nF		7	18	ns
t_F	Fall time	C_{LOAD} = 1.8 nF		6	10	ns
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point		1	4	ns
t_{PW}	Minimum input pulse width that changes the output state			15	25	ns
t_{D1}, t_{D2}	Input to output propagation delay	C_{LOAD} = 1.8 nF, 5-V input pulse	6	13	23	ns
t_{D3}, t_{D4}	EN to output propagation delay	C_{LOAD} = 1.8 nF, 5-V enable pulse	6	13	23	ns

(1) Switching parameters are not tested in production.

6.7 Timing Diagrams

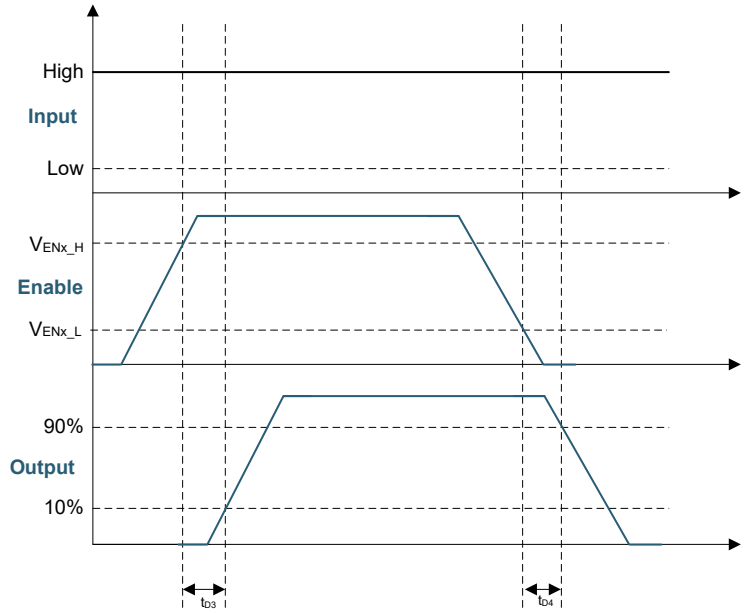


図 6-1. Enable Function

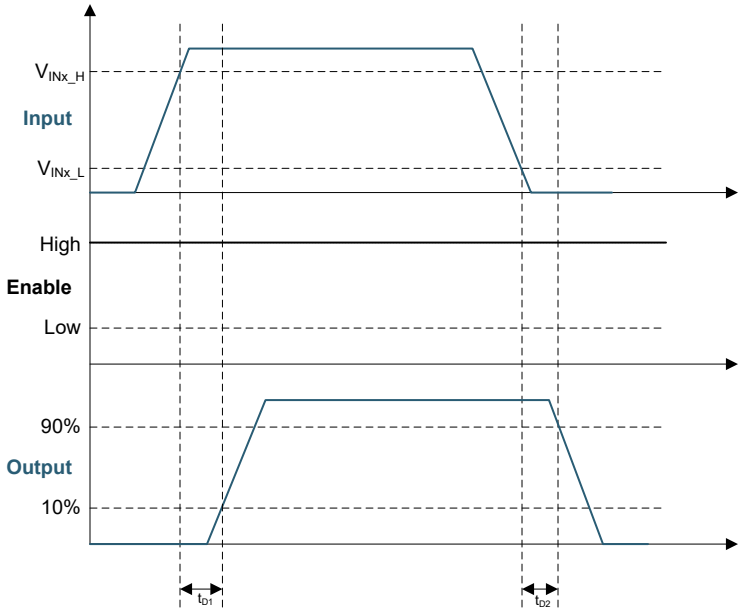


図 6-2. Input-Output Operation

6.8 Typical Characteristics

Unless otherwise specified, VDD=12 V, INx=3.3 V, ENx=3.3 V, T_J = 25°C, no load

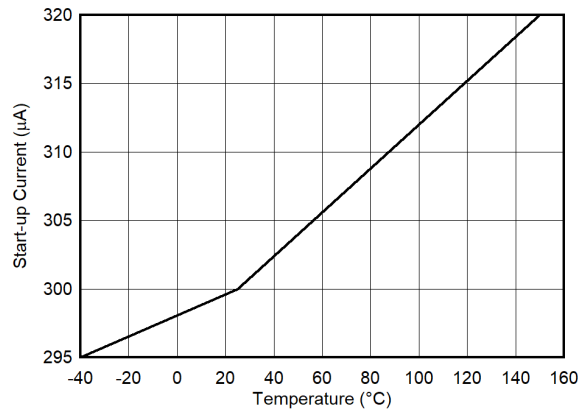


図 6-3. Start-Up and Quiescent Current

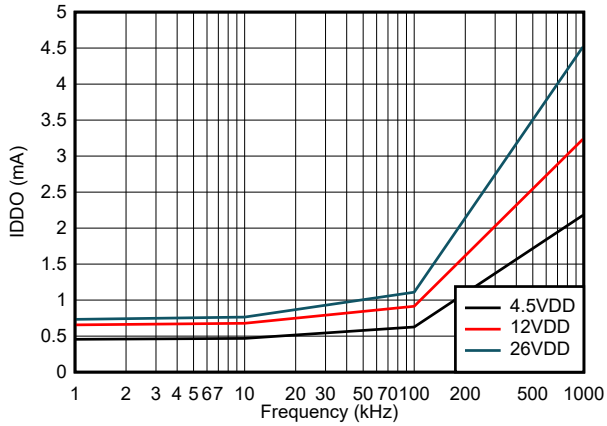


図 6-4. Operating Supply Current (Both Outputs Switching)

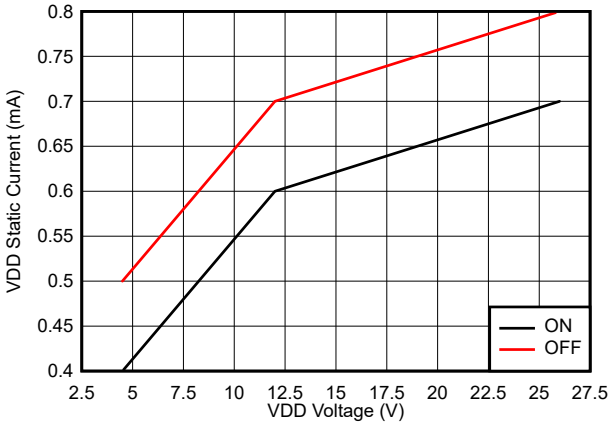


図 6-5. Static Supply Current (Outputs in DC On or Off Condition)

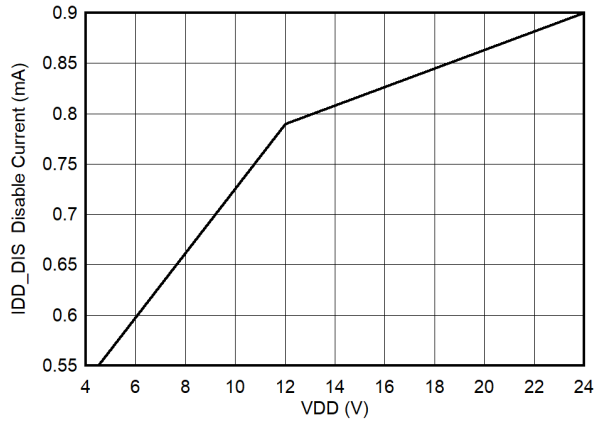


図 6-6. Disable Current (EN = 0 V)

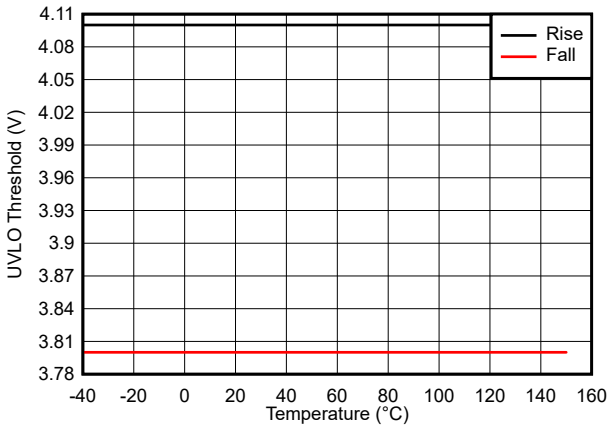


図 6-7. VDD UVLO Threshold

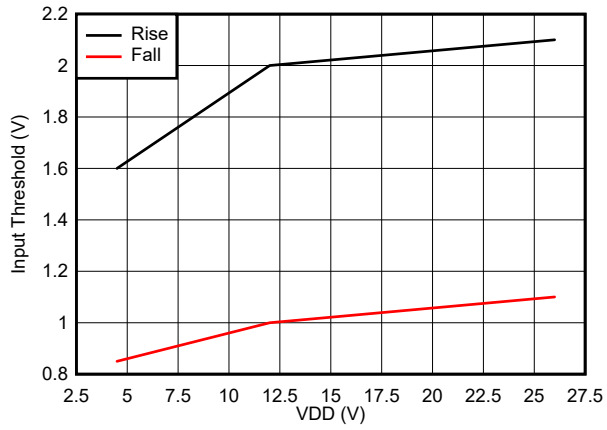


図 6-8. Input Thresholds

6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12 V, INx=3.3 V, ENx=3.3 V, T_J = 25°C, no load

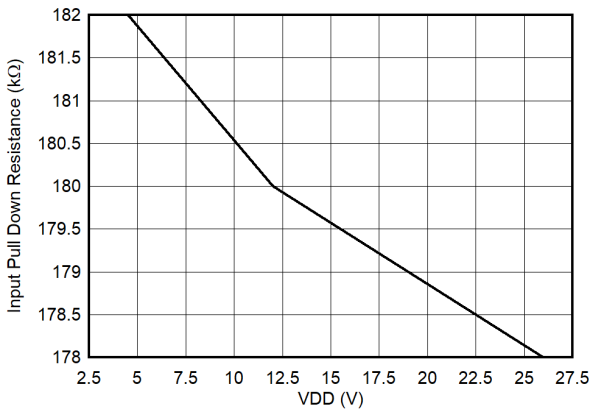


図 6-9. Input Pulldown Resistance

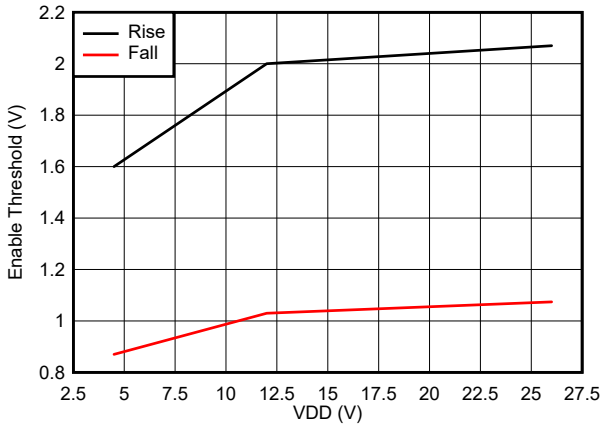


図 6-10. Enable Threshold

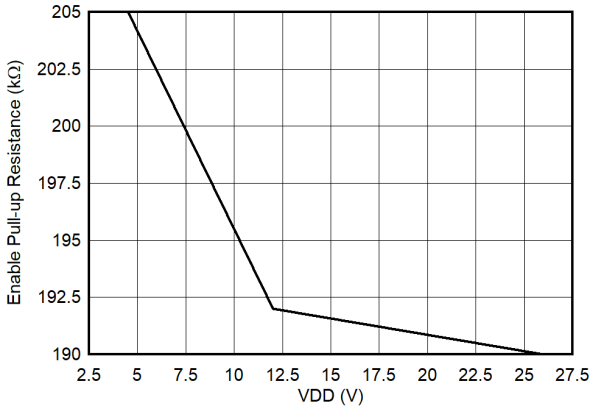


図 6-11. Enable Pullup Resistance

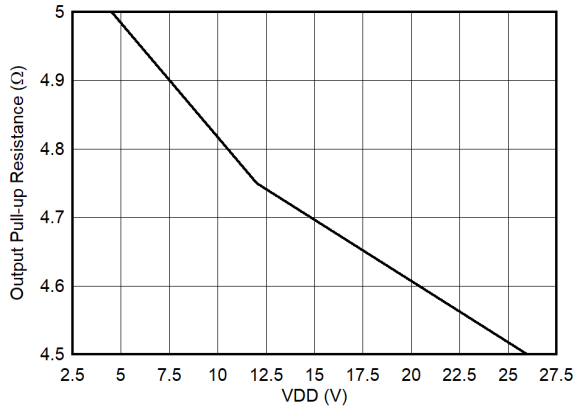


図 6-12. Output Pullup Resistance

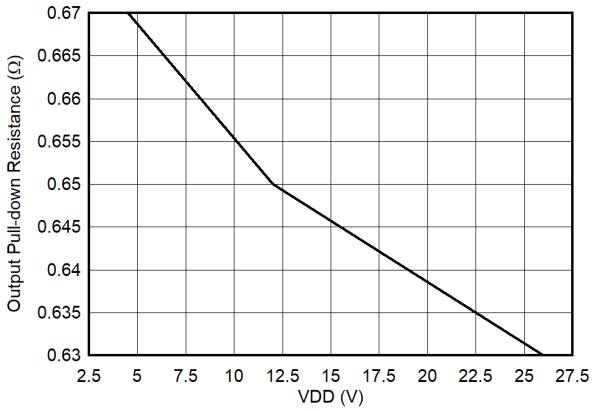
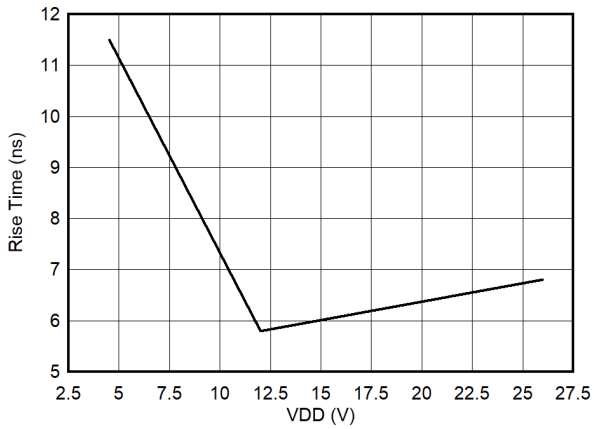


図 6-13. Output Pulldown Resistance

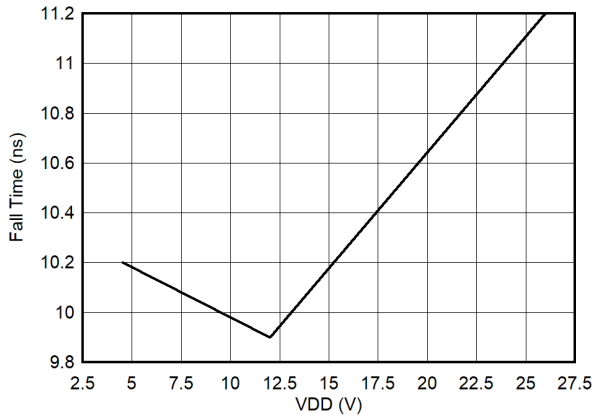


C_{LOAD} = 1.8 nF

図 6-14. Output Rise Time vs VDD

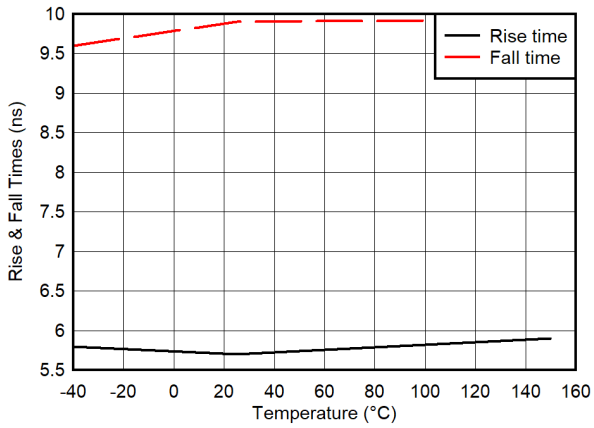
6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12 V, INx=3.3 V, ENx=3.3 V, T_J = 25°C, no load



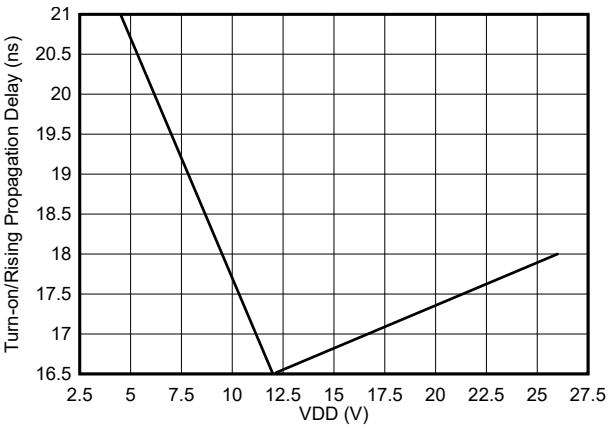
C_{LOAD} = 1.8 nF

図 6-15. Output Fall Time vs VDD



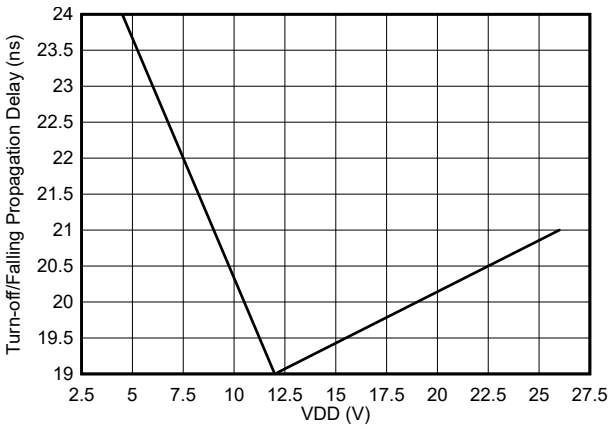
C_{LOAD} = 1.8 nF

図 6-16. Output Rise and Fall Time vs Temperature



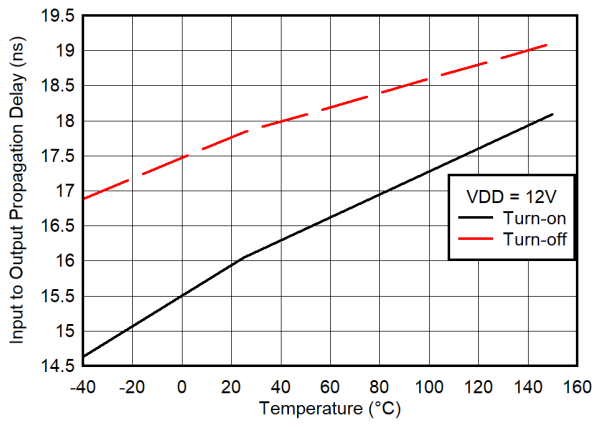
C_{LOAD} = 1.8 nF

図 6-17. Input to Output Rising (Turn-On) Propagation Delay vs VDD



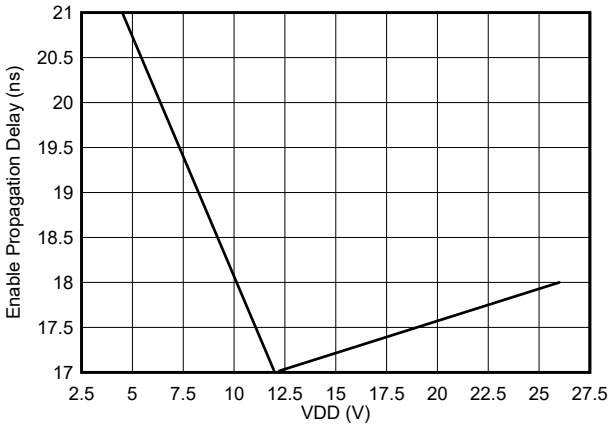
C_{LOAD} = 1.8 nF

図 6-18. Input to Output Falling (Turn-Off) Propagation Delay vs VDD



C_{LOAD} = 1.8 nF

図 6-19. Input Propagation Delay vs Temperature

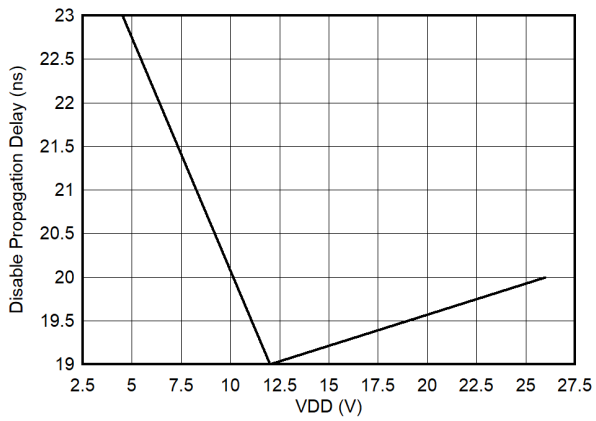


C_{LOAD} = 1.8 nF

図 6-20. Enable to Output Rising Propagation Delay

6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12 V, INx=3.3 V, ENx=3.3 V, T_J = 25°C, no load



C_{LOAD} = 1.8 nF

図 6-21. Enable to Output Falling Propagation Delay

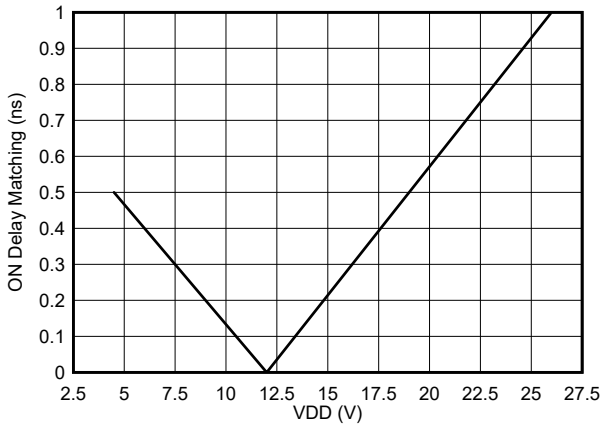


図 6-22. Turn-on/Rising Delay Matching

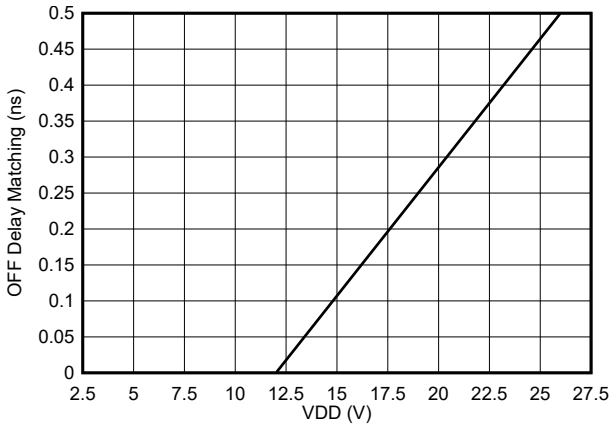


図 6-23. Turn-Off and Falling Delay Matching

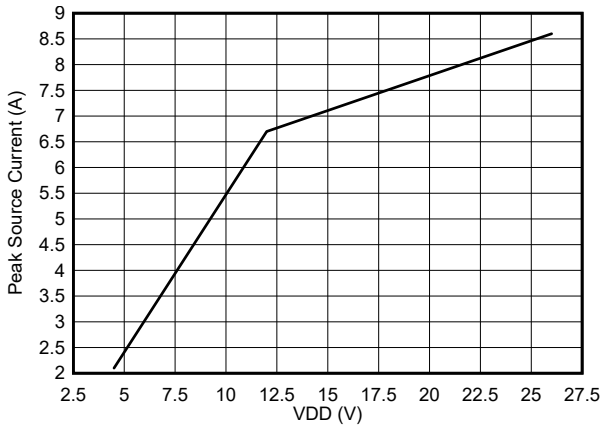


図 6-24. Peak Source Current vs VDD

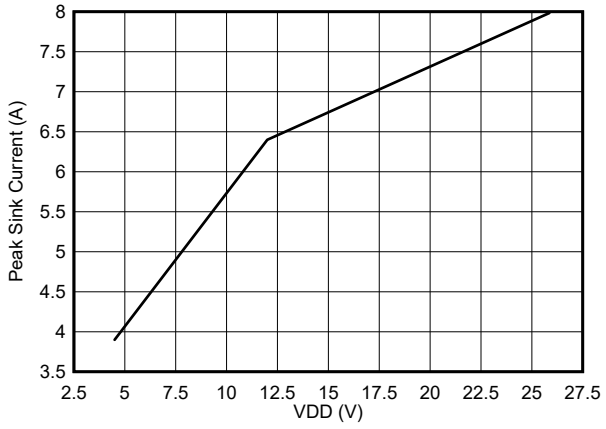


図 6-25. Peak Sink Current vs VDD

7 Detailed Description

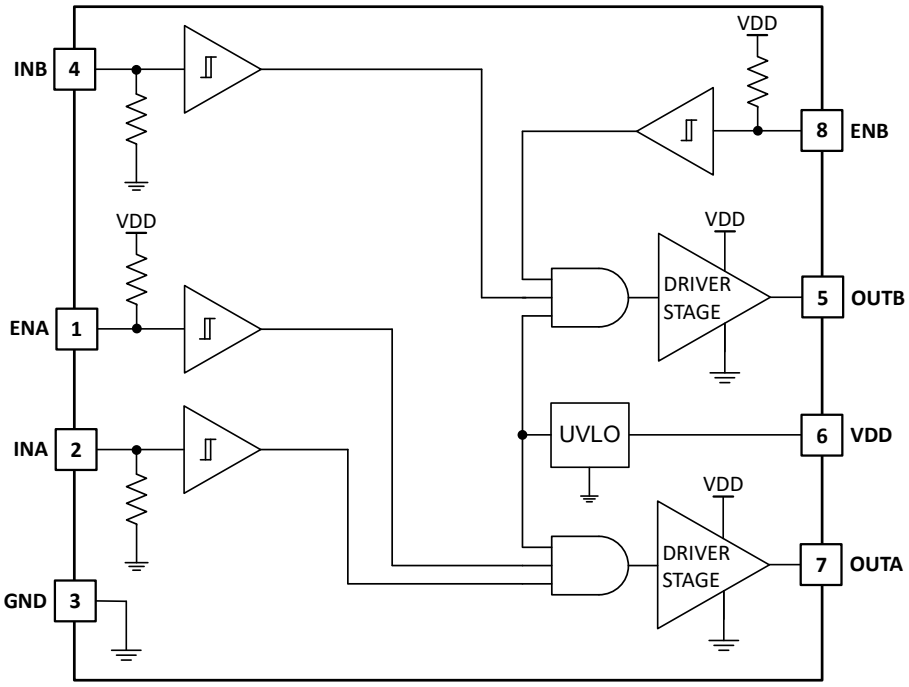
7.1 Overview

The UCC27524 device represents Texas Instruments' latest generation of dual-channel, low-side, high-speed, gate-driver devices featuring a 5-A source and sink current capability, industry best-in-class switching characteristics, and a host of other features listed in 表 7-1 all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

表 7-1. UCC27524 Features and Benefits

FEATURE	BENEFIT
Best-in-class 17-ns (typ) propagation delay	Extremely low-pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded VDD Operating range of 4.5 to 18 V	Flexibility in system design
Expanded operating temperature range of –40 °C to +150 °C (See Electrical Characteristics table)	Flexibility in system design
VDD UVLO Protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held Low when input pins (INx) in floating condition	Protection feature, especially useful in passing abnormal condition tests during safety certification
Outputs enable when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the UCC27324 device from Texas Instruments, in designs where Pin 1 and Pin 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Ability of input and enable pins to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Ability to handle –5 V_{DC} (max) at input pins	Increased robustness in noisy environments

7.2 Functional Block Diagram



Typical ENx pullup resistance is 200 kΩ and INx pulldown resistance is 120 kΩ.

7.3 Feature Description

7.3.1 Operating Supply Current

The UCC27524 devices feature very low quiescent I_{DD} currents. The typical operating-supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in Electrical Characteristics. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, see 図 6-5) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and finally any current related to pullup resistors on the enable pins (see Functional Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels is provided in 図 6-4. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

7.3.2 Input Stage

The input pins of the UCC27524 gate-driver devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typ 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27524 devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Typical Characteristics). The very low input capacitance on these pins reduces loading and increases switching speed.

The UCC27524 device features an important protection feature that holds the output of a channel when the respective pin is in a floating condition. This is achieved using GND pulldown resistors on all of the non-inverting input pins (INA, INB), as shown in the device block diagrams.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns) with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC27524 definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

7.3.3 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices, especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27524 device is equipped with independent enable pins (ENx) for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible, input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC27524 devices also feature tight control of the enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Typical Characteristics). The ENx pins are internally pulled up to VDD using pullup resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this floating allows the UCC27524 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27323, UCC27324, and UCC27325 respectively), where Pin 1 and Pin 8 are N/C pins. If the channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB are connected and driven together.

7.3.4 Output Stage

The UCC27524 device output stage features a unique architecture on the pullup structure, which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn-on. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.04 Ω when activated.

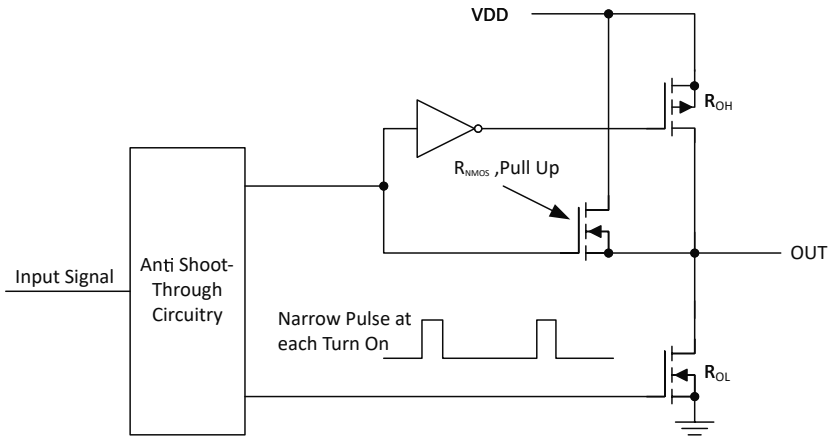


図 7-1. UCC27524 Gate Driver Output Structure

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27524 pull-up stage during the turn-on instance is much lower than what is represented by R_{OH} parameter.

The pull-down structure in the UCC27524 device is simply comprised of a N-Channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in the UCC27524device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 5A of peak reverse current transients without damage to the device.

The UCC27524 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

7.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27524 driver device features a very small, 17-ns (typical) propagation delay between input and output, which offers the lowest level of pulse width distortion for high-frequency switching applications. For example, in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive the SR MOSFETs. Additionally, the driver devices also feature extremely accurate, 1-ns (typical) matched internal propagation delays between the two channels, which is beneficial for applications that require dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels driven by a common control signal from the PFC controller. In this case, the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion, minimizing turn-on and turn-off delay differences. Another benefit of the tight matching between the two channels is that the two channels can be connected together to effectively double the drive current capability. That is, A and B channels may be combined into a single driver by connecting the INA

and INB inputs together and the OUTA and OUTB outputs together; then, a single signal controls the paralleled power devices.

Caution must be exercised when directly connecting OUTA and OUTB pins together because there is the possibility that any delay between the two channels during turnon or turnoff may result in shoot-through current conduction as shown in 図 7-2. While the two channels are inherently very well matched (2-ns Max propagation delay), note that there may be differences in the input threshold voltage level between the two channels which causes the delay between the two outputs especially when slow dV/dt input signals are employed. The following guidelines are recommended whenever the two driver channels are paralleled using direct connections between OUTA and OUTB along with INA and INB:

- Use very fast dV/dt input signals (20 V/µs or greater) on INA and INB pins to minimize impact of differences in input thresholds causing delays between the channels.
- INA and INB connections must be made as close to the device pins as possible.

Wherever possible, a safe practice would be to add an option in the design to have gate resistors in series with OUTA and OUTB. This allows the option to use 0-Ω resistors for paralleling outputs directly or to add appropriate series resistances to limit shoot-through current, should it become necessary.

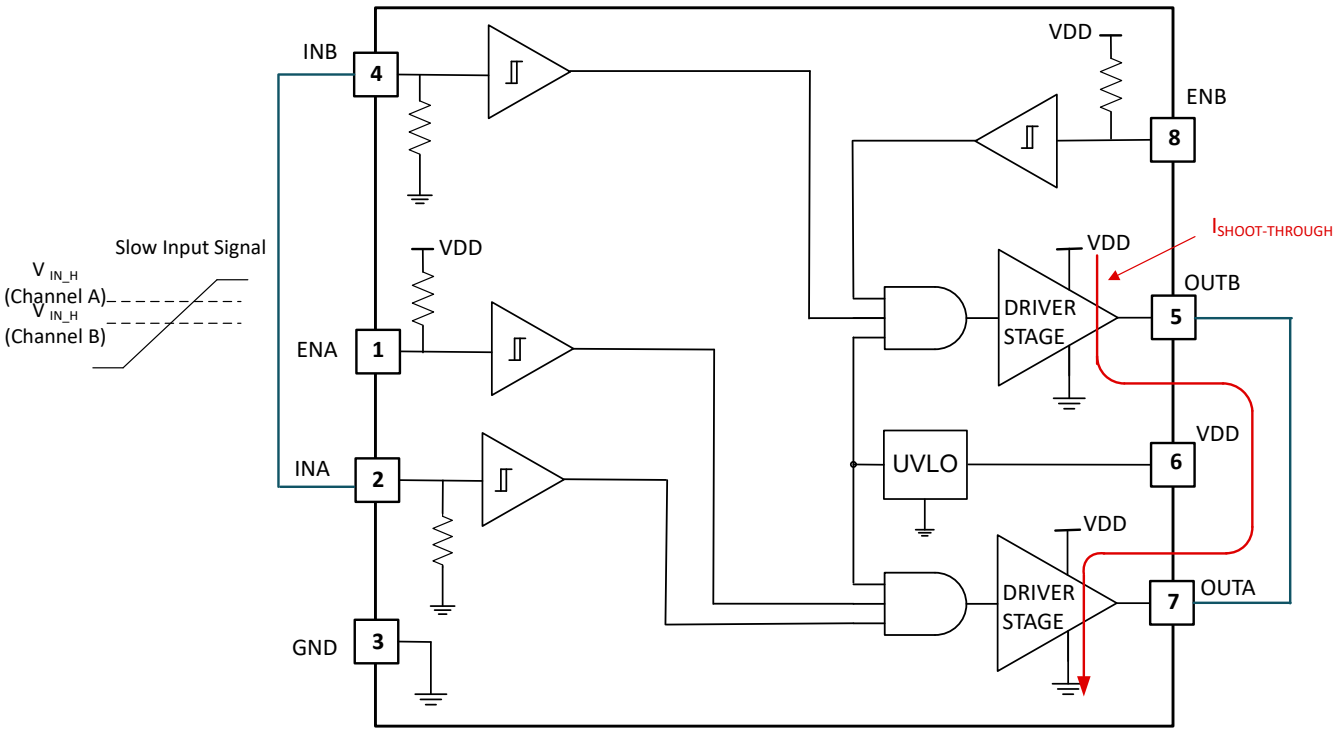


図 7-2. Slow Input Signal Can Cause Shoot-Through Between Channels During Paralleling (Recommended DV/DT is 20 V/Ms or Higher)

7.4 Device Functional Modes

表 7-2. Device Logic Table

ENA	ENB	INA	INB	UCC27524	
				OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L

表 7-2. Device Logic Table (続き)

ENA	ENB	INA	INB	UCC27524	
				OUTA	OUTB
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect the fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller. Finally, emerging wide band-gap power-device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

8.2 Typical Application

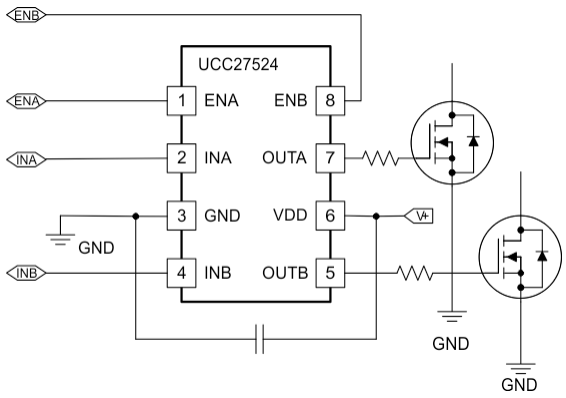


図 8-1. UCC27524 Typical Application Diagram

8.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some desiring considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VDD, UVLO, Drive current and power dissipation.

8.2.2 Detailed Design Procedure

8.2.2.1 VDD and Undervoltage Lockout

The UCC27524 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4V with 300-mV typical hysteresis. This hysteresis prevents chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power up, the UCC27524 driver-device output remains low until the V_{DD} voltage reaches the UVLO threshold if enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The operation in 図 8-2 shows that the output remains low until the UVLO threshold is reached, and then the output is in-phase with the input.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

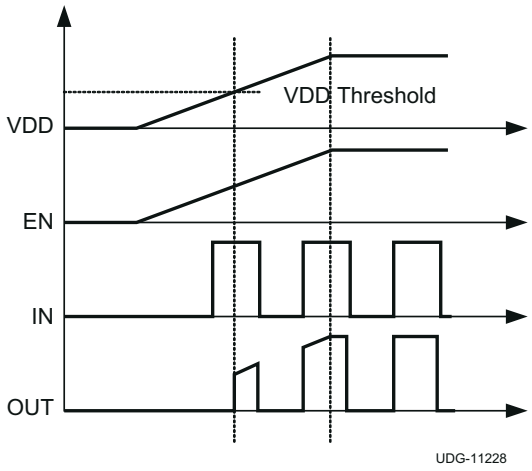


図 8-2. Power-Up Non-Inverting Driver

8.2.2.2 Drive Current and Power Dissipation

The UCC27524 driver is capable of delivering 5-A of current to a MOSFET gate for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Because UCC27524 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 1.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^{\ 2} \tag{1}$$

where

- C_{LOAD} is the load capacitor
- V_{DD} ^{2} is the bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by 式 2.

$$P_G = C_{LOAD} V_{DD}^{\ 2} f_{SW} \tag{2}$$

where

- f_{SW} is the switching frequency

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss is calculated with 式 3.

$$P_G = 10\,\text{nF} \times 12\,\text{V}^2 \times 300\,\text{kHz} = 0.432\,\text{W} \tag{3}$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD} V_{DD}$ to provide 式 4 for power:

$$P_G = C_{LOAD} V_{DD}^{\ 2} f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

Assuming that the UCC27524 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated with 式 5.

$$P_G = 2 \text{x} 60\,\text{nC} \times 12\,\text{V} \times 300\,\text{kHz} = 0.432\,\text{W} \tag{5}$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see 式 6):

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{6}$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.5 x R_{OL}

In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in 図 6-4, the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with 式 7.

$$P_Q = I_{DD} V_{DD} \tag{7}$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6\ \text{mA} \times 12\ \text{V} = 7.2\ \text{mW} \tag{8}$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ \text{W}}{12\ \text{V}} = 0.036\ \text{A} \tag{9}$$

8.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27524 device used in high-voltage boost converter application. In this application, the UCC27524 is driving the IGBT switch that has a gate charge of 110 nC.

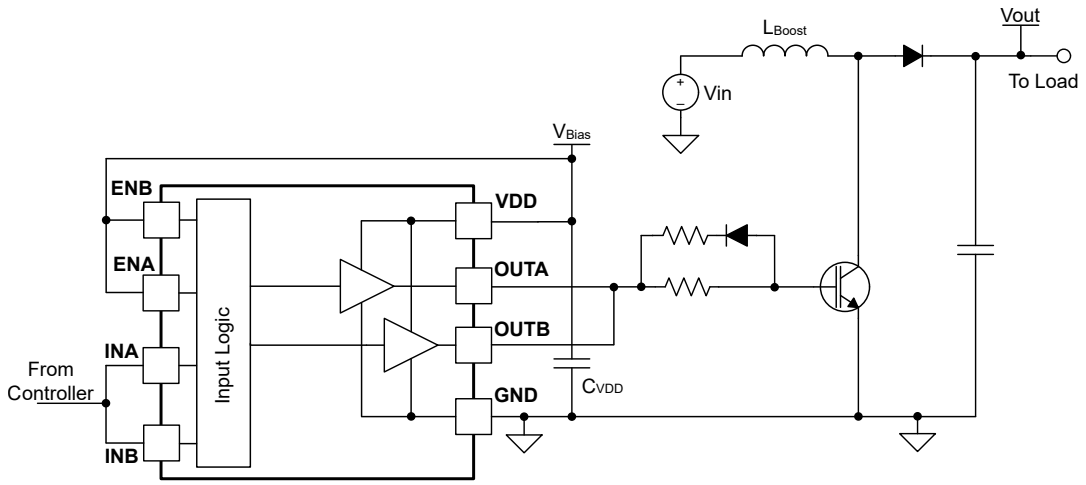
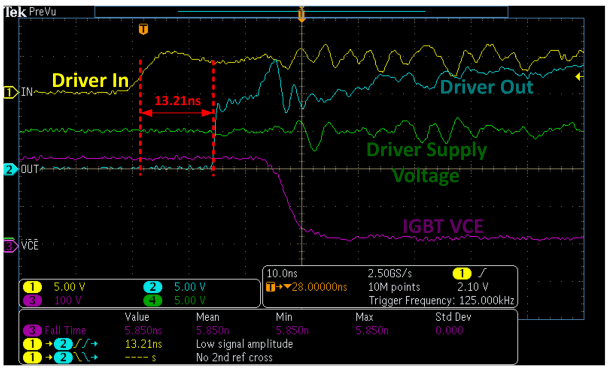
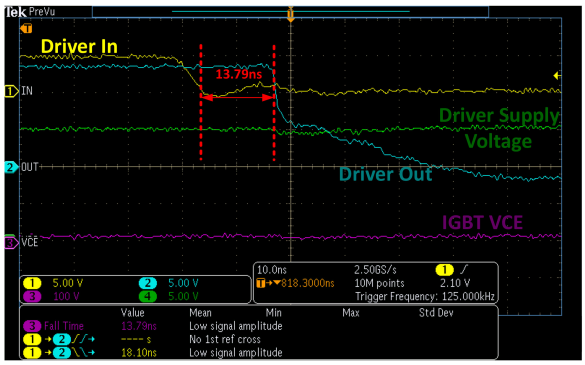


図 8-3. UCC27524 Used to Drive IGBT in the Boost Converter



Vin = 210 V, Vout = 235 V, Iout = 1.14 A, Fsw = 125 kHz, driver supply voltage = 15 V, gate resistor = 0 Ω

図 8-4. Turn-On Propagation Delay Waveform



Vin = 210 V, Vout = 235 V, Iout = 1.14 A, Fsw = 100 kHz, driver supply voltage = 15 V, gate resistor = 0 Ω

図 8-5. Turn-Off Propagation Delay Waveform

9 Power Supply Recommendations

The bias supply voltage range for which the UCC27524 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD_H. Therefore, ensuring that, while operating at or near the 4.5-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_{OFF} threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the V_{ON} threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus ensuring that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27524 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher V_{DD} voltages, the peak current capability is even higher (5-A peak current is at V_{DD} = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the V_{DD} bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from V_{DD} during turnon of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current loop paths (driver device, power MOSFET and V_{DD} bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances during turnon and turnoff transients which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- Exercise caution when replacing the UCC2732x/UCC2742x devices with the UCC27524 device:
  - The UCC27524 device is a much stronger gate driver (5-A peak current versus 4-A peak current).
  - The UCC27524 device is a much faster gate driver (17-ns/17-ns rise and fall propagation delay versus 25-ns/35-ns rise and fall propagation delay).

10.2 Layout Example

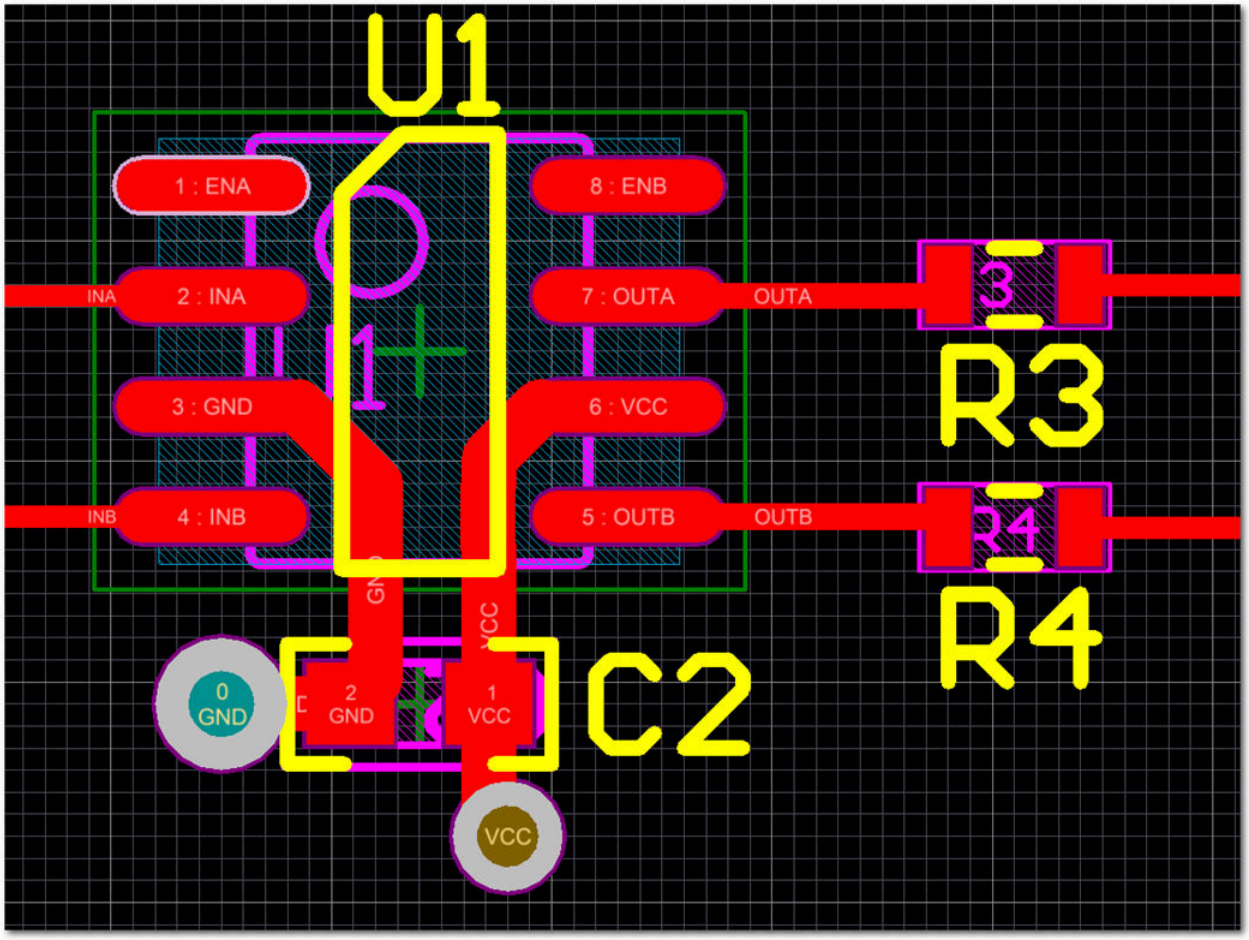


図 10-1. UCC27524 Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled, *Semiconductor and IC Package Thermal Metrics* (SPRA953).

Among the different package options available for the UCC27524 device, power dissipation capability of the DGN package is of particular mention. The HVSSOP-8 (DGN) package offers a means of removing the heat from the semiconductor junction through the bottom of the package. This package offers an exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the HVSSOP-8 package are not directly connected to any leads of the package, however, the PowerPAD is electrically and thermally connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

11 Device and Documentation Support

11.1 Device Support

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テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
June 2024	*	Initial Standalone Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27524D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524
UCC27524DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	27524
UCC27524DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	27524
UCC27524DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	27524
UCC27524DSDR	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	SBA
UCC27524DSDR.A	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	SBA
UCC27524DSDT	Active	Production	SON (DSD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	SBA
UCC27524DSDT.A	Active	Production	SON (DSD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	SBA
UCC27524DSDTG4	Active	Production	SON (DSD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	SBA
UCC27524DSDTG4.A	Active	Production	SON (DSD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	SBA
UCC27524P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 140	27524
UCC27524P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 140	27524

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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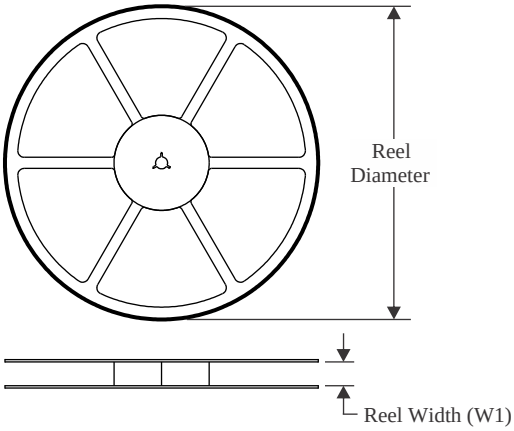
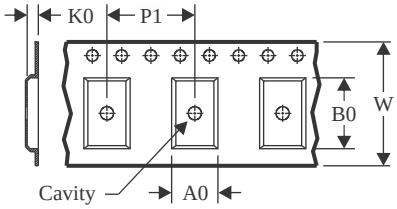
TAPE AND REEL INFORMATION

REEL DIMENSIONS

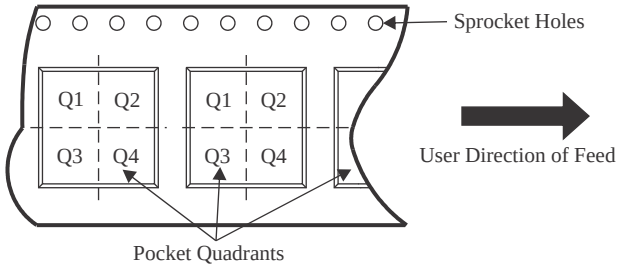


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

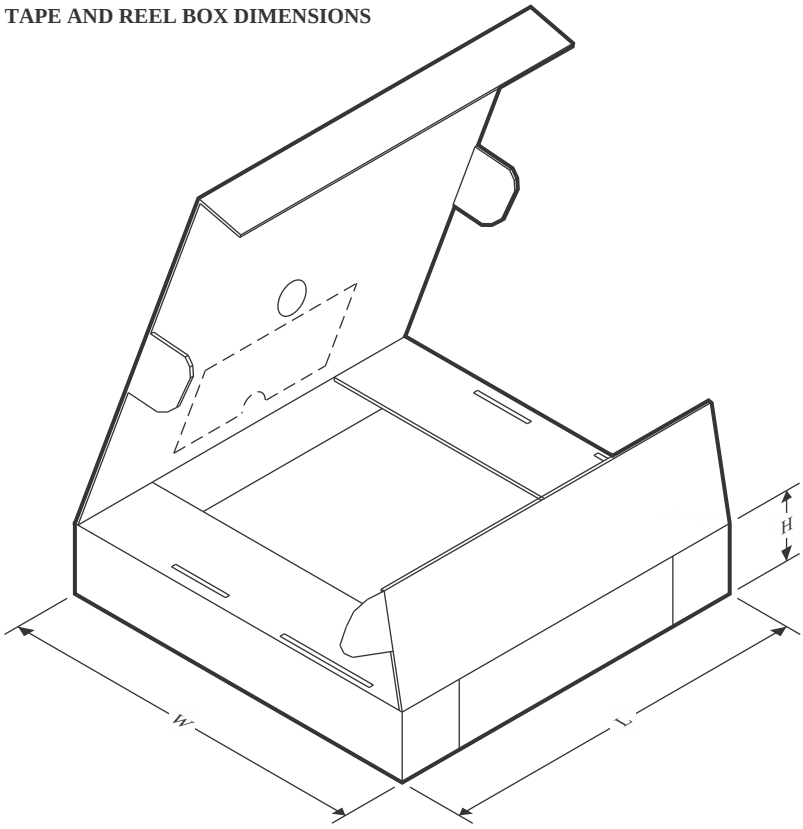
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27524DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27524DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27524DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27524DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27524DSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27524DSDT	SON	DSD	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27524DSDTG4	SON	DSD	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

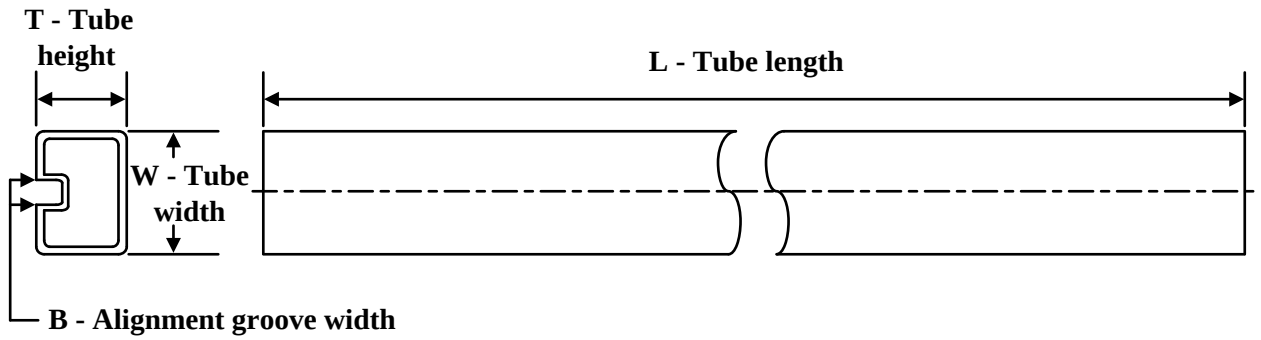
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27524DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27524DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27524DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27524DRG4	SOIC	D	8	2500	353.0	353.0	32.0
UCC27524DSDR	SON	DSD	8	3000	346.0	346.0	33.0
UCC27524DSDT	SON	DSD	8	250	210.0	185.0	35.0
UCC27524DSDTG4	SON	DSD	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27524D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27524D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC27524D.B	D	SOIC	8	75	506.6	8	3940	4.32
UCC27524DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27524DGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27524DGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27524P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27524P.B	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

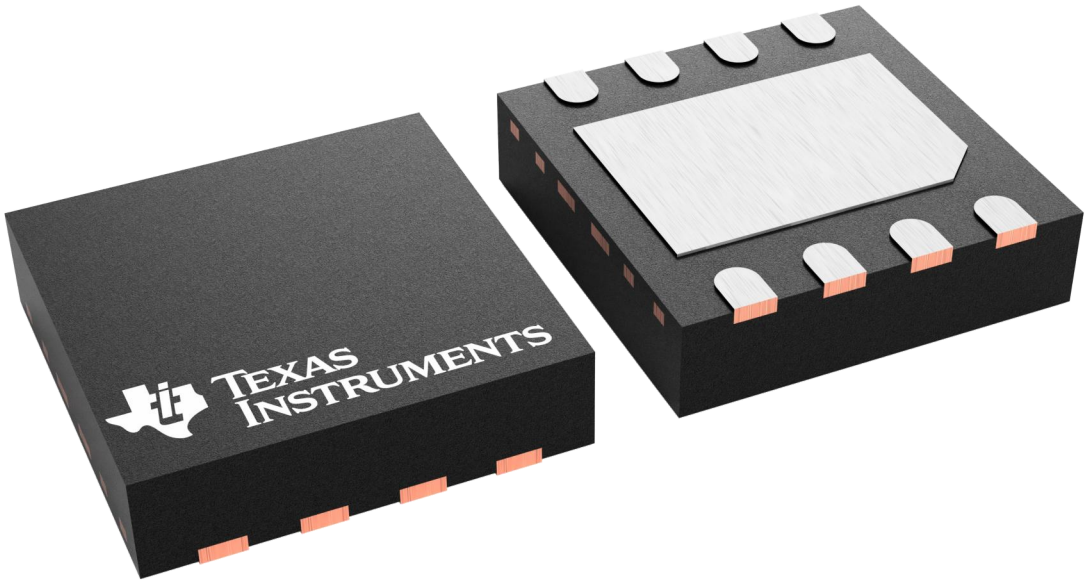
DSD 8

WSON - 0.8 mm max height

3 X 3, 0.8 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



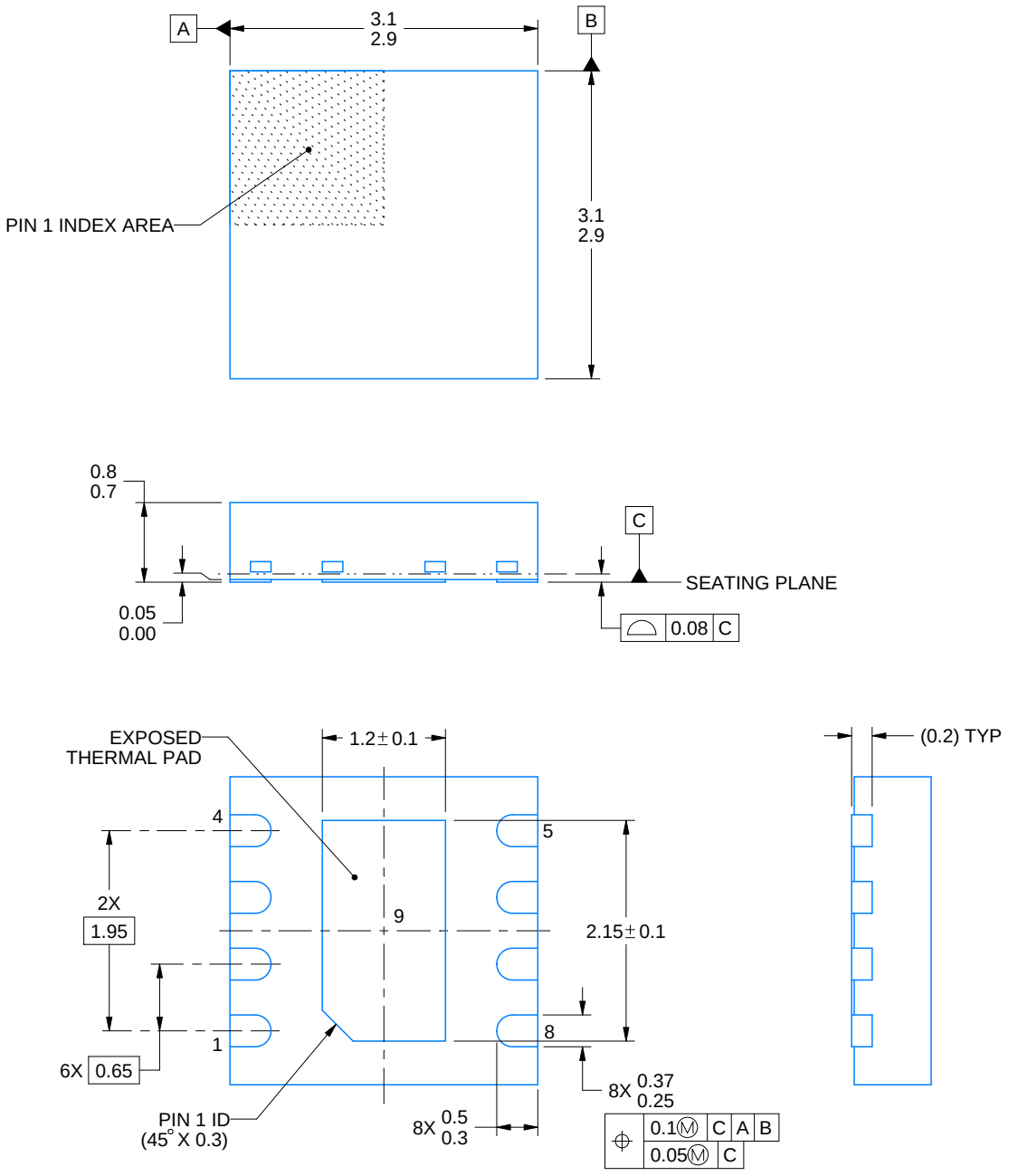
4227007/A

PACKAGE OUTLINE

DSD0008D

WSON - 0.8 mm max height

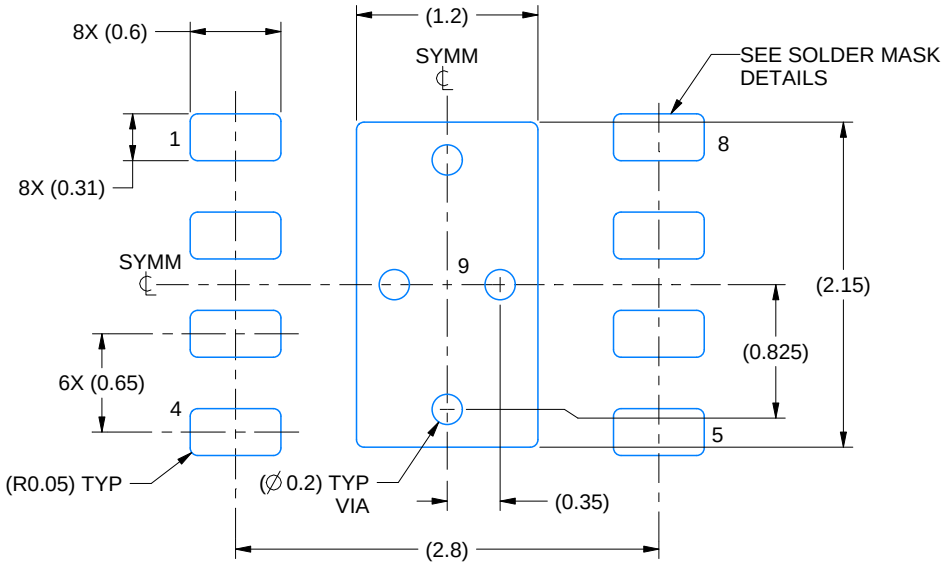
PLASTIC SMALL OUTLINE - NO LEAD



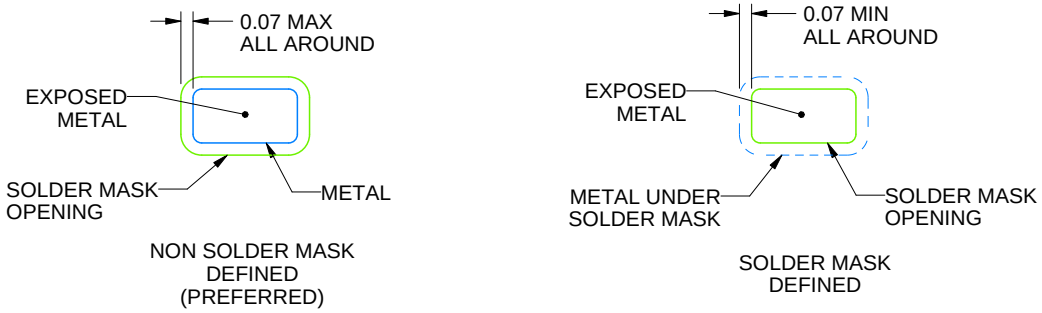
4218899/A 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

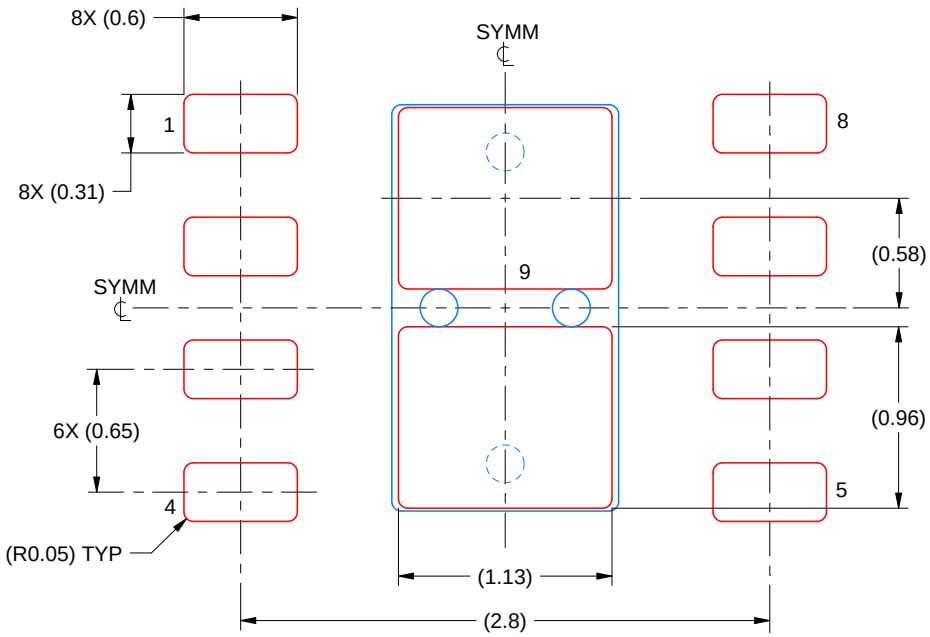


SOLDER MASK DETAILS

4218899/A 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218899/A 09/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

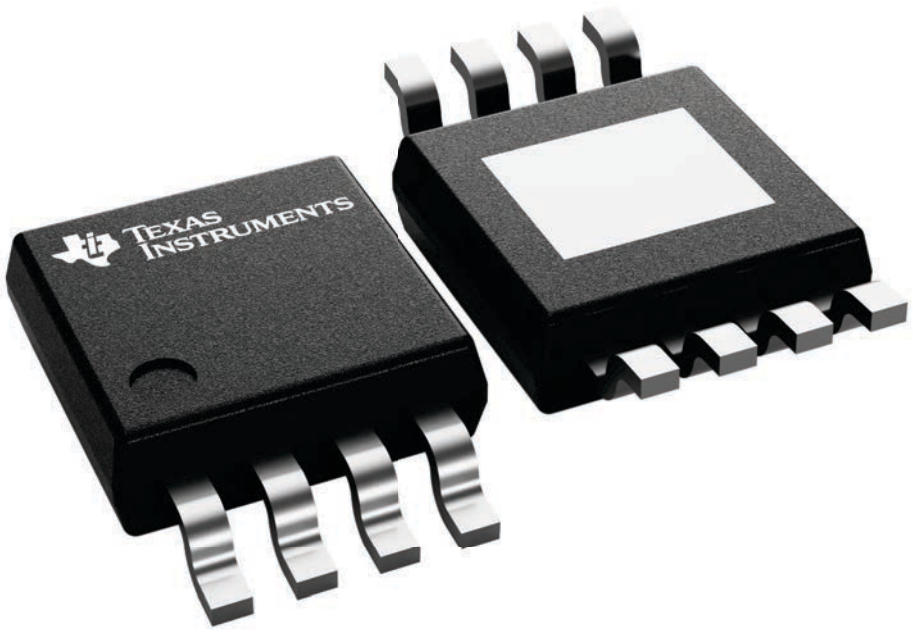
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



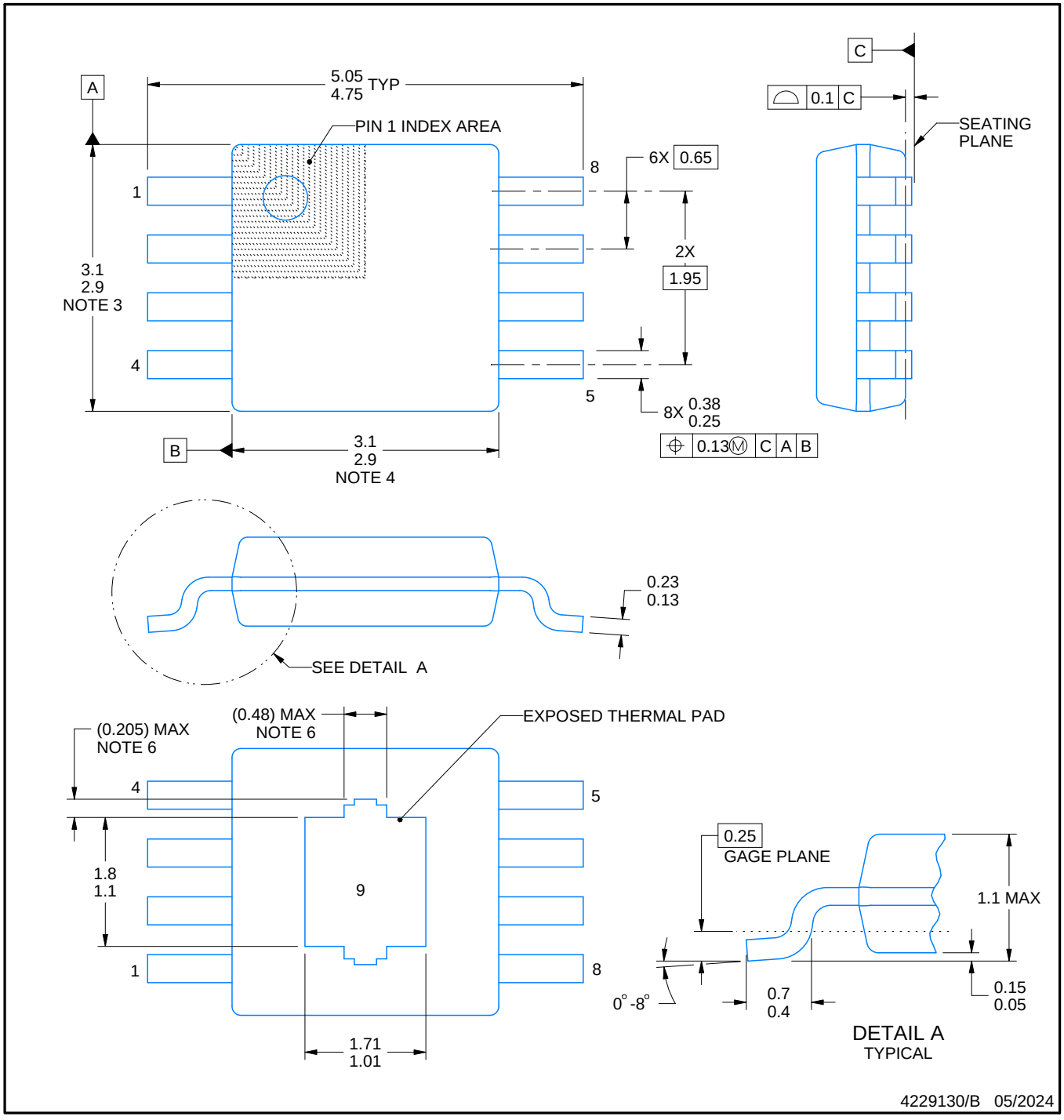
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

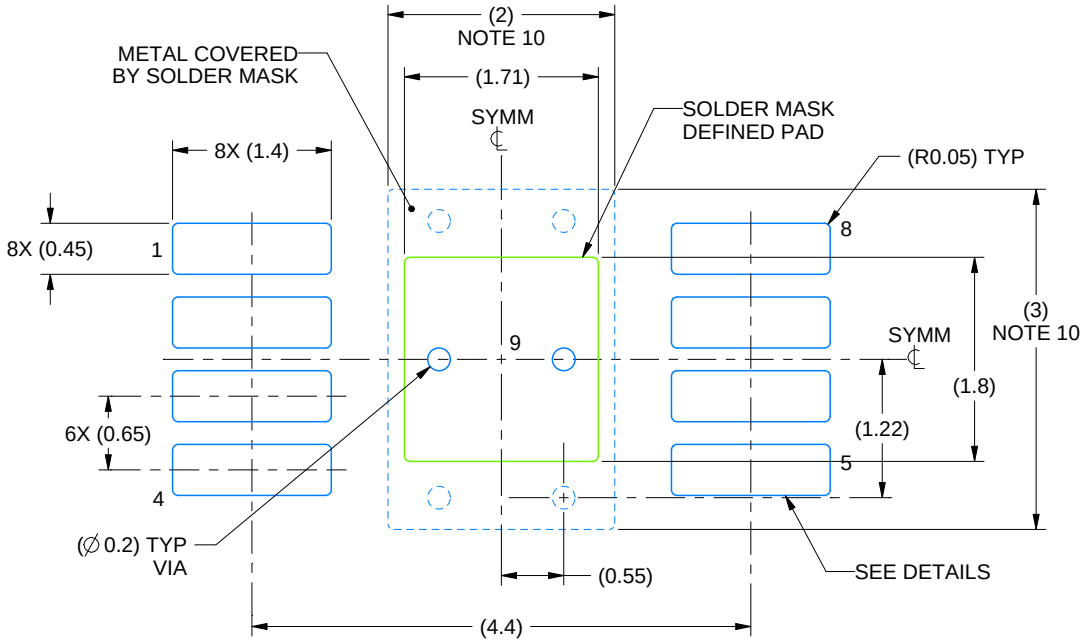
SMALL OUTLINE PACKAGE



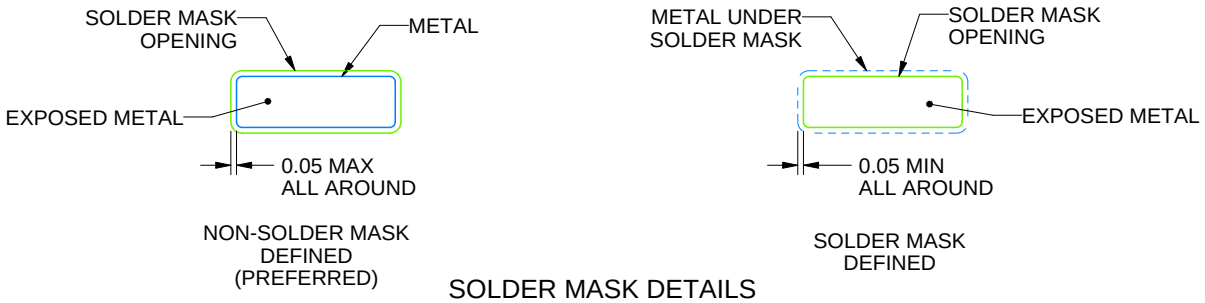
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

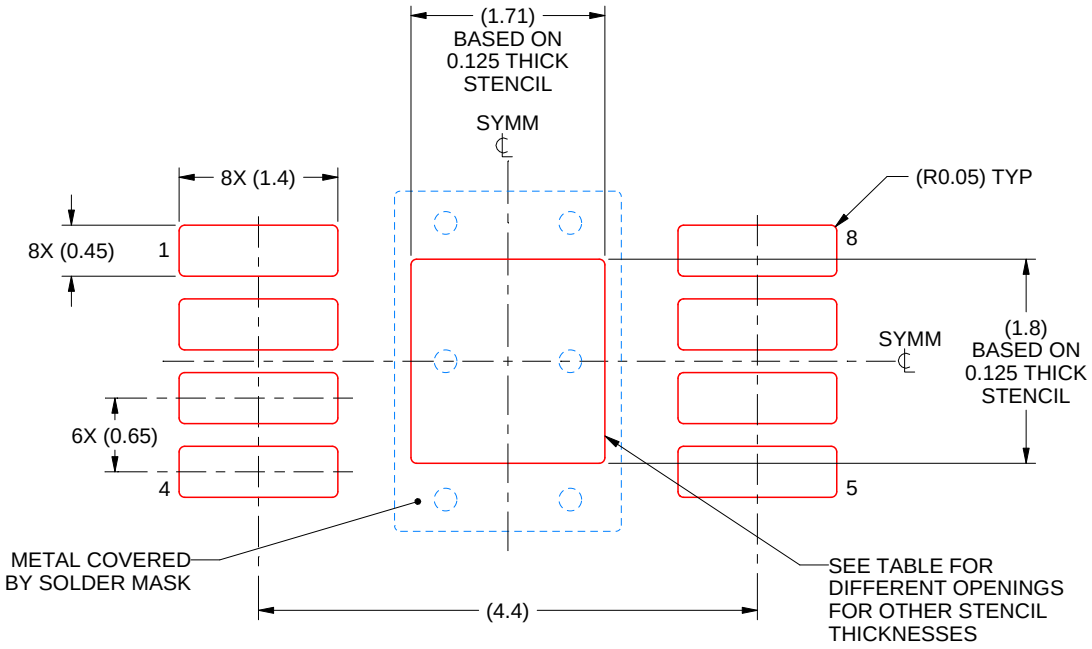


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

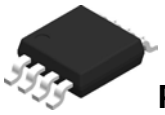
4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

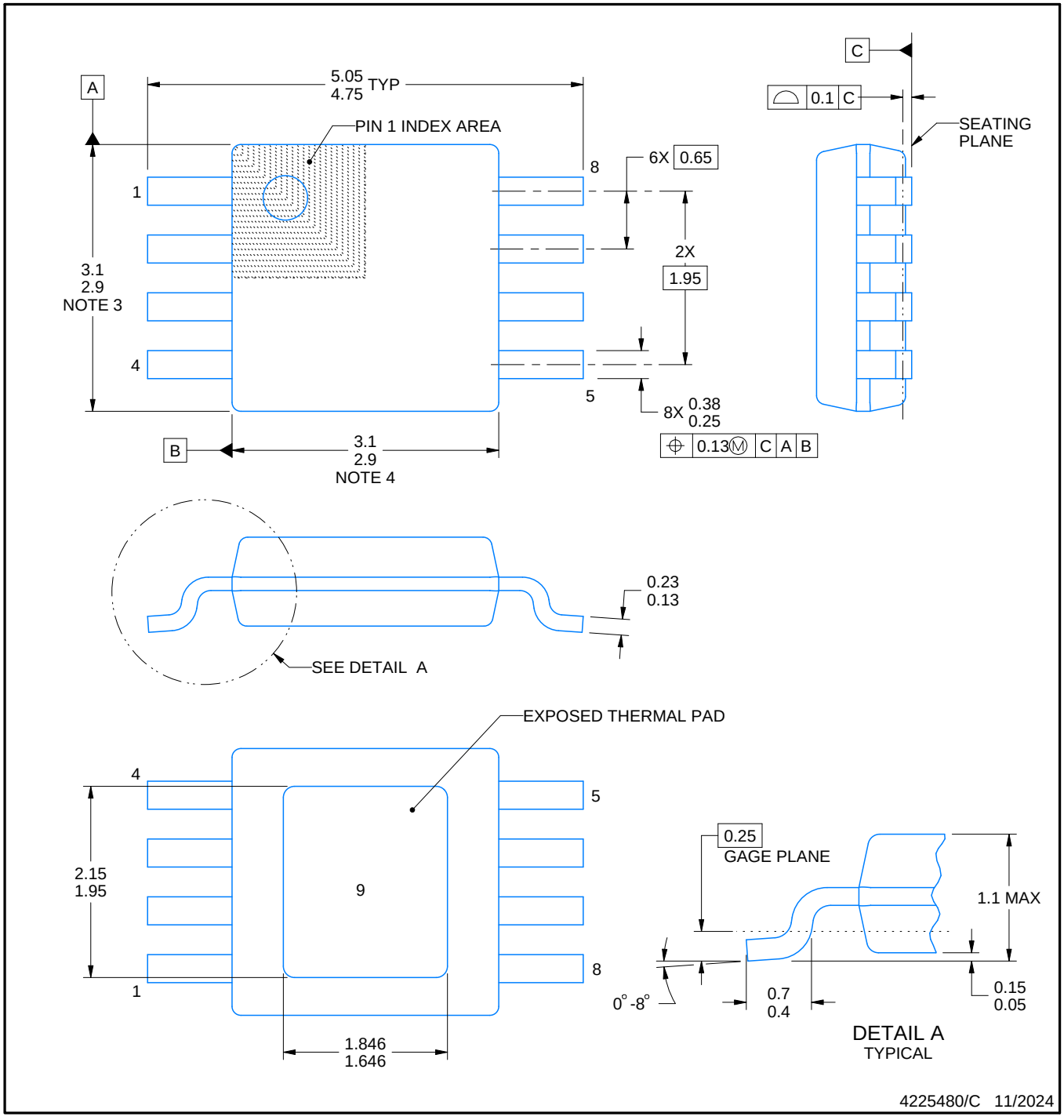
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

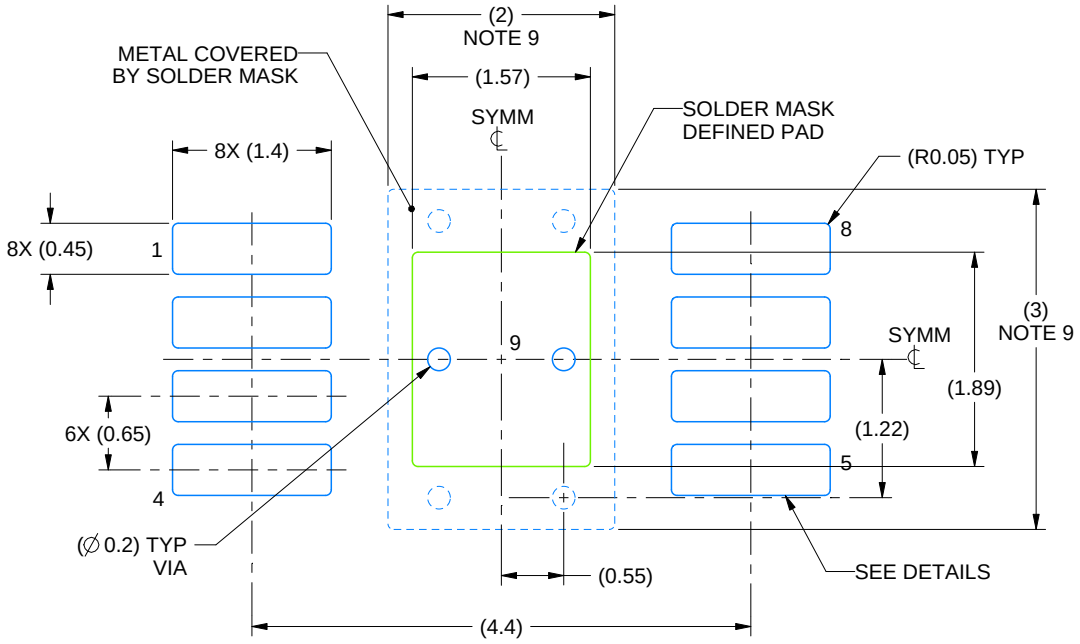
SMALL OUTLINE PACKAGE



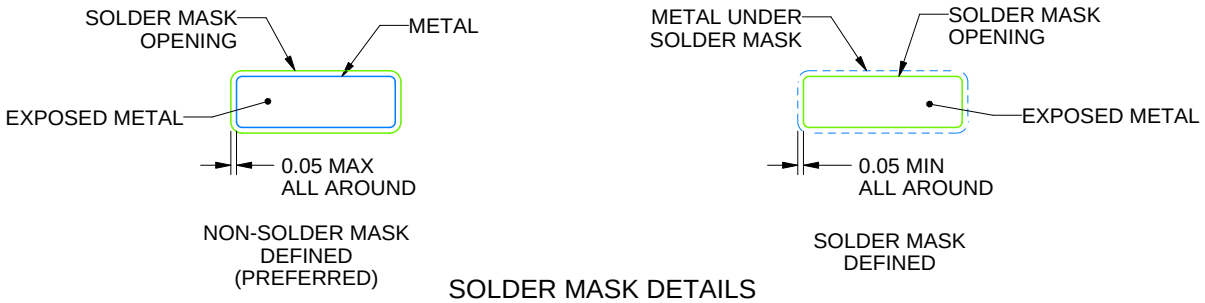
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

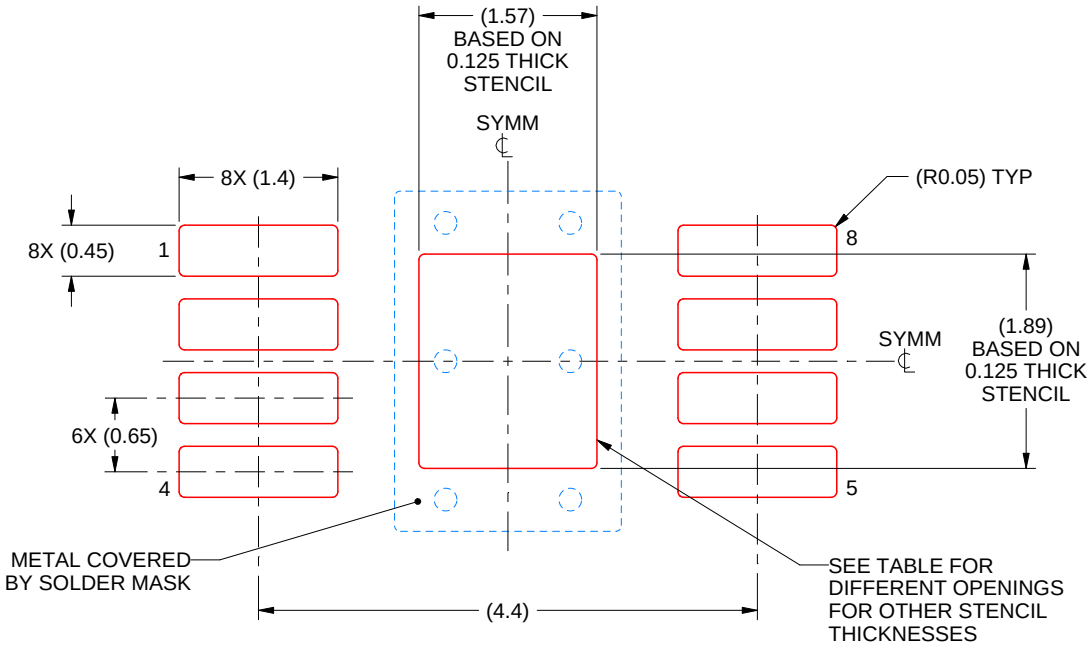


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



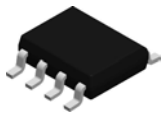
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

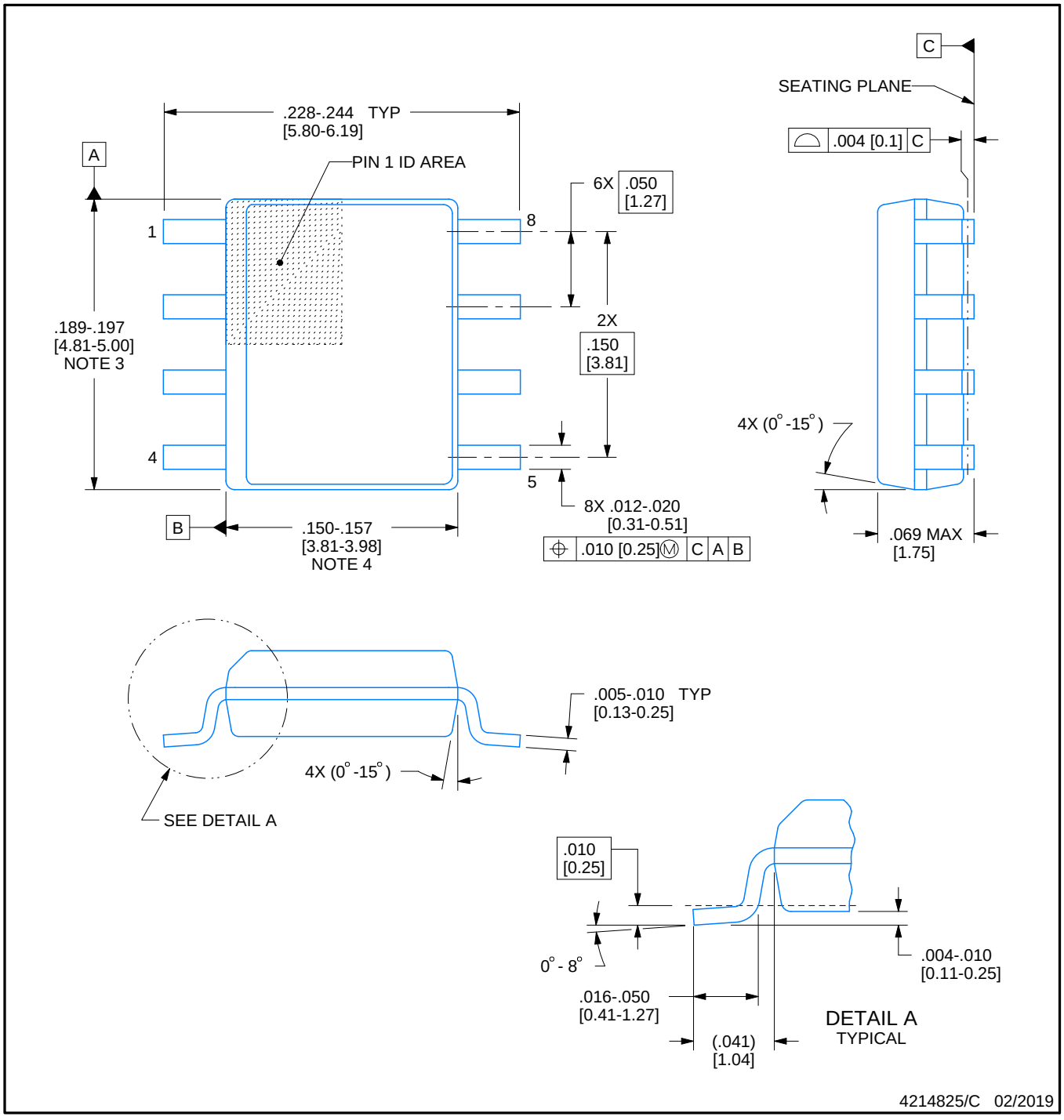


PACKAGE OUTLINE

D0008A

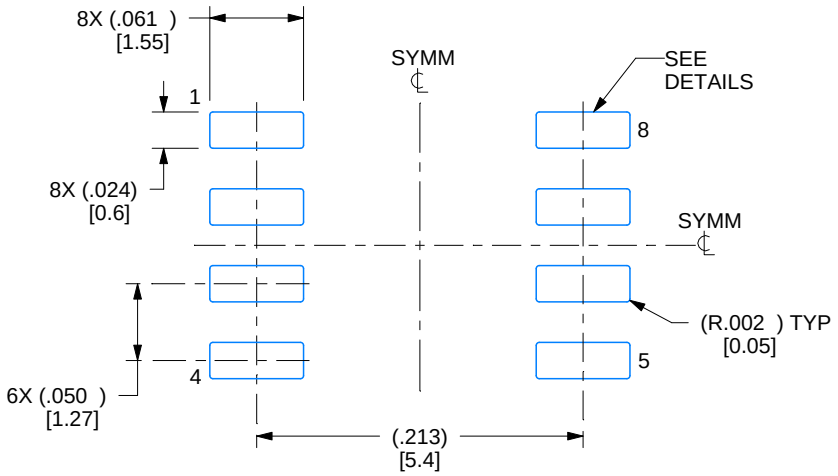
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

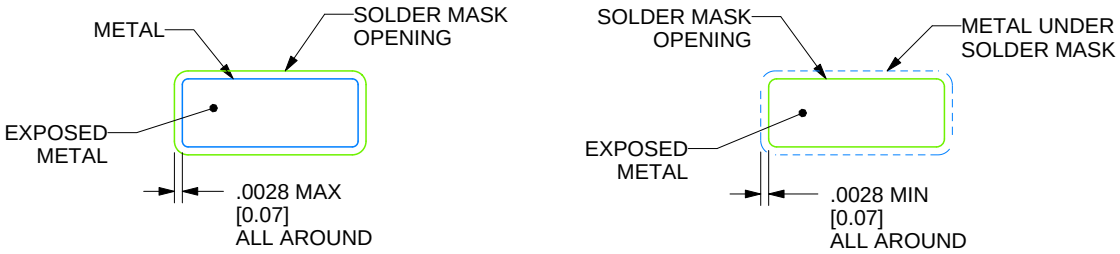


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

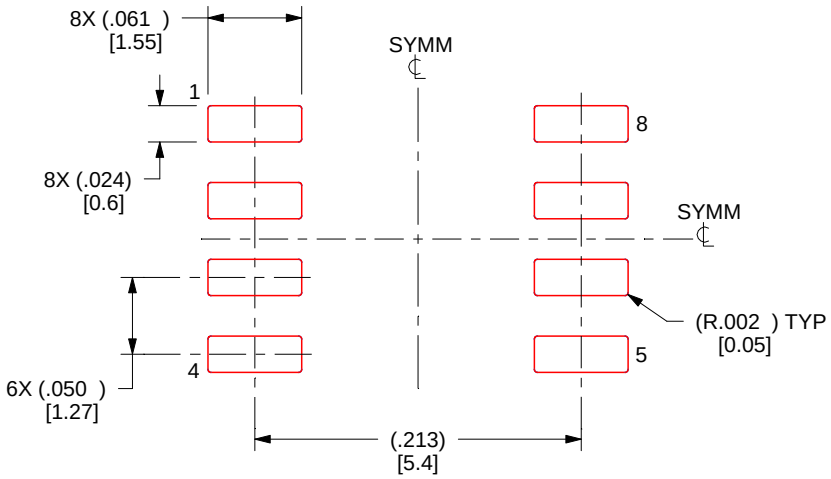
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



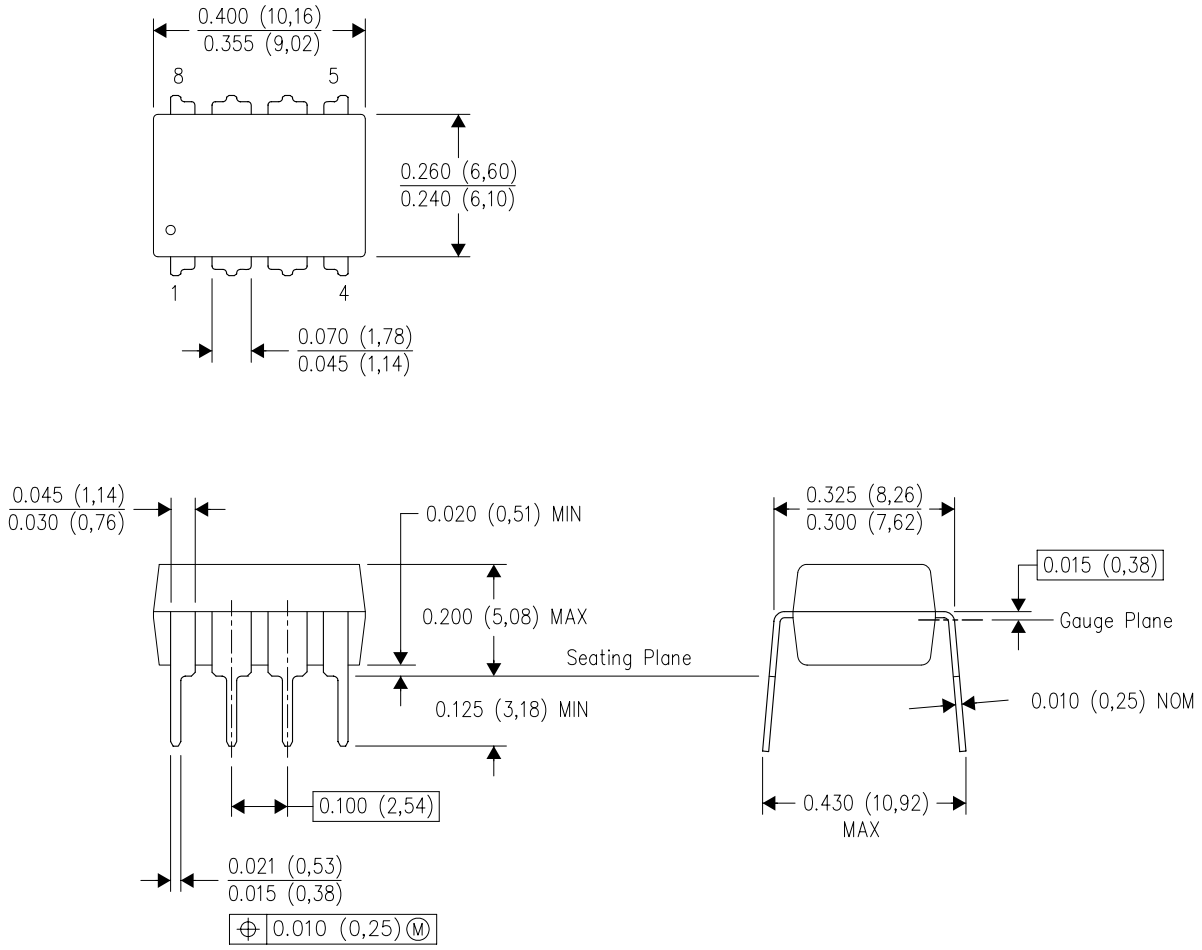
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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最終更新日：2025 年 10 月