Negative Output Flyback Pulse Width Modulator

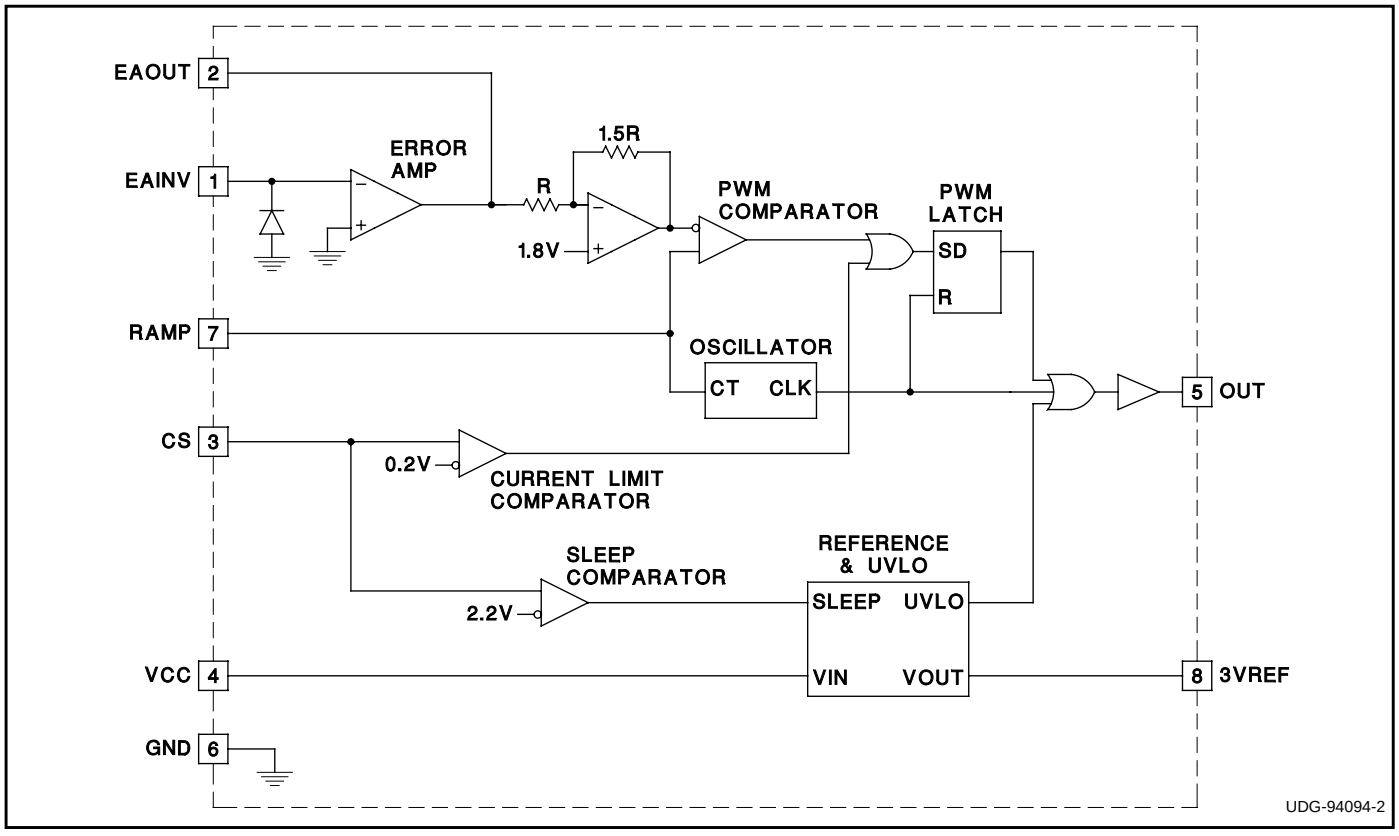
FEATURES

- Simple Single Inductor Flyback PWM for Negative Voltage Generation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50µA Sleep Mode Current

DESCRIPTION

The UC3572 is a negative output flyback pulse width modulator which converts a positive input voltage to a regulated negative output voltage. The chip is optimized for use in a single inductor negative flyback switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3572 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Output current can be sensed and limited to a user determined maximum value. The UVLO circuit turns the chip off when the input voltage is below the UVLO threshold. In addition, a sleep comparator interfaces to the UVLO circuit to turn the chip off. This reduces the supply current to only 50µA, making the UC3572 ideal for battery powered applications.

BLOCK DIAGRAM



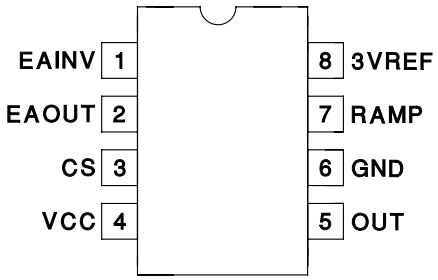
ABSOLUTE MAXIMUM RATINGS

VCC 35V
EAINV . . . . . -0.6V to VCC
I_{EAOUT} 25mA
RAMP . . . . . -0.3V to 4V
CS . . . . . -0.3V to VCC
Iout . . . . . -0.7A to 0.7A
I_{3VREF} . . . . . -15mA
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (TOP VIEW)
D, N or J Packages



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1572	–55°C to +125°C	J
UC2572	–40°C to +85°C	D, N or J
UC3572	0°C to +70°C	D or N

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I_{3VREF} = 0V to –5mA		1	10	mV
Oscillator Section					
Frequency	VCC = 5V to 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	–10	0	10	mV
	I_{EANV} = –1mA		–0.2	–0.9	V
I_{EAINV}	EAOUT = 2V		–0.2	–1.0	µA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = –100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
I_{EAOUT}	EAINV = –100mV, EAOUT = 2V	–350	–500		µA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T_J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold		0.185	0.205	0.225	V
Input Bias Current	CS = 0		–0.4	–1	µA
CS Propogation Delay			300		nS

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output Section					
OUT High Saturation	I_{OUT} = 0		0	0.3	V
	I_{OUT} = –10mA		0.7	1.5	V
	I_{OUT} = –100mA		1.5	2.5	V
OUT Low Saturation	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Fall Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = –100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
IVCC	VCC = 5V, 30V		9	15	mA
	VCC = 30, CS = 3V		50	150	µA

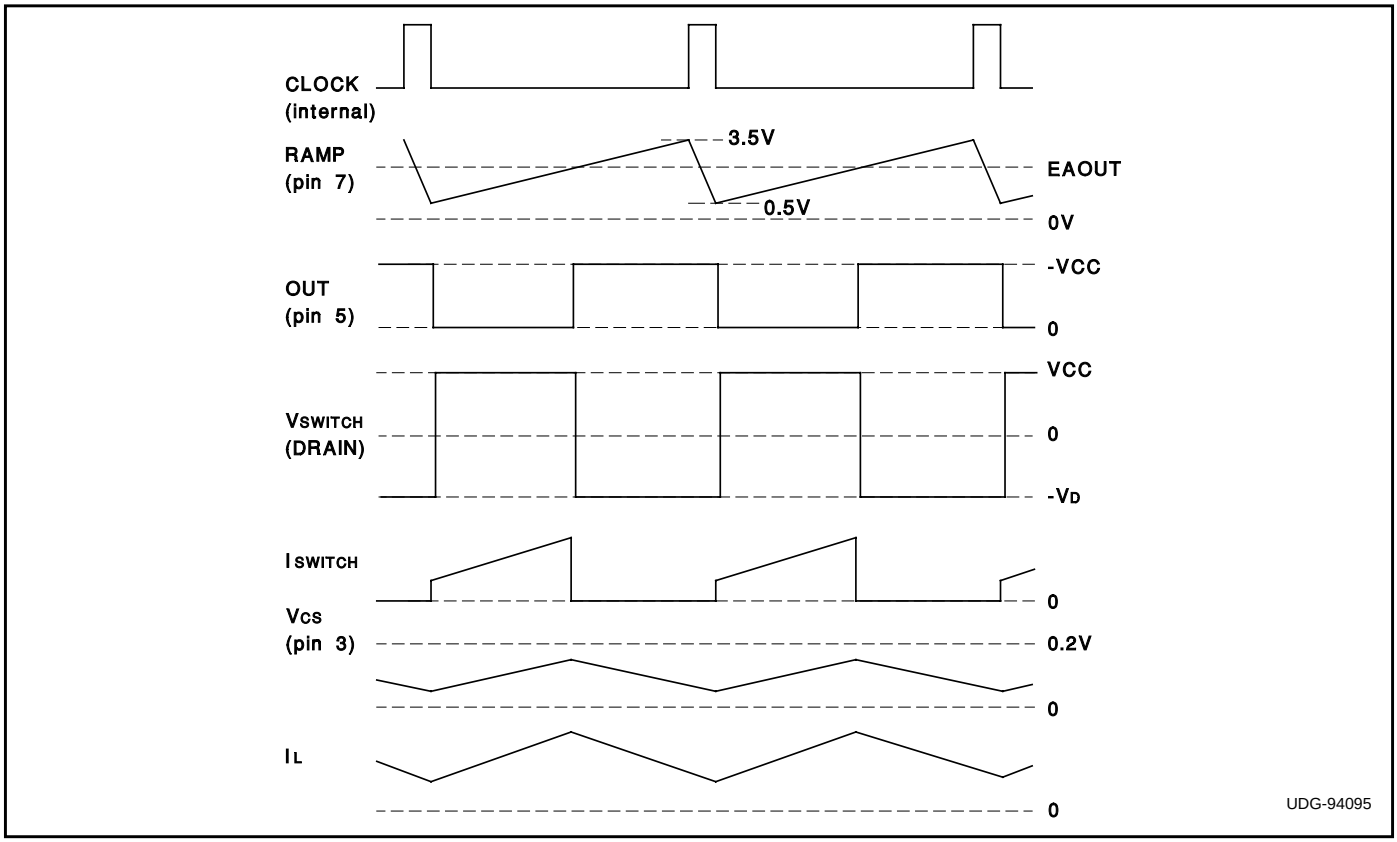


Figure 1. Typical waveforms.

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor to GND.

CS: Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

EAINV: Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND. This pin will source a maximum of 1mA.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

OUT: Gate drive for external PMOS switch connected between V_{CC} and the flyback inductor. OUT drives the gate of the PMOS switch between V_{CC} and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \bullet C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1µF capacitor.

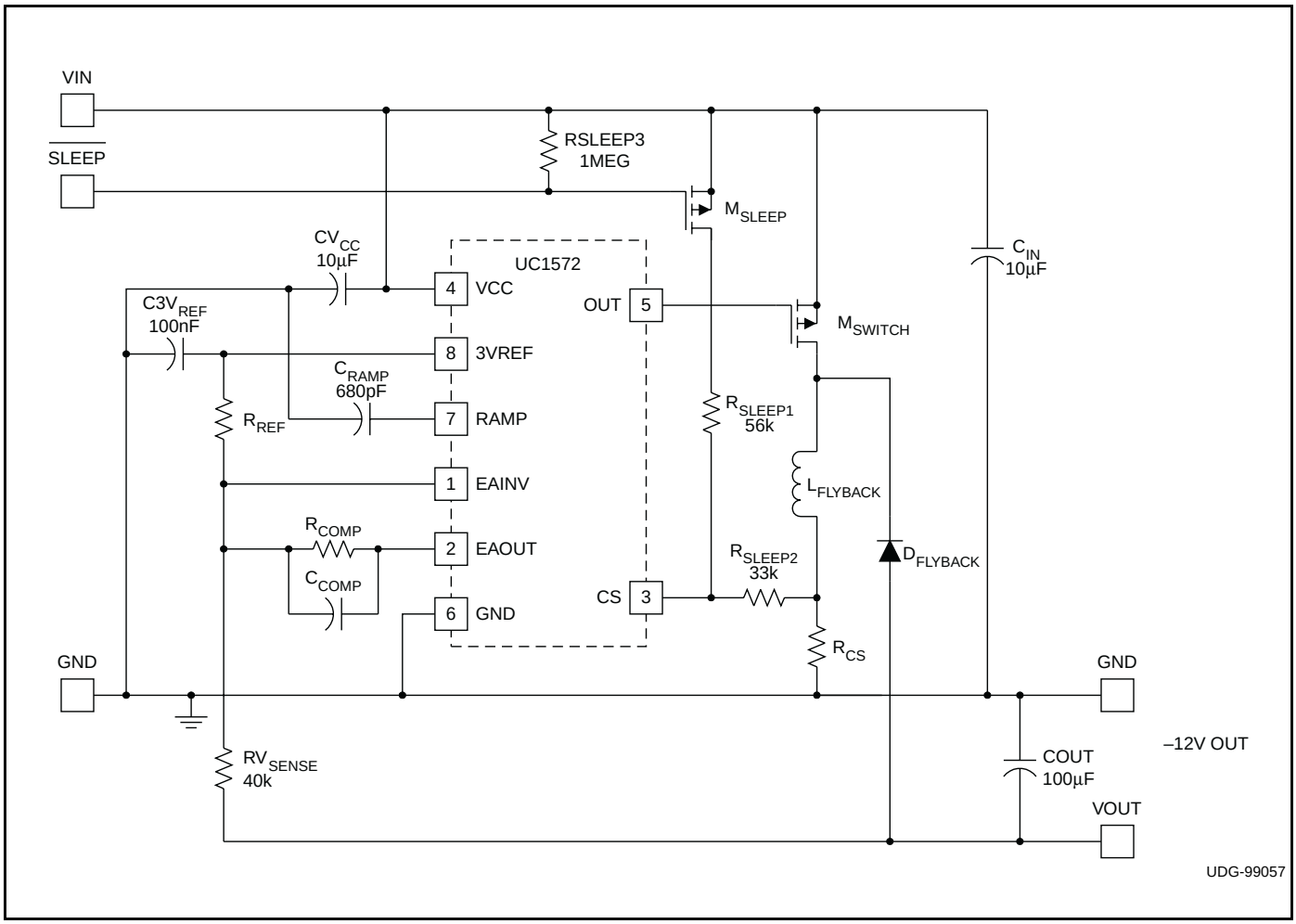


Figure 2. Typical application: +5V to –12V flyback converter.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2572D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D
UC2572D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D
UC2572DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D
UC2572DTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D
UC2572DTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D
UC3572D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D
UC3572D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D
UC3572DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D
UC3572DTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D
UC3572DTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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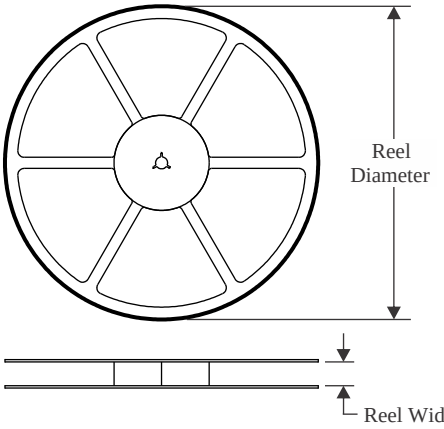
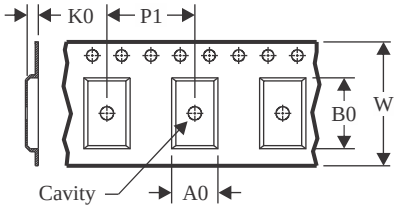
TAPE AND REEL INFORMATION

REEL DIMENSIONS

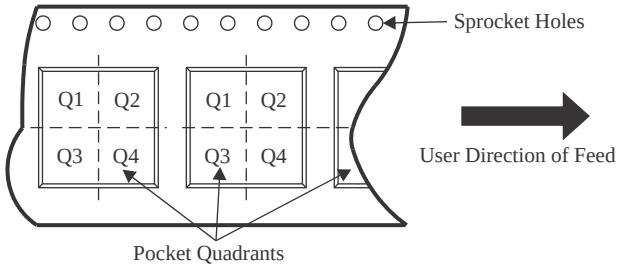


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

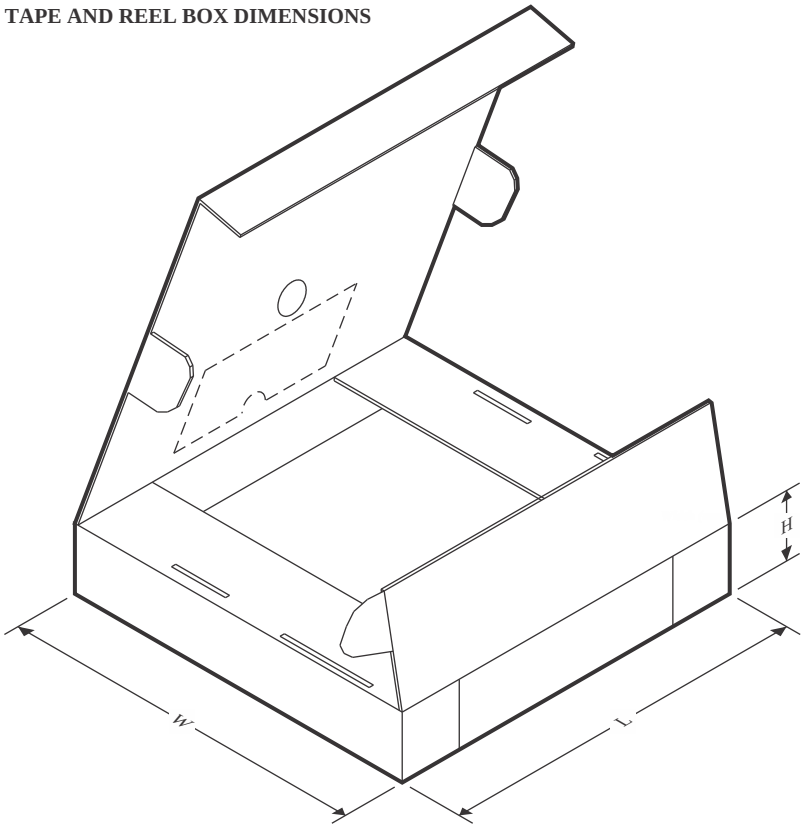
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

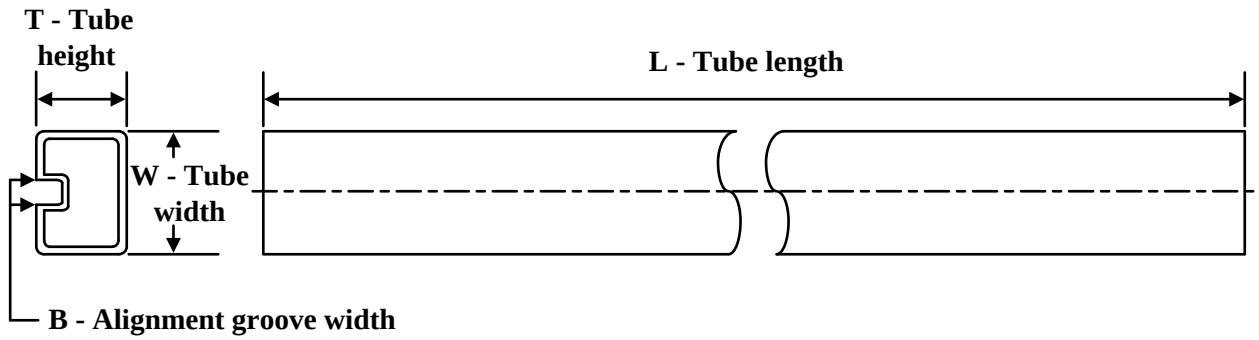
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2572DTR	SOIC	D	8	2500	353.0	353.0	32.0
UC3572DTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2572D	D	SOIC	8	75	507	8	3940	4.32
UC2572D.A	D	SOIC	8	75	507	8	3940	4.32
UC2572DG4	D	SOIC	8	75	507	8	3940	4.32
UC3572D	D	SOIC	8	75	507	8	3940	4.32
UC3572D.A	D	SOIC	8	75	507	8	3940	4.32
UC3572DG4	D	SOIC	8	75	507	8	3940	4.32

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