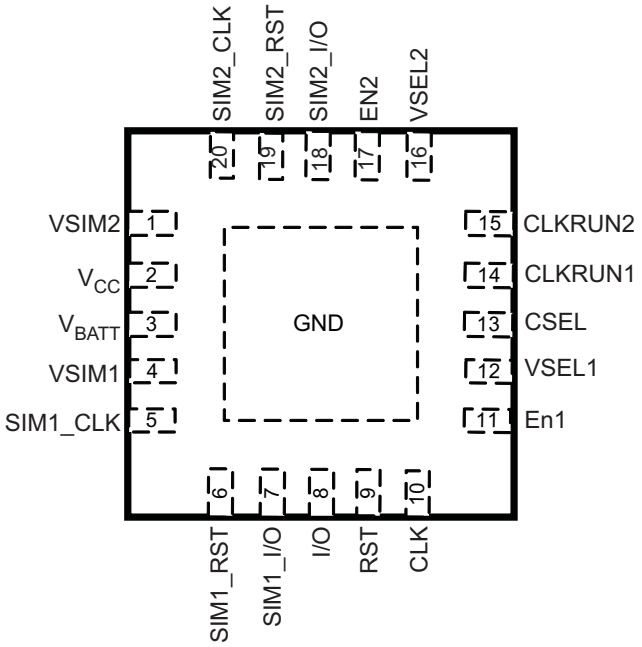
Dual-SIM Card Power Supply with Level Translator and Dedicated Dual LDO

Check for Samples: TXS4558

FEATURES

- **Level Translator**
  - **V_{CC} Range of 1.65 V to 3.3 V**
  - **V_{BATT} Range of 2.3V to 5.5V**
- **Low-Dropout (LDO) Regulator**
  - **50-mA LDO Regulator With Enable**
  - **1.8-V or 2.95-V Selectable Output Voltage**
  - **Very Low Dropout: 100 mV (Max) at 50 mA**
- **Control and Communication Through GPIO Interface with Baseband Processor**
- **Isolated Clock Stop Mode for both SIM1 and SIM2 cards**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **500-V Charged-Device Model (C101)**
  - **8kV HBM for SIM pins**
- **Package**
  - **20-Pin QFN (3 mm x 3 mm)**

RUK PACKAGE
(TOP VIEW)



NOTE: Exposed center thermal pad must be electrically connected to Ground.

DESCRIPTION

The TXS4558 is a complete dual-supply standby Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with two individual SIM subscriber cards to store data for mobile handset applications. It is a custom device which is used to extend a single SIM/UICC interface to be able to support two SIM's/UICC's.

The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. It includes a high-speed level translator capable of supporting Class-B (2.95 V) and Class-C (1.8 V) interfaces, two low-dropout (LDO) voltage regulators that have output voltages that are selectable between 2.95-V Class-B and 1.8-V Class-C interfaces. Simple GPIO inputs are used to switch between the two SIM cards and to put it into different modes. The voltage-level translator has two supply voltage pins. VCC sets the reference for the baseband interface and can be operated from 1.65 V to 3.3 V. VSIM1 and VSIM2 are programmed to either 1.8 V or 2.95 V, each supplied by an independent internal LDO regulator. The integrated LDO accepts input battery voltages from 2.3 V to 5.5 V and outputs up to 50 mA to the B-side circuitry and external Class-B or Class-C SIM card.

The TXS4558 also incorporates shutdown sequence for the SIM card pins based on the ISO 7816-3 specification for SIM cards. The device also has 8kV HBM protection for the SIM card pins and standard 2kV HBM protection for all the other pins.

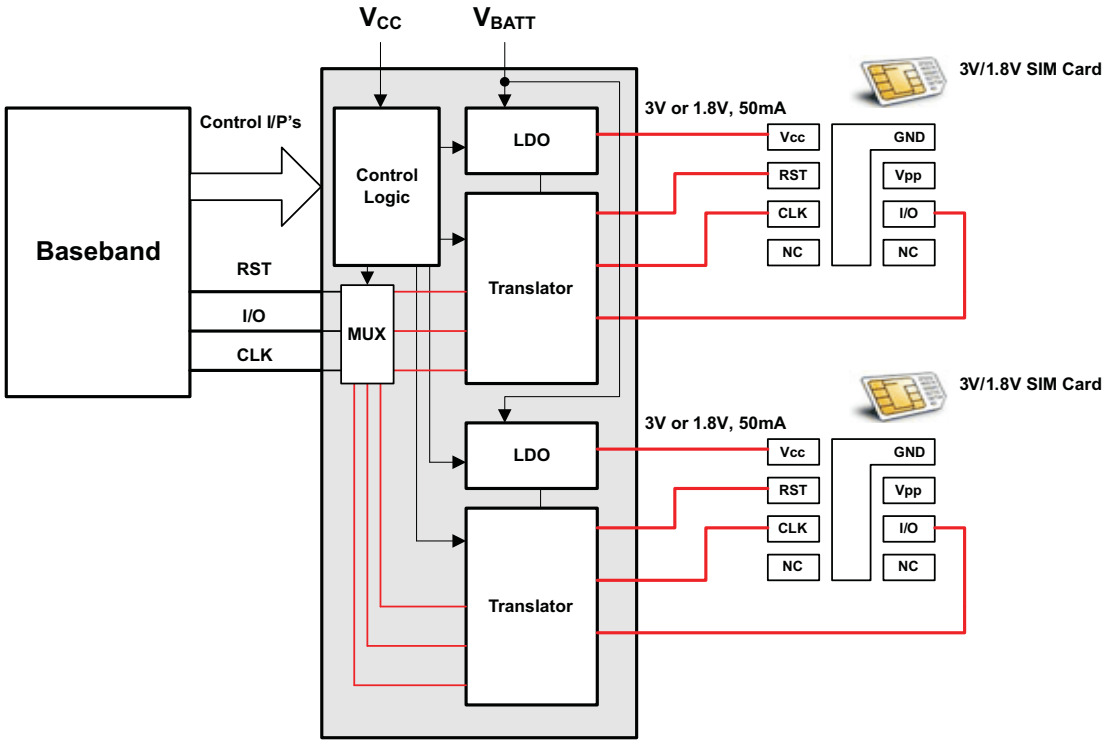
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUK	Tape and reel	TXS4558RUKR	ZTG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

INTERFACING THE SIM CARD



PIN FUNCTIONS(1)

NO.	NAME	TYPE(2)	POWER DOMAIN	DESCRIPTION
1	VSIM2	O	V_{BATT}	1.8 V/2.95 V supply voltage to SIM2
2	V_{CC}	P	—	1.8-V power supply for device operation and I/O buffers toward baseband
3	V_{BATT}	P	—	Battery power supply
4	VSIM1	O	VBATT	1.8 V/2.95 V supply voltage to SIM1
5	SIM1CLK	O	VSIM1	SIM1 clock
6	SIM1RST	O	VSIM1	SIM1 reset
7	SIM1I/O	I/O	VSIM1	SIM1 data
8	I/O	I/O	V_{CC}	UICC/SIM data
9	RST	I	V_{CC}	UICC/SIM reset from baseband
10	CLK	I	V_{CC}	UICC/SIM clock
11	EN1	I	V_{CC}	Enable pin for SIM1 interface
12	VSEL1	I	V_{CC}	Select pin for 1.8V or 2.95V LDO1 output
13	CSEL	I	V_{CC}	Channel select between SIM1 or SIM2

(1) Thermal Pad must be electrically connected to Ground Plane.
(2) G = Ground, I = Input, O = Output, P = Power

PIN FUNCTIONS[1] (continued)

NO.	NAME	TYPE[2]	POWER DOMAIN	DESCRIPTION
14	CLKRUN1	I	V_{CC}	Select pin for SIM1 Clock stop mode
15	CLKRUN2	I	V_{CC}	Select pin for SIM2 Clock stop mode
16	VSEL2	I	V_{CC}	Select pin for 1.8V or 2.95V LDO2 output
17	EN2	I	V_{CC}	Enable pin for SIM2 interface
18	SIM2I/O	I/O	VSIM2	SIM2 data
19	SIM2RST	O	VSIM2	SIM2 reset
20	SIM2CLK	O	VSIM2	SIM2 clock

TRUTH TABLE

CSEL	VSEL1	VSEL2	SELECTED CARD	VSIM1	VSIM2
0	0	0	1	1.8 V	1.8 V
0	0	1	1	1.8 V	2.95 V
0	1	0	1	2.95 V	1.8 V
0	1	1	1	2.95 V	2.95 V
1	0	0	2	1.8 V	1.8 V
1	0	1	2	1.8 V	2.95 V
1	1	0	2	2.95 V	1.8 V
1	1	1	2	2.95 V	2.95 V

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
VCC	Supply voltage range		–0.3	4.0	V
V_I	Input voltage range	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current		±50		mA
	Continuous current through VCCA or GND		±100		mA
T_{stg}	Storage temperature range		–65	150	°C
LDO					
V_{BAT}	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range		–0.3	6	V
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C
	ESD rating (host side)	Human-Body Model (HBM)		2	kV
		Charged-Device Model (CDM)		500	V

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
VCC	Supply voltage		1.7	3.3	V
V_{IH}	High-level input voltage	Applies to pins: EN1, EN2,RST, CLK, I/O, CLKRUN1, CLKRUN2, VSEL1, VSEL2, CSEL	VCC × 0.7	3.3	V
V_{IL}	Low-level input voltage		0	VCC × 0.3	V
Δt/Δv	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS — LEVEL TRANSLATOR

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	VSIM1	VSIM2	MIN	TYP(1)	MAX	UNIT
V_{OH}	SIM1_RST	I_{OH} = –100 µA, Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V, (Supplied by LDO)	1.8 V / 2.95 V, (Supplied by LDO)	VSIM1 × 0.8			V
	SIM1_CLK					VSIM1 × 0.8			
	SIM1_I/O	I_{OH} = –10 µA, Open-Drain				VSIM1 × 0.8			
	SIM2_RST	I_{OH} = –100 µA, Push-Pull				VSIM2 × 0.8			
	SIM2_CLK					VSIM2 × 0.8			
	SIM2_I/O	I_{OH} = –10 µA, Open-Drain				VSIM2 × 0.8			
	I/O	I_{OH} = –10 µA, Open-Drain				VCC × 0.8			
V_{OL}	SIM1_RST	I_{OL} = 1 mA, Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			VSIM1 × 0.2	V
	SIM1_CLK							VSIM1 × 0.2	
	SIM1_I/O	I_{OL} = 1 mA, Open-Drain						0.3	
	SIM2_RST	I_{OL} = 1 mA, Push-Pull						VSIM2 × 0.2	
	SIM2_CLK							VSIM2 × 0.2	
	SIM2_I/O	I_{OL} = 1 mA, Open-Drain						0.3	
	I/O	I_{OL} = 1 mA, Open-Drain						0.3	
I_I	Control inputs	V_I = EN1,EN2, CLKRUN1, CSEL, CLKRUN2, VSEL1, VSEL2,	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±1	µA
$I_{CC\ I/O}$		V_I = V_{CCI}, I_O = 0	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±5	µA
C_{io}	SIM_I/O port						8		pF
	VSIMx port						8		
C_i	Control inputs	V_I = VCC or GND					4		pF

(1) All typical values are at T_A = 25°C.

LDO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
VBAT	Input voltage			2.3		5.5	V
$V_{SIM1,2}$	Output voltage	Class-B Mode , 0 mA < $I_{SIM1,2}$ < 50 mA		2.85	2.95	3.05	V
		Class-C Mode , 0 mA < $I_{SIM1,2}$ < 50 mA		1.7	1.8	1.9	
V_{DO}	Dropout voltage	I_{OUT} = 50 mA				100	mV
I_{VBAT}	Operating current	V_{SIM1} = 2.95 V, V_{SIM2} = 0, ISIM1 = 0 µA			40	50	µA
		V_{SIM1} = 1.8 V, V_{SIM2} = 0, I_{SIM1} = 0 µA			40	50	
I_{SHDN}	Shutdown current (IGND)	V_{ENx} ≤ 0.4 V, (VSIMx + V_{DO}) ≤ VBAT ≤ 5.5 V, T_J = 85°C				1	µA
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 Ω			145		mA
C_{OUT}	Output Capacitor				1		µF
PSRR	Power-supply rejection ratio	V_{BAT} = 3.15 V, $V_{SIM1,2}$ = 1.8 V or 2.95 V, C_{OUT} = 1 µF, I_{OUT} = 10 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T_{STR}	$V_{SIM1,2}$ Start-up time	$V_{SIM1,2}$ = 1.8 V or 3 V, I_{OUT} = 50 mA, C_{OUT} = 1 µF				400	µS
T_J	Operating junction temperature			–40		125	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{I/OPU}$	I/O pull-up		16	20	24	kΩ
R_{SIMPU}	SIM_I/O pull-up	SIM enabled and selected with CSEL	7.4	8.0	8.7	kΩ
R_{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			2	kΩ

SWITCHING CHARACTERISTICS – VSIMx = 1.8 V or 2.95 V Supplied by Internal LDO

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC = 1.8 V ± 0.15 V		UNIT
			MIN	MAX	
t_{rA}	I/O	C_L = 50 pF		1	µs
t_{rB}	SIMx_RST			1	µs
	SIMx_CLK			50	ns
	SIMx_I/O			100	ns
f_{max}	SIMx_CLK			25	MHz
Duty Cycle	SIMx_CLK		40%	60%	

OPERATING CHARACTERISTICS

T_A = 25°C, V_{SIMx} = 1.8 V

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}(1)	Class C (CLK, RST)	VCC-port input, VSIMx-port output	C_L = 0 f = 5 MHz t_r = t_f = 1 ns	12.7	pF
	Class B (CLK, RST)	VCC-port input, VSIMx-port output		15.4	
	CLASS C (IO)	VCC-port input, VSIMx-port output		10.8	pF
	CLASS B (IO)	VCC-port input, VSIMx-port output		20.3	

(1) Power dissipation capacitance per transceiver

PIN FUNCTION

PIN NAME	PIN NUMBER	PIN FUNCTION
VCC	2	Power supply and voltage reference for device operation and I/O buffers toward baseband.
VBATT	3	This is the battery power supply for the TXS4558.
VSIM1, VSIM2	1,4	1.8 V/2.95 V supply voltage for the respective SIM1 and SIM2. These outputs are activated through the EN1 and EN2 pins and set to be 1.8V or 2.95V through VSEL1 and VSEL2.
SIMCLK, SIM2CLK	5, 20	These are voltage level shifted CLK signals for connection to SIM1 and SIM2. Functionality while the corresponding SIM is not selected via CSEL is controlled by CLKRUN1 and CLKRUN2 control pins.
SIM1RST, SIM2RST	6, 19	These are voltage level shifted RST signals for connection to SIM1 and SIM2. Their output level when de-selected is latched at the last state.
SIM1IO, SIM2IO	7, 18	These are voltage level shifted IO signals for connection to SIM1 and SIM2. These are bi-directional data signals.
IO	8	Microcontroller side data IO pin. The IO pin provides the bidirectional communication path to the SIM cards. The SIMxIO communicating with IO is selected by CSEL.
RST	9	Microcontroller side reset RST pin input. RST provides signals directly to the selected SIM SIMxRST. When a SIM interface is deselected with CSEL, the last RST value is held at the SIMxRST.
CLK	10	The CLK pin supplies the clock signal to the cards. It is level shifted and transmitted directly to the SIMxCLK pin of the selected card. If CLKRUNx is HIGH, the clock signal will be transmitted to the SIMxCLK pin, regardless of whether that card is selected.
EN1, EN2	11, 17	EN1 and EN2 enable and disable the power supply to SIM1 and SIM2, and the corresponding interface.
VSEL1, VSEL2	12, 16	These pins set the VSIM1 and VSIM2 voltages and the corresponding interface IO voltages. When VSELx is low, VSIMx is 1.8V. When VSELx is high, VSIMx is 2.95V.
CSEL	13	CSEL selects which SIM is activated and communicates with the baseband. When CSEL is low, SIM1 is active. When CSEL is high, SIM2 is active.
CLKRUN1, CLKRUN2	14, 15	The CLKRUN1 and CLKRUN2 control the functionality of the SIM1CLK and SIM2CLK pins when their corresponding SIM cards are deselected using CSEL. When CLKRUNx is high, the CLK signal is transmitted to the corresponding SIMxCLK, even when the card is deselected with CSEL. When CLKRUNx is low, the SIMxCLK signal is brought low when the corresponding SIM is deselected with CSEL.
Exposed Center Pad	21	This center pad must be connected to ground.

OPERATION

Clock Run Mode

SIMS have varying requirements for the SIM CLK. Using CLKRUN, the user can decide if the SIMxCLK pin continuously transmits the CLK signal, or is brought low when the SIM is deselected with CSEL. If CLKRUNx is LOW, the SIMxCLK is brought LOW two clock cycles after the SIMx is deselected with CSEL. If SIMxCLK is high, the CLK transmits to the SIMxCLK, even if the SIMx is deselected with CSEL.

CSEL

When a channel is deselected using the CSEL pin, the SIMxRST state is latched, the SIMxIO becomes high impedance and SIMxCLK function is dependent on CLKRUNx.

Operation Activation/Deactivation

When the EN1, EN2 pin is brought high, the device performs the activation sequence for the corresponding SIM interface. Each SIM interface is activated independently based on its EN IO.

Activation Sequence

1. The device holds SIMxIO, SIMxCLK and SIMxRST low.
2. VSIMx is activated and powered.
3. The device waits for the VSIMx output to reach the correct voltage. Once this voltage is reached, SIMxIO, and SIMxRST are enabled.
4. The SIMxCLK is activated on the 2nd rising edge after the SIMxIO is enabled.

When the ENx pin is brought low, the device performs the deactivation sequence for the corresponding SIM interface. Deactivation Sequence,

Deactivation Sequence

1. SIMxRST is deactivated and set low.
2. Two clock cycles after EN is brought LOW, the SIMxCLK is disabled and brought LOW. If the CLK is not active, SIMxCLK is disabled and brought low approximately 9us after ENx is brought low.
3. Approximately 9us after the ENx is brought LOW, SIMxIO is disabled and set LOW.
4. After SIMxIO is brought LOW, the VSIMx is deactivated and unpowered.

APPLICATION INFORMATION

The LDO's included on the TXS4558 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{BAT} – $V_{SIM1/2}$). The TXS4558 provides fixed regulation at 1.8V or 2.95V. Low noise, GPIO enable and low ground pin current make it ideal for portable applications. The device offers current limit and thermal protection, and is fully specified from –40°C to 125°C.

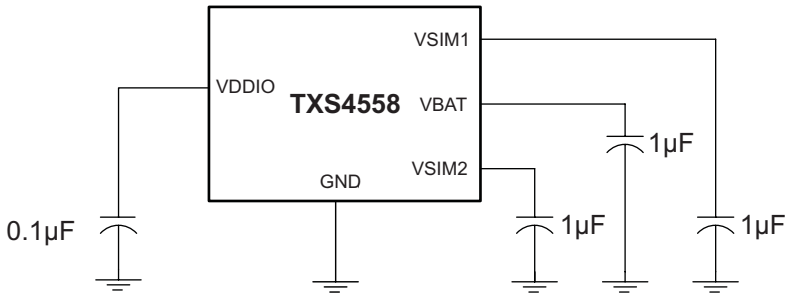


Figure 1. Typical Application Circuit for TXS4558

Input and Output Capacitor Requirements

It is good analog design practice to connect a 1.0 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a 0.1µF is required for the logic core supply (VCC).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values 1.0 µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0 Ω.

Output Noise

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Curent Limit

The TXS4558 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4558 has a built-in body diode that conducts current when the voltage at VSIM1/2 exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Dropout Voltage

The TXS4558 uses a PMOS pass transistor to achieve low dropout. When (V_{BAT} – $V_{SIM1/2}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

Startup

The TXS4558 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Minimum Load

The TXS4558 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4558 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4558 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4558 into thermal shutdown will degrade device reliability.

TYPICAL CHARACTERISTICS

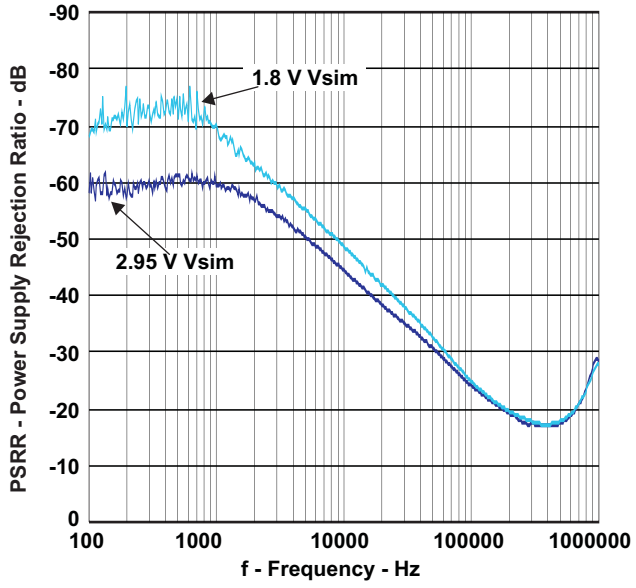


Figure 2. PSRR

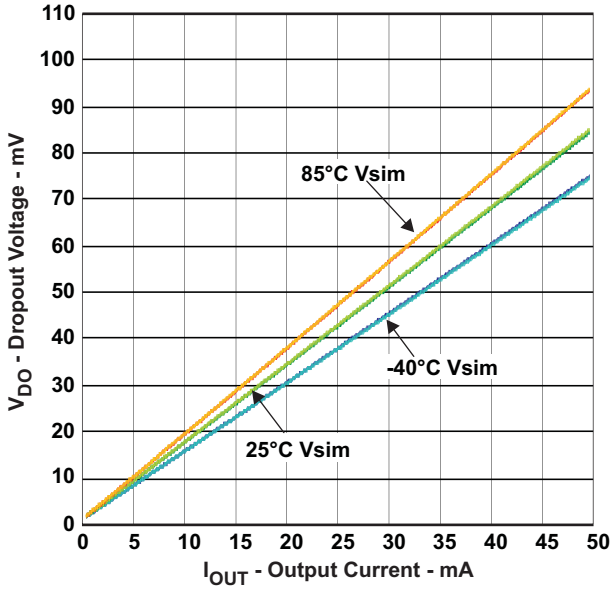


Figure 3. Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

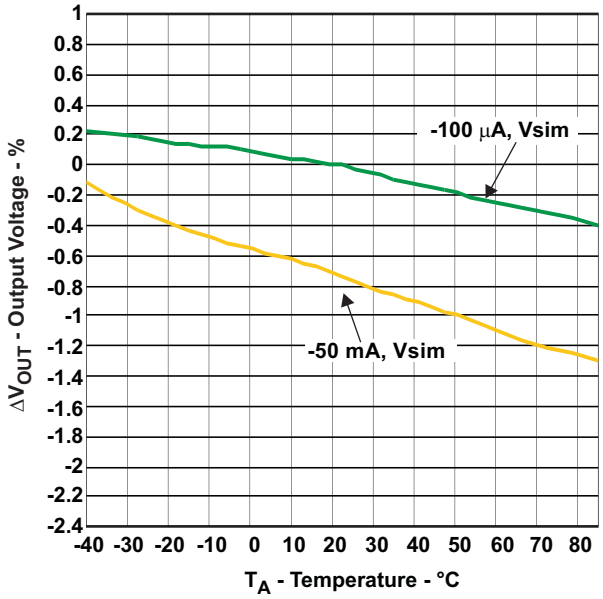


Figure 4. Output Voltage vs Temperature, Class-B/C

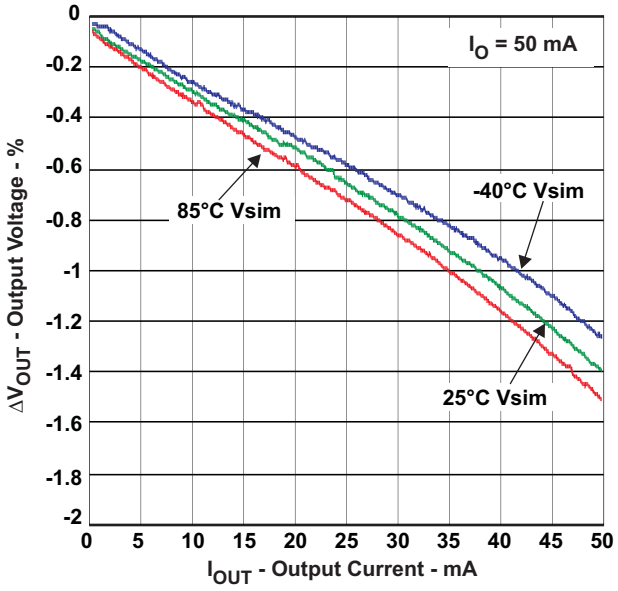


Figure 5. Load Regulation, Iout = 50 mA, Class-C

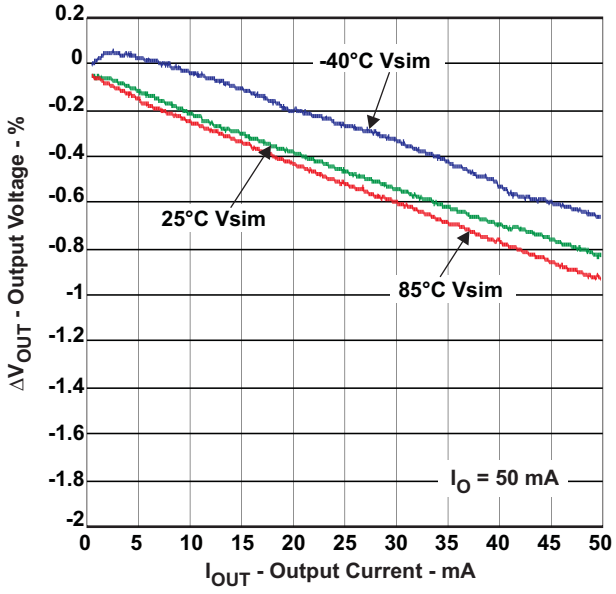


Figure 6. Load Regulation, Iout = 50 mA, Class-B

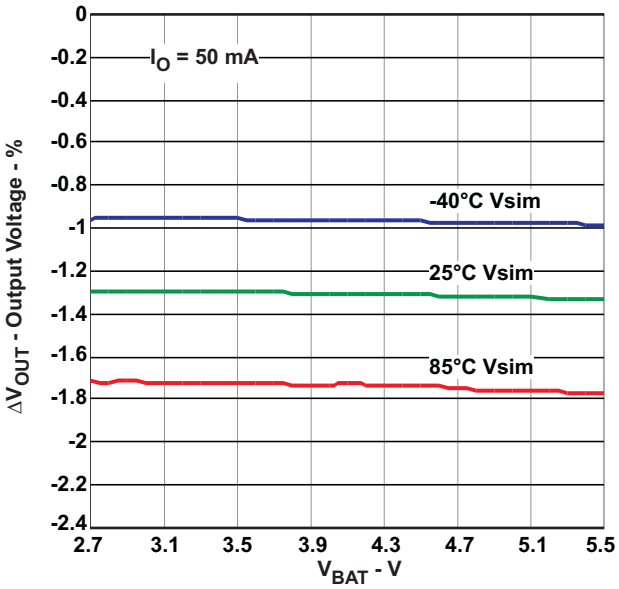


Figure 7. Line Regulation, Iout = 50 mA, Class-C

TYPICAL CHARACTERISTICS (continued)

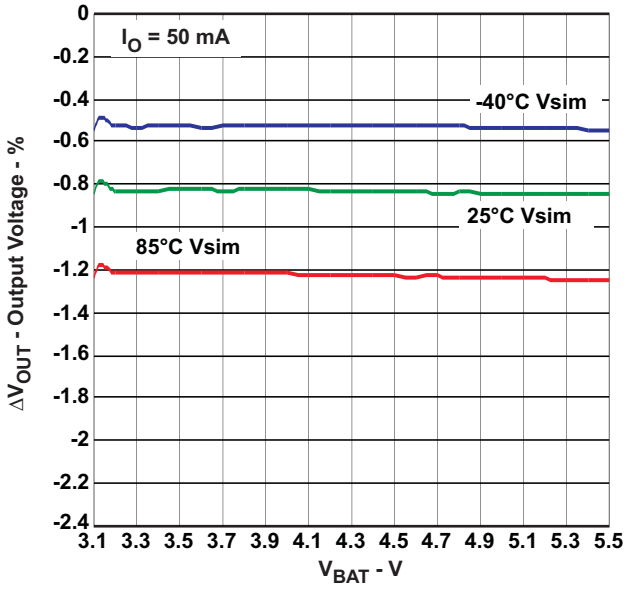


Figure 8. Line Regulation, Iout = 50 mA, Class-B

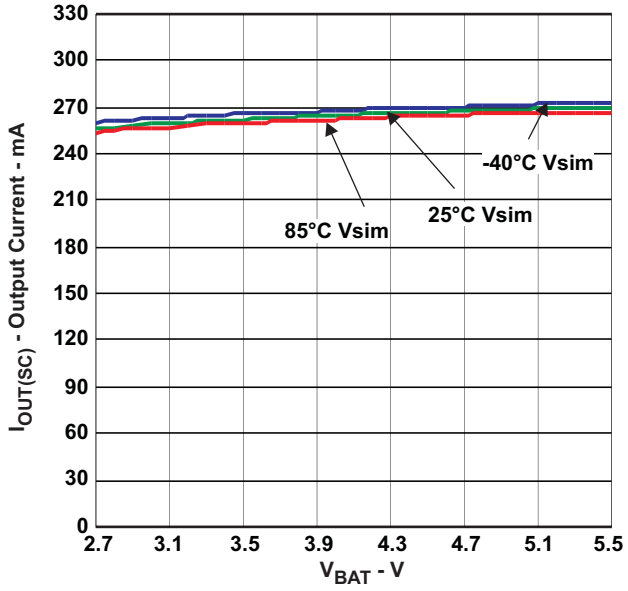


Figure 9. Current Limit vs Input Voltage, Class-B/C

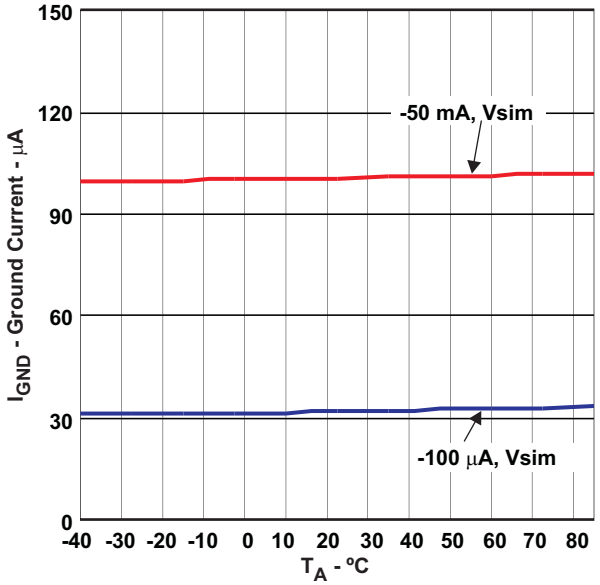


Figure 10. Ground Current vs Temperature, Class-C

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS4558RUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTG
TXS4558RUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTG
TXS4558RUKR.B	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTG
TXS4558RUKRG4	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTG
TXS4558RUKRG4.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

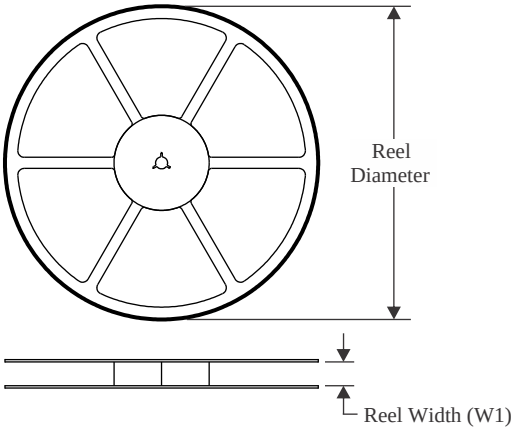
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

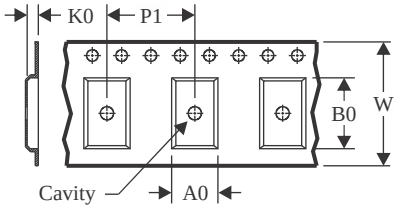
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

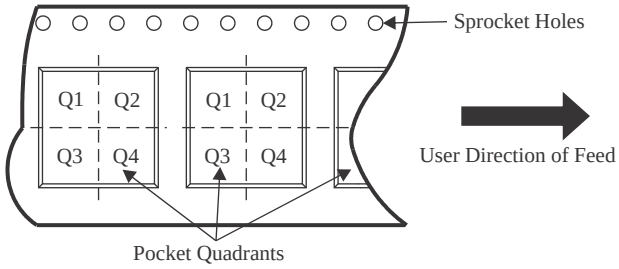


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

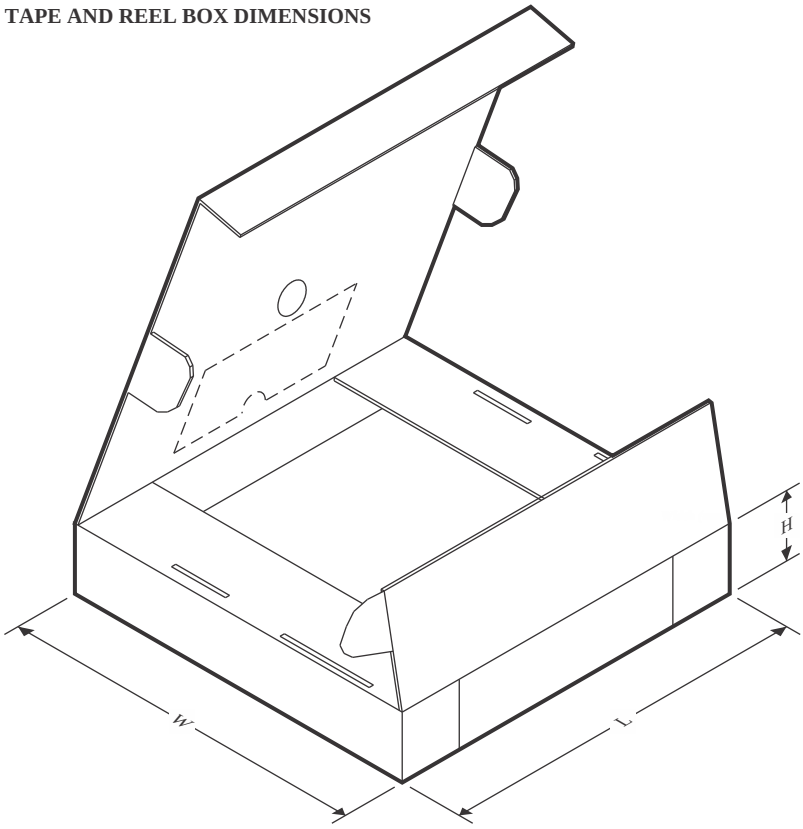
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4558RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TXS4558RUKRG4	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4558RUKR	WQFN	RUK	20	3000	335.0	335.0	25.0
TXS4558RUKRG4	WQFN	RUK	20	3000	335.0	335.0	25.0

GENERIC PACKAGE VIEW

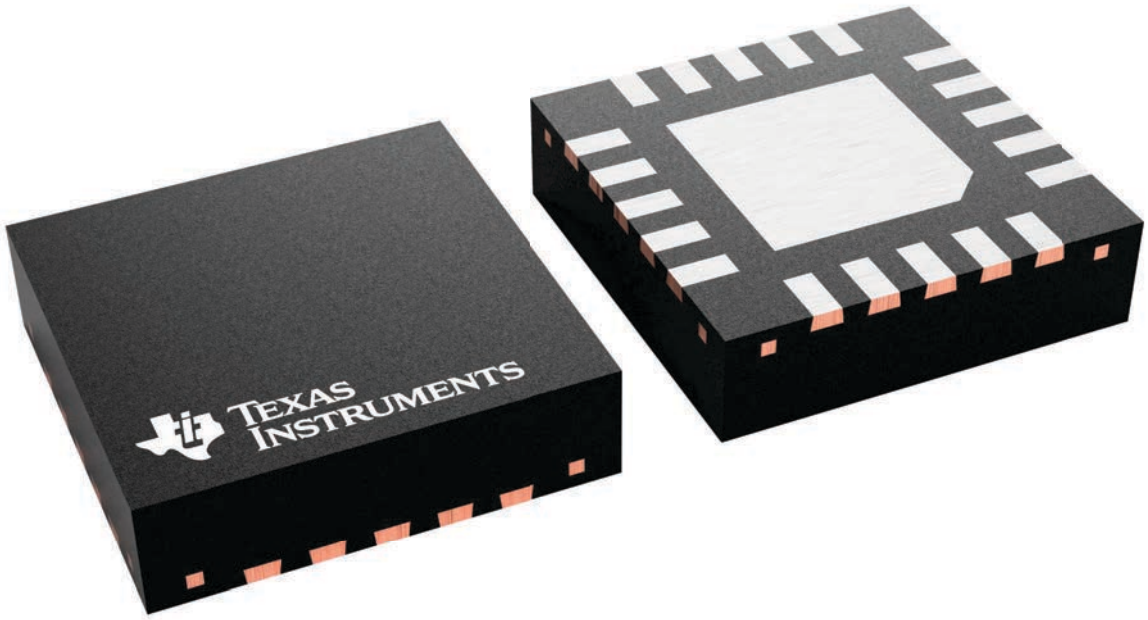
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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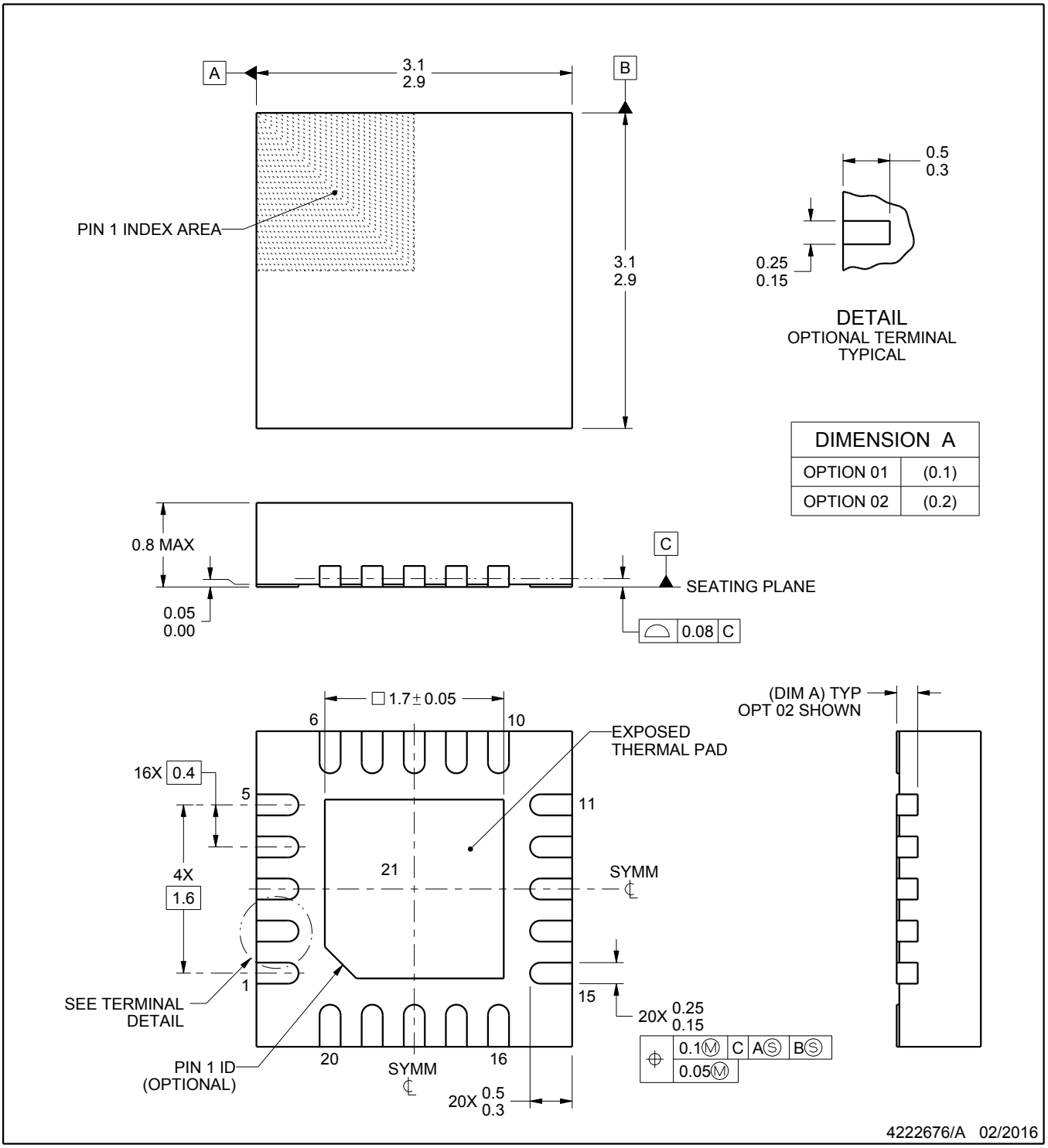
PACKAGE OUTLINE

RUK0020B

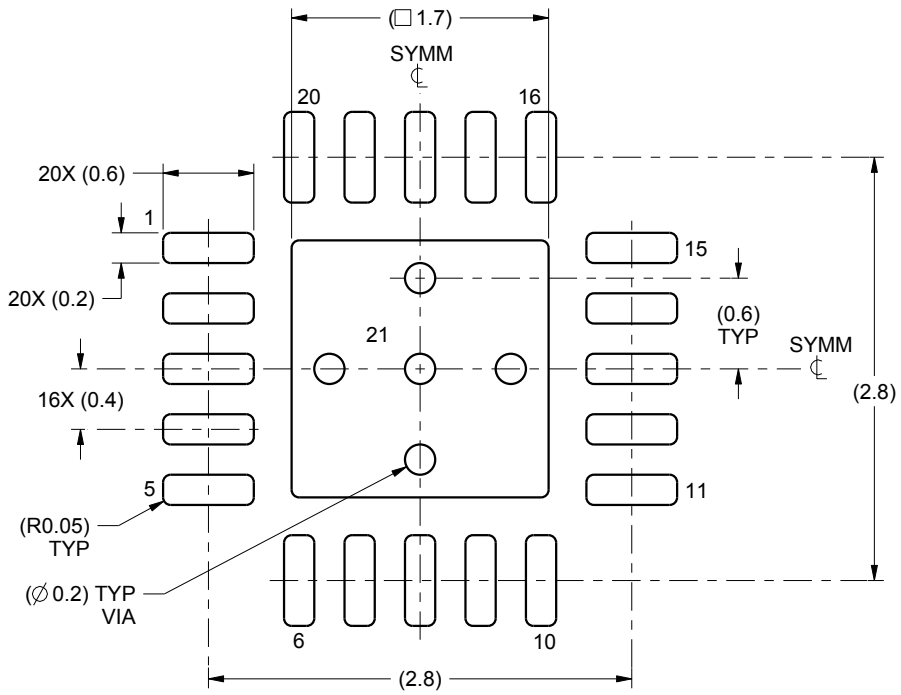
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

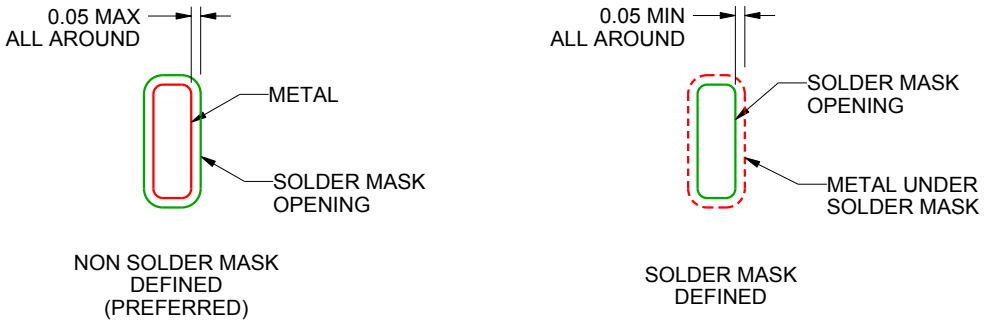


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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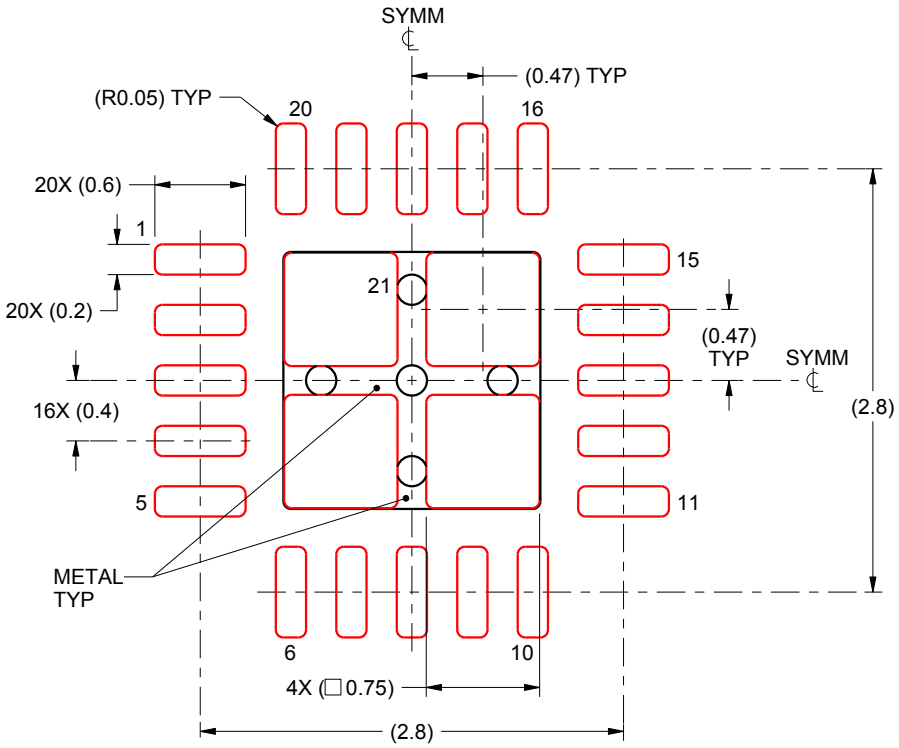
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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