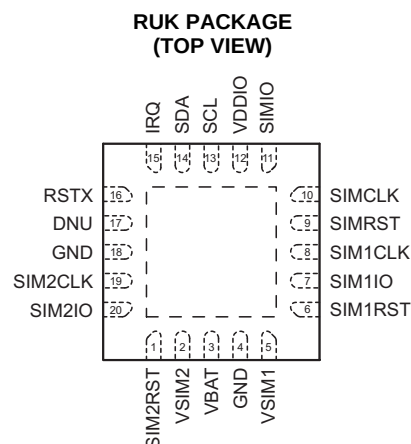


Dual-Supply 2:1 SIM Card Multiplexer/Translator With Slot Dedicated Dual LDO

Check for Samples: [TXS02324](#)

FEATURES

- **Level Translator**
 - VDDIO Range of 1.7 V to 3.3 V
- **Low-Dropout (LDO) Regulator**
 - 50-mA LDO Regulator With Enable
 - 1.8-V or 2.95-V Selectable Output Voltage
 - 2.3-V to 5.5-V Input Voltage Range
 - Very Low Dropout: 100 mV (Max) at 50 mA
- **Control and Communication Through I²C Interface With Baseband Processor**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-B)
 - 1000-V Charged-Device Model (C101)
- **Package**
 - 20-Pin QFN (3 mm x 3 mm)



Note: The Exposed Thermal Pad must be connect to Ground.

DESCRIPTION/ORDERING INFORMATION

The TXS02324 is a complete dual-supply standby Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with two individual SIM subscriber cards to store data for mobile handset applications. It is a custom device which is used to extend a single SIM/UICC interface to be able to support two SIMs/UICCs.

The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. It includes a high-speed level translator capable of supporting Class-B (2.95 V) and Class-C (1.8 V) interfaces, two low-dropout (LDO) voltage regulators that have output voltages that are selectable between 2.95-V Class-B and 1.8-V Class-C interfaces, an integrated "fast-mode" 400 kb/s "slave" I²C control register interface for configuration purposes, a 32-kHz clock input for internal timing generation.

The voltage-level translator has two supply voltage pins. VDDIO sets the reference for the baseband interface and can be operated from 1.7 V to 3.3 V. VSIM1 and VSIM2 are programmed to either 1.8 V or 2.95 V, each supplied by an independent internal LDO regulator. The integrated LDO accepts input battery voltages from 2.3 V to 5.5 V and outputs up to 50 mA to the B-side circuitry and external Class-B or Class-C SIM card.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUK	Tape and reel	TXS02324RUKR	ZUY

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

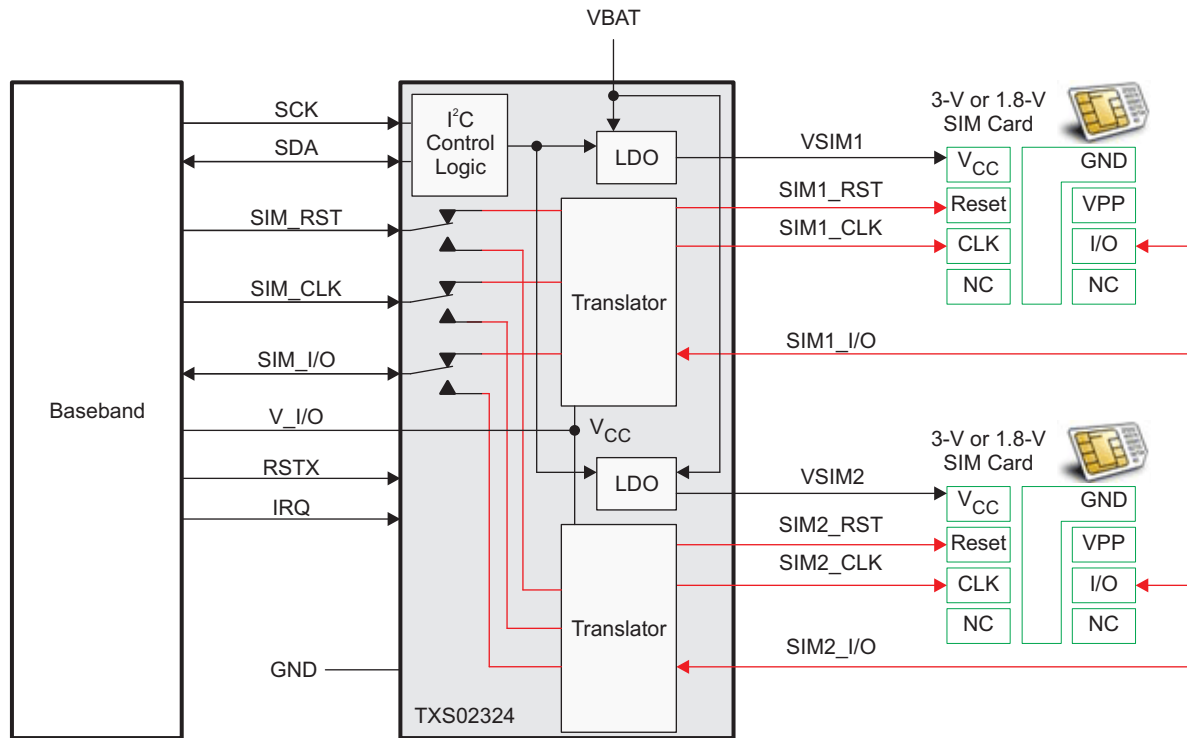


Figure 1. Interfacing With SIM Card

TERMINAL FUNCTIONS

NO.	NAME	TYPE ⁽¹⁾	POWER DOMAIN	DESCRIPTION
1	SIM2RST	O	VSIM2	SIM2 reset
2	VSIM2	O	VSIM2	1.8 V/2.95 V supply voltage to SIM2
3	VBAT	P	VBAT	Battery power supply
4	GND	G		Ground
5	VSIM1	O	VSIM1	1.8 V/2.95 V supply voltage to SIM1
6	SIM1RST	O	VSIM1	SIM1 reset
7	SIM1IO	I/O	VSIM1	SIM1 data
8	SIM1CLK	O	VSIM1	SIM1 clock
9	SIMRST	I	VDDIO	UICC/SIM reset from baseband
10	SIMCLK	I	VDDIO	UICC/SIM clock
11	SIMIO	I/O	VDDIO	UICC/SIM data
12	VDDIO	P	VDDIO	1.8-V power supply for device operation and I/O buffers toward baseband
13	SCL	I	VDDIO	I ² C clock
14	SDA	I/O	VDDIO	I ² C data
15	IRQ	I/O	VDDIO	Interrupt to baseband. This signal is used to set the I2C address.
16	RSTX	I	VDDIO	Active-low reset input from baseband
17	DNU	I	VDDIO	Do not use. Should not be electrically connected.
18	GND	G	-	GROUND
19	SIM2CLK	O	VSIM2	SIM2 clock
20	SIM2IO	I/O	VSIM2	SIM2 data

(1) G = Ground, I = Input, O = Output, P = Power

Table 1. Register Overview

REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	READ OR WRITE	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	1	0	0	0	1	00h	Device hardware revision information	R	0001 0001
0	0	0	0	0	0	0	0	01h	Software revision information	R	0000 0000
SIM2 Interface Status		SIM1 Interface Status		Unused	Unused	Unused	Unused	04h	Status Register	R	0000 0000
SIM2 Interface Status		SIM2 Voltage Select	SIM2 LDO Enable/ Disable	SIM1 Interface Status		SIM1 Voltage Select	SIM1 LDO Enable/ Disable	08h	SIM Interface Control Register	R/W	0000 0000

Table 2. Device Hardware Revision Register (00h)

Device HW Driver Register	Bits(s)	Type (R/W)	Description
HW identification	7:0	R	This register contains the manufacturer and device ID ⁽¹⁾ (value to be specified by the manufacturer)

- (1) The manufacturer ID part of this data shall remain unchanged when the HW revision ID is updated. The manufacturer ID shall uniquely identify the manufacturer. The manufacturer ID is encoded on the MSB nibble.

Table 3. Device Software Revision Register (01h)

Device SW Driver Register	Bits(s)	Type (R/W)	Description
SW Driver Version	7:0	R	This register contains information about the SW driver required for this device. This information shall only be updated when changes to the device requires SW modifications. Initial register value is 00h

Table 4. Status Register (04h)

Status Register	Bits(s)	Type (R/W)	Description
Unused	0	Unused	Unused
Unused	1	Unused	Unused
Unused	2	Unused	Unused
Unused	3	Unused	Unused
SIM1 Interface Status [1:0]	5:4 ⁽¹⁾	R	Status of SIM1 interface '00' Powered down with pull-downs activated '01' Isolated with pull-downs deactivated '10' Powered with pull downs activated '11' Active with pull downs deactivated
SIM2 Interface Status [1:0]	7:6 ⁽¹⁾	R	Status of SIM2 interface '00' Powered down with pull-downs activated '01' Isolated with pull-downs deactivated '10' Powered with pull downs activated '11' Active with pull downs deactivated

- (1) The content of bits 5:4 and 7:6 reflects the value written to the state bits in the SIM Interface control register 3:2 and 7:6 respectively and the setting of the regulator bits in the SIM interface control register 0 and 4 respectively.

Table 5. SIM Interface Control Register (08h)⁽¹⁾⁽²⁾

Status Register	Bit(s)	Type (R/W)	Description
SIM1 Regulator Control	0	R/W	'0' Regulator is off, regulator output is pulled down '1' Regulator is powered on, regulator output pull-down is released
SIM1 Regulator Voltage Selection	1	R/W	'0' 1.8 V '1' 2.95 V
SIM1 Interface State [1:0]	3:2	R/W	Status of SIM1 interface '00' Powered down state with pull-downs activated '01' Isolated state with pull-downs deactivated '10' Not allowed '11' Active state with pull downs deactivated
SIM2 Regulator Control	4	R/W	'0' Regulator is off, regulator output is pulled down '1' Regulator is powered on, regulator output pull-down is released

- (1) Reset value: 00h
(2) The state '10', on bits 3:2 and 7:6, is not prevented by HW but shall never be set by SW. State '10' means that the interface is powered with the pull-downs active, this state correspond to state '00' with the regulator being switched on. Setting the state to '10' does not have any impact on the corresponding regulator bit setting. The regulator control bits do not impact the state bits in this register. The regulator control bits however do impact the status bits in the status register.

Table 5. SIM Interface Control Register (08h)⁽¹⁾⁽²⁾ (continued)

Status Register	Bit(s)	Type (R/W)	Description
SIM2 Regulator Voltage	5	R/W	'0' 1.8 V '1' 2.95 V
SIM2 Interface State [1:0]	7:6	R/W	Status of SIM2 interface '00' Powered down state with pull-downs activated '01' Isolated state with pull-downs deactivated '10' Not allowed '11' Active state with pull downs deactivated

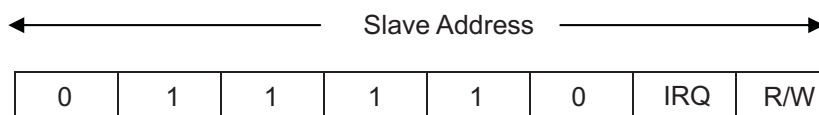
BASIC DEVICE OPERATION

The TXS02324 is controlled through a standard I²C interface reference to VDDIO. It is connected between the two SIM card slots and the SIM/UICC interface of the baseband. The device uses VBAT and VDDIO as supply voltages. The supply voltage for each SIM card is generated by an on-chip low drop out regulator. The interface between the baseband and the TXS02324 is reference to VDDIO while the interface between the TXS02324 and the SIM card is referenced to the LDO output of either VSIM1 or VSIM2 depending on which slot is being selected. The VDDIO on the baseband side normally does not exceed 1.8V, thus voltage level shifting is needed to support a 3V SIM/UICC interface (Class B).

The TXS02324 has two basic states, the reset and operation state. The baseband utilizes information in the status registers to determine how to manipulate the control registers to properly switch between two SIM cards. These fundamental sequences are outlined below and are to help the user to successfully incorporate this device into the system.

DEVICE ADDRESS

The address of the device is shown below:



Address Reference

IRQ@ Reset	R/W	Slave Address
0	0 (W)	120 (decimal), 78(h)
0	1 (R)	121 (decimal), 79(h)
1	0 (W)	122 (decimal), 7A(h)
1	1 (R)	123 (decimal), 7B(h)

RESET STATE

In the reset state the device settings are brought back to their default values and any SIM card that has been active is deactivated. After reset, neither of the UICC/SIM interfaces is selected. The active pull-downs at the UICC/SIM interface are automatically activated. To ensure the system powers up in an operational state, device uses an internal 32 KHz clock for internal timing generation.

- Power up the TXS02324 by asserting VBAT to enter the operation state
- I²C Interface becomes active with the VDDIO supply

RESET summary:

- Any pending interrupts are cleared
- I²C registers are in the default state
- Both on chip regulators are set to 1.8V and disabled
- All SIM1 and SIM2 signals are pulled to GND

SETTING UP THE SIM INTERFACE

The TXS02324 supports both Class C (1.8V) or Class B (2.95V) SIM cards. In order to support these cards types, the interface on the SIM side needs to be properly setup. After power up, the system should default to SIM1 card. The following sequence outlines a rudimentary sequence of preparing the SIM1 card interface:

- Configure the SIM1 regulator to 1.8V by asserting B1 = 0 in the SIM Interface Control Register (08h). The system by default should start in 1.8V mode.
- The baseband SIM interface is set to a LOW state.
- Disable the SIM1 interface by asserting B2 = 0 and B3 = 0 in the SIM Interface Control Register.
- Disable the SIM2 interface by asserting B6 = 0 and B7 = 0 in the SIM Interface Control Register.
- VSIM1 voltage regulator should now be activated by asserting B0 = 1 in the SIM Interface Control Register.
- Enable the SIM1 interface by asserting B2 = 1 and B3 = 1 in the SIM Interface Control Register.
- The SIM1 interface (VSIM1, SIM1CLK, SIM1I/O) is now active. The TXS02324 relies on the baseband to perform the power up sequencing of the SIM card. If there is lack of communication between the baseband and the SIM card, the SIM1 interface must be powered-down and then powered up again through the regulator by configuring it to 2.95V by asserting B1 = 1 in the SIM Interface Control Register.

SWITCHING BETWEEN SIM CARDS

The following sequence outlines a rudimentary sequence of switching between the SIM1 card and SIM2 card:

- Put the SIM1 card interface into “clock stop” mode then assert B2 = 1 and B3 = 0 in the SIM Interface Control Register (08h). This will latch the state of the SIM1 interface (SIM1CLK, SIM1I/O, SIM1RST).
- There can be two scenarios when switching to SIM2 card:
 - SIM2 may be in the power off mode, B6 = 0 and B7 = 0 in the Status Register (04h). If SIM2 is in power off mode, the SIM/UICC interface will need to be set to the power off state. In this case the baseband will most likely need to go through a power up sequence iteration
 - SIM2 may already be in the “clock stop” mode, B6 = 1 and B7 = 0 in the Status Register (04h). If SIM2 is in “clock stop” mode, the interface between the baseband and the device is set to the clock stop mode levels that correspond to the SIM2 card interface.
- After determining whether the SIM2 card is either in power off mode or clock stop mode, the SIM2 card interface is then activated by asserting B6 = 1 and B7 = 1 in the SIM Interface Control Register (08h) and the negotiation between the baseband and card can continue.
- Switching from SIM2 to SIM1 done in the same manner.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

Level Translator⁽¹⁾

		MIN	MAX	UNIT
VDDIO	Supply voltage range	−0.3	4.0	V
V _I	Input voltage range	V _{I/O} -port	−0.5	4.6
		VSIMx-port	−0.5	4.6
		Control inputs	−0.5	4.6
V _O	Voltage range applied to any output in the high-impedance or power-off state	V _{I/O} -port	−0.5	4.6
		VSIMx-port	−0.5	4.6
V _O	Voltage range applied to any output in the high or low state	V _{I/O} -port	−0.5	4.6
		VSIMx-port	−0.5	4.6
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CCA} or GND		±100	mA
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

LDO⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	−0.3	6	V
V _{OUT}	Output voltage range	−0.3	6	V
T _J	Junction temperature range	−55	150	°C
T _{stg}	Storage temperature range	−55	150	°C
ESD rating	Human-Body Model (HBM)		2	kV
	Charged-Device Model (CDM)		1000	V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	RUK package	94.1	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾**Level Translator**

	Description	MIN	MAX	UNIT
VDDIO	Supply voltage	1.7	3.3	V
V _{IH}	High-level input voltage	VDDIO × 0.7	1.9	V
V _{IL}	Low-level input voltage		VDDIO × 0.3	V
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
T _A	Operating free-air temperature	–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VDDIO	VSIM1	VSIM2	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	SIM1RST	I _{OH} = –100 µA Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)	VSIM1 × 0.8			V
	SIM1CLK					VSIM1 × 0.8			
	SIM1IO	I _{OH} = –10 µA Open-Drain				VSIM1 × 0.8			
	SIM2RST	I _{OH} = –100 µA Push-Pull				VSIM2 × 0.8			
	SIM2CLK					VSIM2 × 0.8			
	SIM2IO	I _{OH} = –10 µA Open-Drain				VSIM2 × 0.8			
	SIMIO	I _{OH} = –10 µA Open-Drain				VDDIO × 0.8			
V _{OL}	SIM1RST	I _{OL} = 1 mA Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			VSIM1 × 0.2	V
	SIM1CLK	I _{OL} = 1 mA Push-Pull						VSIM1 × 0.2	
	SIM1IO	I _{OL} = 1 mA Open-Drain						0.3	
	SIM2RST	I _{OL} = 1 mA Push-Pull						VSIM2 × 0.2	
	SIM2CLK	I _{OL} = 1 mA Push-Pull						VSIM2 × 0.2	
	SIM2IO	I _{OL} = 1 mA Open-Drain						0.3	
	SIMIO	I _{OL} = 1 mA Open-Drain						0.3	
I _I	Control inputs	V _I = OE	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±1	µA
I _{CC I/O}		V _I = V _{CCI} I _O = 0	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±5	µA
C _{io}	SIM_I/O port						7		pF
	SIMx port						4		
C _i	Control inputs	V _I = V _{I/O} or GND					3		pF
	Clock input								

(1) All typical values are at T_A = 25°C.

ELECTRICAL CHARACTERISTICS

LDO (Control Input Logic = High)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{BAT}	Input voltage			2.3		5.5	V	
V _{OUT}	Output voltage	Class-B Mode		2.82	2.95	3.18	V	
		Class-C Mode		1.65	1.8	1.95		
V _{DO}	Dropout voltage	I _{OUT} = 50 mA					100	mV
I _{GND}	Ground-pin current	I _{OUT} = 0 mA					35	μA
		I _{OUT} = 50 mA					150	
I _{SHDN}	Shutdown current (I _{GND})	V _{ENx} ≤ 0.4 V, (V _{SIMx} + V _{DO}) ≤ V _{BAT} ≤ 5.5 V, T _J = 85°C					3	μA
I _{OUT(SC)}	Short-circuit current	R _L = 0 Ω					400	mA
C _{OUT}	Output Capacitor			1				μF
PSRR	Power-supply rejection ratio	V _{BAT} = 3.25 V, V _{SIMx} = 1.8 V or 3 V, C _{OUT} = 1 μF, I _{OUT} = 50 mA	f = 1 kHz	50				dB
			f = 10 kHz	40				
T _{STR}	Start-up time	V _{SIMx} = 1.8 V or 3 V, I _{OUT} = 10 mA, C _{OUT} = 1 μF					50	μS
T _J	Operating junction temperature			−40			85	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hyst	Internal hysteresis of comparator			±50		mV
R _{SIMPU}	SIM I/O pull-up			20		kΩ
R _{SIMxPU}	SIMx I/O pull-up	Class B		7.5		kΩ
		Class C		4.5		
R _{SIMPD}	SIMx I/O pull-down	Active pull-downs are connected to the VSIM1/2 regulator output to the SIM1/2 CLK, SIM1/2 RST, SIM1/2 I/O when the respective regulator is disabled		2		kΩ

SWITCHING CHARACTERISTICS
VSIMx = 1.8 V or 2.95 V Supplied by Internal LDO, VBAT = 2.3V to 5.5V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{I/O} = 1.7 V to 3.3 V	UNIT
			TYP	
t_{rA} Baseband side to SIM side	SIMIO	Open Drain	210	ns
	SIMRST	Push Pull	4.3	ns
	SIMCLK	Push Pull	4	ns
t_{rA} Baseband side to SIM side	SIMxIO	Open Drain	16	ns
	SIMRST	Push Pull	4	ns
	SIMxCLK	Push Pull	5	ns
t_{rB} SIM side to Baseband side	SIMxIO	Open Drain	210	ns
t_{rB} SIM side to Baseband side	SIMxIO	Open Drain	6	ns
f_{max}	SIMxCLK	Push Pull	5	MHz
t_{PLH}	SIMCLK to SIMxCLK	Push Pull	8	ns
	SIMRST to SIMxRST	Push Pull	8	ns
	SIMIO to SIMxIO	Open Drain	260	ns
	SIMxIO to SIMIO	Open Drain	260	ns
t_{PHL}	SIMCLK to SIMxCLK	Push Pull	7	ns
	SIMRST to SIMxRST	Push Pull	7	ns
	SIMIO to SIMxIO	Open Drain	23	ns
	SIMxIO to SIMIO	Open Drain	23	ns

OPERATING CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{\text{SIMx}} = 1.8\text{ V}$ for Class C, $V_{\text{SIMx}} = 2.95\text{ V}$ for Class B

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} ⁽¹⁾	Class B	$C_L = 0$, $f = 5\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	11	pF
	Class C		9.5	

(1) Power dissipation capacitance per transceiver

APPLICATION INFORMATION

The LDO's included on the TXS02324 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ($V_{BAT} - V_{SIM1/2}$). The TXS02324 provides fixed regulation at 1.8V or 2.95V. Low noise, enable (through I²C control), low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +85°C.

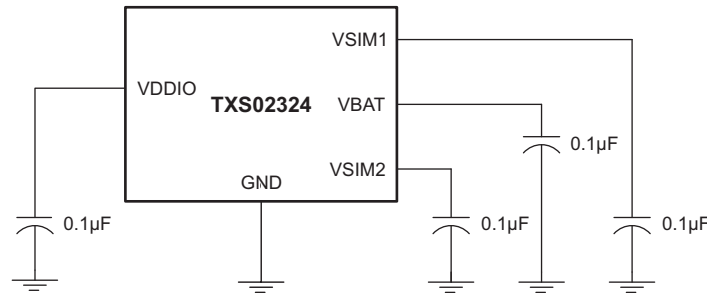


Figure 2. Typical Application circuit for TXS02324

Input and Output Capacitor Requirements

It is good analog design practice to connect a 1.0 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a 0.1µF is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values 1.0 µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0 Ω.

Output Noise

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TXS02324 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS02324 has a built-in body diode that conducts current when the voltage at $V_{SIM1/2}$ exceeds the voltage at V_{BAT} . This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Dropout Voltage

The TXS02324 uses a PMOS pass transistor to achieve low dropout. When $(V_{BAT} - V_{SIM1/2})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

Startup

The TXS02324 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times. Note that for fastest startup, V_{BATT} should be applied first, and then enabled by asserting the I²C register.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Minimum Load

The TXS02324 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS02324 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +85°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +85°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS02324 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS02324 into thermal shutdown will degrade device reliability.

TYPICAL CHARACTERISTICS

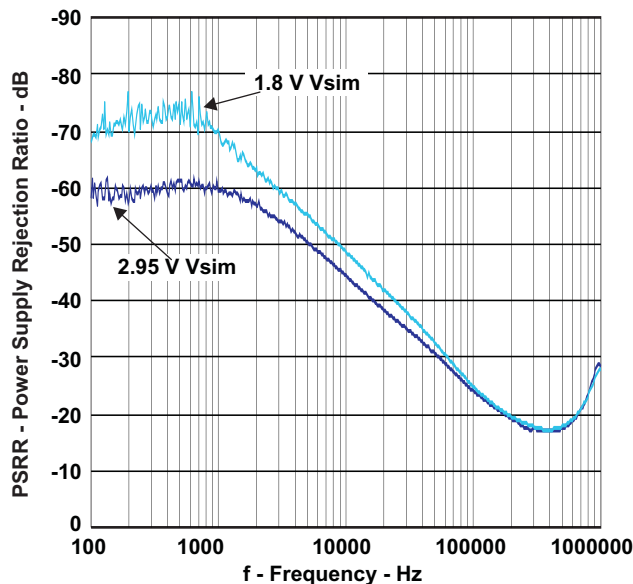


Figure 3. PSRR

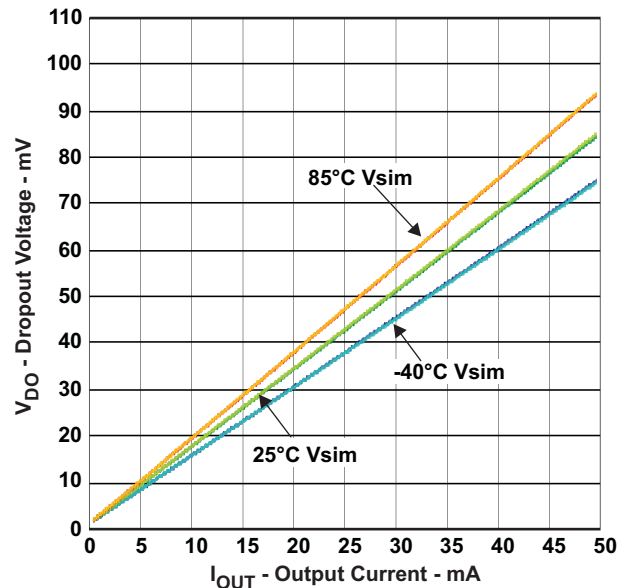


Figure 4. Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

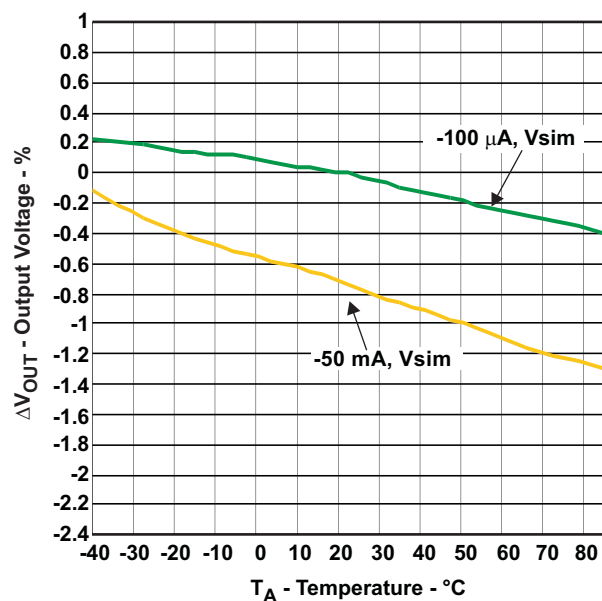


Figure 5. Output Voltage vs Temperature, Class-B/C

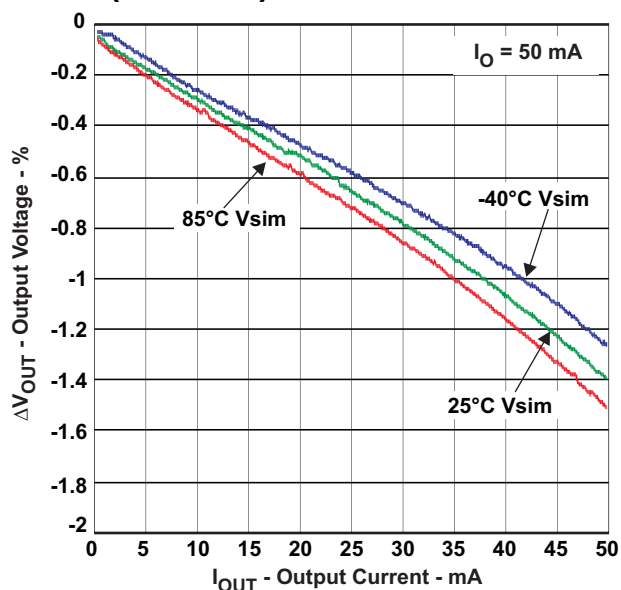


Figure 6. Load Regulation, Iout = 50 mA, Class-C

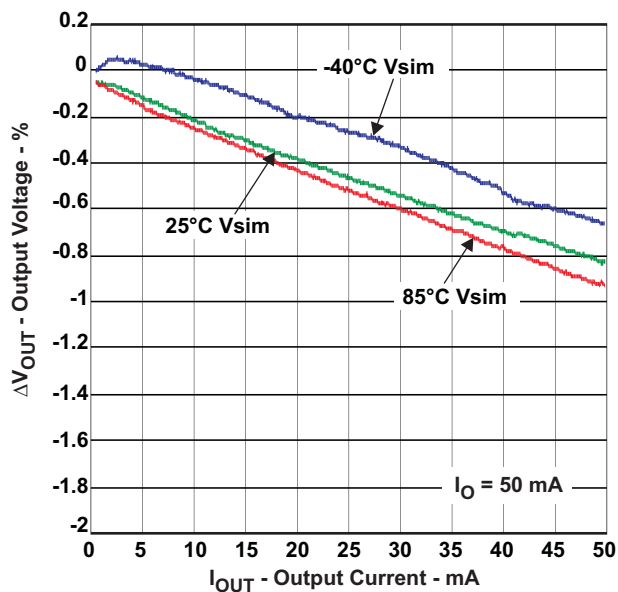


Figure 7. Load Regulation, Iout = 50 mA, Class-B

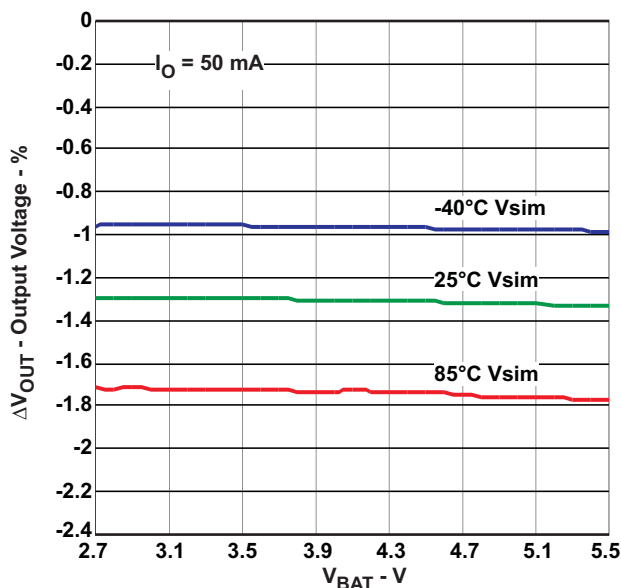


Figure 8. Line Regulation, Iout = 50 mA, Class-C

TYPICAL CHARACTERISTICS (continued)

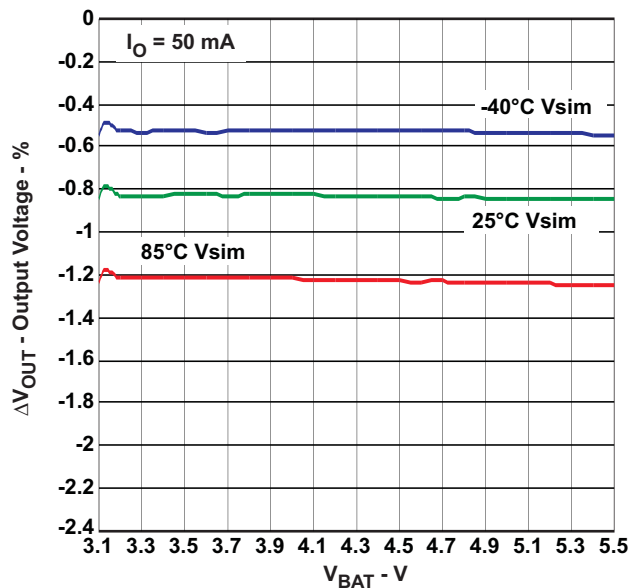
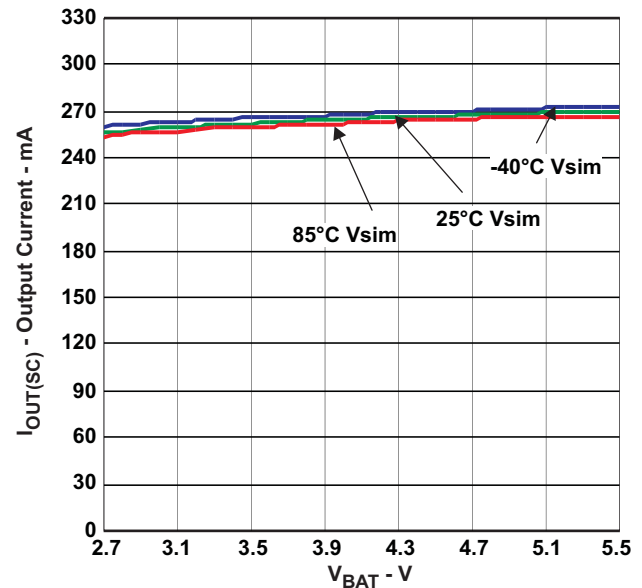
Figure 9. Line Regulation, $I_{out} = 50\text{ mA}$, Class-B

Figure 10. Current Limit vs Input Voltage, Class-B/C

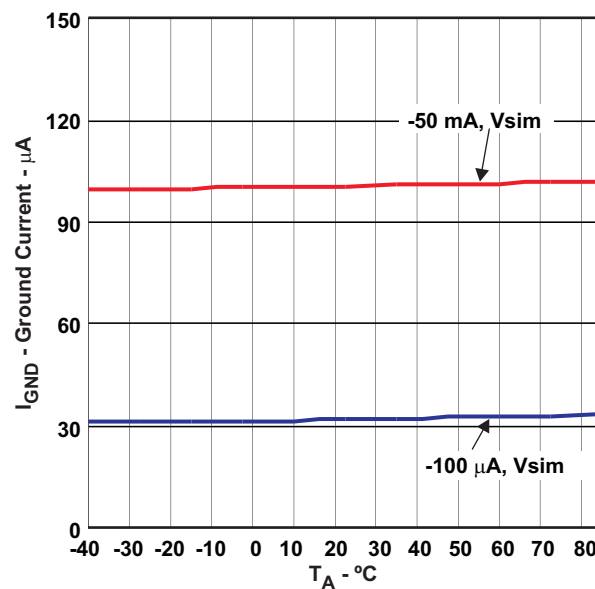


Figure 11. Ground Current vs Temperature, Class-C

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS02324RUKR	Active	Production	WQFN (RUK) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUY
TXS02324RUKR.B	Active	Production	WQFN (RUK) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUY

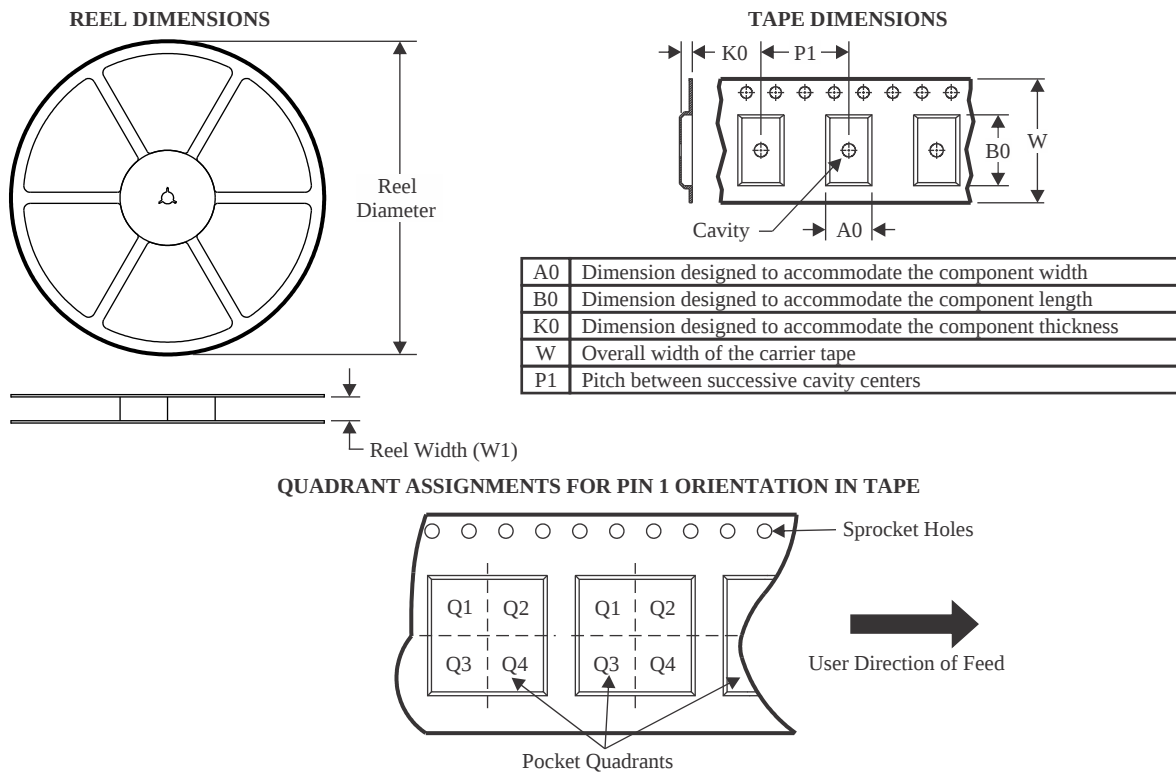
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

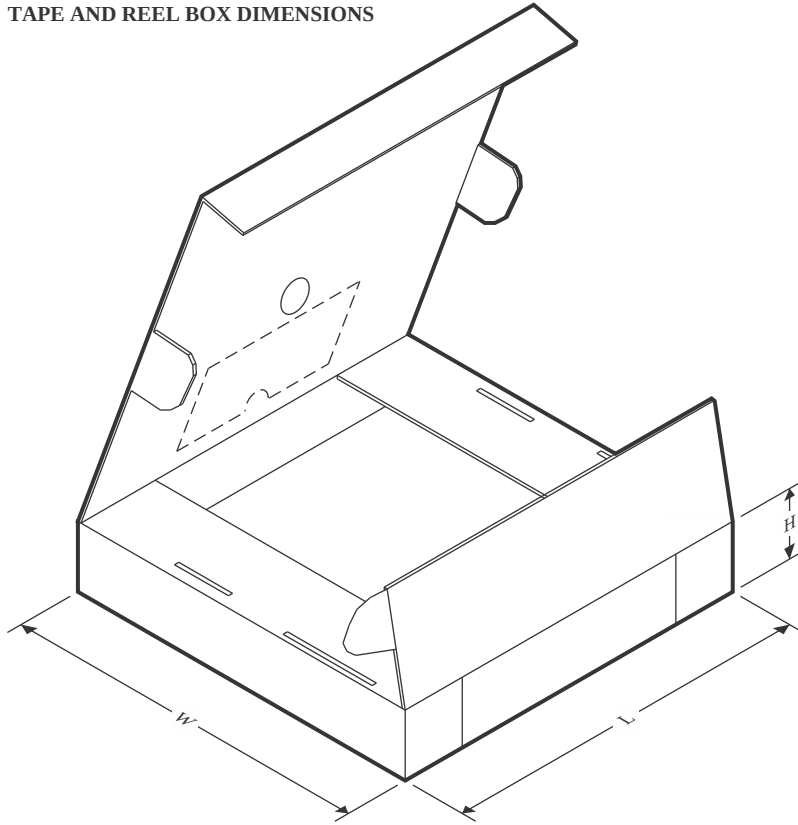
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS02324RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS02324RUKR	WQFN	RUK	20	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

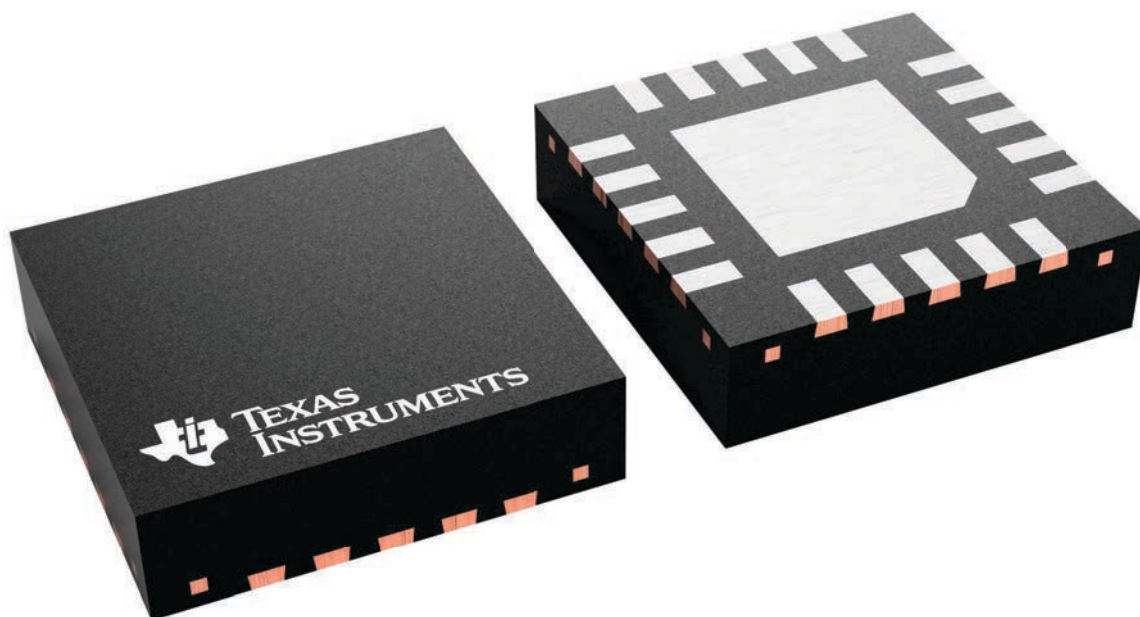
RUK 20

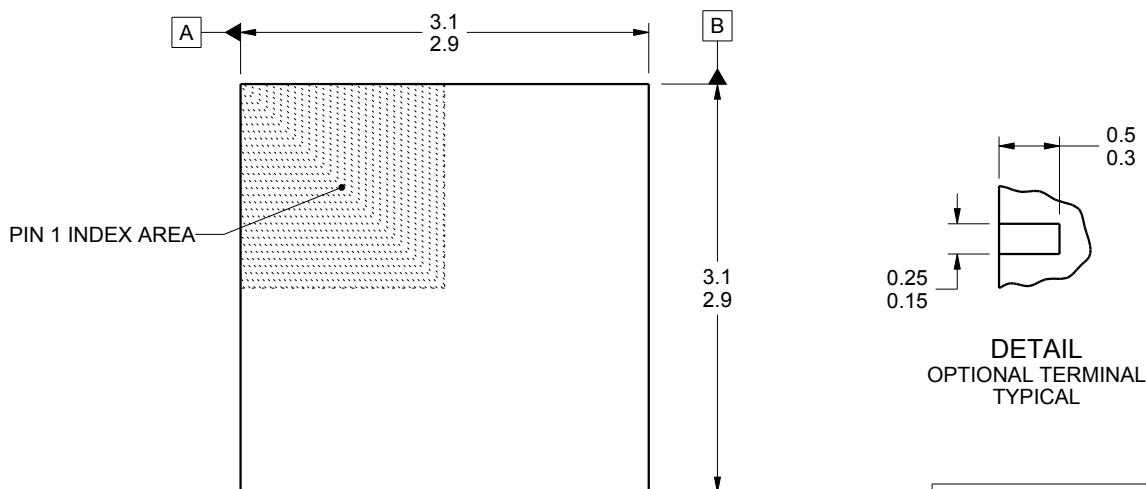
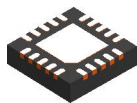
WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

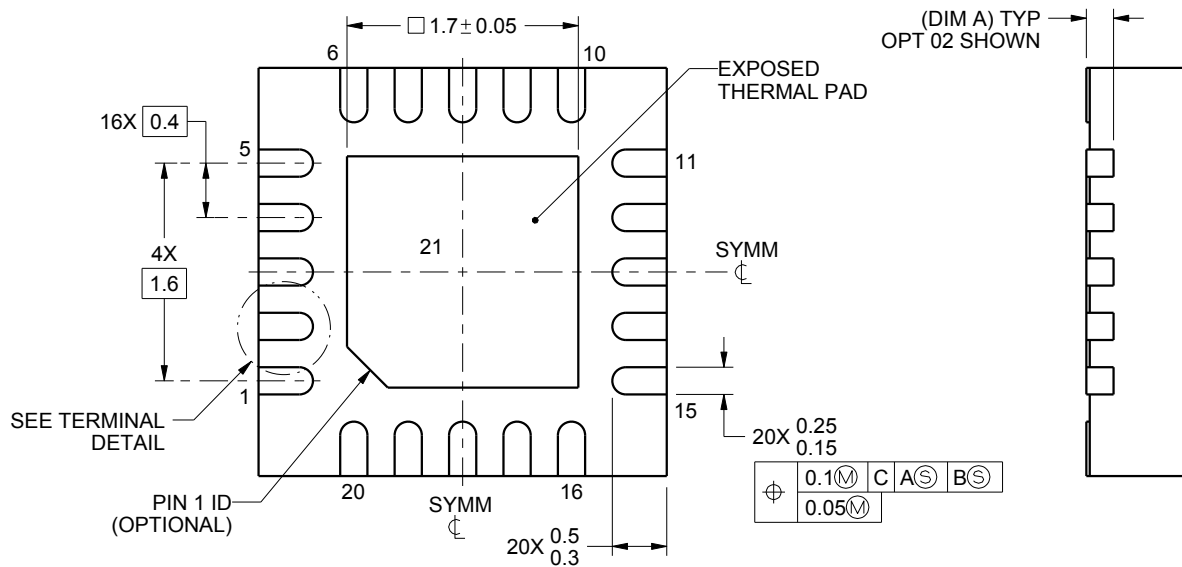
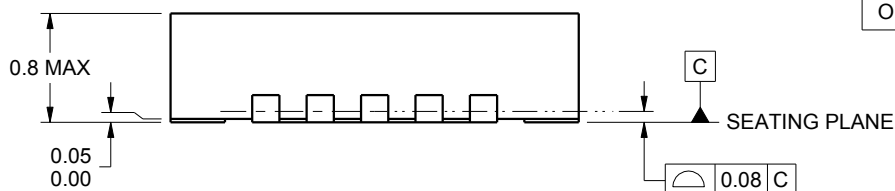
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)



4222676/A 02/2016

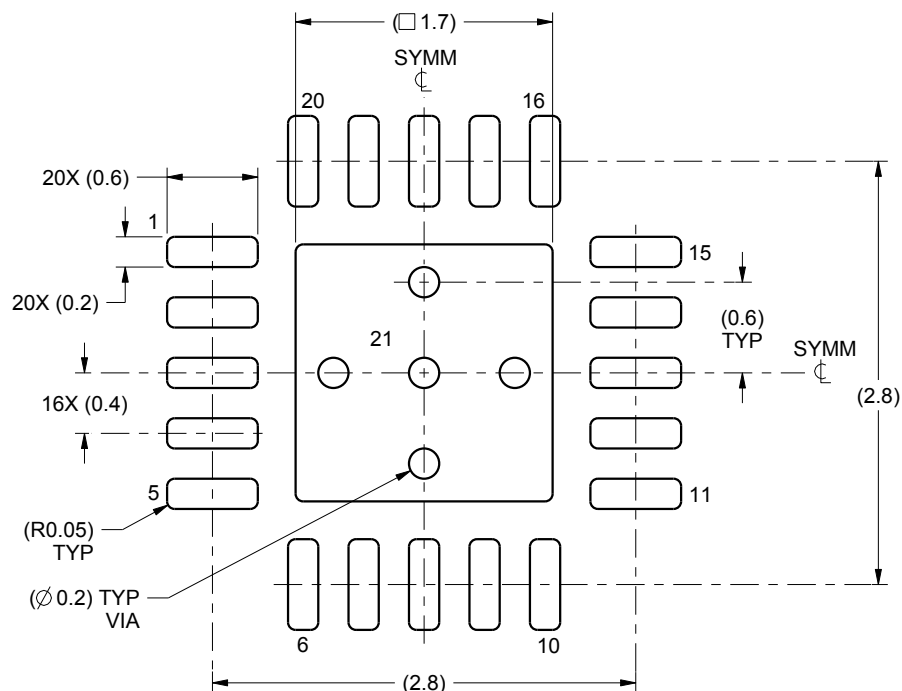
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

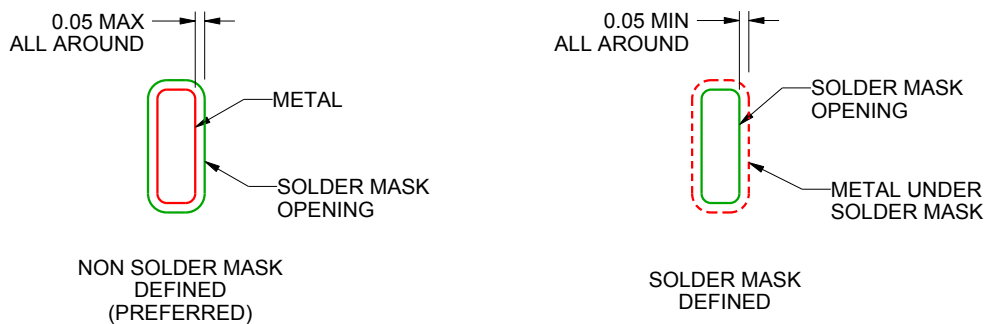
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

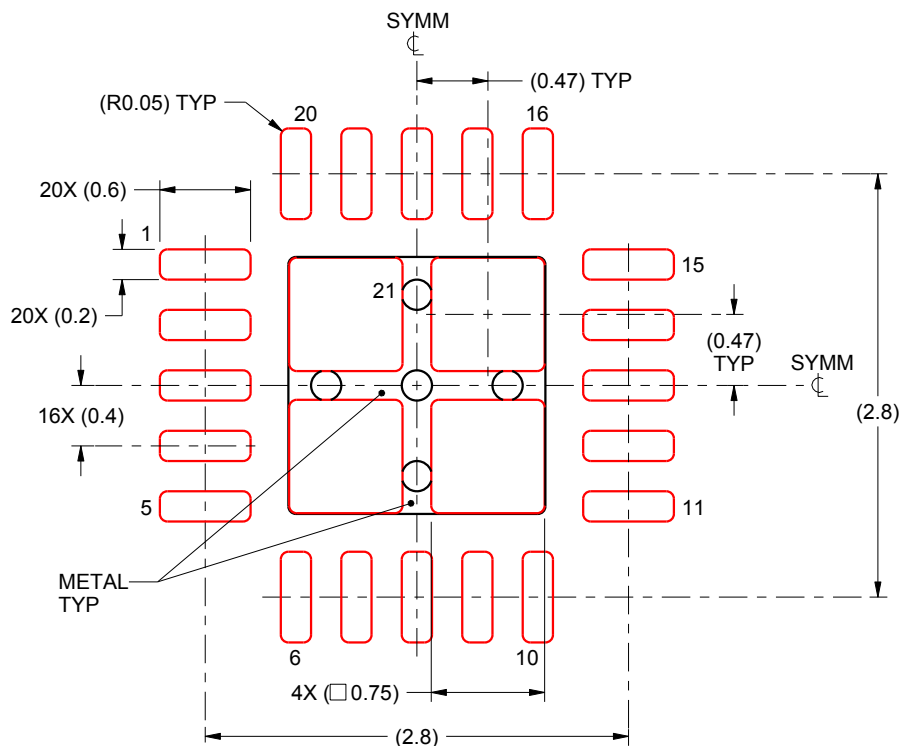
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated