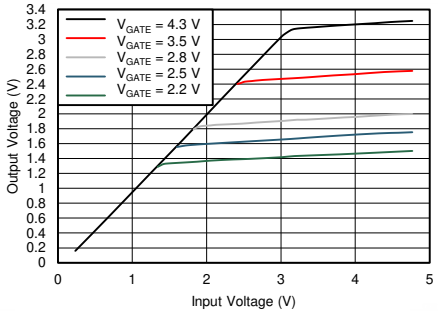
TXS0104E-Q1 オープン ドレイン / プッシュプル アプリケーション用車載 4 ビット双方向電圧レベル トランスレータ

1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 方向制御信号不要
- 最大データ・レート:
  - 最大 24Mbps (プッシュプル)
  - 2Mbps (オープン・ドレイン)
- 1.65V～3.6V (A ポート)、2.3V～5.5V (B ポート) ($V_{CCA} \leq V_{CCB}$)
- 電源投入のシーケンス不要:V_{CCA} または V_{CCB} のいずれからでも立ち上げ可能
- JESD 22 を上回る ESD 保護:
  - A ポート
    - 2000V、人体モデル (A114-B)
    - 1000V、荷電デバイス・モデル (C101)
  - B ポート
    - 15kV、人体モデル (A114-B)
    - 1000V、デバイス帯電モデル (C101)
- IEC 61000-4-2 ESD (B ポート)
  - 接触放電 ±8kV
  - 空中放電 ±10kV

2 アプリケーション

- 車載インフォテイメント、先進運転支援システム (ADAS)
- メイン・プロセッサ・モジュールとペリフェラル・モジュールの間で絶縁とレベル変換を行います
- I^2C または 1 線式の電圧レベル変換



N チャネル・トランジスタの伝達特性

3 概要

TXS0104E-Q1 デバイスは、電圧ミスマッチのため、チップ間で互換性のないロジック通信を接続します。この自動方向トランスレータは、ホストからの方向制御を必要とせずに、ギャップをブリッジするために便利に使用できます。各チャネルは、ホストから介入せずに、さまざまな出力タイプ (オープン・ドレインまたはプッシュプル) および混在データ・フロー (送信または受信) と混在させ、一致させることができます。この 4 ビット非反転トランスレータは、設定可能な 2 本の独立した電源レールを使用します。A ポートおよび B ポートは、それぞれ V_{CCA} および V_{CCB} をトラッキングするように設計されています。V_{CCB} ピンは 2.3V～5.5V の電源電圧に対応し、V_{CCA} が V_{CCB} 以下になるように V_{CCA} ピンは 1.65V～3.6V の電源電圧に対応しています。このトラッキングにより、1.8V、2.5V、3.3V、5V いずれかの電圧ノード間で低電圧の双方向変換が可能になります。

出力イネーブル (OE) 入力が Low のとき、全出力が高インピーダンス状態になります。

TXS0104E-Q1 デバイスは、OE 入力回路が V_{CCA} によって給電されるように設計されています。

電源投入または電源切断時に高インピーダンス状態を保証するため、OE ピンはプルダウン抵抗経由で GND ピンに接続する必要があります。この抵抗の最小値は、ドライバの電流ソーシング能力によって決定されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TXS0104E-Q1	PW (TSSOP、14)	5mm × 6.4mm
	BQA (WQFN、14)	3mm × 2.5mm
	RUT (UQFN、12)	2mm × 1.7mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

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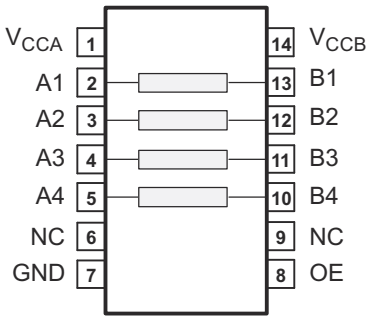
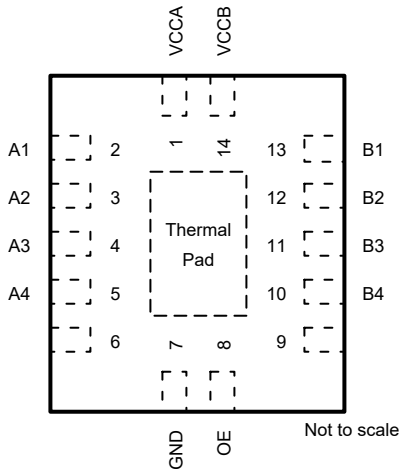
4 Pin Configuration and Functions



NC - No internal connection

図 4-1. PW Package, 14-Pin TSSOP (Top View)



NC - No internal connection

図 4-2. BQA Package, 14-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input-output 1 for the A port. This pin is referenced to V_{CCA}.
A2	3	I/O	Input-output 2 for the A port. This pin is referenced to V_{CCA}.
A3	4	I/O	Input-output 3 for the A port. This pin is referenced to V_{CCA}.
A4	5	I/O	Input-output 4 for the A port. This pin is referenced to V_{CCA}.
B1	13	I/O	Input-output 1 for the B port. This pin is referenced to V_{CCB}.
B2	12	I/O	Input-output 2 for the B port. This pin is referenced to V_{CCB}.
B3	11	I/O	Input-output 3 for the B port. This pin is referenced to V_{CCB}.
B4	10	I/O	Input-output 4 for the B port. This pin is referenced to V_{CCB}.
GND	7	—	Ground
NC	6	—	No connection
	9		
OE	8	I	Tri-state output-mode enable. Pull the OE pin low to place all outputs in tri-state mode. This pin is referenced to V_{CCA}.
V_{CCA}	1	I	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	I	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V.

(1) I = input, O = output

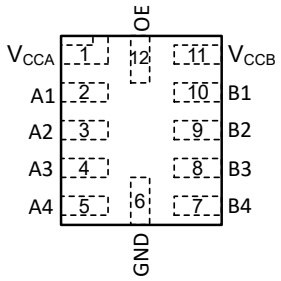


図 4-3. RUT Package, 12-Pin UQFN (Transparent Top View)

表 4-2. Pin Functions: RUT

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	10	I/O	Input/output B1. Referenced to V_{CCB}.
B2	9	I/O	Input/output B2. Referenced to V_{CCB}.
B3	8	I/O	Input/output B3. Referenced to V_{CCB}.
B4	7	I/O	Input/output B4. Referenced to V_{CCB}.
GND	6	—	Ground
OE	12	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	11	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_{CCA}		–0.5	4.6	V
	V_{CCB}		–0.5	6.5	
Input-output pin voltage, V_{IO} (2)	A1, A2, A3, A4	A port	–0.5	4.6	V
	B1, B2, B3, B4	B port	–0.5	6.5	
Output voltage, V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK}		V_I < 0		–50	mA
Output clamp current, I_{OK}		V_O < 0		–50	mA
Continuous output current, I_O				±50	mA
Continuous current through each V_{CCA}, V_{CCB}, or GND				±100	mA
Storage temperature range, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage(1)				1.65	3.6	V
V_{CCB}	Supply voltage(1)				2.3	5.5	
$V_{IH(Ax)}$	High-level input voltage	A-port I/Os	1.65 to 1.95 V	2.3 to 5.5 V	V_{CCA} – 0.2	V_{CCA}	V
			2.3 to 3.6 V		V_{CCA} – 0.4	V_{CCA}	
$V_{IH(Bx)}$	High-level input voltage	B-port I/Os	1.65 to 3.6 V	2.3 to 5.5 V	V_{CCB} – 0.4	V_{CCB}	
$V_{IH(OE)}$	High-level input voltage	OE input			V_{CCA} × 0.65	5.5	
$V_{IL(Ax)}$	Low-level input voltage	A-port I/Os	1.65 to 3.6 V	2.3 to 5.5 V	0	0.15	V
$V_{IL(Bx)}$	Low-level input voltage	B-port I/Os			0	0.15	
$V_{IL(OE)}$	Low-level input voltage	OE input			0	V_{CCA} × 0.35	
$\Delta t/\Delta v_{(Ax)}$	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 to 3.6 V	2.3 to 5.5 V		10	ns/V
$\Delta t/\Delta v_{(Bx)}$	Input transition rise or fall rate	B-port I/Os, push-pull driving				10	
$\Delta t/\Delta v_{(OE)}$	Input transition rise or fall rate	OE input				10	
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted) (1)

THERMAL METRIC(1)		TXS0104E-Q1			UNIT
		PW (TSSOP)	BQA (WQFN)	RUT (UQFN)	
		14 PINS	14 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	73.5	150.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.2	76.9	68.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	43.0	76.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	4.7	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.2	42.9	76.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	19.6	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
$V_{OH(Ax)}$	High-level output voltage, A port	I_{OH} = –20 µA, $V_{I(Bx)} \geq V_{CCB} - 0.4$ V	1.65 to 3.6 V	2.3 to 5.5 V	$V_{CCA} \times 0.75$			V
$V_{OL(Ax)}$	Low-level output voltage, A port	I_{OL} = 1 mA, $V_{I(Bx)} \leq 0.15$ V	1.65 to 3.6 V	2.3 to 5.5 V			0.4	V
$V_{OH(Bx)}$	High-level output voltage, B port	I_{OH} = –20 µA, $V_{I(Ax)} \geq V_{CCA} - 0.2$ V	1.65 to 3.6 V	2.3 to 5.5 V	$V_{CCB} \times 0.75$			V
$V_{OL(Bx)}$	Low-level output voltage, B port	I_{OL} = 1 mA, $V_{I(Ax)} \leq 0.15$ V	1.65 to 3.6 V	2.3 to 5.5 V			0.4	V
$I_{I(OE)}$	Input current, OE	$V_I = V_{CCI}$ or GND	1.65 to 3.6 V	2.3 to 5.5 V			±2	µA
		$V_I = V_{CCI}$ or GND, T_A = 25°C					±1	
I_{OZ}	Off-state output current, A or B port	OE = V_{IL}	1.65 to 3.6 V	2.3 to 5.5 V			±3	µA
		OE = V_{IL}, T_A = 25°C					±1	
I_{CCA}	Supply current, A port	$V_I = V_O$ = Open, I_O = 0	1.65 to V_{CCB}	2.3 to 5.5 V			4	µA
			3.6 V	0			2.2	
			0	5.5 V			–1	
I_{CCB}	Supply current, B port	$V_I = V_O$ = Open, I_O = 0	1.65 to V_{CCB}	2.3 to 5.5 V			21	µA
			3.6 V	0			–1	
			0	5.5 V			5	
$I_{CCA}+I_{CCB}$	Supply current, A port plus B port supply current	$V_I = V_O$ = Open, I_O = 0	1.65 V to V_{CCB}	2.3 to 5.5 V			25	µA
$C_{I(OE)}$	Input capacitance, OE		3.3 V	3.3 V			4	pF
		T_A = 25°C				2.5		
$C_{IO(Ax)}$	Input-output capacitance, A port		3.3 V	3.3 V			6.5	pF
		T_A = 25°C				5		
$C_{IO(Bx)}$	Input-output capacitance, B port						16.5	
		T_A = 25°C				12		

(1) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

5.6 Timing Requirements—V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		18	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		21	
			V_{CCB} = 5 V ± 0.5 V		23	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, data inputs See 図 6-4	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	55		ns
			V_{CCB} = 3.3 V ± 0.3 V	47		
			V_{CCB} = 5 V ± 0.5 V	43		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	500		
			V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

5.7 Timing Requirements—V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		20	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		22	
			V_{CCB} = 5 V ± 0.5 V		24	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, data inputs See 図 6-4	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	50		ns
			V_{CCB} = 3.3 V ± 0.3 V	45		
			V_{CCB} = 5 V ± 0.5 V	41		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	500		
			V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

5.8 Timing Requirements—V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		22	Mbps
			V_{CCB} = 5 V ± 0.5 V		24	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, Data inputs See 図 6-4	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	45		ns
			V_{CCB} = 5 V ± 0.5 V	41		
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

5.9 Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		6	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.8	
			V_{CCB} = 5 V ± 0.5 V		5.8	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		8.8	
			V_{CCB} = 3.3 V ± 0.3 V		9.6	
			V_{CCB} = 5 V ± 0.5 V		10	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		4.4	
			V_{CCB} = 3.3 V ± 0.3 V		4.5	
			V_{CCB} = 5 V ± 0.5 V		4.7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		5.3	
			V_{CCB} = 3.3 V ± 0.3 V		4.4	
			V_{CCB} = 5 V ± 0.5 V		4	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.7	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.8	
			V_{CCB} = 5 V ± 0.5 V		7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		50	
			V_{CCB} = 3.3 V ± 0.3 V		26	
			V_{CCB} = 5 V ± 0.5 V		33	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.3	
			V_{CCB} = 3.3 V ± 0.3 V		4.5	
			V_{CCB} = 5 V ± 0.5 V		0.5	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		36	
			V_{CCB} = 3.3 V ± 0.3 V		16	
			V_{CCB} = 5 V ± 0.5 V		20	
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from *OE* (input) to *A* or *B* (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time, from *OE* (input) to *A* or *B* (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		9.5	ns
			V_{CCB} = 3.3 V ± 0.3 V		9.3	
			V_{CCB} = 5 V ± 0.5 V		15	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	38	199	
			V_{CCB} = 3.3 V ± 0.3 V	30	150	
			V_{CCB} = 5 V ± 0.5 V	22	109	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		10.8	ns
			V_{CCB} = 3.3 V ± 0.3 V		9.1	
			V_{CCB} = 5 V ± 0.5 V		7.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	34	186	
			V_{CCB} = 3.3 V ± 0.3 V	23	112	
			V_{CCB} = 5 V ± 0.5 V	10	58	

5.9 Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.9	ns
			V_{CCB} = 3.3 V ± 0.3 V		6	
			V_{CCB} = 5 V ± 0.5 V		13.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		6.9	
			V_{CCB} = 3.3 V ± 0.3 V		6.4	
			V_{CCB} = 5 V ± 0.5 V		6.1	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.6	
			V_{CCB} = 3.3 V ± 0.3 V		7.5	
			V_{CCB} = 5 V ± 0.5 V		8.8	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		13.8	
			V_{CCB} = 3.3 V ± 0.3 V		16.2	
			V_{CCB} = 5 V ± 0.5 V		16.2	
t_{sk}	Channel-to-channel skew	V_{CCB} = 2.5 V ± 0.2 V			1	ns
		V_{CCB} = 3.3 V ± 0.3 V			1	
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		18	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		21	
			V_{CCB} = 5 V ± 0.5 V		23	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	

5.10 Switching Characteristics—V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.2	ns
			V_{CCB} = 3.3 V ± 0.3 V		3.3	
			V_{CCB} = 5 V ± 0.5 V		3.4	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		6.3	
			V_{CCB} = 3.3 V ± 0.3 V		6	
			V_{CCB} = 5 V ± 0.5 V		5.8	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3	
			V_{CCB} = 3.3 V ± 0.3 V		3.6	
			V_{CCB} = 5 V ± 0.5 V		4.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		4.7	
			V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.5	ns
			V_{CCB} = 3.3 V ± 0.3 V		4.1	
			V_{CCB} = 5 V ± 0.5 V		4.4	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		3.5	
			V_{CCB} = 3.3 V ± 0.3 V		4.1	
			V_{CCB} = 5 V ± 0.5 V		4.4	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		2.5	
			V_{CCB} = 3.3 V ± 0.3 V		1.6	
			V_{CCB} = 5 V ± 0.5 V		0.7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2.5	
			V_{CCB} = 3.3 V ± 0.3 V		1.6	
			V_{CCB} = 5 V ± 0.5 V		1	
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from *OE* (input) to *A* or *B* (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time, from *OE* (input) to *A* or *B* (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.4	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.6	
			V_{CCB} = 5 V ± 0.5 V		5.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	34	180	
			V_{CCB} = 3.3 V ± 0.3 V	28	150	
			V_{CCB} = 5 V ± 0.5 V	24	105	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		8.3	ns
			V_{CCB} = 3.3 V ± 0.3 V		7.2	
			V_{CCB} = 5 V ± 0.5 V		6.1	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	35	170	
			V_{CCB} = 3.3 V ± 0.3 V	24	120	
			V_{CCB} = 5 V ± 0.5 V	12	64	

5.10 Switching Characteristics—V_{CCA} = 2.5 V ± 0.2 V (続き)

over recommended operating free-air temperature range (unless otherwise noted)

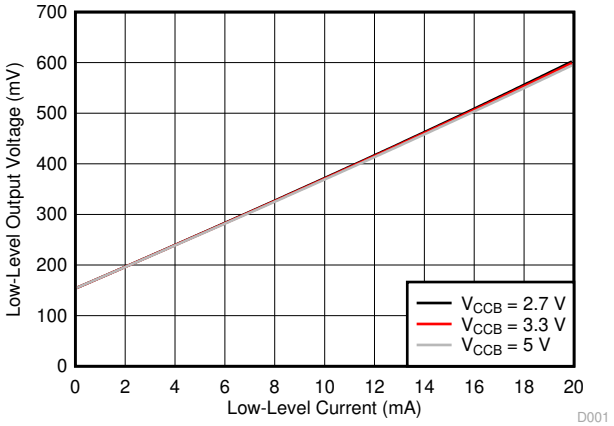
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.7	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.5	
			V_{CCB} = 5 V ± 0.5 V		5.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V			
			V_{CCB} = 3.3 V ± 0.3 V			
			V_{CCB} = 5 V ± 0.5 V		5.8	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.8	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.7	
			V_{CCB} = 5 V ± 0.5 V		6.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		8.8	
			V_{CCB} = 3.3 V ± 0.3 V		9.4	
			V_{CCB} = 5 V ± 0.5 V		10.4	
t_{sk}	Channel-to-channel skew	V_{CCB} = 2.5 V ± 0.2 V			1	ns
		V_{CCB} = 3.3 V ± 0.3 V			1	
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	20		Mbps
			V_{CCB} = 3.3 V ± 0.3 V	22		
			V_{CCB} = 5 V ± 0.5 V	24		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	2		
			V_{CCB} = 3.3 V ± 0.3 V	2		
			V_{CCB} = 5 V ± 0.5 V	2		

5.11 Switching Characteristics—V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

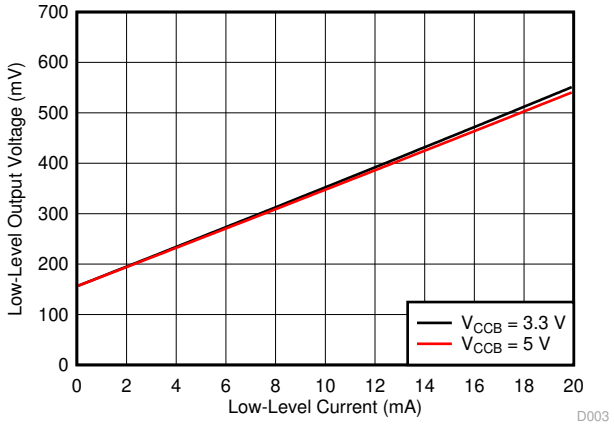
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.4	ns
			V_{CCB} = 5 V ± 0.5 V		3.1	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4.6	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		3.3	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		124	
			V_{CCB} = 5 V ± 0.5 V		97	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from *A* (input) to *B* (output) See 図 6-5	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	ns
			V_{CCB} = 5 V ± 0.5 V		4.4	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4.4	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from *B* (input) to *A* (output) See 図 6-5	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		2.6	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		3.3	
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from *OE* (input) to *A* or *B* (output)	V_{CCB} = 3.3 V ± 0.3 V			200	ns
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time,from *OE* (input) to *A* or *B* (output)	V_{CCB} = 3.3 V ± 0.3 V			200	ns
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		5.6	ns
			V_{CCB} = 5 V ± 0.5 V		5	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	25	140	
			V_{CCB} = 5 V ± 0.5 V	19	102	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		6.4	ns
			V_{CCB} = 5 V ± 0.5 V		7.4	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	26	130	
			V_{CCB} = 5 V ± 0.5 V	14	75	
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		5.4	ns
			V_{CCB} = 5 V ± 0.5 V		5	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		6.1	
			V_{CCB} = 5 V ± 0.5 V		5.7	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		7.4	ns
			V_{CCB} = 5 V ± 0.5 V		7.6	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		7.6	
			V_{CCB} = 5 V ± 0.5 V		8.3	
t_{sk}	Channel-to-channel skew	V_{CCB} = 3.3 V ± 0.3 V			1	ns
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	22		Mbps
			V_{CCB} = 5 V ± 0.5 V	24		
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	2		
			V_{CCB} = 5 V ± 0.5 V	2		

5.12 Typical Characteristics



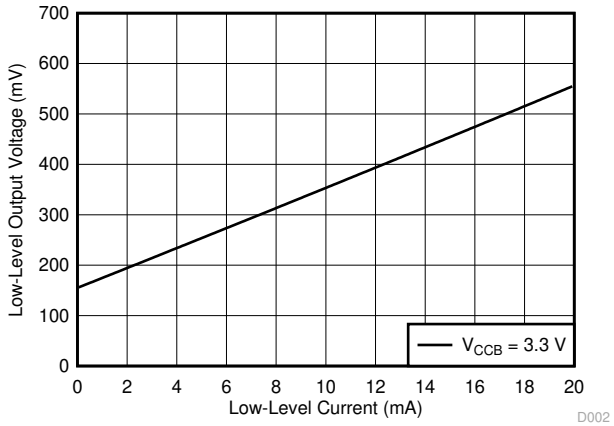
V_{CCA} = 1.8 V $V_{IL(A)}$ = 150 mV

図 5-1. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)



V_{CCA} = 2.7 V $V_{IL(A)}$ = 150 mV

図 5-2. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)



V_{CCA} = 3.3 V $V_{IL(A)}$ = 150 mV

図 5-3. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

6 Parameter Measurement Information

6.1 Load Circuits

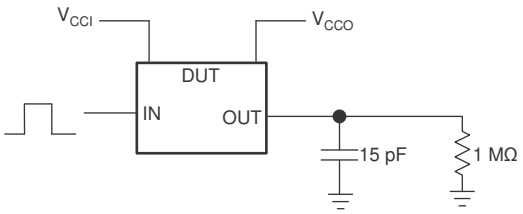


図 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

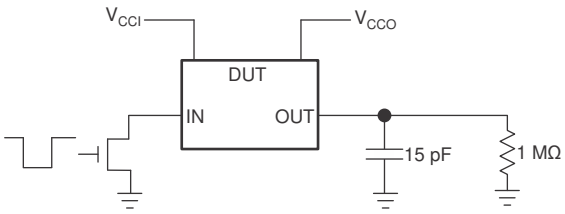
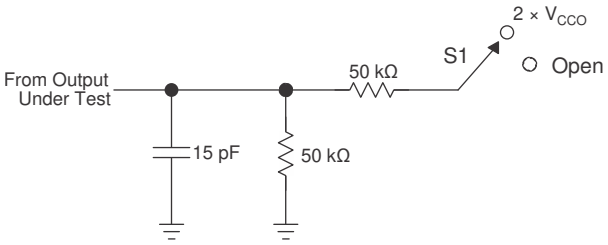


図 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

図 6-3. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

6.2 Voltage Waveforms

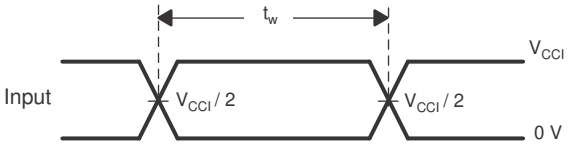


図 6-4. Pulse Duration

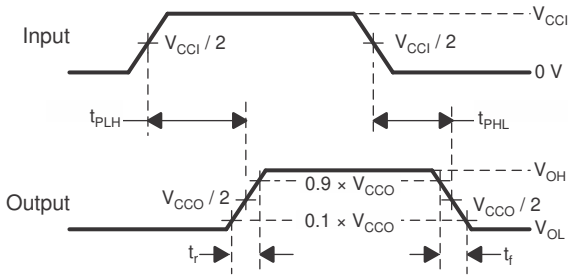
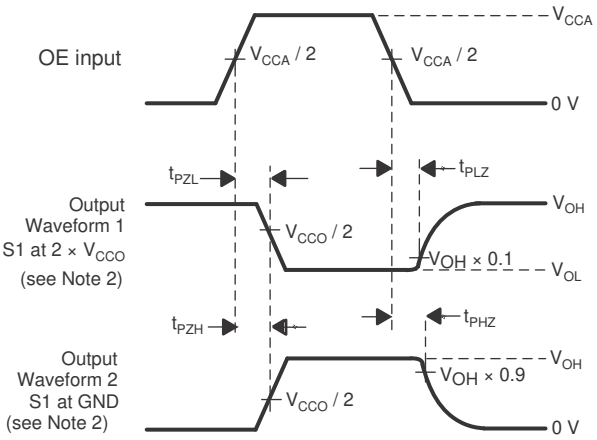


図 6-5. Propagation Delay Times



1. C_L includes probe and jig capacitance.
2. Waveform 1 in 図 6-6 is for an output with internal such that the output is high, except when OE is high (see 図 6-3). Waveform 2 in 図 6-6 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

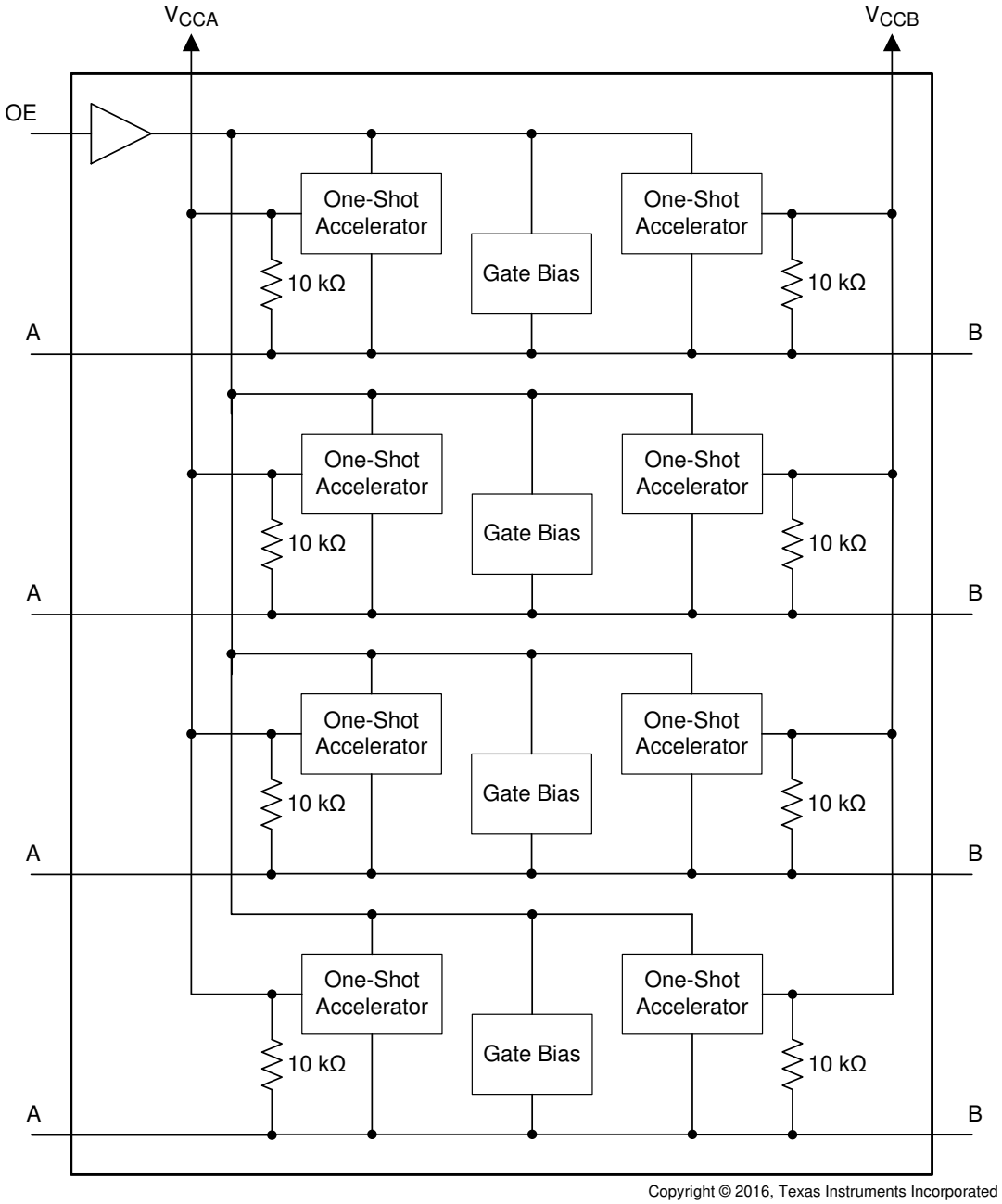
図 6-6. Enable and Disable Times

7 Detailed Description

7.1 Overview

The TXS0104E-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0104E-Q1 architecture (see 図 7-1) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

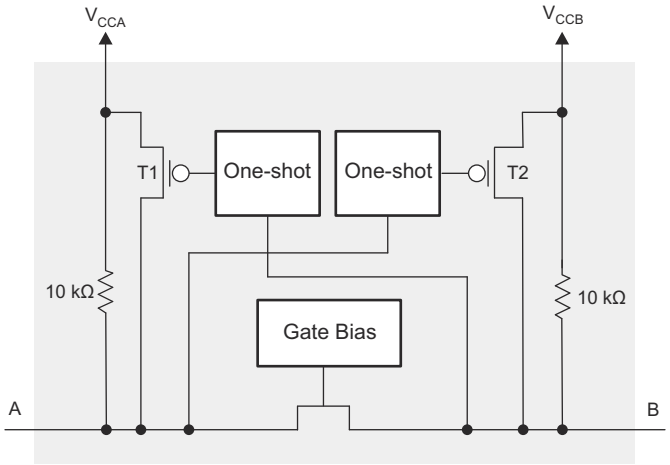


図 7-1. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

7.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104E-Q1 device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

7.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

7.3.4 Enable and Disable

The TXS0104E-Q1 device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

7.3.5 Pull Up and Pull Down Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors).

7.4 Device Functional Modes

The TXS0104E-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TXS0104E-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104E-Q1 device is optimal for use in applications where an open-drain driver is connected to the data I/Os. The TXS0104E-Q1 device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104-Q1 device might be a better option for such push-pull applications.

8.2 Typical Application

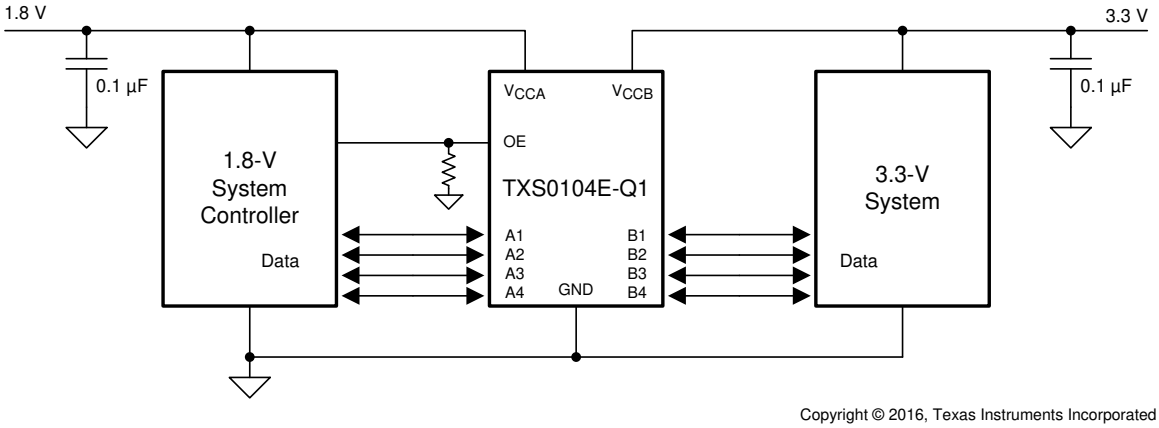


図 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0104E-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0104E-Q1 device is driving to determine the output voltage range.
  - The TXS0104E-Q1 device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use 式 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \quad (1)$$

where

- V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor

8.2.3 Application Curve

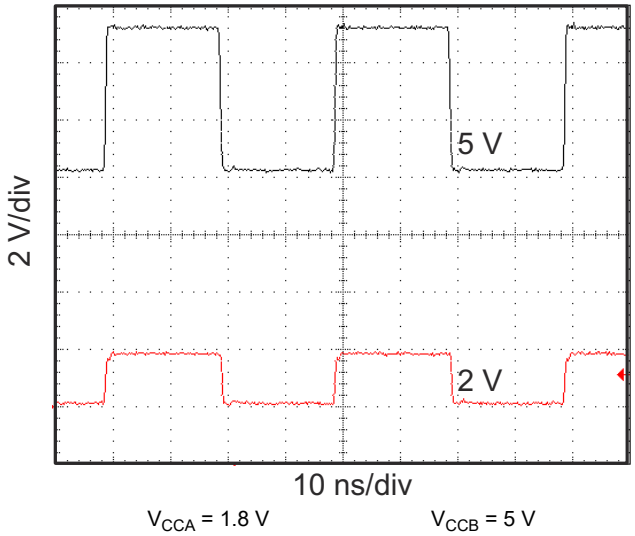


図 8-2. Level-Translation of a 2.5-MHz Signal

8.3 Power Supply Recommendations

The TXS0104E-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V and V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The TXS0104E-Q1 device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To enable the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull down resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pull down resistor to ground is determined by the current-sourcing capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

8.4.2 Layout Example

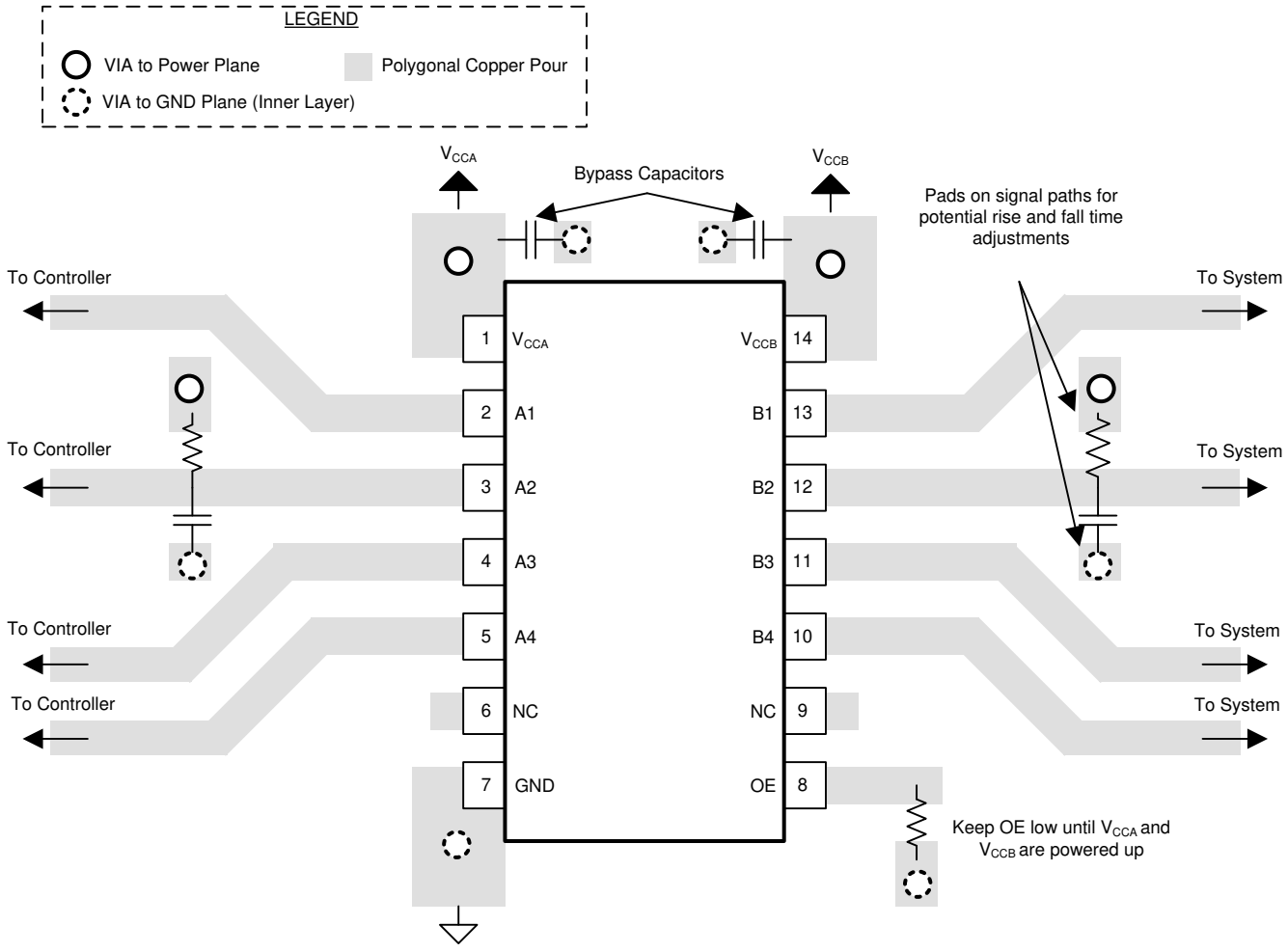


図 8-3. TXS0104E-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Introduction to Logic* application note

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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10 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2023) to Revision F (October 2024)	Page
• Updated thermal values for new packages	6

Changes from Revision D (January 2017) to Revision E (October 2023)	Page
• データシートに RUT パッケージ情報を追加	1

Changes from Revision C (January 2017) to Revision D (June 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• データシートに BQA パッケージ情報を追加	1

Changes from Revision B (May 2014) to Revision C (January 2017)	Page
• Changed the type of the OE pin from output (O) to input (I) in the *Pin Functions* table	3
• Moved T_{stg} back to the *Absolute Maximum Ratings* table and changed the *Handling Ratings* table to *ESD Ratings*	5

Changes from Revision A (April 2014) to Revision B (May 2014)	Page
• デバイスのステータスを「製品プレビュー」から「量産データ」へ変更	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0104EQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	04EQ1
TXS0104EQPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	04EQ1
TXS0104EQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	04EQ1
TXS0104EQRUTRQ1	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1RQ
TXS0104EQRUTRQ1.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1RQ
TXS0104EQWBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF04EQ
TXS0104EQWBQARQ1.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF04EQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TXS0104E-Q1 :

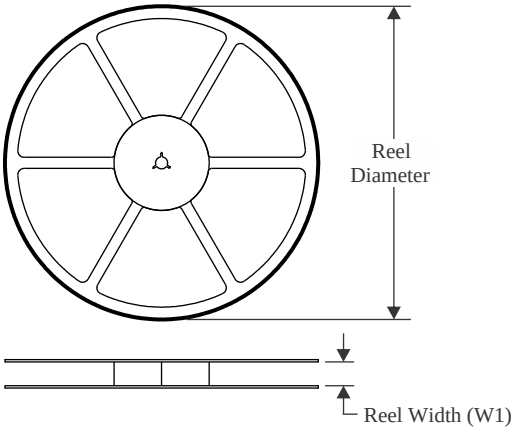
- Catalog : TXS0104E

NOTE: Qualified Version Definitions:

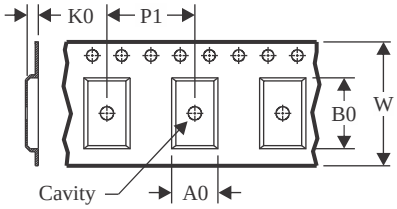
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

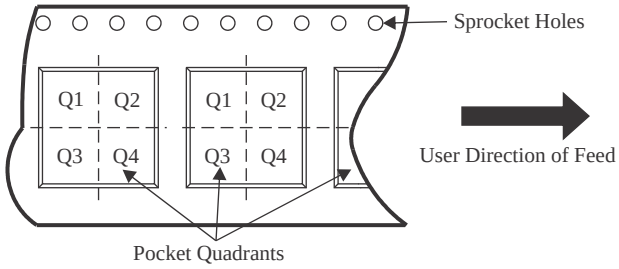


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

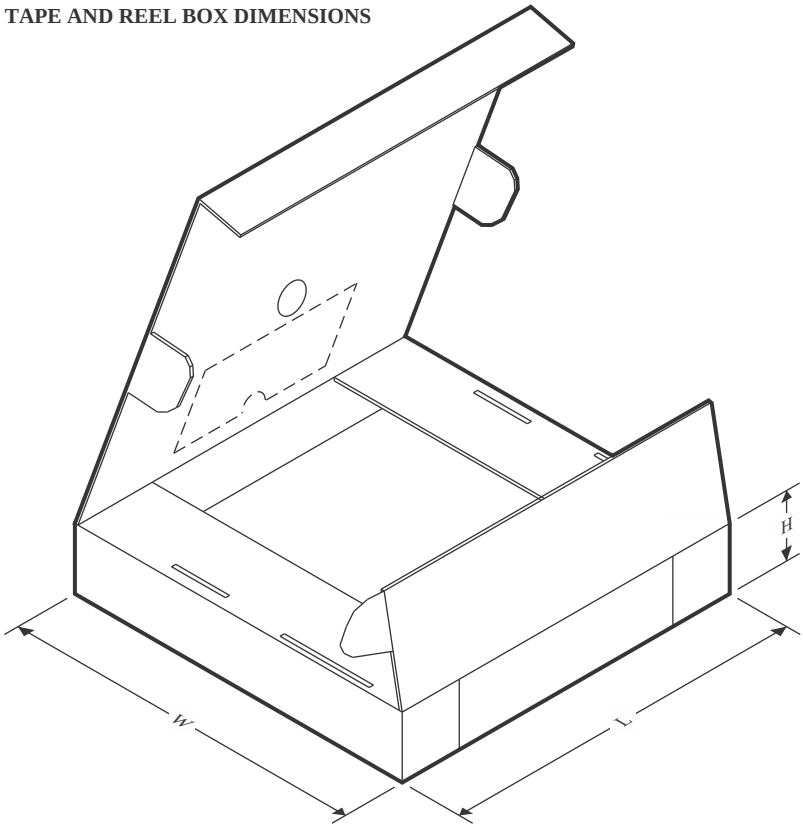
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104EQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXS0104EQRUTRQ1	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1
TXS0104EQWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104EQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
TXS0104EQRUTRQ1	UQFN	RUT	12	3000	210.0	185.0	35.0
TXS0104EQWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

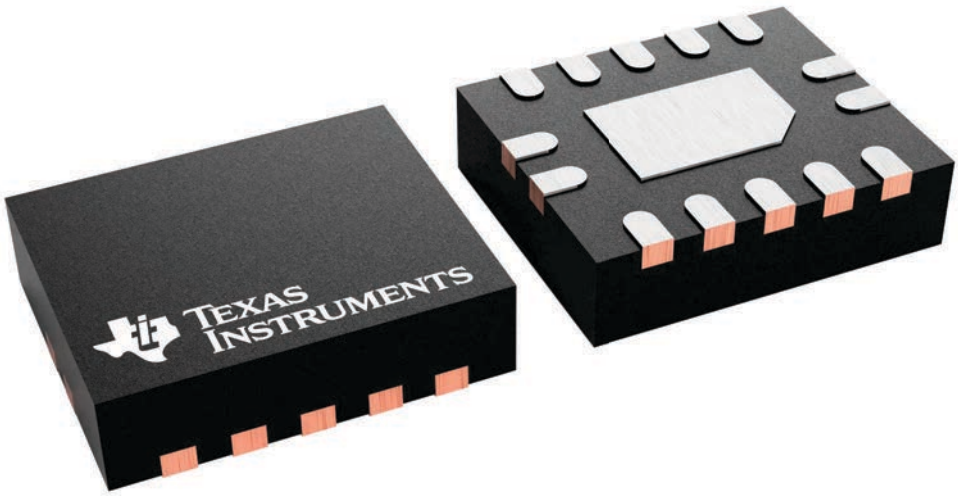
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

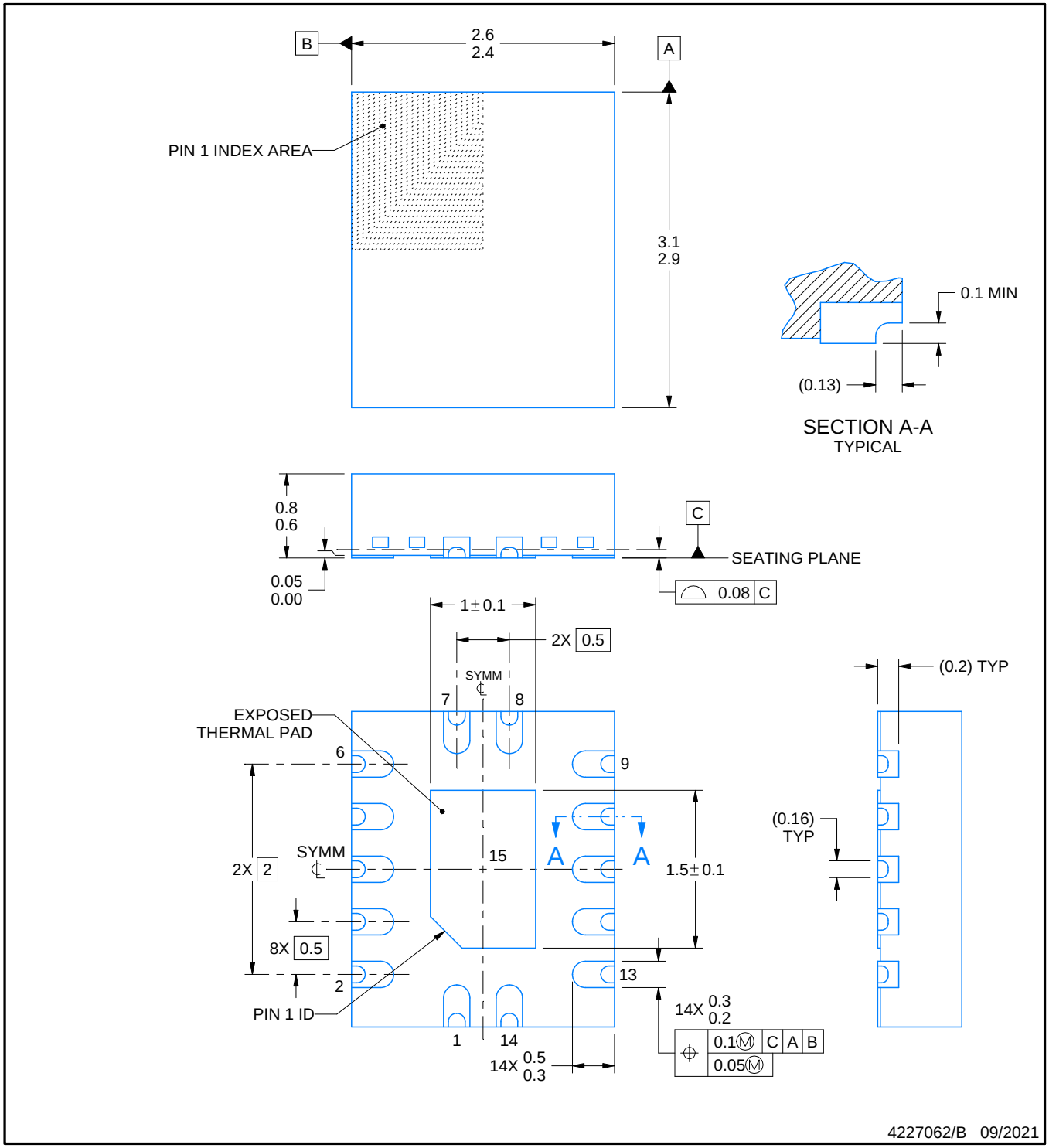


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

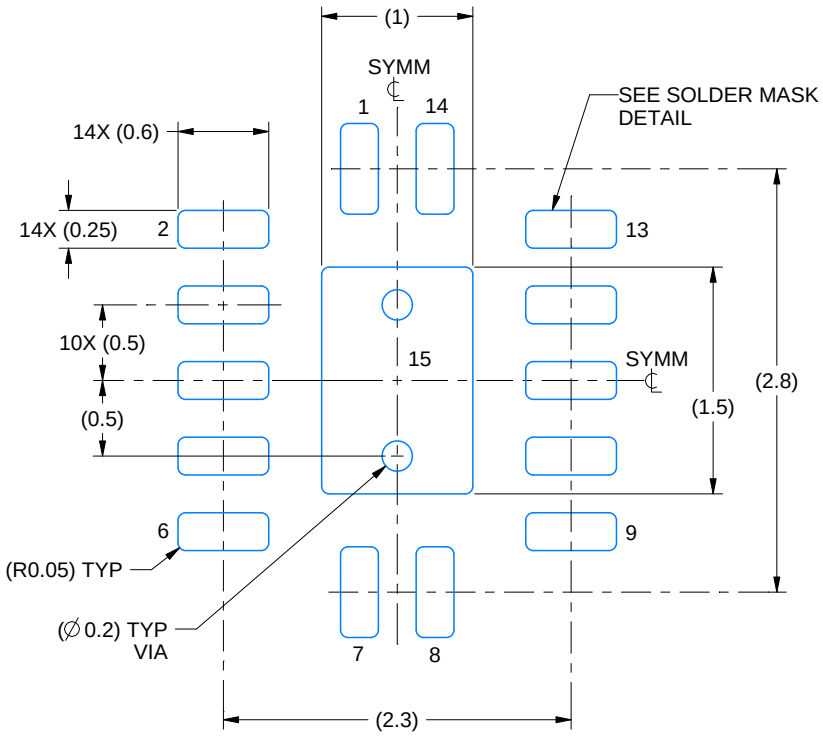
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

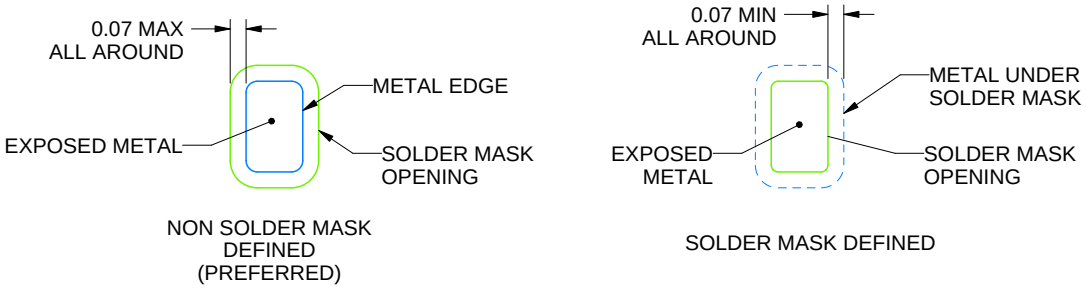
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

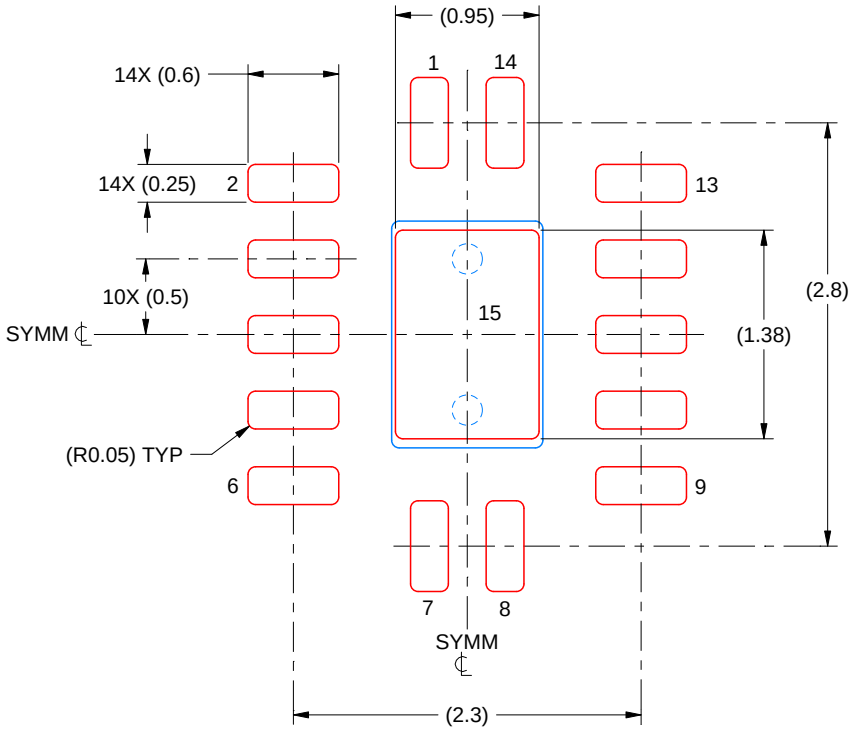


SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

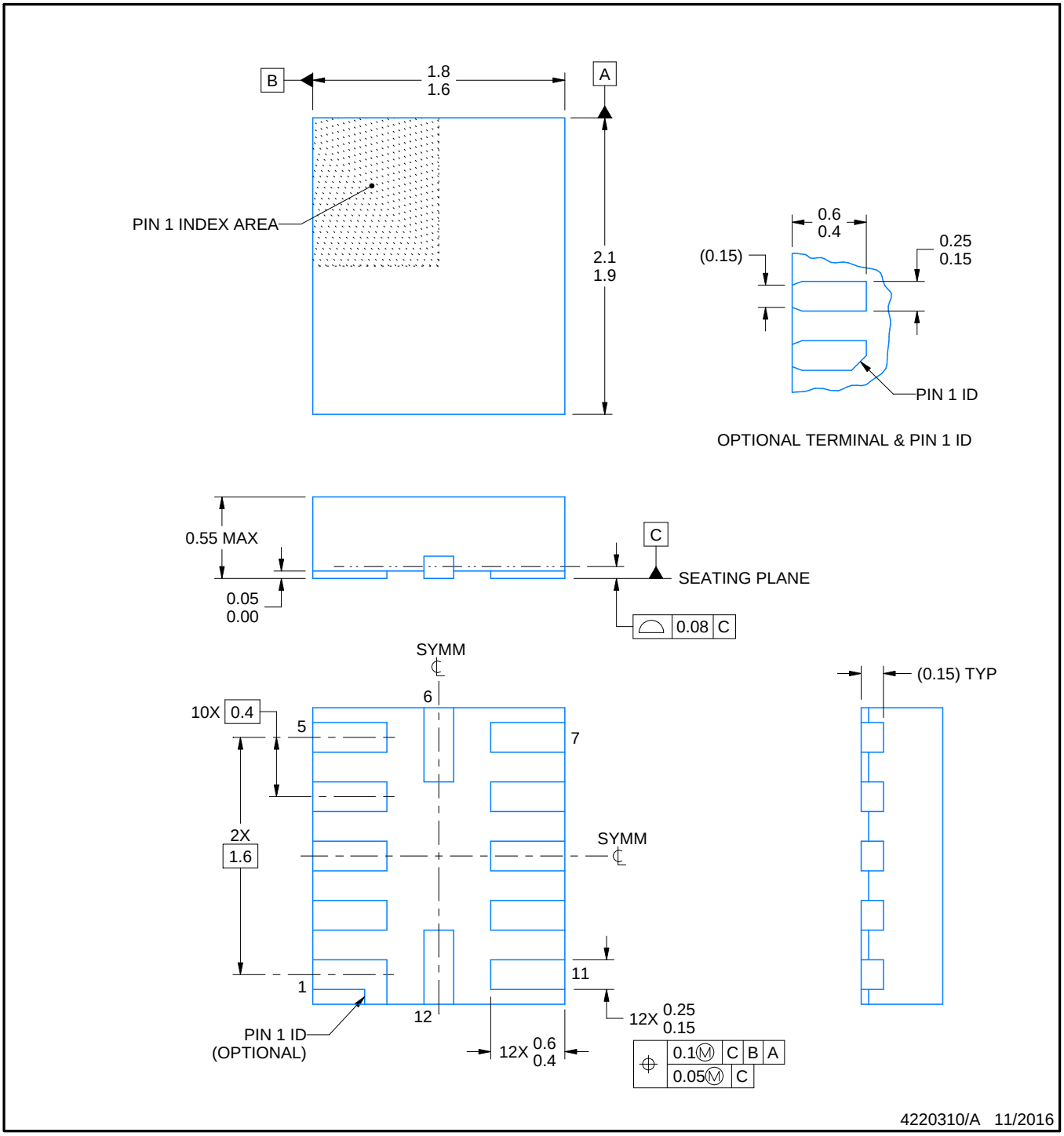
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUT0012A

PACKAGE OUTLINE

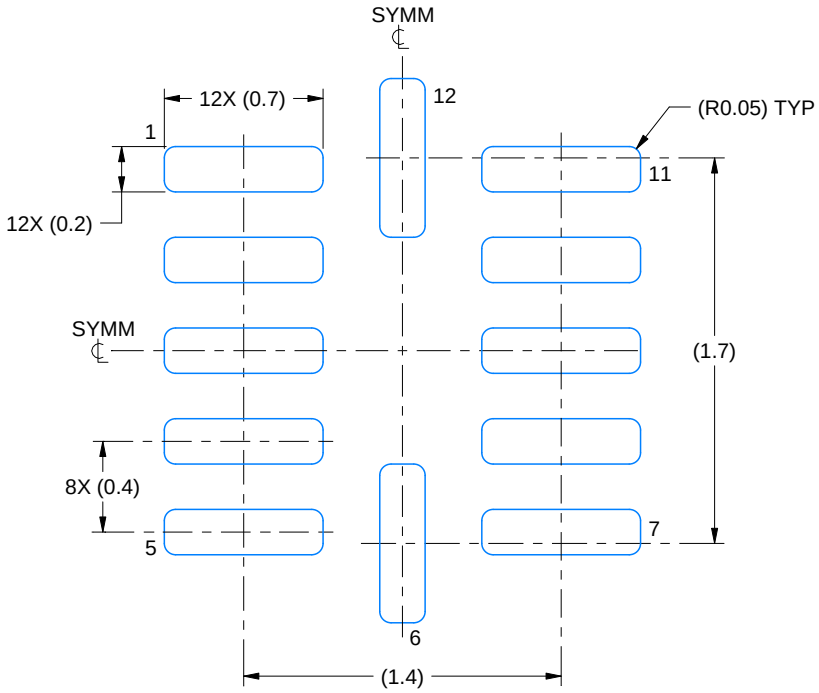
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

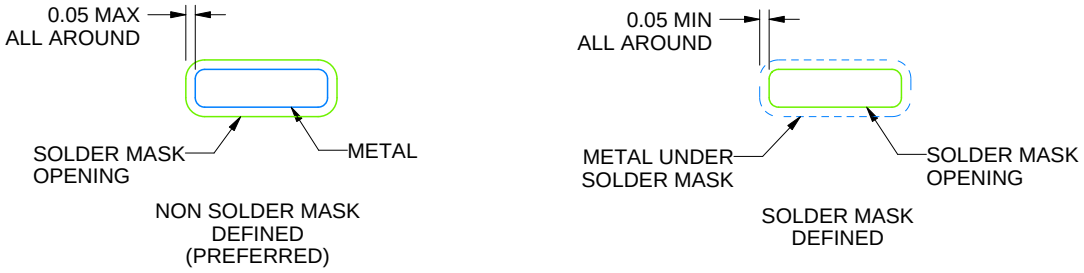


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

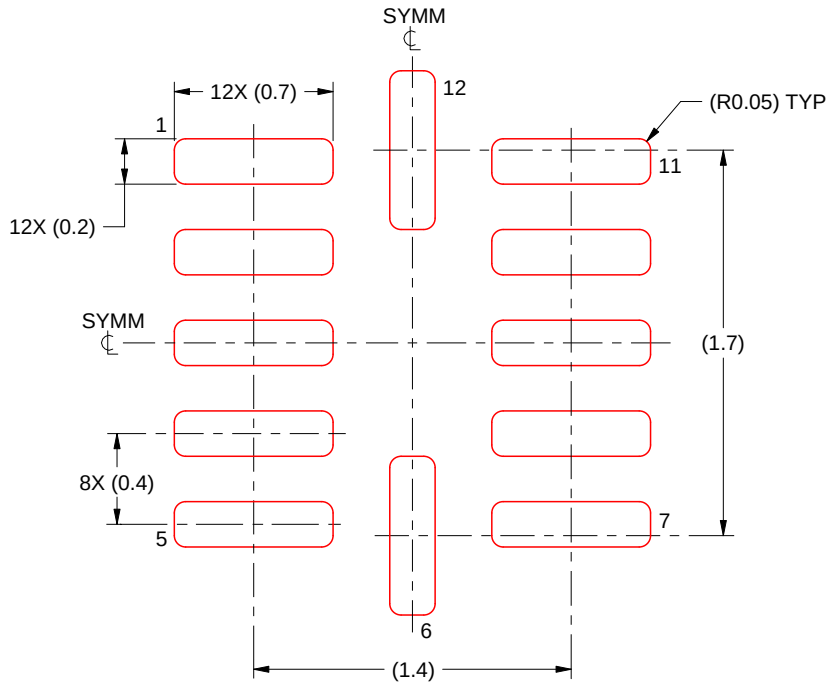


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

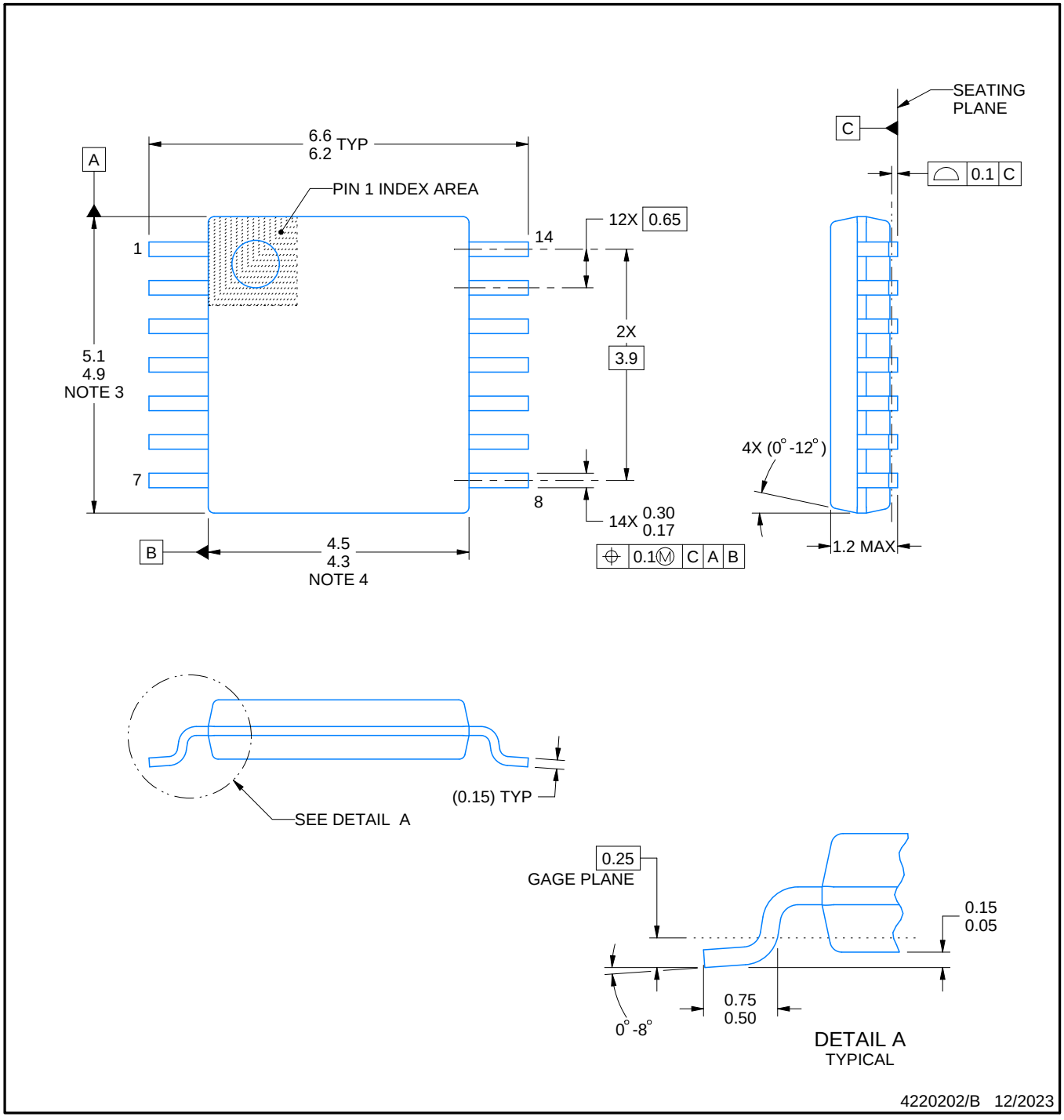
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

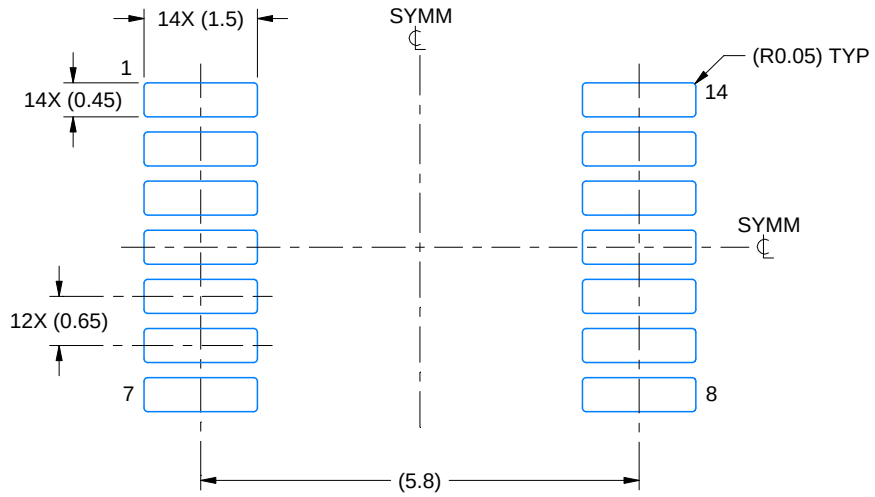
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

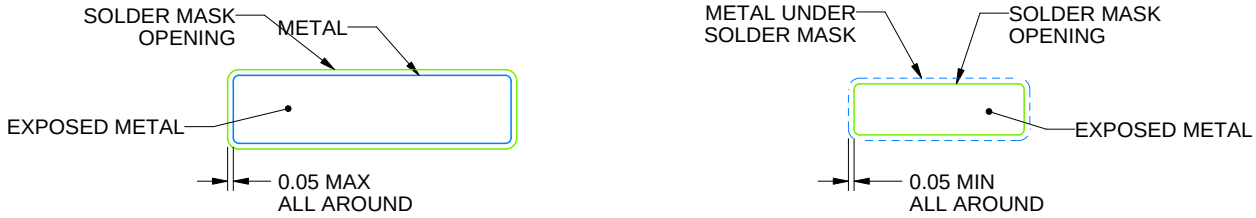


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

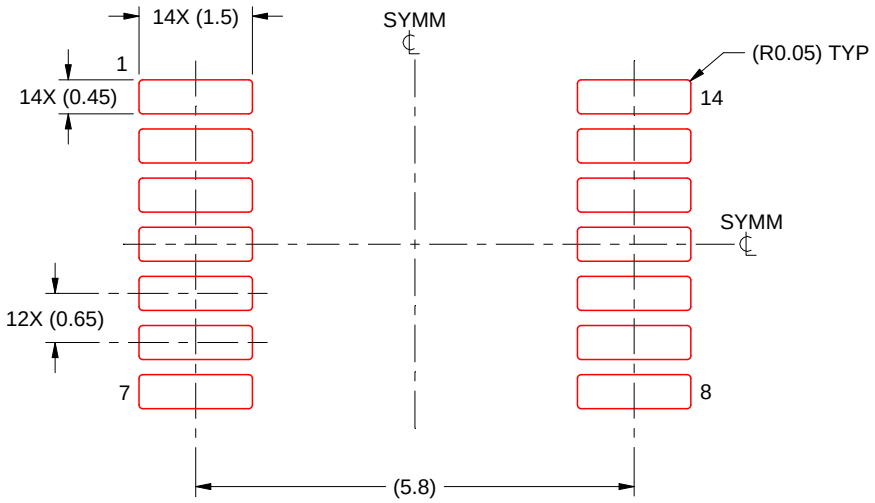


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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