TEXAS INSTRUMENTS
TVS1401
JAJSGA7B – SEPTEMBER 2018 – REVISED NOVEMBER 2021

TVS1401 14V 双方向フラット・クランプ・サージ保護デバイス

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 産業用信号ライン向け 1kV、42Ω の IEC 61000-4-5 サージ・テストに耐える保護機能
- 双方向極性によりバイポーラ信号や誤配線に対して保護
- クランプ電圧:20.5V (サージ電流 30A (8/20µs) 時)
- スタンドオフ電圧:±14V
- 小型の 3mm × 3mm SON フットプリント
- 125℃ で 30A のサージ電流 (8/20µs) の反復ストライクを 5,000 回以上吸収
- 強力なサージ保護
  - IEC61000-4-5 (8/20µs):30A
  - IEC61643-321 (10/1000µs):6A
- 低いリーク電流
  - 27℃ で 1.1nA (標準値)
  - 85℃ で 260nA (最大値)
- 低い静電容量:68pF
- レベル 4 IEC 61000-4-2 に準拠した ESD 保護機能を内蔵

2 アプリケーション

- 産業用センサ I/O
- ソリッド・ステート・ドライブ
- モータ・ドライブ
- 12V 電源ライン
- 家電製品
- 医療用機器
- 電力網の保護および制御

3 概要

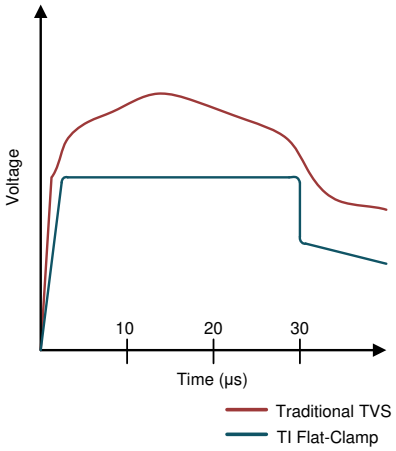
TVS1401 デバイスは、最大 30A の IEC 61000-4-5 フォルト電流をシャントし、大電力の過渡現象や落雷からシステムを保護します。このデバイスは、42Ω のインピーダンスで結合した 1kV IEC 61000-4-5 開路電圧の一般的な産業用信号線 EMC 要件に適合しています。TVS1401 は帰還機構を使用してフォルト中の正確なフラット・クランプを確保し、システムがさらされる電圧を従来の TVS ダイオードよりも低く保ちます。厳格な電圧レギュレーションにより、設計者は許容電圧が低いシステム部品でも安心して選択でき、堅牢性を損なうことなくシステムのコストと複雑性を低減できます。TVS1401 は ±14V の範囲で動作するため、逆配線に対する保護を必要とするシステムでの動作も可能です。

さらに、TVS1401 はスペースの制約が厳しいアプリケーション用に設計された小型の SON フットプリントで供給されるため、標準の SMA および SMB パッケージと比較して大幅なサイズ低減が可能です。デバイスのリーク電流と静電容量が小さいため、保護するラインへの影響も最小限に抑えられます。製品のライフサイクル全体にわたる堅牢な保護を確保するため、TI は TVS1401 のテストにおいて、125℃ で 5,000 回 の反復サージに対してデバイス性能に変化がないことを確認しています。

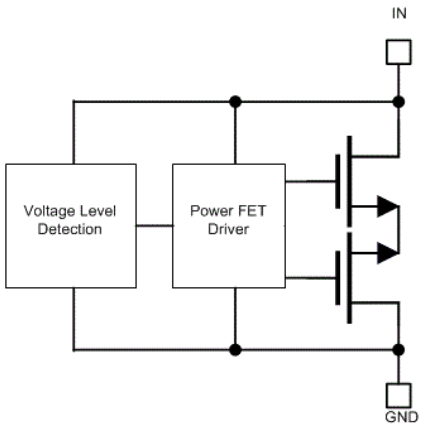
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TVS1401	SON (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



8/20µs のサージ・イベントに対する電圧クランプの応答



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2018) to Revision B (November 2021) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新.....1
- 「*特長*」セクションを更新し、機能安全対応の記述を追加.....1

Changes from Revision * (September 2018) to Revision A (December 2018) **Page**

- 事前情報から量産データに変更.....1

5 概要 (続き)

TVS1401 は TI のフラット・クランプ・ファミリのサージ・デバイスです。フラット・クランプ・ファミリの詳細については、『*Flat-Clamp Surge Protection Technology for Efficient System Protection*』(英語) ホワイト・ペーパーを参照してください。

6 Device Comparison Table

DEVICE	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	Leakage @ V_{rwm}	POLARITY	Package
TVS0500	5	9.2 V	43 A	0.07 nA	Unidirectional	DRV (SON-6)
TVS0701	7	11 V	30 A	0.25 nA	Bidirectional	DRB (SON-8)
TVS1400	14	18.6 V	43 A	2 nA	Unidirectional	DRV (SON-6)
TVS1401	14	20.5 V	30 A	1.1 nA	Bidirectional	DRB (SON-8)
TVS1800	18	22.8 V	40 A	0.3 nA	Unidirectional	DRV (SON-6)
TVS1801	18	27.4 V	30 A	0.4 nA	Bidirectional	DRB (SON-8)
TVS2200	22	27.7 V	40 A	3.2 nA	Unidirectional	DRV (SON-6)
TVS2201	22	29.6 V	30 A	2 nA	Bidirectional	DRB (SON-8)
TVS2700	27	32.5 V	40 A	1.7 nA	Unidirectional	DRV (SON-6)
TVS2701	27	34 V	27 A	0.8 nA	Bidirectional	DRB (SON-8)
TVS3300	33	38 V	35 A	19 nA	Unidirectional	DRV (SON-6), YZF (WCSP)
TVS3301	33	40 V	27 A	2.5 nA	Bidirectional	DRB (SON-8)

7 Pin Configuration and Functions

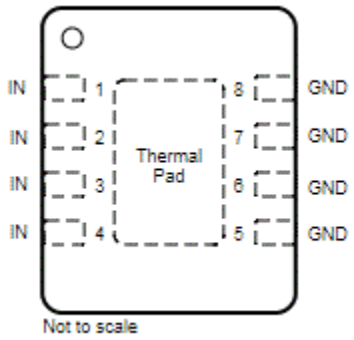


図 7-1. DRB Package
8-Pin SON
Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DRB		
FLOAT	Exposed Thermal Pad	NC	Exposed Thermal Pad Must Be Floating
GND	5, 6, 7, 8	GND	Ground
IN	1, 2, 3, 4	IN	Surge Protected Channel

8 Specifications

8.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs), T_A < 125°C		±30	A
	IEC 61000-4-5 Power (8/20 µs)		600	W
	IEC 61643-321 Current (10/1000 µs)		±6	A
	IEC 61643-321 Power (10/1000 µs)		120	W
EFT	IEC 61000-4-4 EFT Protection		±80	A
I_{BR}	DC Current		45	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8	kV
		IEC 61000-4-2 air-gap discharge	±15	

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-Off Voltage		±14		V

8.5 Thermal Information

THERMAL METRIC(1)		TVS1401 DRB (SON) 8 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	52.0	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	24.9	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Leakage Current	Measured at V_{IN} = ±V_{RWM}, T_A = 27°C		1.1	30	nA
		Measured at V_{IN} = ±V_{RWM}, T_A = 85°C			260	
V_{BR}	Break-down Voltage	I_{IN} = ±1mA	17.1	17.6		V
V_{CLAMP}	Clamp Voltage	±I_{pp} IEC 61000-4-5 Surge (8/20 µs), V_{IN} = 0 V before surge, T_A = 27°C		20.5	22.2	V
		±I_{PP} IEC 61000-4-5 Surge (8/20 µs), V_{IN} =±V_{RWM} before surge, T_A = 125°C			23.55	
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{PP} and I_{PP} surge current, T_A = 25°C		70		mΩ
C_{IN}	Input pin capacitance	V_{IN} = V_{RWM}, f = 1 MHz, 30 mV_{pp}, IO to GND		68		pF
SR	Maximum Slew Rate	0-±V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, T_A = 27°C		2.5		V/µs
		0-±V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, T_A = 85°C		1		

8.7 Typical Characteristics

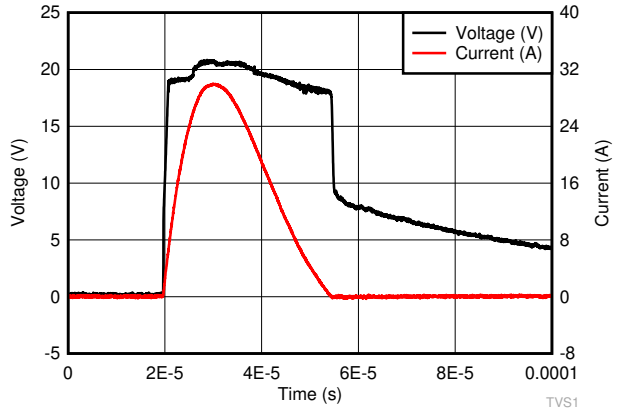


図 8-1. 8/20 µs Surge Response at 30 A

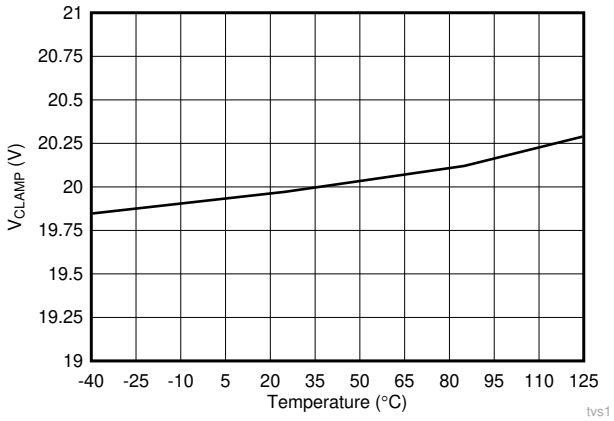
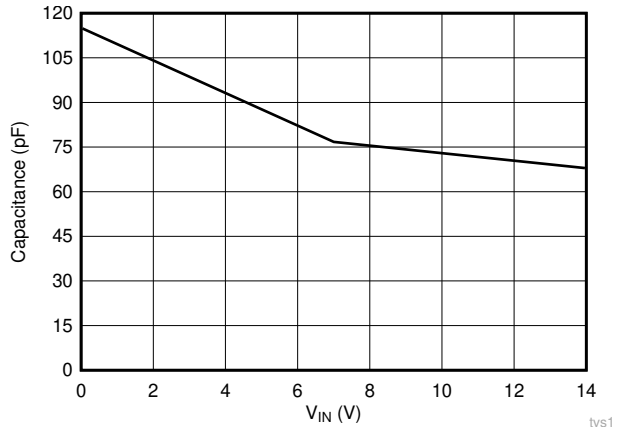


図 8-2. 8/20 µs Surge Clamping Response at 30 A



f = 1 MHz, 30 mVpp, IO to GND

図 8-3. Capacitance vs Voltage Bias

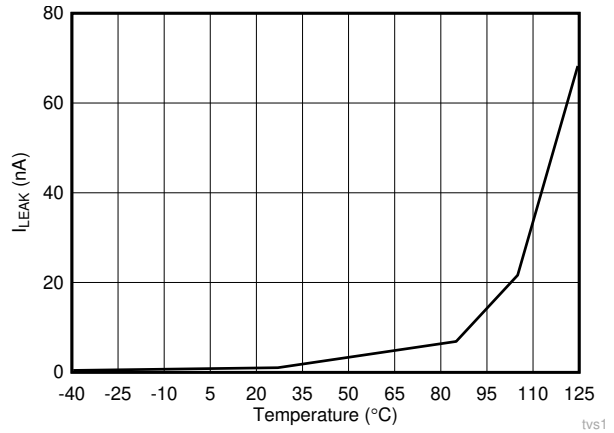


図 8-4. Leakage Current vs Temperature at ±14 V

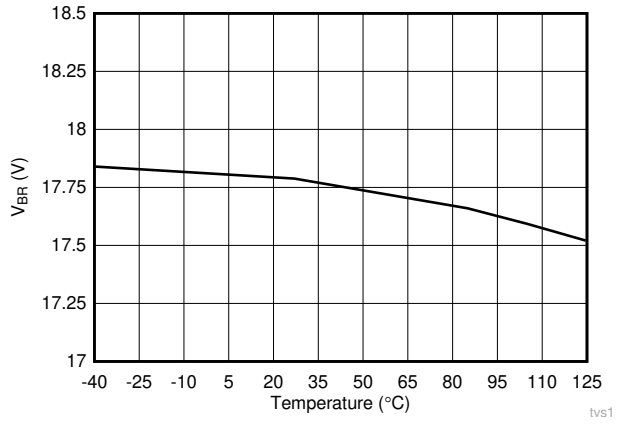


図 8-5. Breakdown Voltage (1 mA) vs Temperature

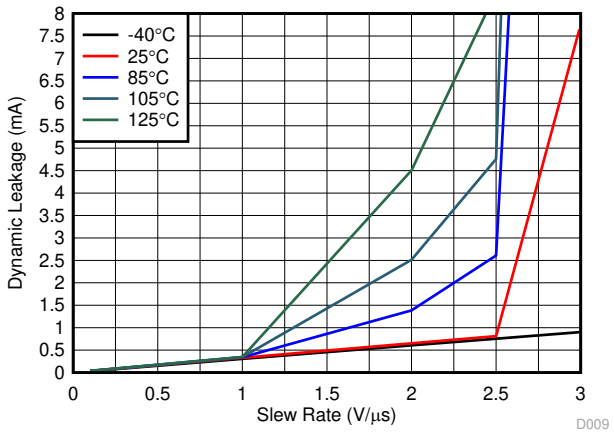


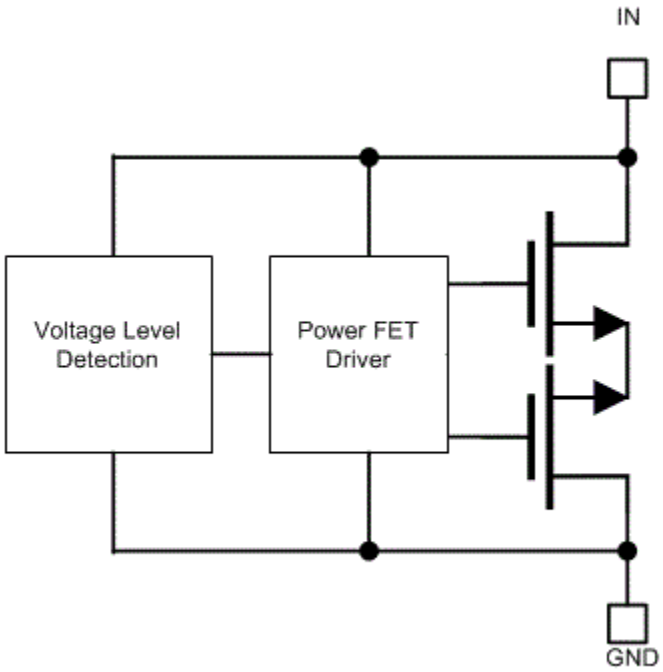
図 8-6. Dynamic Leakage vs Signal Slew Rate across Temperature

9 Detailed Description

9.1 Overview

The TVS1401 is a bidirectional precision clamp with two integrated FETs driven by a feedback loop to tightly regulate the input voltage during an overvoltage event. This feedback loop leads to a very low dynamic resistance, giving a flat clamping voltage during transient overvoltage events like a surge.

9.2 Functional Block Diagram



9.3 Feature Description

The TVS1401 is a precision clamp that handles ±30 A of IEC 61000-4-5 8/20 µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. This device provides a bidirectional operating range, with a symmetrical V_{RWM} of ±14 V, which is designed for applications that have bipolar input signals or that must withstand reverse wiring conditions. The TVS1401 has minimal leakage at V_{RWM} designed for applications where low leakage and power dissipation is a necessity. Built-in IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events, and the TVS1401 wide ambient temperature range of –40°C to +125°C enables usage in harsh industrial environments.

9.4 Device Functional Modes

9.4.1 Protection Specifications

The TVS1401 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required by relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 µs and a half-length of 20 µs, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half-length of 1000 µs.

The positive and negative surges are imposed to the TVS1401 by a combination wave generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered-on transient tests that need power supply bias, inductances are used to decouple the transient stress and protect the power supply. The TVS1401 is post-tested by assuring that there is no shift in device breakdown or leakage at V_{RWM}.

In addition, the TVS1401 has been tested according to IEC 61000-4-5 to pass a ±1-kV surge test through a 42-Ω coupling resistor and a 0.5-µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS1401 precision clamp can be used in applications that have that requirement.

The TVS1401 integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most common transient test requirements.

For more information on TI's test methods for Surge, ESD, and EFT testing, refer to the *TI's IEC 61000--4-x Tests for TI's Protection Devices* application report.

9.4.2 Reliability Testing

To ensure device reliability, the TVS1401 is characterized against 5,000 repetitive pulses of 25-A IEC 61000-4-5 8/20-µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst-case scenarios for fault regulation. After each surge pulse, the TVS1401 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS1401 enables fault protection in applications that must withstand years of continuous operation with no performance change.

9.4.3 Zero Derating

Unlike traditional diodes, the TVS1401 has zero derating of maximum power dissipation and ensures robust performance up to 125°C. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS1401 prevents this so the designer can see the surge protection regardless of temperature. Because of this, Flat-Clamp devices can provide robust protection against surge pulses that occur at high ambient temperatures, as shown in TI's *TVS Surge Protection in High-Temperature Environments* application report.

9.4.4 Bidirectional Operation

The TVS1401 is a bidirectional TVS with a symmetrical operating region. This allows for operation with positive and negative voltages, rather than just positive voltages like the unidirectional TVS1400. This allows for single chip protection for applications where the signal is expected to operate below 0 V or where there is a need to withstand a large common-mode voltage. In addition, in many cases, there is a system requirement to be able to withstand reverse wiring conditions, in many cases where a high voltage signal is accidentally applied to the system ground and a ground is accidentally applied to the input terminal. This causes a large reverse voltage on the TVS diode that the device must be able to withstand. The TVS1401 is designed to not break down or see failures under reverse wiring conditions for applications that must withstand these miswiring issues.

Note

If the applied signal is not expected to go below 0 V, an unidirectional device will clamp much lower in the reverse direction and should be used. In this case, the recommended device would be the TVS1400.

9.4.5 Transient Performance

During large transient swings, the TVS1401 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. To keep power dissipation low and remove the chance of signal distortion, TI recommends that the designer keep the slew rate of any input signal on the TVS1401 below 2.5 V/µs at room temperature and below 1 V/µs at 85°C as shown in 図 8-6. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however, it can cause device overheating if the fast input voltage swings occur regularly.

10 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The TVS1401 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

10.2 Typical Application

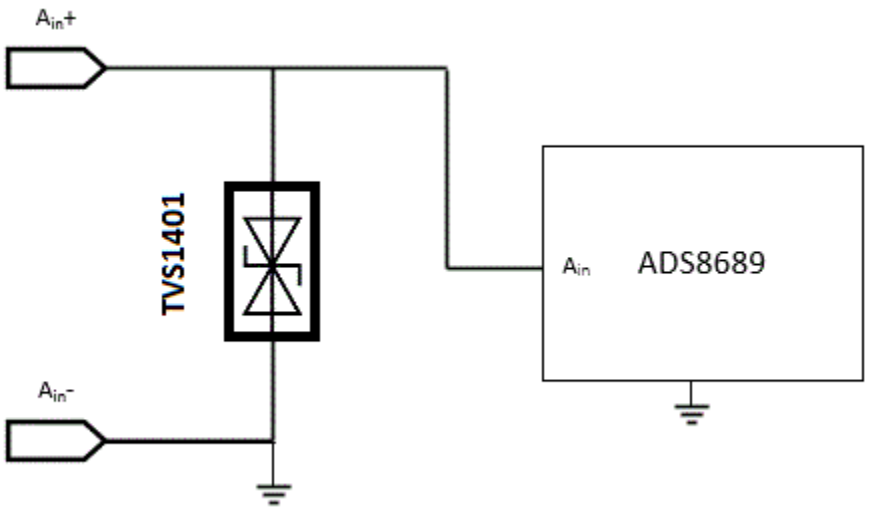


図 10-1. TVS1401 Application Schematic

10.2.1 Design Requirements

A typical operation for the TVS1401 would be protecting in a factory control application and protecting an analog input to an ADC input similar to 図 10-1. In this example, the TVS1401 is protecting the input to an ADS8689, an ADC with an input voltage range of ±12.288 V and an absolute maximum input voltage range of ±20 V. Without any input protection, this input voltage will rise to hundreds of volts for multiple microseconds, and violate the absolute maximum input voltage and harm the device if a surge event is caused by lightning, coupling, ringing, or any other fault condition. TI's Flat-Clamp technology provides surge protection diodes that can maximize the useable voltage range at a safe level for the system.

10.2.2 Detailed Design Procedure

If the TVS1401 is in place to protect the device, the voltage will rise to the breakdown of the diode at 17.6 V during a surge event. The TVS0701 will then turn on to shunt the surge current to ground. With the low dynamic resistance of the TVS1401, large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS1401 is around 70 mΩ, which means a 25-A surge current will cause a voltage raise of 25 A × 70 mΩ = 1.75 V. Because the device turns on at 17.6 V, this means the ADC input will be exposed to a maximum of 17.6 V + 1.75 V = 19.35 V during surge pulses, well within the ADS8689 absolute maximum to ensure robust protection of the circuit. The same magnitude of voltage will be seen during a negative pulse, still safely protecting the system.

In addition, the low leakage and capacitance of the TVS1401 assures low input distortion. At 14 V, giving margin on the ±12.288 V range of the ADS8689, the device will see typical 1.1-nA leakage, which will have minimal

effect on the overall system. The TVS1401 low capacitance of 68 pF will also cause less effect on signal integrity compared to industry standard devices like the SMBJ14CA which has 1500 pF of capacitance and can cause up to 3 dB of THD attenuation in measured systems.

Finally, the small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS1401 allows the device to be placed extremely close to the input connector, which lowers the length of the path fault current going through the system compared to larger protection solutions.

10.2.3 Application Curves

When a surge is applied to a system with the TVS1401, the device will clamp the overvoltage to a safe level as shown in 図 10-2.

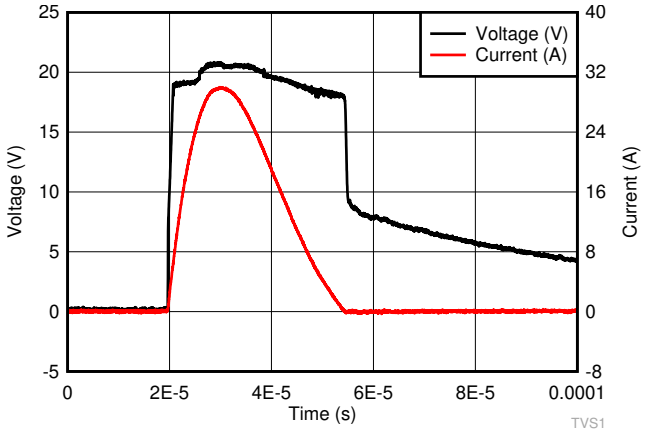


図 10-2. TVS1401 Surge Clamping Response

11 Power Supply Recommendations

The TVS1401 is a clamping device so there is no need to power it. To ensure the device functions properly, do not violate the recommended V_{IN} voltage range (-14 V to 14 V).

12 Layout

12.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the tested trace to other nearby unprotected traces, which could result in system failures. The PCB designer must minimize the possibility of EMI coupling by keeping all unprotected traces away from protected traces between the TVS and the connector. Route the protected traces straight. Use rounded corners with the largest radii possible to eliminate any sharp corners on the protected traces between the TVS1401 and the connector. Electric fields tend to build up on corners, which could increase EMI coupling.

Ensure that the thermal pad on the layout is floating rather than grounded. Grounding the thermal pad will impede the operating range of the TVS1401 and can cause failures when the applied voltage is negative. A floating thermal pad allows the maximum operating range without sacrificing any transient performance.

12.2 Layout Example

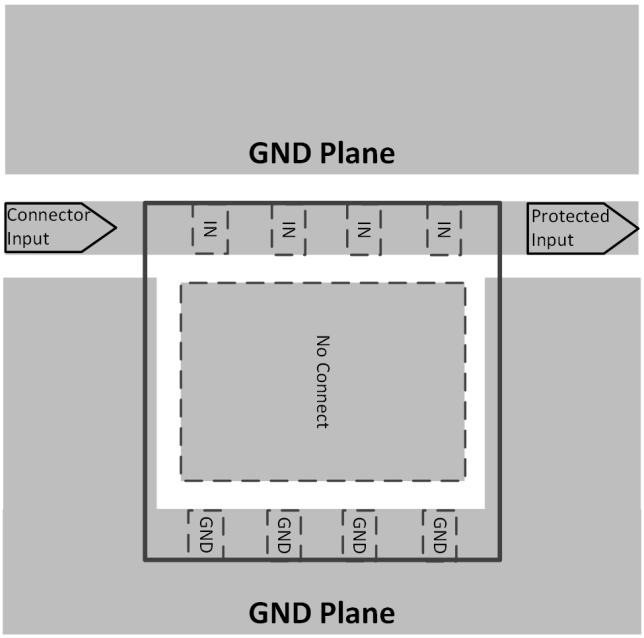


図 12-1. TVS1401 Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flat-Clamp Surge Protection Technology for Efficient System Protection* white paper
- Texas Instruments, *TI's IEC 61000--4-x Tests for TI's Protection Devices* application report
- Texas Instruments, *TVS Surge Protection in High-Temperature Environments* application report
- Texas Instruments, *TVS1401 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVS1401DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1PSP
TVS1401DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1PSP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

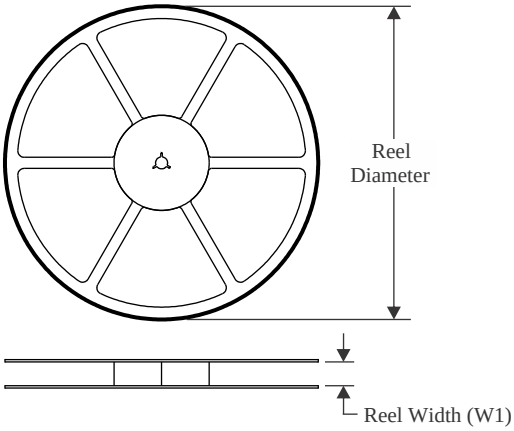
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

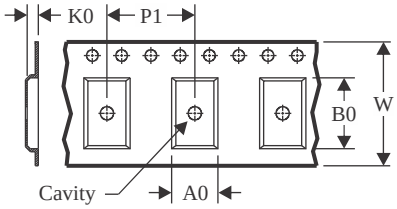
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

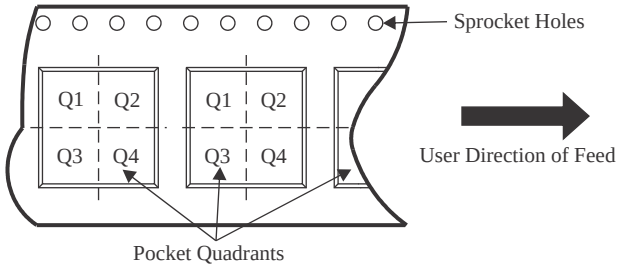


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

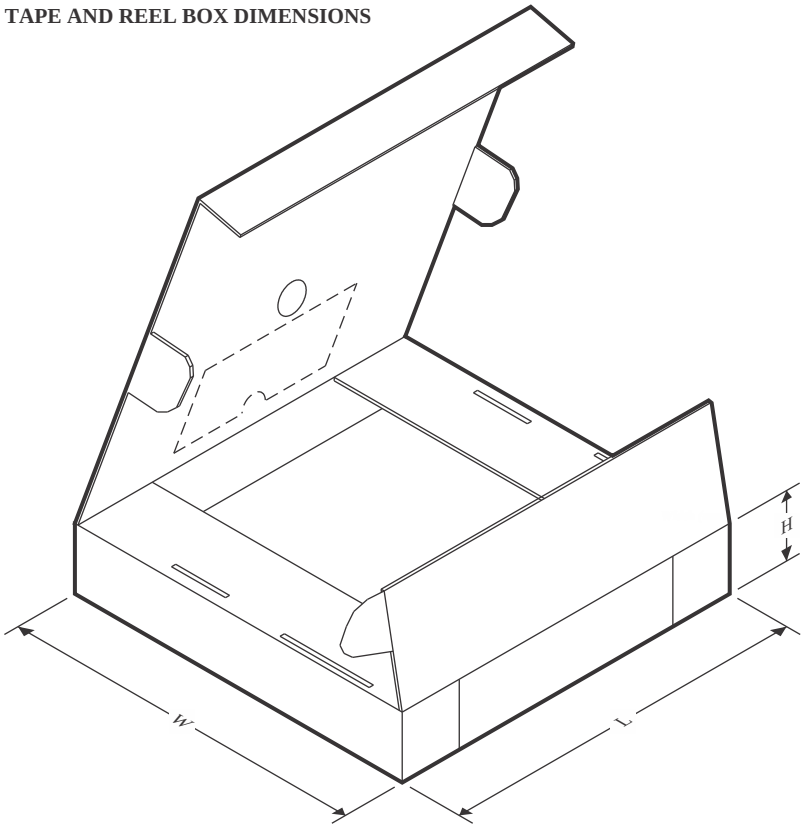
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS1401DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS1401DRBR	SON	DRB	8	3000	338.0	355.0	50.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

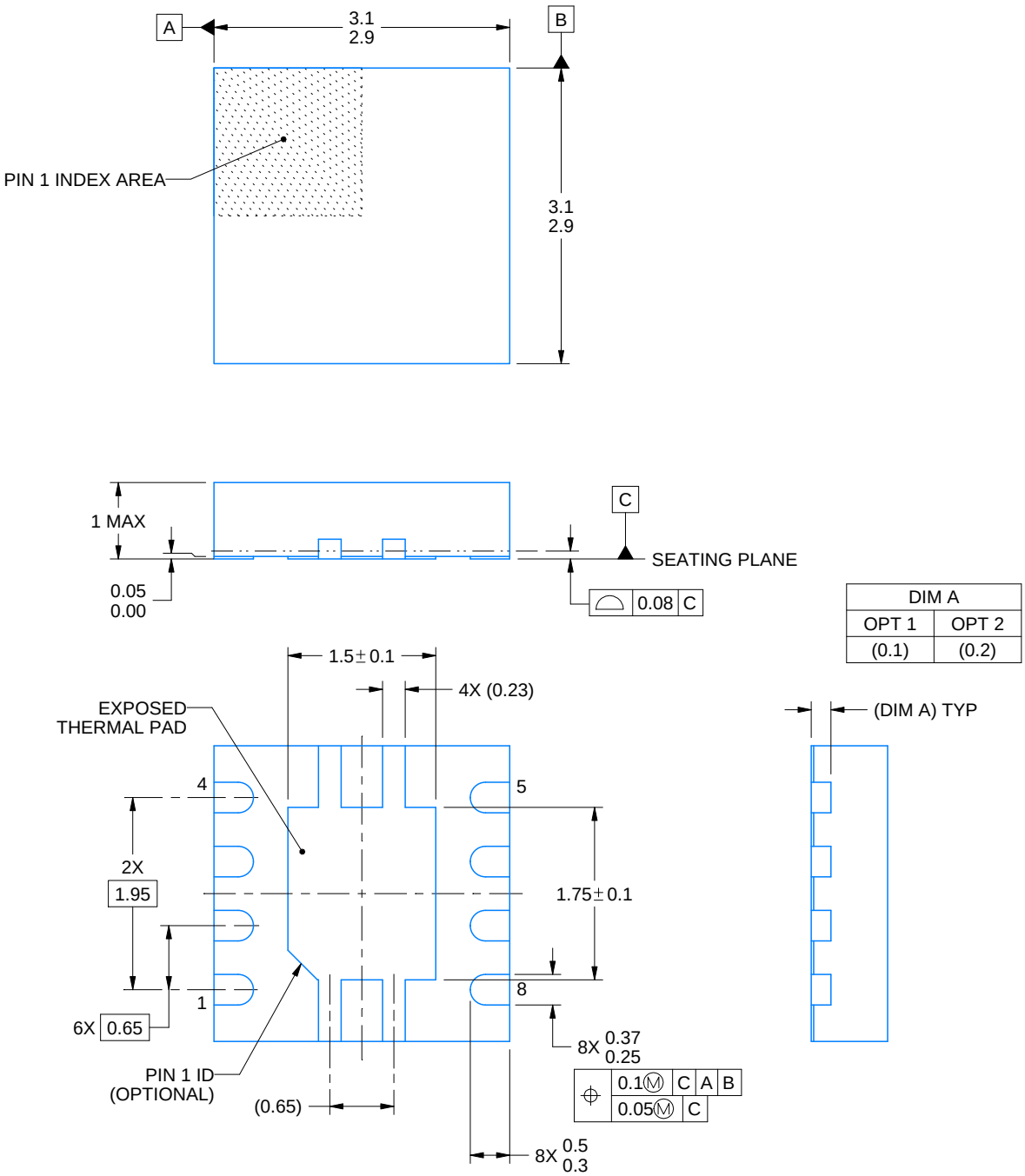
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

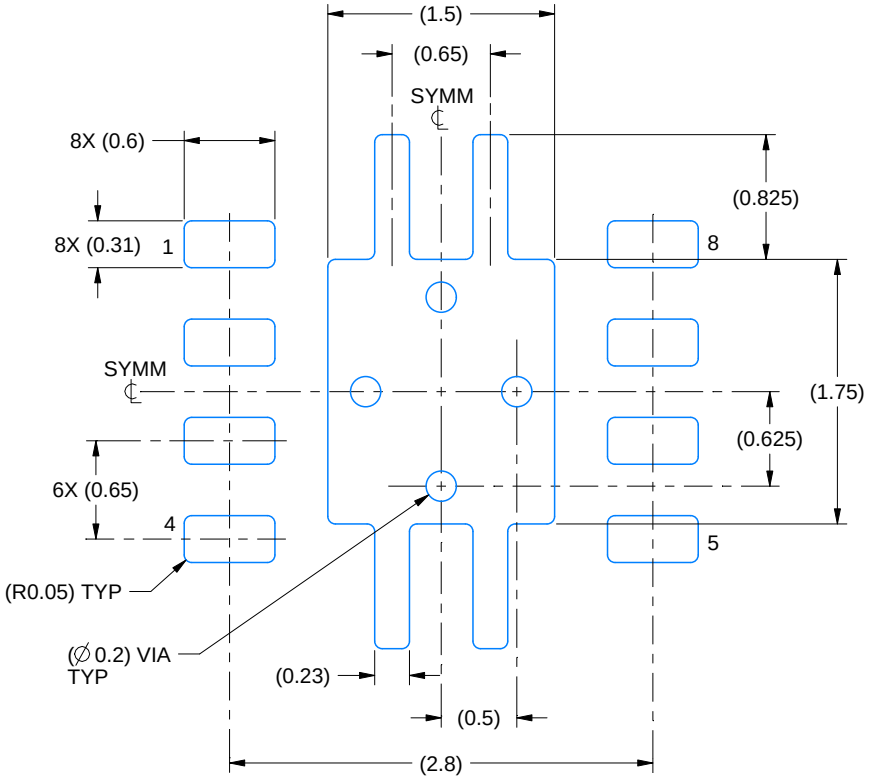
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

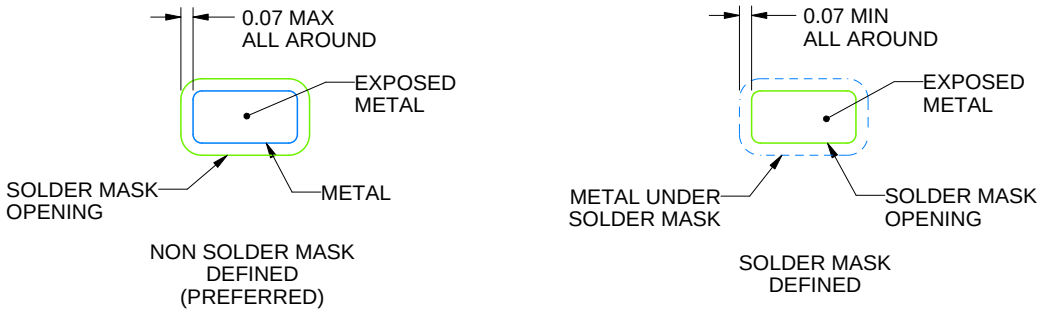
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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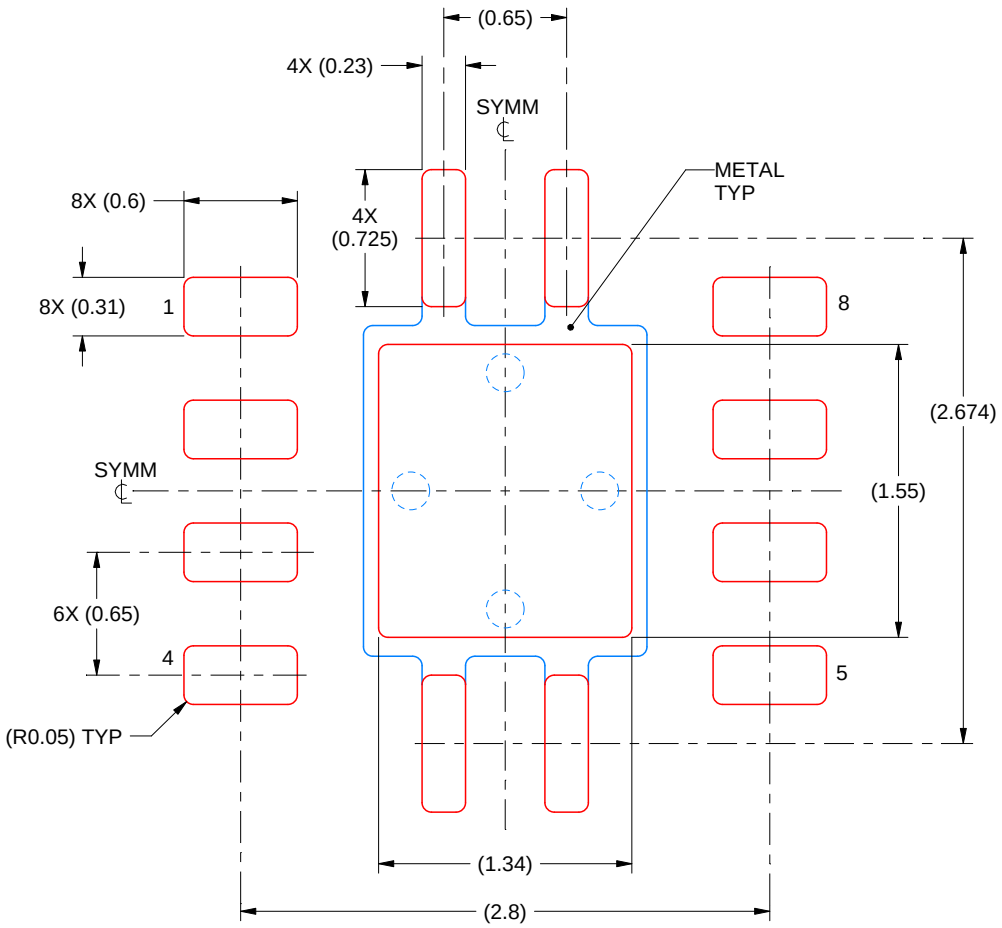
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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