TEXAS INSTRUMENTS
TUSB2E22
JAJSRL5C – FEBRUARY 2019 – REVISED AUGUST 2024

TUSB2E22 eUSB2-USB 2.0 デュアル・リピータ

1 特長

- USB 2.0 および eUSB2 (rev 1.1) 準拠
- ロースピード (LS)、フルスピード (FS)、ハイスピード (HS) をサポート
- 2:2 クロスバー マルチプレクサ搭載デュアル リピータ
- ホスト モードおよびデバイス モード (DRD) をサポート
- 4 つの eUSB2 補償設定により、さまざまなシステム要件に対応
- eUSB2 LS/FS 信号は eUSB2 インターフェイスの 1.2V オプションに対応

2 アプリケーション

- 通信機器
- エンタープライズ・システム
- ノート PC およびデスクトップ PC
- 産業用
- タブレット
- 携帯電子機器

3 概要

TUSB2E22 を使うと、低電圧プロセスを使用する新しいプロセッサに USB 2.0 準拠ポートを実装できます。

TUSB2E22 は、デバイス モードとホスト モードの両方をサポートする USB 準拠の eUSB2-USB 2.0 リピータです。

TUSB2E22 は、USB ロースピード (LS) 信号、フルスピード (FS) 信号、ハイスピード (HS) 信号をサポートしています。

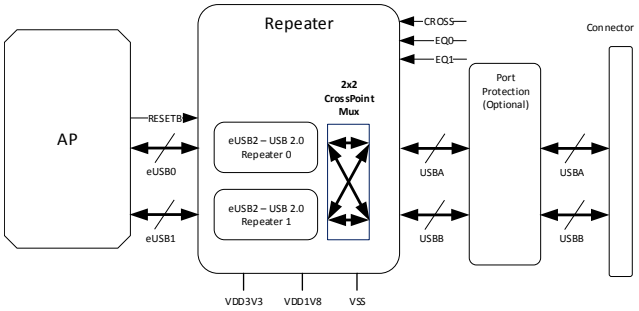
TUSB2E22 は、1.2V のシングルエンド信号で動作する eUSB2 eDSPr または eUSPr と接続するように設計されています。

TUSB2E22 には、EQ0 ピンおよび EQ1 ピンによる 4 レベルの補償設定があります。これらの設定を使用して、さまざまな eUSB2 チャネル損失プロファイルに対して補償を最適化できます。

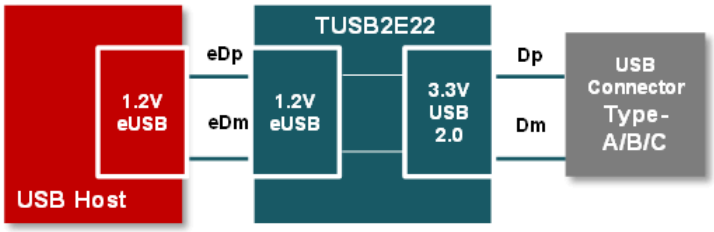
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TUSB2E22	YCG (DSBGA、25)	2 mm × 2 mm
	RZA (VQFN、20)	3.5mm × 3.5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



TUSB2E22

Table of Contents

4 Pin Configuration and Functions

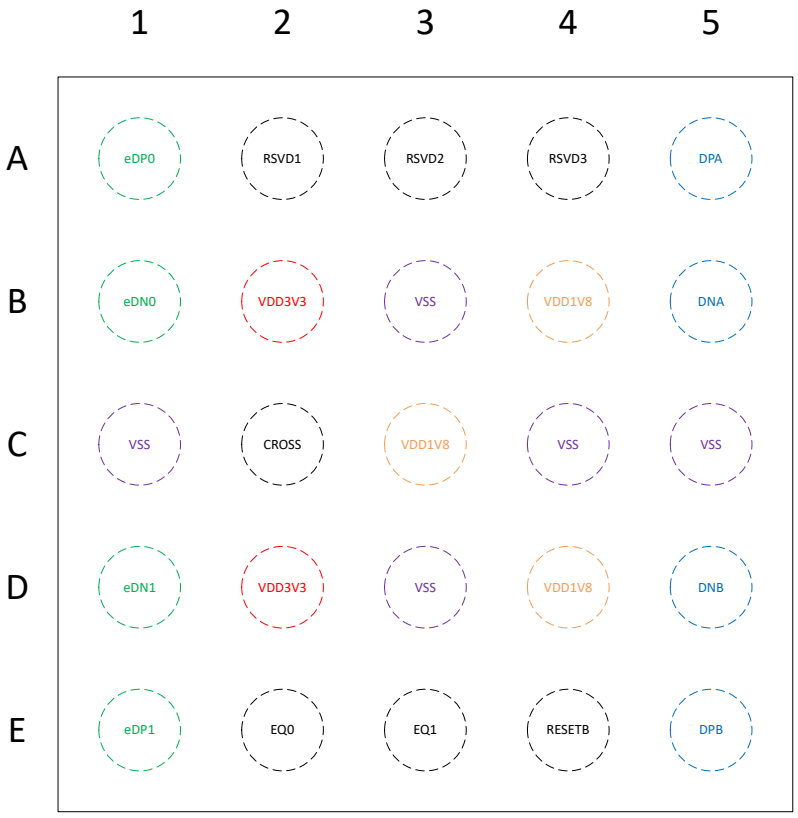


図 4-1. YCG Package, 25-Pin DSBGA (Top View)

Legend		
3.3 V Rails	1.8 V Rails	eUSB2 Data Signals
USB2 Data Signals	GPIO Digital Input or Output	

表 4-1. Pin Functions

PIN		TYPE	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NO.	NAME				
B2, D2	VDD3V3	PWR	N/A	N/A	3.3 V Supply Voltage
C3, B4, D4	VDD1V8	PWR	N/A	N/A	1.8 V Analog Supply Voltage
C1, C4, B3, D3, C5	VSS	GND	N/A	N/A	GND
E4	RESETB	Digital Input	N/A	VDD1V8	Active Low Reset. Upon deassertion of RESETB both repeaters will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
C2	CROSS	Digital Input	N/A	VDD3V3	Indicates mux orientation. Used to specify orientation of internal Crossbar switch CROSS = Low: eUSB0 «–» USBA and eUSB1 «–» USBB CROSS = High: eUSB0 «–» USBB and eUSB1«–» USBA Sampled at deassertion of RESETB
A2	RSVD1	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
A3	RSVD2	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
A4	RSVD3	Digital Output	Hi-Z	VDD3V3	Reserved pin leave it unconnected

表 4-1. Pin Functions (続き)

PIN		TYPE	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NO.	NAME				
E2	EQ0	Digital I/O	Hi-Z (input)	VDD3V3	Compensation Level 0: EQ1=low EQ0= low Compensation Level 1: EQ1=low EQ0=high Compensation Level 2: EQ1=high EQ0=low Compensation Level 3: EQ1=high EQ0=high Pins are sampled at RESETB deassertion
E3	EQ1	Digital I/O	Hi-Z (input)	VDD3V3	
A1	eDP0	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D+ pin
B1	eDN0	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D- pin
D1	eDN1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D- pin
E1	eDP1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D+ pin
A5	DPA	Analog I/O	Hi-Z	VDD3V3	USB port A D+ pin
B5	DNA	Analog I/O	Hi-Z	VDD3V3	USB port A D- pin
D5	DNB	Analog I/O	Hi-Z	VDD3V3	USB port B D- pin
E5	DPB	Analog I/O	Hi-Z	VDD3V3	USB port B D+ pin

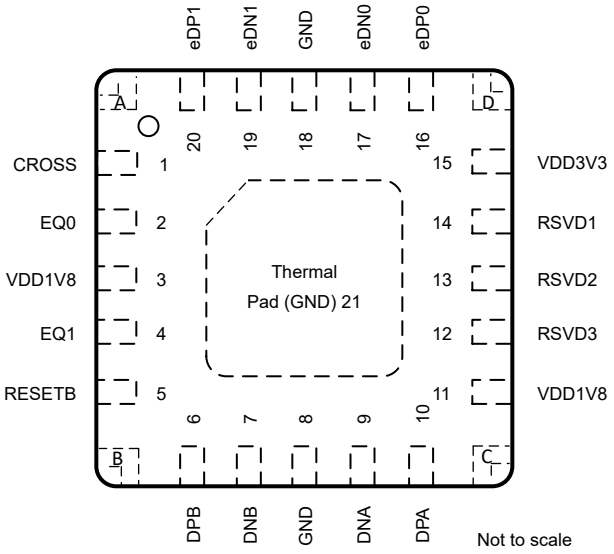


図 4-2. 0.5-mm Pitch RZA Package, 20-Pin VQFN (Top View)

表 4-2. Pin Functions

PIN		TYPE[1]	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
VDD3V3	15	PWR	N/A	N/A	3.3 V supply voltage
VDD1V8	3, 11	PWR	N/A	N/A	1.8 V analog supply voltage
GND	8, 18, Thermal Pad (21), Corner Anchors (A, B, C, D)	GND	N/A	N/A	GND
RESETB	5	Digital Input	N/A	VDD1V8	Active Low Reset. Upon deassertion of RESETB both repeaters will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
CROSS	1	Digital Input	N/A	VDD3V3	Indicates mux orientation. Used to specify orientation of internal Crossbar switch CROSS = Low: eUSB0 «–» USBA and eUSB1 «–» USBB CROSS = High: eUSB0 «–» USBB and eUSB1«–» USBA Sampled at deassertion of RESETB
RSVD1	14	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
RSVD2	13	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
RSVD3	12	Digital Output	Hi-Z	VDD3V3	Reserved pin leave it unconnected

表 4-2. Pin Functions (続き)

PIN		TYPE(1)	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
EQ0	2	Digital I/O	Hi-Z (input)	VDD3V3	Compensation Level 0: EQ1=low EQ0= low Compensation Level 1: EQ1=low EQ0=high Compensation Level 2: EQ1=high EQ0=low Compensation Level 3: EQ1=high EQ0=high Pins are sampled at RESETB deassertion
EQ1	4	Digital I/O	Hi-Z (input)	VDD3V3	
eDP0	16	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D+ pin
eDN0	17	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D- pin
eDN1	19	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D- pin
eDP1	20	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D+ pin
DPA	10	Analog I/O	Hi-Z	VDD3V3	USB port A D+ pin
DNA	9	Analog I/O	Hi-Z	VDD3V3	USB port A D- pin
DNB	7	Analog I/O	Hi-Z	VDD3V3	USB port B D- pin
DPB	6	Analog I/O	Hi-Z	VDD3V3	USB port B D+ pin

(1) PWR = power, GND = ground, I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{DD3V3}	–0.3	4.32	V
Analog Supply voltage range	V_{DD1V8}	–0.3	2.1	V
Voltage range	DPA, DNA, DPB, DNB , 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
Voltage range	eDP0, eDN0, eDP1, eDN1	–0.3	1.6	V
Voltage range	CROSS, RESETB, RSVD1, RSVD2, RSVD3, EQ1, EQ0	–0.3	2.1	V
Junction temperature	$T_{J(max)}$		125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD3V3}	Supply voltage (VDD3V3)	3.0	3.3	3.6	V
V_{DD1V8}	Analog Supply voltage (VDD1V8)	1.62	1.8	1.98	V
T_A	Operating free-air temperature	-20		85	°C
T_J	Junction temperature	-20		105	°C
T_{CASE}	Case temperature	-20		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	-20		92	°C

5.4 Thermal Information

THERMAL METRIC[1]		TUSB2E22 YCG (DSBGA) 25 PINS	TUSB2E22 RZA (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	46.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	39.0	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	—	13.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.9	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.9	21.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IH}	High level input voltage	CROSS, EQ1, EQ0	1.053			V
V_{IL}	Low-level input voltage	CROSS, EQ1, EQ0			0.693	V
V_{IL}	Low-level input voltage	RESETB			0.35	V
V_{IH}	High level input voltage	RESETB	0.75			V
I_{IH}	High level input current	V_{IH} = 1.98 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62V or 0 V CROSS, RESETB, EQ1, EQ0			2	µA
I_{IL}	Low level input current	V_{IL} = 0 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62V or 0 V CROSS, RESETB, EQ1, EQ0			2	µA
USBA (DPA, DNA), USBB (DPB, DNB)						
Z_{inp_Dx}	Impedance to GND, no pull up/down	Vin=3.6 V, V_{DD3V3}=3.0 V USB 2.0 Specification Section 7.1.6	390			kΩ
R_{PUI}	Bus Pull-up Resistor on Upstream Facing Port (idle)	USB 2.0 Specification Section 7.1.5	0.92	1.1	1.475	kΩ
R_{PUR}	Bus Pull-up Resistor on Upstream Facing Port (receiving)	USB 2.0 Specification Section 7.1.5	1.525	2.2	2.99	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Specification Section 7.1.5	14.35	19	24.6	kΩ
V_{HSTERM}	Termination voltage in highspeed	USB 2.0 Specification Section 7.1.6.2, The output voltage in the high-speed idle state	–10		10	mV
USB TERMINATION						
Z_{HSTERM}	Driver Output Resistance (which also serves as high speed termination)	(VOH= 0 to 600 mV) USB 2.0 Specification Section 7.1.1.1,	40.5	45	49.5	Ω
USBA, USBB INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Specification Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Specification Section 7.1.4 (HOST downstream port pull down resistor enabled and external device pull up 1.5K +/-5% to 3.0-3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Specification Section 7.1.4			0.8	V
USBA, USBB OUTPUT LEVELS LS/FS						

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low	USB 2.0 Specification Section 7.1.1, (measured at connector with RL of 1.425 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Specification Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Specification Section 7.1.1, Measured it during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Specification Section 7.1.1 Figure 7-8; Excluding the first transition from the Idle state	1.3		2	V
USBA, USBB OUTPUT LEVELS HS						
V_{HSOH}	High-speed data signaling high	USB 2.0 Specification Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, Test load is an ideal 45 Ω to GND on DP and DN	360		440	mV
V_{HSOL}	High-speed data signaling low, driver is off termination is on (measured single ended)	USB 2.0 Specification Section 7.1.7.2, Test load is an ideal 45 Ω to GND on DP and DN.	–10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	USB 2.0 Specification Section 7.1.7.2 , Test load is an ideal 45 Ω to GND on DP and DN.	700	900	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	USB 2.0 Specification Section 7.1.7.2 , Test load is an ideal 45 Ω to GND on DP and DN.	-900	-700	-500	mV
$U2\_TX_{CM}$	High-speed TX DC Common Mode		-50	200	500	mV
eUSB2 TERMINATION						
R_{SRC_HS}	High speed transmit source termination impedance	eUSB2 Specification Section 7.1.1	33	40	47	Ω
ΔR_{SRC_HS}	High speed source impedance mismatch	eUSB2 Specification Section 7.1.1			4	Ω
R_{RCV_DIF}	High speed differential receiver termination (repeater)	eUSB2 Specification Section 7.1.2	74	80	86	Ω
R_{PD}	Pull-down resistors on eDP/eDN	eUSB2 Specification Section 7.3, active during LS, FS and HS	6	8	10	kΩ
R_{SRC_LSFS}	Transmit output impedance	eUSB2 Specification Section 7.2.1, Table 7-13 TX output impedance to match spec version 1.10	28	44	59	Ω
eUSB0, eUSB1 FS/LS INPUT LEVELS						
V_{IL}	Single-ended input low	eUSB2 Specification Section 7.2.1, Table 7-13	–0.1		0.399	V
V_{IH}	Single-ended input high	eUSB2 Specification Section 7.2.1, Table 7-13	0.819		1.386	V
V_{HYS}	Receive single-ended hysteresis voltage	eUSB2 Specification Section 7.2.1, Table 7-13	43.2			mV
eUSB0, eUSB1 FS/LS OUTPUT LEVELS						
V_{OL}	Single-ended output low	eUSB2 Specification Section 7.2.1, Table 7-13			0.198	V
V_{OH}	Single-ended output high	eUSB2 Specification Section 7.2.1, Table 7-13	0.918		1.32	V
eUSB0, eUSB1 HS INPUT LEVELS						

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RX_CM}	Receive DC common mode range (low)	eUSB2 Specification Section 7.1.2 (normative), low DC common mode RX must tolerate			120	mV
V_{RX_CM}	Receive DC common mode range (high)	eUSB2 Specification Section 7.1.2 (normative), high DC common mode RX must tolerate	280			mV
$V_{CM\_RX\_AC}$	Receiver AC common mode (50MHz-480MHz)	eUSB2 Specification Section 7.1.2 (informative), across the DC common mode range of 120 mV to 280 mV. (RX capability tested with intentional TX Rise/Fall Time mismatch and prop delay mismatch)	–60		60	mV
C_{RX_CM}	Receive center-tapped capacitance	eUSB2 Specification Section 7.1.2 (informative)	15		50	pF
$V_{RX\_DIF\_SENS}$	Receive differential sensitivity, RX should be able to receive less than this value.	eUSB2 Specification Section 7.1.2, V_{CM} = 120 mV to 450 mV			120	mVp-p
eUSB0, eUSB1 HS OUTPUT LEVELS						
$V_{ETX\_CM\_AC}$	Transmit CM AC (50MHz-480MHz)	eUSB2 Specification Section 7.1.1, An ideal 80 Ω Rx differential termination and center tap cap of 15pF, with maximum DC common mode range	–30		30	mV
V_{EHSOD}	Transmit differential (terminated)	Measured p2p, R_L = 80 Ω, ideal 80 Ω Rx differential termination load		400		mV
$V_{E\_TX\_CM}$	Transmit DC common mode	eUSB2 Specification Section 7.1.1	170		230	mV

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DPA, DNA, DPB, DNB, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Specification Figure 7-8; Figure 7-9	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Specification Figure 7-8; Figure 7-9	4		20	ns
T_{FRFM}	(T_{FR}/T_{FM})	USB 2.0 Specification 7.1.2, Excluding the first transition from the Idle state	90		111.1	%
DPA, DNA, DPB , DNB, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Specification Figure 7-8	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Specification Figure 7-8	75		300	ns
eDP0, eDN0, eDP1, eDN1, HS Driver Switching Characteristics						
T_{EHSRF_MM}	Transmit rise/fall mismatch	eUSB2 Specification Section 7.2.1, Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).			25	%
eDP0, eDN0, eDP1, eDN1, LS/FS Driver Switching Characteristics						
T_{ERF}	Rise/Fall Time (10% - 90%)	eUSB2 Specification Section 7.2.1	2		6	ns
T_{ERF_MM}	Transmit rise/fall mismatch	eUSB2 Specification Section 7.2.1			25	%

5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
RESET TIMING					
$t_{\_VDD1V8\_RAMP}$	Ramp time for VDD1V8 to reach minimum 1.62 V			2	ms
$t_{\_VDD3V3\_RAMP}$	Ramp time for VDD3V3 to reach minimum 3.0 V			2	ms
$t_{\_su\_CROSS}$	Setup time for CROSS sampled at the deassertion of RESETB	0			ms
$t_{\_hd\_CROSS}$	Hold time for CROSS sampled at the deassertion of RESETB	3			ms
$t_{\_aRESETB}$	duration for RESETB to be asserted low to complete reset while powered	10			us
$t_{\_RH\_READY}$	Time for eUSB2 interface to be ready after RESETB is deasserted or (VDD1V8 and VDD3V3) reach minimum recommended voltages, whichever is later			3	ms

6 Parametric Measurement Information

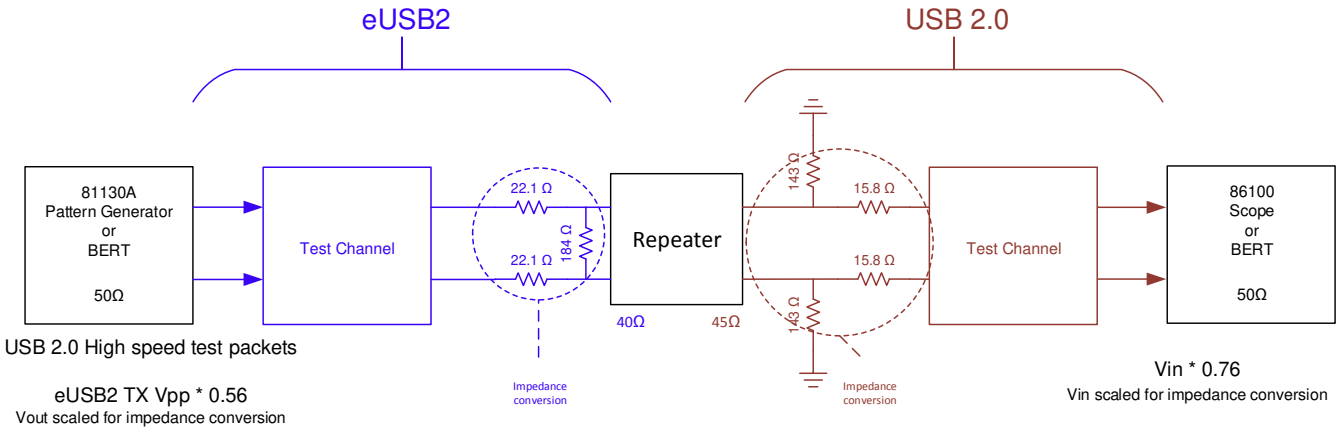


図 6-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup

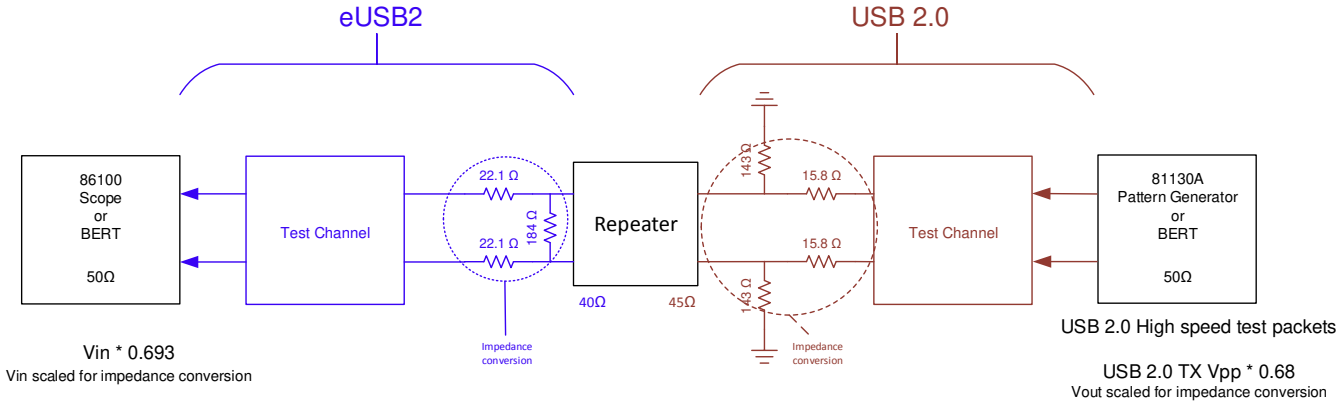


図 6-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

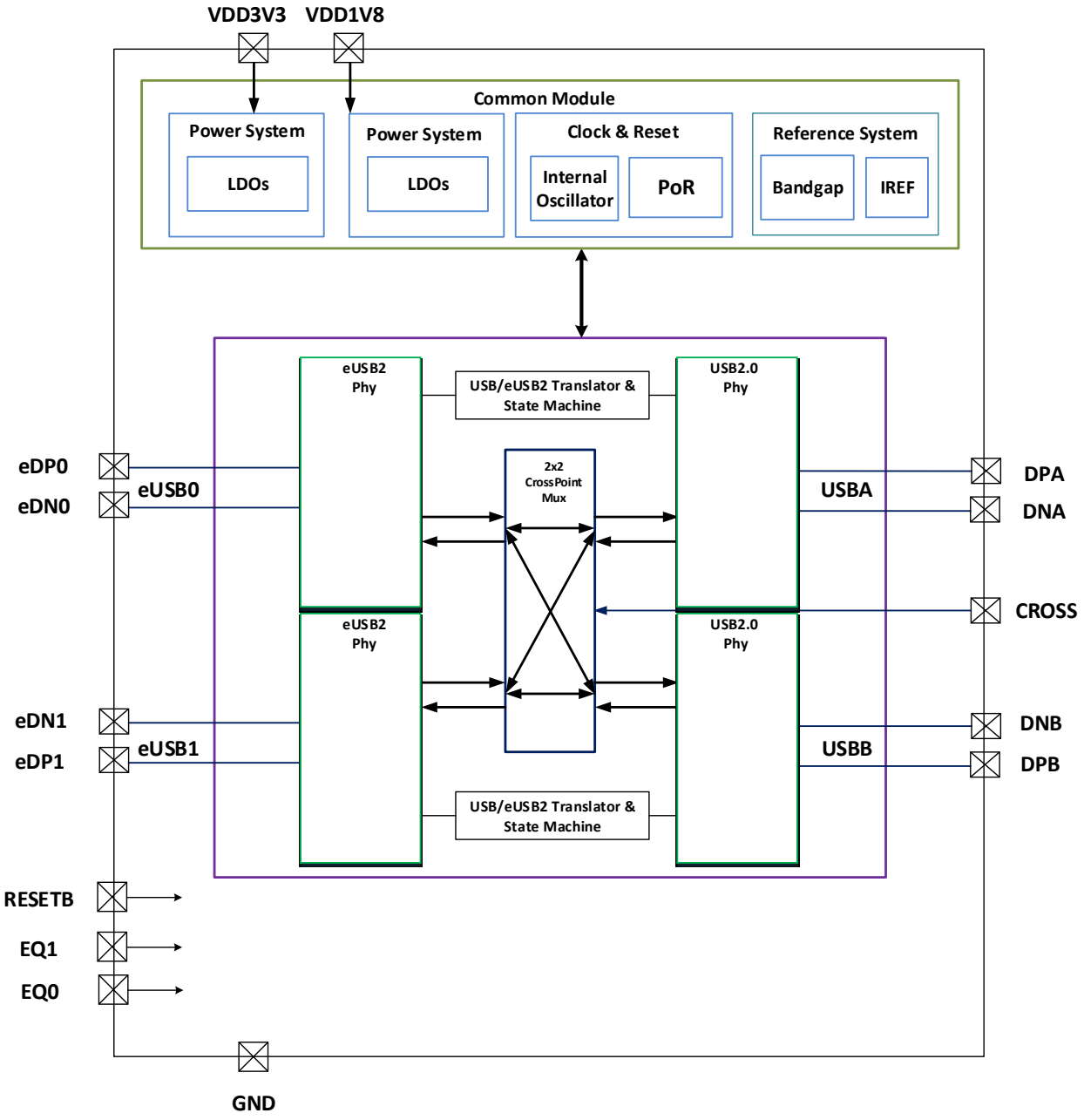
7 Detailed Description

7.1 Overview

The TUSB2E22 is a dual eUSB2 to USB 2.0 repeater that resides between SoC with one or two eUSB2 port and an external connector that supports USB 2.0. Each repeater is independently configurable as either a host or device repeater (DRD repeater).

The USB 2.0 ports A and B can be swapped by an internal crossbar switch by configuring CROSS pin at reset. CROSS pin is ignored after power up reset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB 2.0

TUSB2E22 supports two USB 2.0 ports. Each port supports Low Speed, Full Speed and High Speed operations.

7.3.2 eUSB2

TUSB2E22 supports two eUSB2 ports with 1.2V single ended signaling. Each port support Low Speed, Full Speed and High Speed operations.

7.3.3 Cross MUX

TUSB2E22 supports a cross mux functionality that can map either of the two eUSB2 ports to the two USB 2.0 ports providing design flexibility.

7.4 Device Functional Modes

7.4.1 Repeater Mode

Upon deassertion of RESETB and after t_{RH_READY} , TUSB2E22 will enable and enter default state and be ready to accept eUSB2 packets.

表 7-1. Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}. Number of hubs operating at HS is reduced due to SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

7.4.2 Power Down Mode

RESETB could be used as a power down pin when asserted low. Power down mode will put TUSB2E22 in lowest power mode.

7.4.3 CROSS

CROSS pin will control the orientation of the integrated cross bar mux.

Upon deassertion of RESETB followed by internally generated reset signal and 1ms delay, CROSS pin is sampled and latched.

The system needs to make sure that CROSS meets t_{su_CROSS} and t_{hd_CROSS} with respect to power supply ramp and RESETB deassertion per セクション 8.3 .

Changes to the state of the CROSS input while RESETB is high will be ignored.

表 7-2. eUSB2 to USB Mapping

	CROSS = 0	CROSS = 1
eUSB0 (eDP0, eDN0)	USBA (DPA, DNA)	USBB (DPB, DNB)
eUSB1 (eDP1, eDN1)	USBB (DPB, DNB)	USBA (DPA, DNA)

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

TUSB2E22 can be used in either HOST or Peripheral implementation. The mode is configured by the eUSB2 SoC.

8.2 Typical Dual Port System Implementation

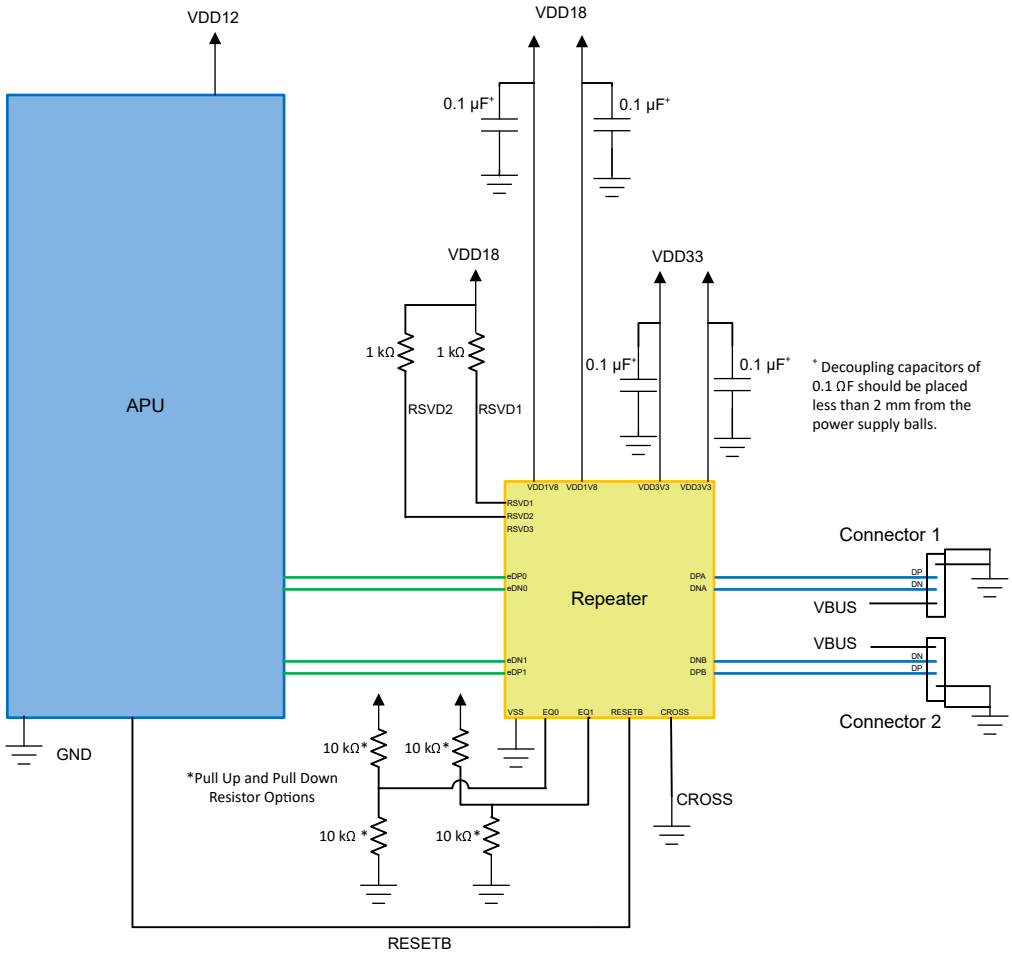


図 8-1. Typical Dual Port System Implementation

8.2.1 Design Requirements

TUSB2E22 supports the 1.2 V option of the eUSB2 specification. eUSB2 SoC must be compliant to the 1.2 V option of the eUSB2 specification.

8.2.2 Detailed Design Procedure

TUSB2E22 has four loss compensation settings for high speed operation and proper setting should be selected to match the system loss profile to optimize jitter performance. USB 2.0 high speed eye diagram measurements could be used as a guide to confirm the loss compensation is optimum for a given system.

8.2.3 Application Curve

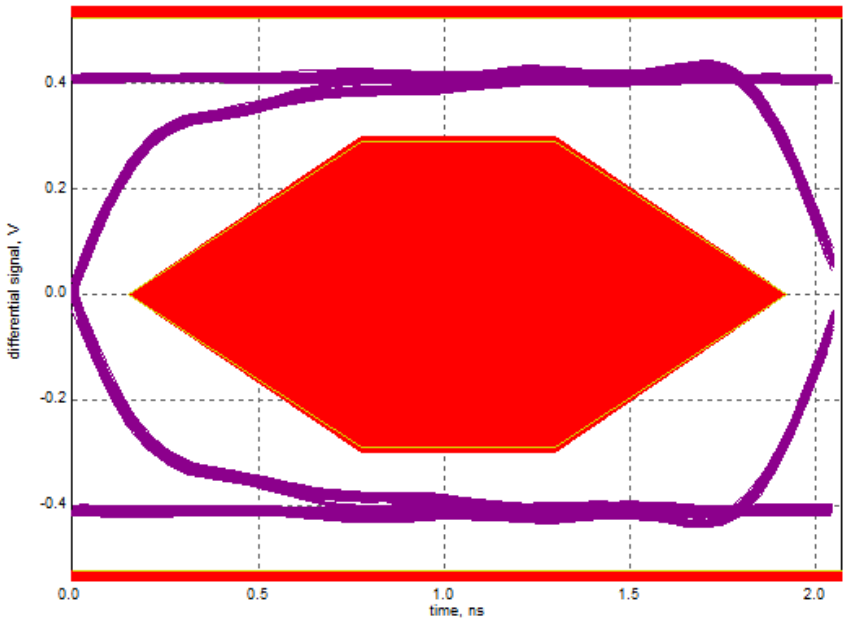


図 8-2. Typical USB 2.0 High Speed Eye Diagram

8.3 Power Supply Recommendations

8.3.1 Power Up Reset

RESETB pin is active low reset pin and can also be used as a power down pin.

TUSB2E22 does not have power supply sequence requirements between VDD3V3 and VDD1V8.

Maximum VDD3V3 and VDD1V8 ramp time to reach minimum supply voltages should be 2 ms.

Internal power on reset circuit along with the external RESETB input pin allows for proper initialization when RESETB is deasserted high prior to the power rails being valid. If RESETB deassert high before the power supplies are stable, internal power on reset circuit will hold off internal reset until the supplies are stable.

Upon deassertion of RESETB followed by internally generated reset signal and 1ms delay, CROSS pin is sampled and latched.

Upon deassertion of RESETB and after t_{RH_READY}, TUSB2E22 will enable and enter default state and be ready to accept eUSB2 packets. Each repeater will either be in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

8.4 Layout

8.4.1 Layout Guidelines

1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 図 8-3.

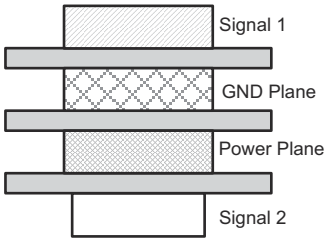


図 8-3. Four-Layer Board Stack-Up

8.4.2 Example YCG Layout For Application With No Cross MUX Function.

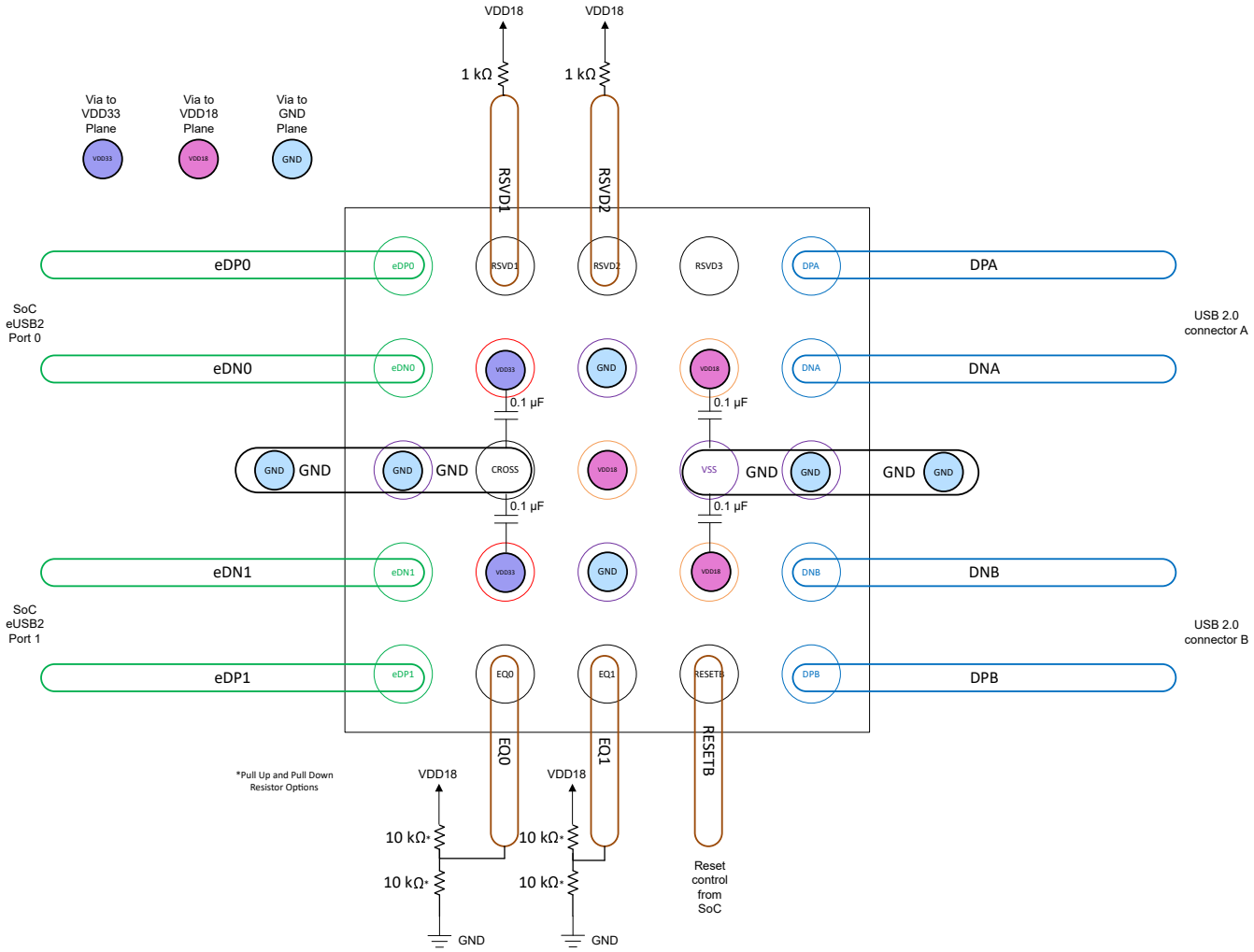


図 8-4. Example Layout of Application With No Cross MUX Function

8.4.3 Example RZA Layout For Application With No Cross MUX Function

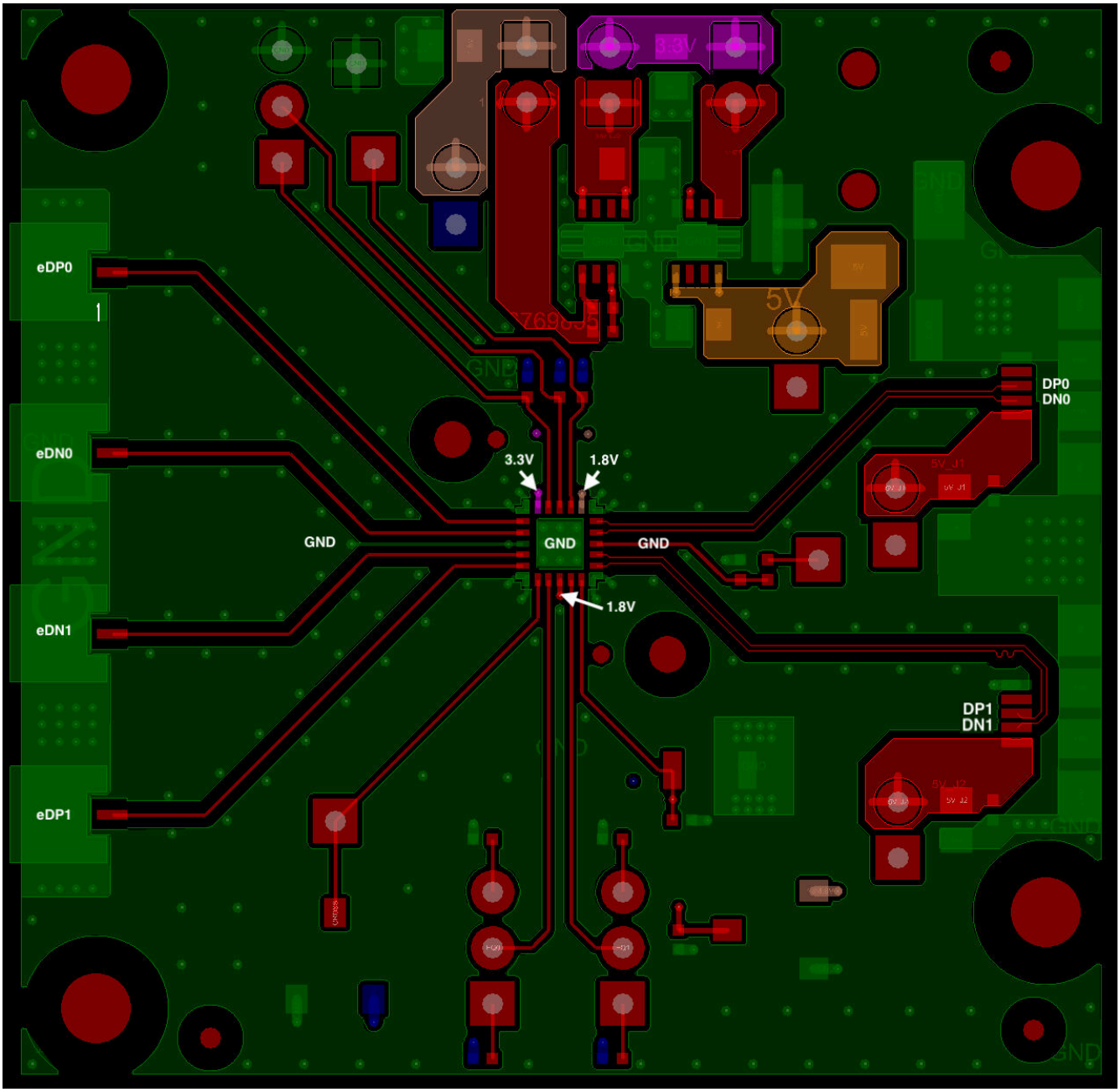


図 8-5. VQFN Example Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*
- Texas Instruments, *High-Speed Layout Guidelines Application Report*
- Texas Instruments, *High-Speed Interface Layout Guidelines*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (October 2023) to Revision C (August 2024)	Page
• YCG (DSBGA、25) パッケージのサイズを 1.75mm × 1.75mm から 2mm × 2mm に変更	1

Changes from Revision A (December 2019) to Revision B (October 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• パッケージ リード サイズを含めるよう「パッケージ情報」表を更新	1
• Added the RZA VQFN package option	3
• Added example layout for VQFN with no cross MUX control	18

Changes from Revision * (February 2019) to Revision A (December 2019) **Page**

- データシートの最初の公開リリース..... 1

11 Mechanical, Packaging, and Orderable Information

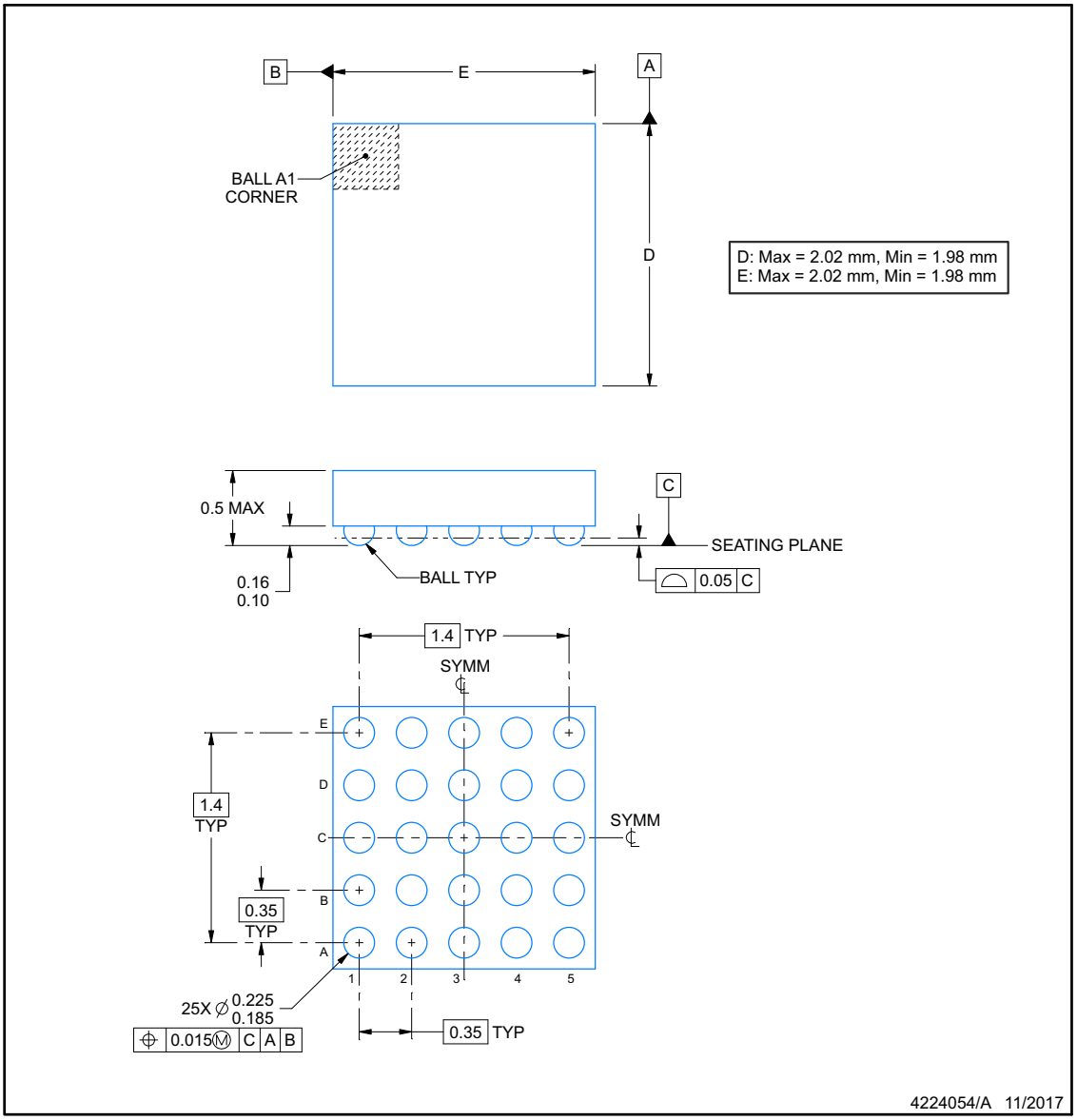
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

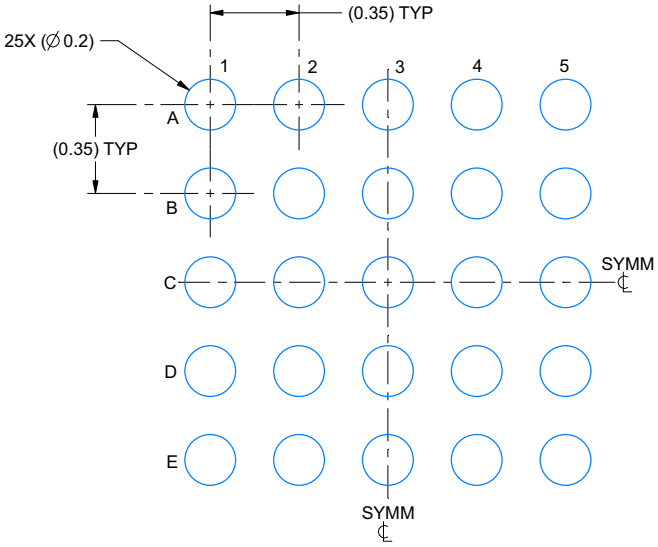
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

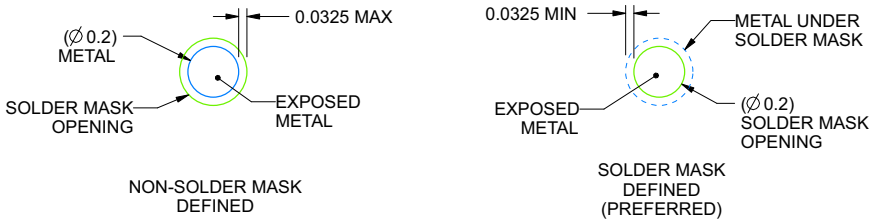
YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224054/A 11/2017

NOTES: (continued)

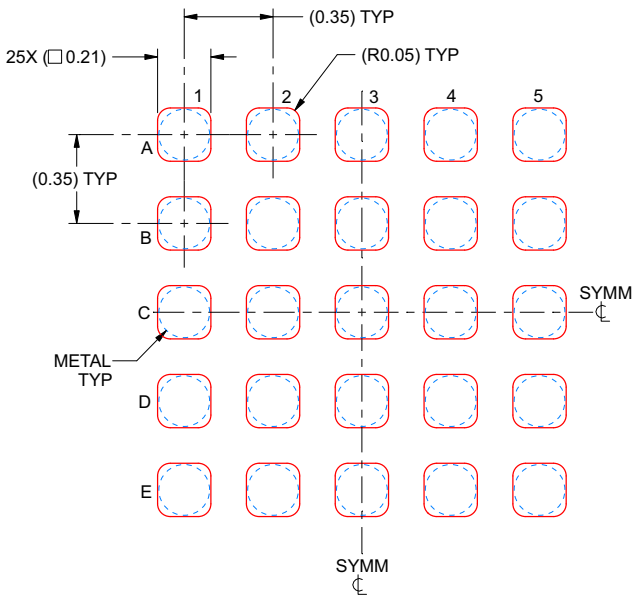
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224054/A 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB2E22RZAR	Active	Production	VQFN-FCRLF (RZA) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22
TUSB2E22RZAR.A	Active	Production	VQFN-FCRLF (RZA) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22
TUSB2E22RZAT	Active	Production	VQFN-FCRLF (RZA) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22
TUSB2E22RZAT.A	Active	Production	VQFN-FCRLF (RZA) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22
TUSB2E22YCGR	Active	Production	DSBGA (YCG) | 25	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2
TUSB2E22YCGR.A	Active	Production	DSBGA (YCG) | 25	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2
TUSB2E22YCGT	Active	Production	DSBGA (YCG) | 25	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2
TUSB2E22YCGT.A	Active	Production	DSBGA (YCG) | 25	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

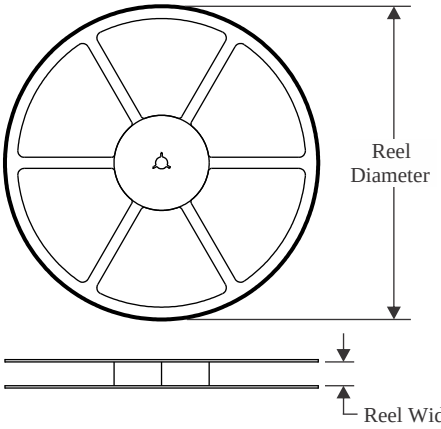
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

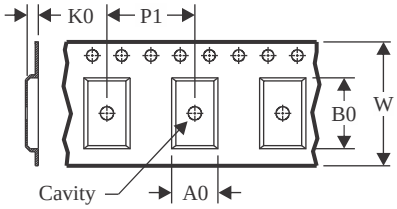
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

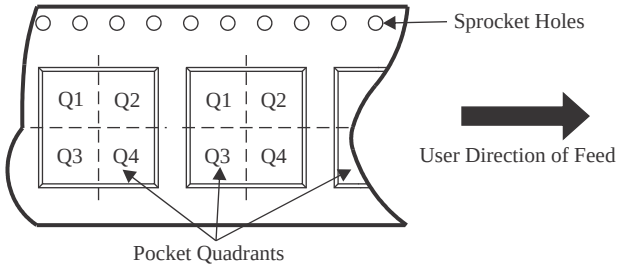


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

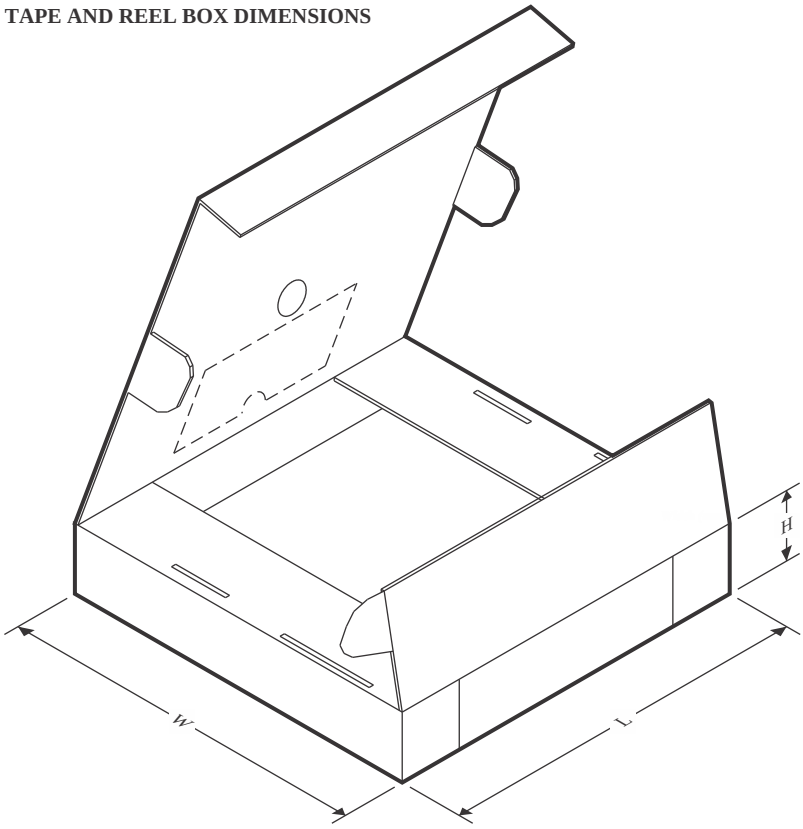
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2E22RZAR	VQFN-FCRLF	RZA	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TUSB2E22RZAT	VQFN-FCRLF	RZA	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TUSB2E22YCGR	DSBGA	YCG	25	3000	180.0	8.4	2.14	2.14	0.7	4.0	8.0	Q1
TUSB2E22YCGT	DSBGA	YCG	25	250	180.0	8.4	2.14	2.14	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

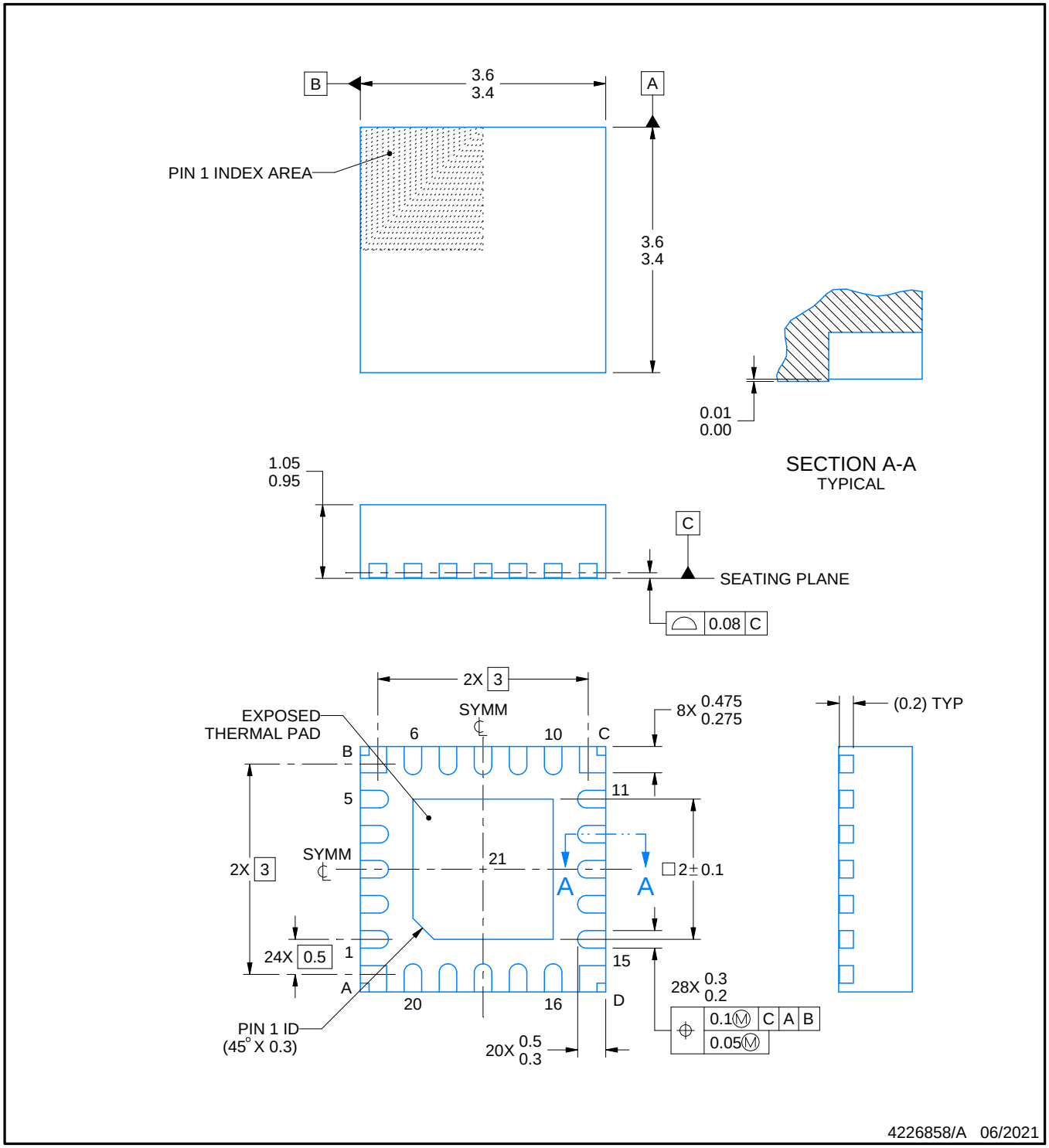
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2E22RZAR	VQFN-FCRLF	RZA	20	3000	367.0	367.0	35.0
TUSB2E22RZAT	VQFN-FCRLF	RZA	20	250	210.0	185.0	35.0
TUSB2E22YCGR	DSBGA	YCG	25	3000	182.0	182.0	20.0
TUSB2E22YCGT	DSBGA	YCG	25	250	182.0	182.0	20.0

PACKAGE OUTLINE

RZA0020A

VQFN - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

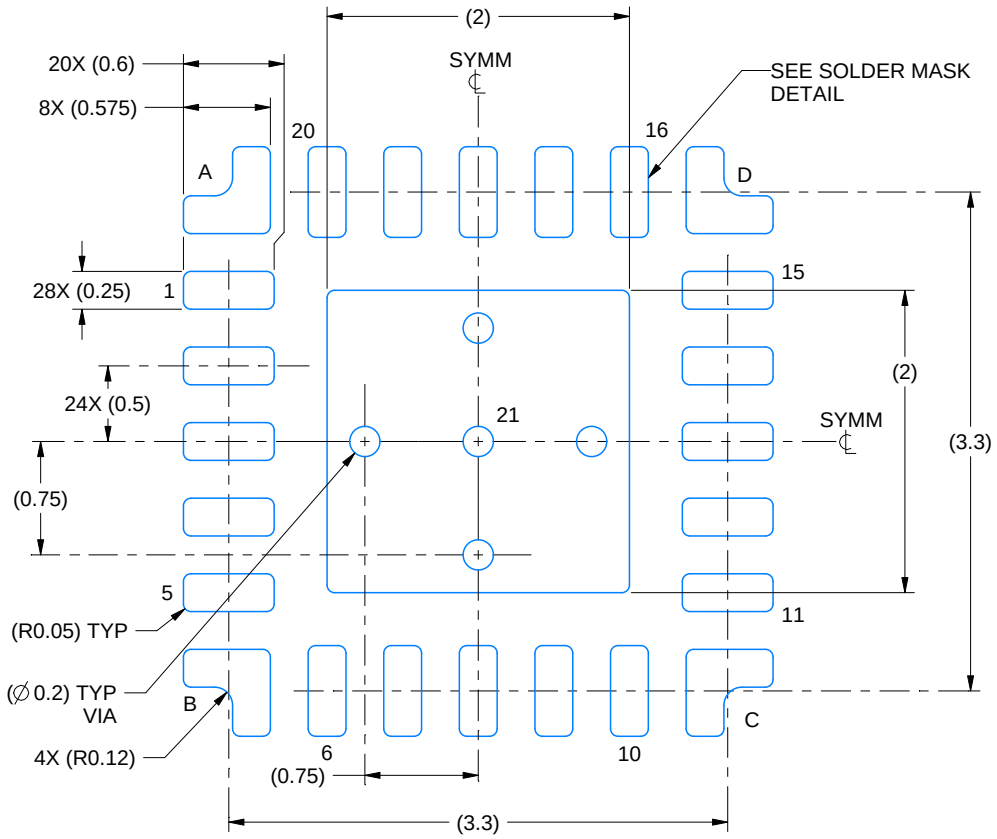
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

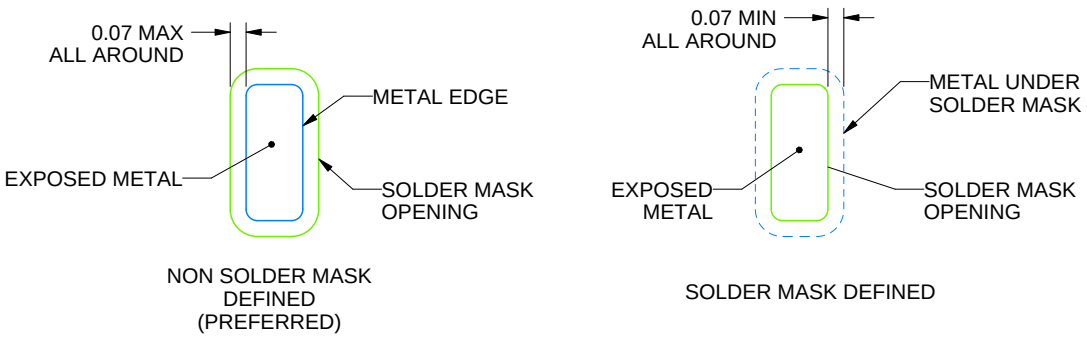
RZA0020A

VQFN - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

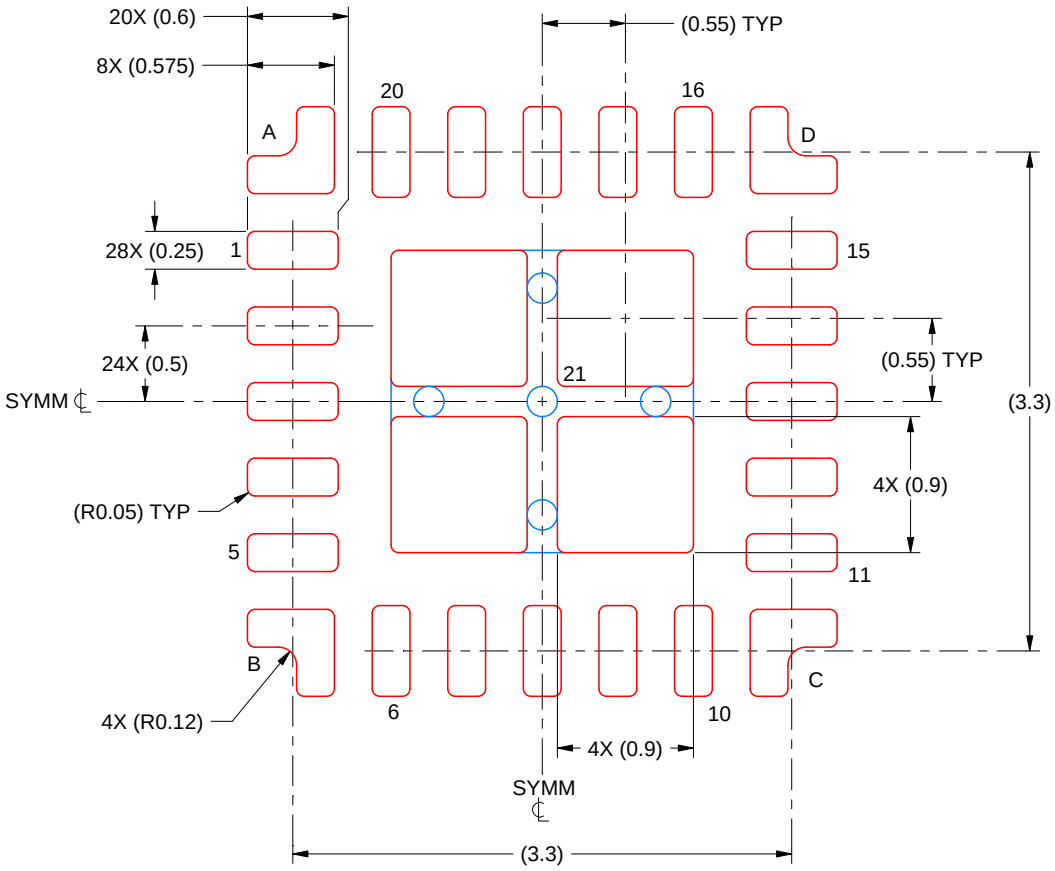


SOLDER MASK DETAILS

4226858/A 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226858/A 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265