



TUSB217-Q1 USB High Speed信号コンディショナー

1 特長

- 車載アプリケーション用にAEC-Q100認定済み
 - デバイス温度グレード2:
 - $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$
- 広い電源電圧範囲: 2.3~6.5V
- USB切断およびシャットダウン時の非常に低い消費電力
- USB 2.0 High Speed信号のコンディショニング
- USB 2.0、OTG 2.0、BC 1.2に対応
- Low Speed、Full Speed、High Speed信号処理をサポート
- 特定のホスト/デバイスに依存しない
- 最大5mのケーブルをサポート
 - 外付けのプルダウン抵抗により4つの信号ブースト(エッジブーストとDCブースト)設定を選択可能
 - プルアップまたはプルダウン構成が可能なピンにより3つのRX感度を選択でき、損失の大きいアプリケーションでISIジッタを補償
- スケーラブルなソリューション - 損失の大きいアプリケーションにはデジタイゼーション・デバイスを使用
- TUSB213 (5V)とピン互換

2 アプリケーション

- 車載インフォテインメント
- 車載用ヘッド・ユニット
- 車載用メディア・ハブ
- ラップトップ/デスクトップ/ドッキング・ステーション
- タブレット/携帯電話
- テレビ
- アクティブ・ケーブル、延長ケーブル
- バックプレーン

3 概要

TUSB217-Q1は第3世代USB 2.0 High Speed信号コンディショナーで、伝送チャネルでのAC損失(容量性負荷による)およびDC損失(抵抗損失による)を補償するように設計されています。

TUSB217-Q1には、エッジ昇圧器によりUSB 2.0 High Speed信号の遷移エッジを高速化し、DC昇圧機能により静的電圧レベルを上げる特許取得済みの設計が採用されています。また、TUSB217-Q1はプリーコライゼーション機能を備えているため、レシーバ感度を高め、長いケーブルを使用するアプリケーションでISIジッタを補償できます。USB Low SpeedおよびFull Speed信号特性は、TUSB217-Q1による影響を受けません。

TUSB217-Q1は、パケット・タイミングの変更や伝搬遅延の増加を伴わずに、信号品質を向上できるため、低レイテンシが要求されるアプリケーションに最適です。

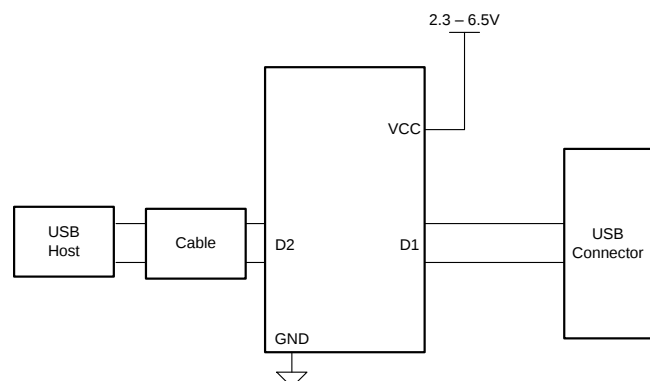
TUSB217-Q1により、最長5メートルのケーブルを使用したシステムで、USB 2.0 High Speed電気近端アイ・コンプライアンス・テストに合格することが可能になります。

TUSB217-Q1はUSB On-The-Go (OTG)およびBattery Charging (BC 1.2)プロトコルにも対応しています。

製品情報

型番	パッケージ	本体サイズ(公称)
TUSB217-Q1	VQFN (14)	3.50mm×3.50mm

概略回路図



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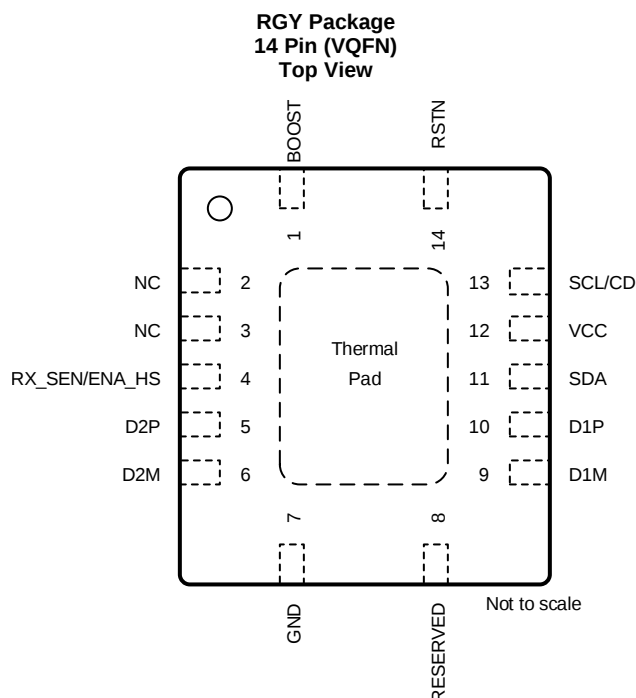
4 改訂履歴

2018年9月発行のものから更新

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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
BOOST	1	I	N/A	USB High Speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
NC	2,3	I		Leave unconnected
RESERVED	8	O		Leave unconnected or connect a decoupling cap 0.1µF
RX_SEN ⁽¹⁾ /ENA_HS	4	I/O	N/A	In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High Speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) – high RX sensitivity (high loss channel) M (pin is left floating) – medium RX sensitivity (medium loss channel) L (pin is pulled low) – low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].
D2P	5	I/O	N/A	USB High Speed positive port.
D2M	6	I/O	N/A	USB High Speed negative port.
GND	7	P	N/A	Ground
D1M	9	I/O	N/A	USB High Speed negative port..
D1P	10	I/O	N/A	USB High Speed positive port.

(1) Pull-down and pull-up resistors for RX_SEN pin must follow R_{RXSEN1} and R_{RXSEN2} resistor recommendations in non I²C mode.

Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
SDA ⁽²⁾	11	I/O	500 kΩ PU 1.8 MΩ PD	I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
VCC	12	P	N/A	Supply power
RSTN	14	I	500 kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-μF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
SCL ⁽²⁾ /CD	13	I/O	When RSTN asserted there is a 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
Thermal Pad	TPAD	N/A	N/A	Thermal Pad is electrically not connected to device ground. Connection to board ground is optional.

- (2) Pull-up resistors for SDA and SCL pins in I²C mode should be R_{Pull-up} (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I²C mode.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	VCC	−0.3	7	V
Voltage range USB data	DxP, DxM	−0.3	5.5	V
Voltage range on BOOST pin	BOOST	−0.3	1.98	V
Voltage range other pins	SCL, SDA, RX_SEN, RSTN	−0.3	5	V
Storage temperature, T _{stg}		−65	150	°C
Maximum junction temperature, T _{J (max)}			125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100- 011 CDM ESD Classification Level C4A	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.3	5	6.5	V
T _A	Operating free-air temperature (AEC-Q100)	−40		105	°C
T _J	Junction temperature (AEC-Q100)			115	°C
V _{I2C_BUS}	I2C Bus Voltage	1.62		3.6	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
SCL, SDA, RX_SEN, RSTN	Voltage range other pins (SCL, SDA, RX_SEN, RSTN)	0		3.6	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RGY (VQFN)	UNIT
		14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	49.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	52.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	24.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	24.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
POWER						
I _{ACTIVE_HS}	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V _{CC} supply stable, with Boost = Max		22	36	mA
I _{IDLE_HS}	High Speed Idle Current	USB channel = HS mode, no traffic. V _{CC} supply stable, Boost = Max		22	36	mA
I _{HS_SUSPEND}	High Speed Suspend Current	USB channel = HS Suspend mode. V _{CC} supply stable		0.75	1.4	mA
I _{FS}	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V _{CC} supply stable		0.75	1.4	mA
I _{DISCONN}	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I _{SHUTDOWN}	Shutdown Power	RSTN driven low, V _{CC} supply stable		35	95	μA
CONTROL PIN LEAKAGE						
I _{LKG_FS}	Pin failsafe leakage current for SDA, RSTN	V _{CC} = 0 V, pin at V _{IH, max}		10	15	μA
I _{LKG_FS}	Pin failsafe leakage current for BOOST, RX_SEN	V _{CC} = 0 V, pin at V _{IH, max}		6	10	μA
I _{LKG_FS}	Pin failsafe leakage current for SCL	V _{CC} = 0 V, pin at V _{IH, max}			70	nA
INPUT RSTN						
V _{IH}	High level input voltage		1.5		3.6	V
V _{IL}	Low-level input voltage		0		0.5	V
I _{IH}	High level input current	V _{IH} = 3.6 V, R _{PU} enabled			±15	μA
I _{IL}	Low level input current	V _{IL} = 0V, R _{PU} enabled			±20	μA
INPUT RX_SEN (3-level input, for mid level leave pin floating)						
V _{IH}	High level input voltage R _{RXSEN1} =47kΩ, R _{RXSEN2} =10kΩ	V _{CC} ≤4.3V	1.8		3.6	V
V _{IH}	High level input voltage R _{RXSEN1} =37kΩ, R _{RXSEN2} =47kΩ	V _{CC} >4.3V	2.0		3.6	V

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IL}	Low level input voltage 22kΩ ≤ R _{RXSEN1} ≤ 33kΩ				0.4	V
INPUT BOOST						
R _{BOOST_LVL0}	External pulldown resistor for BOOST Level 0				160	Ω
R _{BOOST_LVL1}	External pulldown resistor for BOOST Level 1		1.5	1.8	2	kΩ
R _{BOOST_LVL2}	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	kΩ
R _{BOOST_LVL3}	External pulldown resistor for BOOST Level 3		7.5			kΩ
OUTPUTS CD, ENA_HS						
V _{OH}	High level output voltage	I _O = −50 μA, V _{CC} ≥ 3.0V	2.5			V
V _{OH}	High level output voltage	I _O = −50 μA, V _{CC} = 2.3V	1.8			V
V _{OL}	Low level output voltage	I _O = 50 μA			0.3	V
I²C						
C _{I2C_BUS}	I ² C Bus Capacitance		4		150	pF
I _{OL}	I ² C open drain output current	V _{OL} = 0.4V	1.5			mA
V _{IL}	V _{I2C_BUS} = 1.8V ±10%	R _{Pull-up} = 1.6kΩ to 2.5kΩ, % of V _{I2C_BUS}			25	%
V _{IL}	V _{I2C_BUS} = 3.3V ±10%	R _{Pull-up} = 2.8kΩ to 7kΩ, % of V _{I2C_BUS}			25	%
V _{IH}	V _{I2C_BUS} = 1.8V ±10%	R _{Pull-up} = 1.6kΩ to 2.5kΩ, % of V _{I2C_BUS}	75			%
V _{IH}	V _{I2C_BUS} = 3.3V ±10%	R _{Pull-up} = 2.8kΩ to 7kΩ, % of V _{I2C_BUS}	75			%
R _{Pull-up}	V _{I2C_BUS} = 1.8V ±10%		1.6	2	2.5	kΩ
R _{Pull-up}	V _{I2C_BUS} = 3.3V ±10%		2.8	4.7	7	kΩ
SCL Frequency					100	kHz
DxP, DxM						
C _{IO_DXX}	Capacitance to GND	Measured with VNA at 240 MHz, V _{CC} supply stable, Redriver off		2.5		pF

6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DxP, DxM USB Signals						
F _{BR_DXX}	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V _{CC} supply stable			480	Mbps
t _{R/F_DXX}	Rise/Fall time		100			ps

 (1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER UP TIMING					
T_{RSTN_PW}	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			μ s
T_{STABLE}	VCC must be stable before RSTN de-assertion	300			μ s
T_{READY}	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	μ s
T_{RAMP}	VCC ramp time	0.2		100	ms
I2C (STD)					
t_{SUSTO}	Stop setup time, SCL ($T_r=600$ ns-1000ns), SDA ($T_f=6.5$ ns-106.5ns), 100kHz STD	4			μ s
t_{HDSTA}	Start hold time, SCL ($T_r=600$ ns-1000ns), SDA ($T_f=6.5$ ns-106.5ns), 100kHz STD	4			μ s
t_{SUSTA}	Start setup time, SCL ($T_r=600$ ns-1000ns), SDA ($T_f=6.5$ ns-106.5ns), 100kHz STD	4.7			μ s
t_{SUDAT}	Data input or False start/stop, setup time, SCL ($T_r=600$ ns-1000ns), SDA ($T_f=6.5$ ns-106.5ns), 100kHz STD	250			ns
t_{HDDAT}	Data input or False start/stop, hold time, SCL ($T_r=600$ ns-1000ns), SDA ($T_f=6.5$ ns-106.5ns), 100kHz STD	5			μ s
t_{BUF}	Bus free time between START and STOP conditions	4.7			μ s
t_{LOW}	Low period of the I2C clock	4.7			μ s
t_{HIGH}	High period of the I2C clock	4			μ s
t_F	Fall time of both SDA and SCL signals			300	ns
t_R	Rise time of both SDA and SCL signals			1000	ns

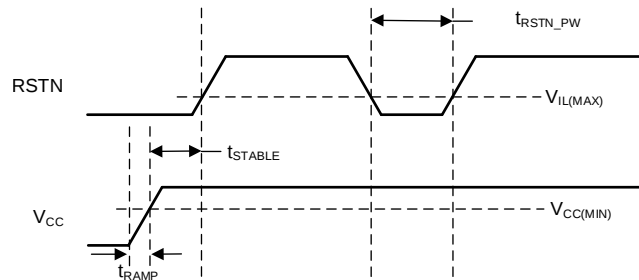


图 1. Power On and Reset Timing

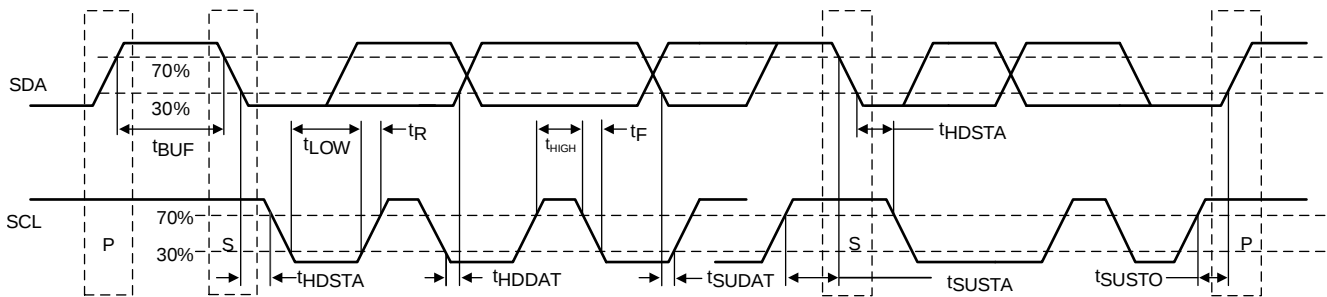


图 2. I2C Timing

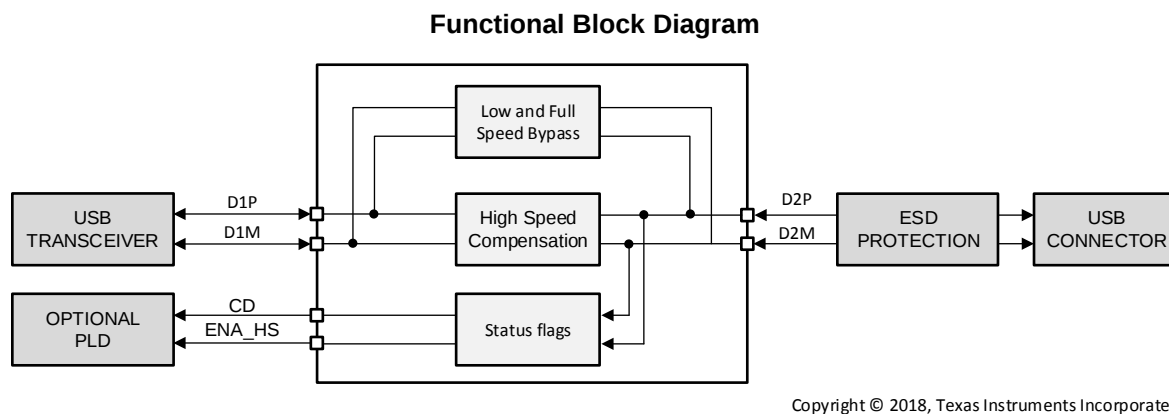
7 Detailed Description

7.1 Overview

The TUSB217-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB217-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB217-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High speed boost

The high speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high speed signals. It is direction independent and by that is compatible to OTG systems. The **BOOST** pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set via I²C register according to [I²C mode](#). Internal circuitry of the signal conditioner reduces possible overshoot.

7.3.2 RX Sensitivity

The **RX_SEN** pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

7.4 Device Functional Modes

7.4.1 Low Speed (LS) mode

TUSB217-Q1 automatically detects a LS connection and does not enable signal compensation. **CD** pin is asserted high but **ENA_HS** will be low.

7.4.2 Full Speed (FS) mode

TUSB217-Q1 automatically detects a FS connection and does not enable signal compensation. **CD** pin is asserted high but **ENA_HS** will be low

Device Functional Modes (continued)

7.4.3 High Speed (HS) mode

TUSB217-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA_HS pin are asserted high when high speed boost is active.

7.4.4 High Speed downstream port electrical compliance test mode

TUSB217-Q1 will detect HS compliance test fixture and enter downstream port high speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB217-Q1 is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB217-Q1 is operating in HS functional mode, TUSB217-Q1 will transition to HS eye compliance test mode and CD asserts low and ENA_HS remains high. When this occurs signal compensation is enabled.

7.4.5 Shutdown mode

TUSB217-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 1. CD and ENA_HS Pins in Different Modes

MODE	CD	ENA_HS
Low speed	HIGH	LOW
Full speed	HIGH	LOW
High speed	HIGH	HIGH
High speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

7.4.6 I²C mode

TUSB217-Q1 supports 100 KHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification 2.1, 2001 – STANDARD MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high speed mode.

7.5 TUSB217 Registers

[Table 2](#) lists the memory-mapped registers for the TUSB217 registers. All register offset addresses not listed in [Table 2](#) should be considered as reserved locations and the register contents should not be modified.

Table 2. TUSB217 Registers

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	Go
0x3	CONFIGURATION	This register is selecting device mode.	Go
0xE	DC_BOOST	This register is setting DC BOOST level.	Go
0x25	RX_SEN	This register is setting RX Sensitivity level.	Go

Complex bit access types are encoded to fit into small table cells. [Table 3](#) shows the codes that are used for access types in this section.

Table 3. TUSB217 Access Type Codes

Access Type	Code	Description
Read Type		
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1 EDGE_BOOST Register (Offset = 0x1) [reset = X]

EDGE_BOOST is shown in [Figure 3](#) and described in [Table 4](#).

Return to [Summary Table](#).

This register is setting EDGE BOOST level.

Figure 3. EDGE_BOOST Register

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

Table 4. EDGE_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting) 0x3 = BOOST PIN LEVEL 1 0x6 = BOOST PIN LEVEL 2 0x8 = BOOST PIN LEVEL 3 0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in [Figure 4](#) and described in [Table 5](#).

Return to [Summary Table](#).

This register is selecting device mode.

Figure 4. CONFIGURATION Register

7	6	5	4	3	2	1	0
RESERVED							CFG_ACTIVE
RH/W-X							RH/W-0x1

Table 5. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

Table 5. CONFIGURATION Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode. 0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

7.5.3 DC_BOOST Register (Offset = 0xE) [reset = X]

DC_BOOST is shown in [Figure 5](#) and described in [Table 6](#).

Return to [Summary Table](#).

This register is setting DC BOOST level.

Figure 5. DC_BOOST Register

7	6	5	4	3	2	1	0
RESERVED				DCB_LVL			
RH/W-X				RH/W-X			

Table 6. DC_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting) 0x2 = BOOST PIN LEVEL 1 and 2 0x6 = BOOST PIN LEVEL 3 0xF = (highest dc boost setting)

7.5.4 RX_SEN Register (Offset = 0x25) [reset = X]

RX_SEN is shown in [Figure 6](#) and described in [Table 7](#).

Return to [Summary Table](#).

This register is setting RX Sensitivity level.

Figure 6. RX_SEN Register

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

Table 7. RX_SEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range 0x0 = RX_SEN LEVEL LOW 0x44 = RX_SEN LEVEL MID 0x77 = RX_SEN LEVEL HIGH 0xFF = (highest setting)

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

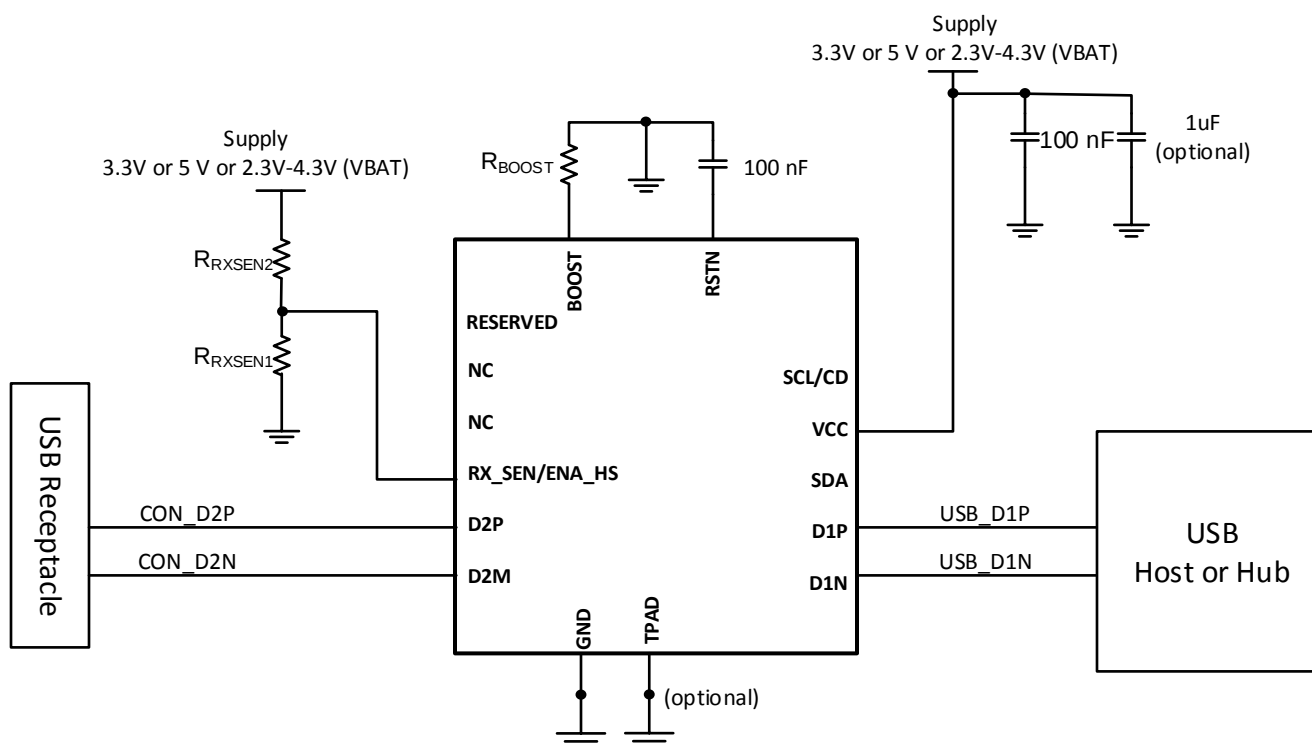
8.1 Application Information

The purpose of the TUSB217-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB217-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB217-Q1 to control other blocks on the customer platform, if so desired.

8.2 Typical Application

A typical application is shown in [Figure 7](#). In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



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Figure 7. Reference Schematic (design example)

Typical Application (continued)

8.2.1 Design Requirements

TUSB217-Q1 requires a valid reset signal as described in the *power supply recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in 表 8, 表 9 and 表 10

表 8. Design Parameters for 5 V Supply with High Loss System

PARAMETER				VALUE ⁽¹⁾
V _{CC}				5 V ±10%
I ² C support required in system (Yes/No)				No
Edge and DC Boost	R_{BOOST}		BOOST Level	Boost Level 1: R _{BOOST} = 1.8 kΩ
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
	Do Not Install (DNI)		3	
RX Sensitivity	R_{RXSEN1}	R_{RXSEN2}	RX_SEN Level	High RX Sensitivity Level: R _{RXSEN1} = 37 kΩ R _{RXSEN2} = 47 kΩ
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 kΩ ⁽²⁾	47 kΩ	High	

- (1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 5V supply system could be applicable to 3.3V supply system as well.
- (2) This resistor is needed for a 5V supply to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

表 9. Design Parameters for 3.3 V Supply with Low to Medium Loss System

PARAMETER				VALUE ⁽¹⁾
V _{CC}				3.3 V ±10%
I ² C support required in system (Yes/No)				No
Edge and DC Boost	R_{BOOST}		BOOST Level	Boost Level 0: R _{BOOST} = 0-Ω
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
	Do Not Install (DNI)		3	
RX Sensitivity	R_{RXSEN1}	R_{RXSEN2}	RX_SEN Level	Medium RX Sensitivity Level: R _{RXSEN1} = DNI R _{RXSEN2} = DNI
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ - 33 kΩ (27 kΩ typical)	High	

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system could be applicable to 5V supply system as well.

表 10. Design Parameters for 2.3V - 4.3V VBAT Supply with Low to Medium Loss System

PARAMETER				VALUE ⁽¹⁾
V _{CC}				2.3 V to 4.3V
I ² C support required in system (Yes/No)				No
Edge and DC Boost	R _{BOOST}		BOOST Level	Boost Level 0: R _{BOOST} = 0-Ω
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
	Do Not Install (DNI)		3	
RX Sensitivity	R _{RXSEN1}	R _{RXSEN2}	RX_SEN Level	Medium RX Sensitivity Level: R _{RXSEN1} = DNI R _{RXSEN2} = DNI
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 kΩ ⁽²⁾	10 kΩ	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 2.3V-4.3V supply system could be applicable to 5V supply system as well.

(2) This resistor is needed for a VBAT supply (2.3V - 4.3V) to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. if permissible. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level 1.

In order for the TUSB217-Q1 to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

注

The TUSB217-Q1 compensates for extra attenuation in the signal path according to the configuration of the RX_SEN pin. This pin is not 5 V tolerant and therefore when selecting the highest RX sensitivity level, the voltage level at RX_SEN pin must be less than 3.6V.

Placement of the device is also dependent on the application goal. 表 11 summarizes our recommendations.

表 11. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB217-Q1 PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB217s to improve device enumeration	Midway between each USB interconnect

表 12. Table of Recommended Settings

BOOST and RX_SEN settings ⁽¹⁾ for channel loss		
Pre-channel cable length (Between USB PHY and TUSB217-Q1)	BOOST	RX_SEN
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB217-Q1 and inter-connect)	BOOST	RX_SEN
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host and/or device as well as cable length and loss profile.

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

注

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB217-Q1
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB217-Q1. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

TUSB217-Q1

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8.2.3 Application Curves

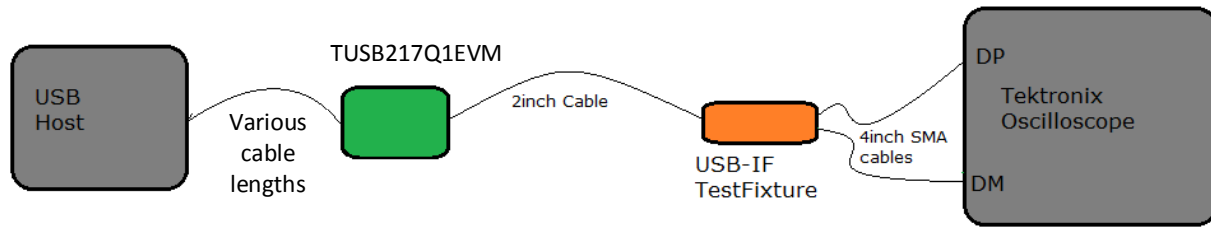


图 8. Near End Eye Measurement Set up With Pre-channel Cable

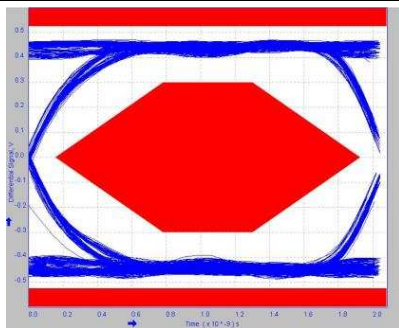


图 9. 6 inches without TUSB217-Q1

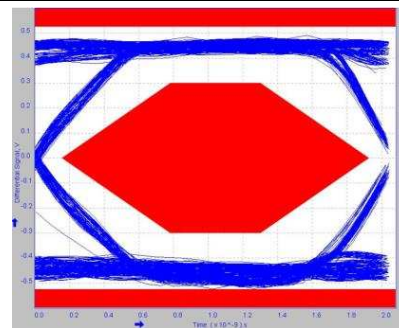


图 10. 6 inches pre-channel with TUSB217-Q1 BOOST=0
RX_SEN=MED

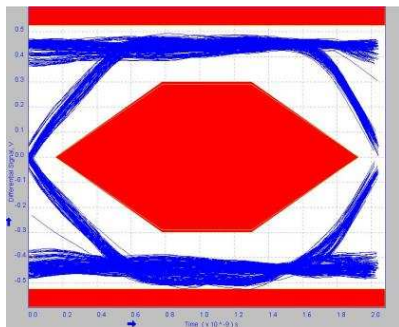


图 11. 6 inches pre-channel with TUSB217-Q1 BOOST=0
RX_SEN=HIGH

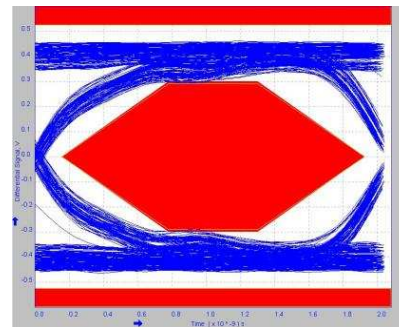


图 12. 3 meter without TUSB217-Q1

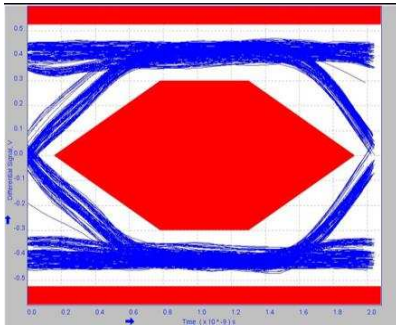


Figure 13. 3 meter pre-channel with TUSB217-Q1 BOOST=0
RX_SEN=MED

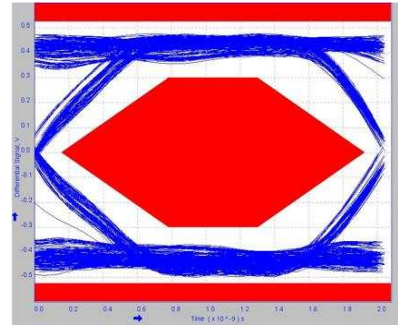


Figure 14. 3 meter pre-channel with TUSB217-Q1 BOOST=0
RX_SEN=HIGH

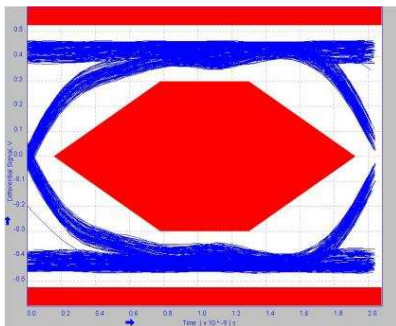


Figure 15. 2 meter without TUSB217-Q1

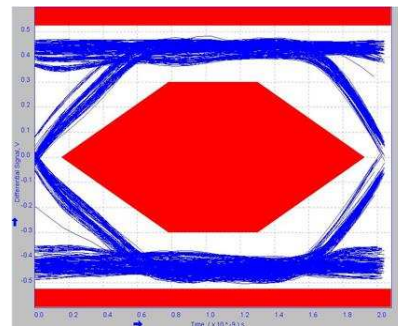


Figure 16. 2 meter pre-channel with TUSB217-Q1 BOOST=1
RX_SEN=MED

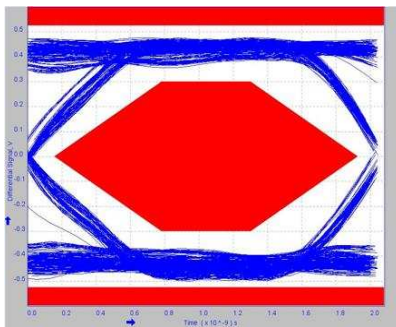


Figure 17. 2 meter pre-channel with TUSB217-Q1 BOOST=1
RX_SEN=HIGH

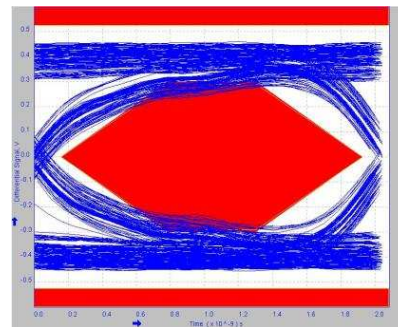


Figure 18. 5 meter without TUSB217-Q1

TUSB217-Q1

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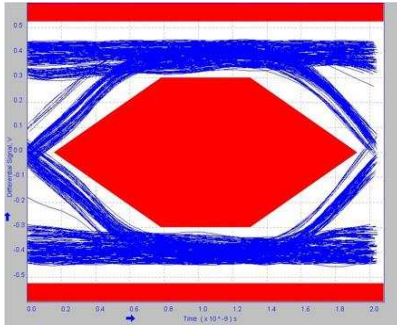


Figure 19. 5 meter pre-channel with TUSB217-Q1 BOOST=1
RX_SEN=MED

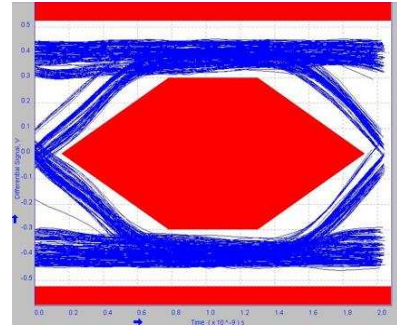
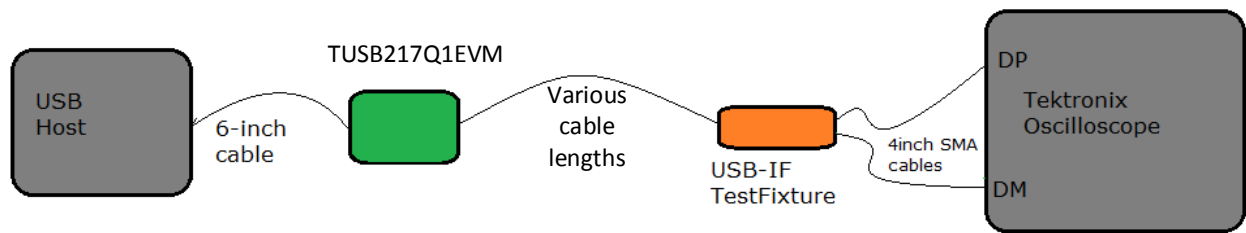
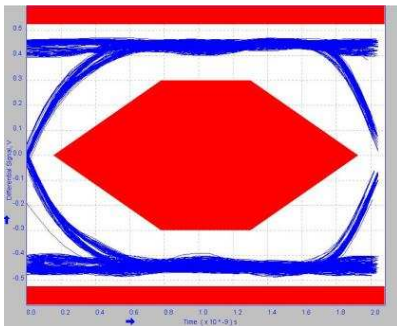


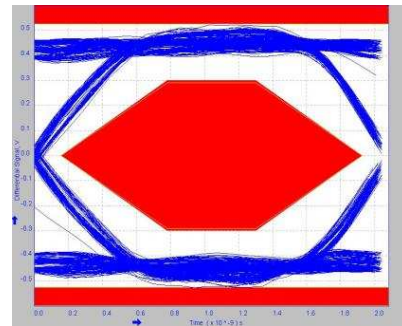
Figure 20. 5 meter pre-channel with TUSB217-Q1 BOOST=1
RX_SEN=HIGH



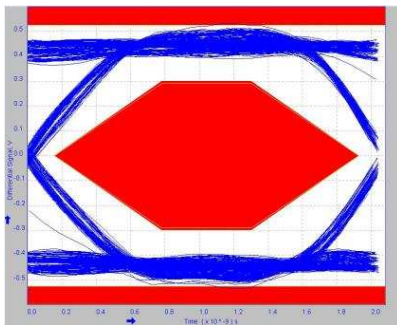
✎ 21. Near end eye measurement set up with post-channel cable



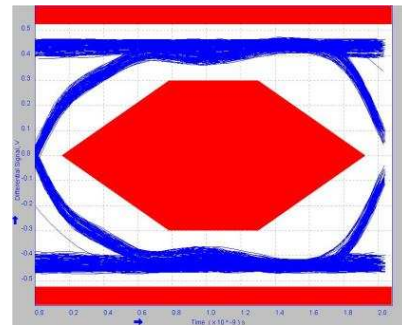
✎ 22. 6 inches without TUSB217-Q1



✎ 23. 6 inches post-channel with TUSB217-Q1 BOOST=0
RX_SEN=MED



✎ 24. 6 inches post-channel with TUSB217-Q1 BOOST=0
RX_SEN=HIGH



✎ 25. 1 meter without TUSB217-Q1

TUSB217-Q1

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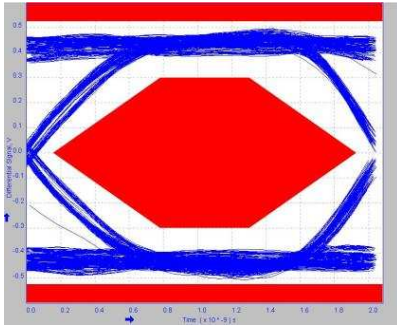


図 26. 1 meter post-channel with TUSB217-Q1 BOOST=0
RX_SEN=MED

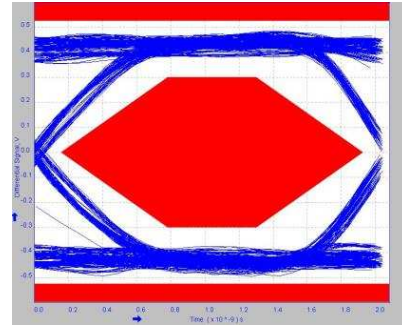


図 27. 1 meter post-channel with TUSB217-Q1 BOOST=0
RX_SEN=HIGH

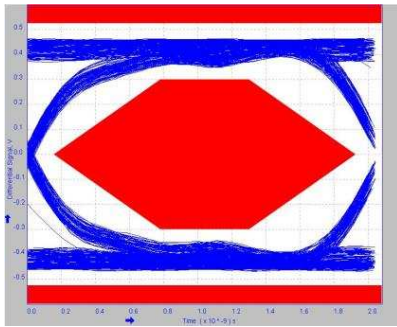


図 28. 2 meter without TUSB217-Q1

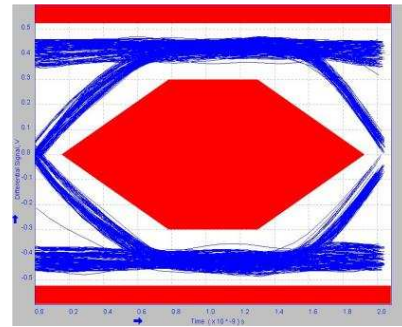


図 29. 2 meter post-channel with TUSB217-Q1 BOOST=1
RX_SEN=MED

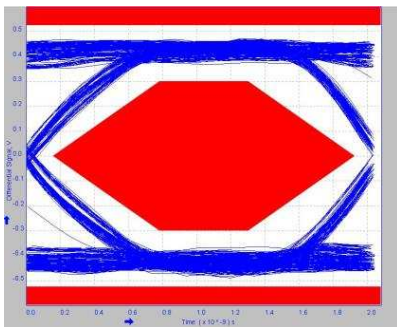


図 30. 2 meter post-channel with TUSB217-Q1 BOOST=1
RX_SEN=HIGH

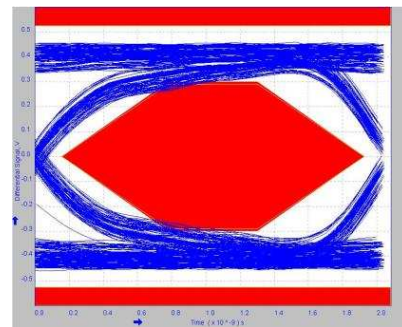


図 31. 4 meter without TUSB217-Q1

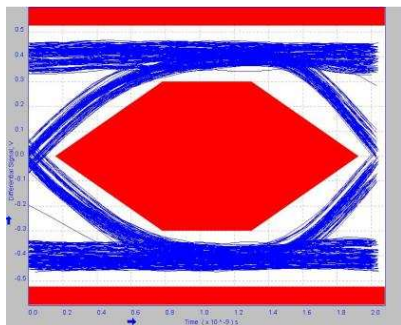


図 32. 4 meter post-channel with TUSB217-Q1 BOOST=1
RX_SEN=MED

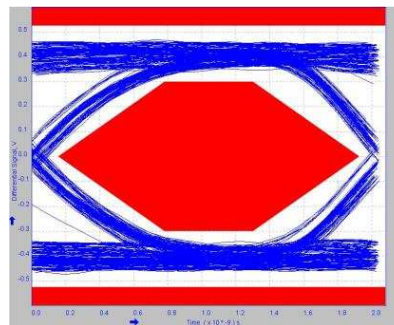


図 33. 4 meter post-channel with TUSB217-Q1 BOOST=1
RX_SEN=HIGH

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 k Ω , the recommended minimum external capacitance is calculated as:

$$[\text{Ramp Time} \times 5] \div [500 \text{ k}\Omega] \quad (1)$$

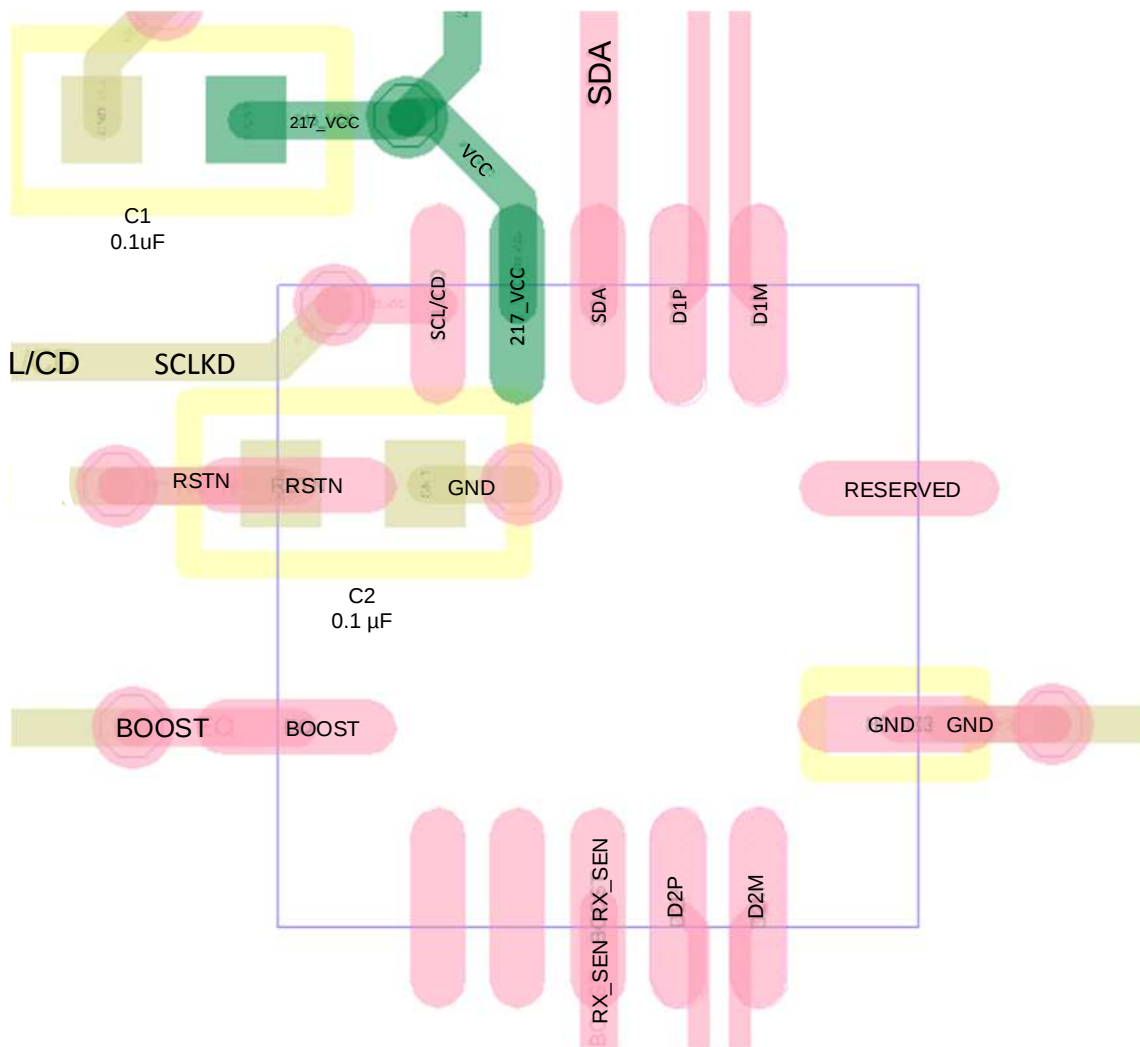
10 Layout

10.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

All dimensions are in millimetres (mm).

10.2 Layout Example



✎ 34. Layout Example (thermal pad grounding is optional)

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.

11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

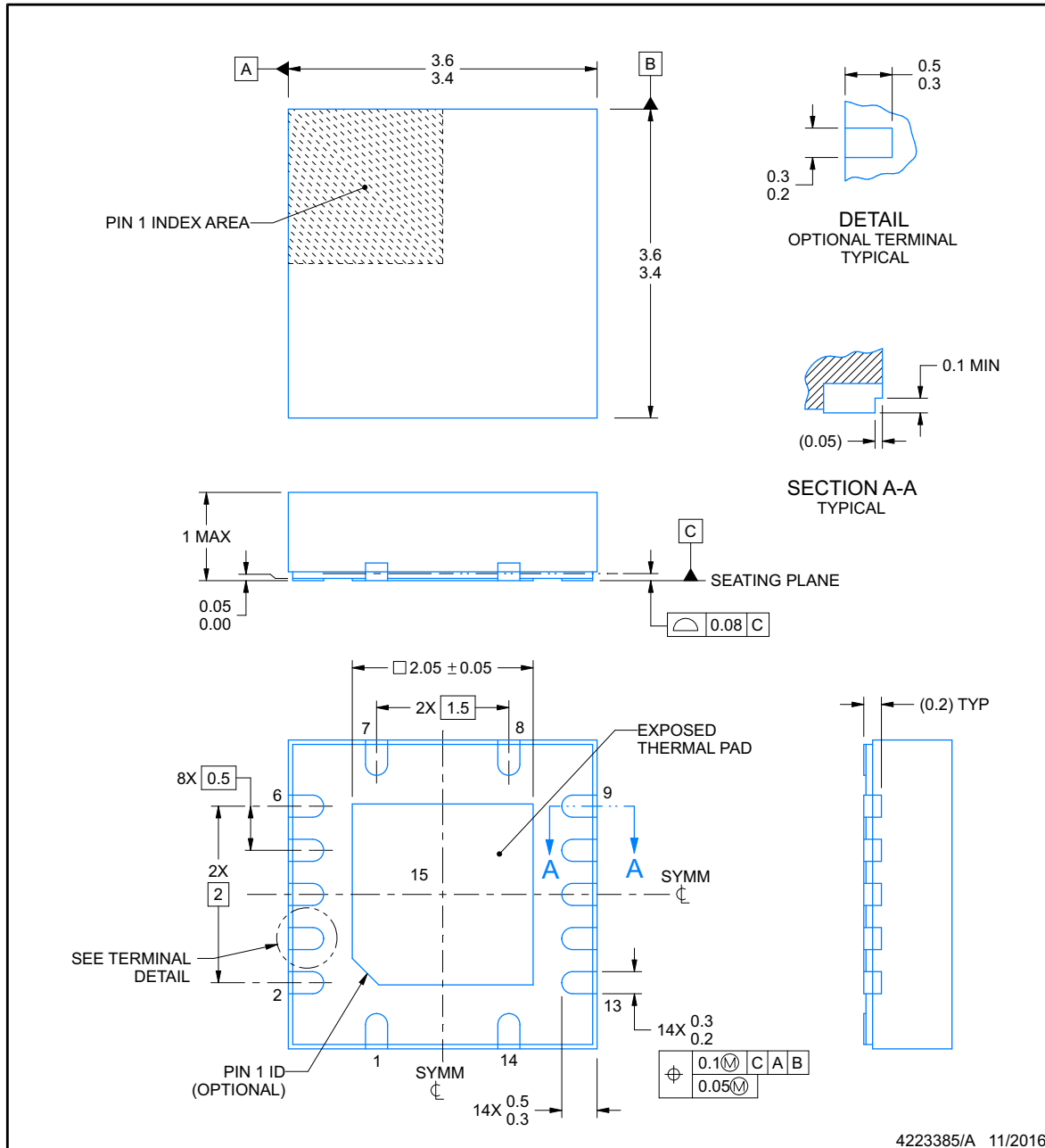
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


RGY0014B
PACKAGE OUTLINE
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223385/A 11/2016

NOTES:

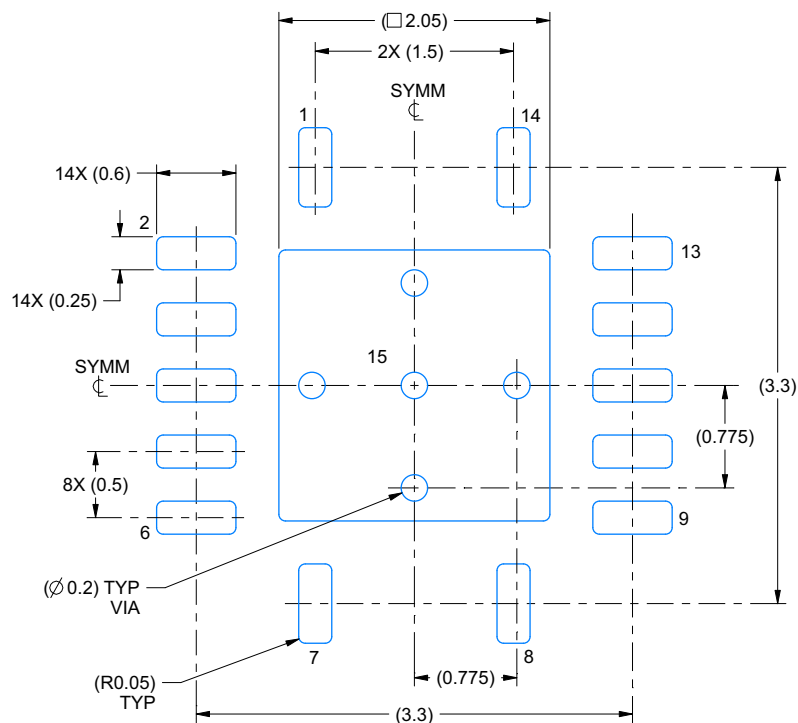
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

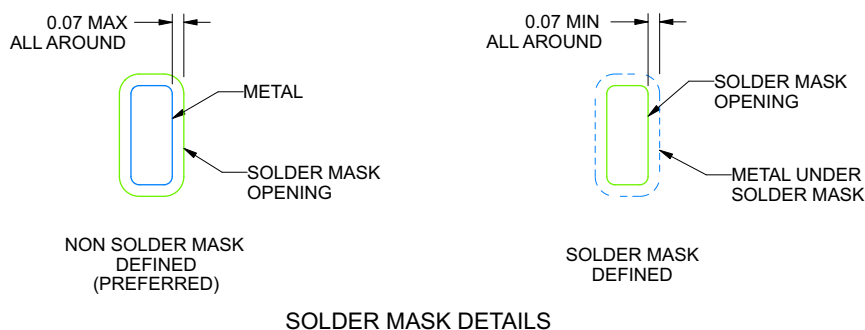
RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4223385/A 11/2016

NOTES: (continued)

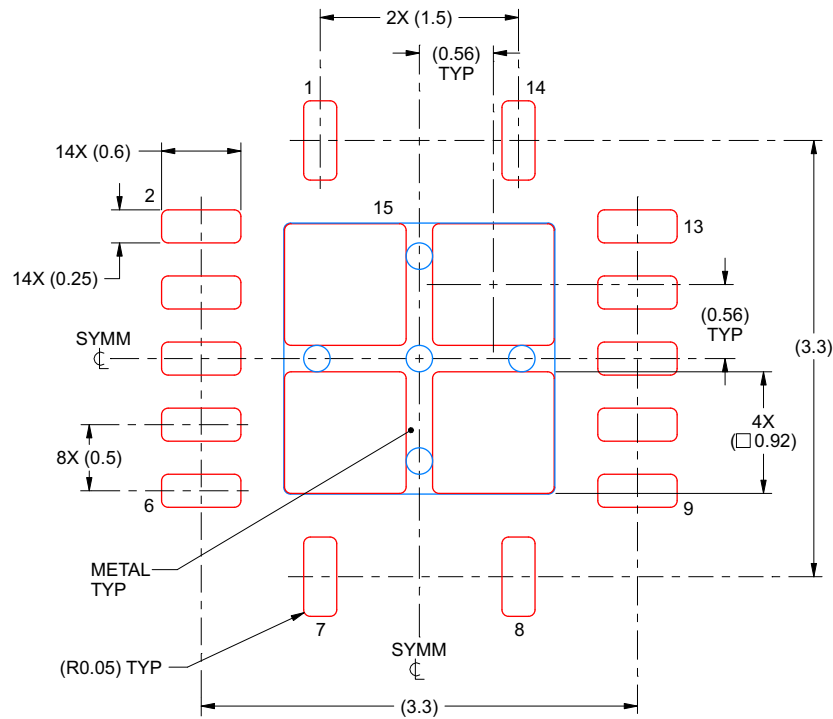
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223385/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB217RGYRQ1	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1
TUSB217RGYRQ1.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	U217Q1
TUSB217RGYTQ1	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1
TUSB217RGYTQ1.A	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	U217Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB217RGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB217RGYTQ1	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB217RGYRQ1	VQFN	RGY	14	3000	367.0	367.0	35.0
TUSB217RGYTQ1	VQFN	RGY	14	250	210.0	185.0	35.0

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