TSM36A SOT-23 パッケージのサージ保護デバイス

1 特長

- 産業用信号ライン向け 1.7kV、42Ω の IEC 61000-4-5 サージ・テストに耐える単方向のサージ保護機能
- 強力なサージ保護:
  - IEC61000-4-5 (8/20µs):41A
- 25A でクランプ電圧が 50V と低く、8/20µs のサージ電流で下流の部品を保護
- 動作電圧が 36V で、24V システムの信号を保護
- 小さいリーク電流:1µA
- 低い動的抵抗:0.5Ω
- レベル 4 IEC 61000-4-2 に準拠した ESD 保護機能を内蔵
- 30kV の ESD 保護 (IEC 61000-4-2)
- SOT-23 (DBZ):小型、標準、共通フットプリント
- 自動光学検査 (AOI) に適したリード付きパッケージ

2 アプリケーション

- 産業機器用センサ
- IO-Link
- PLC I/O モジュール
- 24V の電源ライン、またはデジタル入出力ライン
- 4/20mA ループ
- 家電製品
- 医療用機器
- モーター・ドライバ

3 概要

TSM36A はテキサス・インスツルメンツのサージ保護デバイス・ファミリの一部です。TSM36A は、最大 41A の IEC 61000-4-5 フォルト電流を確実に分流して、システムを大電力の過渡や落雷から保護します。本デバイスは、一般的な産業用信号ラインの EMC 要件向けのソリューションとして、42Ω のインピーダンスにより結合される、最大 1.7kV の IEC 61000-4-5 開路電圧に耐えられます。サージ・イベントでは TSM36A がクランプされるため、I_{PP} = 25A でシステムがさらされる電圧を 50V 未満にします。

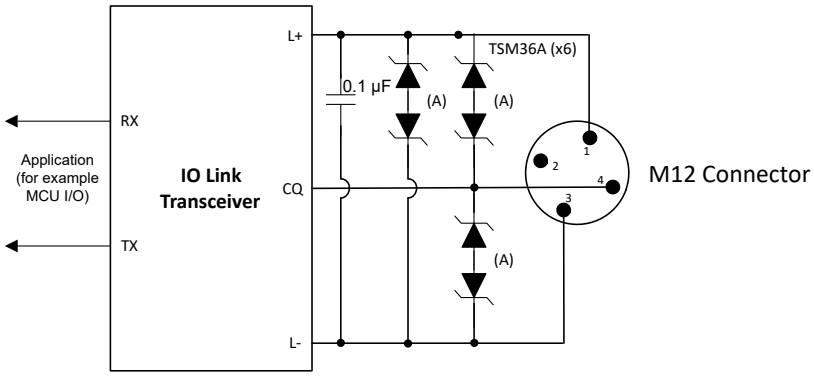
また、TSM36A は、業界標準の SMA パッケージに比べて約 50% 小型化された小型のリード付き SOT-23 (DBZ) パッケージで供給されています。リーク電流と容量が極めて小さいため、保護するラインへの影響も最小限に抑えられます。

サージ・ファミリに属する他のデバイスの詳細については、このリンクに掲載されている製品をご覧ください。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TSM36A	DBZ (SOT-23、3)	2.92mm × 1.30mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. この図は、2 つの TSM36A 単方向デバイスを直列に接続し、各信号間を保護するため陽極を双方向で結合した状態を示しています。

産業用センサの IO-Link アプリケーション

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2022) to Revision A (October 2022)	Page
• データシートのステータスを「事前情報」から「*量産データ*」に変更	1

5 Pin Configuration and Functions

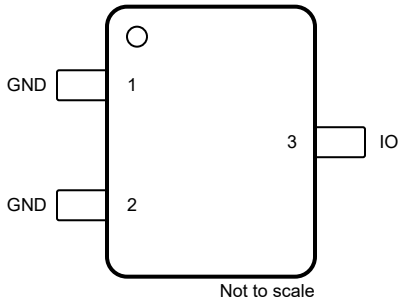


**図 5-1. DBZ Package,
3-Pin SOT-23
(Top View)**

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	3	I/O	Surge and ESD protected IO
GND	1, 2	G	Connect to ground. To achieve the rated performance, it is required to connect pin 1 and 2 together on the PCB as close to the device as possible.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

Parameter		Device	MIN	MAX	UNIT
$P_{pk\_8\_20}$	IEC 61000-4-5 Power (t_p - 8/20 µs)	TSM36A		2000	W
$I_{pp\_8\_20}$	IEC 61000-4-5 Current (t_p - 8/20 µs)	TSM36A		41	A
T_A	Operating free-air temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

6.3 ESD Ratings—IEC Specification

T_A = 25°C (unless otherwise noted)

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		36	V
T_A	Operating free-air temperature	–55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		TSM36A DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Device	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		TSM36A	0		36	V
V_{BRF}	Forward breakdown voltage(1)	I_{IO} = –10 mA	TSM36A		0.8		V
V_{BRR}	Reverse breakdown voltage(1)	I_{IO} = 10 mA	TSM36A	37.8		44.2	V
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 25A, t_p = 8/20 µs, from IO to GND	TSM36A		50		V
		I_{PP} = 40 A, t_p = 8/20 µs, from IO to GND	TSM36A		57		
I_{LEAK}	Leakage current	V_{IO} = +36 V	TSM36A			1	µA
R_{DYN}	Dynamic resistance	t_p = 8/20 µs, from IO to GND	TSM36A		0.5		Ω
C_{IO-GND}	Line capacitance	V_{IO} = 0 V, f = 1 MHz, V_{p-p} = 30 mV	TSM36A		50	80	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.

6.7 Typical Characteristics

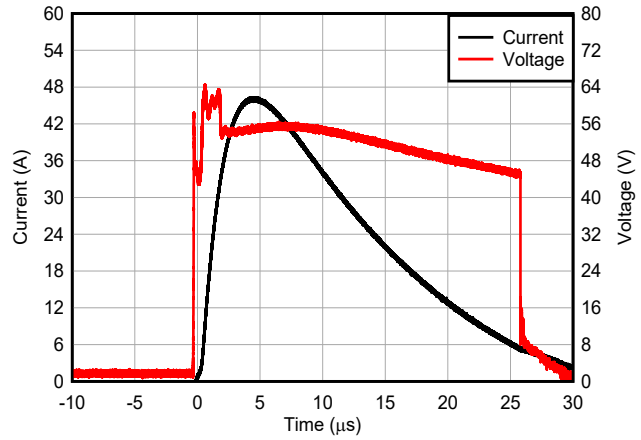


図 6-1. 8/20 µs Surge Response

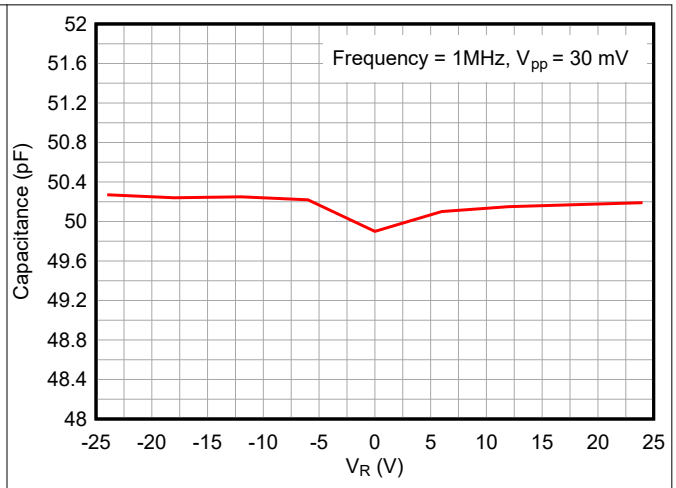


図 6-2. Capacitance vs Bias Voltage

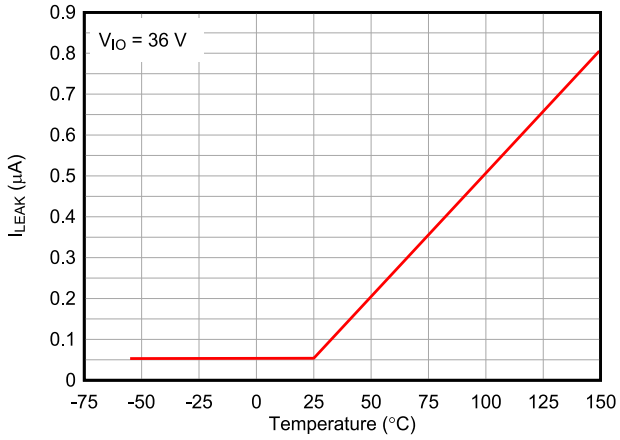


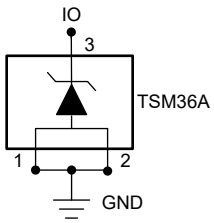
図 6-3. Leakage vs Temperature

7 Detailed Description

7.1 Overview

The TSM36A is a surge protection diode that clamps the voltage during a fault and protects downstream components from overvoltage events.

7.2 Functional Block Diagram



7.3 Feature Description

The TSM36A is a surge protection diode that handles 41 A of IEC 61000-4-5 8/20 µs surge current. The low clamping voltage protects downstream circuits from being stressed during a surge event. The TSM36A has minimal leakage current at the standoff voltage of 36 V, making it a good candidate for applications where low leakage is needed to reduce power dissipation. A 30-kV IEC 61000-4-2 rating makes it a robust protection solution for ESD events as well. The TSM36A has a wide ambient temperature range of –55°C to +150°C which enables it to work in applications requiring an extended temperature range. The small SOT-23 (DBZ) package enables it to save board area compared to other surge protection devices in a traditional SMA package. The leaded SOT-23 (DBZ) package enables automatic optical inspection during the assembly process.

7.4 Device Functional Modes

7.4.1 Protection Specifications

The TSM36A is specified according to both the IEC 61000-4-5 standard. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs.

Additionally, the TSM36A is tested according to IEC 61000-4-5 to pass a ±1.7 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, which is a common test requirement for industrial signal I/O lines. The TSM36A will serve as a protection solution for applications with that requirement.

The TSM36A integrates 30-kV IEC 61000-4-2 rated ESD protection, which ensures that the device can protect against both surge and ESD transient events.

For more information on TI's test method for surge and ESD testing, reference *TI's IEC 61000-4-x Testing* application note.

8 Application and Implementation

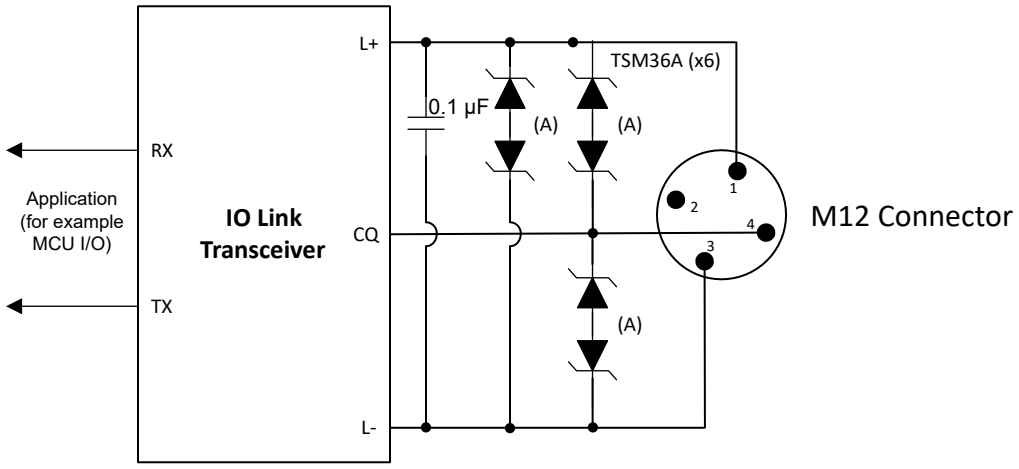
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TSM36A can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

8.2 Typical Application



A. Diagram shows two TSM36A unidirectional devices stacked in series with the anodes tied back-to-back to protect between the respective signals.

図 8-1. TSM36A Application Schematic

8.2.1 Design Requirements

In the previous example, the TSM36A is protecting an IO Link tranceiver that has a nominal voltage of 24 V and a maximum input voltage of 30 V. Most industrial interfaces such as this require protection against ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, equaling approximately 24 A of surge current. If a surge event caused by lightning, coupling, ringing, or any other fault condition occurs without any input protection, then this input voltage will rise to hundreds of volts in microseconds, which violates the absolute maximum input voltage and will harm the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system.

8.2.2 Detailed Design Procedure

If the TSM36A is protecting the device, then during a surge event the voltage will rise to the breakdown of the diode at 37.8 V (minimum), the TSM36A will turn on and shunt the surge current to ground. With the low dynamic resistance of the TSM36A, large amounts of surge current will have some impact on the clamping voltage. The dynamic resistance of the TSM36A is around 0.5 Ω, which means 24 A of surge current will cause a voltage rise of 24 A × 0.5 Ω = 12 V. Because the device turns on at 37.8 V (minimum), the IO Link transceiver input will be exposed to 37.8 V + 12 V = 49.8 V during surge pulses, which is well within the absolute maximum voltage of the IO Link transceiver input pins (L+, L-, and CQ) and will protect the circuit. The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the SOT-23 package allows the device to be placed extremely close to the input connector, lowering the length of the fault current path through the system compared to larger protection solutions. Finally, the low leakage of the TSM36A will have low input power losses. The device will receive a maximum of 1 µA leakage at 36 V for a constant power dissipation of 36 µW; a small quantity that will minimally effect overall efficiency metrics and heating concerns.

8.2.3 Configuration Options

The TSM36A can either be used in an unidirectional or bidirectional configuration. For bidirectional operation, place two TSM36A devices in series with reverse orientation, which allows a working voltage of ±36 V. TSM36A bidirectional operation is similar to its unidirectional operation, but with a minor increase in breakdown voltage and clamping voltage.

9 Power Supply Recommendations

This is a passive TVS diode-based surge protection device; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- For optimal performance, place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Pin 1 and 2 are not internally connected. To achieve the rated performance, it is required to connect Pin 1 and 2 together on the PCB as close to the device as possible and route the signal to ground. Also use a thick and short trace for this return path.

10.2 Layout Example

The following is a typical example of the layout routing for the TSM36A undirectional device.

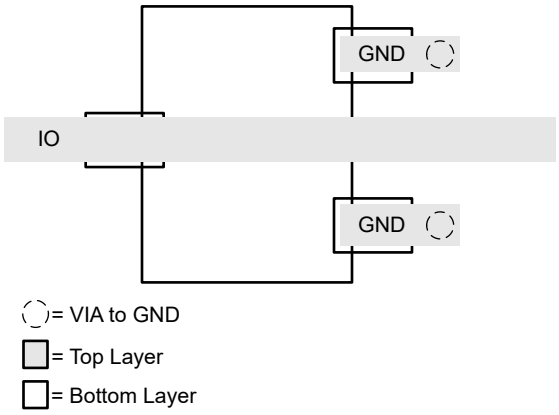


図 10-1. Routing with DBZ Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TI's IEC 61000-4-x Testing* application note
- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSM36ADBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2O98
TSM36ADBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2O98

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TSM36A :

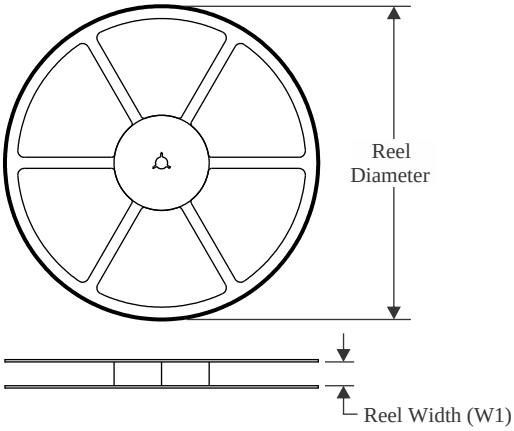
- Automotive : TSM36A-Q1

NOTE: Qualified Version Definitions:

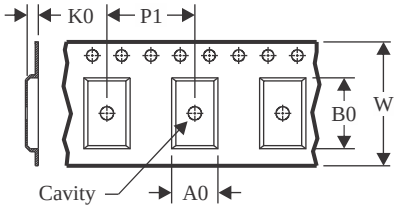
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

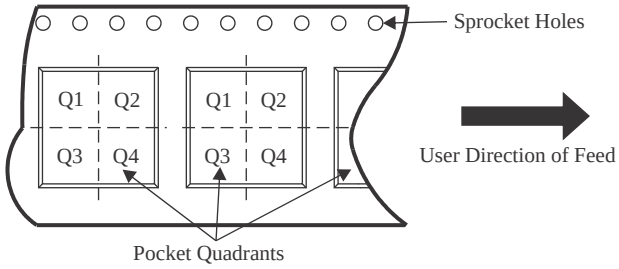


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

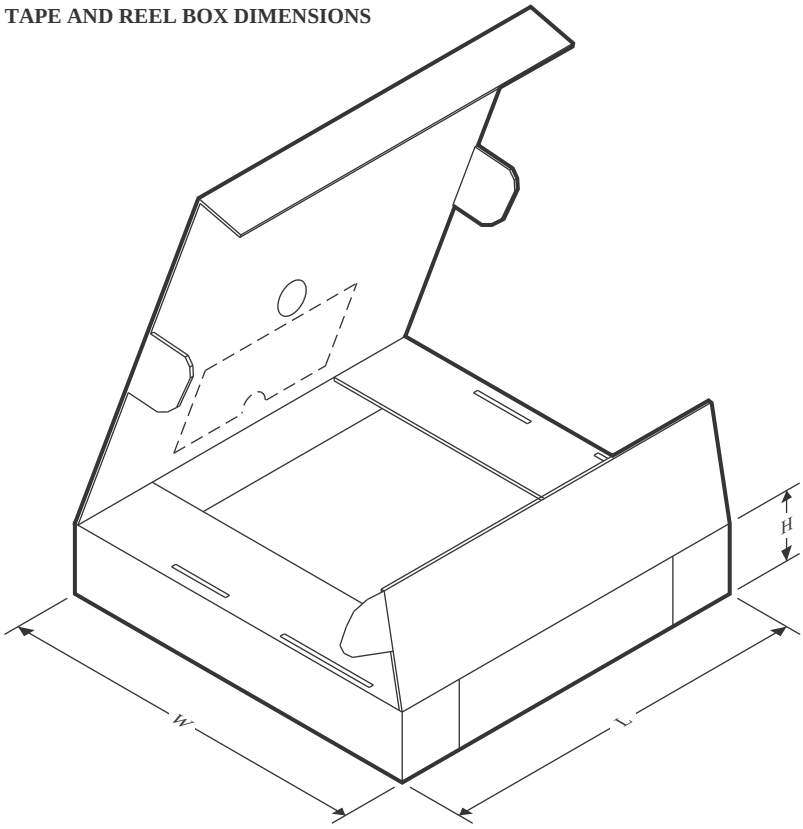
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM36ADBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

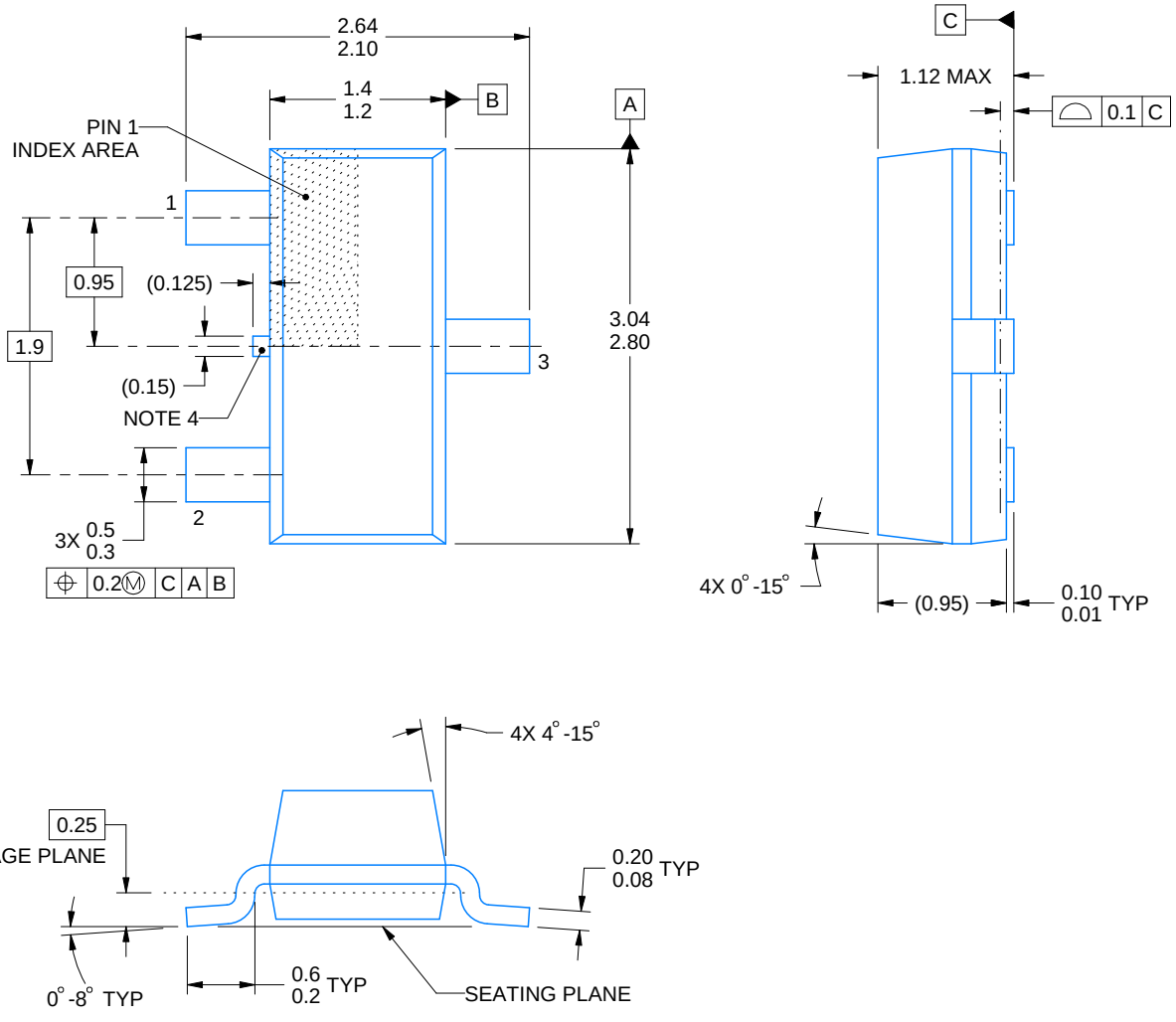
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM36ADBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

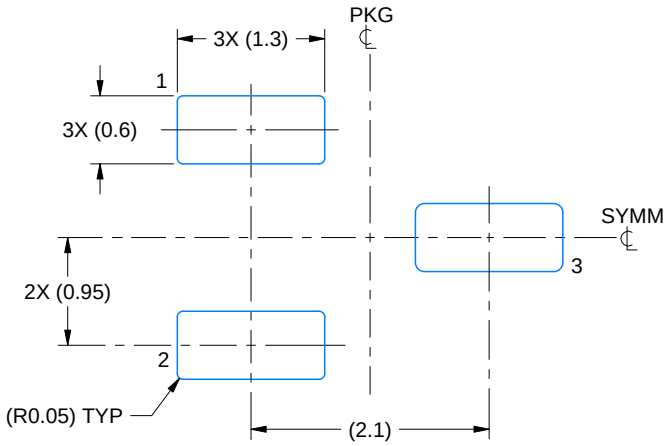
SMALL OUTLINE TRANSISTOR



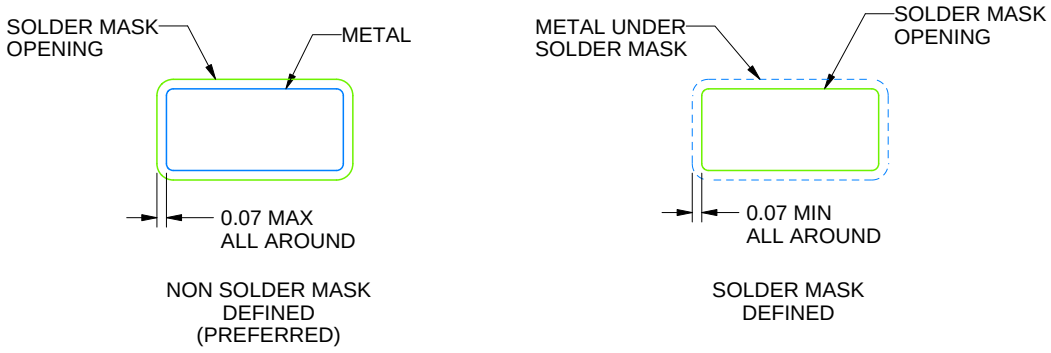
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

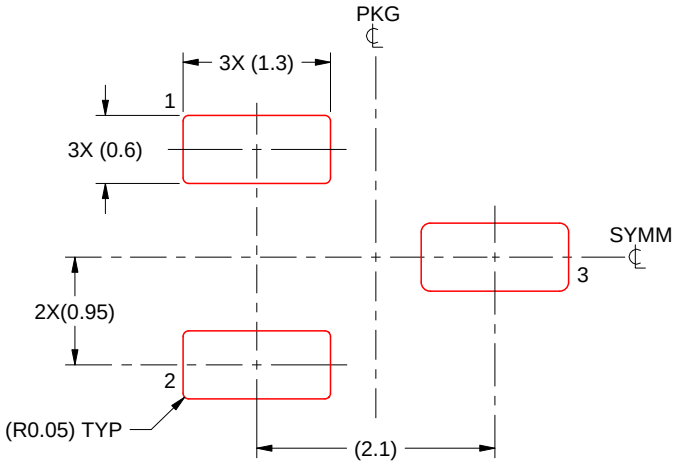


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265