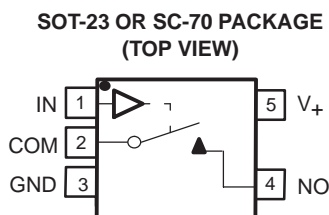


## Description

The TS5A4596 is a single-pole single-throw (SPST) analog switch that is designed to operate from 2 V to 5 V. This device can handle both digital and analog signals, and signals up to  $V_+$  (peak) can be transmitted in either direction.

## Applications

- Sample-and-Hold Circuit
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits



**FUNCTION TABLE**

IN	NO TO COM, COM TO NO
L	OFF
H	ON

## Features

- Low ON-State Resistance (8 Ω)
- ON-State Resistance Flatness (1.5 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection (5 pC Max)
- 450-MHz –3-dB Bandwidth at 25°C
- Low Total Harmonic Distortion (THD) (0.04%)
- 2-V to 5.5-V Single-Supply Operation
- –85-dB OFF-Isolation at 1 MHz
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- 0.5-nA Max OFF Leakage
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- TTL/CMOS-Logic Compatible

## Summary of Characteristics

$V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance ( $r_{ON}$ )	8 Ω
ON-state resistance flatness ( $r_{ON(flat)}$ )	1.5 Ω
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	17 ns/14 ns
Charge injection ( $Q_C$ )	5 pC
Bandwidth (BW)	450 MHz
OFF isolation ( $O_{ISO}$ )	–85 dB at 1 MHz
Total harmonic distortion (THD)	0.04%
Leakage current ( $I_{COM(OFF)}/I_{NO(OFF)}$ )	±0.5 nA
Power-supply current ( $I_+$ )	0.25 μA
Package option	5-pin SOT-23 or SC-70

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	SOT (SOT-23) – DBV	Tape and reel	TS5A4596DBVR	JSC_
	SOT (SC-70) – DCK	Tape and reel	TS5A4596DCKR	JU_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

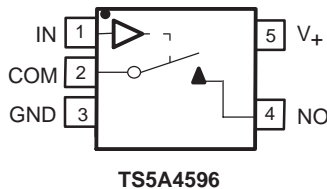
# TS5A4596

## 8-Ω SPST ANALOG SWITCH

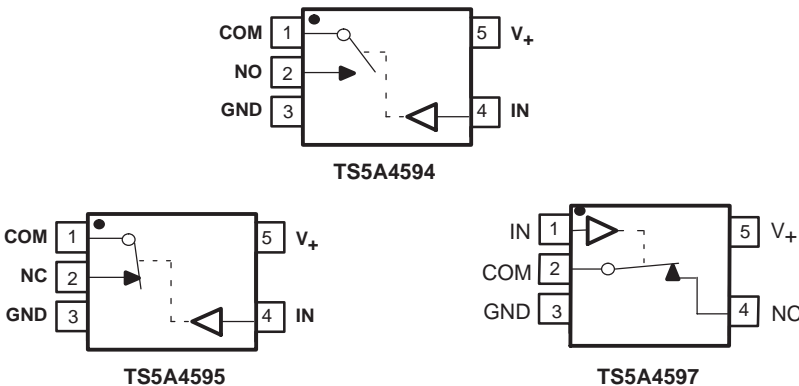
### 5-V/3.3-V SINGLE-CHANNEL ANALOG SWITCH

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#### Pin Configurations



#### Available in Other Pin Configurations



#### Absolute Minimum and Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	-0.3	6	V
$V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3)(4)</sup>	-0.3	$V_+ + 0.3$	V
$I_K$	Analog port diode current $V_{NO}, V_{COM} < 0$	-50		mA
$I_{NO}$ $I_{COM}$	On-state switch current $V_{NO}, V_{COM} = 0$ to $V_+$	-20	20	mA
$I_{NO}$ $I_{COM}$	On-state switch current (pulsed at 1 ms, 10% duty cycle) $V_{NO}, V_{COM} = 0$ to $V_+$	-40	40	mA
$V_I$	Digital input voltage range <sup>(3)(4)</sup>	-0.3	6	V
$I_{IK}$	Digital input clamp current $V_I < 0$	-50		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	-100		mA
$\theta_{JA}$	Package thermal impedance <sup>(5)</sup>	DBV package		206
		DCK package		252
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(5) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$V_{NO} = 3.5 \text{ V}$ , $I_{COM} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V		5	8 10	Ω
ON-state resistance flatness	$r_{on(flat)}$	$V_{NO} = 1.5 \text{ V}, 2.5 \text{ V}, 3.5 \text{ V}$ , $I_{COM} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V		0.5	1.5 2	Ω
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1 \text{ V}, V_{COM} = 4.5 \text{ V}$ , or $V_{NO} = 4.5 \text{ V}, V_{COM} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-0.5 -5	0.01	0.5 5	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}, V_{NO} = 4.5 \text{ V}$ , or $V_{COM} = 4.5 \text{ V}, V_{NO} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-0.5 -5	0.01	0.5 5	nA
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}, V_{COM} = 1 \text{ V}$ , or $V_{NO} = 4.5 \text{ V}, V_{COM} = 4.5 \text{ V}$ , or $V_{NO} = 1 \text{ V}, 4.5 \text{ V}, V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-1 -10	0.01	1 10	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}, V_{NO} = 1 \text{ V}$ , or $V_{COM} = 4.5 \text{ V}, V_{NO} = 4.5 \text{ V}$ , or $V_{COM} = 1 \text{ V}, 4.5 \text{ V}, V_{NO} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-1 -10	0.01	1 10	nA
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		2.4		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_+ \text{ or } 0$	25°C Full	5.5 V	-0.5 -5	0.01	0.5 5	nA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**TS5A4596**  
**8-Ω SPST ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL ANALOG SWITCH**

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**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = 3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V		12	17	ns
			Full	4.5 V to 5.5 V			19	
Turn-off time	$t_{OFF}$	$V_{COM} = 3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V		9	14	ns
			Full	4.5 V to 5.5 V			17	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See Figure 20	25°C	5 V		2	5	pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, $f = 1\text{ MHz}$ , Switch OFF, See Figure 16	25°C	5 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, $f = 1\text{ MHz}$ , Switch OFF, See Figure 16	25°C	5 V		6.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, $f = 1\text{ MHz}$ , Switch ON, See Figure 16	25°C	5 V		13		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, $f = 1\text{ MHz}$ , Switch ON, See Figure 16	25°C	5 V		13		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	5 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Signal = 0 dBm, Switch ON, See Figure 18	25°C	5 V		450		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $V_{NO} = 1\text{ V}_{RMS}$ , $f = 1\text{ MHz}$ , Switch OFF, See Figure 19	25°C	5 V		-85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{SOURCE} = 5\text{ V}_{p-p}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 21	25°C	5 V		0.04		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V		0.01	0.25	$\mu\text{A}$
			Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 3-V Supply<sup>(1)</sup>

$V_+ = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$V_{NO} = 1.5 \text{ V}$ , $I_{COM} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.7 V		9.5	16 20	Ω
ON-state resistance flatness	$r_{on(Flat)}$	$V_{NO} = 1.5 \text{ V}, 2.5 \text{ V}$ , $I_{COM} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.7 V		1.8	6 7	Ω
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1 \text{ V}, V_{COM} = 3 \text{ V}$ , or $V_{NO} = 3 \text{ V}, V_{COM} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}, V_{NO} = 3 \text{ V}$ , or $V_{COM} = 3 \text{ V}, V_{NO} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}, V_{COM} = 1 \text{ V}$ , or $V_{NO} = 3 \text{ V}, V_{COM} = 3 \text{ V}$ , or $V_{NO} = 1 \text{ V}, 3 \text{ V}, V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-1 -10	0.01	1 10	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}, V_{NO} = 1 \text{ V}$ , or $V_{COM} = 3 \text{ V}, V_{NO} = 3 \text{ V}$ , or $V_{COM} = 1 \text{ V}, 3 \text{ V}, V_{NO} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-1 -10	0.01	1 10	nA
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		2		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_+ \text{ or } 0$	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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**8-Ω SPST ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL ANALOG SWITCH**

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**Electrical Characteristics for 3-V Supply<sup>(1)</sup> (continued)**

$V_+ = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = 2 \text{ V}$ , $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	3 V		20	30	ns
			Full	2.7 V to 3.6 V			35	
Turn-off time	$t_{OFF}$	$V_{NO} = 2 \text{ V}$ , $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	3 V		15	25	ns
			Full	2.7 V to 3.6 V			30	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1 \text{ nF}$ , See Figure 20	25°C	3 V		1	4	pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = 0$ , $f = 1 \text{ MHz}$ , Switch OFF, See Figure 16	25°C	3 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = 0$ , $f = 1 \text{ MHz}$ , Switch OFF, See Figure 16	25°C	3 V		6.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = 0$ , $f = 1 \text{ MHz}$ , Switch ON, See Figure 16	25°C	3 V		13		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = 0$ , $f = 1 \text{ MHz}$ , Switch ON, See Figure 16	25°C	3 V		13		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	3 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Signal = 0 dBm, Switch ON, See Figure 18	25°C	3 V		450		MHz
OFF isolation	$O_{ISO}$	$V_{NO} = 1 \text{ V}_{RMS}$ , $f = 1 \text{ MHz}$ , $C_L = 5 \text{ pF}$ , Switch OFF, See Figure 19	25°C	3 V		-85		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $V_{SOURCE} = 3 \text{ V}_{p-p}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See Figure 21	25°C	3 V		0.09		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V		0.01	0.25	$\mu\text{A}$
			Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## TYPICAL PERFORMANCE

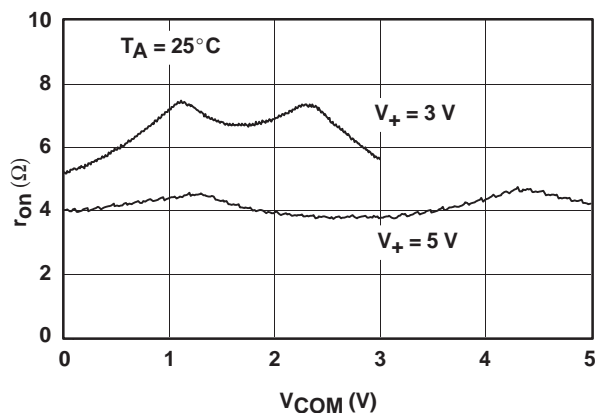


Figure 1.  $r_{on}$  vs  $V_{COM}$

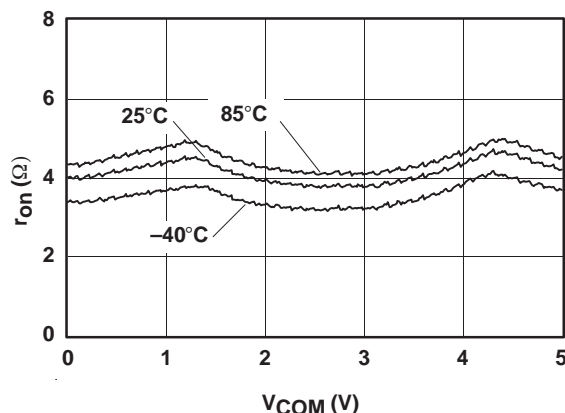


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5\text{ V}$ )

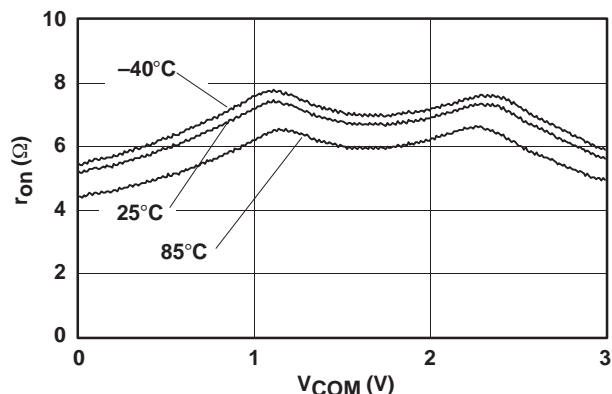


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3\text{ V}$ )

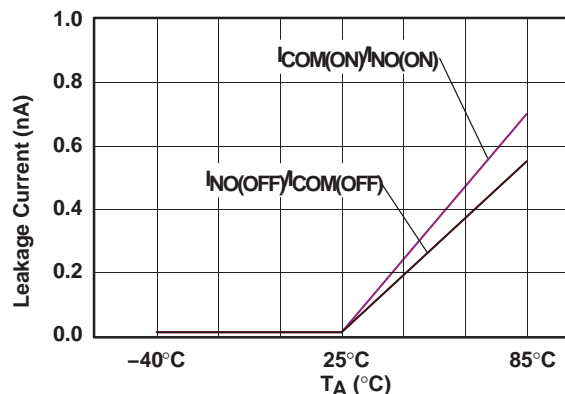


Figure 4. Leakage Current vs Temperature ( $V_+ = 5\text{ V}$ )

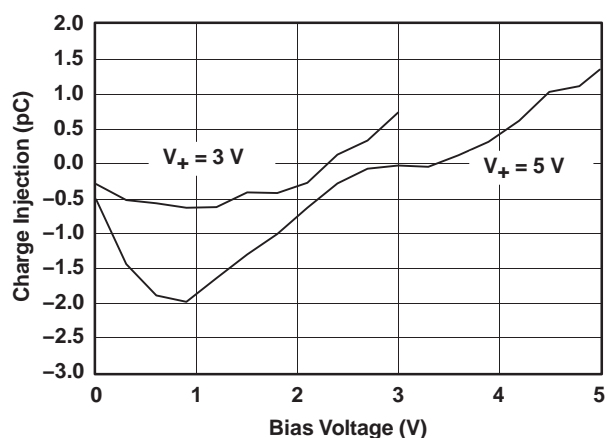


Figure 5. Charge-Injection ( $Q_C$ ) vs  $V_{COM}$

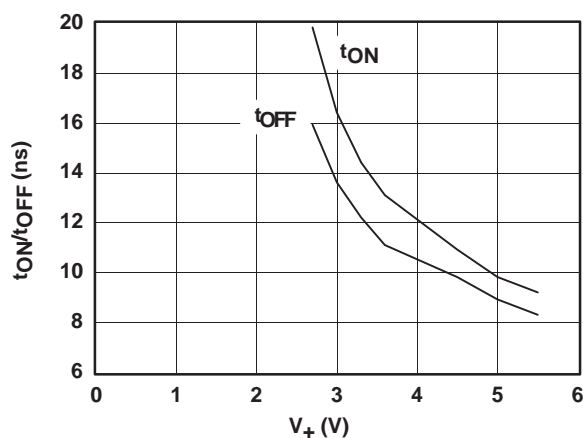
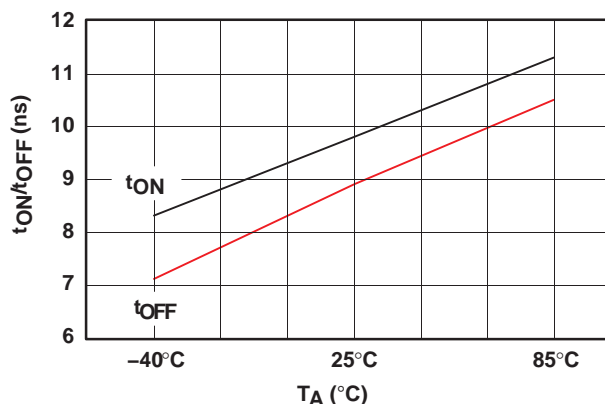
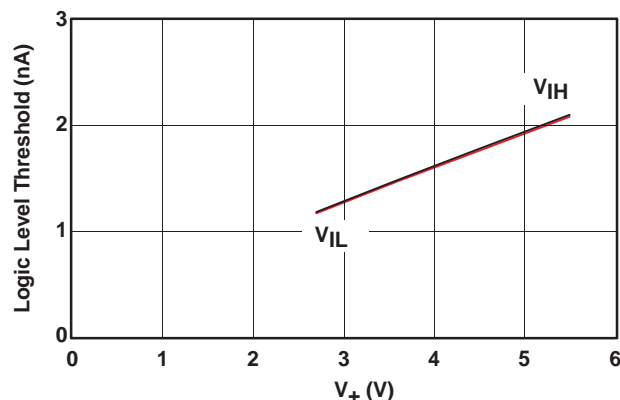


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

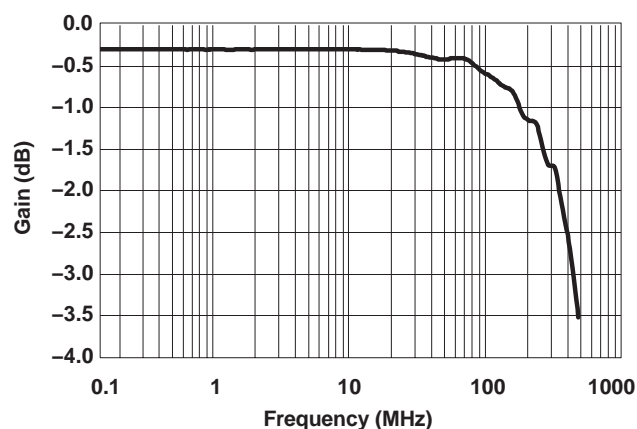
**TYPICAL PERFORMANCE (continued)**



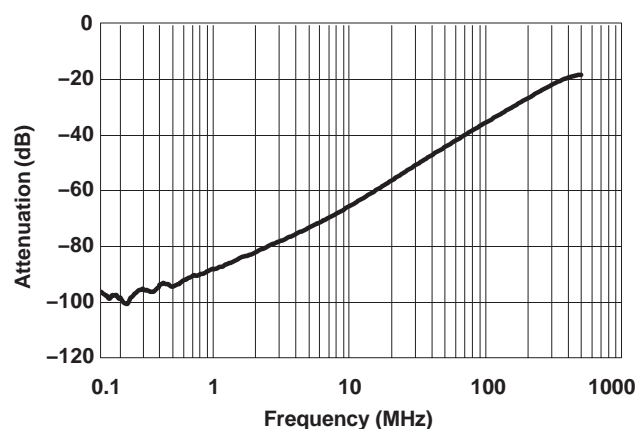
**Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5$  V)**



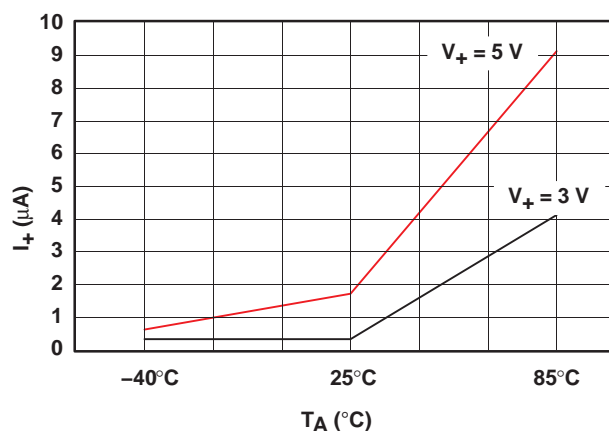
**Figure 8. Logic-Level Threshold vs  $V_+$**



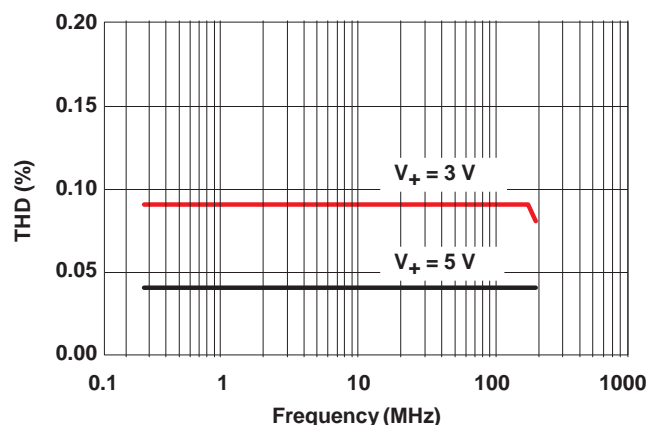
**Figure 9. Bandwidth (Gain vs Frequency) ( $V_+ = 5$  V)**



**Figure 10. OFF Isolation vs Frequency**



**Figure 11. Power-Supply Current vs Temperature**



**Figure 12. Total Harmonic Distortion vs Frequency**

**PIN DESCRIPTION**

PIN NUMBER	NAME	DESCRIPTION
1	IN	Digital control pin to connect COM to NO
2	COM	Common
3	GND	Digital ground
4	NO	Normally open
5	V <sub>+</sub>	Power supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NO ports when the channel is ON
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of r <sub>on</sub> in a channel over the specified range of conditions
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN)
V <sub>I</sub>	Voltage at the control input (IN)
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN)
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q <sub>C</sub> = C <sub>L</sub> × ΔV <sub>COM</sub> , C <sub>L</sub> is the load capacitance, and ΔV <sub>COM</sub> is the change in analog output voltage.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C <sub>I</sub>	Capacitance of control input (IN)
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I <sub>+</sub>	Static power-supply current with the control (IN) pin at V <sub>+</sub> or GND

## PARAMETER MEASUREMENT INFORMATION

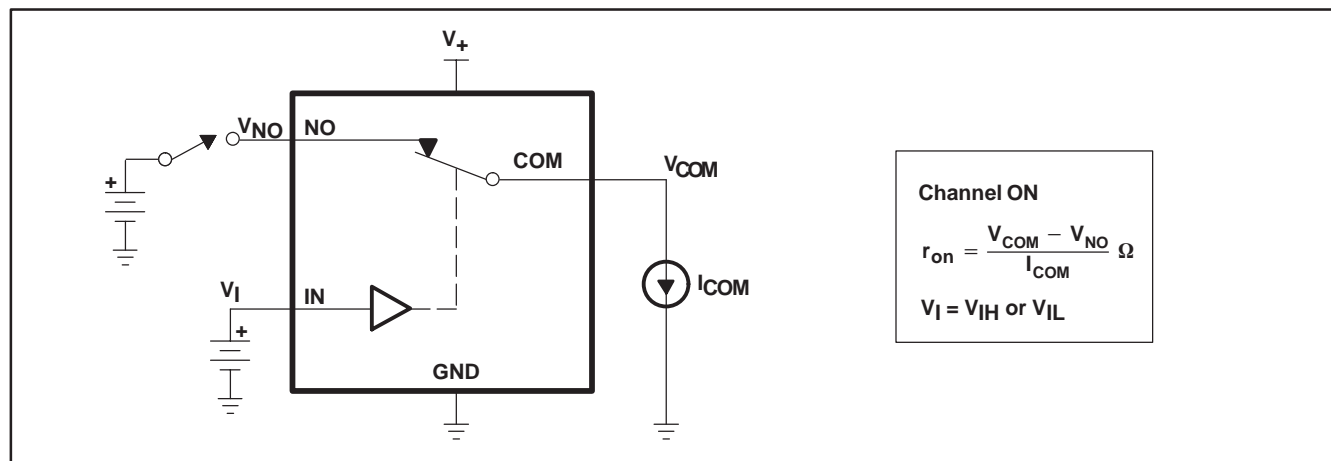


Figure 13. ON-State Resistance ( $r_{on}$ )

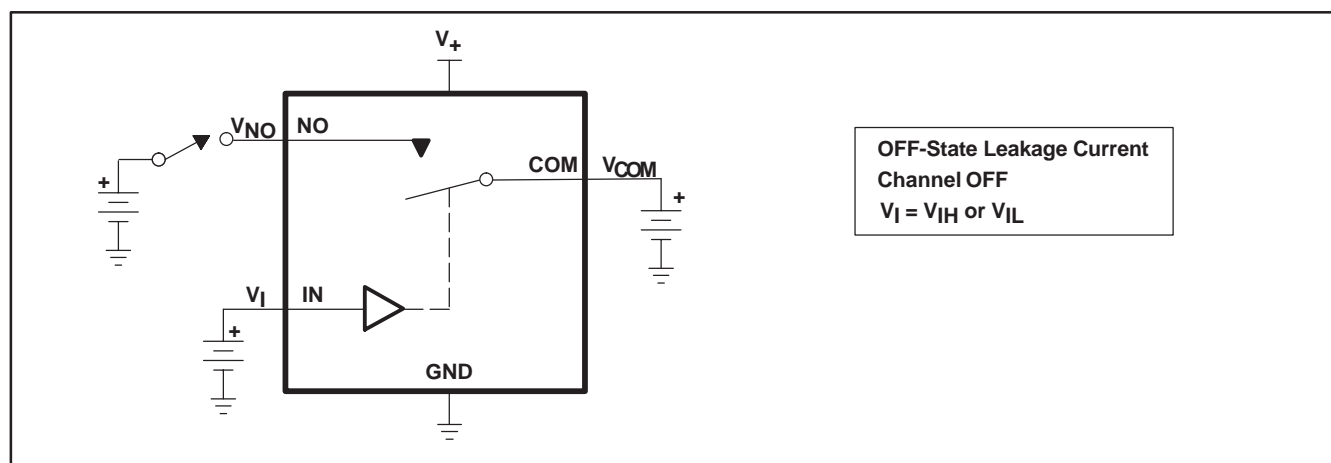


Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ )

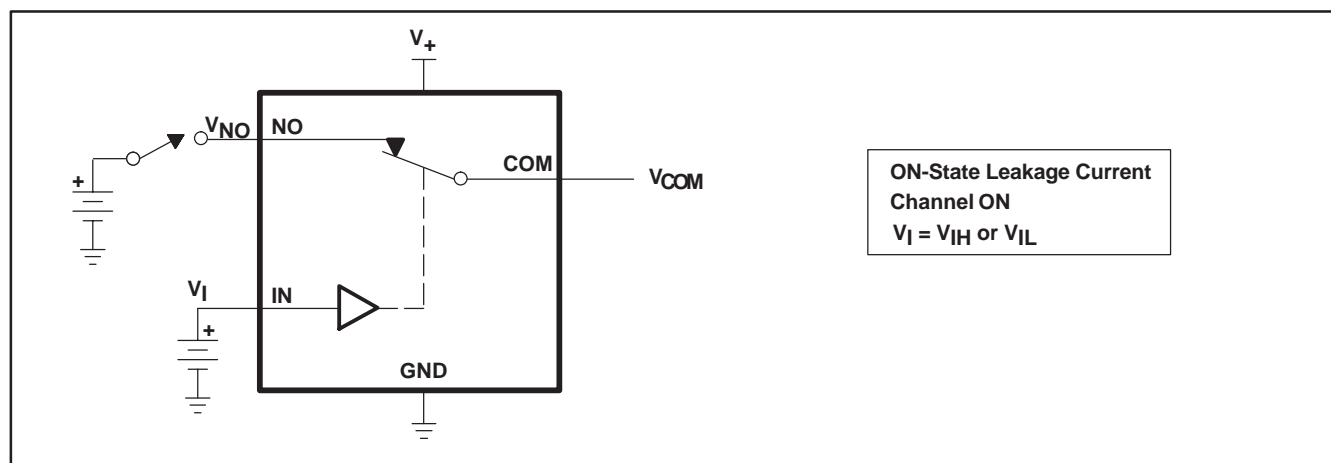


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )

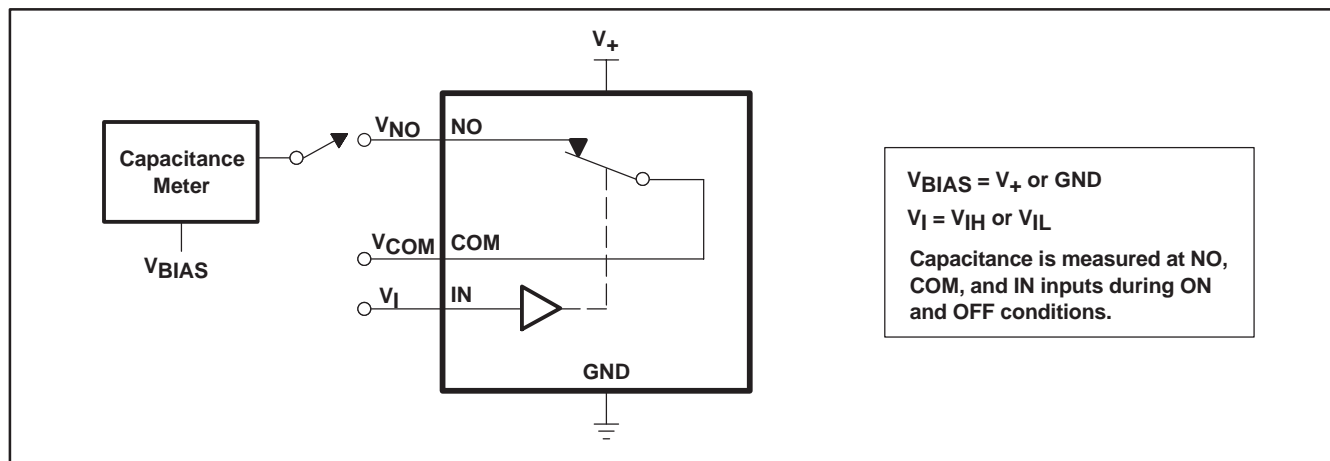
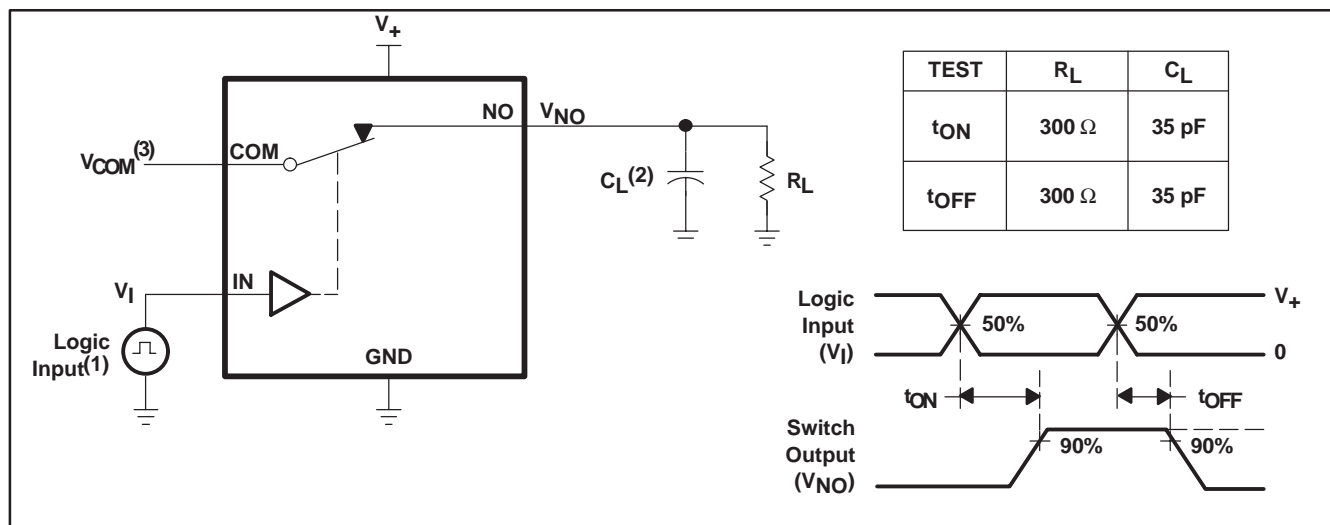


Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
 (2)  $C_L$  includes probe and jig capacitance.  
 (3) See Electrical Characteristics for  $V_{COM}$ .

Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

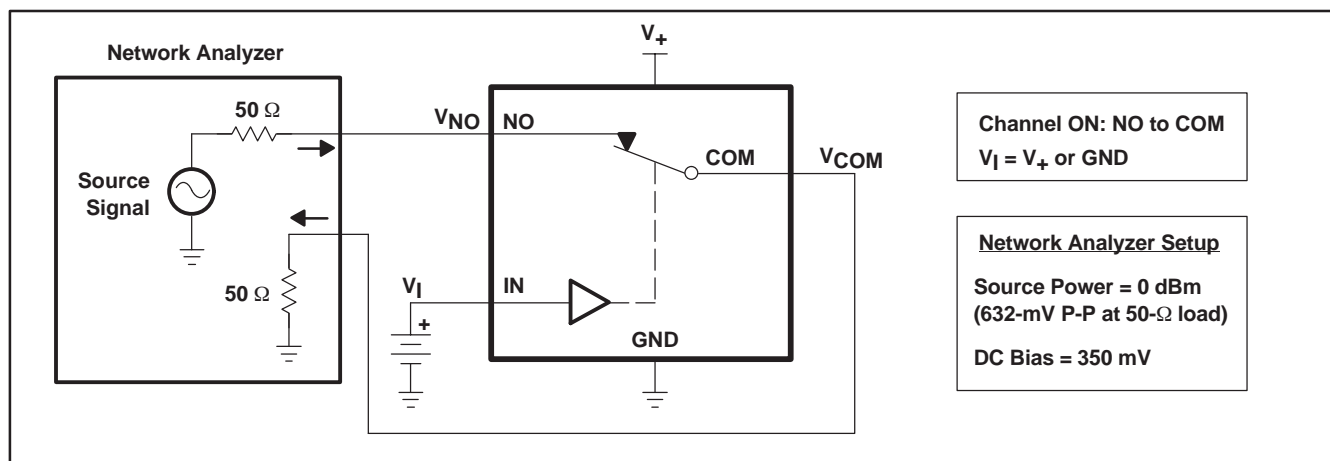
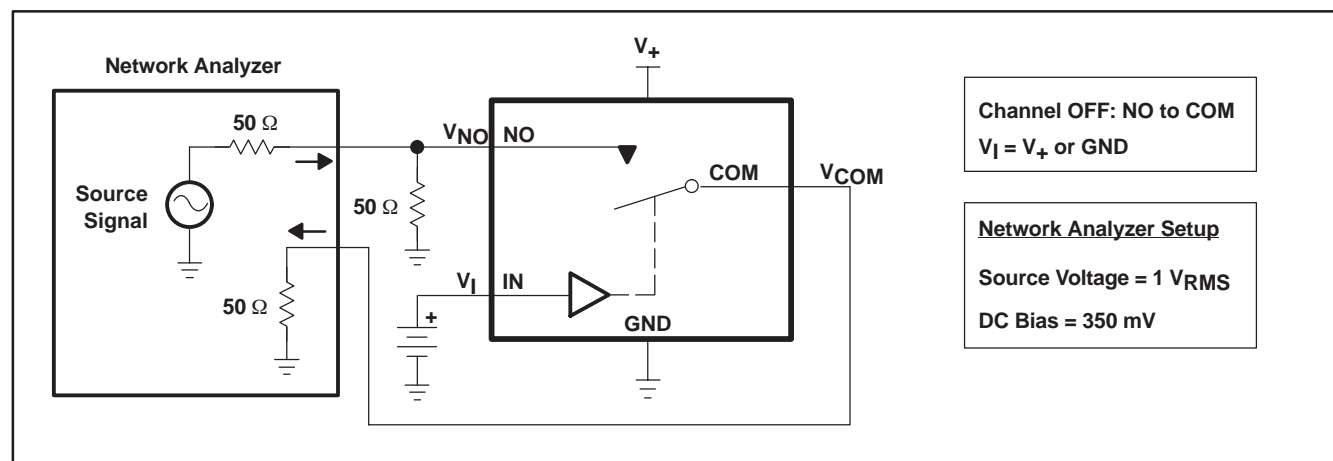


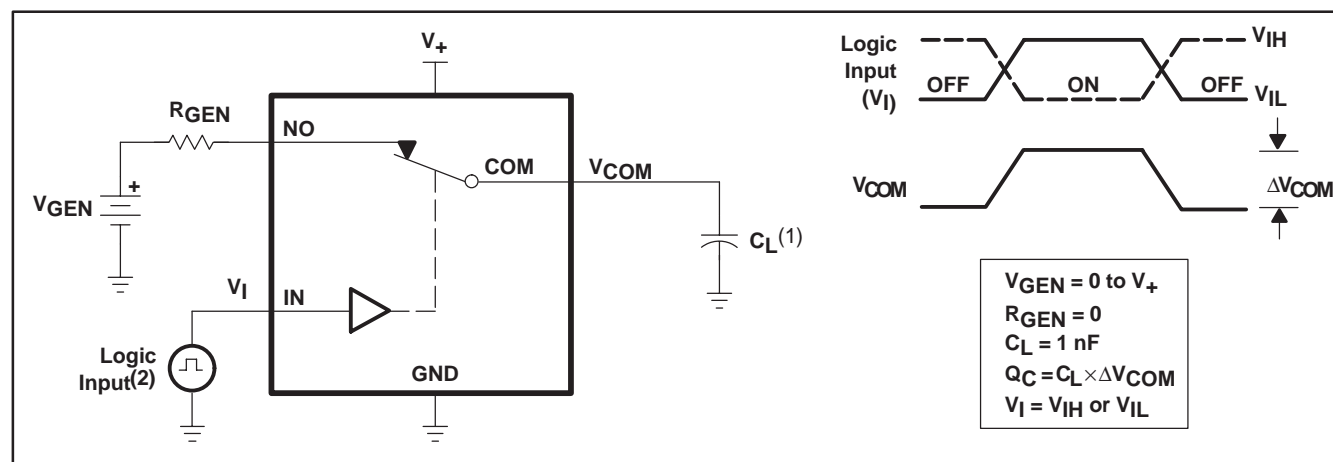
Figure 18. Bandwidth (BW)

**TS5A4596**  
**8-Ω SPST ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL ANALOG SWITCH**

SCDS181 – FEBRUARY 2005



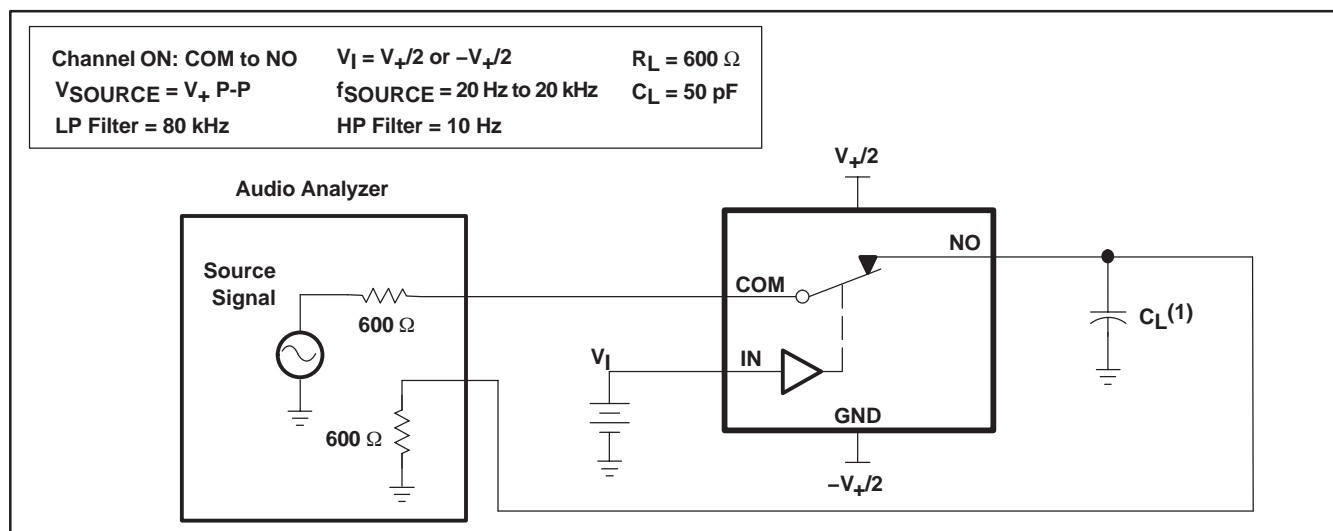
**Figure 19. OFF Isolation ( $O_{ISO}$ )**



(1) C<sub>L</sub> includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.

**Figure 20. Charge Injection (Q<sub>C</sub>)**



(2) C<sub>L</sub> includes probe and jig capacitance.

**Figure 21. Total Harmonic Distortion (THD)**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A4596DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSCR
TS5A4596DBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSCR
<a href="#">TS5A4596DCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JUR
TS5A4596DCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JUR
TS5A4596DCKRG4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JUR
TS5A4596DCKRG4.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JUR

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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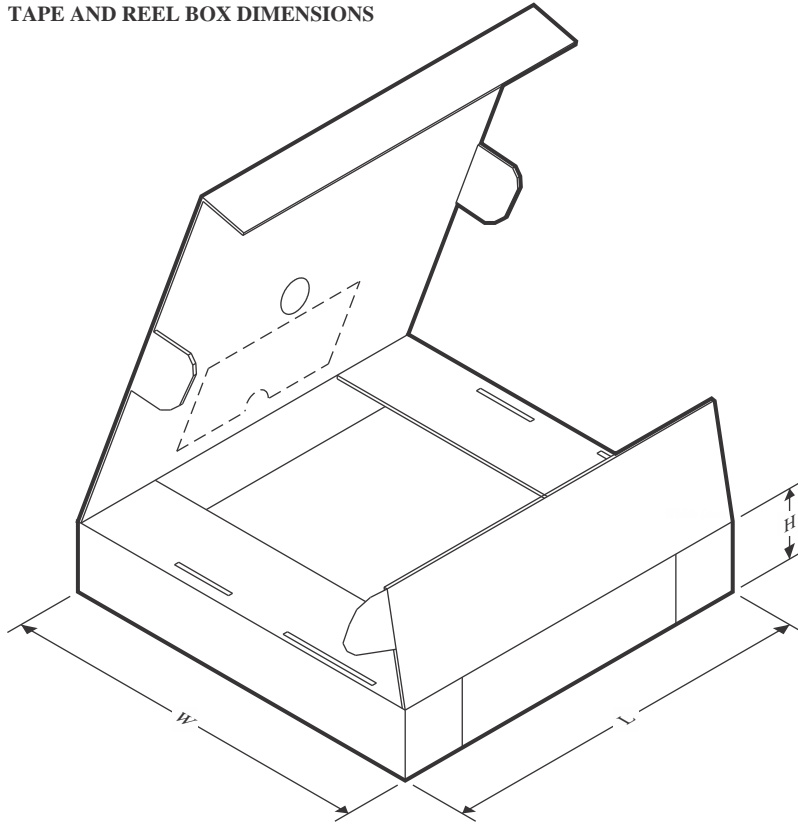
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A4596DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A4596DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A4596DCKRG4	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A4596DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A4596DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A4596DCKRG4	SC70	DCK	5	3000	202.0	201.0	28.0



### SOT - 1.1 max height

Technical drawing of a mechanical part showing three views: front, side, and top.

**Front View Dimensions:**

- Overall width: 2.4 (1.8)
- Overall height: 2.15 (1.85)
- Pin 1 Index Area (hatched)
- Feature 1: 1.3 (0.65)
- Feature 2: 1.3 (0.65)
- Feature 3: 1.3 (0.65)
- Feature 4: 1.3 (0.65)
- Feature 5: 1.3 (0.65)
- Feature 6: 1.3 (0.65)
- Feature 7: 1.3 (0.65)
- Feature 8: 1.3 (0.65)
- Feature 9: 1.3 (0.65)
- Feature 10: 1.3 (0.65)
- Feature 11: 1.3 (0.65)
- Feature 12: 1.3 (0.65)
- Feature 13: 1.3 (0.65)
- Feature 14: 1.3 (0.65)
- Feature 15: 1.3 (0.65)
- Feature 16: 1.3 (0.65)
- Feature 17: 1.3 (0.65)
- Feature 18: 1.3 (0.65)
- Feature 19: 1.3 (0.65)
- Feature 20: 1.3 (0.65)
- Feature 21: 1.3 (0.65)
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- Feature 69: 1.3 (0.65)
- Feature 70: 1.3 (0.65)
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- Feature 94: 1.3 (0.65)
- Feature 95: 1.3 (0.65)
- Feature 96: 1.3 (0.65)
- Feature 97: 1.3 (0.65)
- Feature 98: 1.3 (0.65)
- Feature 99: 1.3 (0.65)
- Feature 100: 1.3 (0.65)

**Side View Dimensions:**

- Overall width: 1.1 MAX
- Overall height: 0.1 C

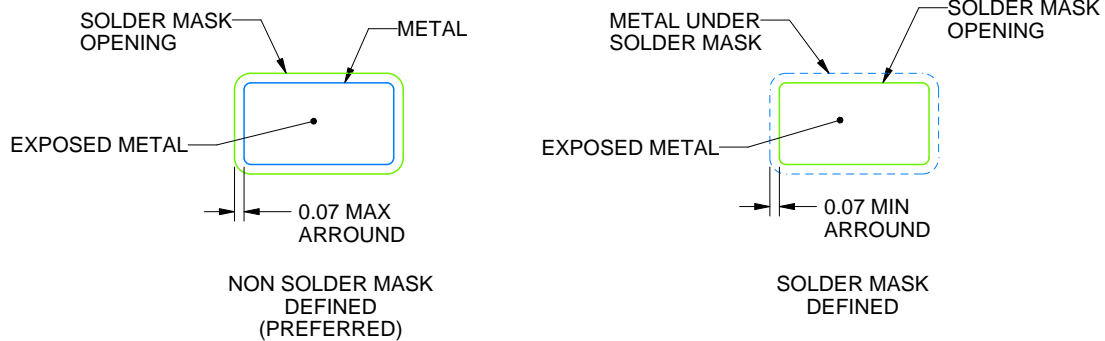
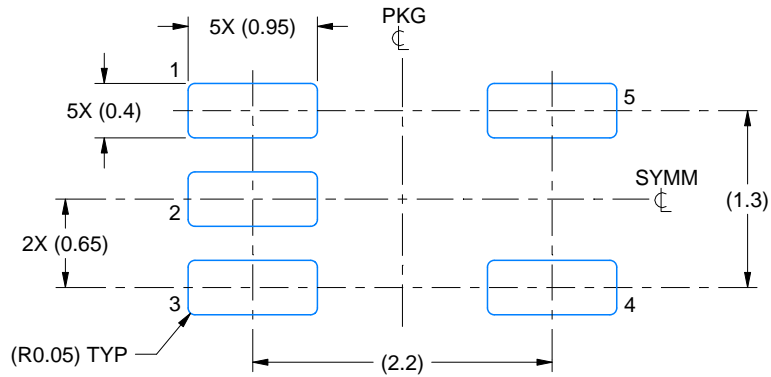
**Top View Dimensions:**

- Overall width: 0.46 TYP
- Overall height: 0.22 TYP
- Feature 1: 0.15
- Feature 2: 0.15
- Feature 3: 0.15
- Feature 4: 0.15
- Feature 5: 0.15
- Feature 6: 0.15
- Feature 7: 0.15
- Feature 8: 0.15
- Feature 9: 0.15
- Feature 10: 0.15
- Feature 11: 0.15
- Feature 12: 0.15
- Feature 13: 0.15
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- Feature 16: 0.15
- Feature 17: 0.15
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- Feature 19: 0.15
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- Feature 38: 0.15
- Feature 39: 0.15
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- Feature 43: 0.15
- Feature 44: 0.15
- Feature 45: 0.15
- Feature 46: 0.15
- Feature 47: 0.15
- Feature 48: 0.15
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- Feature 64: 0.15
- Feature 65: 0.15
- Feature 66: 0.15
- Feature 67: 0.15
- Feature 68: 0.15
- Feature 69: 0.15
- Feature 70: 0.15
- Feature 71: 0.15
- Feature 72: 0.15
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- Feature 88: 0.15
- Feature 89: 0.15
- Feature 90: 0.15
- Feature 91: 0.15
- Feature 92: 0.15
- Feature 93: 0.15
- Feature 94: 0.15
- Feature 95: 0.15
- Feature 96: 0.15
- Feature 97: 0.15
- Feature 98: 0.15
- Feature 99: 0.15
- Feature 100: 0.15

**Notes:**

- NOTE 1: PIN 1 INDEX AREA
- NOTE 2: 5X 0.33 0.15
- NOTE 3: 4X 4° -15°
- NOTE 4: (0.15) (0.1)
- NOTE 5: 0.15 0.08 TYP

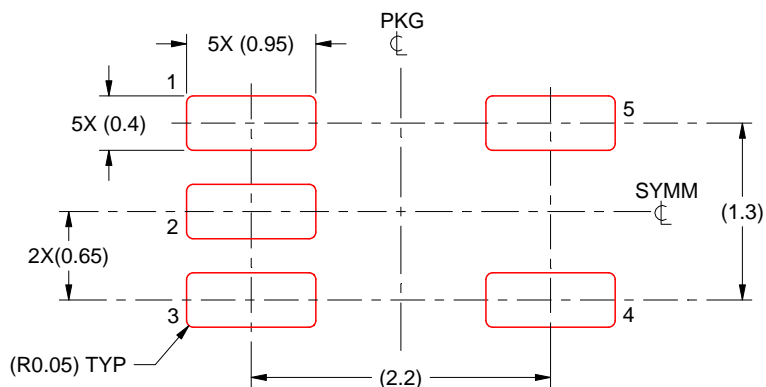
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

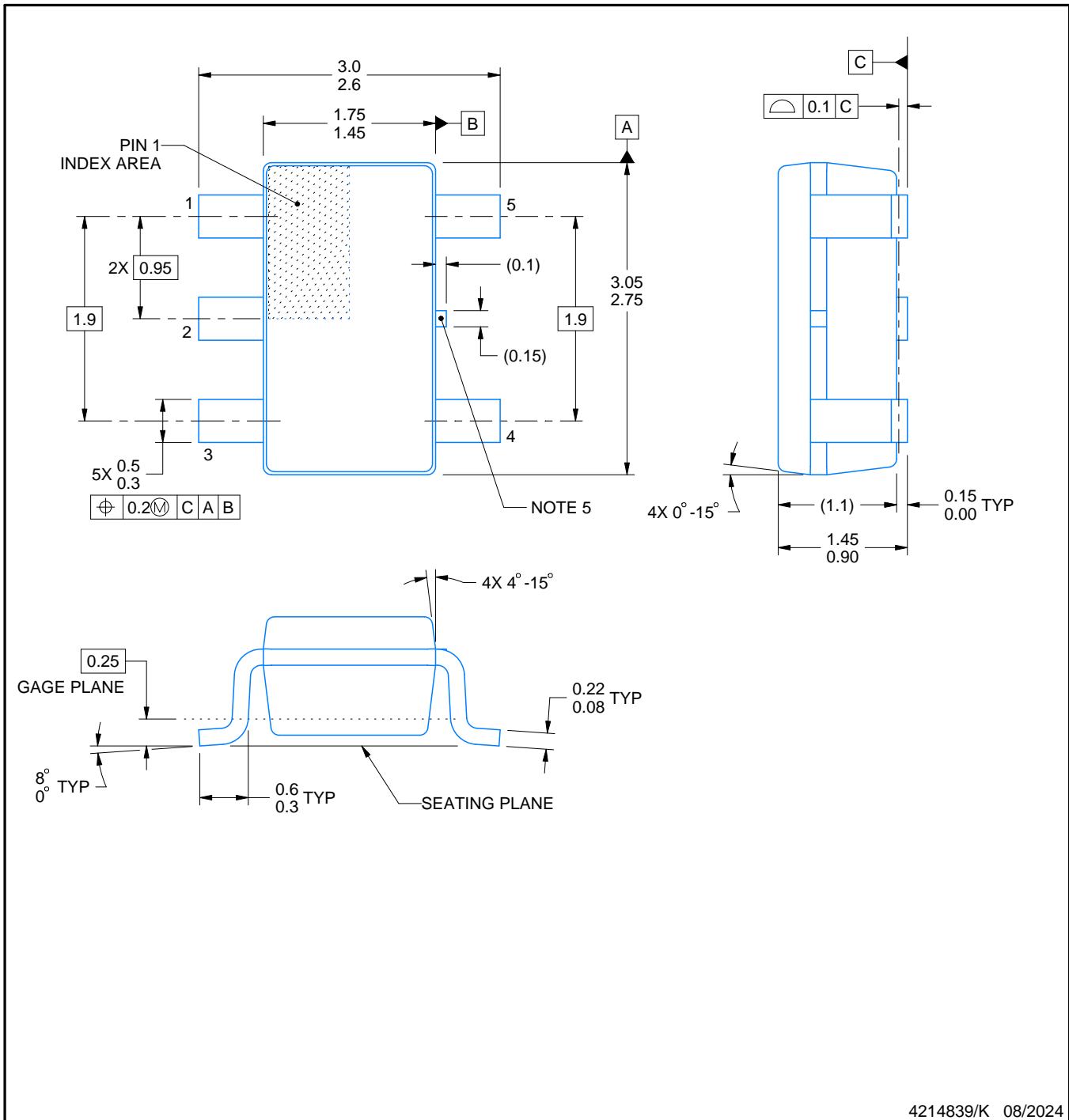
4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

**DBV0005A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

**NOTES:**

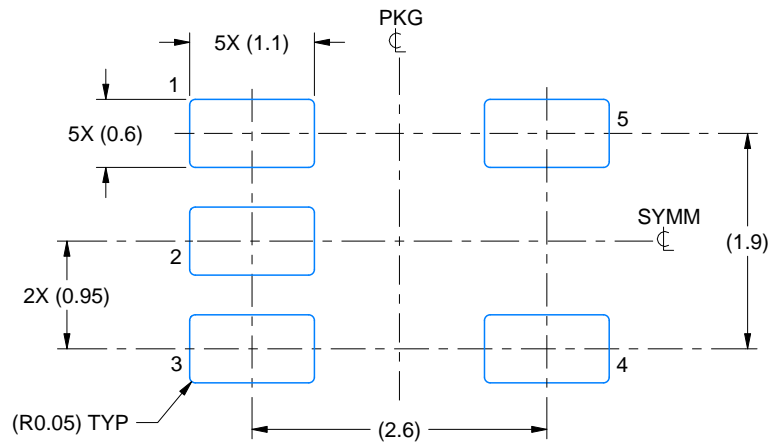
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

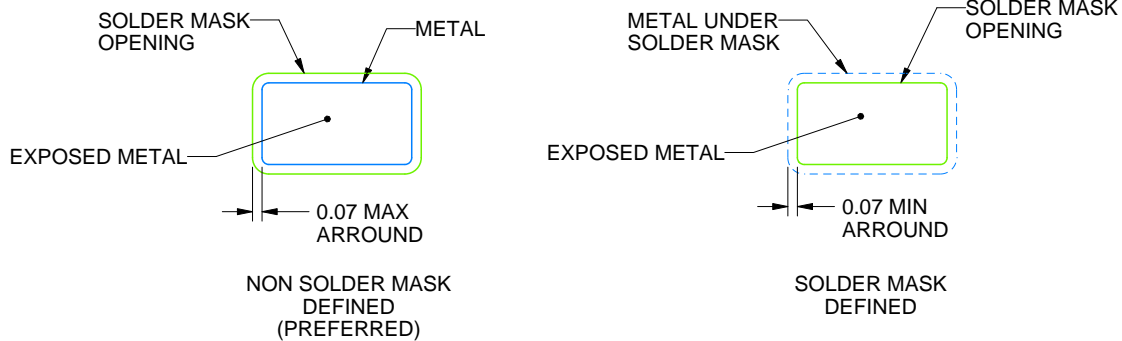
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

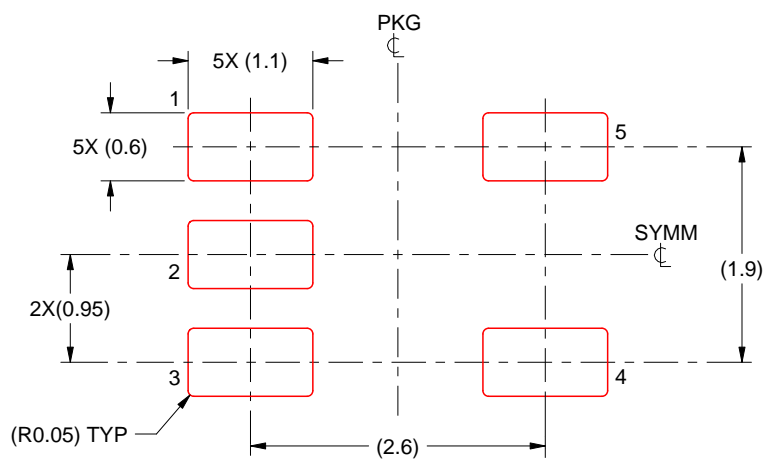
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DBV0005A**

## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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