TS5A3166 0.9Ω SPSTアナログ・スイッチ

1 特長

- オン状態での低い抵抗(0.9Ω)
- 制御入力は5.5V許容
- 低電荷注入
- 低い全高調波歪(THD)
- 1.65V～5.5Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
  - 人体モデルで2000V (A114-B、クラスII)
  - 1000V、荷電デバイス・モデル(C101)

2 アプリケーション

- 携帯電話
- 携帯情報端末
- ポータブル機器
- オーディオおよびビデオ信号のルーティング
- 低電圧のデータ収集システム
- 通信用回路
- モデム
- ハードディスク
- コンピュータ・ペリフェラル
- ワイヤレス端末およびペリフェラル
- マイクロフォンのスイッチ - ノートブック・ドッキング

3 概要

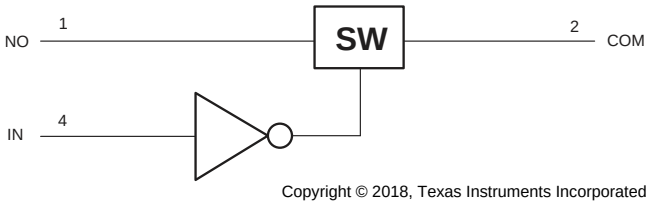
TS5A3166デバイスは単極単投(SPST)のアナログ・スイッチであり、1.65V～5.5Vで動作するよう設計され、オン抵抗が低い特徴があります。このデバイスは全高調波歪み(THD)特性が非常に優れており、極めて低消費電力です。これらの特長から、このデバイスは携帯用オーディオ・アプリケーションに適しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5A3166	SOT-23 (5)	2.90mm×1.60mm
	SC70 (5)	2.00mm×1.25mm
	DSBGA (5)	1.388mm×0.888mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (February 2016) から Revision E に変更 **Page**

- Changed the YZP package pin numbers ... 3

Revision C (May 2015) から Revision D に変更 **Page**

- Added "port" to COM description in *Pin Functions* table ... 3
- Deleted "digitial" from GND description in *Pin Functions* table ... 3

Revision B (September 2013) から Revision C に変更 **Page**

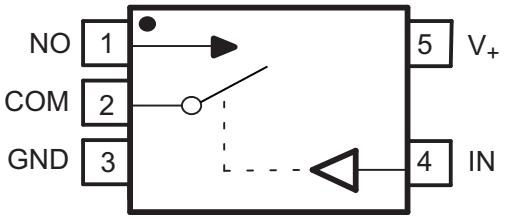
- 「*アプリケーション*」セクション、「*製品情報*」表、「*ピン機能*」表、「*ESD定格*」表、「*熱に関する情報*」表、「*代表的特性*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「*注文情報*」表 削除 ... 1

Revision A (October 2012) から Revision B に変更 **Page**

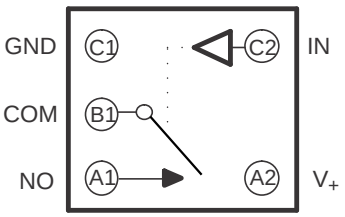
- 「電源オフ・モード、V_+ = 0での絶縁」箇条書き項目を「*特長*」から削除 ... 1
- データシート全体を通して、ピン名をNCからNOに変更 ... 1

5 Pin Configuration and Functions

DBV and DCK Packages
5-Pin SOT-23 and SC-70
Top View



YZP Package
5-Pin DSBGA
Bottom View



Pin Functions

PIN			TYPE	DESCRIPTION
DBC, DCK NO.	YZP NO.	NAME		
1	A1	NO	I/O	Normally opened port
2	B1	COM	I/O	Common port
3	C1	GND	GND	Ground
4	C2	IN	I	Digital control pin to connect COM to NO
5	A2	V_+	Power	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	ON-state switch current	V_{NO}, V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)		–400	400	
V_I	Digital input voltage(3)(4)		–0.5	6.5	V
I_{IK}	Digital clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C
T_j	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	V_+	V
V_+	Supply voltage	1.65	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TS5A3166			UNIT
		DBV (SOT)	DCK (SC-70)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	4.5 V		0.8	1.1	Ω
				Full				1.2	
r_{on}	ON-state resistance	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	4.5 V		0.7	0.9	Ω
				Full				1	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	4.5 V		0.15		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,		25°C			0.09	0.15	
				Full				0.15	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see 図 14	25°C	5.5 V	–20	4	20	nA
				Full		–100		100	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–5	0.4	5	µA
				Full		–15		15	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, see 図 14	25°C	5.5 V	–20	4	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$		V_{COM} = 5.5 V to 0, V_{NO} = 0 to 5.5 V,		25°C	0 V	–5	0.4	5	µA
				Full		–15		15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see 図 15	25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, see 図 15	25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	5 V	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	5 V	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, see 図 20	25°C	5 V		1		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 図 16	25°C	5 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 図 16	25°C	5 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 図 16	25°C	5 V		35.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 図 16	25°C	5 V		35.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 16	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 18	25°C	5 V		200		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 図 19	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 図 21	25°C	5 V		0.005%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full				0.5	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	3 V		1	1.4	Ω
				Full				1.5	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	3 V		0.3		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.09	0.15	
				Full				0.15	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 図 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20		20	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 図 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20		20	
$I_{COM(PWROFF)}$		V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 図 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 図 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	3.3 V	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	
t_{OFF}	Turnoff time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	3.3 V	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 図 21	25°C	3.3 V		1		pC
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+$ or GND, Switch OFF,	See 図 16	25°C	3.3 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF,	See 図 16	25°C	3.3 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See 図 16	25°C	3.3 V		36		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See 図 16	25°C	3.3 V		36		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 16	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 18	25°C	3.3 V		200		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 図 19	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 図 21	25°C	3.3 V		0.01%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.1	μA
				Full				0.25	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range				2.3 V	0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	2.3 V		0.7		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.4	0.6	
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 図 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 図 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 図 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 図 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 図 21	25°C	2.5 V		4		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 図 16	25°C	2.5 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 図 16	25°C	2.5 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 図 16	25°C	2.5 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 図 16	25°C	2.5 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 16	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 18	25°C	2.5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 図 19	25°C	2.5 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 図 21	25°C	2.5 V		0.02%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	μA
				Full				0.25	

6.8 Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 図 13	25°C	1.65 V		2.8		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			4.1	22	
				Full				27	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 図 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2		2	μA
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 図 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,		25°C	0 V	–2		2	μA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 図 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 図 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 図 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 図 21	25°C	1.8 V		2		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 図 16	25°C	1.8 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 図 16	25°C	1.8 V		18.5		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 図 16	25°C	1.8 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 図 16	25°C	1.8 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 16	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 18	25°C	1.8 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 図 19	25°C	1.8 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz see 図 21	25°C	1.8 V		0.055 %		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	μA
				Full				0.15	

6.9 Typical Characteristics

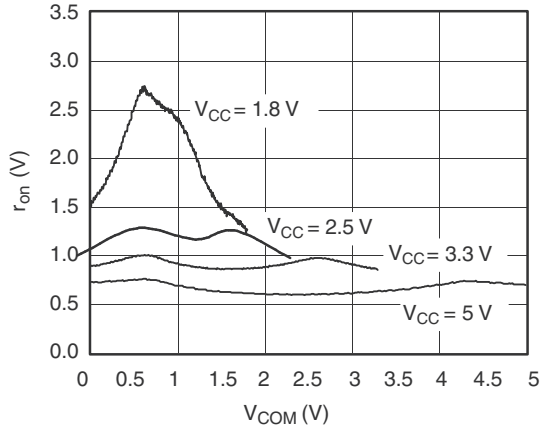


図 1. r_{on} vs V_{COM}

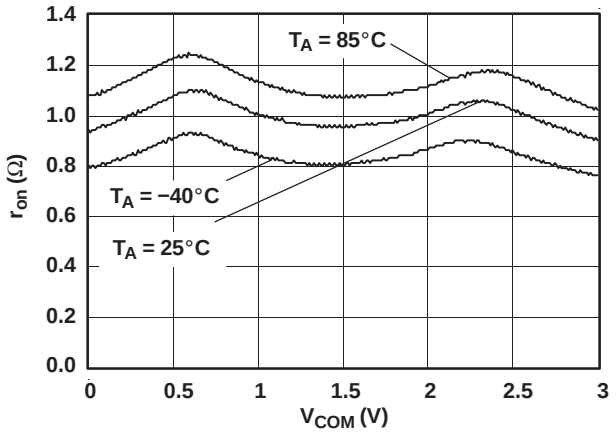


図 2. r_{on} vs V_{COM} (V_+ = 3 V)

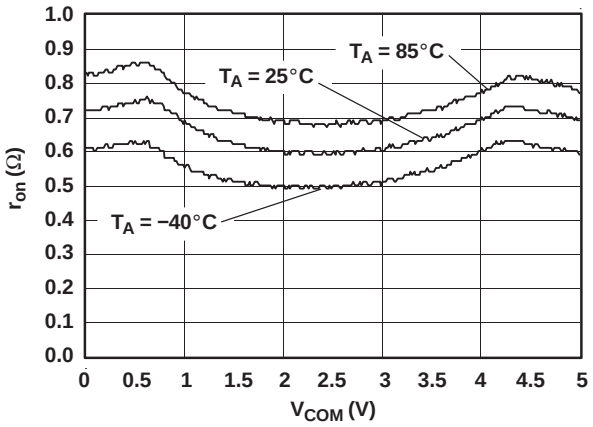


図 3. r_{on} vs V_{COM} (V_+ = 5 V)

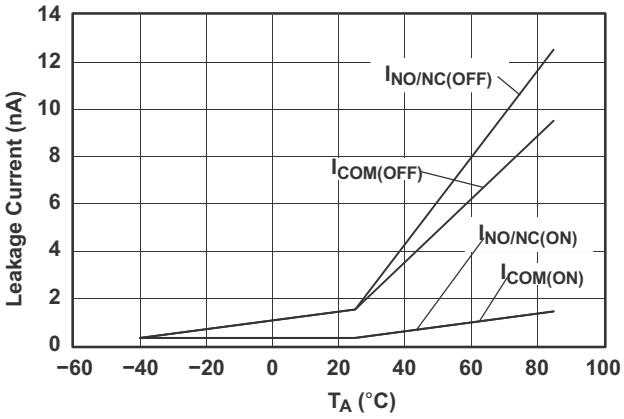


図 4. Leakage Current vs Temperature (V_+ = 5.5 V)

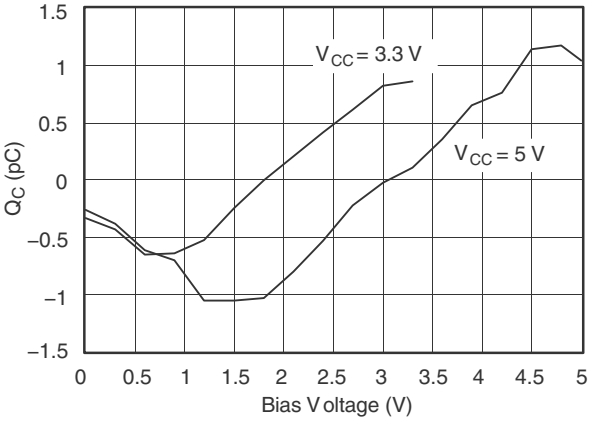


図 5. Charge Injection (Q_C) vs V_{COM}

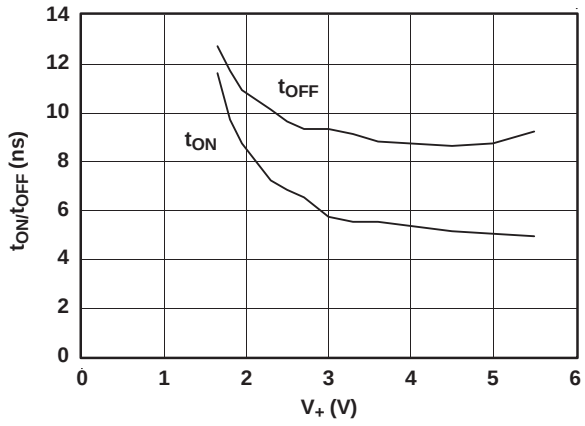


図 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

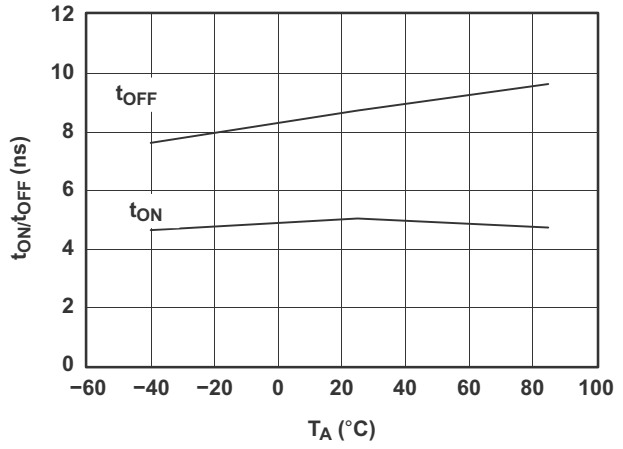


図 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

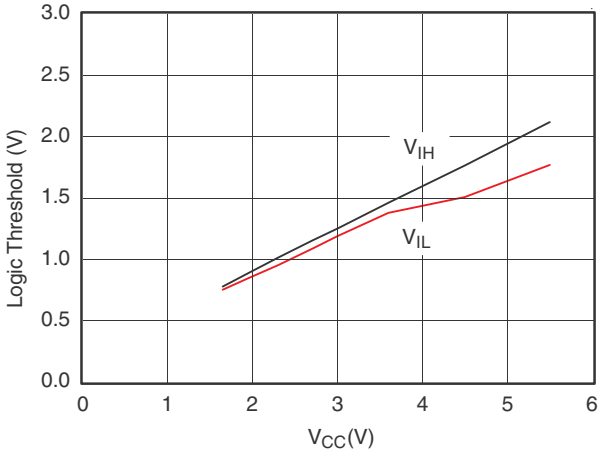


図 8. Logic Threshold vs V_+

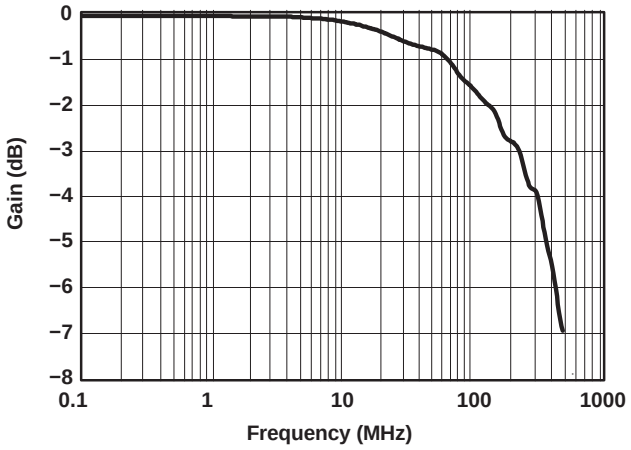


図 9. Gain vs Frequency (V_+ = 5 V)

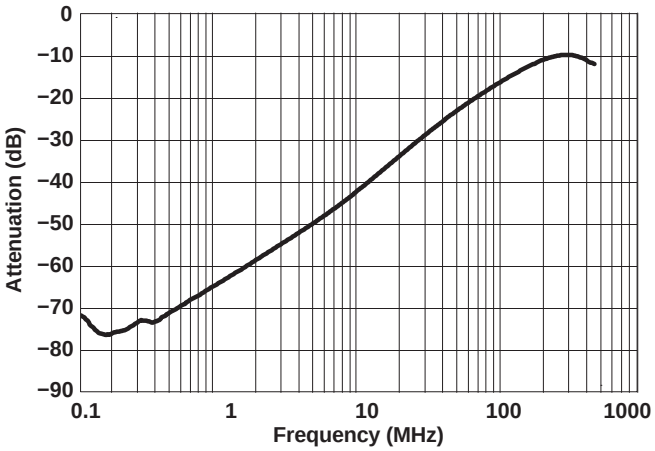


図 10. OFF Isolation vs Frequency (V_+ = 5 V)

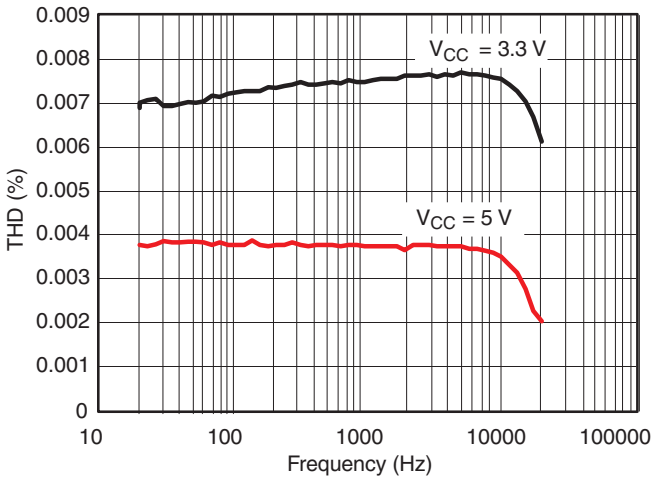


図 11. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

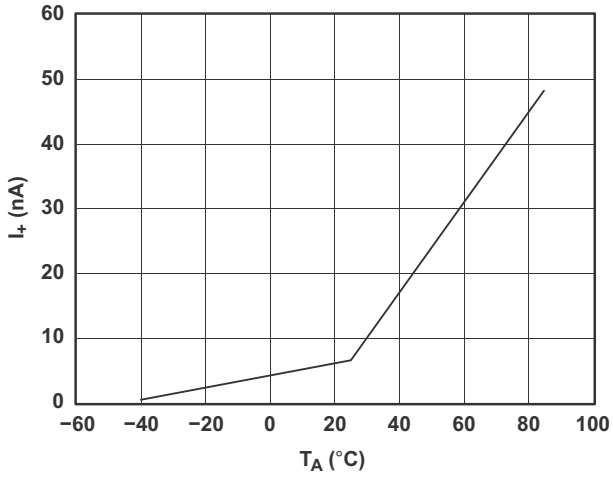
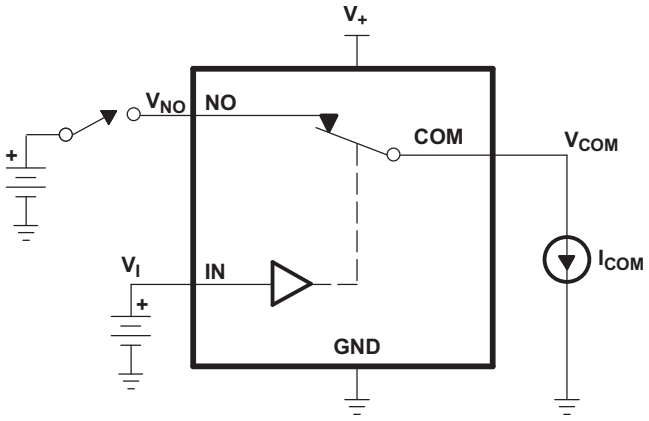


図 12. Power-Supply Current vs Temperature (V_+ = 5 V)

7 Parameter Measurement Information

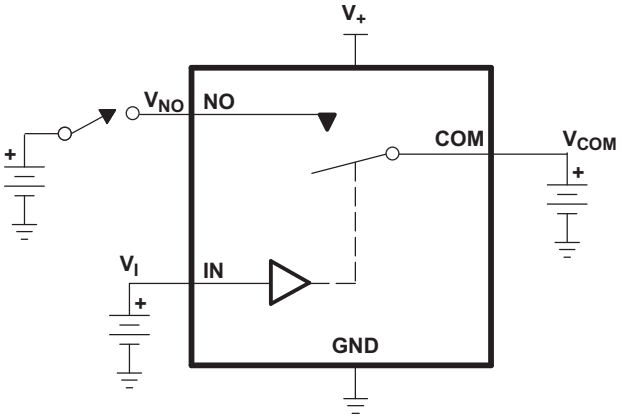


Channel ON

$$r_{on} = \frac{V_{COM} - V_{NC}}{I_{COM}} \ \Omega$$

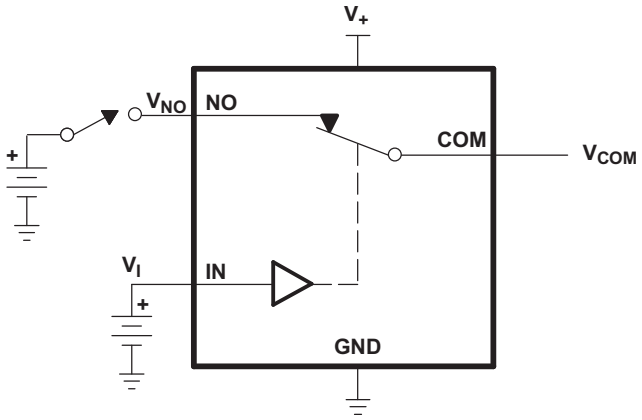
$V_I = V_{IH}$ or V_{IL}

図 13. ON-State Resistance (r_{on})



OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}

図 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NO(PWR(FF)}$)



ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

図 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

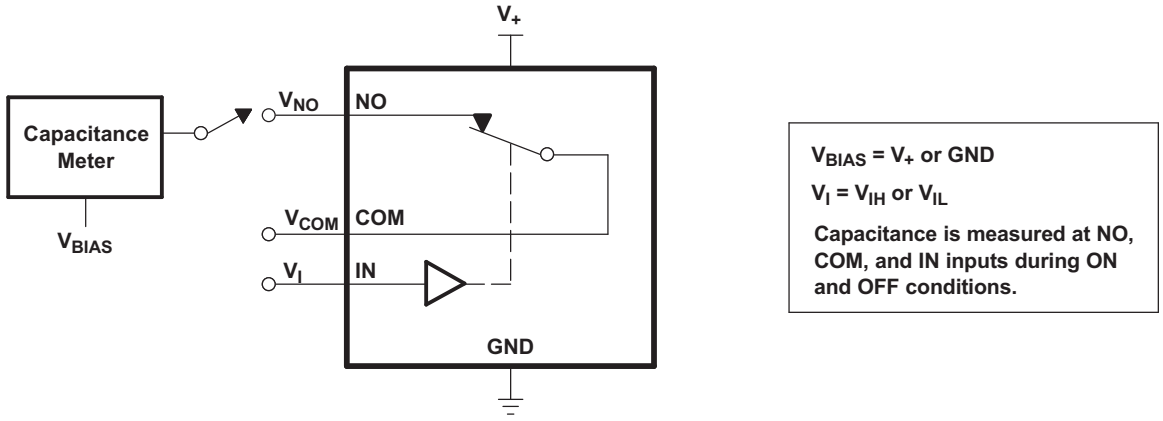
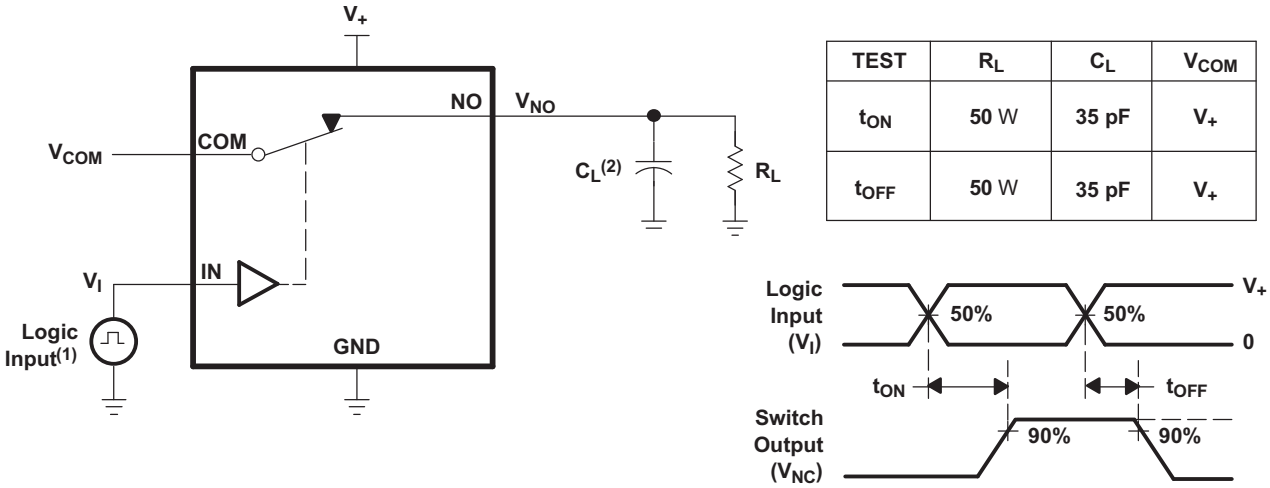


図 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

図 17. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

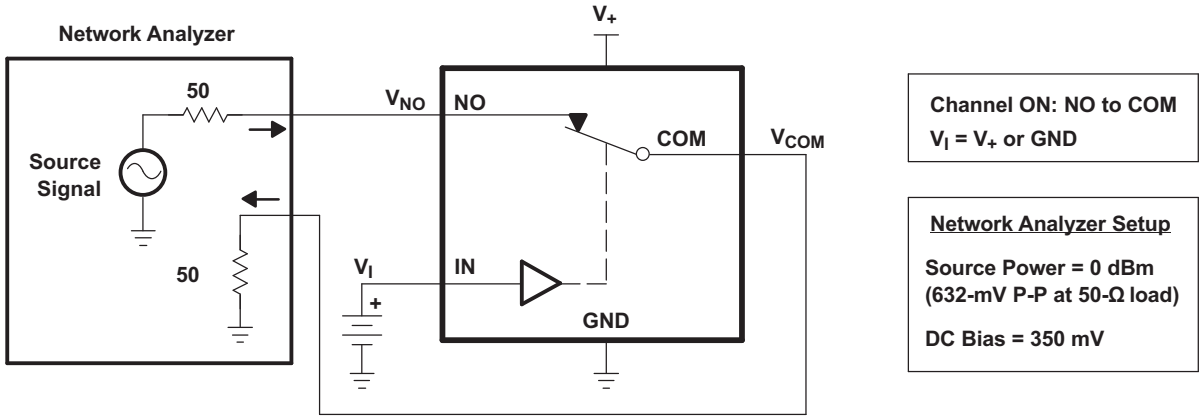


図 18. Bandwidth (BW)

Parameter Measurement Information (continued)

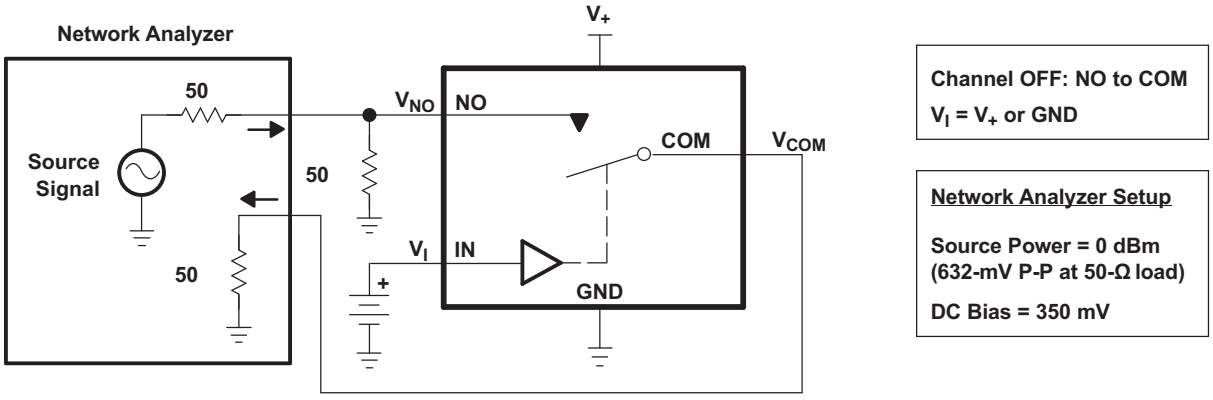
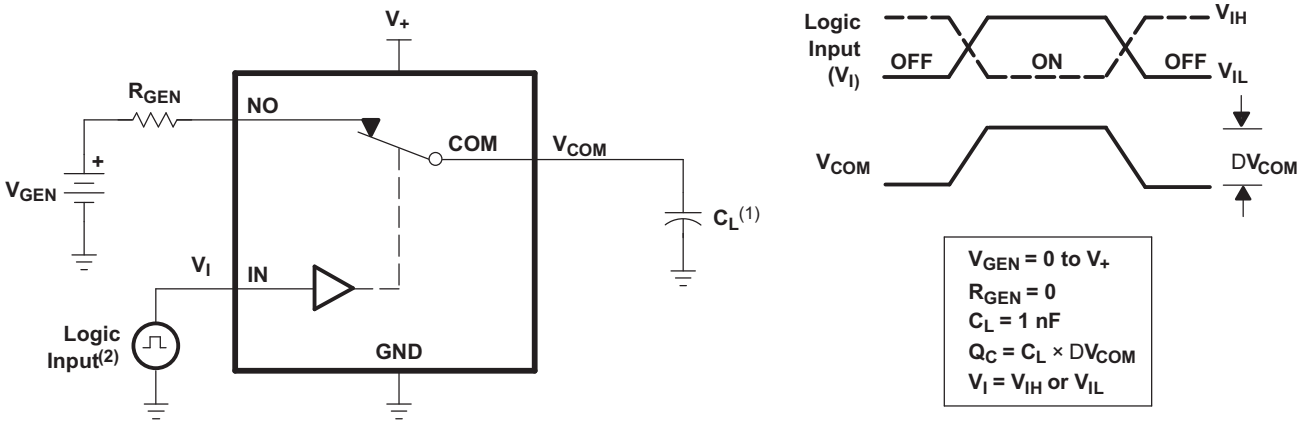


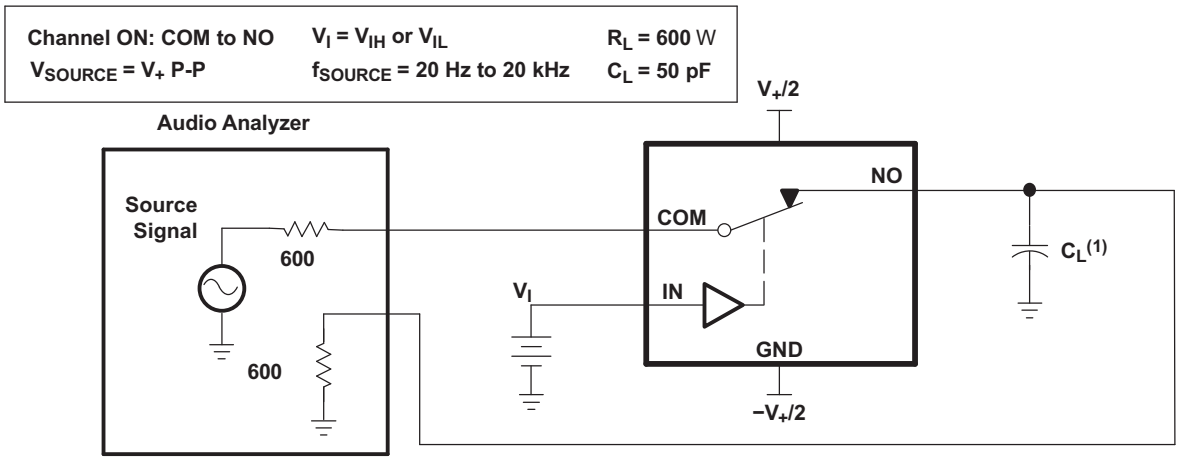
図 19. OFF Isolation (O_{ISO})



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

図 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

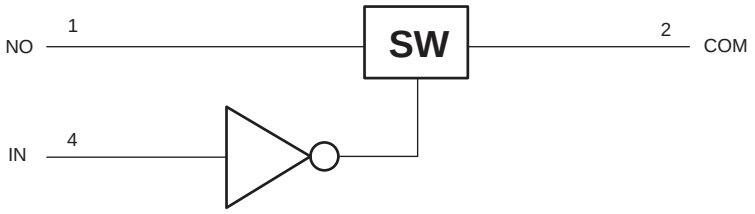
図 21. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A3166 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3166 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

表 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. 図 22 and 図 23 are some basic applications that utilize the TS5A3166.

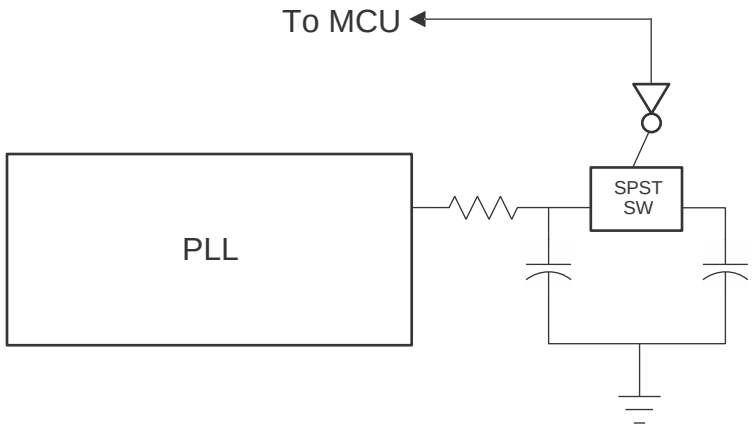


図 22. Improved Lock Time Circuit Simplified Block Diagram

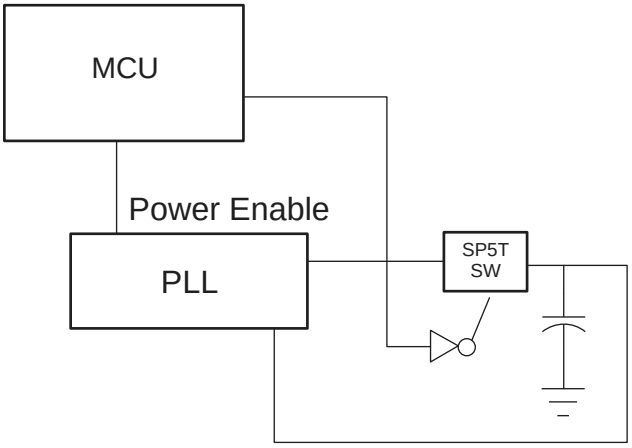


図 23. PLL Improved Power Consumption Simplified Block Diagram

9.2 Typical Application

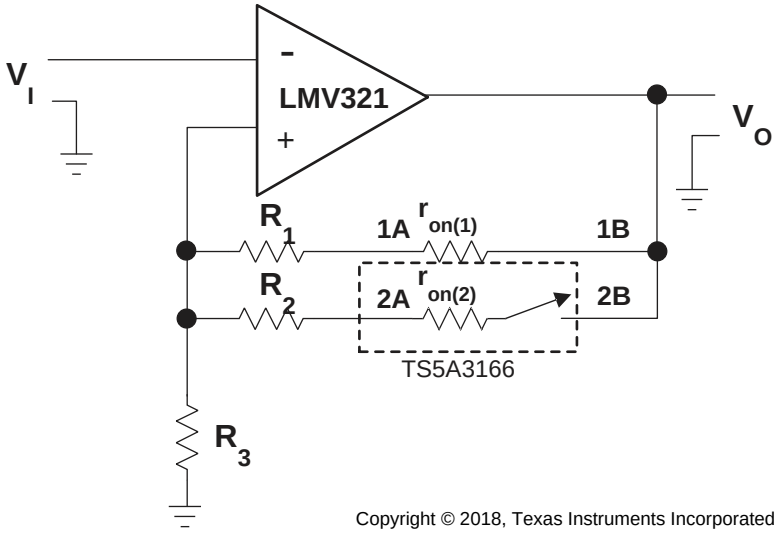


図 24. Gain-Control Circuit for Operational Amplifier

9.2.1 Design Requirements

By choosing values of R1 and R2, such that Rx >> $r_{on(x)}$, r_{on} of TS5A3166 can be ignored. The gain of operational amplifier can be calculated as follow:

$$Vo / VI = 1 + R|| / R3 \quad (1)$$

$$R|| = (R1+r_{on(1)}) \,||\, (R2+r_{on(2)}) \quad (2)$$

9.2.2 Detailed Design Procedure

Place a switch in series with the input of the operational amplifier. Since the operational amplifier input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

9.2.3 Application Curves

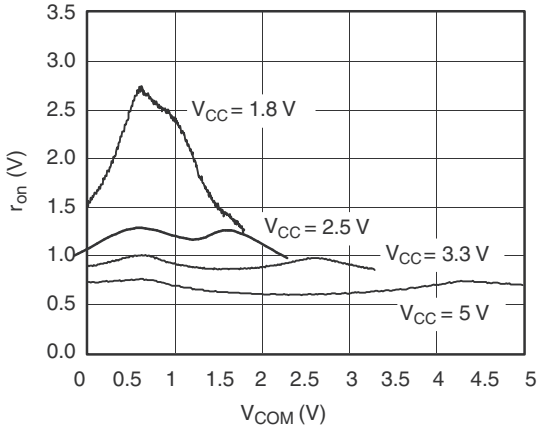


図 25. r_{on} vs V_{COM}

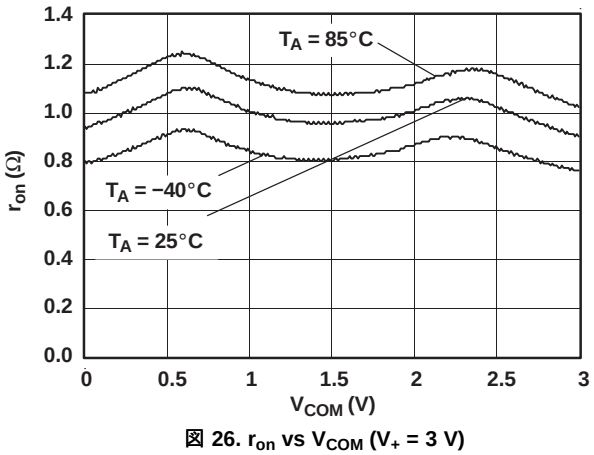


図 26. r_{on} vs V_{COM} (V_+ = 3 V)

Typical Application (continued)

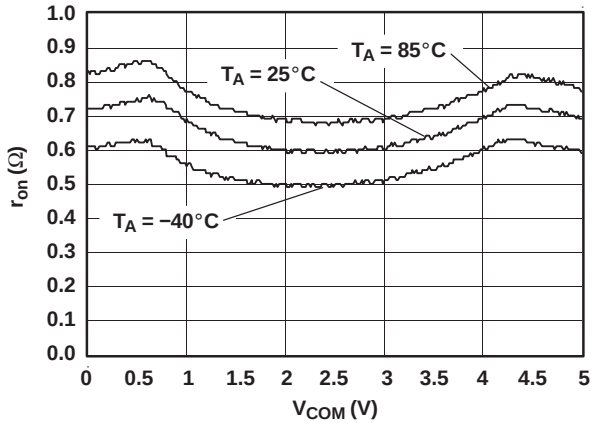


図 27. r_{on} vs V_{COM} (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 図 28 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

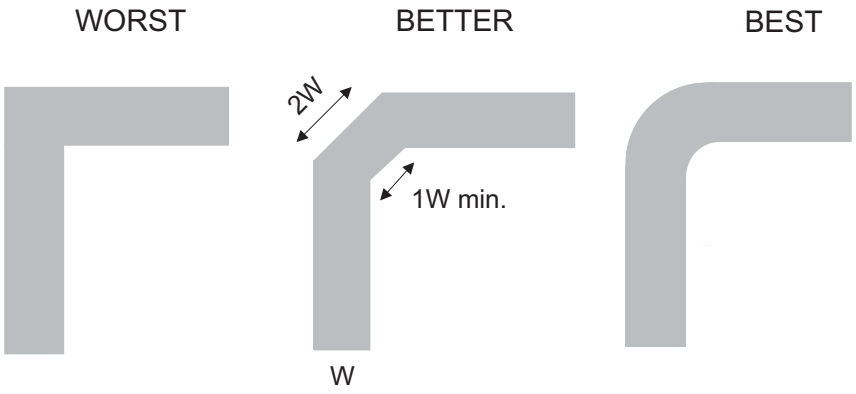


図 28. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NO}	NO電圧
r_{on}	チャネルがオンのときのCOMとNOポート間の抵抗
r_{peak}	規定電圧範囲内でのピーク・オン抵抗
$r_{on(flat)}$	規定の条件の範囲における、チャネルのr_{on}の最大値と最小値との差
$I_{NO(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NO(PWROFF)}$	パワーダウン状況、V_+ = 0のとき、NOポートで測定されるリーク電流
$I_{COM(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(COMからNO)がオフ状態のとき、COMポートで測定されるリーク電流
$I_{COM(PWROFF)}$	パワーダウン状況、V_+ = 0のとき、COMポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャネル(COMからNO)がオン状態、出力(NO)がオープンのとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN)の論理LOWの最大入力電圧
V_I	制御入力(IN)の電圧
I_{IH}、I_{IL}	制御入力(IN)で測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(COM、NO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(COM、NO)信号との間の伝搬遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NO、COM)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入$Q_C = C_L \times \Delta V_{COM}$で、$C_L$は負荷容量、$\Delta V_{COM}$はアナログ出力電圧の変化です。
$C_{NO(OFF)}$	対応チャネル(NOからCOM)がオフのときのNOポートの容量
$C_{COM(OFF)}$	対応チャネル(COMからNO)がオフのときのCOMポートの容量
$C_{NO(ON)}$	対応チャネル(NOからCOM)がオンのときのNOポートの容量
$C_{COM(ON)}$	対応チャネル(COMからNO)がオンのときのCOMポートの容量
C_I	制御入力(IN)の容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、オフ状態の対応チャネル(NOからCOM)で、特定の周波数についてdB単位で測定されます。
BW	スイッチの帯域幅。オン状態のチャネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪 は、アナログ・スイッチにより発生する信号の歪みです。この値は、2次、3次、およびさらに高次の高調波の二乗平均(RMS)値と、基本波の絶対振幅との比として定義されます。
I_+	制御(IN)ピンがV_+またはGNDであるときの静的消費電流

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3166DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JASF, JASR)
TS5A3166DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JASF, JASR)
TS5A3166DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)
TS5A3166DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)
TS5A3166YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JFN
TS5A3166YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JFN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A3166 :

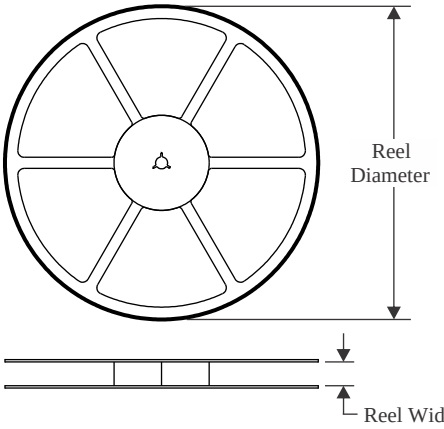
- Automotive : TS5A3166-Q1

NOTE: Qualified Version Definitions:

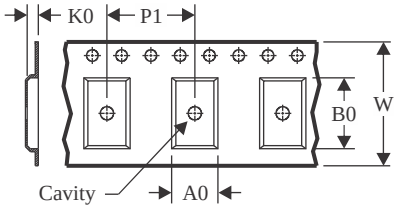
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

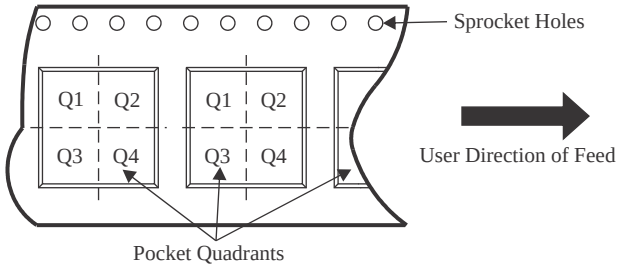


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

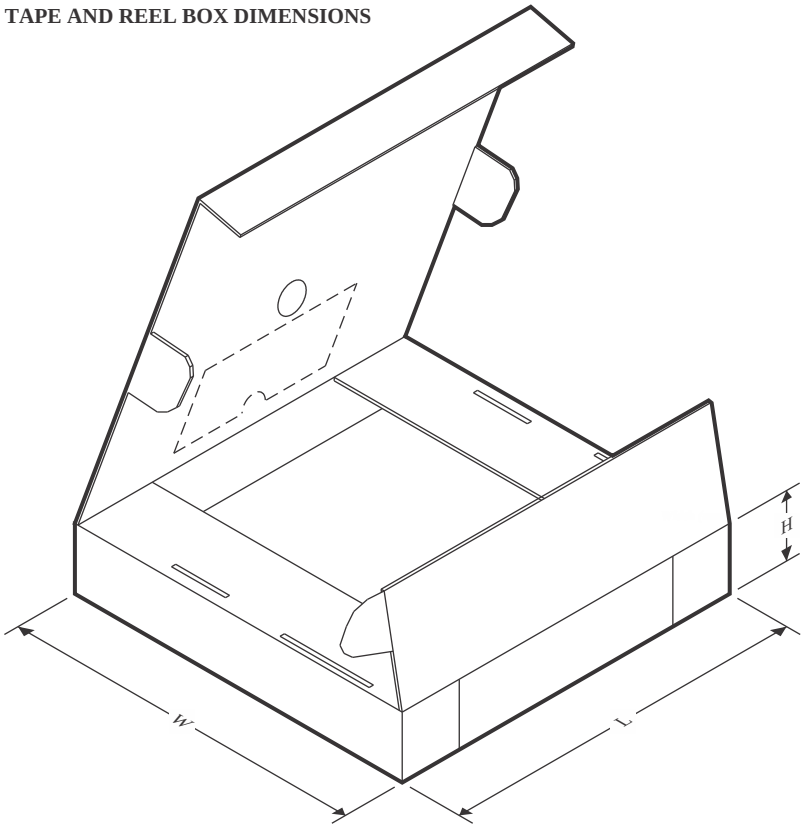
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3166YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

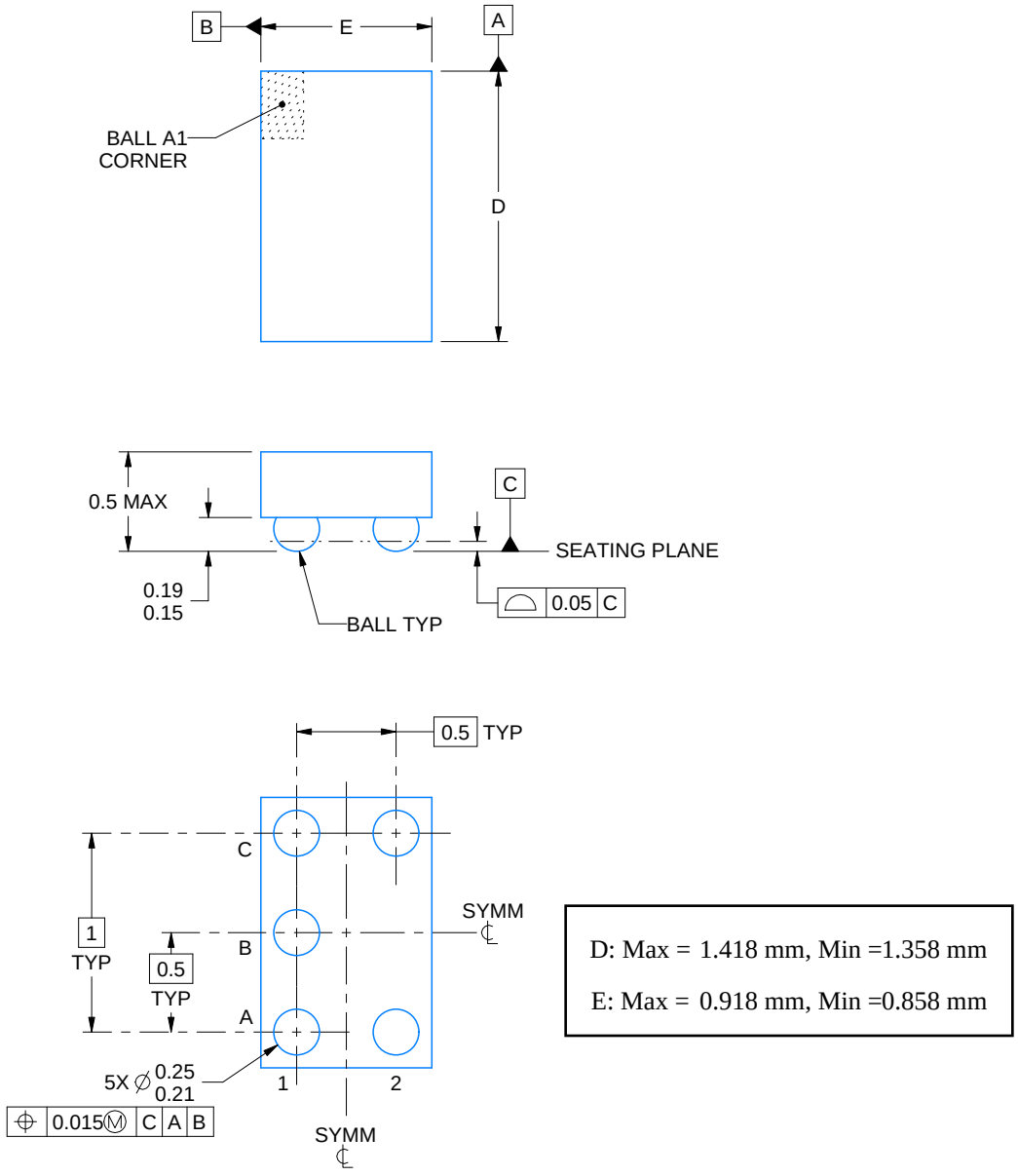
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3166YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



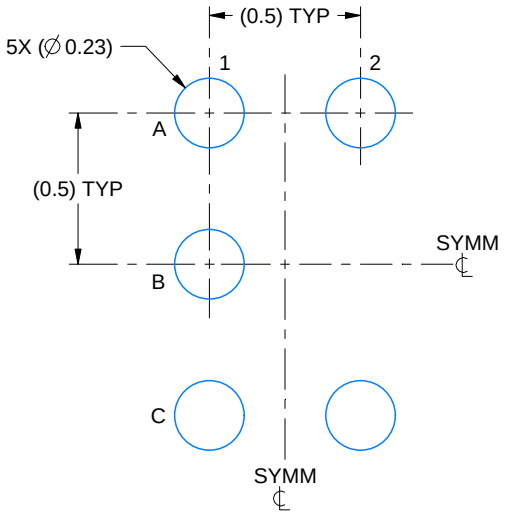
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

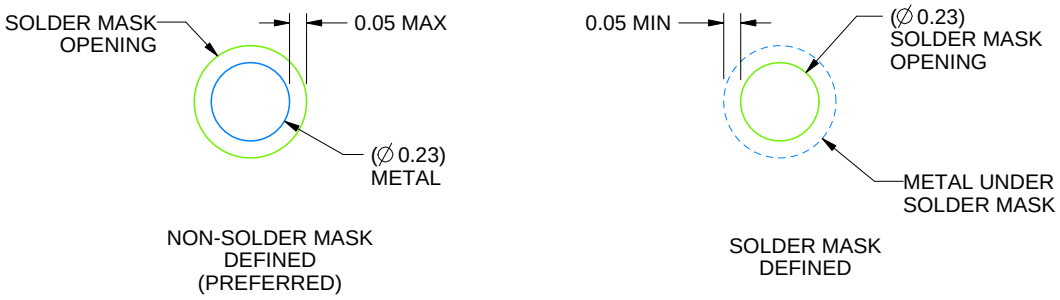
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

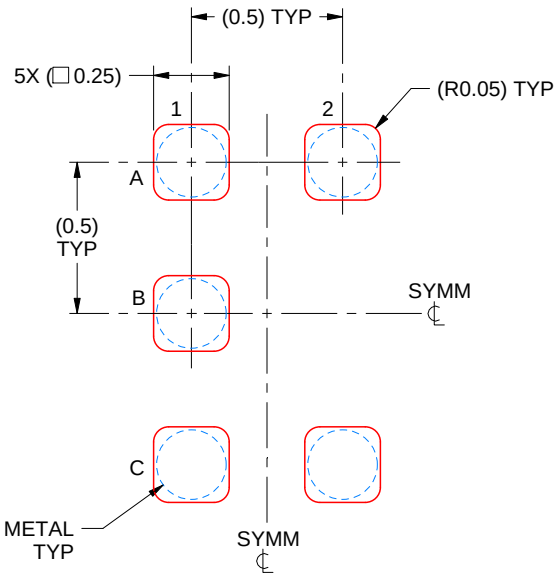


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

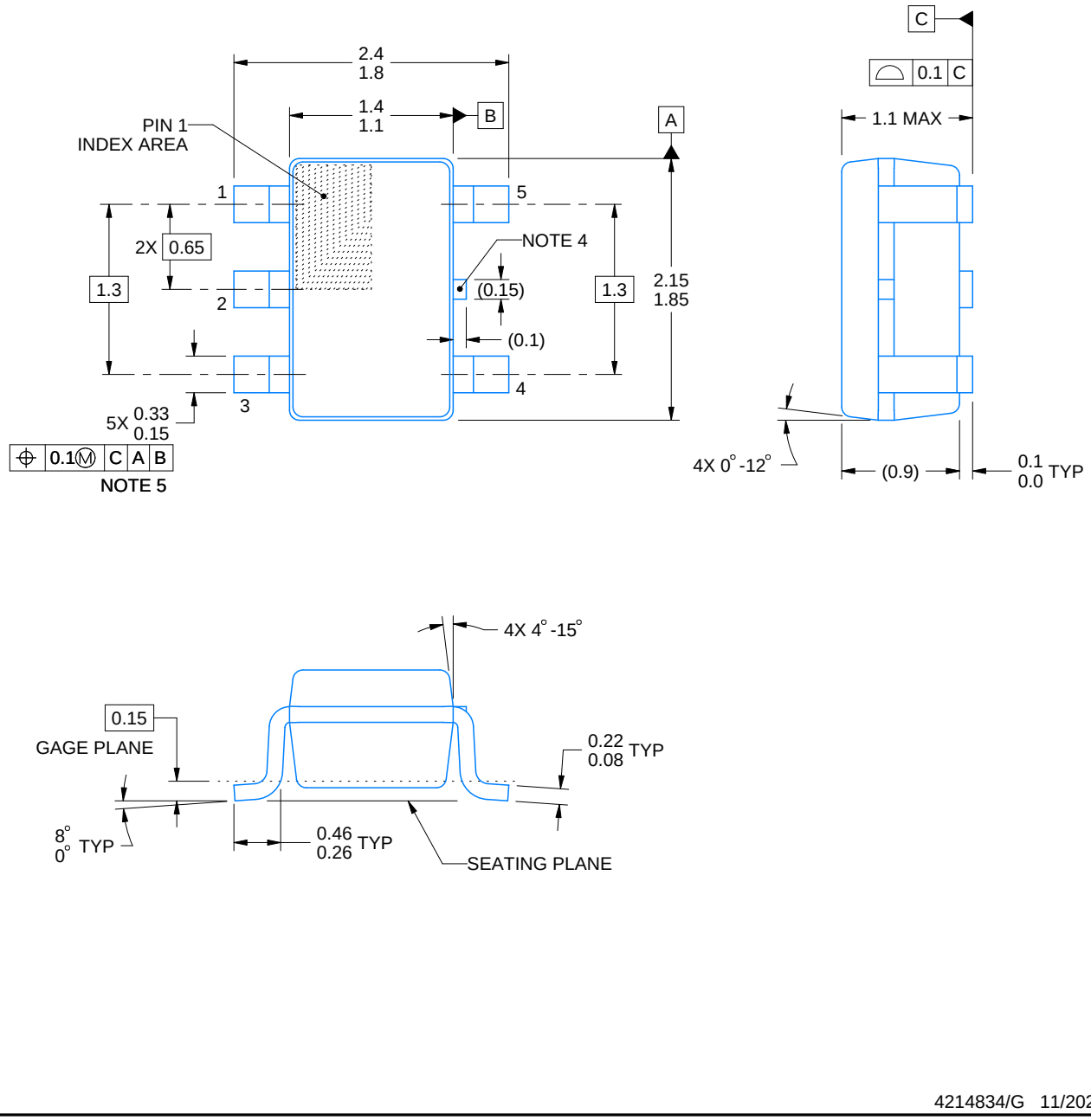
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

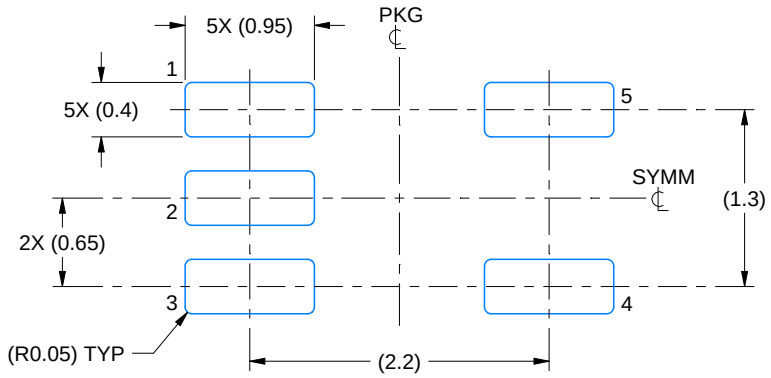
SMALL OUTLINE TRANSISTOR



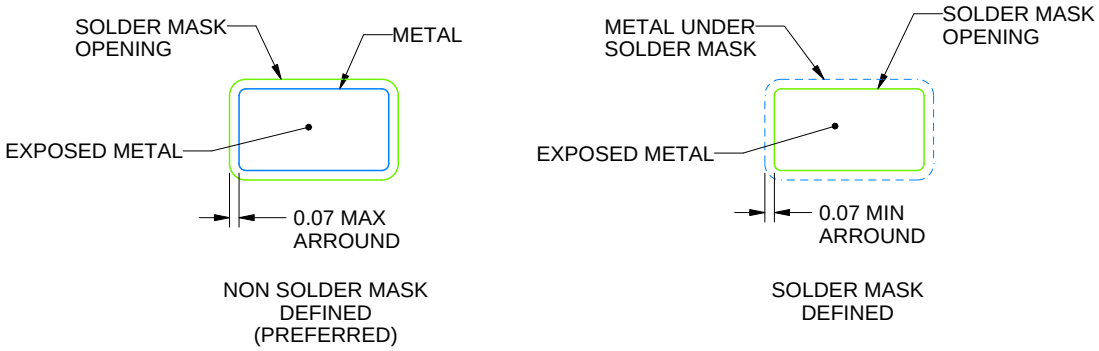
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

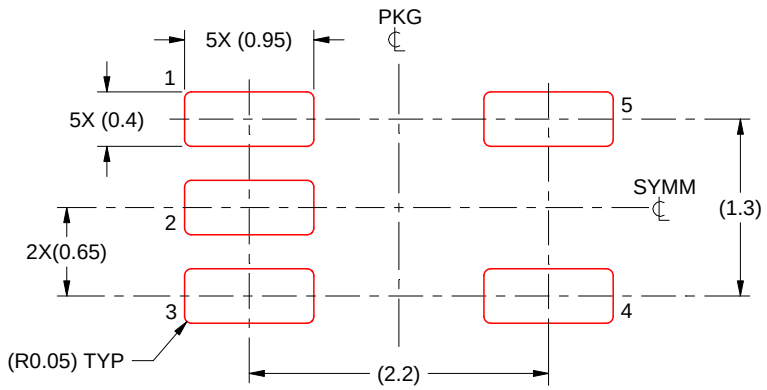


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

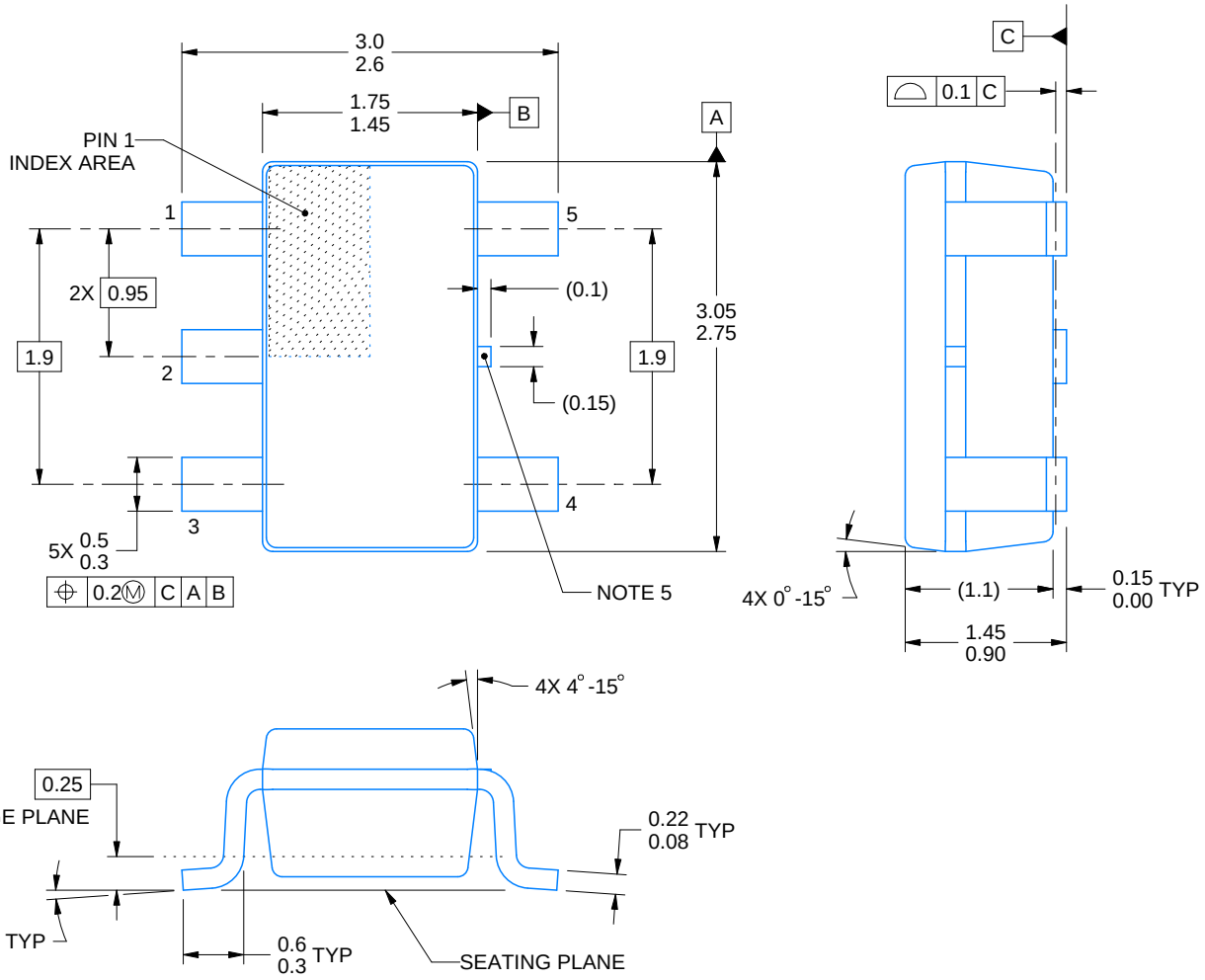
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

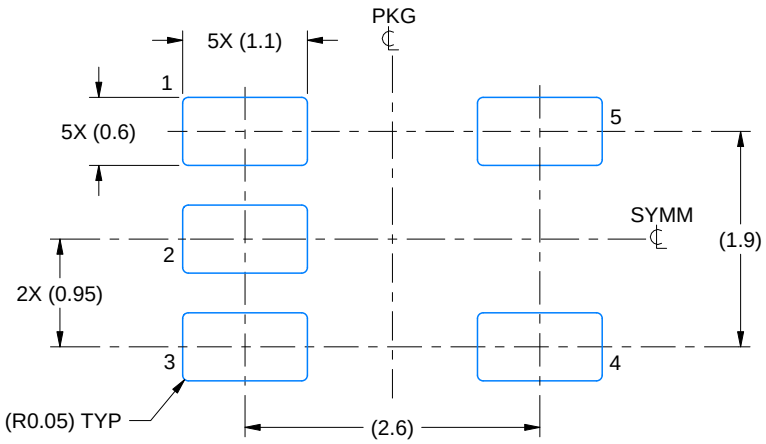
SMALL OUTLINE TRANSISTOR



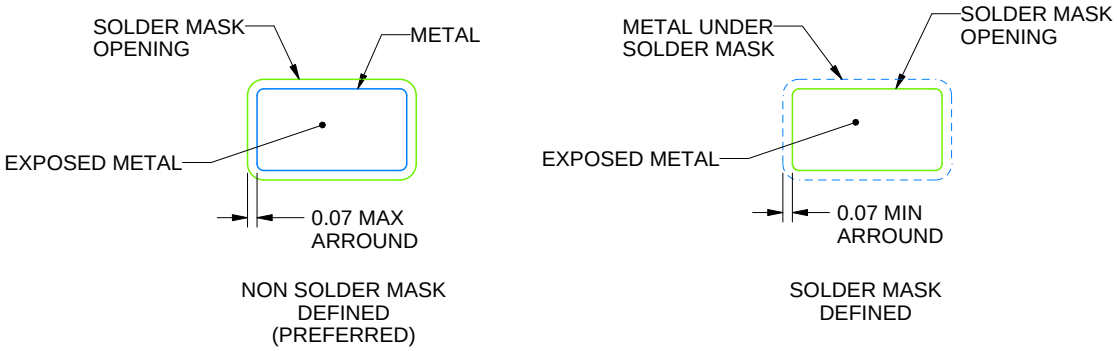
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

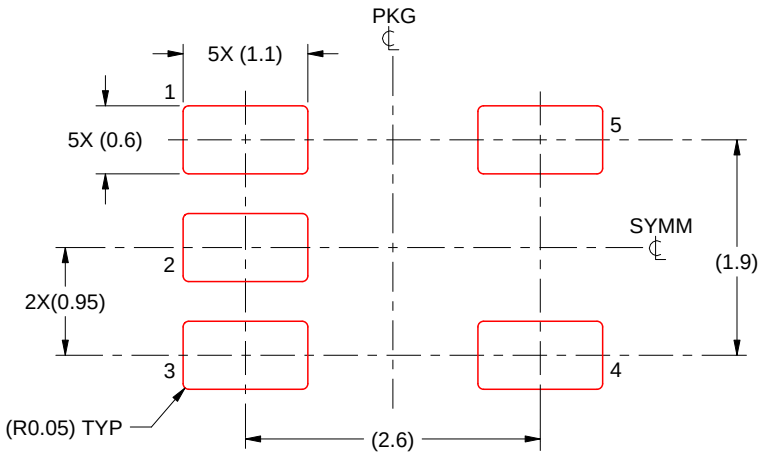


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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