

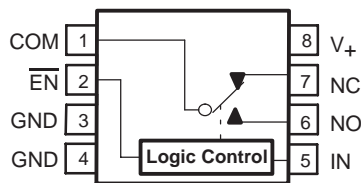
## Description

The TS5A2053 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to  $V_+$  can be transmitted in either direction.

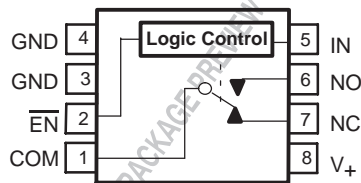
## Applications

- Cell Phones
- Portable Audio Video Equipment
- Battery-Powered Equipment
- Low-Voltage Data-Acquisition Systems
- Test Equipment
- Communication Circuits

SSOP OR VSSOP PACKAGE  
(TOP VIEW)



YEP OR YZP PACKAGE  
(BOTTOM VIEW)



FUNCTION TABLE

$\overline{\text{EN}}$	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

## Features

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

## Summary of Characteristics

$V_+ = 5 \text{ V}$  and  $T_A = 25^\circ \text{C}$

Configuration	Single Pole Double Throw (SPDT)
Number of channels	1
ON-state resistance ( $r_{\text{ON}}$ )	7.5 Ω
ON-state resistance match ( $\Delta r_{\text{ON}}$ )	0.8 Ω
ON-state resistance flatness ( $r_{\text{ON}}(\text{flat})$ )	1.7 Ω
Turn-on/turn-off time ( $t_{\text{ON}}/t_{\text{OFF}}$ )	6.8 ns/4.1 ns
Charge injection ( $Q_C$ )	3 pC
Bandwidth (BW)	330 MHz
OFF isolation ( $O_{\text{ISO}}$ )	–64 dB at 10 MHz
Crosstalk ( $X_{\text{TALK}}$ )	–68 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ( $I_{\text{COM}}(\text{OFF})$ )	±10 nA
Power-supply current ( $I_+$ )	0.1 μA
Package options	8-pin DSBGA, SSOP, or VSSOP



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TS5A2053 SINGLE-CHANNEL 10-Ω SPDT ANALOG SWITCH WITH ENABLE

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## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	TS5A2053YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		TS5A2053YZPR	
	SSOP – DCT	Tape and reel	TS5A2053DCTR	JAF_ _ _
	VSSOP – DCU	Tape and reel	TS5A2053DCUR	JAF_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

## Absolute Minimum and Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range <sup>(3)</sup>	–0.5	6.5	V
V <sub>NO</sub> V <sub>NC</sub> V <sub>COM</sub>	Analog voltage range <sup>(3)(4)(5)</sup>	–0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> < 0 or V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub> > V <sub>+</sub>		–50 50 mA
I <sub>NO</sub> I <sub>NC</sub> I <sub>COM</sub>	On-state switch current	V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		–50 50 mA
V <sub>I</sub>	Digital input voltage range <sup>(3)(4)</sup>	–0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		–50 mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>			100 mA
I <sub>GND</sub>	Continuous current through GND			–100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(6)</sup>	DCT package		220
		DCU package		227
		YEP/YZP package		102
T <sub>stg</sub>	Storage temperature range	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(5) This value is limited to 5.5 V maximum.

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -32 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V	7.5		13.8 16	Ω
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 3.15 \text{ V}$ , $I_{COM} = -32 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V	0.8		4.5	Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -32 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V	1.7		4.5	Ω
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} \text{ or } V_{NC} = 1 \text{ V}$ , $V_{COM} = 4.5 \text{ V}$ , or $V_{NO} \text{ or } V_{NC} = 4.5 \text{ V}$ , $V_{COM} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-100	5	100 200	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = 4.5 \text{ V}$ , or $V_{COM} = 4.5 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-100	-1	100 200	nA
NO, NC ON leakage current	$I_{NO(ON)}, I_{NC(ON)}$	$V_{NO} = 1 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 4.5 \text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-100	5.5	100 200	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , or $V_{COM} = 4.5 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-100	-1	100 200	nA
<b>Digital Control Inputs (IN, EN)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.7$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.3$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C Full	5.5 V	-0.1	0.05	0.1 1	μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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### Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = 3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	3.8	5.3	6.8	ns
			Full	4.5 V to 5.5 V	3		7.1	
Turn-off time	$t_{OFF}$	$V_{COM} = 3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	0.8	1.9	4.1	ns
			Full	4.5 V to 5.5 V	0.4		4.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See Figure 21	25°C	5 V		3		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ , $C_{NC(OFF)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch OFF, See Figure 16	25°C	5 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	5 V		9.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$ , $C_{NC(ON)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch ON, See Figure 16	25°C	5 V		18		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	5 V		18		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	5 V		2.5		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	5 V		330		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See Figure 19	25°C	5 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See Figure 20	25°C	5 V		-68		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	5 V		0.01		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V		0.1	1	$\mu\text{A}$
			Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See Figure 13	25°C Full	3 V	13.2 20			Ω
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.1\text{ V}$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See Figure 13	25°C Full	3 V	1 5.5			Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See Figure 13	25°C Full	3 V	5.3 11			Ω
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} \text{ or } V_{NC} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NO} \text{ or } V_{NC} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-100 -200	4 200	100	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} \text{ or } V_{NC} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} \text{ or } V_{NC} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-100 -200	-1 200	100	nA
NO, NC ON leakage current	$I_{NO(ON)}, I_{NC(ON)}$	$V_{NO} \text{ or } V_{NC} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} \text{ or } V_{NC} = 3\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-100 -200	4.5 200	100	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-100 -200	-1 200	100	nA
<b>Digital Control Inputs (<math>I_N, \overline{EN}</math>)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.7$ 5.5			V
Input logic low	$V_{IL}$		Full		0 $V_+ \times 0.3$			V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C Full	3.6 V	-0.1 -1	0.05 1	0.1	μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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### Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = 2\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	5	6.4	7.9	ns
			Full	3 V to 3.6 V	4.5		8.2	
Turn-off time	$t_{OFF}$	$V_{COM} = 2\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	1.1	2.4	4.7	ns
			Full	3 V to 3.6 V	0.3		5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See Figure 21	25°C	3.3 V		1		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch OFF, See Figure 16	25°C	3.3 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	3.3 V		9.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch ON, See Figure 16	25°C	3.3 V		18.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	3.3 V		18.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	3.3 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	3.3 V		320		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See Figure 19	25°C	3.3 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See Figure 20	25 °C	3.3 V		-68		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	3.3 V		0.035		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V		0.1	1	$\mu\text{A}$
			Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.3 V	20		40	Ω
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.6 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.3 V	1.1		6	Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.3 V	15		20	Ω
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} \text{ or } V_{NC} = 0.5 \text{ V}$ , $V_{COM} = 2.2 \text{ V}$ , or $V_{NO} \text{ or } V_{NC} = 2.2 \text{ V}$ , $V_{COM} = 0.5 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	2.7 V	-100	3.5	100	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0.5 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = 2.2 \text{ V}$ , or $V_{COM} = 2.2 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = 0.5 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	2.7 V	-100	-2	100	nA
NO, NC ON leakage current	$I_{NO(ON)}, I_{NC(ON)}$	$V_{NO} \text{ or } V_{NC} = 0.5 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} \text{ or } V_{NC} = 2.2 \text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	2.7 V	-100	4	100	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.5 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , or $V_{COM} = 2.2 \text{ V}$ , $V_{NO} \text{ or } V_{NC} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	2.7 V	-100	-2	100	nA
<b>Digital Control Inputs (IN, <math>\overline{\text{EN}}</math>)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.7$		5.5	V
Input logic low	$V_{IL}$		Full		0	$V_+ \times 0.3$		V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C Full	2.7 V	-0.1	0.05	0.1	μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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### Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = 1.5 \text{ V}$ , $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	5.9	7.1	9.3	ns
			Full	2.3 V to 2.7 V	5.1		10	
Turn-off time	$t_{OFF}$	$V_{COM} = 1.5 \text{ V}$ , $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	2.1	3.2	5.1	ns
			Full	2.3 V to 2.7 V	1.2		5.2	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1 \text{ nF}$ , See Figure 21	25°C	2.5 V		0.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ $C_{NC(OFF)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		10		pF
NO, NC ON capacitance	$C_{NO(ON)}$ $C_{NC(ON)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		18.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		18.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON, See Figure 18	25°C	2.5 V		320		MHz
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ , Switch OFF, See Figure 19	25°C	2.5 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ , Switch ON, See Figure 20	25 °C	2.5 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See Figure 22	25°C	2.5 V		0.26		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V		0.1	1	$\mu\text{A}$
			Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



## Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

$V_+ = 1.65 \text{ V}$  to  $1.95 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		$V_+$	V
ON-state resistance	$r_{\text{on}}$	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$ , $I_{\text{COM}} = -4 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	1.65 V		85	120	Ω
ON-state resistance match between channels	$\Delta r_{\text{on}}$	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.15 \text{ V}$ , $I_{\text{COM}} = -4 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	1.65 V		2	7.5	Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$ , $I_{\text{COM}} = -4 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	1.65 V		76	100	Ω
NO, NC OFF leakage current	$I_{\text{NO(OFF)}}, I_{\text{NC(OFF)}}$	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 0.3 \text{ V}$ , $V_{\text{COM}} = 1.65 \text{ V}$ , or $V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.65 \text{ V}$ , $V_{\text{COM}} = 0.3 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	1.95 V	-100	3.5	100	nA
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{COM}} = 0.3 \text{ V}$ , $V_{\text{NO}} = 1.65 \text{ V}$ , or $V_{\text{COM}} = 1.65 \text{ V}$ , $V_{\text{NO}} = 0.3 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	1.95 V	-100	1	100	nA
NO, NC ON leakage current	$I_{\text{NO(ON)}}, I_{\text{NC(ON)}}$	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 0.3 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ , or $V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.65 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	1.95 V	-100	4	100	nA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{COM}} = 0.3 \text{ V}$ , $V_{\text{NO}} \text{ or } V_{\text{NC}} = \text{Open}$ , or $V_{\text{COM}} = 1.65 \text{ V}$ , $V_{\text{NO}} \text{ or } V_{\text{NC}} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	1.95 V	-100	1	100	nA
<b>Digital Control Inputs (<math>I_{\text{IN}}, \overline{\text{EN}}</math>)</b>								
Input logic high	$V_{\text{IH}}$		Full		$V_+ \times 0.65$		5.5	V
Input logic low	$V_{\text{IL}}$		Full		0		$V_+ \times 0.35$	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 5.5 \text{ V}$ or 0	25°C Full	1.95 V	-0.1	0.05	0.1	μA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

# TS5A2053

## SINGLE-CHANNEL 10-Ω SPDT ANALOG SWITCH WITH ENABLE

SCDS183A – JANUARY 2005 – REVISED APRIL 2006

### Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = 1.3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	10.2	11.8	14.5	ns
			Full	1.65 V to 1.95 V	8.4		15.5	
Turn-off time	$t_{OFF}$	$V_{COM} = 1.3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	2.9	4.3	6.5	ns
			Full	1.65 V to 1.95 V	2.2		7	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See Figure 21	25°C	1.8 V		0.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ , $C_{NC(OFF)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch OFF, See Figure 16	25°C	1.8 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	1.8 V		10		pF
NO, NC ON capacitance	$C_{NO(ON)}$ , $C_{NC(ON)}$	$V_{NO}$ or $V_{NC} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V		19		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V		14		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	1.8 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	1.8 V		320		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See Figure 19	25°C	1.8 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See Figure 20	25 °C	1.8 V		-68		dB
Total harmonic distortion	THD	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	1.8 V		2.6		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V		0.1	1	$\mu\text{A}$
			Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## TYPICAL PERFORMANCE

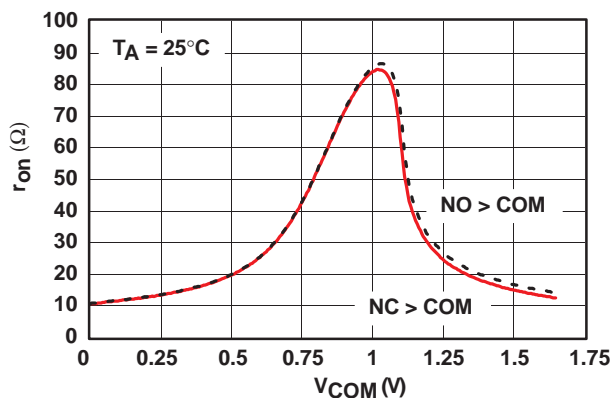


Figure 1A.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 1.65$  V)

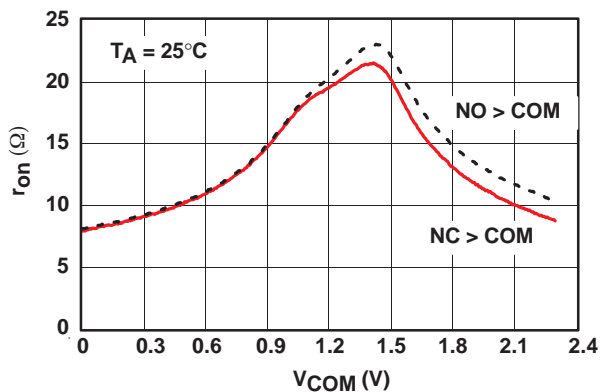


Figure 1B.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 2.3$  V)

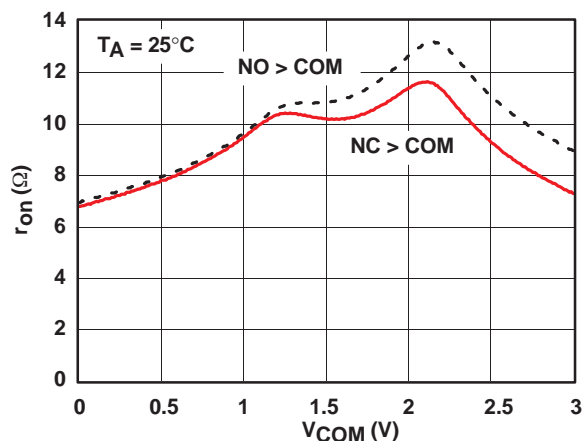


Figure 1C.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3$  V)

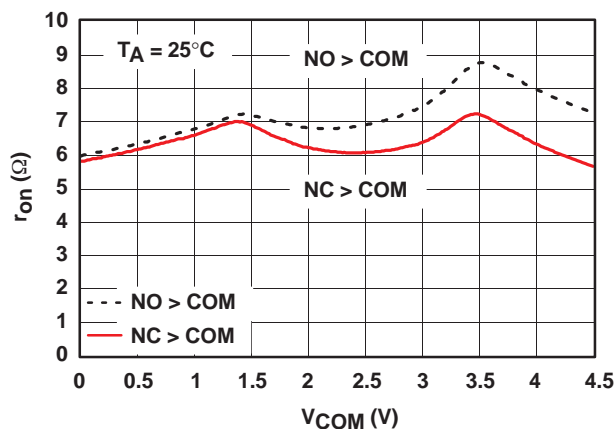


Figure 1D.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 4.5$  V)

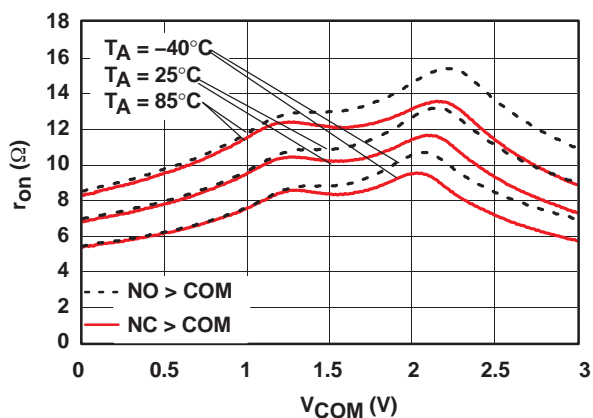


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3$  V)

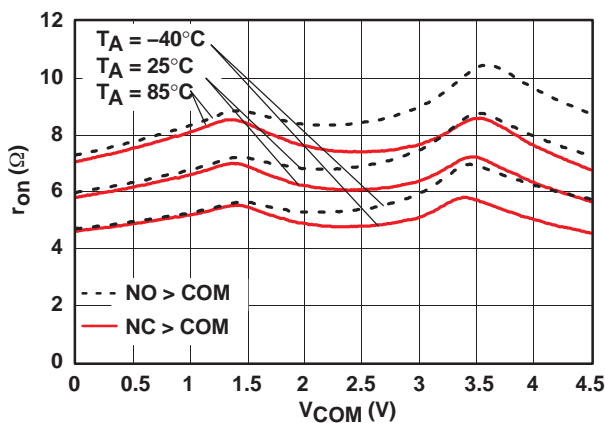
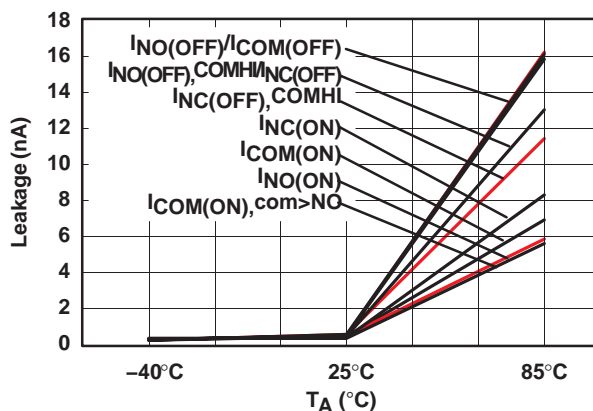
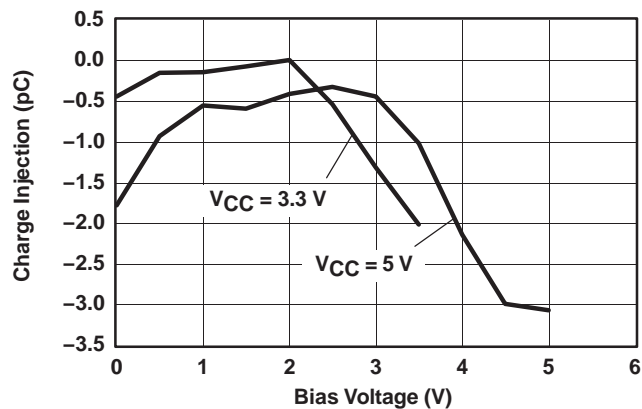


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 4.5$  V)

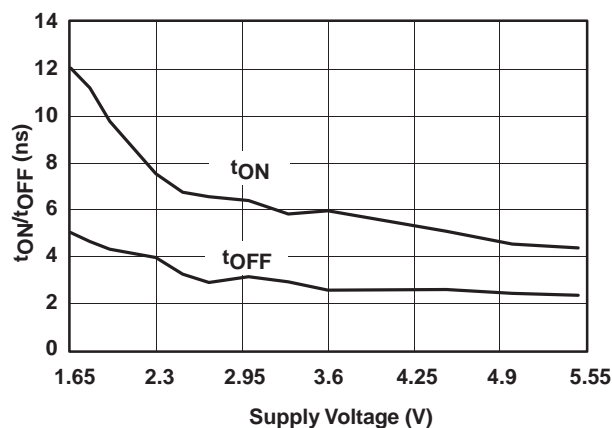
**TYPICAL PERFORMANCE (continued)**



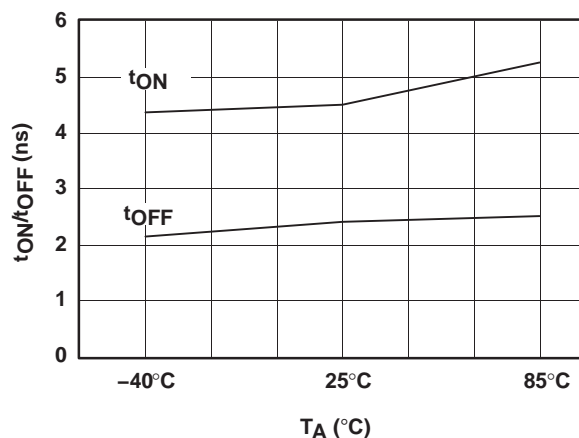
**Figure 4. Leakage Current vs Temperature**  
( $V_+ = 5.5 \text{ V}$ )



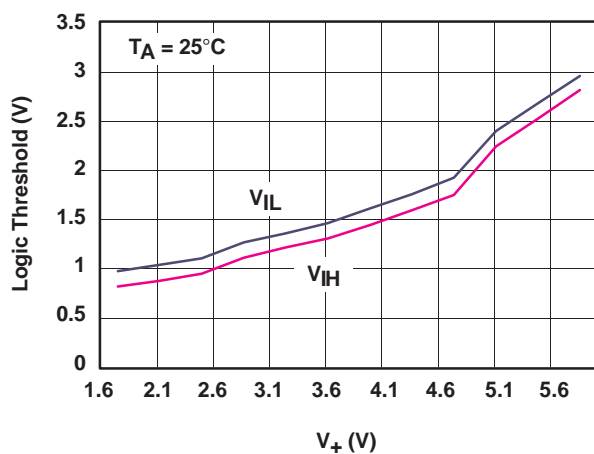
**Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$**



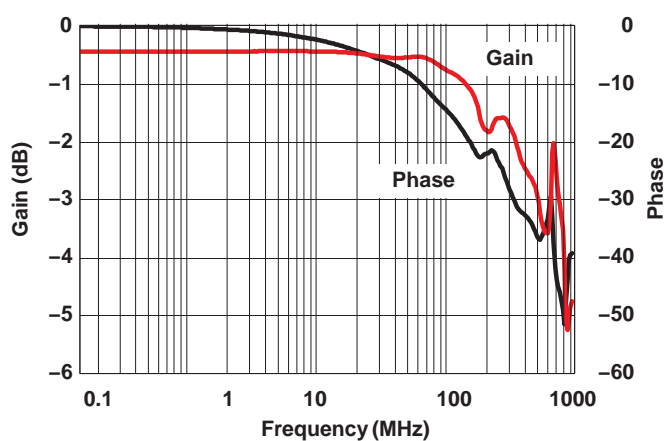
**Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs  $V_+$**



**Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5 \text{ V}$ )**



**Figure 8. Logic Threshold vs  $V_+$**



**Figure 9. Bandwidth ( $V_+ = 5 \text{ V}$ )**

TYPICAL PERFORMANCE (continued)

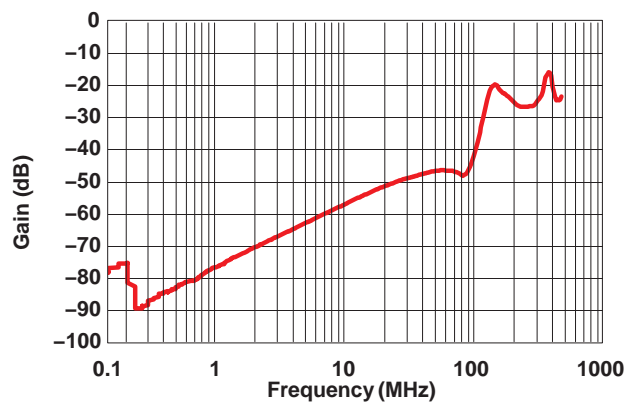


Figure 10. OFF Isolation ( $V_+ = 5\text{ V}$ )

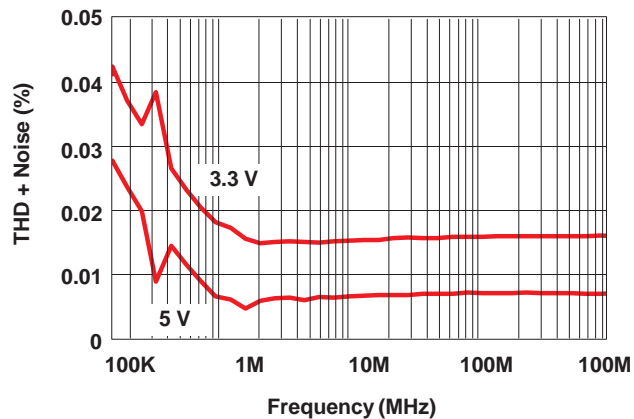


Figure 11. Total Harmonic Distortion vs Frequency

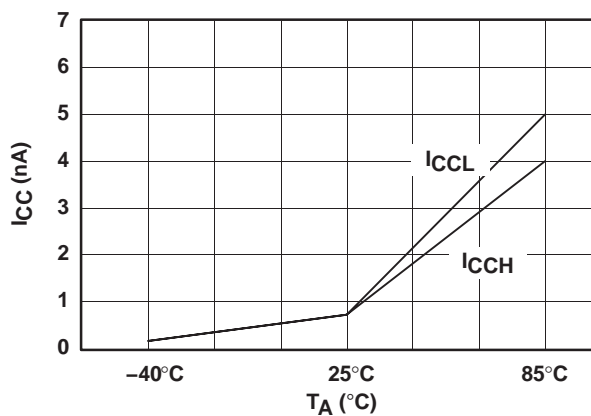


Figure 12. Power-Supply Current vs Temperature  
( $V_+ = 5\text{ V}$ )

# TS5A2053

## SINGLE-CHANNEL 10-Ω SPDT ANALOG SWITCH WITH ENABLE

SCDS183A – JANUARY 2005 – REVISED APRIL 2006

### PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	COM	Common
2	$\overline{\text{EN}}$	Chip enable (active low)
3	GND	Digital ground
4	GND	Digital ground
5	IN	Digital control to connect COM to NC or NO
6	NO	Normally open
7	NC	Normally closed
8	V <sub>+</sub>	Power supply

### PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NC</sub>	Voltage at NC
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr <sub>on</sub>	Difference of r <sub>on</sub> between channels in a specific device
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of r <sub>on</sub> in a channel over the specified range of conditions
I <sub>NC(OFF)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NC(ON)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the OFF state and the output (NC or NO) open
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN, $\overline{\text{EN}}$ )
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN, $\overline{\text{EN}}$ )
V <sub>I</sub>	Voltage at the control input (IN, $\overline{\text{EN}}$ )
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN, $\overline{\text{EN}}$ )
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q <sub>C</sub> = C <sub>L</sub> × ΔV <sub>COM</sub> , C <sub>L</sub> is the load capacitance and ΔV <sub>COM</sub> is the change in analog output voltage.

**PARAMETER DESCRIPTION (continued)**

SYMBOL	DESCRIPTION
CNC(OFF)	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
CNO(OFF)	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
CNC(ON)	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
CNO(ON)	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
CCOM(OFF)	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is OFF
CCOM(ON)	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C <sub>I</sub>	Capacitance of control input (IN, $\overline{\text{EN}}$ )
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X <sub>TALK</sub>	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I <sub>+</sub>	Static power-supply current with the control (IN, $\overline{\text{EN}}$ ) pin at V <sub>+</sub> or GND

## PARAMETER MEASUREMENT INFORMATION

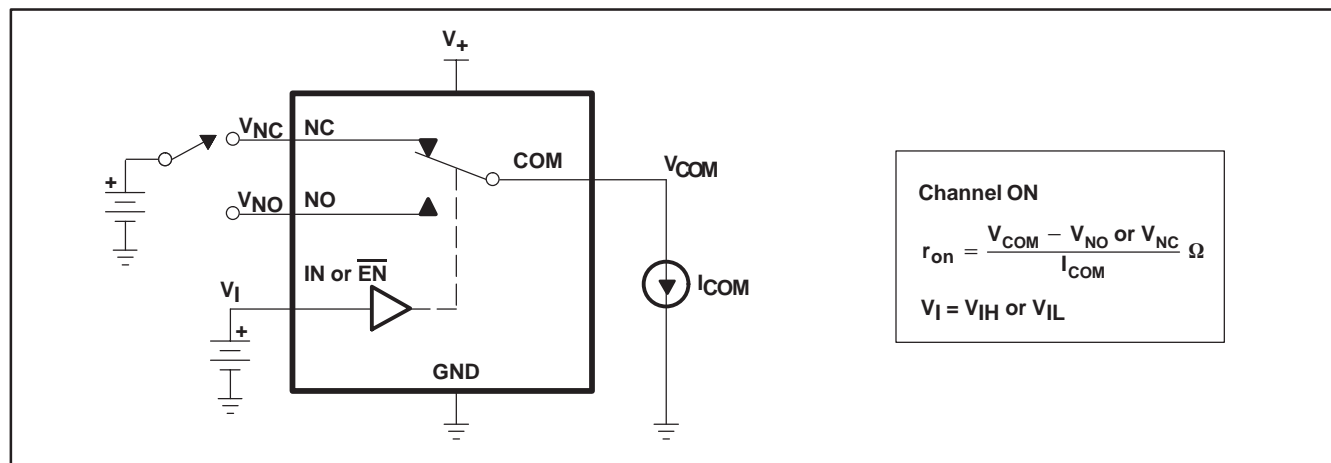


Figure 13. ON-State Resistance ( $r_{on}$ )

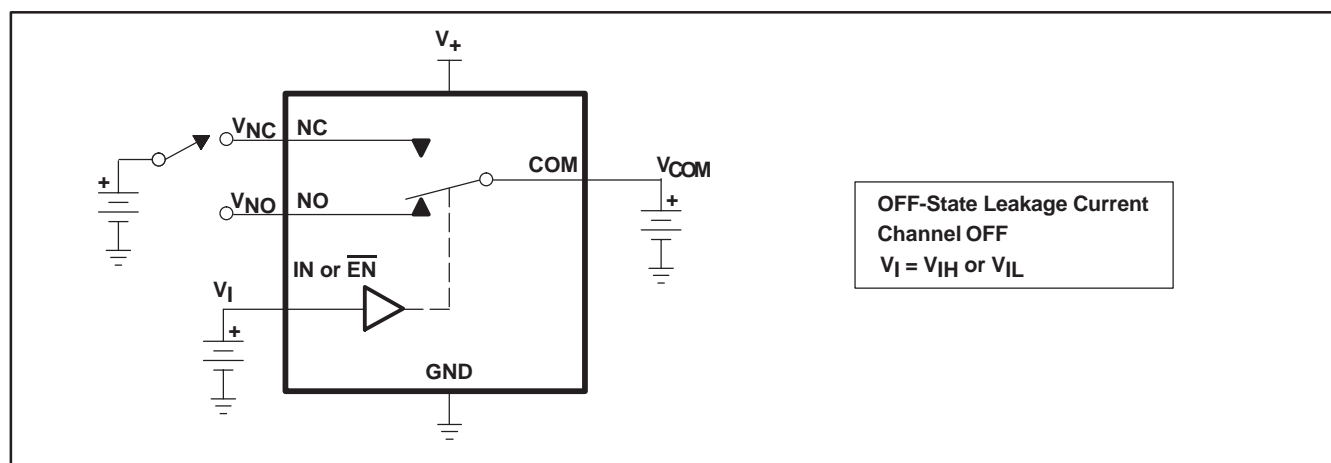


Figure 14. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{COM(OFF)}$ )

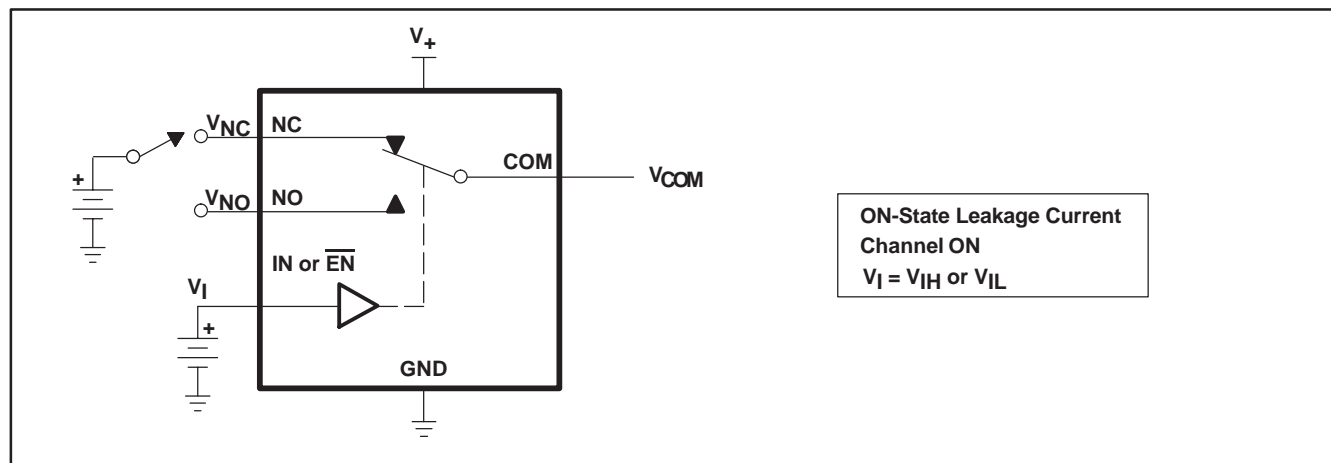


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )





# TS5A2053 SINGLE-CHANNEL 10-Ω SPDT ANALOG SWITCH WITH ENABLE

SCDS183A – JANUARY 2005 – REVISED APRIL 2006

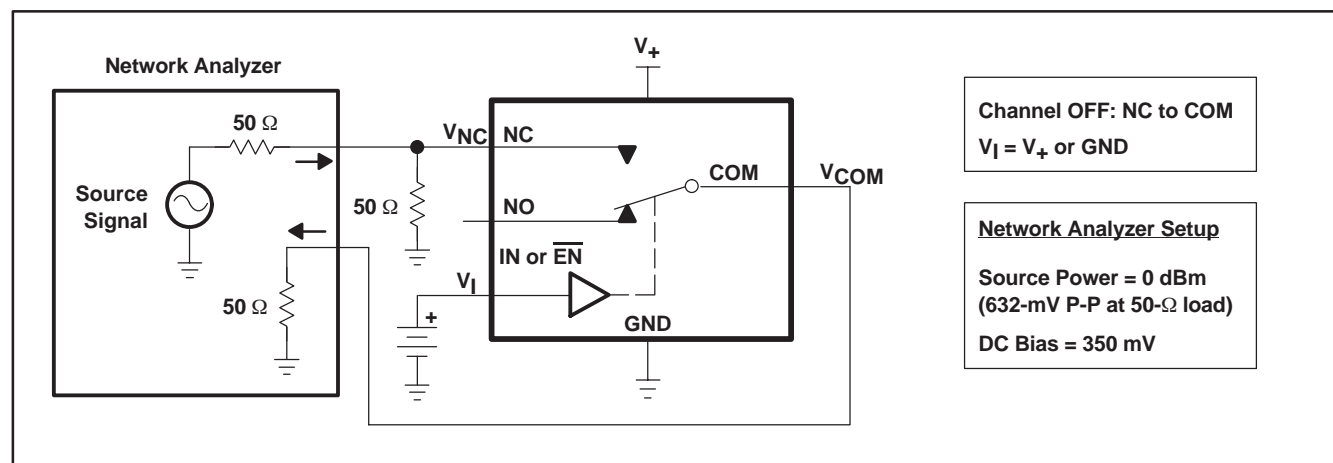


Figure 19. OFF Isolation ( $O_{ISO}$ )

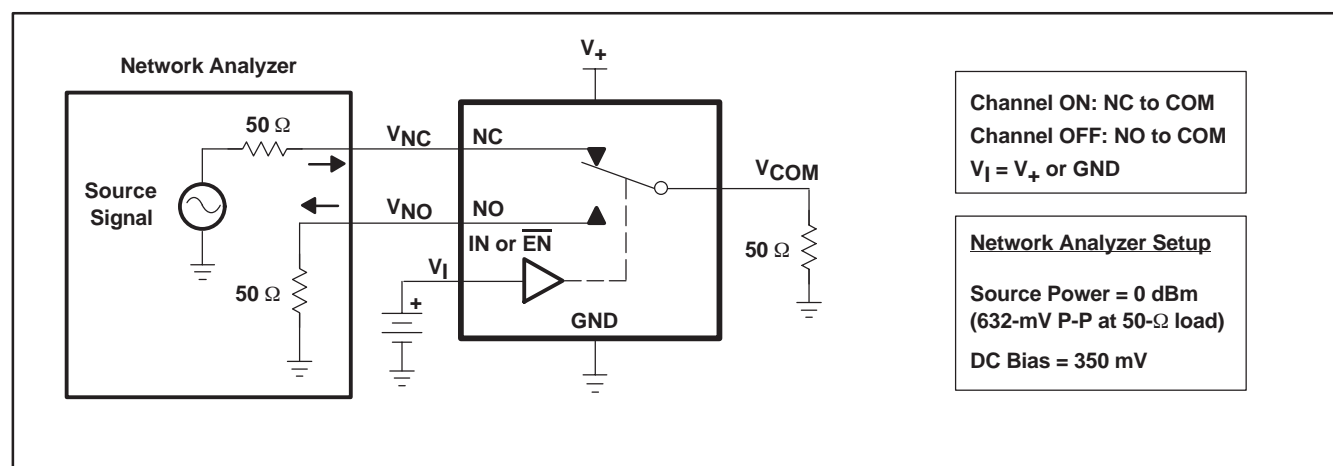
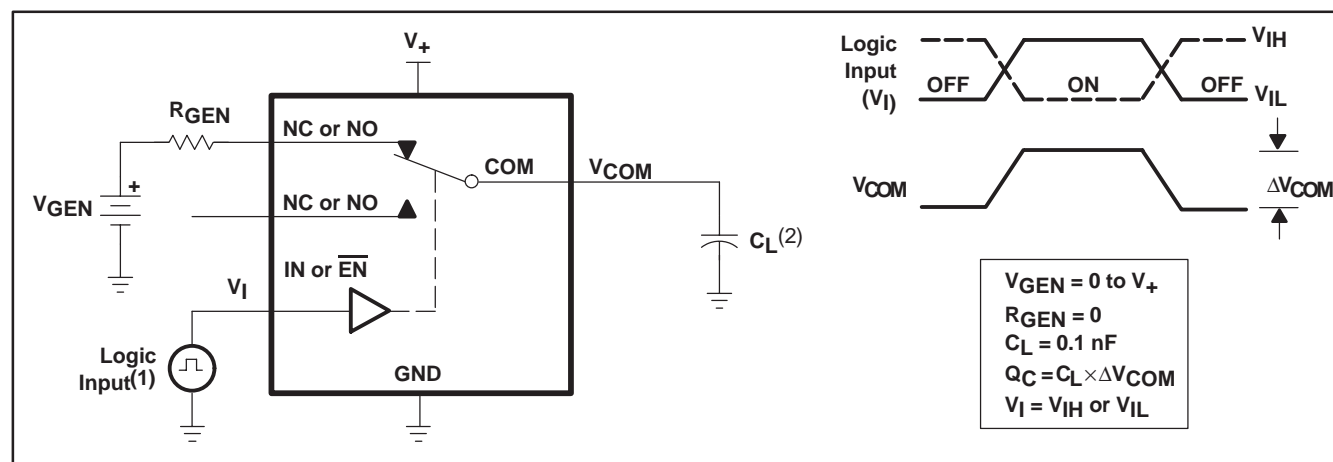


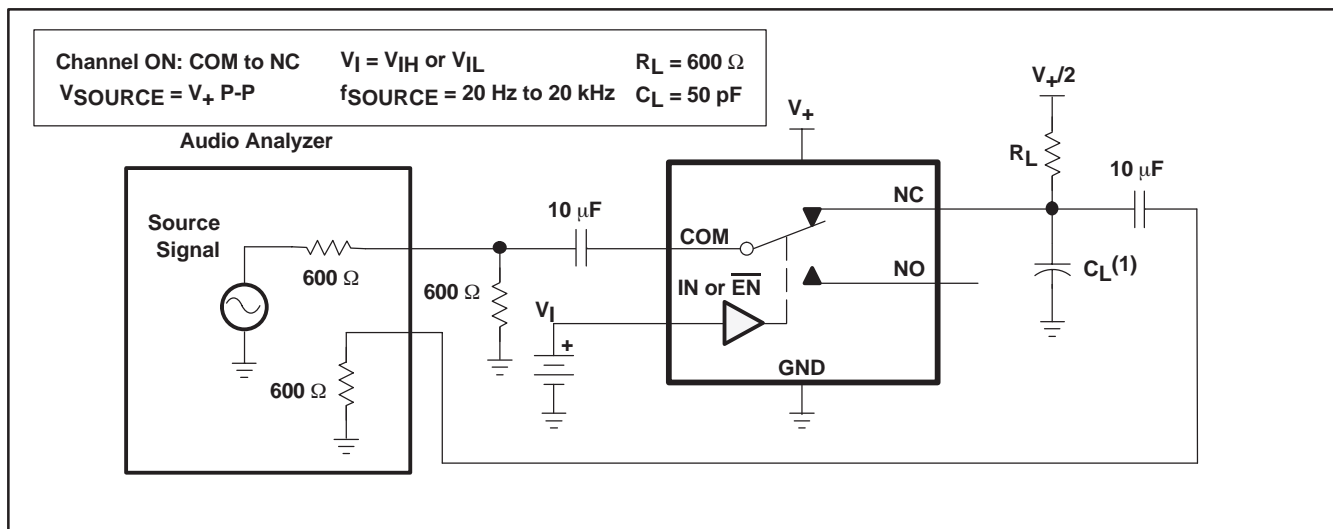
Figure 20. Crosstalk ( $X_{TALK}$ )



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

(2)  $C_L$  includes probe and jig capacitance.

Figure 21. Charge Injection ( $Q_C$ )



(1)  $C_L$  includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A2053DCTR</a>	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAF (R, Z)
TS5A2053DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAF (R, Z)
<a href="#">TS5A2053DCUR</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(AF, JAFQ, JAFR) JZ
TS5A2053DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(AF, JAFQ, JAFR) JZ
<a href="#">TS5A2053DCURG4</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAFR
TS5A2053DCURG4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAFR

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2053DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2053DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TS5A2053DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2053DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A2053DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
TS5A2053DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
TS5A2053DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TS5A2053DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0



4225266/A 09/2014

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

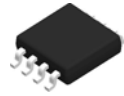


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

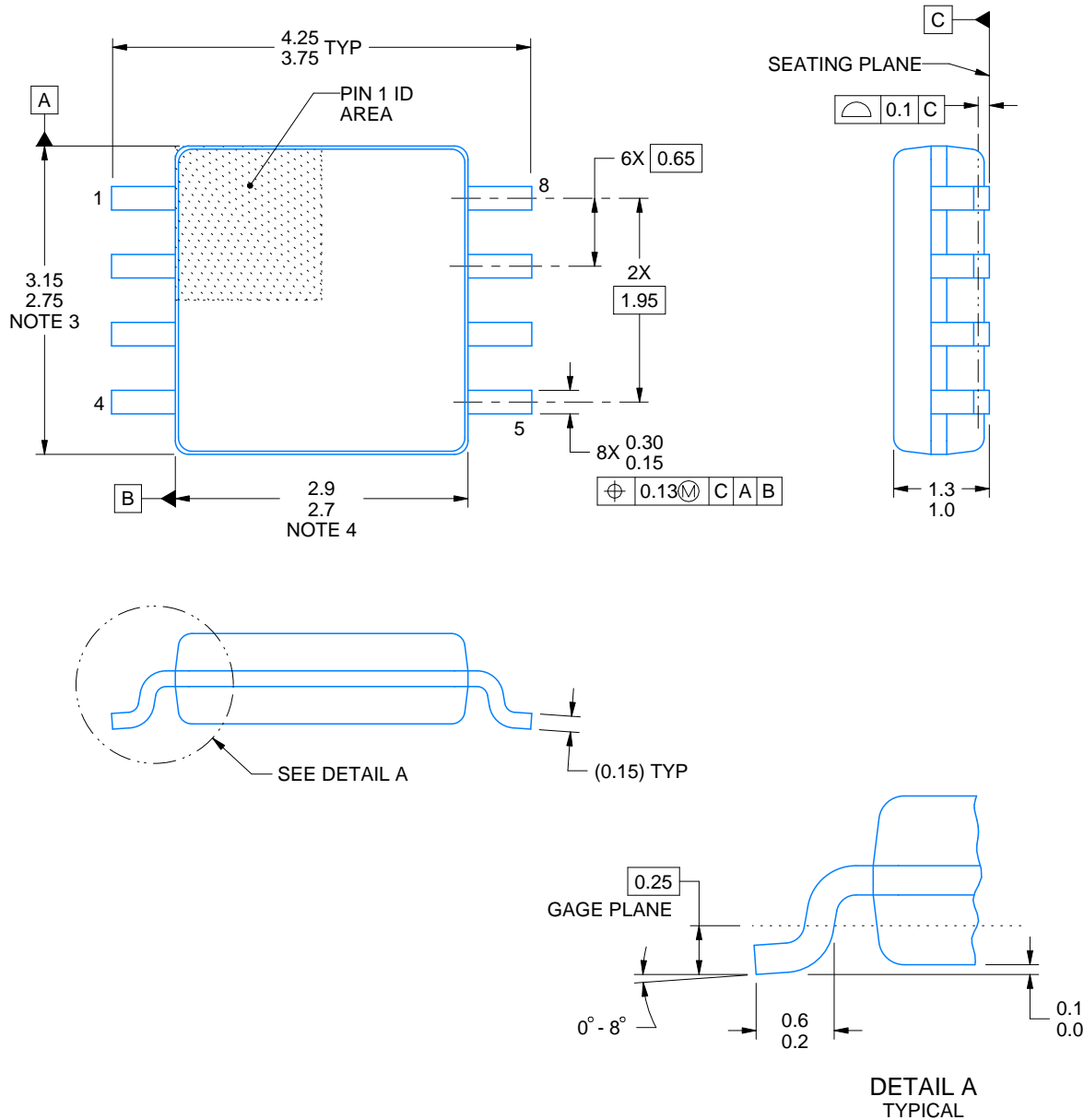
4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**DCT0008A****PACKAGE OUTLINE****SSOP - 1.3 mm max height**

SMALL OUTLINE PACKAGE



4220784/C 06/2021

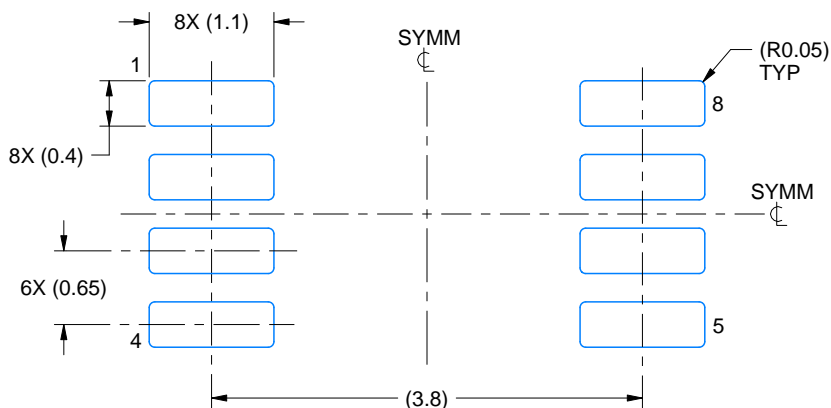
**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

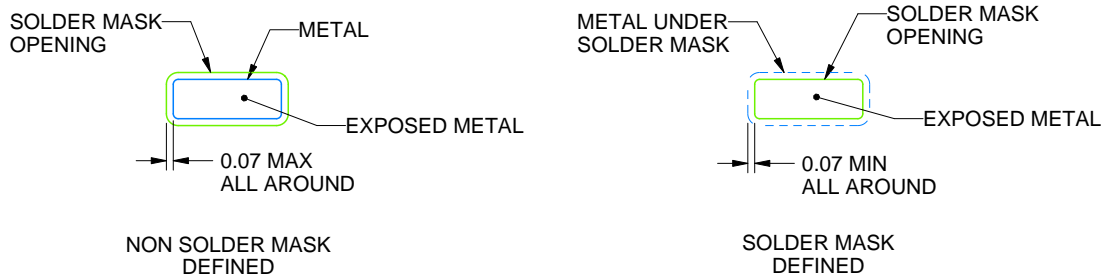
**DCT0008A**

### SSOP - 1.3 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



## SOLDER MASK DETAILS

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NOTES: (continued)

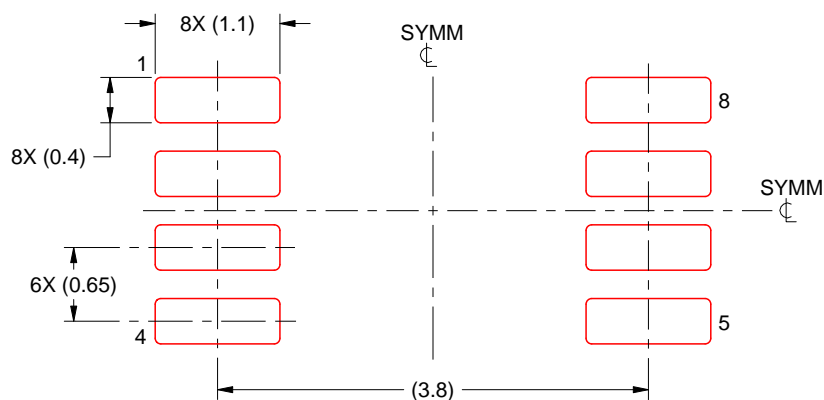
5. Publication IPC-7351 may have alternate designs.  
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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