

TS3DV642-Q1 6Gbps 12 チャネル差動 1 : 2 / 2 : 1 マルチプレクサ

1 特長

- 車載用に Q100 認証取得済み
- -40°C~105°Cの温度範囲 (グレード 2)
- 6 つの差動または 12 のシングルエンド信号、または差動/シングル・エンドの他の組み合わせをサポート
- HDMI 1.4b/2.0、DisplayPort 1.4 HBR2、DP++、Mipi DPHY / CPHY DSI / CSI-2、LVDS をサポート
- 双方向アナログ・マルチプレクサ: 0V~5.5V の範囲、DC~6Gbps の範囲でのほとんどの電気信号に対応
- 5.8GHz の -3dB 差動帯域幅
- 非常に優れた動的性能
 - 挿入損失: 3.0GHz において -1.6dB
 - 反射 (リターン) 損失: 3.0GHz において -17dB
- 1.8V、3.3V、5.0V の制御ロジックをサポート
- 3.3V の単一電源電圧
- アクティブ時 45μA、スタンバイ時 6μA の低消費電流
- 電源レールが消失 (V_{CC} = 0V) した場合の電流リークを防止する I_{OFF} 保護
- 3kV HBM、1kV CDM の ESD 耐圧
- ウェットプル・フランク付きの 42 ピン、3.5mm×9mm、0.5mm ピッチの WQFN パッケージで供給

2 アプリケーション

- 先進運転支援システム (ADAS)
- 車載インフォテインメントおよびクラスター
- 後部座席用エンターテインメント
- 車載用ヘッド・ユニット
- 航空宇宙 / 防衛

3 概要

TS3DV642-Q1 は、マルチプレクサ / デマルチプレクサ構成で最高 6Gbps のデータ・レートの各種高速差動インターフェイスに使用できる、高速・双方向のパッシブ・アナログ・スイッチです。HDMI 1.4/2.0、DisplayPort 1.4、Mipi DPHY / CPHY DSI / CSI-2 など、多くのアプリケーションに適しています。TS3DV642-Q1 は差動信号とシングルエンド信号の両方に対応できるため、事実上ほとんどの標準および非標準のインターフェイスとの互換性を持ちます。TS3DV642-Q1 の動的特性が可能にした高速スイッチングでは、信号アイ・ダイアグラムの減衰は最小化され、発生するジッタは非常に低いレベルに抑えられます。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。このデバイスは、0V~3.6V の範囲の同相電圧 (CMV) を含む差動信号をサポートしています。また、0V~5.5V のシングルエンド CMOS 信号もサポートしています。

TS3DV642-Q1 は、アクティブ状態において 45μA という非常に低い消費電力を実現しています。本デバイスにはパワー・ダウン・モードも備わっており、このモードでは、すべてのチャンネルがハイ・インピーダンス状態となり、デバイスは最小の電力で動作します。

製品情報 ⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
TS3DV642-Q1	WQFN (42)	3.50mm x 9.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略使用事例

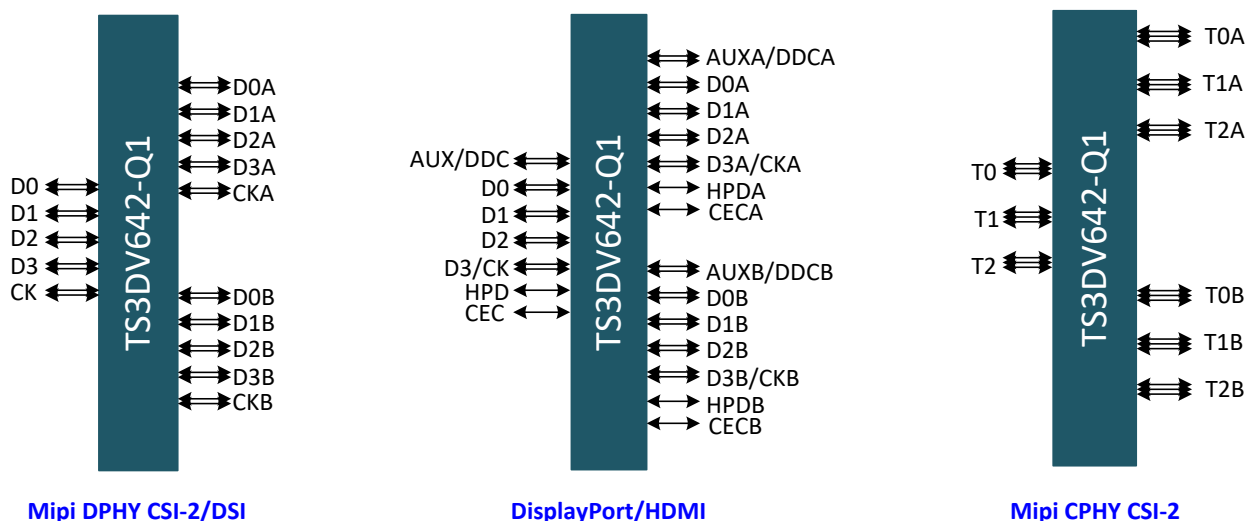


Table of Contents

1 特長	1	8.4 Device Functional Modes.....	14
2 アプリケーション	1	9 Application and Implementation	15
3 概要	1	9.1 Application Information.....	15
4 Revision History	2	9.2 Typical Application - Demultiplexing HDMI Signals..	15
5 Pin Configuration and Functions	3	9.3 Typical Application - Multiplexing HDMI Signals.....	17
6 Specifications	5	9.4 Systems Examples.....	18
6.1 Absolute Maximum Ratings	5	10 Power Supply Recommendations	20
6.2 ESD Ratings	5	11 Layout	21
6.3 Recommended Operating Conditions	5	11.1 Layout Guidelines.....	21
6.4 Thermal Information	5	11.2 Layout Example.....	22
6.5 Electrical Characteristics	6	12 Device and Documentation Support	23
6.6 High-Speed Performances	6	12.1 ドキュメントの更新通知を受け取る方法.....	23
6.7 Switching Characteristics	7	12.2 サポート・リソース.....	23
6.8 Typical Characteristics.....	8	12.3 Trademarks.....	23
7 Parameter Measurement Information	11	12.4 静電気放電に関する注意事項.....	23
8 Detailed Description	13	12.5 用語集.....	23
8.1 Overview.....	13	13 Mechanical, Packaging, and Orderable	
8.2 Functional Block Diagram.....	13	Information	23
8.3 Feature Description.....	13		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2020) to Revision A (May 2021)	Page
• デバイスのステータスを「量産データ」に更新.....	1

5 Pin Configuration and Functions

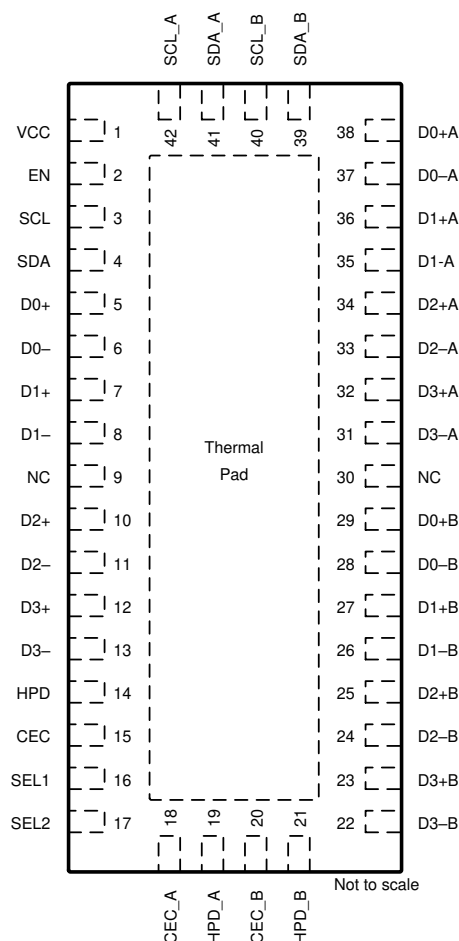


图 5-1. 42 Pin WQFN RUA Package with exposed thermal pad - top view - not to scale

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VCC	1	Power	Supply Voltage
SEL1	16	I	Select Input 1
SEL2	17	I	Select Input 2
EN	2	I	Device Enable
D0+A	38	I/O	Port A, Channel 0, +ve signal
D0-A	37	I/O	Port A, Channel 0, -ve signal
D1+A	36	I/O	Port A, Channel 1, +ve signal
D1-A	35	I/O	Port A, Channel 1, -ve signal
D2+A	34	I/O	Port A, Channel 2, +ve signal
D2-A	33	I/O	Port A, Channel 2, -ve signal
D3+A	32	I/O	Port A, Channel 3, +ve signal
D3-A	31	I/O	Port A, Channel 3, -ve signal
SCL_A	42	I/O	Port A, DDC Clock
SDA_A	41	I/O	Port A, DDC Data
HPD_A	19	I/O	Port A, Hot Plug Detects

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CEC_A	18	I/O	Port A, Consumer Electronics Control
D0+B	29	I/O	Port B, Channel 0, +ve signal
D0-B	28	I/O	Port B, Channel 0, -ve signal
D1+B	27	I/O	Port B, Channel 1, +ve signal
D1-B	26	I/O	Port B, Channel 1, -ve signal
D2+B	25	I/O	Port B, Channel 2, +ve signal
D2-B	24	I/O	Port B, Channel 2, -ve signal
D3+B	23	I/O	Port B, Channel 3, +ve signal
D3-B	22	I/O	Port B, Channel 3, -ve signal
SCL_B	40	I/O	Port B, DDC Clock
SDA_B	39	I/O	Port B, DDC Data
HPD_B	21	I/O	Port B, Hot Plug Detects
CEC_B	20	I/O	Port B, Consumer Electronics Control
D0+	5	I/O	Common Port, Channel 0, +ve signal
D0-	6	I/O	Common Port, Channel 0, -ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal
D1-	8	I/O	Common Port, Channel 1, -ve signal
D2+	10	I/O	Common Port, Channel 2, +ve signal
D2-	11	I/O	Common Port, Channel 2, -ve signal
D3+	12	I/O	Common Port, Channel 3, +ve signal
D3-	13	I/O	Common Port, Channel 3, -ve signal
SCL	3	I/O	Common Port, DDC Clock
SDA	4	I/O	Common Port, DDC Data
HPD	14	I/O	Common Port, Hot Plug Detects
CEC	15	I/O	Common Port, Consumer Electronics Control
NC	9, 30	NC	No Connect
GND	PowerPad	GND	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC} _{ABSMAX}	Supply voltage range	−0.5	5.5	V
V _{I/O-ABSMAX}	Analog voltage range ^{(2) (3) (4)}	−0.5	5.5	V
V _{IN-ABSMAX}	Digital input voltage range ^{(2) (3)}	−0.5	5.5	V
T _{jmax}	Maximum junction temperature	−40	125	°C
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, ⁽¹⁾	±3000
		Charged device model (CDM), per JEDEC specification JESD22-C101, ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	3.0	3.6	V
V _{I/O,CM}	Input/Output common mode voltage (data pins)	0	3.6	V
V _{I/O}	Input/Output voltage (data pins)	0	5.5	V
V _{IN}	Digital input voltage (control pins)	0	5.5	V
DR	Data rate for differential signals		6.0	Gbps
T _A	Operating ambient temperature	−40	105	°C
T _J	Operating junction temperature	−40	110	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *TI application report, Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3DV642-Q1	UNIT
		RUA	
		42 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	28.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	16.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	9.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	9.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
DC Characteristics							
R _{ON}	ON-state resistance	All data pins	V _{I/O} = 0 V, I _{I/O} = -10 mA		6.5	12	Ω
R _{ON,FLAT} ⁽³⁾	ON-state resistance flatness	All data pins	R _{ON} at V _{I/O} = 1.5 V minus R _{ON} at V _{I/O} = 0 V, I _{I/O} = -10 mA			0.6	Ω
			R _{ON} at V _{I/O} = 3.6 V minus R _{ON} at V _{I/O} = 0 V, I _{I/O} = -10 mA			2.0	Ω
I _{OFF}	Leakage under power off (failsafe current)	All data and control pins	VCC = 0 V, V _{I/O} or V _{IN} = 0 V to 5.5 V			±20	μA
Control Inputs (SEL1, SEL2, EN)							
V _{IH}	High-level input voltage for control pins	SEL1, SEL2, EN		1.4			V
V _{IL}	Low-level input voltage for control pins	SEL1, SEL2, EN				0.5	V
I _{IH}	Input high leakage current for control pins	SEL1, SEL2, EN	VCC = 3.6 V, V _{IN} = 5.5 V			±10	μA
I _{IL}	Input low leakage current for control pins	SEL1, SEL2, EN	VCC = 3.6 V, V _{IN} = GND			±10	μA
Power Supply							
I _{CC}	VCC supply current in active mode	EN = H			45		μA
I _{CC_PD}	VCC supply current in power-down mode	EN = L			6		μA

(1) V_I, V_O, I_I, and I_O refer to data I/O pins, V_{IN} refers to the control inputs.

(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.

(3) R_{ON,FLAT} is the difference of R_{ON} in a given channel at specified voltages.

6.6 High-Speed Performances

Over recommended operation free-air temperature range, V_{DD} = 3.3V ± 0.3V (unless otherwise noted). For all data pins. R_L = 50 Ω where applicable.

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
BW	Differential Bandwidth		-3 dB from DC		5.8		GHz
IL	Differential insertion loss		DC		-0.5		dB
			1.7 GHz		-1.0		dB
			2.7 GHz		-1.4		dB
			3.0 GHz		-1.6		dB
RL	Differential return loss		DC		-24		dB
			1.7 GHz		-21		dB
			2.7 GHz		-19		dB
			3.0 GHz		-17		dB
Xtalk	Differential crosstalk		DC		-72		dB
			1.7 GHz		-35		dB
			2.7 GHz		-30		dB
			3.0 GHz		-27	-	dB
OISO	Differential off isolation		DC		-82		dB
			1.7 GHz		-20		dB
			2.7 GHz		-16		dB
			3.0 GHz		-16		dB

(1) All Typical Values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.

6.7 Switching Characteristics

over recommended operation free-air temperature range, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted). For all data pins.

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation Delay	All I/O			66		ps
$t_{SK,INTER}$	Inter-pair Skew	D0-3	The maximum difference in differential prop delay between data channels; 1.7 GHz; at nominal corner		10		ps
$t_{SK,INTRA}$	Intra-pair Skew	D0-3	The maximum difference in prop delay between +ve and -ve signals of each channel (for all channels); at 1.7 GHz; at nominal corner		8		ps
t_{ON} ⁽²⁾	Switch turn-on time	All I/O	When EN goes from L to H			5	μs
t_{SWITCH} ⁽³⁾	Switching time between channels	All I/O	When SEL pins toggles			5	μs

(1) All typical values are at $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(2) t_{ON} is the time it takes the output to recover within 95% of final value after enabling switches

(3) t_{SWITCH} is the time it takes for the output to recover within 95% of final value after the state is changed

6.8 Typical Characteristics

Figure 6-1, Figure 6-2, Figure 6-3 and Figure 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

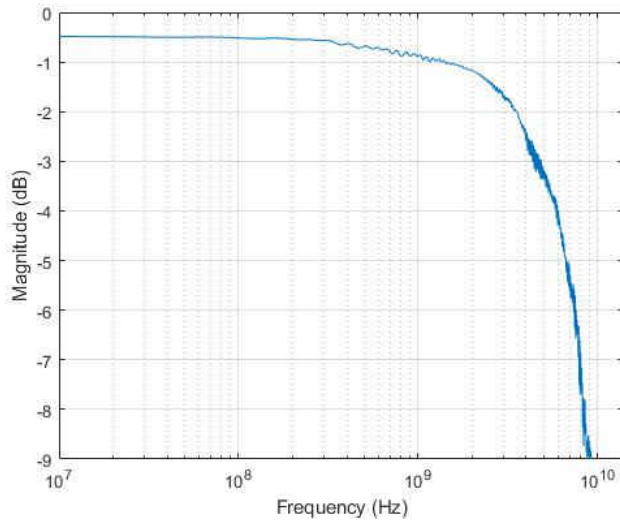


Figure 6-1. Typical differential gain vs frequency

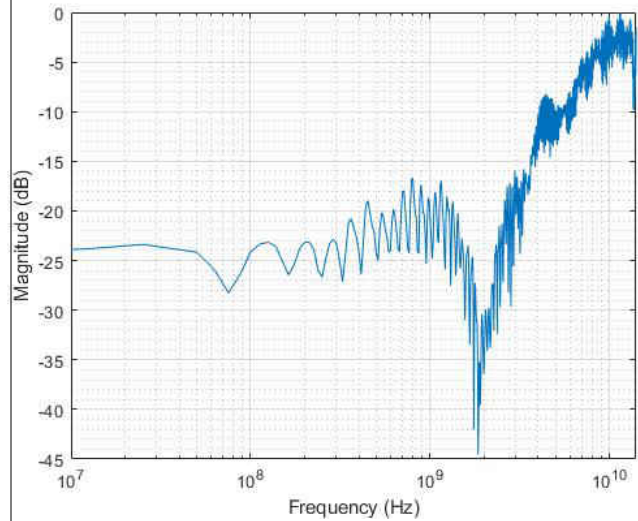


Figure 6-2. Typical return loss vs frequency

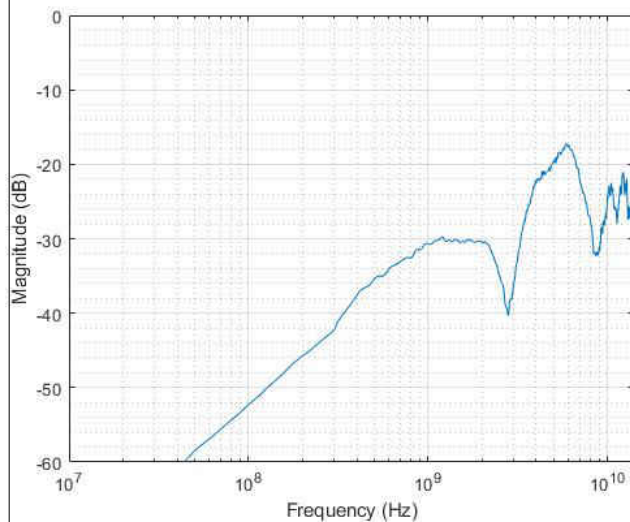


Figure 6-3. Typical differential cross-talk vs frequency

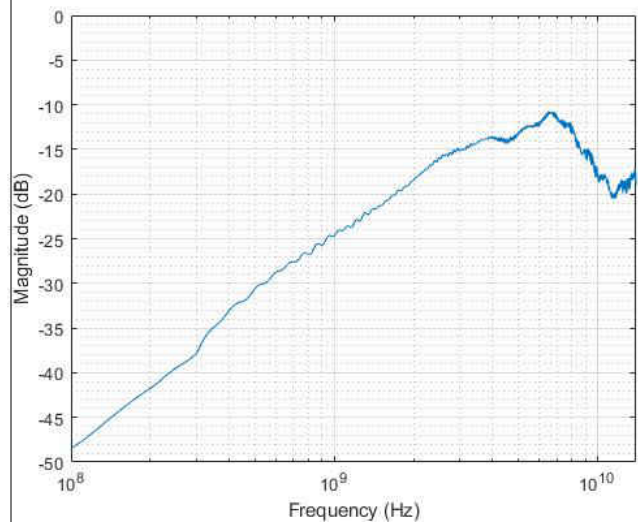


Figure 6-4. Typical differential off-isolation vs frequency

6.8 Typical Characteristics

Figure 6-1, Figure 6-2, Figure 6-3 and Figure 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

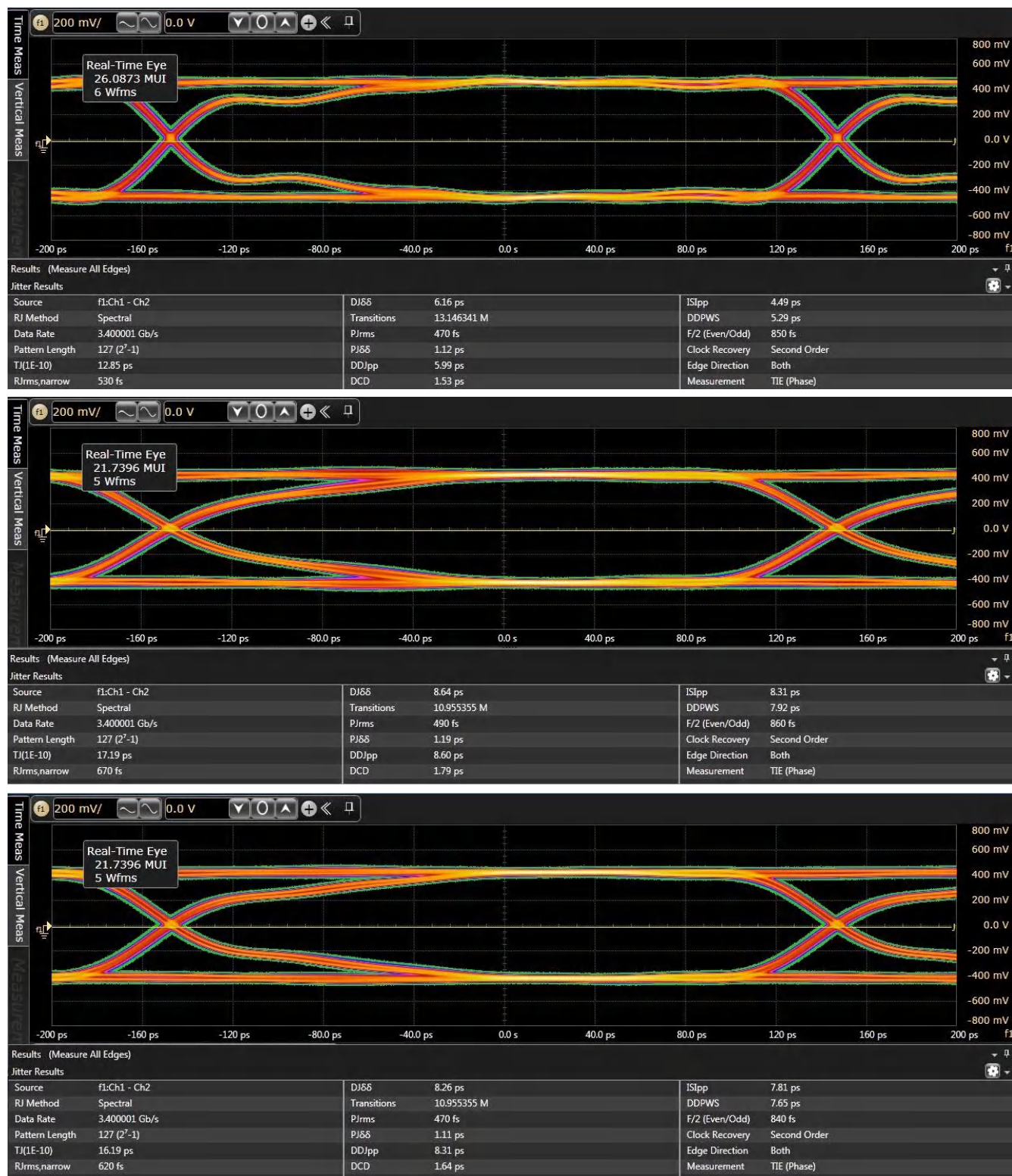


Figure 6-5. Typical eye diagrams at 3.4 Gbps. Top: baseline calibration setup. Middle: through TS3DV642-Q1 Port A. Bottom: through TS3DV642-Q1 Port B.

6.8 Typical Characteristics

Figure 6-1, Figure 6-2, Figure 6-3 and Figure 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

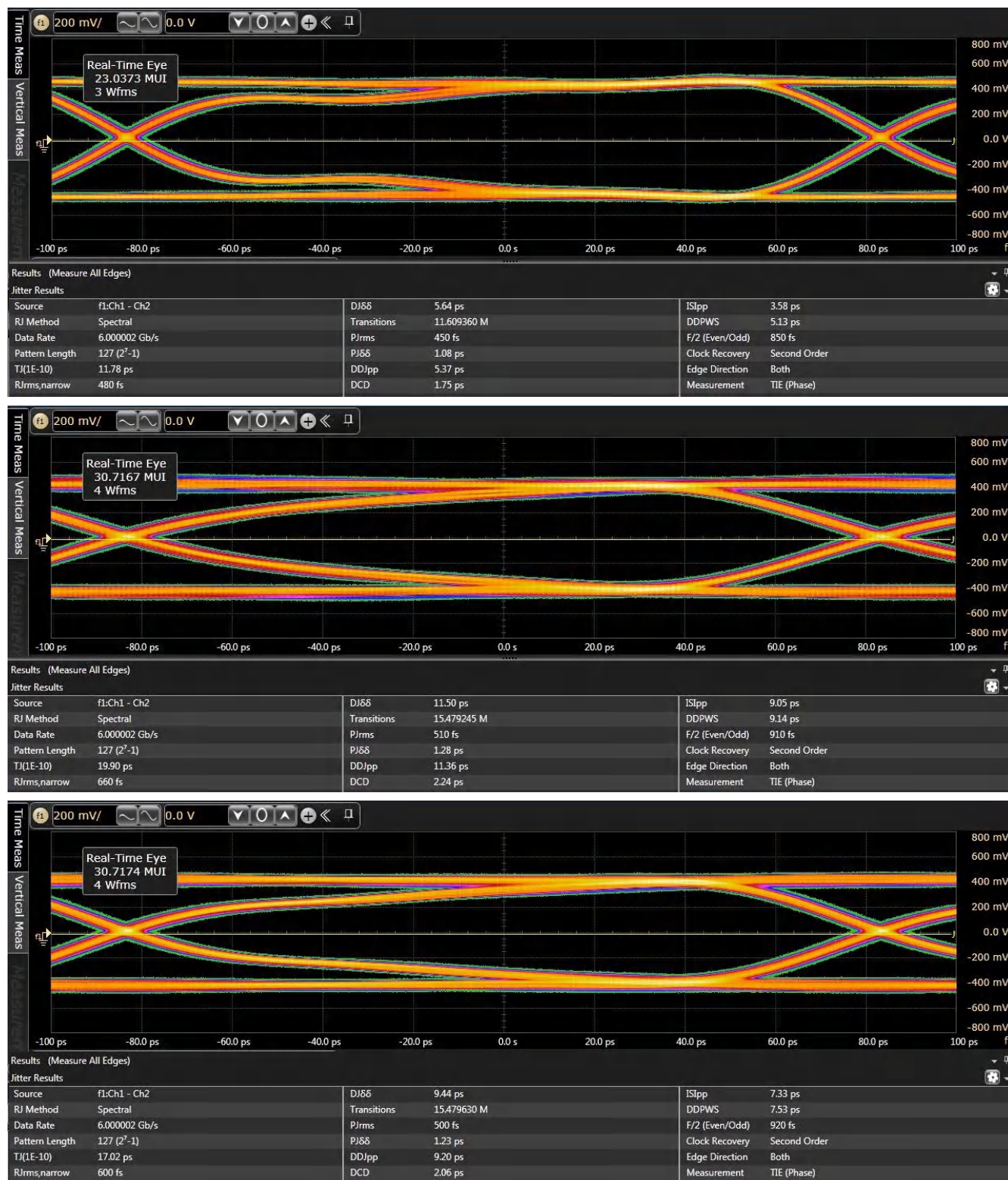
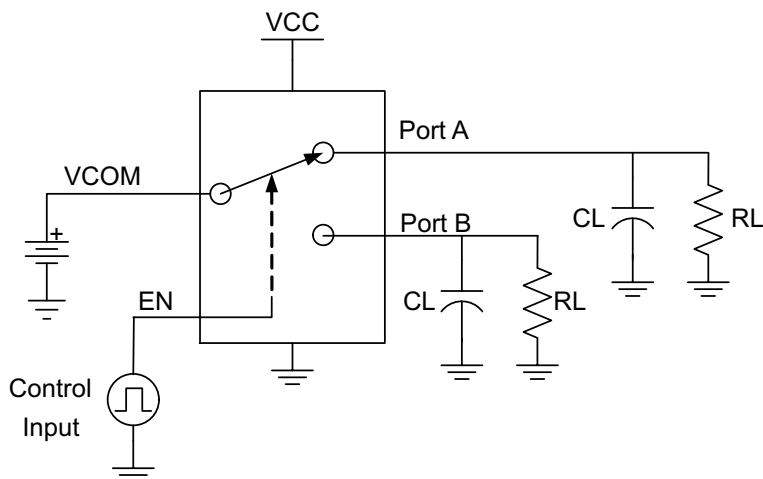


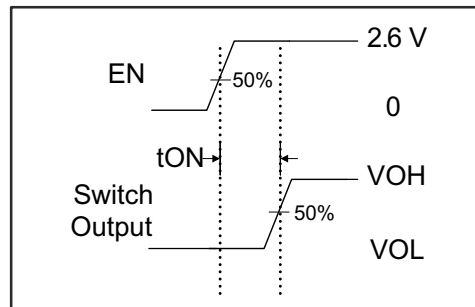
Figure 6-6. Typical eye diagrams at 6.0 Gbps. Top: baseline calibration setup. Middle: through TS3DV642-Q1 Port A. Bottom: through TS3DV642-Q1 Port B.

7 Parameter Measurement Information

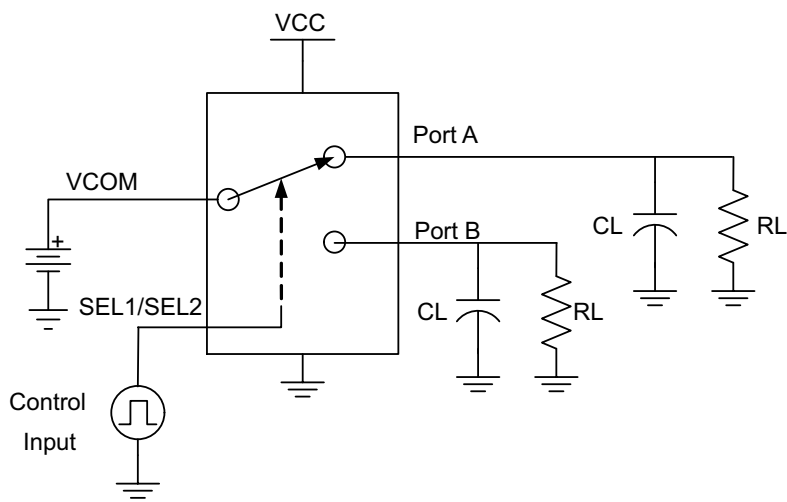


RL	CL	VCOM
50 Ω	4 pF	VCC

*CL includes probe, cable, and board capacitance

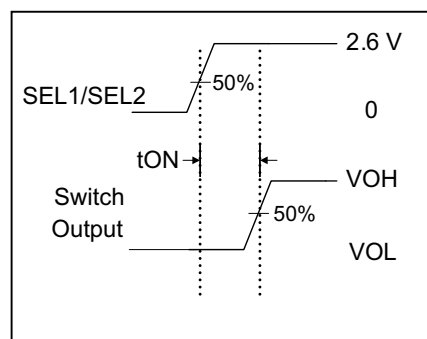


7-1. Switch Turn-On Time (t_{ON})

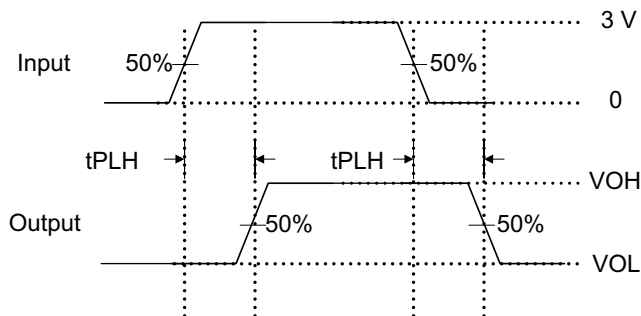


RL	CL	VCOM
50 Ω	4 pF	VCC

*CL includes probe, cable, and board capacitance

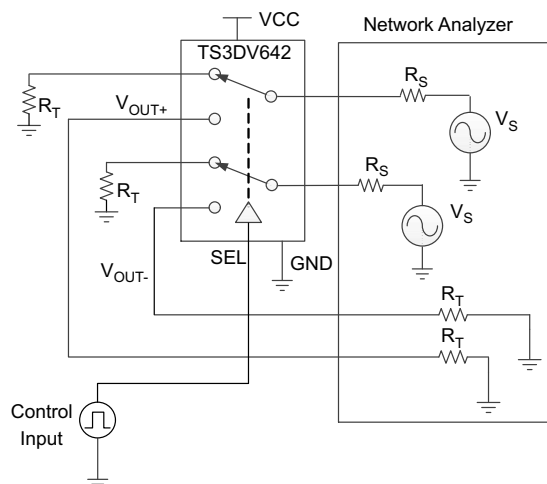


7-2. Switching Time Between Channels (t_{SWITCH})



$$t_{pd} = (t_{PLH} + t_{PLH}) / 2$$

7-3. Propagation Delay (t_{pd})

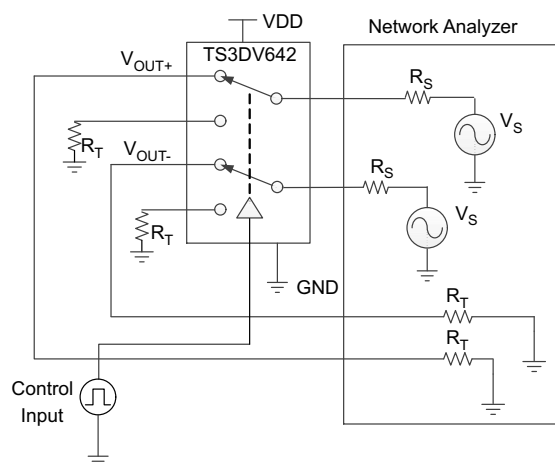


Channel OFF

SEL = H or L
 $R_S = R_T = 50\Omega$

$V_S = -10\text{dBm}$ (200mV at 50Ω Load)
 $V_{\text{DC_BIAS}} = 1\text{ V}$

Figure 7-4. Differential Off-Isolation and Xtalk



Channel ON

SEL = H or L
 $R_S = R_T = 50\Omega$

$V_S = -10\text{dBm}$ (200mV at 50Ω Load)
 $V_{\text{DC_BIAS}} = 1\text{ V}$

Figure 7-5. Differential Bandwidth (BW)

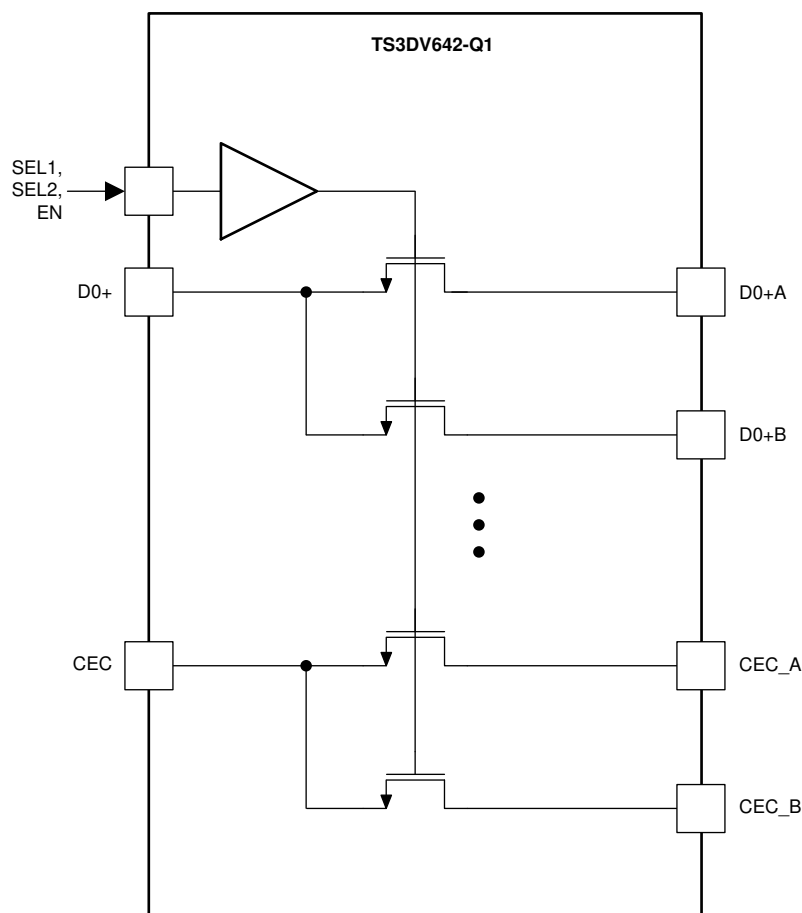
8 Detailed Description

8.1 Overview

The TS3DV642-Q1 is a 6 differential channel or 12 single ended channel bidirectional multiplexer/demultiplexer. It offers low on-state resistance as well as low datapath parasitics which allows it to achieve a high bandwidth. The TS3DV642-Q1 is a passive mux that is recommended for data rates up to 6 Gbps, however the device can be used for interfaces with higher data rates depending on how much loss is permissible for the mux from the overall electrical link budget. The device provides the high bandwidth necessary for many interfaces to handle differential and as well as single ended signals. The device supports differential signaling with common mode voltage range (CMV) of 0 to 3.6 V and 0 - 5.5 V CMOS signals.

The TS3DV642-Q1 has total 6 differential channels. All these channels are functionally equivalent and provides almost identical electrical performance. The channels can be used in an arbitrary fashion for differential and single ended signals in any order.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3DV642-Q1 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. TS3DV642-Q1 has 6 differential channel or 12 single ended channel bidirectional switches with a high bandwidth. TS3DV642-Q1 uses an extremely low power technology and uses only 45 μA I_{CC} in active mode. The device has integrated ESD that can support up to 3-kV Human-Body Model (HBM) and 1-kV Charge Device Model (CDM). TS3DV642-Q1 is offered in a 42-pin QFN package (9 mm x 3.5 mm) with 0.5 mm pitch. The device can support analog I/O signal in 0 to 5.5 V range. TS3DV642-Q1 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature

prevents leakage current in the device. The TS3DV642-Q1 is not designed for passing signals with negative swings.

8.4 Device Functional Modes

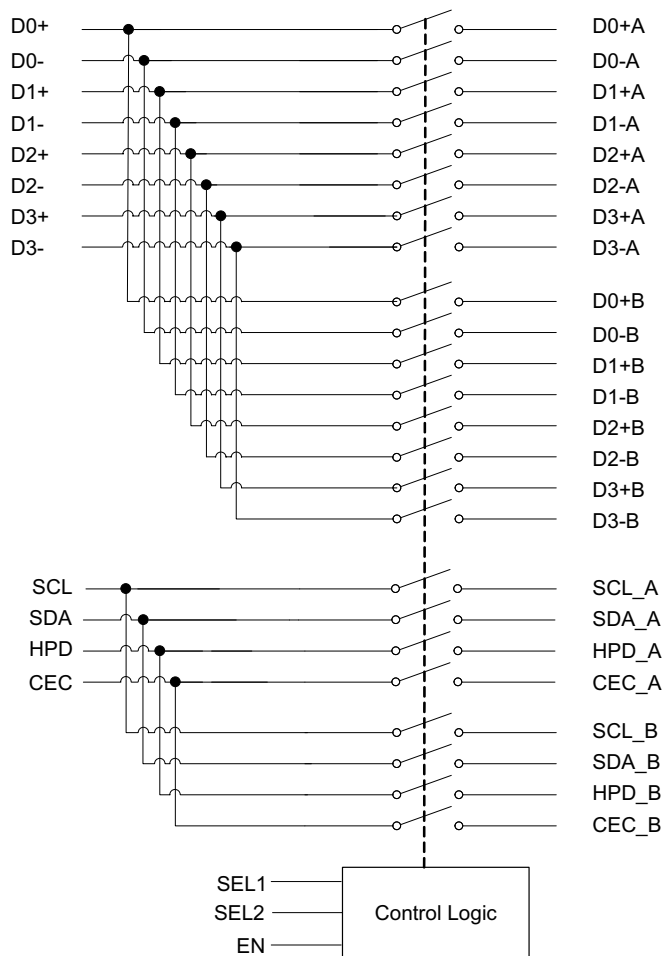


图 8-1. Logic Diagram

表 8-1 lists the device functions for the TS3DV642-Q1 device.

表 8-1. Functional Table

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	Channel D0+/D0- to D0+A/D0-A is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	L	H	Channel D0+/D0- to D0+B/D0-B is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	H	L	All A channels are enabled. All B channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3DV642-Q1 is an analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 6 Gbps. The device also works for single ended signals. The TS3DV642-Q1 supports differential signaling with common mode voltage range (CMV) of 0 to 3.6 V and with differential amplitude up to 1800 mVpp, and single ended CMOS signaling with swing limited to 0 to 5.5 V. TS3DV642-Q1 can be used as mux or demux switch for:

- HDMI 1.4 and HDMI 2.0 - up to 6 Gbps per channel
- DisplayPort (DP) for RBR, HBR, and HBR-2 data rates - up to 5.4 Gbps per lane
- DP++
- Mipi DPHY interfaces such as DSI and CSI-2 - up to 4.5 Gbps per lane
- Mipi CPHY based CSI-2
- LVDS

6 Channels of the TS3DV642-Q1 are functionally equivalent and can be used in an arbitrary fashion for differential and single ended signals in any order. For example in Mipi DPHY applications any of the 6 differential channels can be used for clock signals. For Mipi CPHY applications the data pins can be grouped any order to form trio signals. For HDMI application, while TS3DV642-Q1 data signal pins are marked for specific HDMI use, the main-link data, main-link clock, DDC, HPD, CEC can be assigned in any order if required.

9.2 Typical Application - Demultiplexing HDMI Signals

The TS3DV642-Q1 can be used to mux HDMI signals. [Figure 9-1](#) shows use case where TS3DV642-Q1 switches HDMI signals from a source to either to an external connector or to an SOC. This section provides detailed design implementation for a HDMI application where TS3DV642-Q1 provides 1:2 multiplexing function.

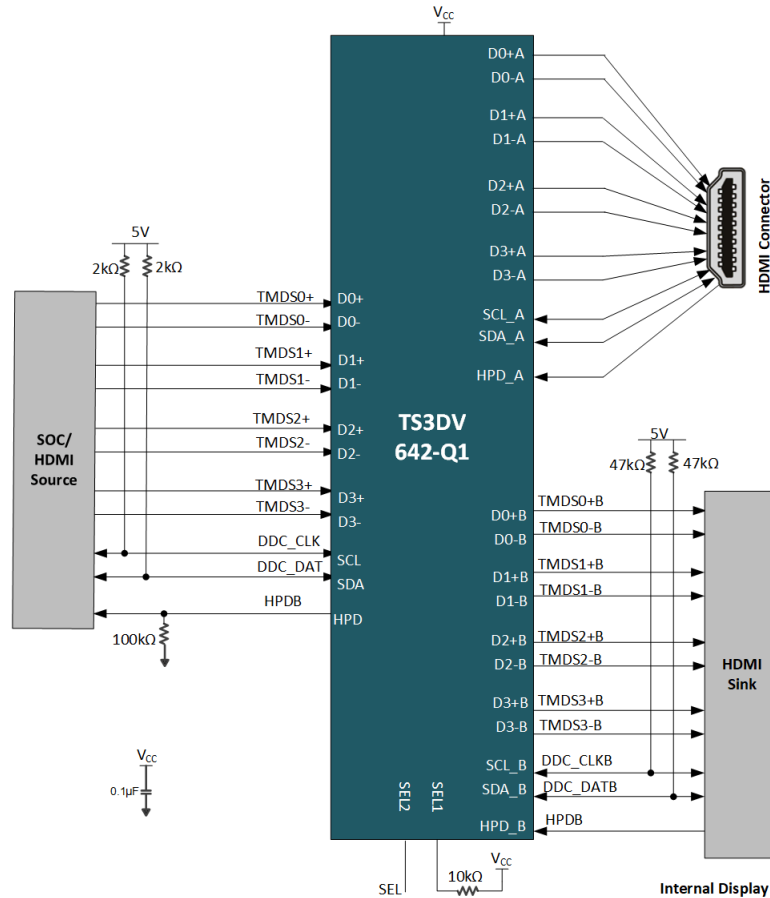


图 9-1. Demultiplexing HDMI signals - schematic

9.2.1 Design Requirements

表 9-1. Design Parameters for HDMI Application

Design parameter	Example value
V _{CC}	3.0 V to 3.6 V
VCC decoupling capacitor	0.1 μF
DDC Pull-up resistors on sink side (only for internal display path)	47 kΩ to 5 V
DDC Pull-up resistors on source side	2 kΩ to 5 V
HPD pull-down resistor on source side	100 kΩ to GND
Pull-up / Pull-down resistors for SEL1 / SEL2 pins	10 kΩ

9.2.2 Detailed Design Procedure

The TS3DV642-Q1 is designed to operate with 3.0 V to 3.6 V power supply. Decoupling capacitors may be used to reduce noise and improve power supply integrity. Pull-up resistors to 5 V must be placed on the sink side DDC clock and data lines according to the HDMI standard.

9.2.3 Application Curves

An HDMI connector functioning as a source is subject to HDMI source compliance test. This section provides application curves related to HDMI 1.4 and 2.0 source compliance for jitter and eye mask respectively.

图 9-2 shows HDMI 1.4 compliance jitter performance at 3.0 Gbps data rate. For brevity only one of the three data channels and Port A illustrated. Other channels have similar performances. As illustration shows the TS3DV642-Q1 adds minimal jitter to the link - 89 mTbit through mux vs 73 mTbit without mux.

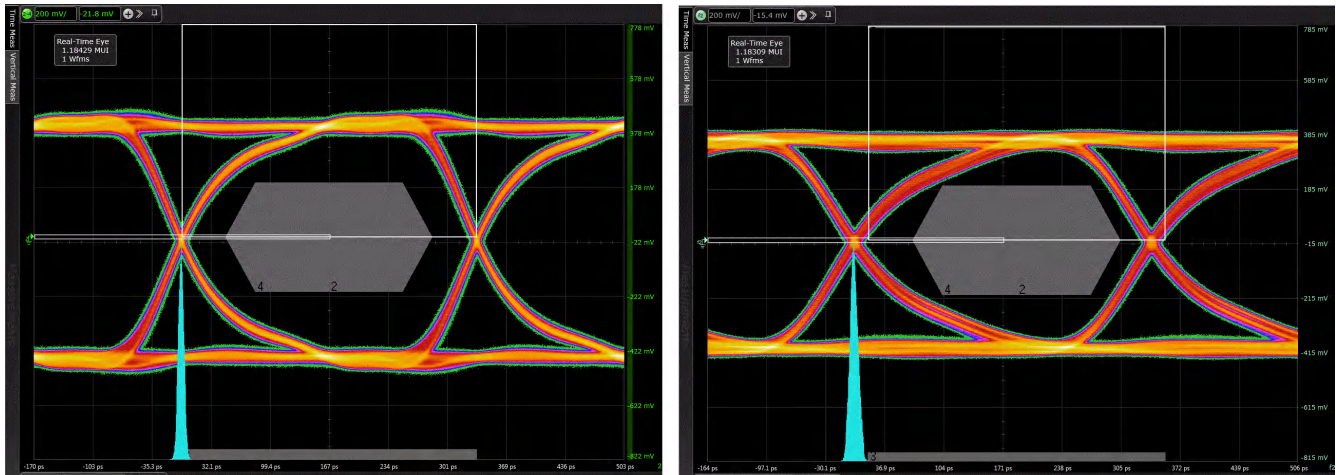


Figure 9-2. HDMI 1.4 compliance at 3.0 Gbps - jitter performance. Left: with no DUT in the path. Right: TS3DV642-Q1 in the path

Figure 9-3 shows HDMI 2.0 eye mask performance at 6.0 Gbps data rate. For brevity only one of the three data channels and Port A is illustrated. Eye masks are for worst case positive skew. Other channels, and cases have similar performances.

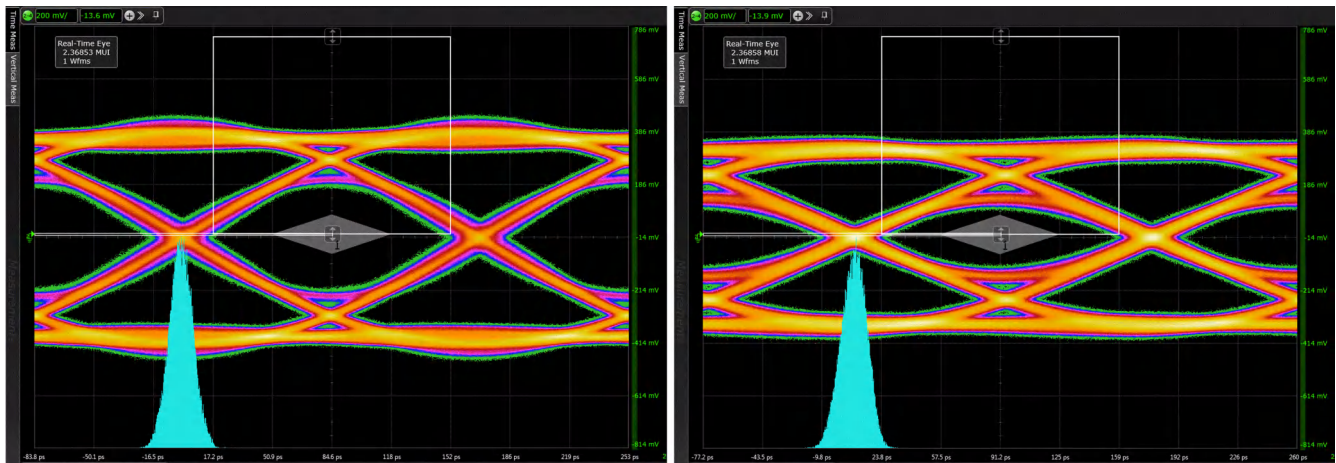


Figure 9-3. HDMI 2.0 compliance at 6.0 Gbps - eye mask at TP2_EQ. Left - with no DUT in the path. Right - TS3DV642-Q1 in the path

9.3 Typical Application - Multiplexing HDMI Signals

Figure 9-4 shows a 2:1 multiplexing use case where TS3DV642-Q1 is being used to choose HDMI signals from either an external HDMI connector or an internal HDMI source to connect to a HDMI sink device. Note HDMI connector in this use case represents a Sink port and is subject to HDMI sink compliance requirements. Part of the compliance requirements the mainlink data and clock signals needs to have 50Ω termination from each pin to 3.3 V supply with certain tolerance depending on data rate. Note the TS3DV642-Q1 adds a series resistance (R_{ON}) to the mainlink sink termination. To account for the additional series resistance it is recommended that sink internal termination resistance is reduce by equal amount. Where such provisioning is not possible, alternate solution is to install external resistors on board from each pin to VCC as shown in Figure 9-4. In applications where a retimer is used behind a HDMI connector in sink application, this series resistance provisioning is not required as retimer termination is tested for HDMI compliance.

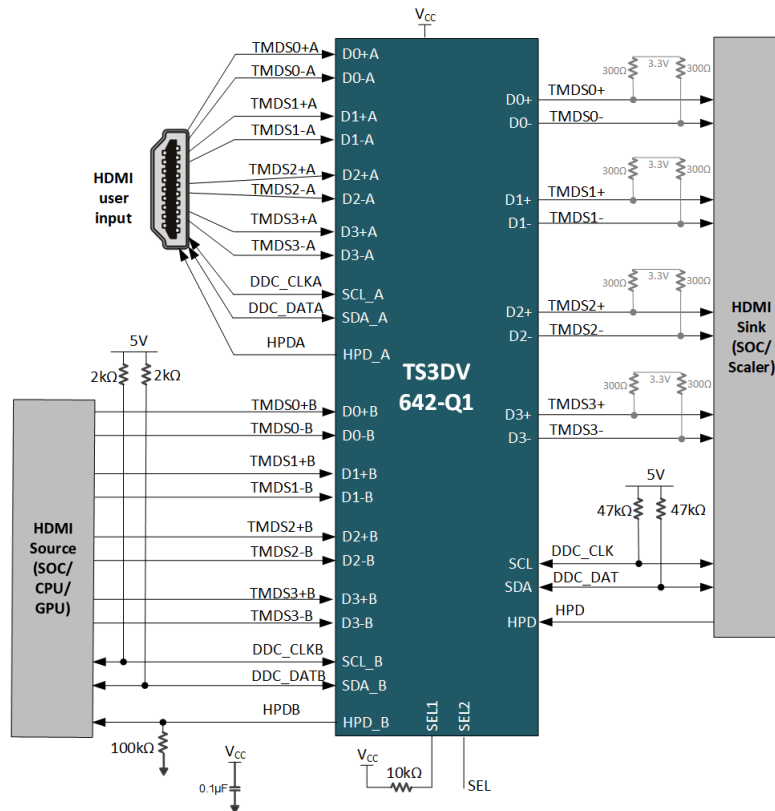
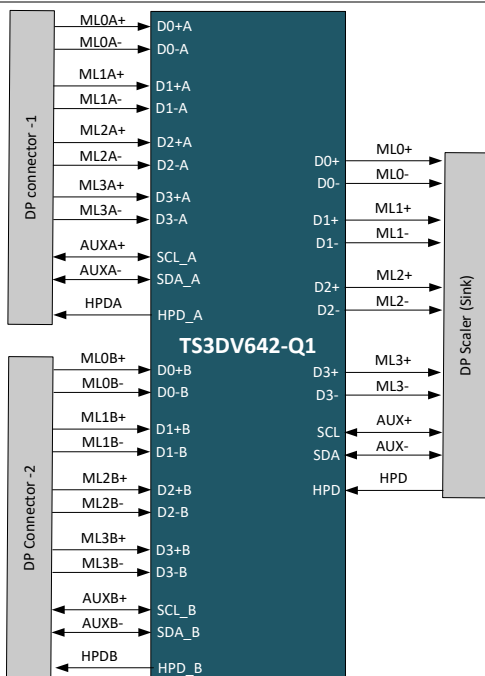


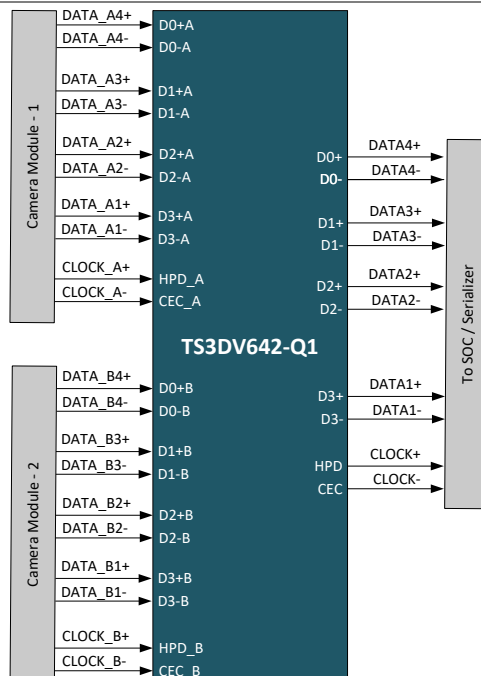
图 9-4. Multiplexing HDMI signals - schematic

9.4 Systems Examples

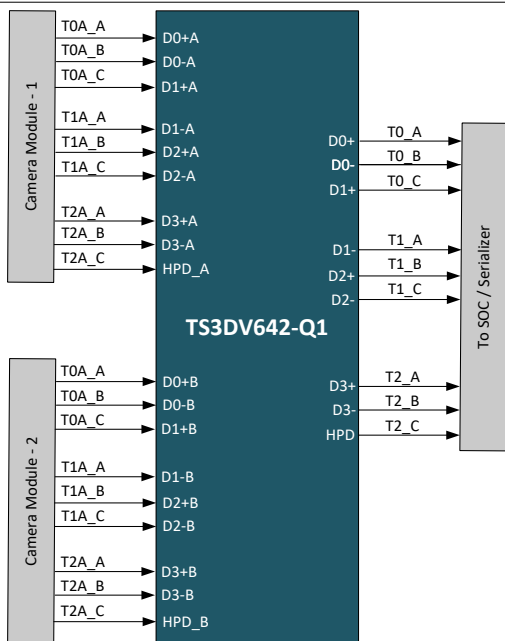
TS3DV642-Q1 can be used for many high speed interfaces. 图 9-5, 图 9-6, 图 9-7, and 图 9-8 show some system level examples for select few interfaces. Note for brevity exact detail design implementation is not shown.



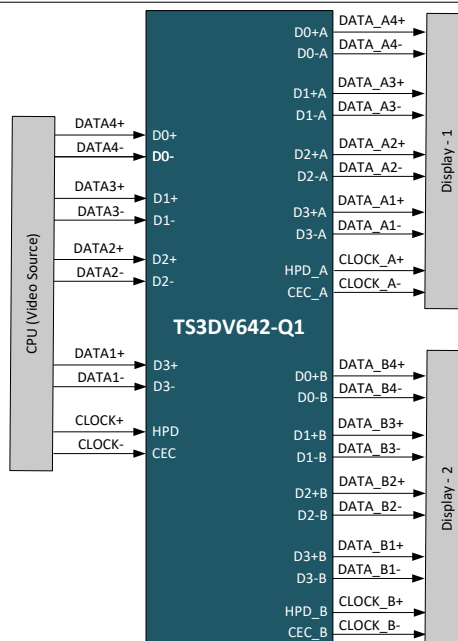
9-5. DisplayPort 2:1 switching



9-6. Mipi DPHY based CSI-2 switching



9-7. Mipi CPHY based CSI-2 switching



9-8. Mipi DPHY based DSI switching

10 Power Supply Recommendations

V_{CC} should be in the range of 3.0 V to 3.6 V. Voltage levels above those listed in the Absolute Ratings table should not be used. Decoupling capacitor(s) such as 0.1 μ F may be used to reduce noise and improve power supply integrity. There are no power sequence requirements for the TS3DV642-Q1.

11 Layout

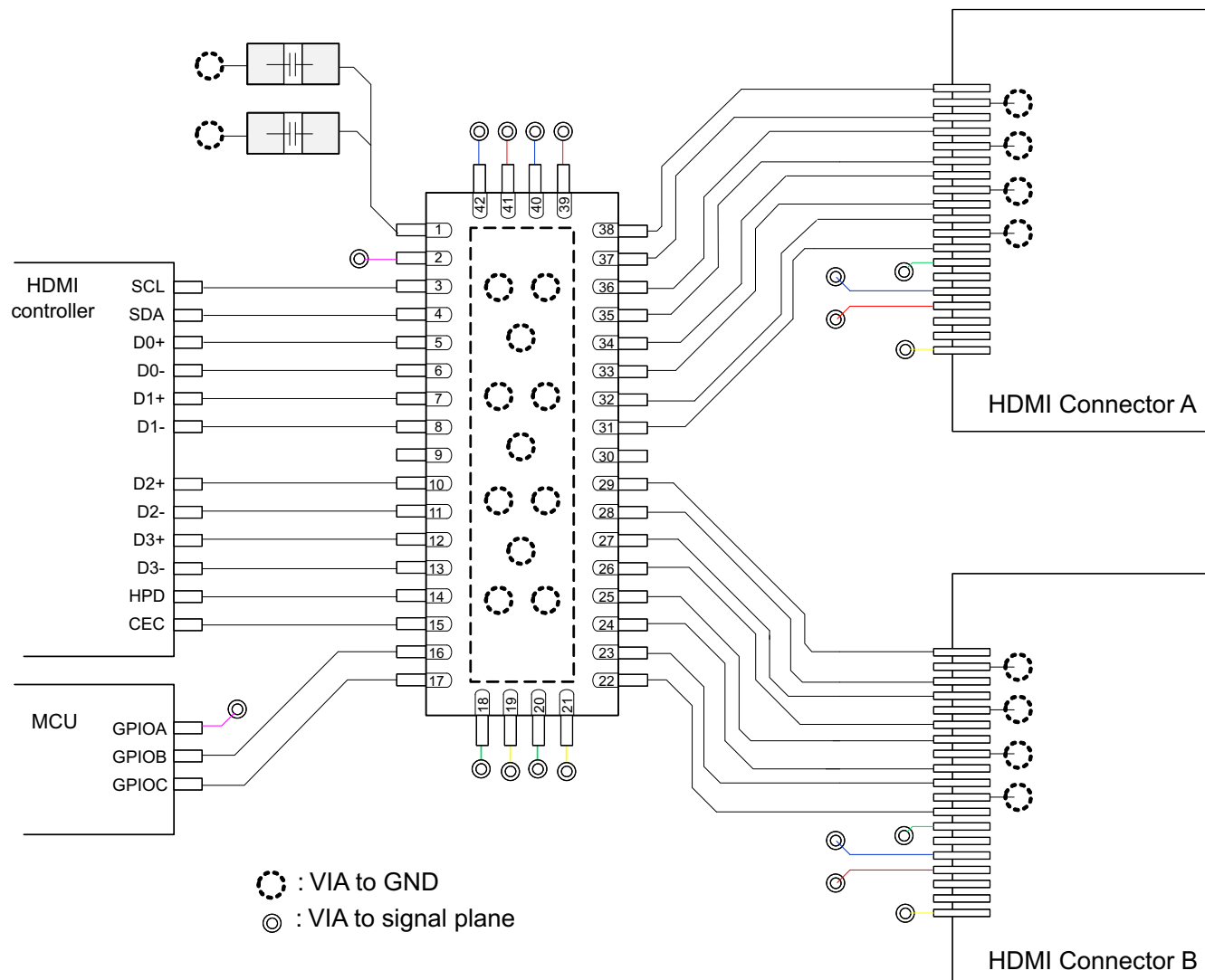
11.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed-circuit board layout guidelines are recommended:

- Decoupling capacitors should be used between power supply pin and ground pin to ensure low impedance to reduce noise. To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- ESD and EMI protection devices (if used) should be placed as close as possible to the connector.
- Short trace lengths should be used to avoid excessive loading.
- To minimize the effects of crosstalk on adjacent traces, keep the traces at least two times the trace width apart.
- Separate high-speed signals from low-speed signals and digital from analog signals.
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- The high-speed differential signal traces should be routed parallel to each other as much as possible. The traces are recommended to be symmetrical.
- A solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

11.2 Layout Example

TS3DV642-Q1 application with a single controller interfacing with two HDMI connectors.



11-1. Layout Example

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://www.ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

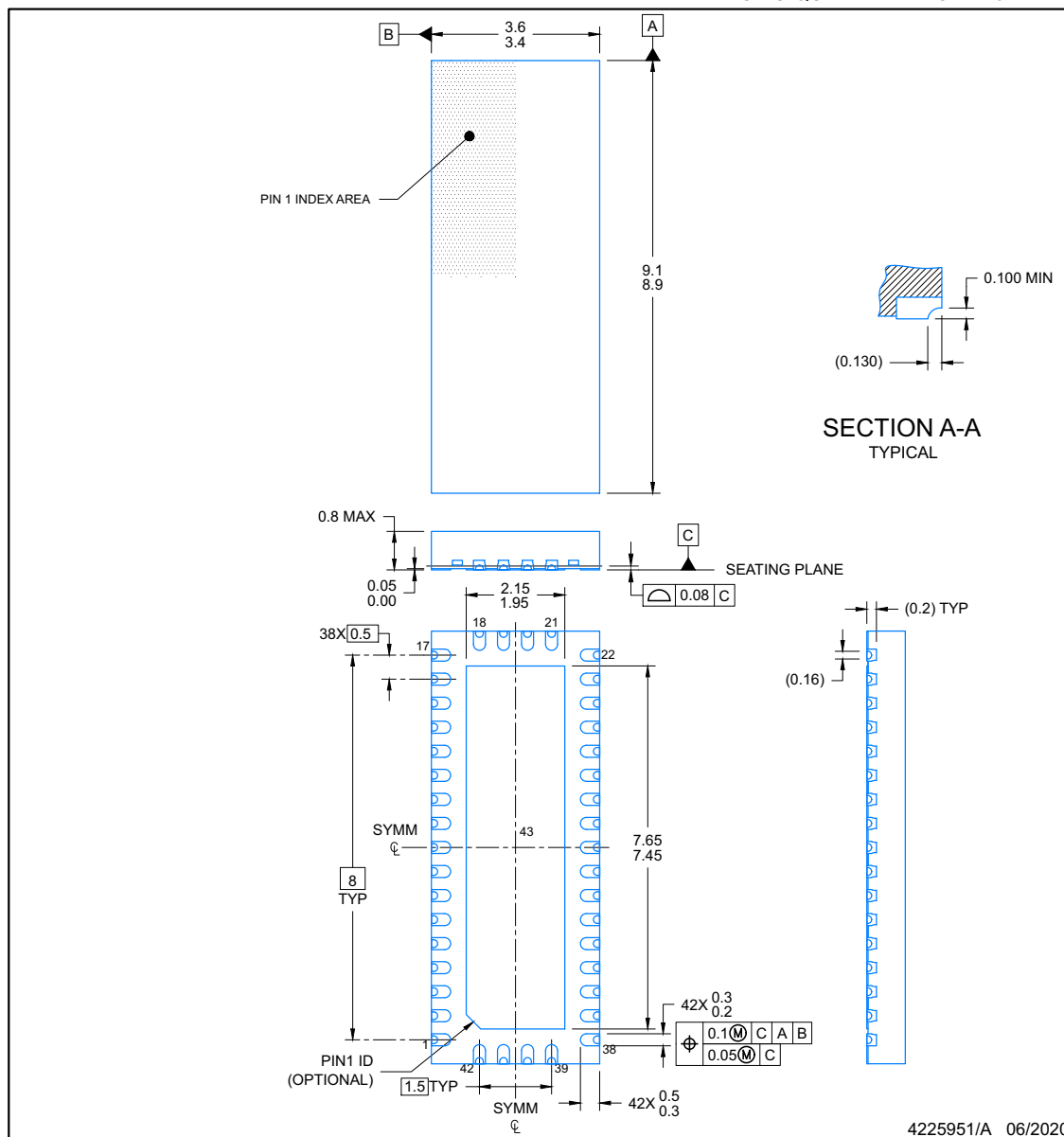
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RUA0042B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

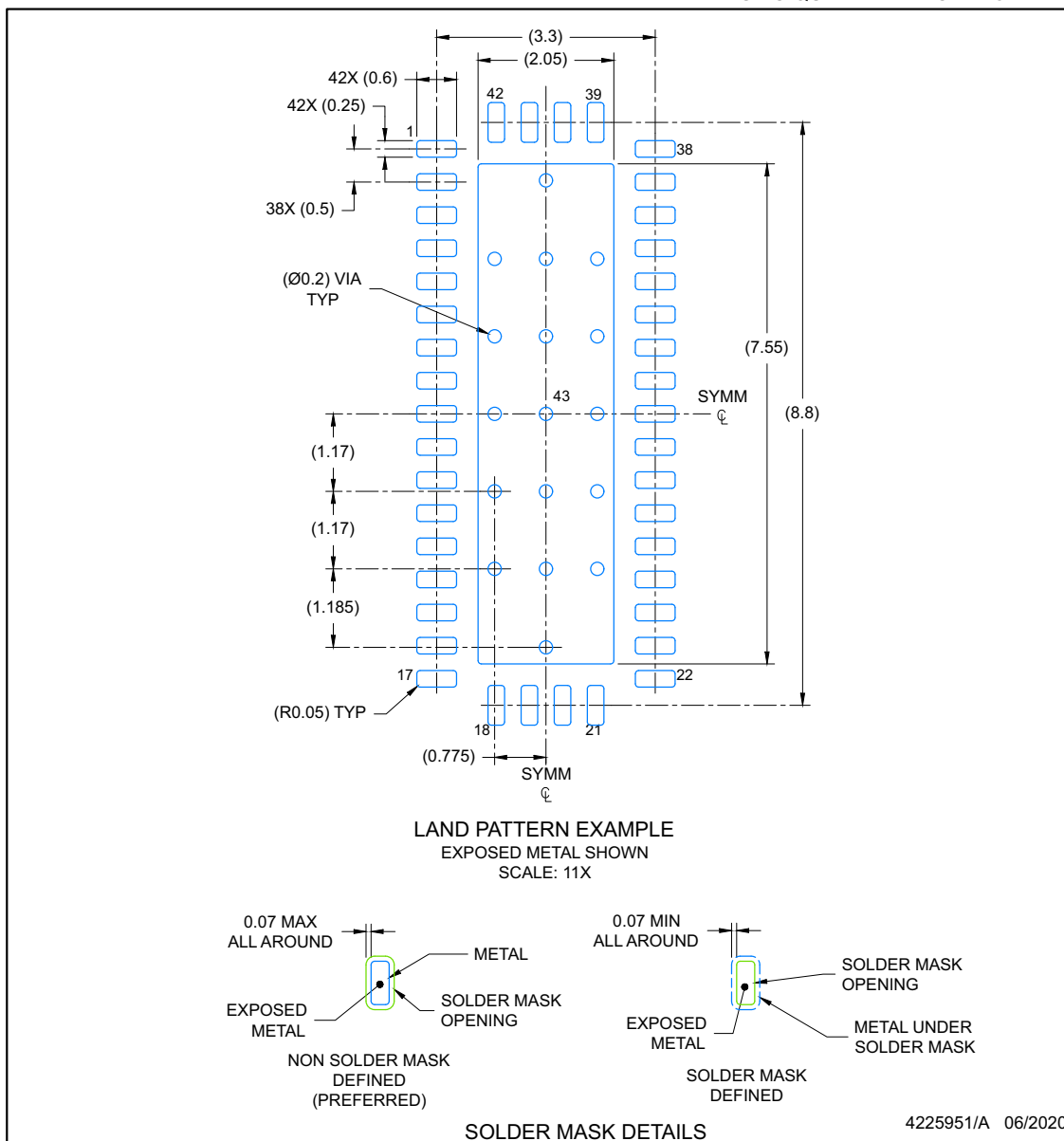
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

RUA0042B

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

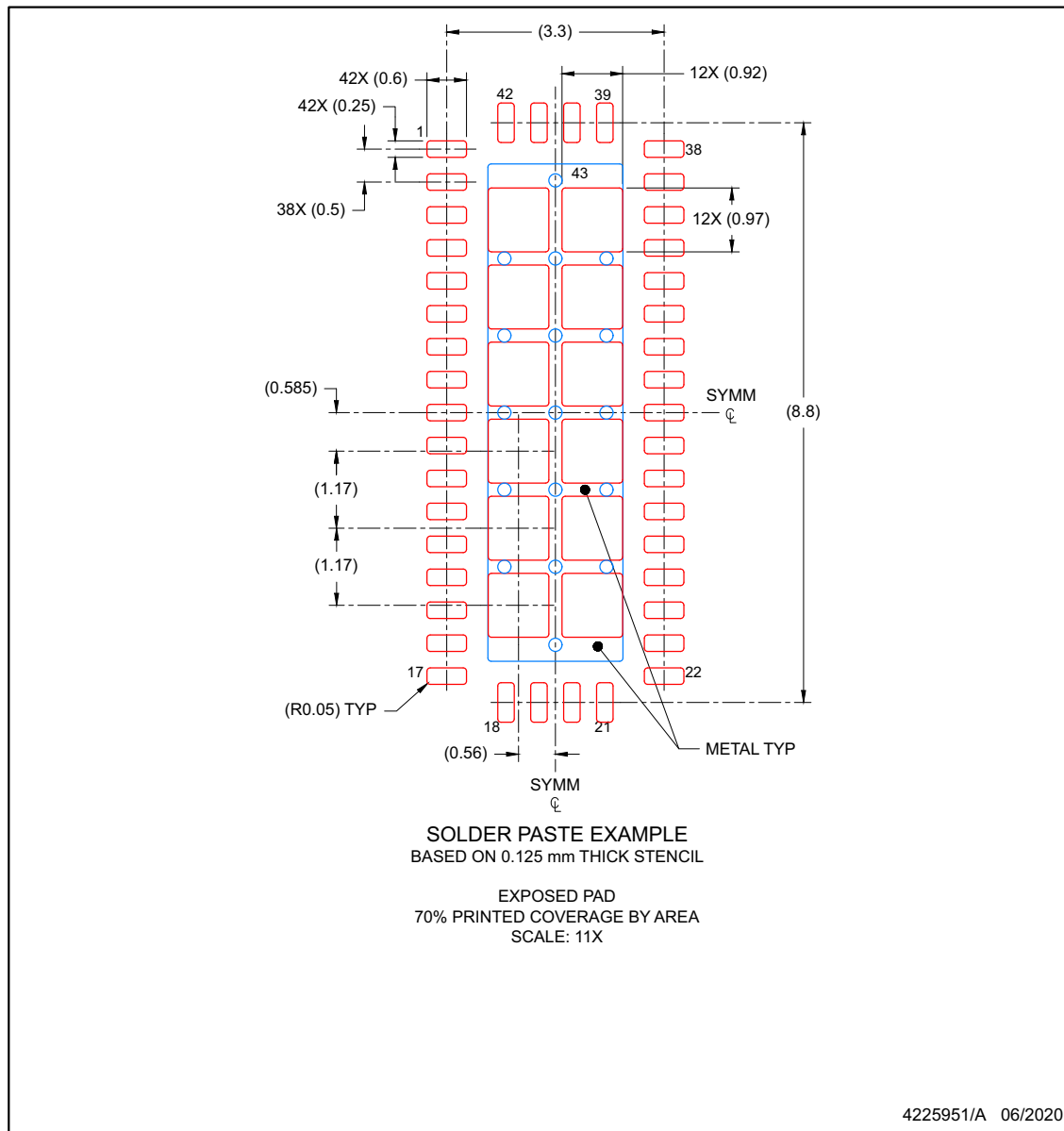
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

RUA0042B

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DV642RUARQ1	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q
TS3DV642RUARQ1.A	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q
TS3DV642RUATQ1	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q
TS3DV642RUATQ1.A	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS3DV642-Q1 :

- Catalog : [TS3DV642](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV642RUARQ1	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3DV642RUATQ1	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV642RUARQ1	WQFN	RUA	42	3000	367.0	367.0	35.0
TS3DV642RUATQ1	WQFN	RUA	42	250	210.0	185.0	35.0

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月