

12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications

Check for Samples: [TS3DDR3812](#)

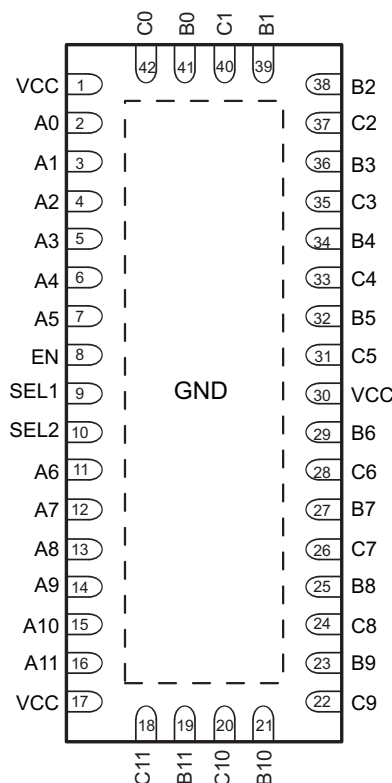
FEATURES

- Compatible with DDR3 SDRAM Standard (JESD79-3D)
- Wide Bandwidth of 1.675 GHz
- Low Propagation Delay ($t_{pd} = 40$ ps Typ)
- Low Bit-to-Bit Skew ($t_{sk(o)} = 6$ ps Typ)
- Low and Flat ON-State Resistance ($r_{ON} = 8 \Omega$ Typ)
- Low Input/Output Capacitance ($C_{ON} = 5.6$ pF Typ)
- Low Crosstalk ($X_{TALK} = -43$ dB, Typ at 250 MHz)
- V_{CC} Operating Range from 3 V to 3.6 V
- Rail-to-Rail Switching on Data I/O Ports (0 to V_{CC})
- Separate Switch Control Logic for Upper and Lower 6-Channels
- Dedicated Enable Logic Supports Hi-Z Mode
- I_{OFF} Protection Prevents Current Leakage in Powered Down State ($V_{CC} = 0$ V)
- ESD Performance Tested Per JESD22
 - 2000 V Human Body Model (A114B, Class II)
 - 1000 V Charged Device Model (C101)
- 42-pin RUA Package (9 × 3.5 mm, 0.5 mm Pitch)

APPLICATIONS

- DDR3 Signal Switching
- DIMM Modules
- Notebook/Desktop PCs
- Servers

**Figure 1. RUA PACKAGE
(TOP VIEW)**



DESCRIPTION

The TS3DDR3812 is a 12-channel, 1:2 multiplexer/demultiplexer switch designed for DDR3 applications. It operates from a 3 to 3.6 V supply and offers low and flat ON-state resistance as well as low I/O capacitance which allow it to achieve a typical bandwidth of 1.675 GHz.

Channels A_0 through A_{11} are divided into two banks of six bits and are independently controlled via two digital inputs called SEL1 and SEL2. These select inputs control the switch position of each 6-bit DDR3 source and allow them to be routed to one of two end-points. Alternatively, the switch can be used to connect a single endpoint to one of two 6-bit DDR3 sources. For switching 12-bit DDR3 sources, simply connect SEL1 and SEL2 together externally and control all 12 channels with a single GPIO input. An EN input allows the entire chip to be placed into a high-impedance (Hi-Z) state while not in use.

These characteristics make the TS3DDR3812 an excellent choice for use in memory, analog/digital video, LAN, and other high-speed signal switching applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS3DDR3812

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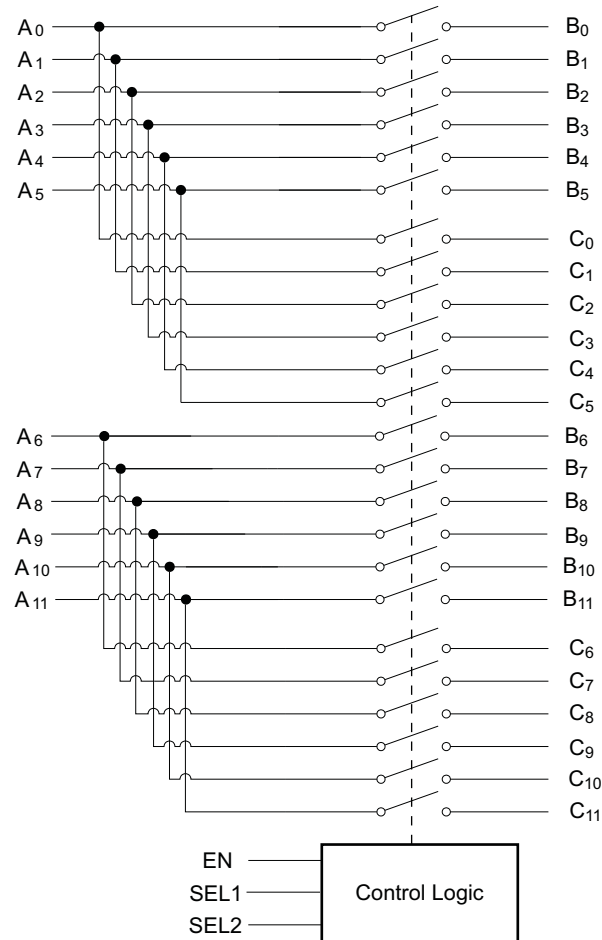
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

Figure 2. LOGIC DIAGRAM



FUNCTION TABLE

EN	SEL1	SEL2	FUNCTION
L	X	X	A ₀ to A ₁₁ , B ₀ to B ₁₁ , and C ₀ to C ₁₁ are Hi-Z
H	L	L	A ₀ to A ₅ = B ₀ to B ₅ and A ₆ to A ₁₁ = B ₆ to B ₁₁
H	L	H	A ₀ to A ₅ = B ₀ to B ₅ and A ₆ to A ₁₁ = C ₆ to C ₁₁
H	H	L	A ₀ to A ₅ = C ₀ to C ₅ and A ₆ to A ₁₁ = B ₆ to B ₁₁
H	H	H	A ₀ to A ₅ = C ₀ to C ₅ and A ₆ to A ₁₁ = C ₆ to C ₁₁

TERMINAL FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
V _{CC}	1,17, 30	Supply Voltage
GND	ThermalPad	Ground

TERMINAL FUNCTIONS (continued)

PIN		DESCRIPTION
NAME	NUMBER	
EN	8	Enable Input
SEL1	9	Select Input
SEL2	10	Select Input
A ₀ , A ₁ , A ₂ , A ₃ , A ₄ , A ₅ , A ₆ , A ₇ , A ₈ , A ₉ , A ₁₀ , A ₁₁	2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16	Data I/Os
B ₀ , B ₁ , B ₂ , B ₃ , B ₄ , B ₅ , B ₆ , B ₇ , B ₈ , B ₉ , B ₁₀ , B ₁₁	41, 39, 38, 36, 34, 32, 29, 27, 25, 23, 21, 19	Data I/Os
C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁	42, 40, 37, 35, 33, 31, 28, 26, 24, 22, 20, 18	Data I/Os

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		–0.5	4.6	V
V _{I/O}	Analog voltage range ⁽²⁾⁽³⁾⁽⁴⁾	A, B, C	–0.5	7	V
V _{IN}	Digital input voltage range ⁽²⁾⁽³⁾	SEL1, SEL2	–0.5	7	V
I _{I/O}	Analog port diode current	V _{I/O} < 0		–50	mA
I _{IK}	Digital input clamp current	V _{IN} < 0		–50	mA
I _{I/O}	On-state switch current ⁽⁵⁾	A, B, C	–128	128	mA
I _{DD} , I _{GND}	Continuous current through V _{DD} or GND		–100	100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	RUA package		31.8	°C/W
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

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RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	3	3.6	V
V _{IH}	High-level control input voltage	2	5.5	V
V _{IL}	Low-level control input voltage	0	0.8	V
V _{IN}	Input voltage	0	5.5	V
V _{I/O}	Input/Output voltage	0	V _{CC}	V
T _A	Operating free-air temperature	–40	85	°C

- (1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#)

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	Digital input clamp voltage	SEL1, SEL2	V _{CC} = 3.6 V, I _{IN} = –18 mA	–1.2	–0.8		V
R _{ON}	ON-state resistance	A, B, C	V _{CC} = 3 V, 1.5 V ≤ V _{I/O} ≤ V _{CC} , I _{I/O} = –40 mA		8	12	Ω
R _{ON(FLAT)} ⁽³⁾	ON-state resistance flatness	A, B, C	V _{CC} = 3 V, V _{I/O} = 1.5 V and V _{CC} , I _{I/O} = –40 mA		1.5		Ω
ΔR _{ON} ⁽⁴⁾	On-state resistance match between channels	A, B, C	V _{CC} = 3 V, 1.5 V ≤ V _{I/O} ≤ V _{CC} , I _{I/O} = –40 mA		0.4	1	Ω
I _{IH}	Digital input high leakage current	SEL1, SEL2	V _{CC} = 3.6 V, V _{IN} = V _{DD}			±1	μA
I _{IL}	Digital input low leakage current	SEL1, SEL2	V _{CC} = 3.6 V, V _{IN} = GND			±1	μA
I _{OFF}	Leakage under power off conditions	All outputs	V _{CC} = 0 V, V _{I/O} = 0 to 3.6 V, V _{IN} = 0 to 5.5 V			±1	μA
C _{IN}	Digital input capacitance	SEL1, SEL2	f = 1 MHz, V _{IN} = 0 V		2.6	3.2	pF
C _{OFF}	Switch OFF capacitance	A, B, C	f = 1 MHz, V _{I/O} = 0 V, Output is open, Switch is OFF		2		pF
C _{ON}	Switch ON capacitance	A, B, C	f = 1 MHz, V _{I/O} = 0 V, Output is open, Switch is ON		5.6		pF
I _{CC}	V _{CC} supply current		V _{CC} = 3.6 V, I _{I/O} = 0, V _{IN} = V _{DD} or GND	300	400		μA

- (1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) R_{ON(FLAT)} is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of R_{ON} from center port (A₅, A₆) to any other ports.

SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $R_L = 200\ \Omega$, $C_L = 4\text{ pF}$ (unless otherwise noted) (see [Figure 7](#) and [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{pd}^{(2)}$	A or B,C	B,C or A		40		ps
t_{PZH} , t_{PZL}	SEL1	A_{0-5} or B_{0-5} , C_{0-5}	2		7	ns
	SEL2	A_{6-11} or B_{6-11} , C_{6-11}	2		7	ns
t_{PHZ} , t_{PLZ}	SEL1	A_{0-5} or B_{0-5} , C_{0-5}	2		5	ns
	SEL2	A_{6-11} or B_{6-11} , C_{6-11}	2		5	ns
$t_{sk(o)}^{(3)}$	A or B,C	B, C or A		6	30	ps
$t_{sk(p)}^{(4)}$	A or B, C	B, C or A		6	30	ps

- (1) All typical values are at $V_{CC} = 3.3\text{V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
- (2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- (3) Output skew between center port (A_5 , A_6) and any other channel.
- (4) Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
X_{TALK}	$R_L = 50\ \Omega$, $f = 250\text{ MHz}$ (see Figure 11)	–43	dB
O_{IRR}	$R_L = 50\ \Omega$, $f = 250\text{ MHz}$ (see Figure 12)	–42	dB
BW	$R_L = 50\ \Omega$, Switch ON (see Figure 10)	1.675	GHz

- (1) All Typical Values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

OPERATING CHARACTERISTICS

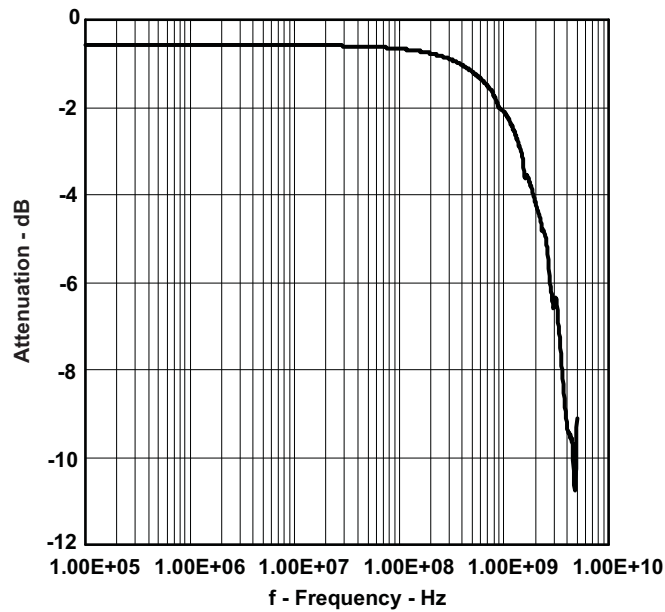


Figure 3. Gain vs Frequency

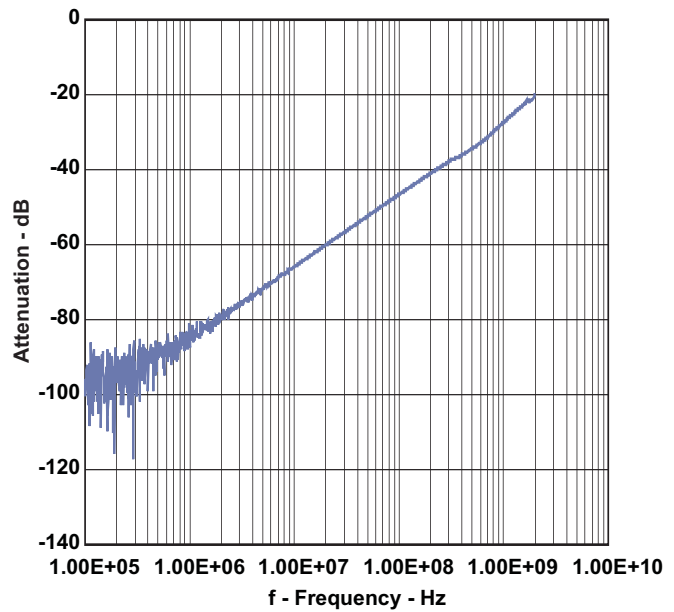


Figure 4. Off Isolation vs Frequency

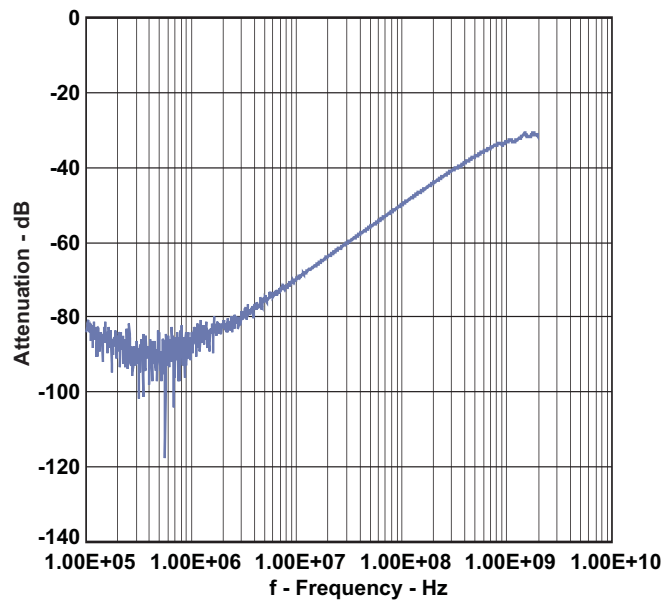


Figure 5. Crosstalk vs Frequency

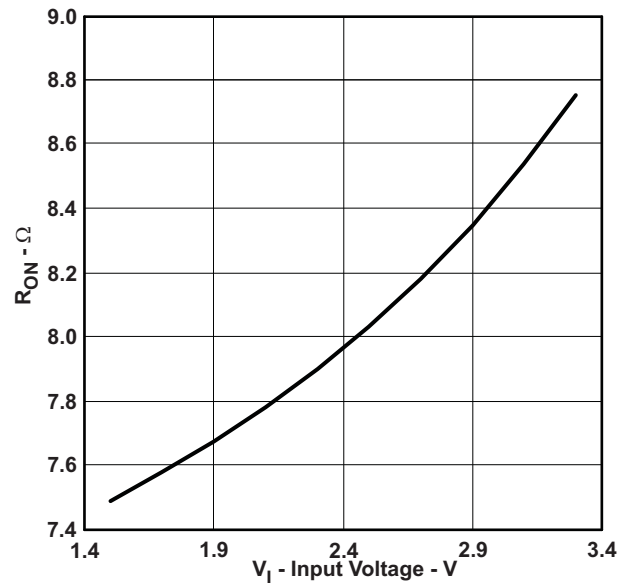
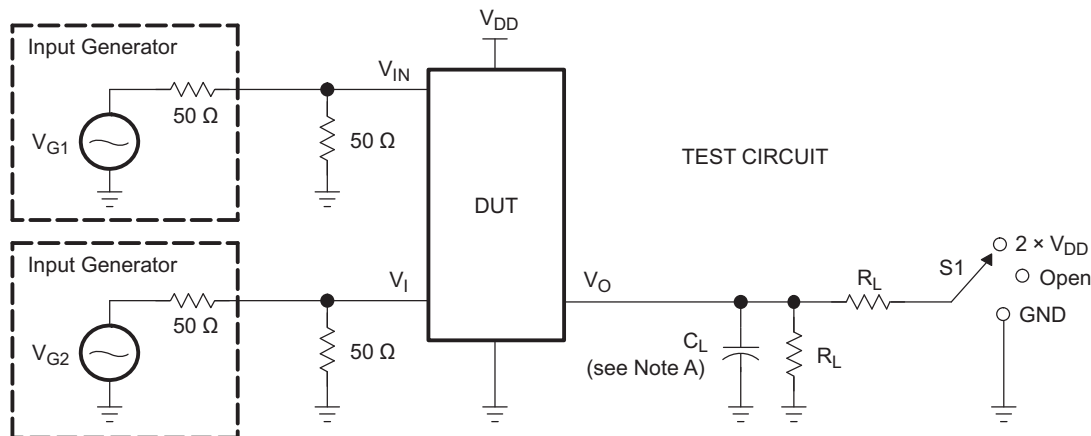


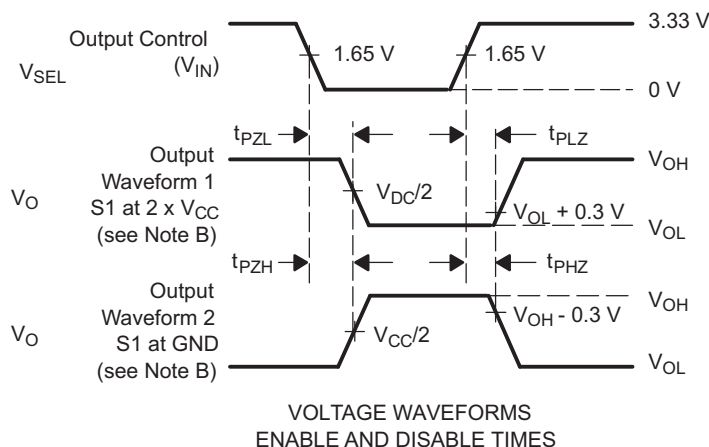
Figure 6. R_{ON} vs V_{IN}

PARAMETER MEASUREMENT INFORMATION

Enable and Disable Times

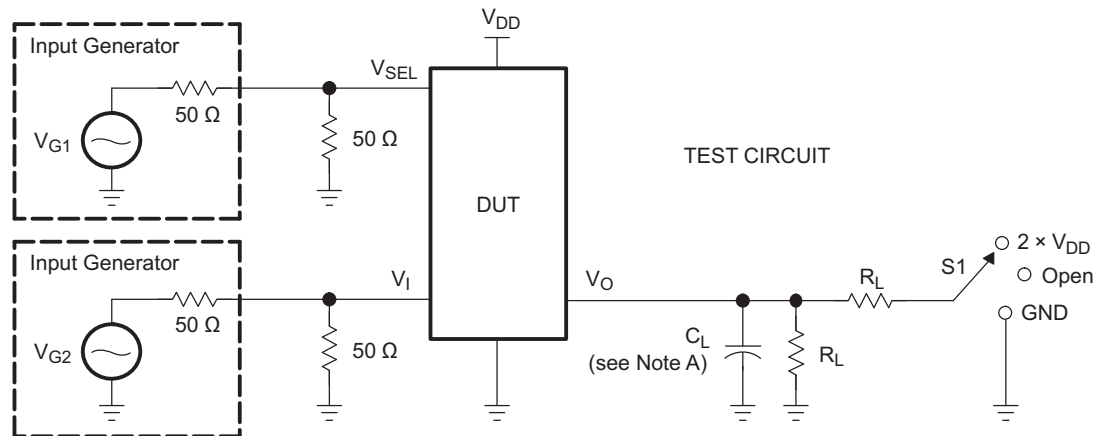


TEST	V _{DD}	S1	R _L	V _{in}	C _L	V _Δ
t _{PLZ} /t _{PZL}	3.3 V ± 0.3 V	2 × V _{DD}	200 Ω	GND	4 pF	0.3 V
t _{PHZ} /t _{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V _{DD}	4 pF	0.3 V

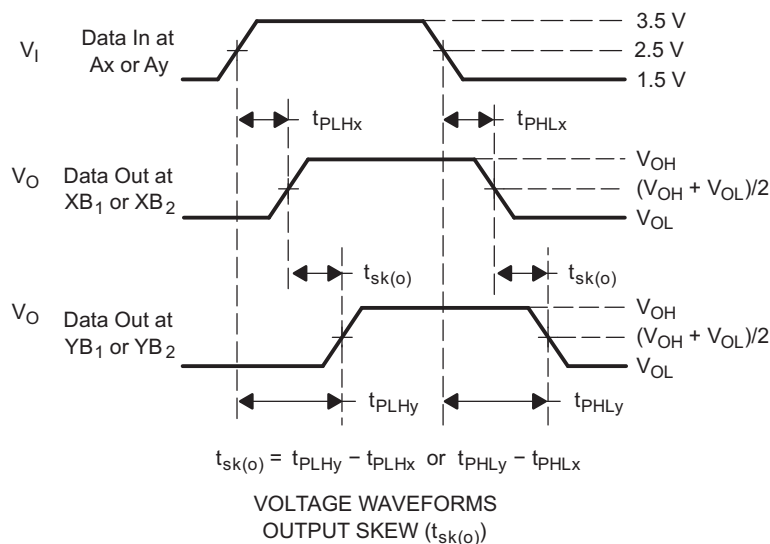


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 7. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
Figure 8. Skew


TEST	V _{CC}	S1	R _L	V _{in}	C _L
t _{sk(o)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	4 pF
t _{sk(p)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	4 pF



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

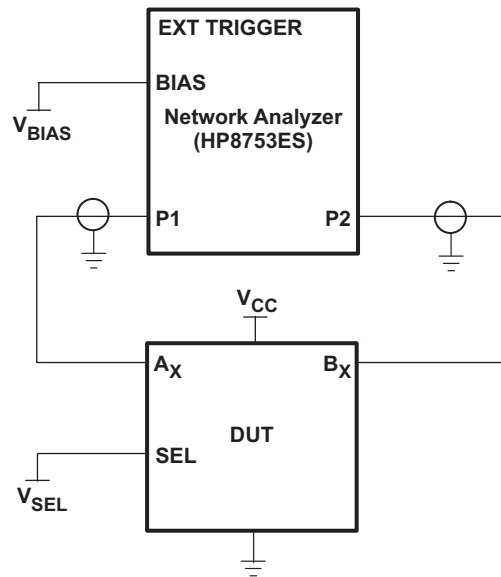


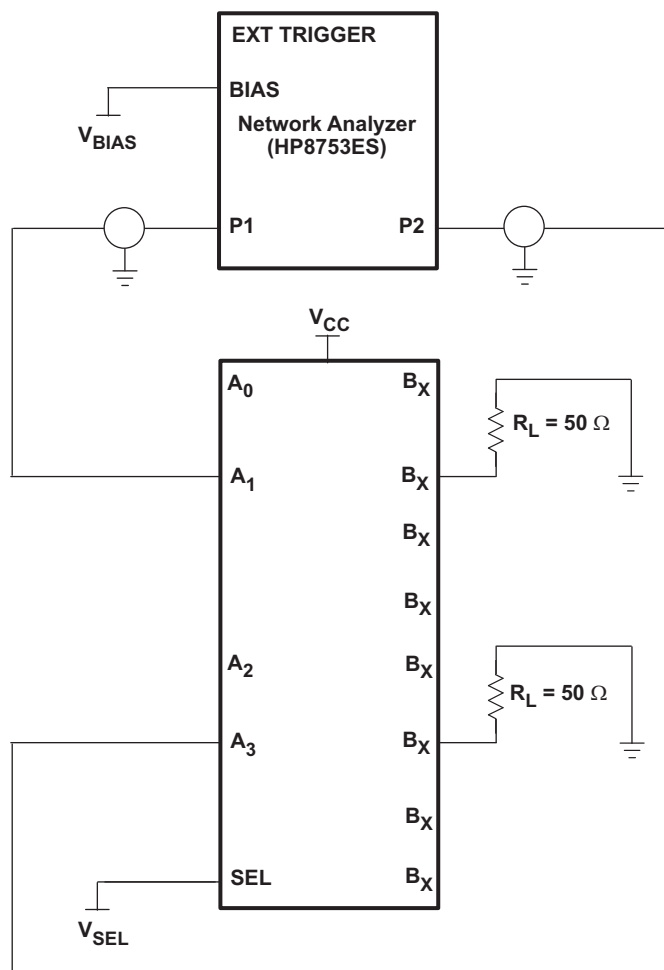
Figure 10. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at B_0 . All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35\text{ V}$
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 11. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_1 is the input, the output is measured at A_3 . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4

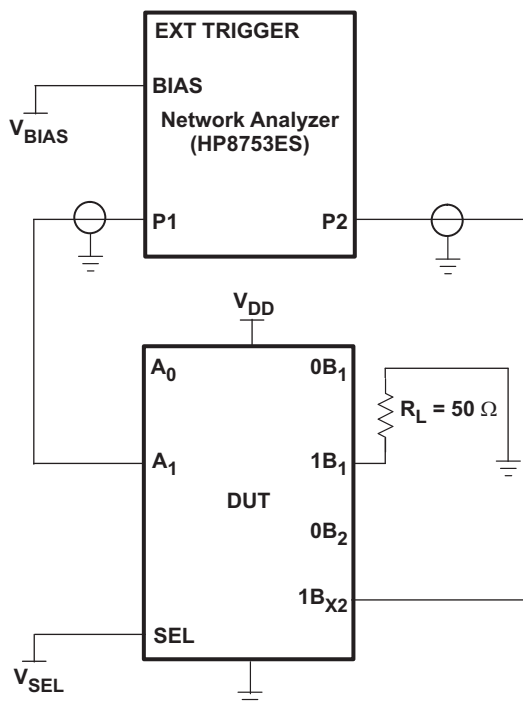
RBW = 3 kHz

$V_{BIAS} = 0.35$ V

ST = 2 s

P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50 Ω termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = \text{GND}$ and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35 \text{ V}$

ST = 2 s

P1 = 0 dBm

REVISION HISTORY

Changes from Revision A (March 2012) to Revision B

Page

- Changed Low B Low Bit-to-Bit Skew in the FEATURES list from ($t_{sk(0)} = 6$ ps Max) to ($t_{sk(0)} = 6$ ps Typ) [1](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DDR3812RUAR	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812
TS3DDR3812RUAR.B	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812
TS3DDR3812RUARG4	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812
TS3DDR3812RUARG4.B	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DDR3812RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3DDR3812RUARG4	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DDR3812RUAR	WQFN	RUA	42	3000	358.0	335.0	35.0
TS3DDR3812RUARG4	WQFN	RUA	42	3000	358.0	335.0	35.0

GENERIC PACKAGE VIEW

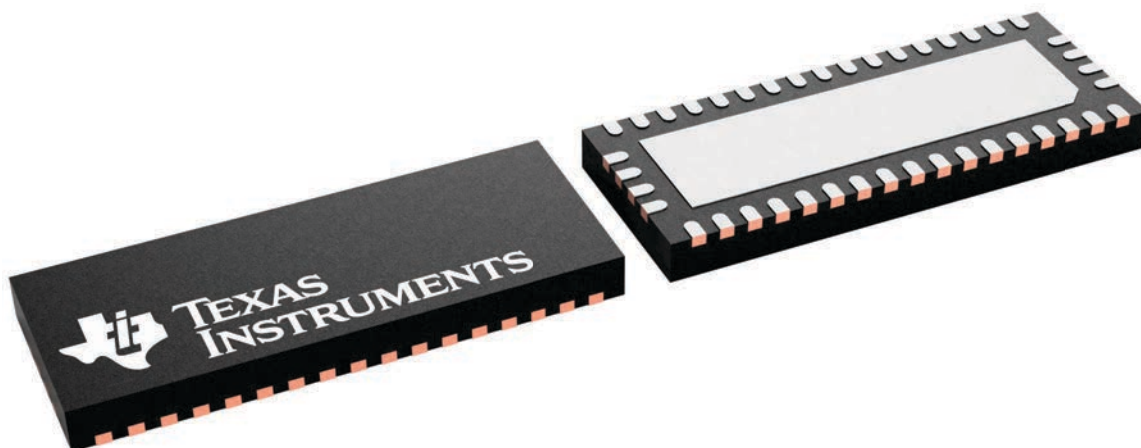
RUA 42

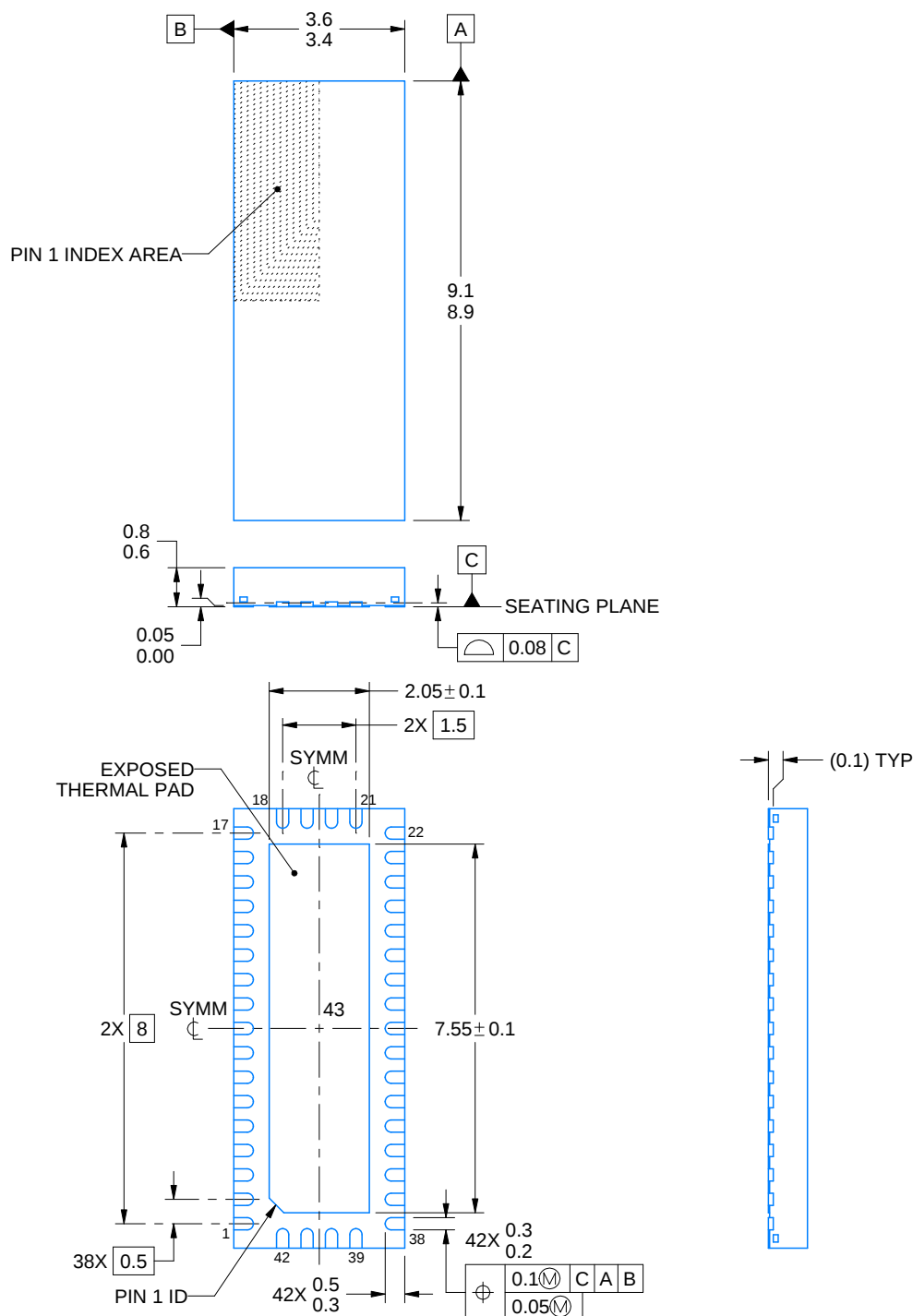
WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4219139/A 03/2020

NOTES:

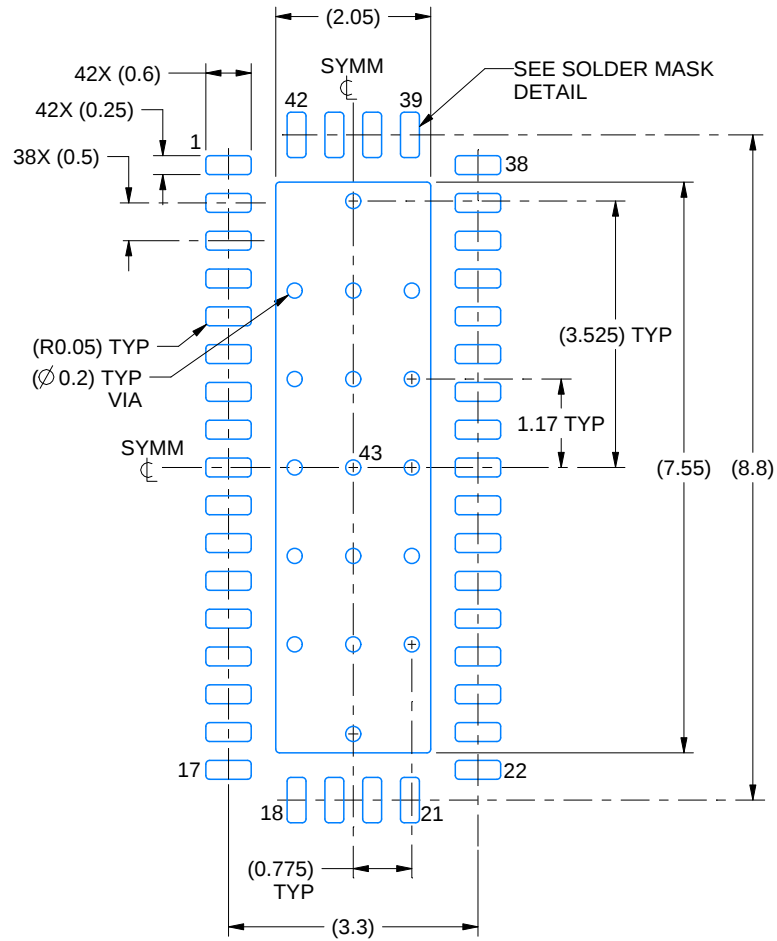
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

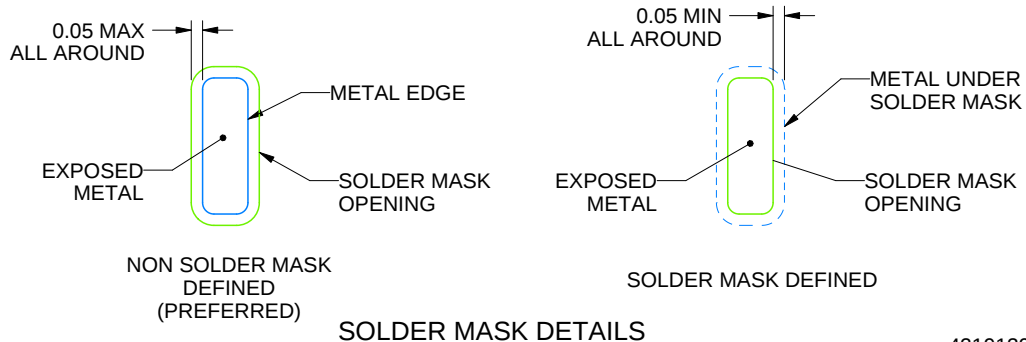
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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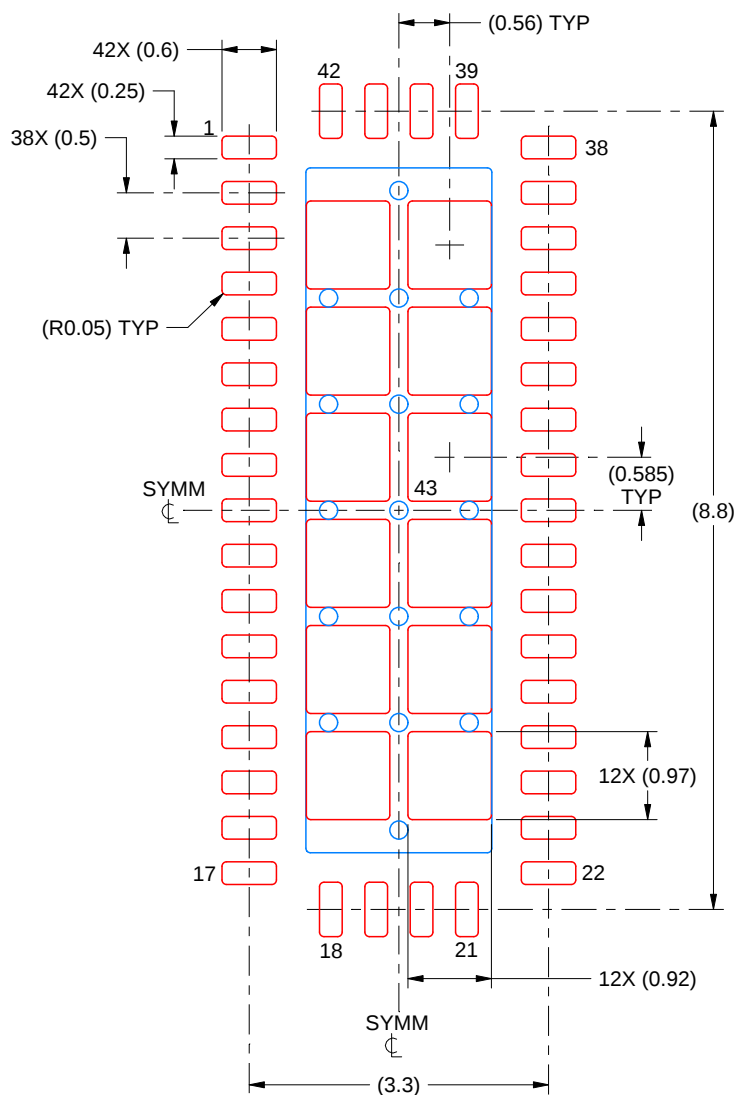
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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