



TS3A5018 10Ω、クワッドSPDTアナログ・スイッチ

1 特長

- 低いオン抵抗(10Ω)
- 低い電荷注入
- 非常に優れたオン抵抗マッチング
- 低い全高調波歪(THD)
- 1.8V～3.6Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
 - 人体モデルで2000V (A114-B、クラスII)
 - 荷電デバイス・モデルで1000V (C101)

2 アプリケーション

- サンプル・アンド・ホールド回路
- バッテリ駆動の機器
- オーディオおよびビデオ信号のルーティング
- 通信用回路

3 概要

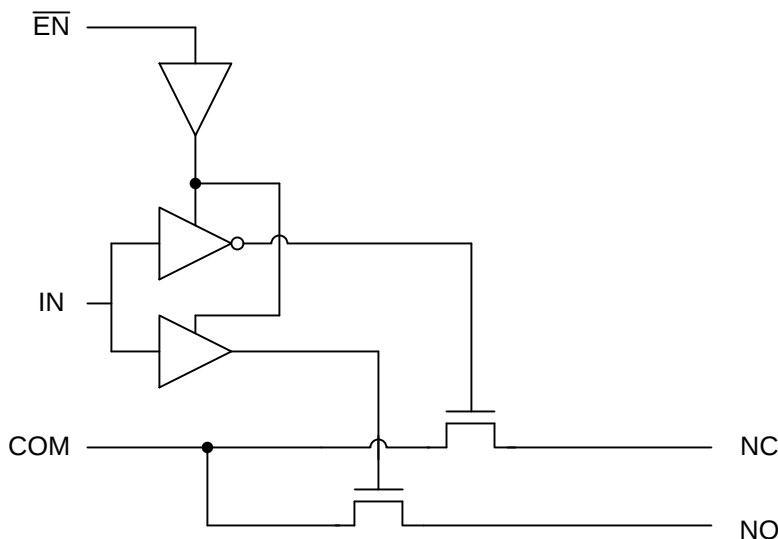
TS3A5018デバイスはクワッド単極双投(SPDT)アナログ・スイッチで、1.8V～3.6Vで動作するように設計されています。このデバイスはデジタルとアナログの両方の信号を処理でき、 V_{+} までの信号をどちらの方向にも転送できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TS3A5018	SOIC (16)	9.90mm×6.00mm
	SSOP (16)	6.00mm×4.90mm
	TSSOP (16)	5.00mm×4.40mm
	TVSOP (16)	4.40mm×3.60mm
	UQFN (16)	2.50mm×1.80mm
	VQFN (16)	4.00mm×3.50mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

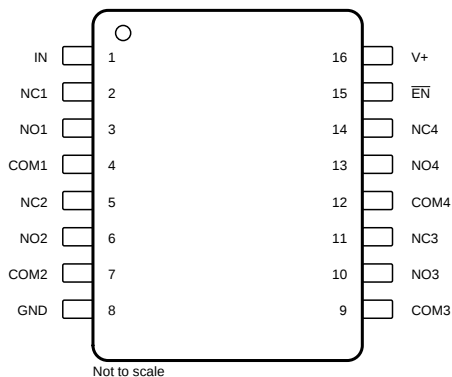
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (March 2015) から Revision H に変更	Page
• Changed the pinout images	3
• Changed the r_{on} MAX value at 25°C From: 8 Ω To: 17 Ω in the <i>Electrical Characteristics for 1.8-V Supply</i> table	7
• Changed the r_{on} MAX value at Full From: 14.55 Ω To: 32 Ω in the <i>Electrical Characteristics for 1.8-V Supply</i> table	7

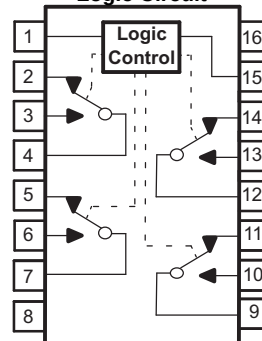
Revision F (June 2013) から Revision G に変更	Page
• 「アプリケーション」セクション、「製品情報」表、「ピン機能」表、「ESD定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「注文情報」表を削除	1

5 Pin Configuration and Functions

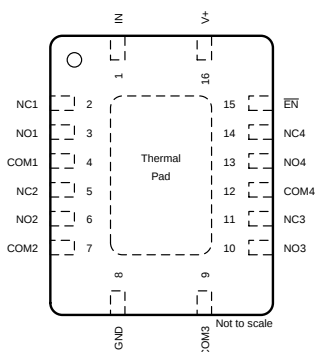
**D, DBQ, DGV and PW Package
16-Pin SOIC, SSOP, TVSOP and TSSOP
(Top View)**



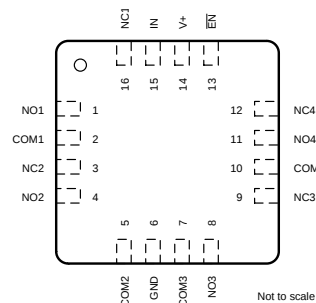
Logic Circuit



**RGY Package
16-Pin VQFN
(Top View)**



**RSV Package
16-Pin UQFN
(Top View)**



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, VQFN NO.	UQFN NO.		
COM1	4	2	I/O	Common path for switch
COM2	7	5	I/O	Common path for switch
COM3	9	7	I/O	Common path for switch
COM4	12	10	I/O	Common path for switch
EN	15	13	I	Active-low switch enable input
GND	8	6	—	Ground
IN	1	15	I	Switch path selector input
NC1	2	16	I/O	Normally closed path for switch
NC2	5	3	I/O	Normally closed path for switch
NC3	11	9	I/O	Normally closed path for switch
NC4	14	12	I/O	Normally closed path for switch
NO1	3	1	I/O	Normally open path for switch
NO2	6	4	I/O	Normally open path for switch
NO3	10	8	I/O	Normally open path for switch
NO4	13	11	I/O	Normally open path for switch
V+	16	14	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V_+	Supply voltage ⁽³⁾	−0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage ⁽³⁾⁽⁴⁾	−0.5	4.6	V
I_K	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	$V_{NC}, V_{NO}, V_{COM} = 0 \text{ to } 7 \text{ V}$		mA
V_I	Digital input voltage ⁽³⁾⁽⁴⁾	−0.5	4.6	V
I_{IK}	Digital input clamp current	$V_I < 0$		mA
I_+	Continuous current through V_+	−100	100	mA
I_{GND}	Continuous current through GND	−100	100	mA
T_{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input and output voltage	0	V_+	V
V_+	Supply voltage	1.65	3.6	V
V_I	Control input voltage	0	3.6	V
T_A	Operating temperature	−40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A5018						UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	RSV (UQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	73	90	120	108	51	184	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
V _{COM} , V _{NO} , V _{NC}	Analog signal range					0		V ₊	V
r _{on}	ON-state resistance	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = −32 mA,	Switch ON, see Figure 17	25°C	3 V	7		10	Ω
				Full				12	
Δr _{on}	ON-state resistance match between channels	V _{NC} or V _{NO} = 2.1 V, I _{COM} = −32 mA,	Switch ON, see Figure 17	25°C	3 V	0.3		0.8	Ω
				Full				1	
r _{on(flat)}	ON-state resistance flatness	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = −32 mA,	Switch ON, see Figure 17	25°C	3 V	5		7	Ω
				Full				8	
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V, or V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, see Figure 18	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full			−0.2		
		V _{NC} or V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0, or V _{NC} or V _{NO} = 3.6 V to 0, V _{COM} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	−2	0.05	2	
				Full			−10		
I _{COM(OFF)}	COM OFF leakage current	V _{COM} = 1 V, V _{NC} or V _{NO} = 3 V, or V _{COM} = 3 V, V _{NC} or V _{NO} = 3 V,	Switch OFF, see Figure 18	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full			−0.2		
		V _{COM} = 0 to 3.6 V, V _{NC} or V _{NO} = 3.6 V to 0, or V _{COM} = 3.6 V to 0, V _{NC} or V _{NO} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	−2	0.05	2	
				Full			−10		
I _{NC(ON)} , I _{NO(ON)}	NC, NO ON leakage current	V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, see Figure 19	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full			−0.2		
I _{COM(ON)}	COM ON leakage current	V _{COM} = 1 V, V _{NC} or V _{NO} = Open, or V _{COM} = 3 V, V _{NC} or V _{NO} = Open,	Switch ON, see Figure 19	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full			−0.2		
V _{IH}	Input logic high			Full		2		V ₊	V
V _{IL}	Input logic low			Full		0		0.8	V
I _{IH} , I _{IL}	Input leakage current	V _I = V ₊ or 0		25°C	3.6 V	−1	0.05	1	μA
				Full				−1	
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0,	C _L = 0.1 nF, see Figure 26	25°C	3.3 V		2		pC
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V _{NC} or V _{NO} = V ₊ or GND,	Switch OFF, see Figure 20	25°C	3.3 V		4.5		pF
C _{COM(OFF)}	COM OFF capacitance	V _{COM} = V ₊ or GND,	Switch OFF, see Figure 20	25°C	3.3 V		9		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V _{NC} or V _{NO} = V ₊ or GND,	Switch ON, see Figure 20	25°C	3.3 V		16		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND,	Switch ON, see Figure 20	25°C	3.3 V		16		pF

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 3.3-V Supply (continued)

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance $V_I = V_+$ or GND, See Figure 20	25°C	3.3 V		3		pF
BW	Bandwidth $R_L = 50\ \Omega$, Switch ON, see Figure 22	25°C	3.3 V		300		MHz
O_{ISO}	OFF isolation $R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch OFF, see Figure 23	25°C	3.3 V		-48		dB
X_{TALK}	Crosstalk $R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, see Figure 24	25°C	3.3 V		-48		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent $R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, see Figure 25	25°C	3.3 V		-81		dB
THD	Total harmonic distortion $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, see Figure 27	25°C	3.3 V		0.21%		
I_+	Positive supply current $V_I = V_+$ or GND, Switch ON or OFF	25°C Full	3.6 V		2.5	7 10	μA

6.6 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3\text{ V to }2.7\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
V_{COM} , V_{NC} , V_{NO}	Analog signal range			0		V_+	V
r_{on}	ON-state resistance $0 \leq (V_{NC} \text{ or } V_{NO}) \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 17	25°C Full	2.3 V		12	20 22	Ω
Δr_{on}	ON-state resistance match between channels $V_{NC} \text{ or } V_{NO} = 1.6\text{ V}$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 17	25°C Full	2.3 V		0.3	1 2	Ω
$r_{on(flat)}$	ON-state resistance flatness $0 \leq (V_{NC} \text{ or } V_{NO}) \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 17	25°C Full	2.3 V		14	18 20	Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, $V_{COM} = 2.2\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 2.2\text{ V}$, $V_{COM} = 0.5\text{ V}$, Switch OFF, see Figure 18	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	μA
	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6\text{ V}$, $V_{COM} = 3.6\text{ V to } 0$, or $V_{NC} \text{ or } V_{NO} = 3.6\text{ V to } 0$, $V_{COM} = 0 \text{ to } 3.6\text{ V}$, Switch OFF, see Figure 18	25°C Full	0 V	-2	0.05	2 10	μA
$I_{COM(OFF)}$	COM OFF leakage current $V_{COM} = 0.5\text{ V}$, $V_{NC} \text{ or } V_{NO} = 2.2\text{ V}$, or $V_{COM} = 2.2\text{ V}$, $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, Switch OFF, see Figure 18	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	μA
	$V_{COM} = 0 \text{ to } 3.6\text{ V}$, $V_{NC} \text{ or } V_{NO} = 3.6\text{ V to } 0$, or $V_{COM} = 3.6\text{ V to } 0$, $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6\text{ V}$, Switch OFF, see Figure 18	25°C Full	0 V	-2	0.05	2 10	μA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 2.2\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, see Figure 19	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	μA
$I_{COM(ON)}$	COM ON leakage current $V_{COM} = 0.5\text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, or $V_{COM} = 2.2\text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, Switch ON, see Figure 19	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	μA
V_{IH}	Input logic high	Full		1.7		V_+	V
V_{IL}	Input logic low	Full		0		0.7	V

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 2.5-V Supply (continued)

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
I_{IH} , I_{IL} Input leakage current	$V_I = V_+$ or 0	25°C	2.7 V	-0.1	0.05	0.1	μA
		Full		-1		1	
Q_C Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 0.1 \text{ nF}$, see Figure 26	25°C	2.5 V		1		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$ NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, see Figure 20	25°C	2.5 V		3		pF
$C_{COM(OFF)}$ COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF, see Figure 20	25°C	2.5 V		9		pF
$C_{NC(ON)}$, $C_{NO(ON)}$ NC, NO ON capacitance	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, see Figure 20	25°C	2.5 V		16		pF
$C_{COM(ON)}$ COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON, see Figure 20	25°C	2.5 V		16		pF
C_I Digital input capacitance	$V_I = V_+$ or GND, See Figure 20	25°C	2.5 V		3		pF
BW Bandwidth	$R_L = 50 \Omega$, Switch ON, see Figure 22	25°C	2.5 V		300		MHz
O_{ISO} OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch OFF, see Figure 23	25°C	2.5 V		-48		dB
X_{TALK} Crosstalk	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch ON, see Figure 24	25°C	2.5 V		-48		dB
$X_{TALK(ADJ)}$ Crosstalk adjacent	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch ON, see Figure 25	25°C	3.3 V		-81		dB
THD Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 27	25°C	2.5 V		0.33%		
I_+ Positive supply current	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V		2.5	7	μA
		Full				10	

6.7 Electrical Characteristics for 2.1-V Supply

 $V_+ = 2.00 \text{ V to } 2.20 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
V_{IH} Input logic high		Full		1.2		4.3	V
V_{IL} Input logic low		Full		0		0.5	V

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.8 Electrical Characteristics for 1.8-V Supply

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
V_{COM} , V_{NC} , V_{NO} Analog signal range				0		V_+	V
r_{on} ON-state resistance	$0 \leq (V_{NC} \text{ or } V_{NO}) \leq V_+$, $I_{COM} = -32 \text{ mA}$, Switch ON, see Figure 17	25°C	1.65 V		5.5	17	Ω
		Full				32	
Δr_{on} ON-state resistance match between channels	V_{NC} or $V_{NO} = 1.5 \text{ V}$, $I_{COM} = -32 \text{ mA}$, Switch ON, see Figure 17	25°C	1.65 V		0.3	1	Ω
		Full				1.2	
$r_{on(Flat)}$ ON-state resistance flatness	$0 \leq (V_{NC} \text{ or } V_{NO}) \leq V_+$, $I_{COM} = -32 \text{ mA}$, Switch ON, see Figure 17	25°C	1.65 V		2.7	5.5	Ω
		Full				7.3	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 1.8-V Supply (continued)

 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or $V_{NO} = 0.3\text{ V}$, $V_{COM} = 1.65\text{ V}$, or V_{NC} or $V_{NO} = 1.65\text{ V}$, $V_{COM} = 0.3\text{ V}$, Switch OFF, see Figure 18	25°C	1.95 V	-0.25	0.03	0.25	μA
		Full		-4.5		4.5	
	V_{NC} or $V_{NO} = 1.95\text{ V to }0\text{ V}$, $V_{COM} = 0\text{ V to }1.95\text{ V}$, or V_{NC} or $V_{NO} = 0\text{ V to }1.95\text{ V}$, $V_{COM} = 1.95\text{ V to }0\text{ V}$, Switch OFF, see Figure 18	25°C	0 V	-0.4	0.01	0.4	
		Full		-6.5		6.5	
$I_{COM(OFF)}$	$V_{COM} = 1.65\text{ V}$, V_{NC} or $V_{NO} = 0.3\text{ V}$, or $V_{COM} = 0.3\text{ V}$, V_{NC} or $V_{NO} = 1.65\text{ V}$, Switch OFF, see Figure 18	25°C	1.95 V	-0.4	0.02	0.4	μA
		Full		-0.9		0.9	
	$V_{COM} = 0\text{ V to }1.95\text{ V}$, V_{NC} or $V_{NO} = 1.95\text{ V to }0\text{ V}$, or $V_{COM} = 1.95\text{ V to }0$, V_{NC} or $V_{NO} = 0\text{ to }1.95\text{ V}$, Switch OFF, see Figure 18	25°C	0 V	-0.4	0.02	0.4	
		Full		-4.5		4.5	
$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or $V_{NO} = 0.3\text{ V}$, $V_{COM} = \text{Open}$, or V_{NC} or $V_{NO} = 1.65\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, see Figure 19	25°C	1.95 V	-2.	0.02	2	μA
		Full		-2	0.02	2	
$I_{COM(ON)}$	$V_{COM} = 0.3\text{ V}$, V_{NC} or $V_{NO} = \text{Open}$, or $V_{COM} = 1.65\text{ V}$, V_{NC} or $V_{NO} = \text{Open}$, Switch ON, see Figure 19	25°C	1.95 V	-4.5		4.5	μA
		Full					
V_{IH}	Input logic high	Full	1.95 V	1		3.6	V
V_{IL}	Input logic low	Full	1.95 V	0		0.4	V
I_{IH} , I_{IL}	Input leakage current	25°C	1.95 V	-0.1	0.01	0.1	μA
		Full		-2.1		2.1	

6.9 Switching Characteristics for 3.3-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	$V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 21	25°C	3.3 V	2.5	3.5	8	ns
		Full	3 V to 3.6 V	2.5		9	
t_{OFF}	$V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 21	25°C	3.3 V	0.5	2	6.5	ns
		Full	3 V to 3.6 V	0.5		7	

6.10 Switching Characteristics for 2.5-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	$V_{COM} = 1.5\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 21	25°C	2.5 V	2.5	5	9.5	ns
		Full	2.3 V to 2.7 V	2.5		10.5	
t_{OFF}	$V_{COM} = 1.5\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 21	25°C	2.5 V	0.5	3	7.5	ns
		Full	2.3 V to 2.7 V	0.5		9	

6.11 Switching Characteristics for 1.8-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
t _{ON}	Turnon time	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, see Figure 21	25°C	1.8 V		14.1	49.3	ns
				Full	1.65 V to 1.95 V		49.3	56.7	
t _{OFF}	Turnoff time	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, see Figure 21	25°C	1.8 V		16.1	26.5	ns
				Full	1.65 V to 1.95 V			31.2	
t _{BBM}	Break-before-make time	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, see Figure 21	25°C	1.8 V	5.3	18.4	58	ns
				Full	1.65 V to 1.95 V			58	

6.12 Typical Characteristics

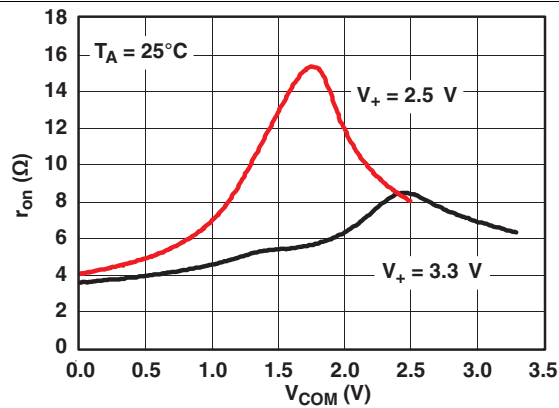


Figure 1. r_{on} vs V_{COM} ($V_+ = 3.3$ V)

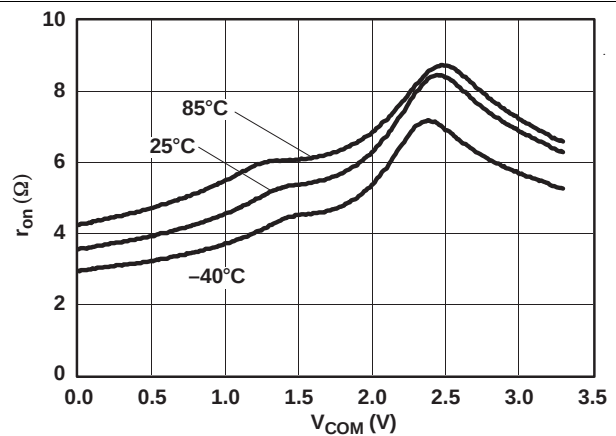


Figure 2. r_{on} vs V_{COM} ($V_+ = 2.5$ V)

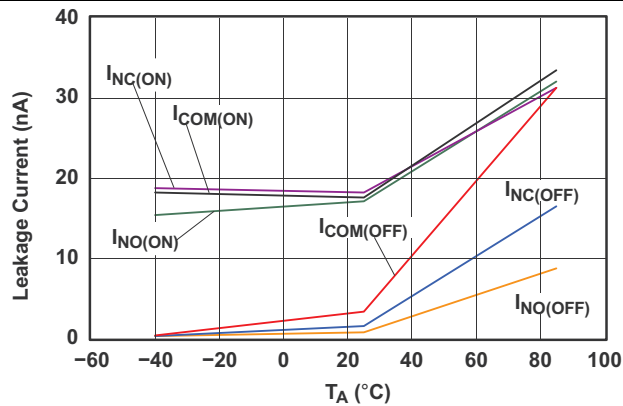


Figure 3. Leakage Current vs Temperature ($V_+ = 3.6$ V)

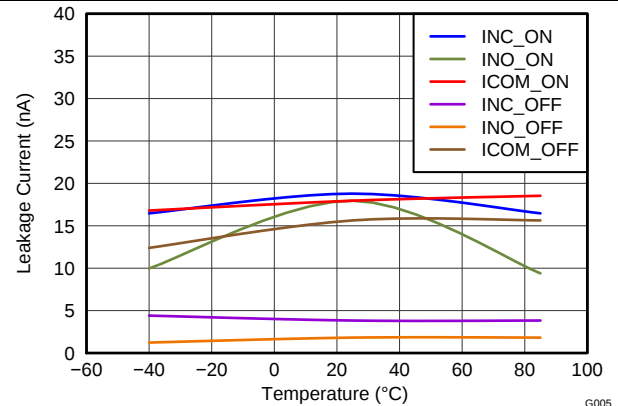


Figure 4. Leakage Current vs Temperature ($V_+ = 1.8$ V)

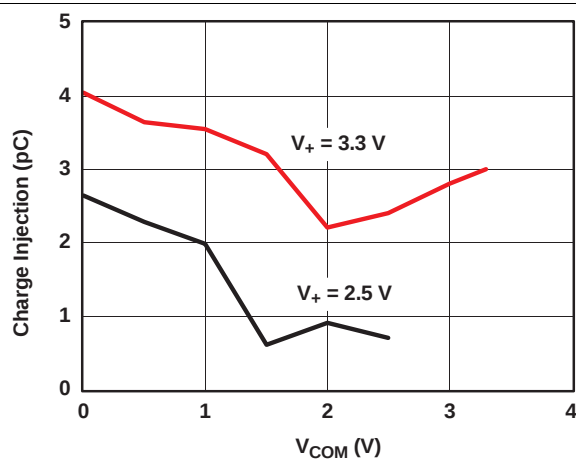


Figure 5. Charge Injection (Q_C) vs V_{COM}

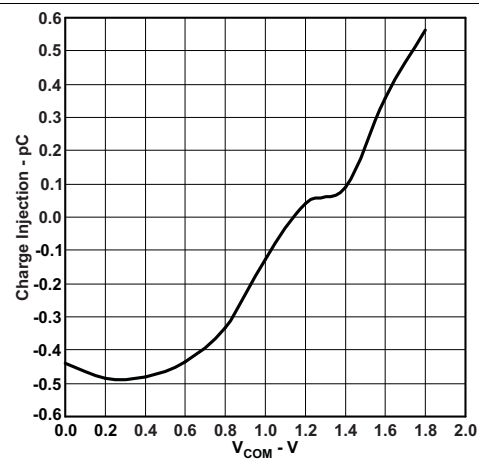


Figure 6. Charge Injection (Q_C) vs V_{COM} ($V_+ = 1.8$ V)

Typical Characteristics (continued)

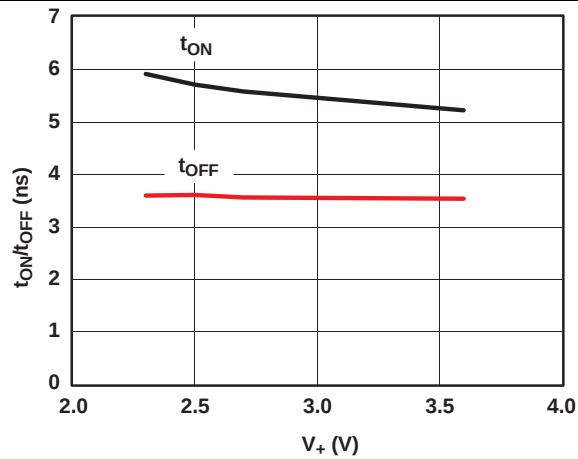


Figure 7. t_{ON} and t_{OFF} vs Supply Voltage

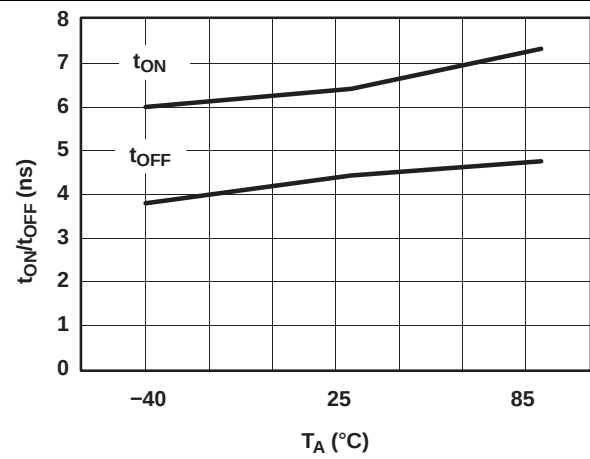


Figure 8. t_{ON} and t_{OFF} vs Temperature (V₊ = 3.3 V)

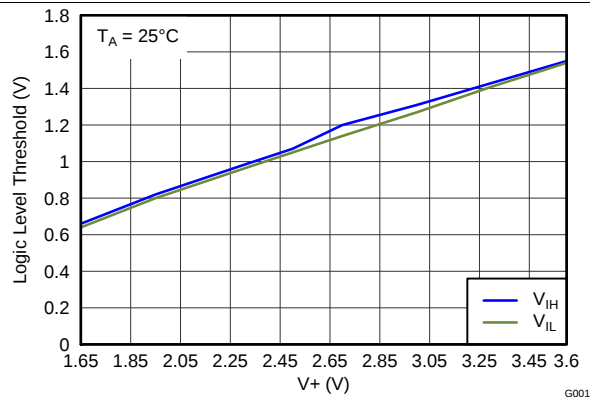


Figure 9. Logic-Level Threshold vs V₊

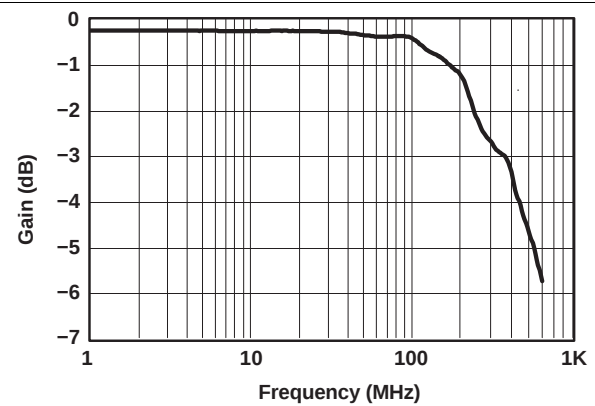


Figure 10. Gain vs Frequency Bandwidth (V₊ = 3.3 V)

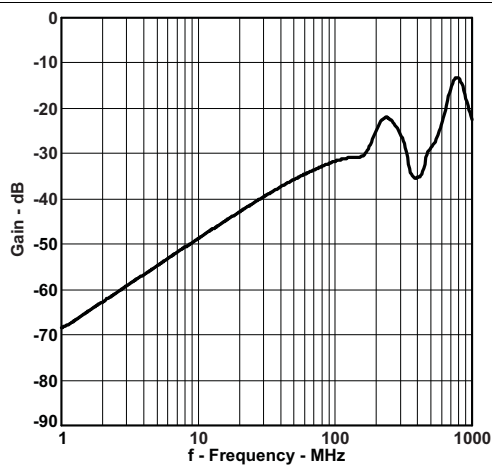


Figure 11. OFF Isolation vs Frequency (V₊ = 1.8 V)

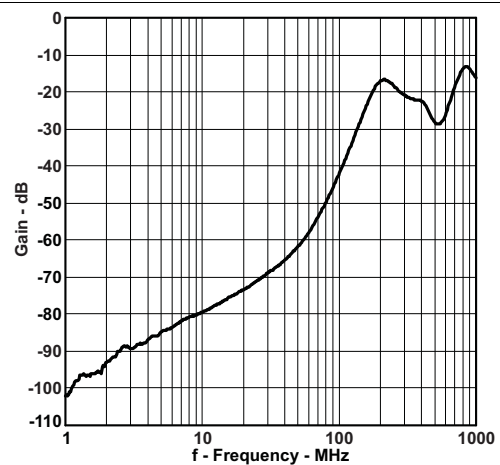
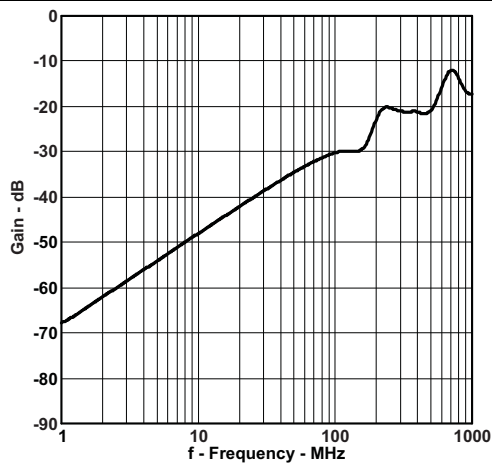
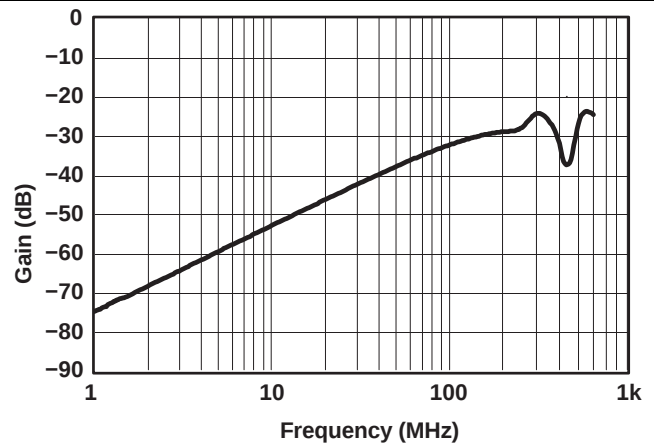
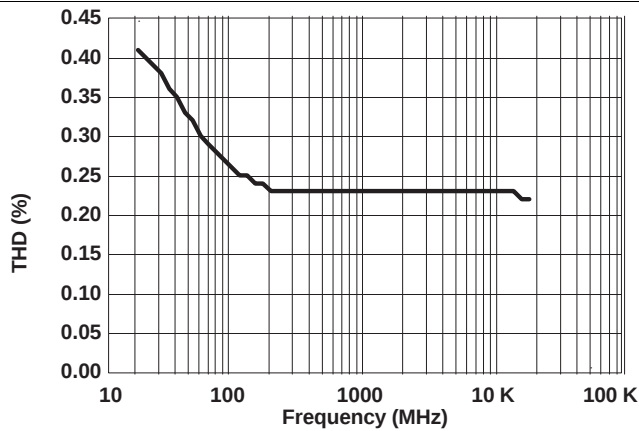
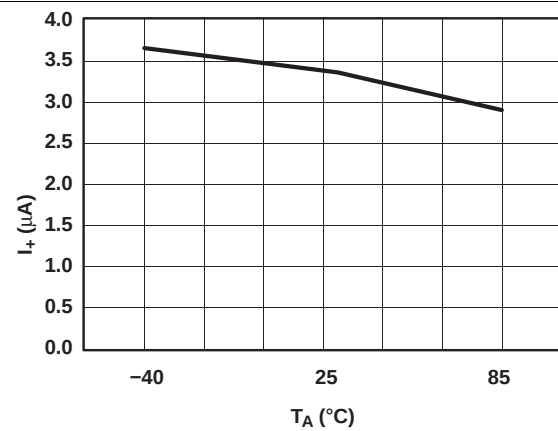


Figure 12. Crosstalk Adjacent vs Frequency (V₊ = 1.8 V)

Typical Characteristics (continued)

Figure 13. Crosstalk vs Frequency ($V_+ = 1.8\text{ V}$)

Figure 14. OFF Isolation vs Frequency ($V_+ = 3.3\text{ V}$)

Figure 15. Total Harmonic Distortion vs Frequency

Figure 16. Power-Supply Current vs Temperature ($V_+ = 3.3\text{ V}$)

7 Parameter Measurement Information

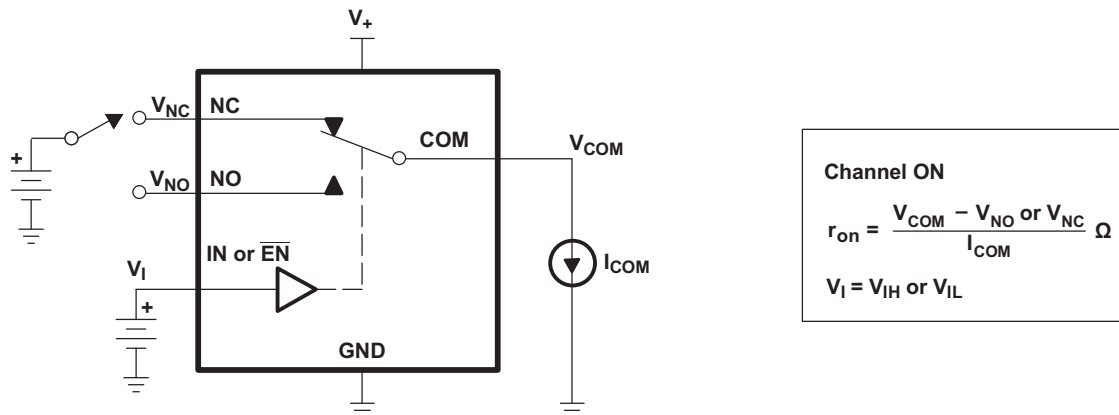


Figure 17. ON-State Resistance (r_{on})

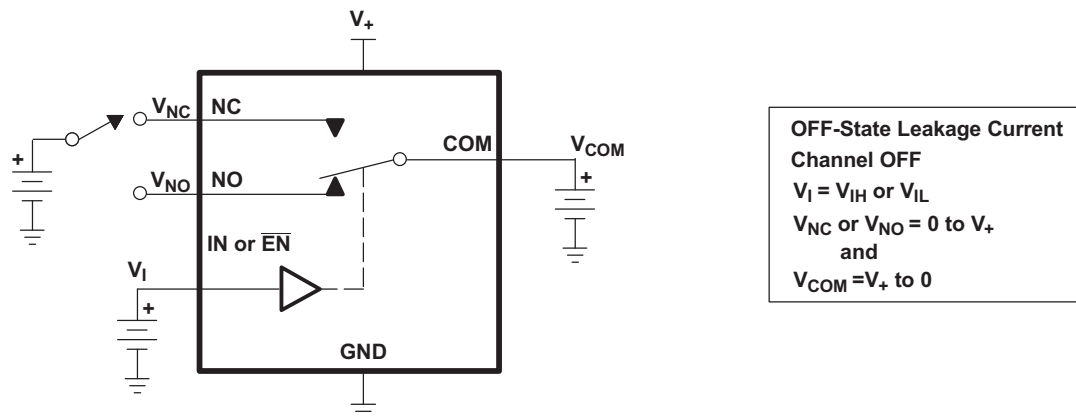


Figure 18. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$)

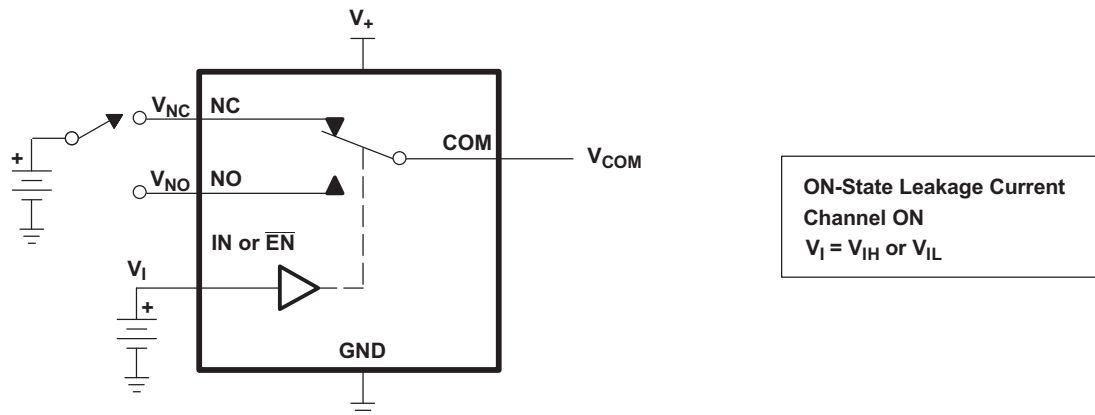
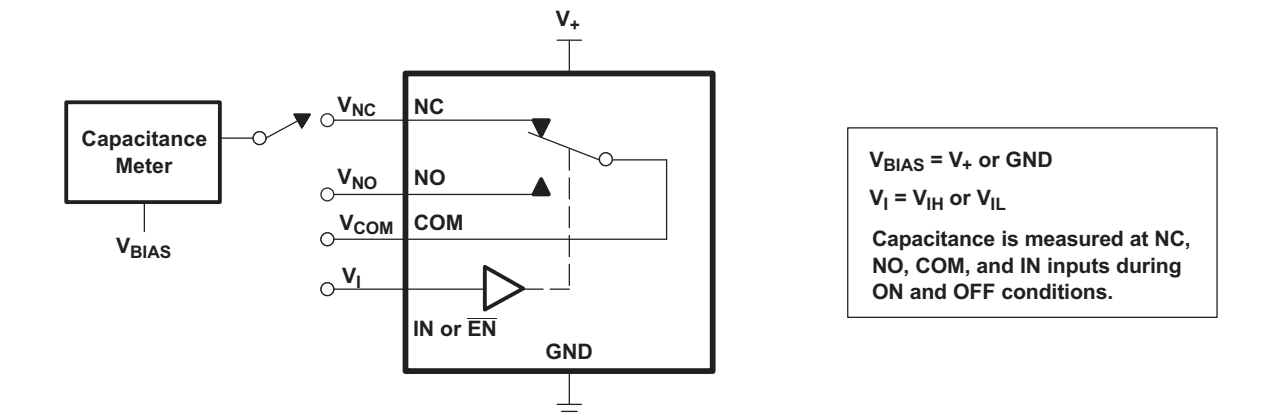
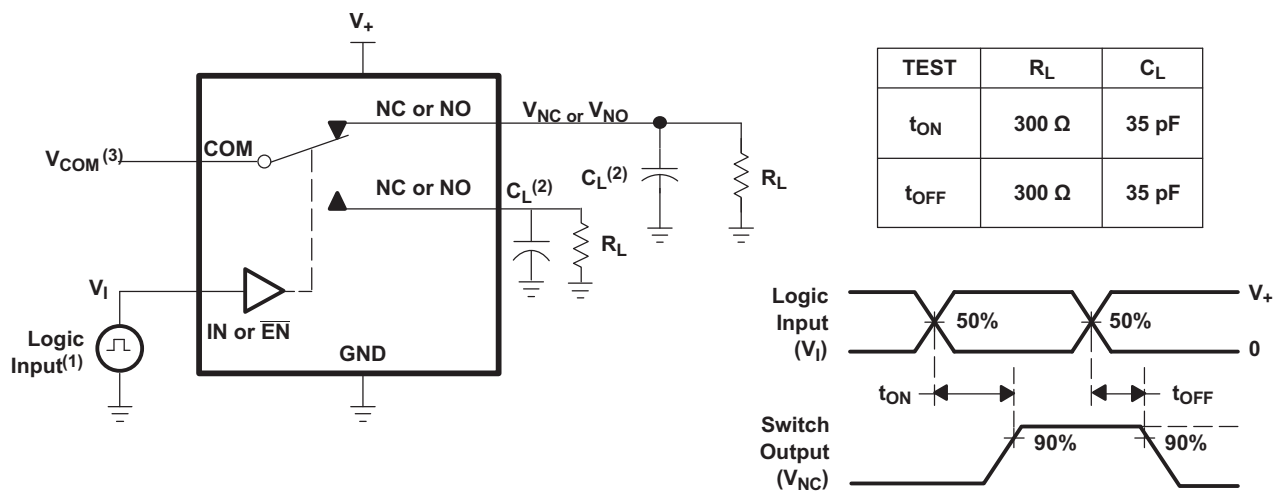
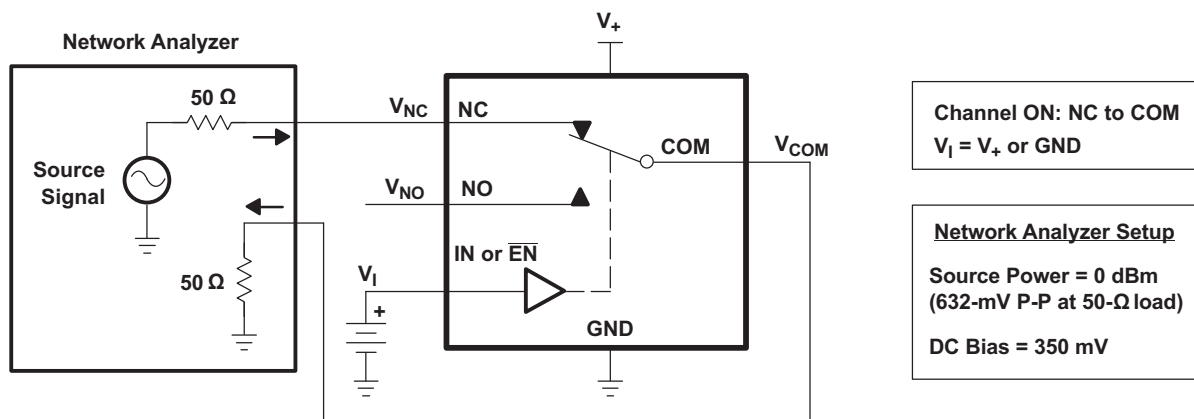


Figure 19. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

Figure 20. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)


- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.
- (3) See Electrical Characteristics for V_{COM} .

Figure 21. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Figure 22. Bandwidth (BW)

Parameter Measurement Information (continued)

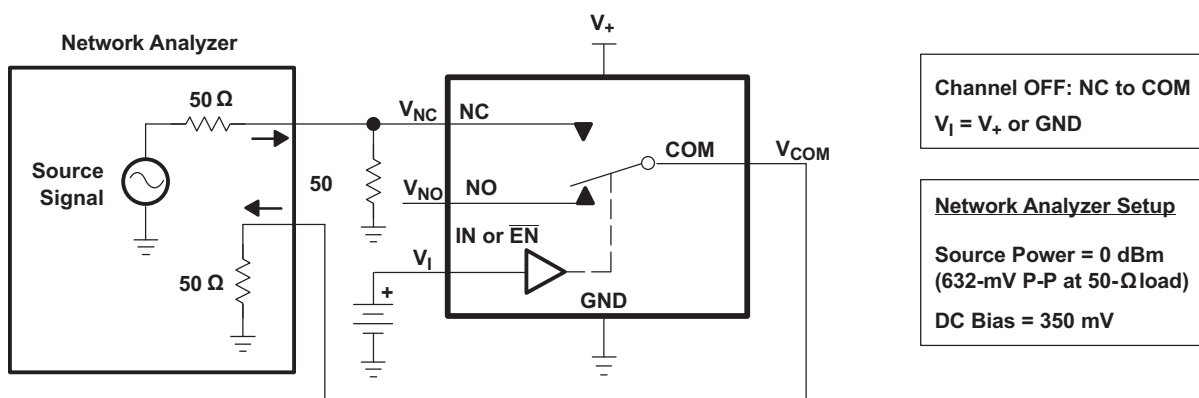


Figure 23. OFF Isolation (O_{ISO})

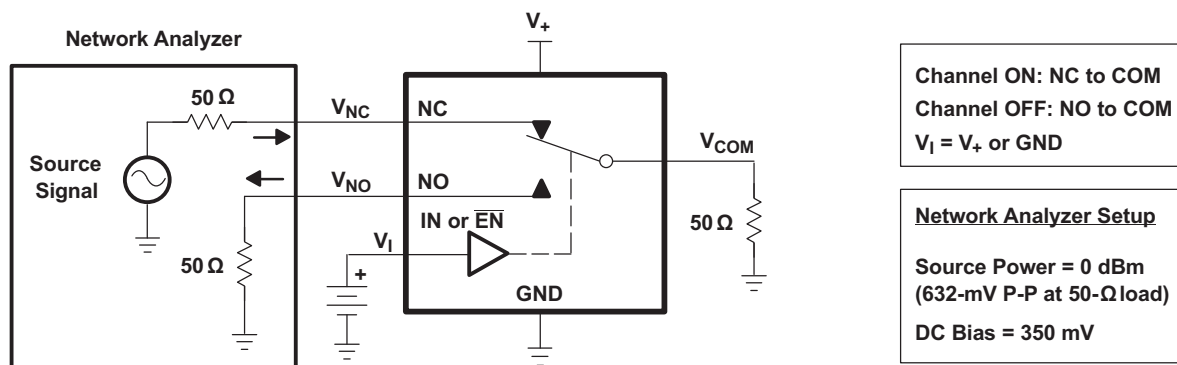


Figure 24. Crosstalk (X_{TALK})

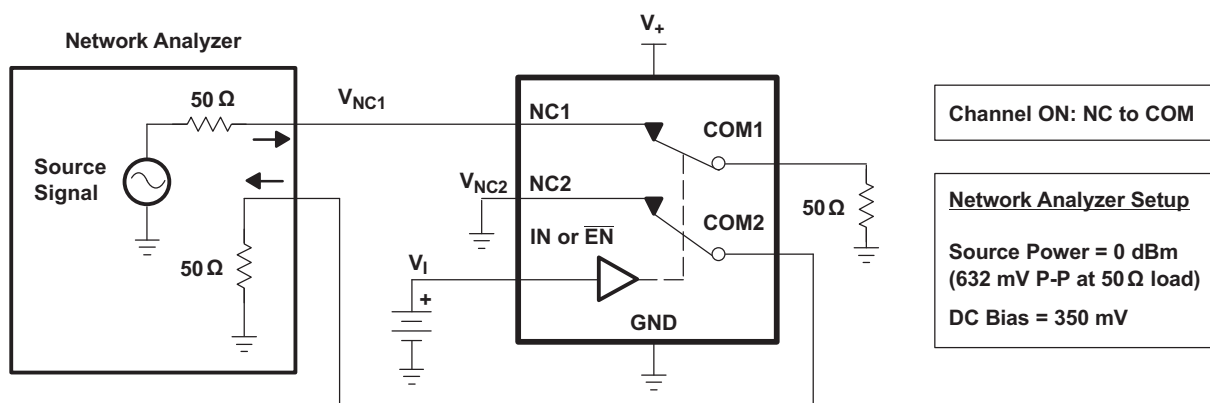
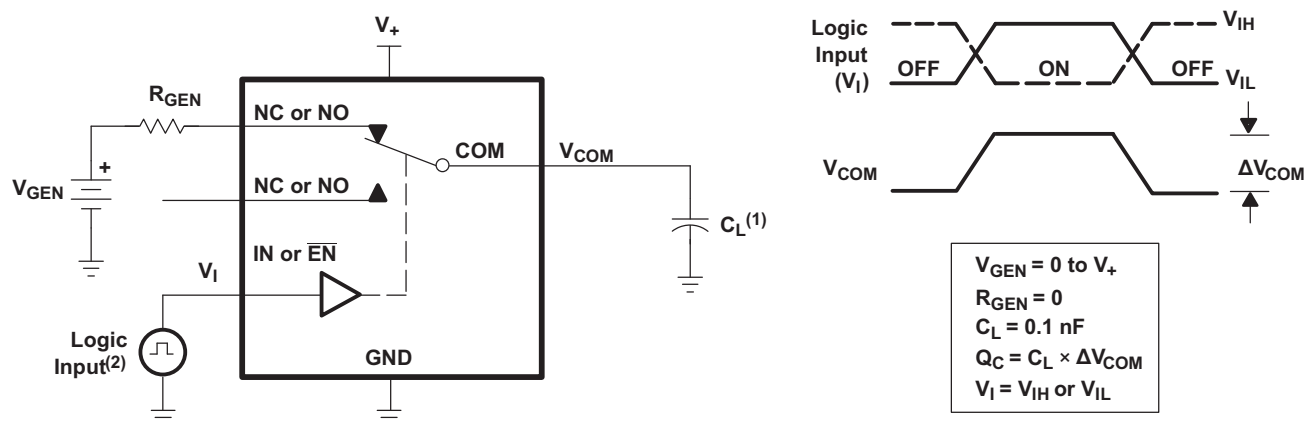
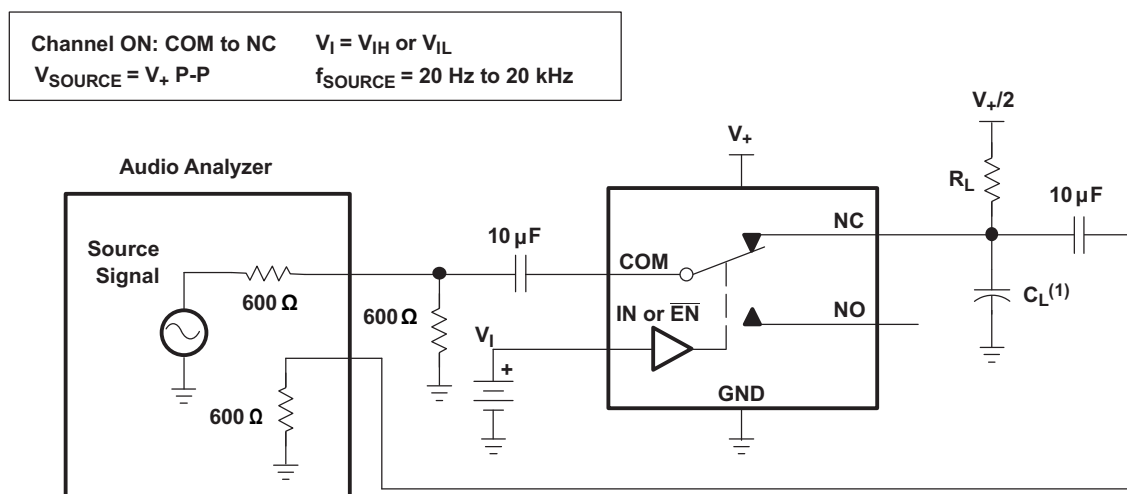


Figure 25. Crosstalk Adjacent

Parameter Measurement Information (continued)


- (1) C_L includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Figure 26. Charge Injection (Q_C)


- (1) C_L includes probe and jig capacitance.

Figure 27. Total Harmonic Distortion (THD)

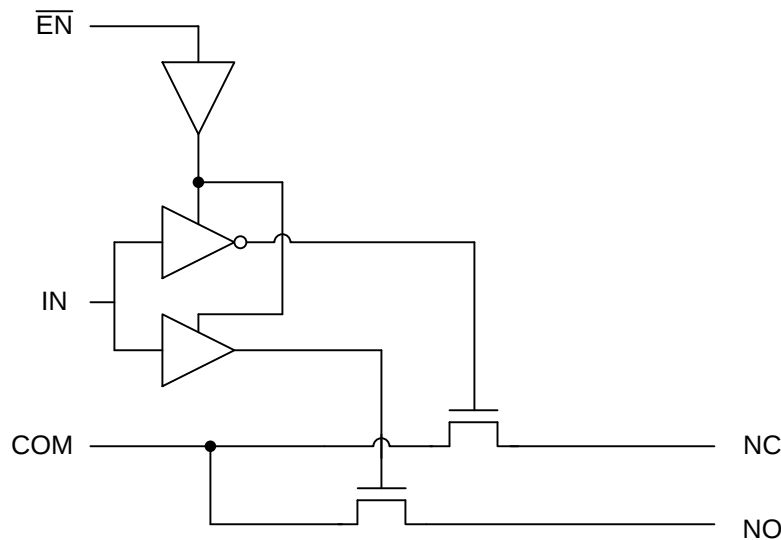
8 Detailed Description

8.1 Overview

The TS3A5018 is a quad single-pole-double-throw (SPDT) solid-state analog switch. The TS3A5018, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. The switch is enabled when $\overline{\text{EN}}$ is low. If IN is also low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS3A5018 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram (Each Switch)



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS3A5018 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.8-V to 3.6-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1. Function Table

$\overline{\text{EN}}$	IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
L	L	OFF	ON
L	H	ON	OFF
H	X	OFF	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5018 can be used in a variety of customer systems. The TS3A5018 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

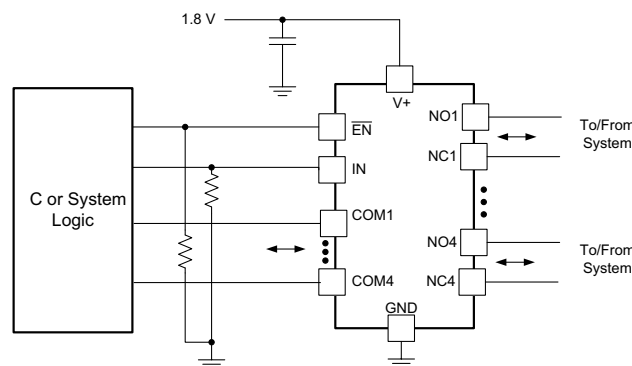


Figure 28. System Schematic for TS3A5018

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in [Recommended Operating Conditions](#). A decoupling capacitor is recommended on the V_+ pin. See [Power Supply Recommendations](#) for more details.

9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$ and IN are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

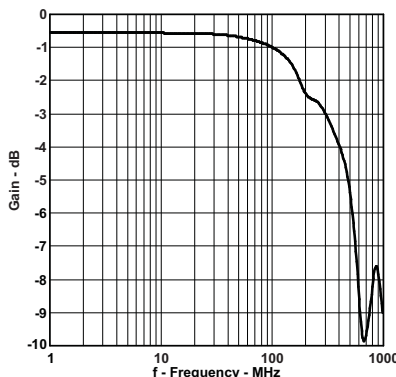


Figure 29. Gain vs Frequency Bandwidth ($V_+ = 1.8$ V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 30](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN and $\overline{\text{EN}}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

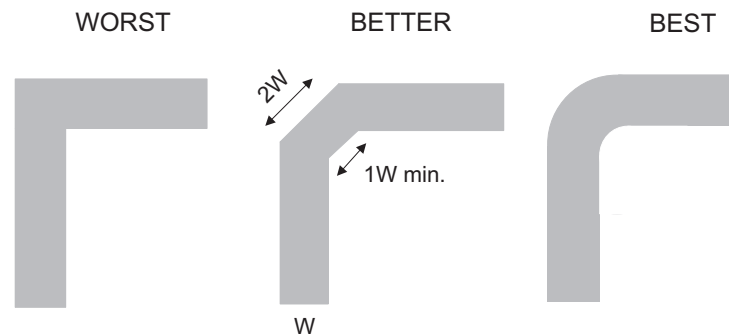


Figure 30. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャンネルがオンのときのCOMとNCポート間、またはCOMとNOポート間の抵抗
Δr_{on}	特定デバイスでのチャンネル間の r_{on} の差
$r_{on(flat)}$	規定の条件の範囲における、チャンネルの r_{on} の最大値と最小値との差
$I_{NC(OFF)}$	対応チャンネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャンネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	対応チャンネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャンネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(OFF)}$	対応チャンネル(COMからNCまたはNO)がオフ状態のとき、COMポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャンネル(COMからNCまたはNO)がオン状態、出力(NCまたはNO)がオープンのとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN, $\overline{EN}$)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN, $\overline{EN}$)の論理LOWの最大入力電圧
V_I	制御入力(IN, $\overline{EN}$)の電圧
I_{IH}, I_{IL}	制御入力(IN, $\overline{EN}$)で測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NCまたはNO)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入 $Q_C = C_L \times \Delta V_{COM}$ で、 C_L は負荷容量、 ΔV_{COM} はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャンネル(NCからCOM)がオフのときのNCポートの容量
$C_{NC(ON)}$	対応チャンネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(OFF)}$	対応チャンネル(NOからCOM)がオフのときのNCポートの容量
$C_{NO(ON)}$	対応チャンネル(NOからCOM)がオンのときのNCポートの容量
$C_{COM(OFF)}$	対応チャンネル(COMからNC)がオフのときのCOMポートの容量
$C_{COM(ON)}$	対応チャンネル(COMからNC)がオンのときのCOMポートの容量
C_I	制御入力(IN, $\overline{EN}$)の容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャンネル(NCからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。
X_{TALK}	クロストークは、オンのチャンネルからオフのチャンネル(NC1からNO1)への、望ましくない信号カップリングの測定値です。隣接クロストークは、オンのチャンネルから隣接するオンのチャンネル(NC1からNC2)への、望ましくない信号カップリングの測定値です。この値は特定の周波数において、dB単位で測定されます。
BW	スイッチの帯域幅。オン状態のチャンネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪は、アナログ・スイッチにより発生する信号の歪みです。この値は、2次、3次、およびさらに高次の高調波の二乗平均(RMS)値と、基本波の絶対振幅との比として定義されます。
I_+	制御(IN)ピンが V_+ またはGNDであるときの静的消費電流

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

ドキュメントのサポート (continued)

- 『低速またはフローティングCMOS入力の影響』、[SCBA004](#)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

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12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A5018D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	TS3A5018
TS3A5018DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018
TS3A5018DBQR.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018
TS3A5018DGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018
TS3A5018DGVR.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018
TS3A5018DGVRG4.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018
TS3A5018DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018
TS3A5018DR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018
TS3A5018DRG4.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018
TS3A5018PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	YA018
TS3A5018PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018
TS3A5018PWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018
TS3A5018RGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018
TS3A5018RGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018
TS3A5018RGYRG4.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018
TS3A5018RSVR	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZUN
TS3A5018RSVR.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZUN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5018DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3A5018DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5018DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5018PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A5018RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3A5018RSVR	UQFN	RSV	16	3000	180.0	13.2	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5018DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
TS3A5018DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
TS3A5018DR	SOIC	D	16	2500	353.0	353.0	32.0
TS3A5018PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TS3A5018RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0
TS3A5018RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES:

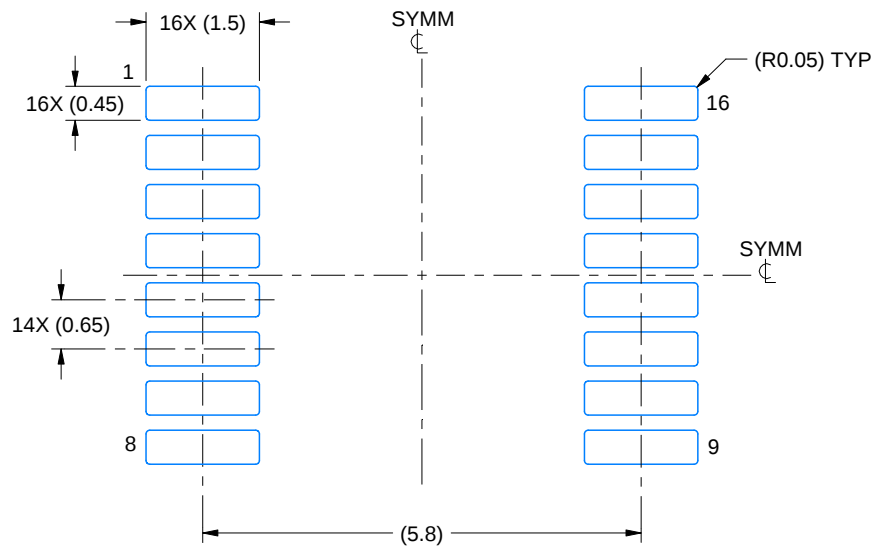
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

EXAMPLE BOARD LAYOUT

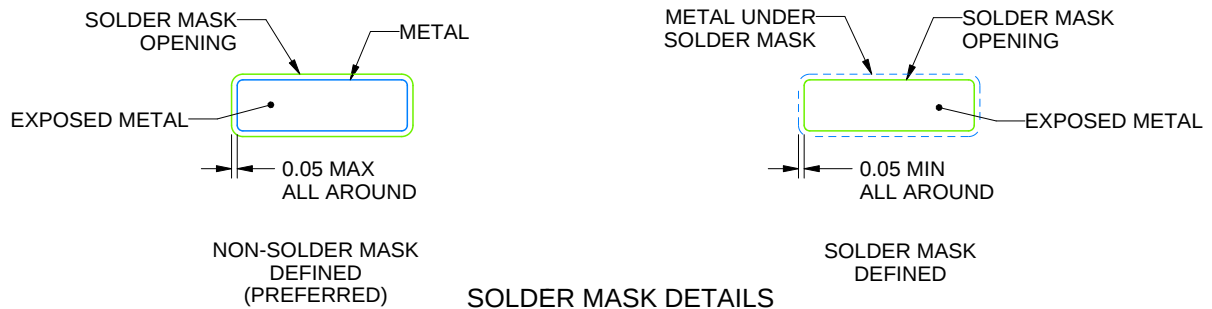
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

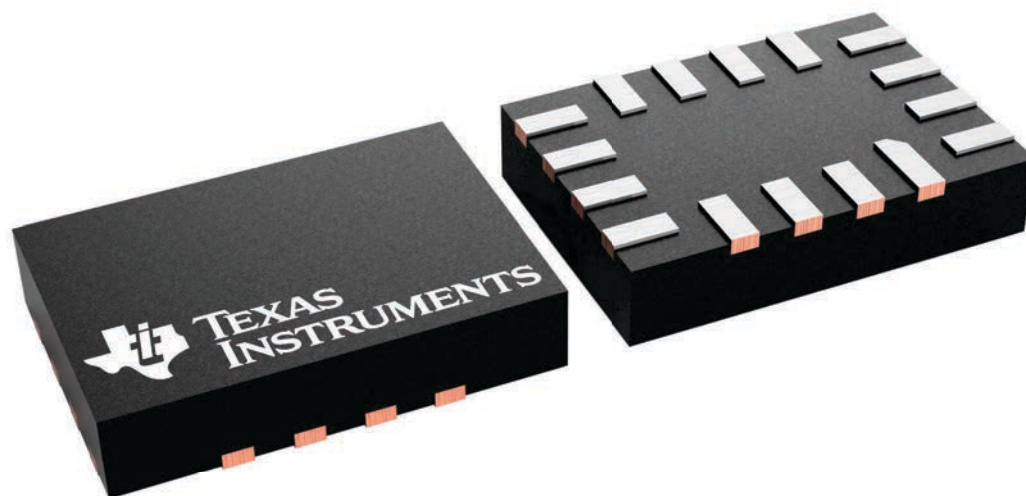
RSV 16

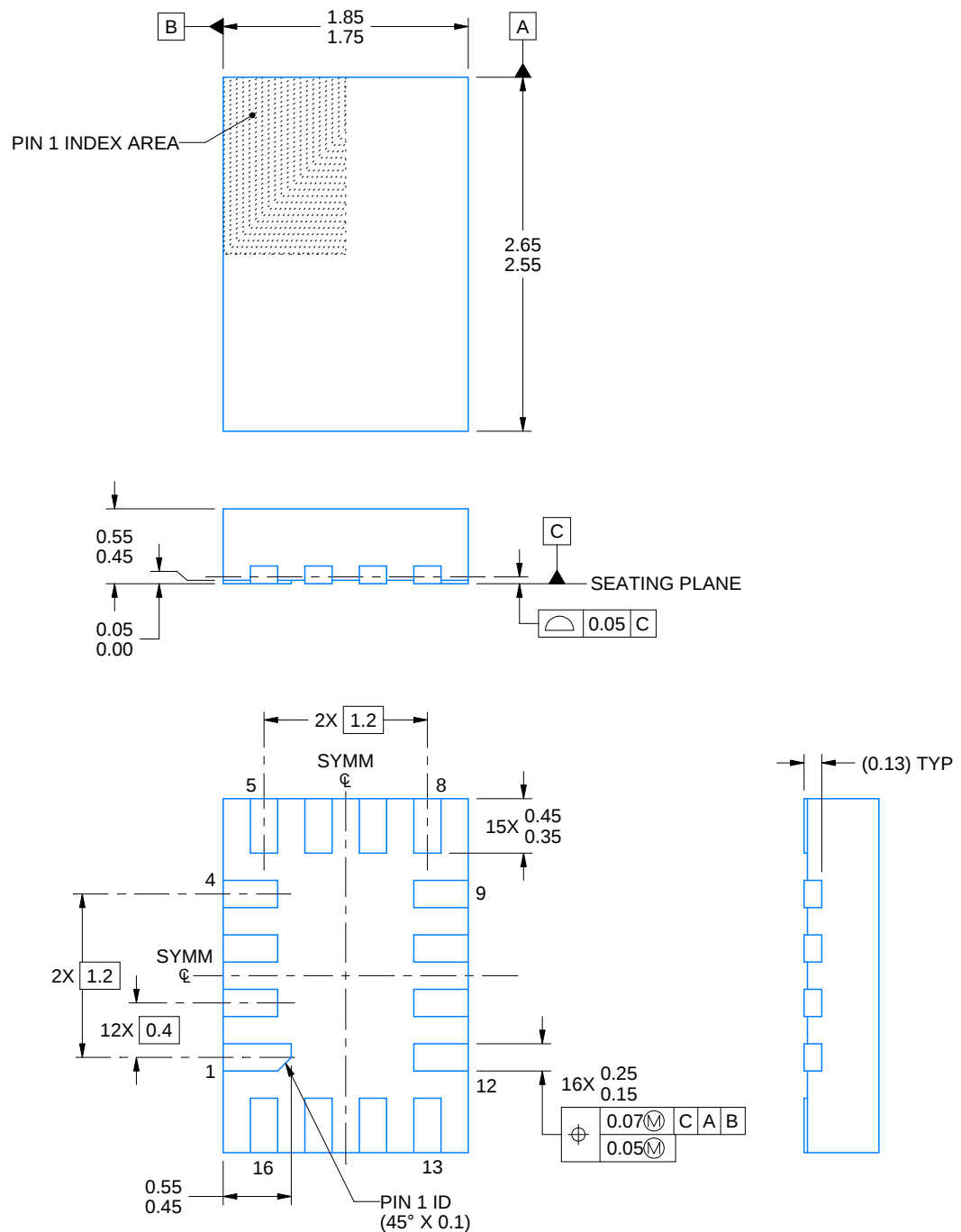
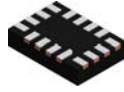
UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4220314/C 02/2020

NOTES:

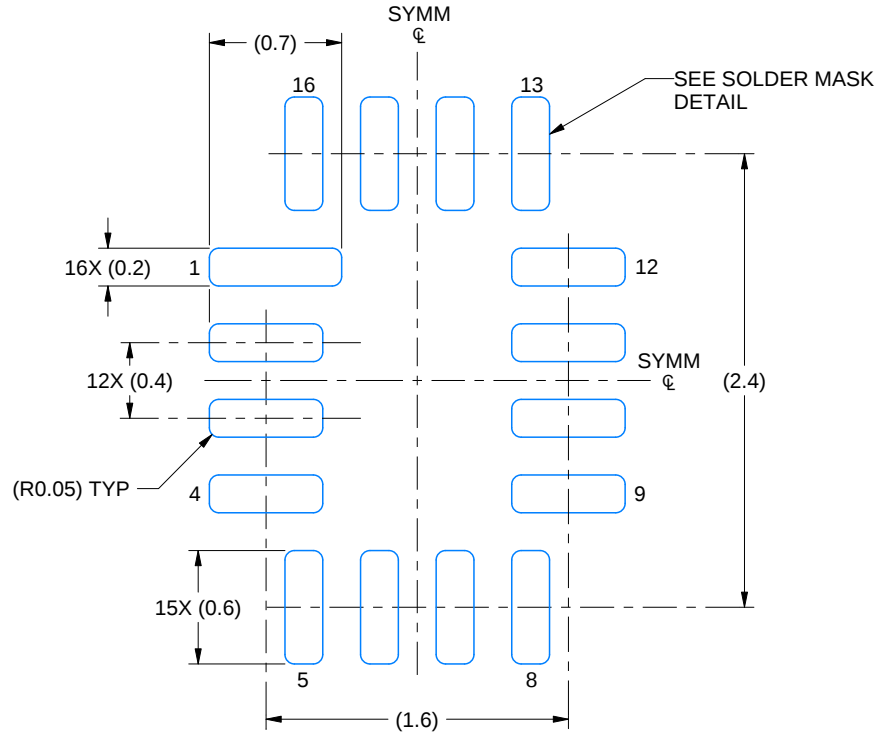
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

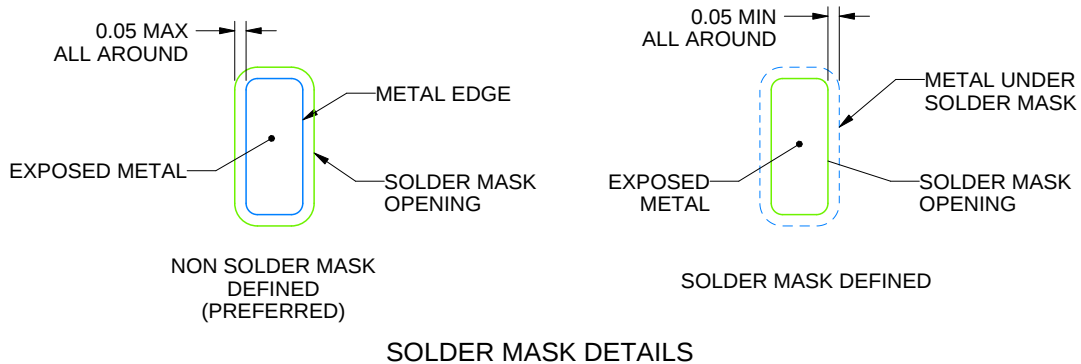
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

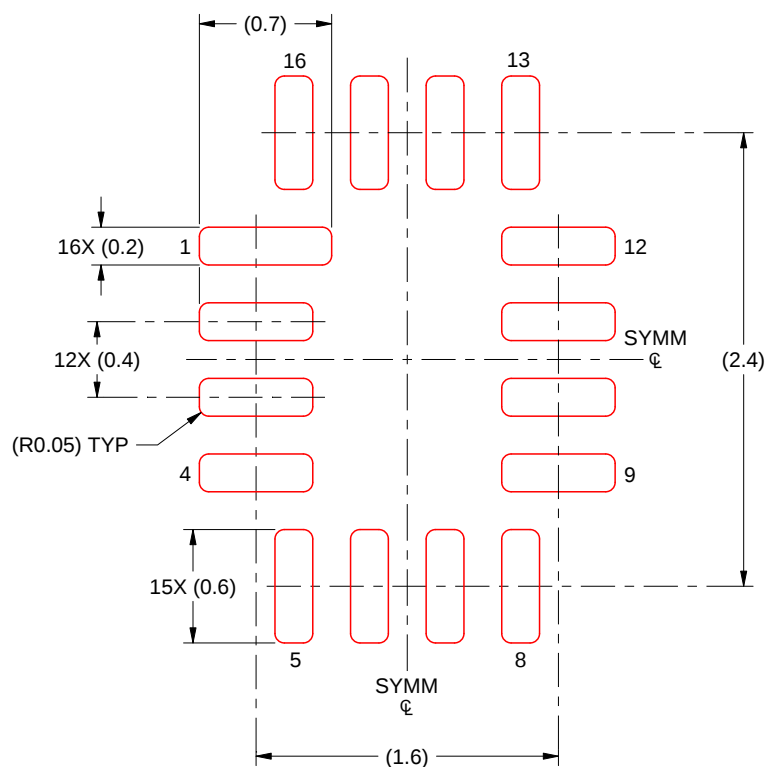
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 25X

4220314/C 02/2020

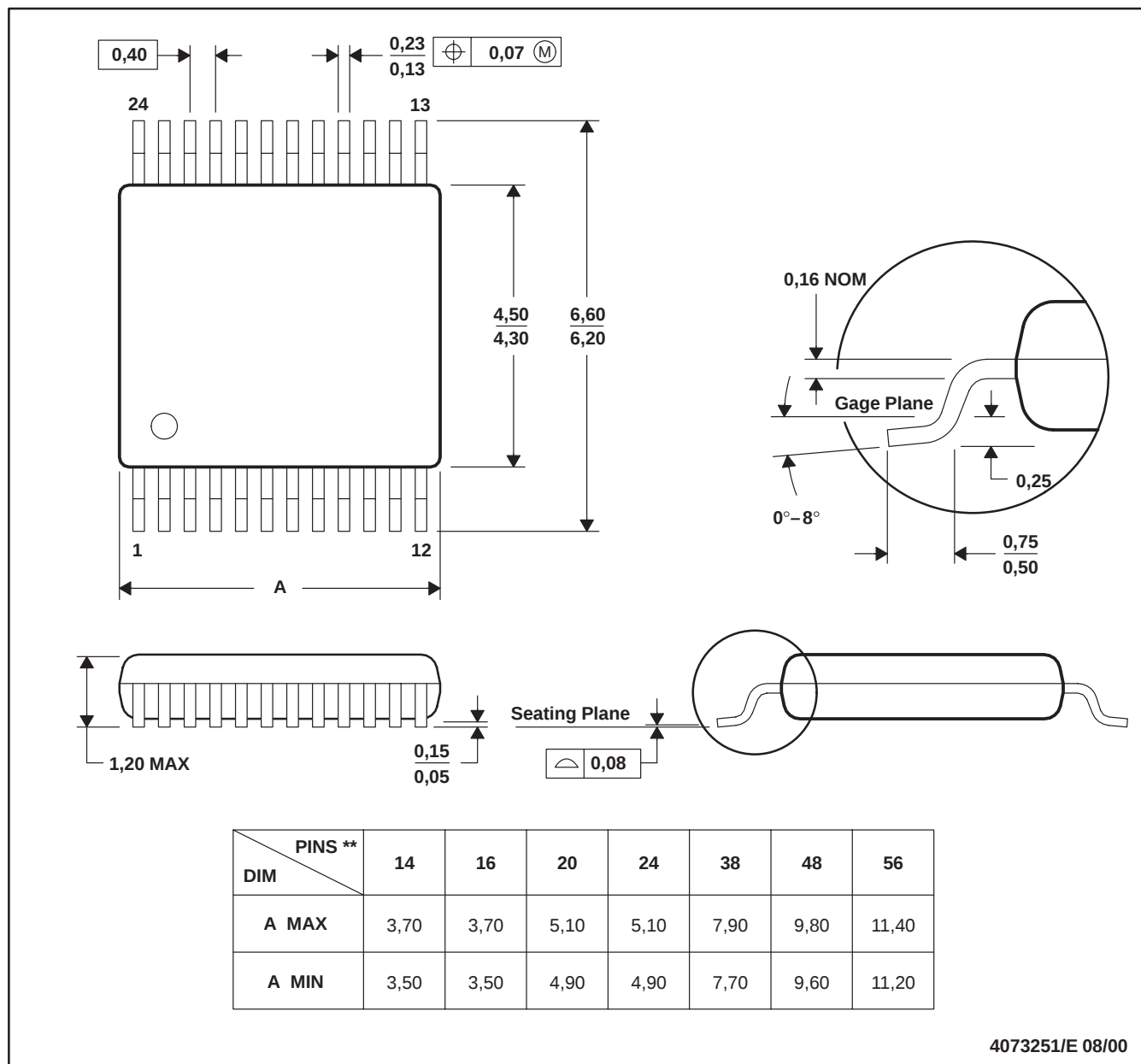
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

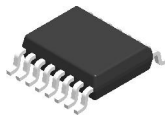
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

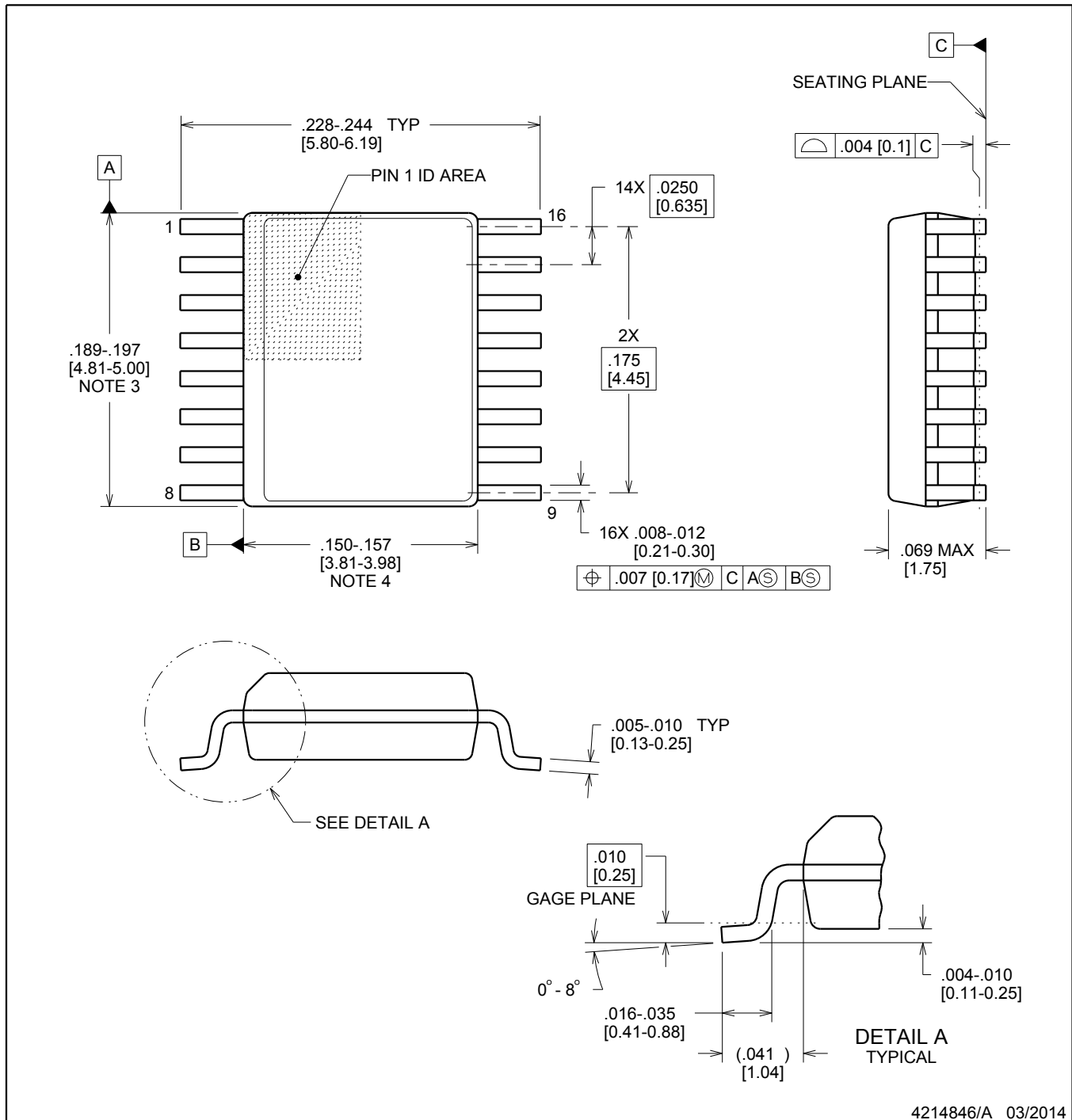


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

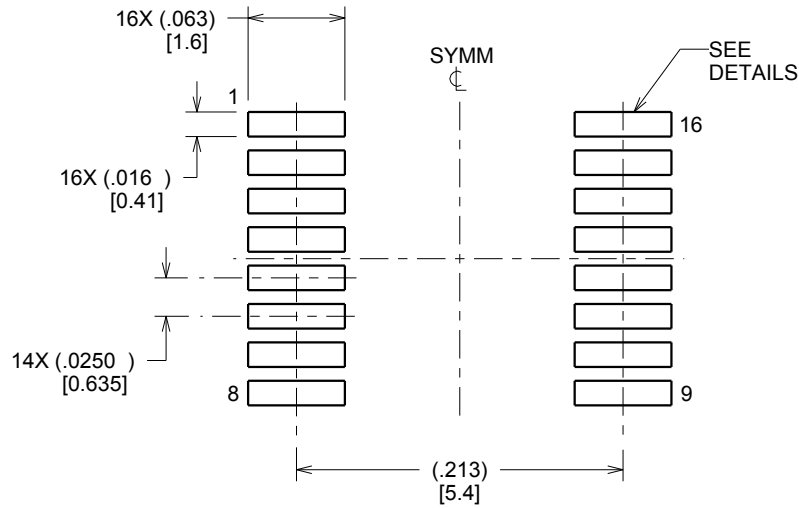
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

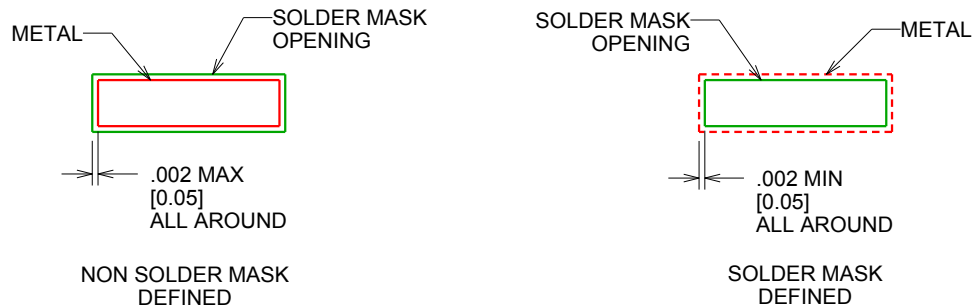
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

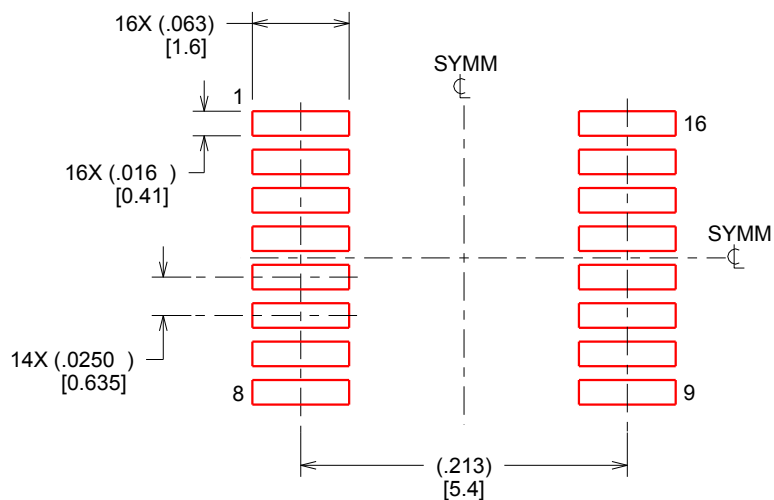
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

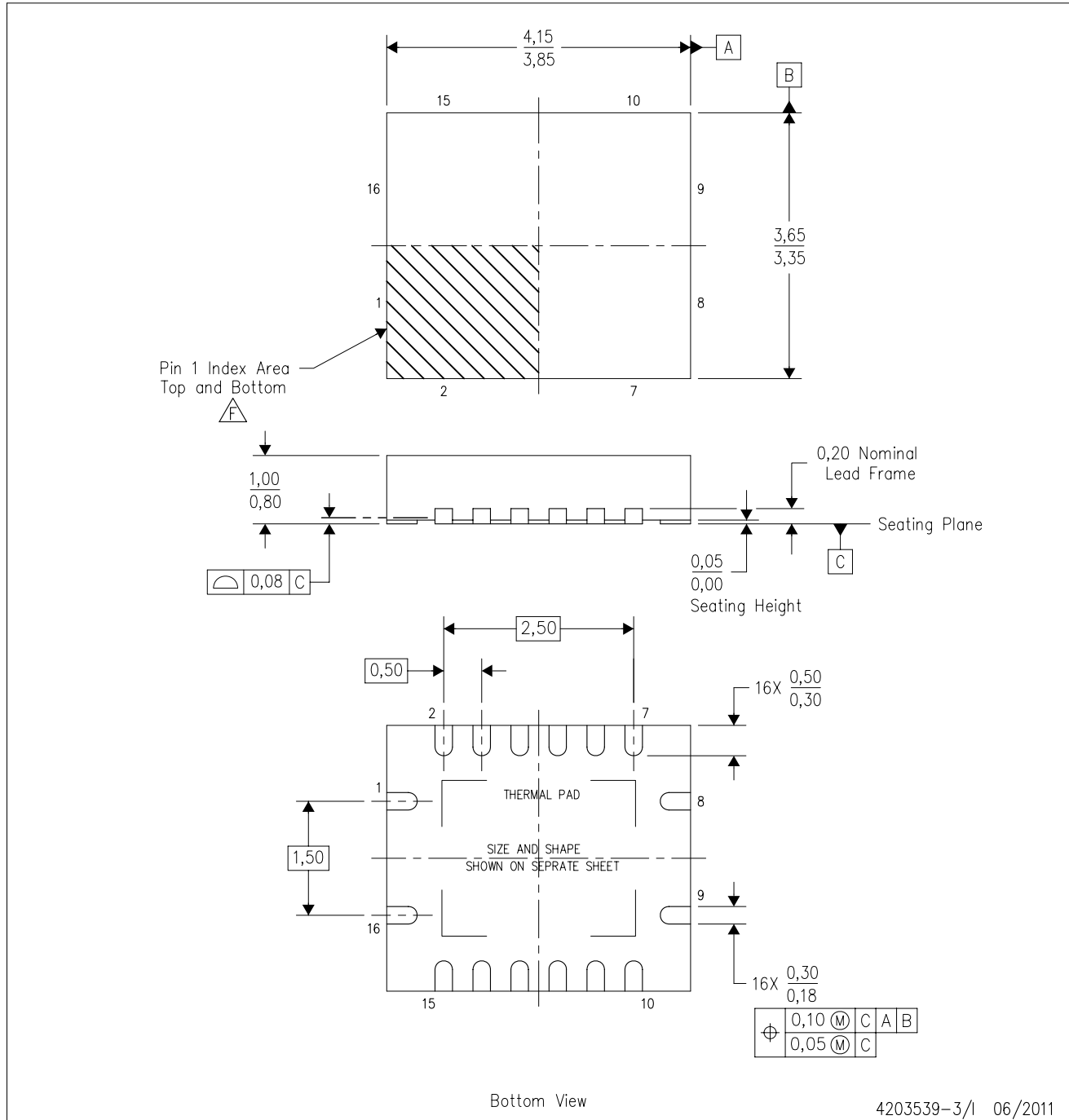
4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

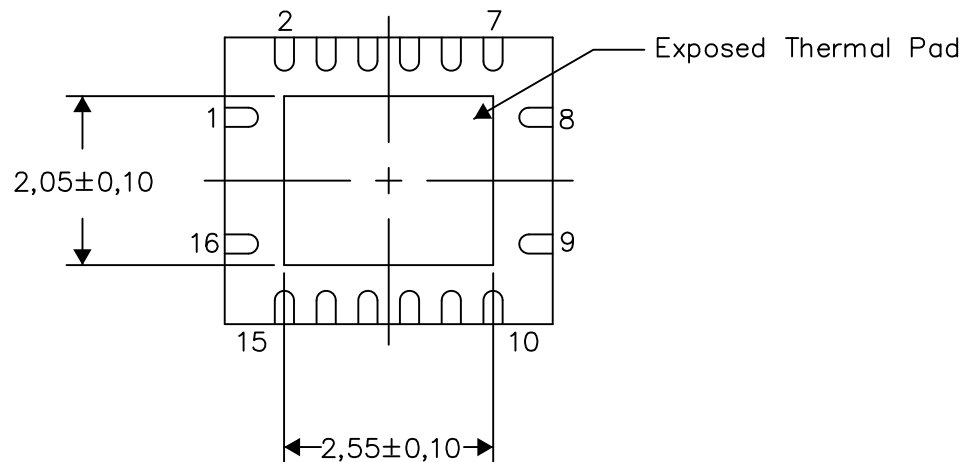
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

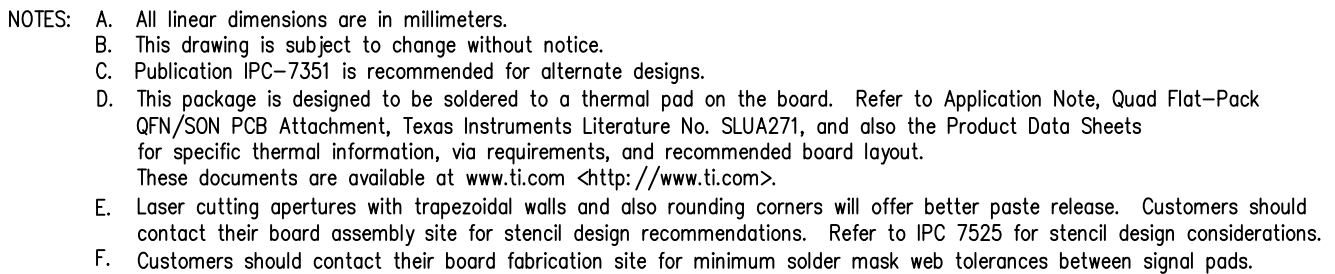


Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



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