TS3A24157 0.65-Ω 2-Channel SPDT Analog Switch 2-Channel 2:1 Multiplexer and Demultiplexer

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.65-Ω Maximum)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion
- 1.65-V to 3.6-V Single-Supply Operation
- Bidirectional Signal Paths
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

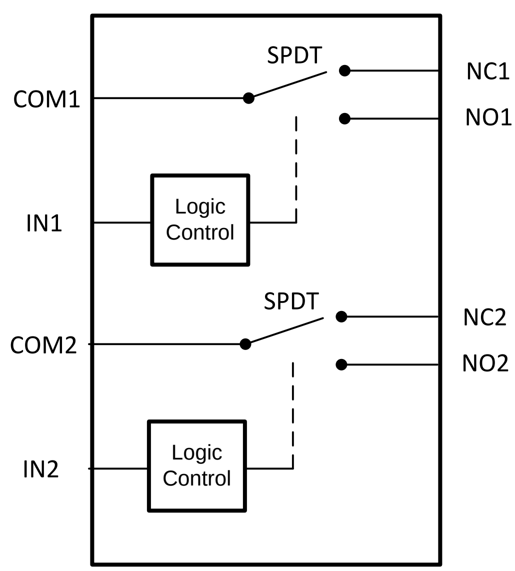
The TS3A24157 is a bidirectional, 2-channel, single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transfer of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very-low power. These features make this device suitable for portable audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A24157	UQFN (10)	1.50 mm × 2.00 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

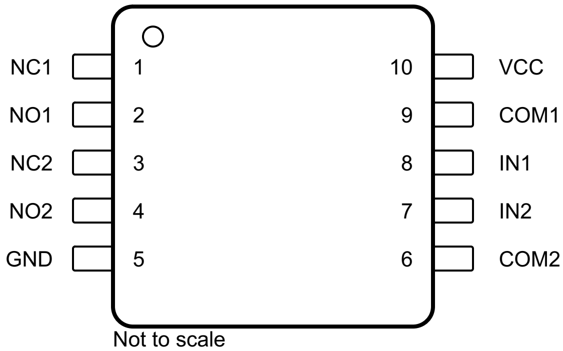
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2007) to Revision B — **Page**

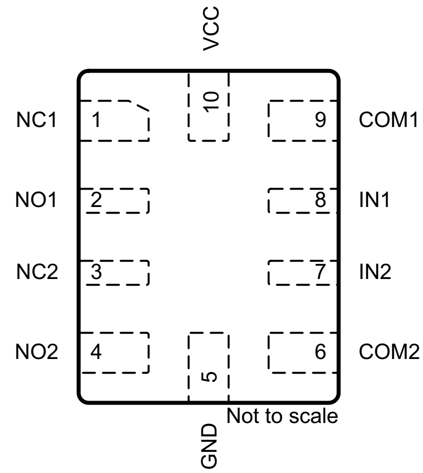
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet 1
- Deleted *Summary of Characteristics* table 1
- Changed V_+ pin name to VCC 3
- Added *Thermal Information* table 4

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



RSE Package
10-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC1	I/O	Normally closed signal path
2	NO1	I/O	Normally open signal path
3	NC2	I/O	Normally closed signal path
4	NO2	I/O	Normally open signal path
5	GND	—	Ground
6	COM2	I/O	Common signal path
7	IN2	I	Digital control to connect COM2 to NO2 or NC2
8	IN1	I	Digital control to connect COM1 to NO1 or NC1
9	COM1	I/O	Common signal path
10	VCC	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage		–0.5	3.6	V
Analog signal voltage(4)		–0.5	V_{CC} + 0.5	V
Digital input voltage		–0.5	3.6	V
Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50	50	mA
ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–300	300	mA
ON-state peak switch current(5)	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–500	500	mA
Digital input clamp current	V_{IN} < 0	–50		mA
Continuous current through VCC			100	mA
Continuous current through GND		–100		mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(4) This value is limited to 5.5 V (maximum).
(5) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{NC}	Analog signal voltage	NC1, NC2	0	V_{CC}	V
V_{NO}		NO1, NO2	0	V_{CC}	
V_{COM}		COM1, COM2	0	V_{CC}	
V_{IN}	Digital input voltage		0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS3A24157		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.5	160.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.5	77.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.2	82.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	4.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.8	82.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 3-V Supply

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ANALOG SWITCH								
r_{PEAK}	Peak ON resistance	0 ≤ (V_{NC} or V_{NO}) ≤ V_{CC}, V_{CC} = 2.7 V, I_{COM} = –100 mA, Switch ON, See Figure 10		T_A = 25°C		0.5	0.65	Ω
				–40°C ≤ T_A ≤ 85°C			0.75	
r_{ON}	ON-state resistance	V_{NC} or V_{NO} = 2 V, V_{CC} = 2.7 V, I_{COM} = –100 mA, Switch ON, See Figure 10		T_A = 25°C		0.45	0.6	Ω
				–40°C ≤ T_A ≤ 85°C			0.65	
Δr_{ON}	ON-state resistance match between channels	V_{NC} or V_{NO} = 2 V or 0.8 V, V_{CC} = 2.7 V, I_{COM} = –100 mA, Switch ON, See Figure 10		T_A = 25°C		0.05	0.07	Ω
				–40°C ≤ T_A ≤ 85°C			0.08	
$r_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 2.7 V, I_{COM} = –100 mA, Switch ON, See Figure 10	0 ≤ (V_{NC} or V_{NO}) ≤ V_{CC}			0.025		Ω
			V_{NC} or V_{NO} = 2 V or 0.8 V	T_A = 25°C		0.01	0.04	
				–40°C ≤ T_A ≤ 85°C			0.1	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC and NO OFF leakage current	V_{NC} or V_{NO} = 1 V and V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V and V_{COM} = 1 V; V_{CC} = 3.6 V, Switch OFF, See Figure 11		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–250		250	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC and NO ON leakage current	V_{NC} or V_{NO} = 1 V or 3 V, V_{COM} = Open, V_{CC} = 3.6 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V or 3 V, V_{CC} = 3.6 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
DIGITAL CONTROL INPUTS (IN1, IN2)(1)								
V_{IH}	Input logic high	2.7 V ≤ V_{CC} ≤ 3.6 V, –40°C ≤ T_A ≤ 85°C			1.4			V
V_{IL}	Input logic low	2.7 V ≤ V_{CC} ≤ 3.6 V, –40°C ≤ T_A ≤ 85°C					0.5	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 3.6 V or GND, V_{CC} = 3.6 V		T_A = 25°C	–50	5	50	nA
				–40°C ≤ T_A ≤ 85°C	–150		150	
DYNAMIC								
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 3 V, T_A = 25°C			20	35	ns
			2.7 V ≤ V_{CC} ≤ 3.6 V, –40°C ≤ T_A ≤ 85°C				40	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 3 V, T_A = 25°C			12	25	ns
			2.7 V ≤ V_{CC} ≤ 3.6 V, –40°C ≤ T_A ≤ 85°C				30	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 15	V_{CC} = 3 V, T_A = 25°C		1	10	25	ns
			2.7 V ≤ V_{CC} ≤ 3.6 V, –40°C ≤ T_A ≤ 85°C		0.5		30	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 19				8.75		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC and NO OFF capacitance	(V_{NC} or V_{NO}) = V_{CC} or GND, Switch OFF, See Figure 13				50		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC and NO ON capacitance	(V_{NC} or V_{NO}) = V_{CC} or GND, Switch ON, See Figure 13				140		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON, See Figure 13				140		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND, See Figure 13				2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, See Figure 16				50		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, See Figure 17				–72		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, See Figure 18				–72		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, See Figure 20				0.005%		
SUPPLY								
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND, V_{CC} = 3.6 V		T_A = 25°C		15	200	nA
				–40°C ≤ T_A ≤ 85°C			1200	

(1) All unused digital inputs of the device must be held at V_{CC}or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.6 Electrical Characteristics: 2.5-V Supply

V_{CC} = 2.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ANALOG SWITCH								
r_{PEAK}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, V_{CC} = 2.3 V, I_{COM} = –8 mA, Switch ON, See Figure 10		T_A = 25°C		0.55	0.75	Ω
				–40°C ≤ T_A ≤ 85°C			0.9	
r_{ON}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, V_{CC} = 2.3 V, I_{COM} = –8 mA, Switch ON, See Figure 10		T_A = 25°C		0.56	0.75	Ω
				–40°C ≤ T_A ≤ 85°C			0.85	
Δr_{ON}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V or 0.8 V, V_{CC} = 2.3 V, I_{COM} = –8 mA, Switch ON, See Figure 10		T_A = 25°C		0.1	0.15	Ω
				–40°C ≤ T_A ≤ 85°C			0.15	
$r_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 2.3 V, I_{COM} = –8 mA, Switch ON, See Figure 10	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}			0.1	0.15	Ω
			V_{NO} or V_{NC} = 0.8 V or 1.8 V	T_A = 25°C			0.17	
				–40°C ≤ T_A ≤ 85°C			0.2	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC and NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V and V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V and V_{COM} = 0.5 V; V_{CC} = 2.7 V, Switch OFF, See Figure 11		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–250		250	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC and NO ON leakage current	V_{NC} or V_{NO} = 0.5 V or 2.2 V, V_{COM} = Open, V_{CC} = 2.7 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V or 2.2 V, V_{CC} = 2.7 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
DIGITAL CONTROL INPUTS (IN1, IN2)(1)								
V_{IH}	Input logic high	2.3 V ≤ V_{CC} ≤ 2.7 V, –40°C ≤ T_A ≤ 85°C			1.25			V
V_{IL}	Input logic low	2.3 V ≤ V_{CC} ≤ 2.7 V, –40°C ≤ T_A ≤ 85°C					0.5	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 2.7 V or GND, V_{CC} = 2.7 V		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–50		50	
DYNAMIC								
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 2.5 V, T_A = 25°C			23	45	ns
			2.3 V ≤ V_{CC} ≤ 2.7 V, –40°C ≤ T_A ≤ 85°C				50	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 2.5 V, T_A = 25°C			17	27	ns
			2.3 V ≤ V_{CC} ≤ 2.7 V, –40°C ≤ T_A ≤ 85°C				30	
t_{BBM}	Break-before- make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 15	V_{CC} = 2.5 V, T_A = 25°C		2	14	30	ns
			2.3 V ≤ V_{CC} ≤ 2.7 V, –40°C ≤ T_A ≤ 85°C		1		35	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 19				8		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC and NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF, See Figure 13				50		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC and NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON, See Figure 13				140		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON, See Figure 13				140		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND, See Figure 13				2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, See Figure 16				50		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, See Figure 17				–72		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, See Figure 18				–72		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, See Figure 20				0.006%		
SUPPLY								
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND, V_{CC} = 2.7 V		T_A = 25°C		10	150	nA
				–40°C ≤ T_A ≤ 85°C			700	

(1) All unused digital inputs of the device must be held at V_{CC}or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.7 Electrical Characteristics: 1.8-V Supply

V_{CC} = 1.8 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ANALOG SWITCH								
r_{PEAK}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, V_{CC} = 1.65 V, I_{COM} = –2 mA, Switch ON, See Figure 10		T_A = 25°C	0.8		1.25	Ω
				–40°C ≤ T_A ≤ 85°C			1.4	
r_{ON}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, V_{CC} = 1.65 V, I_{COM} = –2 mA, Switch ON, See Figure 10		T_A = 25°C	0.6		0.95	Ω
				–40°C ≤ T_A ≤ 85°C			1	
Δr_{ON}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.6 V or 1.5 V, V_{CC} = 1.65 V, I_{COM} = –2 mA, Switch ON, See Figure 10		T_A = 25°C	0.1		0.15	Ω
				–40°C ≤ T_A ≤ 85°C			0.15	
$r_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 1.65 V, I_{COM} = –2 mA, Switch ON, See Figure 10	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}			0.35	0.13	Ω
			V_{NO} or V_{NC} = 0.6 V or 1.5 V	T_A = 25°C		0.05		
				–40°C ≤ T_A ≤ 85°C			0.2	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC and NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V and V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V and V_{COM} = 0.3 V; V_{CC} = 1.65, Switch OFF, See Figure 11		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–250		250	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC and NO ON leakage current	V_{NC} or V_{NO} = 0.3 V or 1.65 V, V_{COM} = Open, V_{CC} = 1.95 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V or 1.65 V, V_{CC} = 1.95 V, Switch ON, See Figure 12		T_A = 25°C	–50		50	nA
				–40°C ≤ T_A ≤ 85°C	–400		400	
DIGITAL CONTROL INPUTS (IN1, IN2)(1)								
V_{IH}	Input logic high	1.65 V ≤ V_{CC} ≤ 1.95 V, –40°C ≤ T_A ≤ 85°C			1			V
V_{IL}	Input logic low	1.65 V ≤ V_{CC} ≤ 1.95 V, –40°C ≤ T_A ≤ 85°C					0.4	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 1.95 V or GND, V_{CC} = 1.95 V		25°C		0	50	nA
				–40°C ≤ T_A ≤ 85°C			150	
DYNAMIC								
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 1.8 V, T_A = 25°C			33	75	ns
			1.65 V ≤ V_{CC} ≤ 1.95 V, –40°C ≤ T_A ≤ 85°C				80	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 14	V_{CC} = 1.8 V, T_A = 25°C			24	35	ns
			1.65 V ≤ V_{CC} ≤ 1.95 V, –40°C ≤ T_A ≤ 85°C				40	
t_{BBM}	Break-before- make time	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω, C_L = 35 pF, See Figure 15	V_{CC} = 1.8 V, T_A = 25°C		2	20	40	ns
			1.65 V ≤ V_{CC} ≤ 1.95 V, –40°C ≤ T_A ≤ 85°C		1		50	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 19				4		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC and NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF, See Figure 13				50		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC and NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON, See Figure 13				140		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON, See Figure 13				140		pF
C_I	Digital input capacitance	V_{IN} = V_{CC} or GND, See Figure 13				2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, See Figure 16				48		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, See Figure 17				–73		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, See Figure 18				–72		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, See Figure 20				0.005%		
Supply								
I_{CC}	Positive supply current	V_{IN} = V_{CC} or GND, V_{CC} = 1.95 V		T_A = 25°C		10	100	nA
				–40°C ≤ T_A ≤ 85°C			600	

(1) All unused digital inputs of the device must be held at V_{CC}or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.8 Typical Characteristics

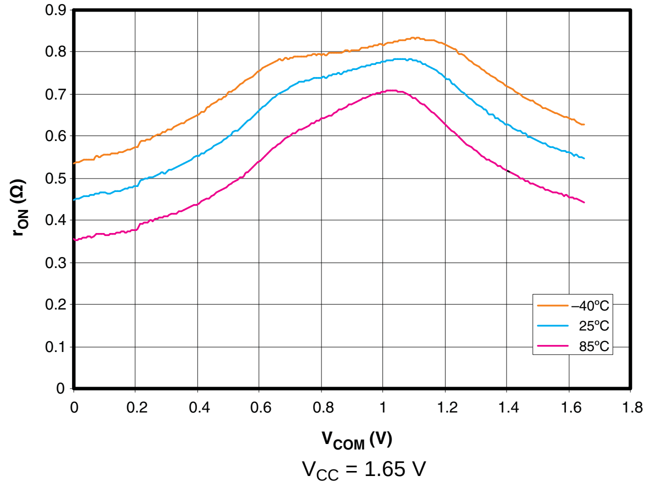


Figure 1. r_{ON} vs V_{COM}

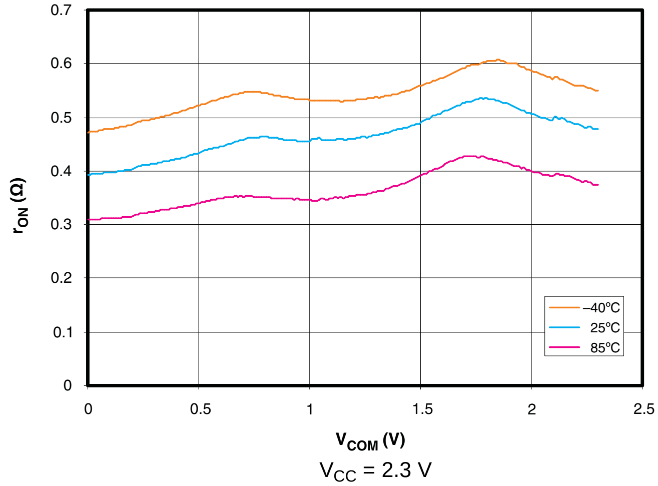


Figure 2. r_{ON} vs V_{COM}

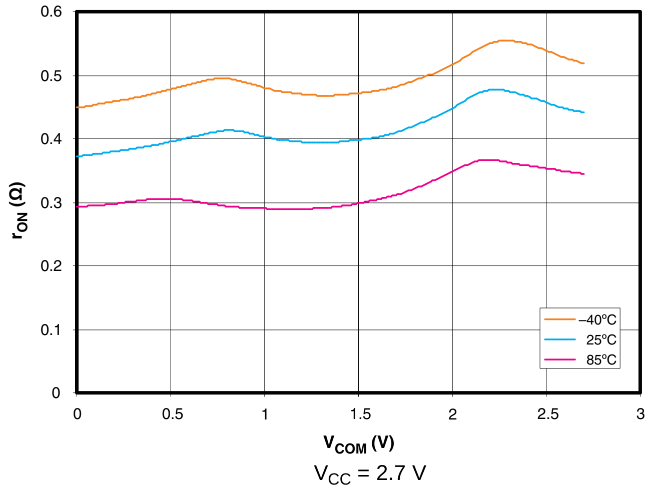


Figure 3. r_{ON} vs V_{COM}

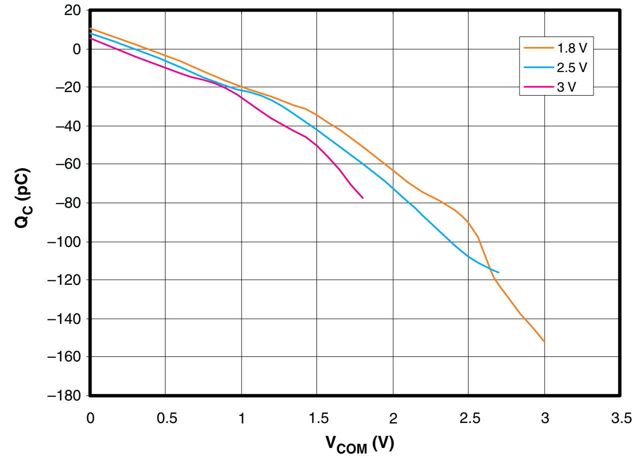


Figure 4. Charge Injection vs V_{COM}

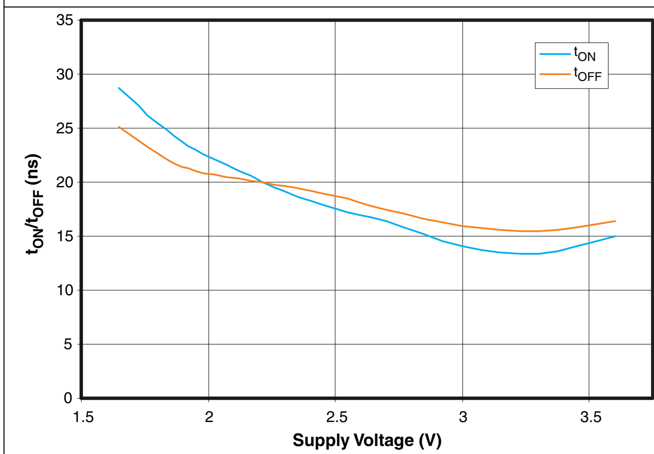


Figure 5. t_{ON} and t_{OFF} vs Supply Voltage

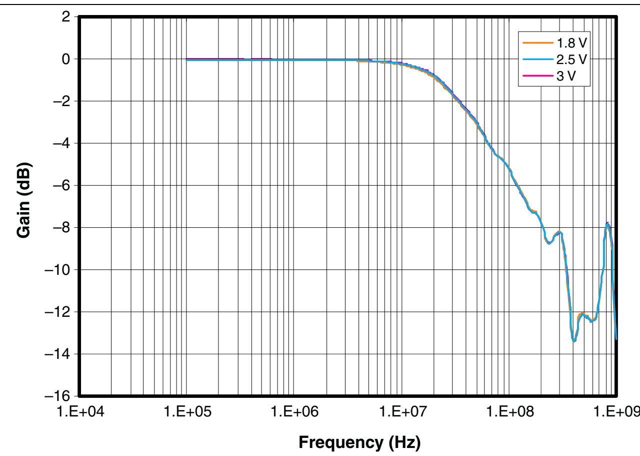


Figure 6. Bandwidth

Typical Characteristics (continued)

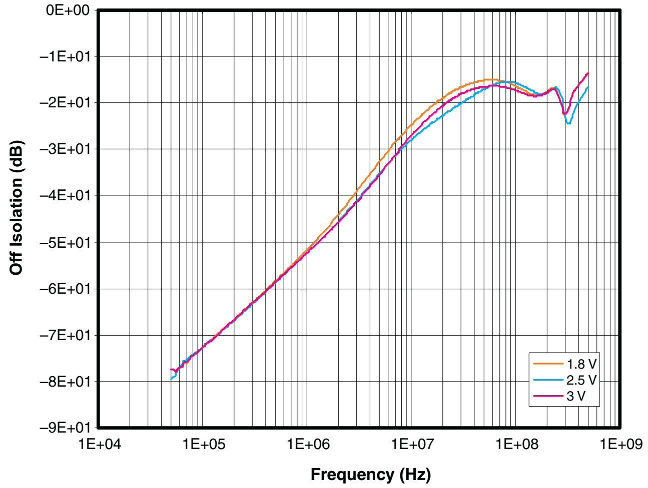


Figure 7. OFF Isolation

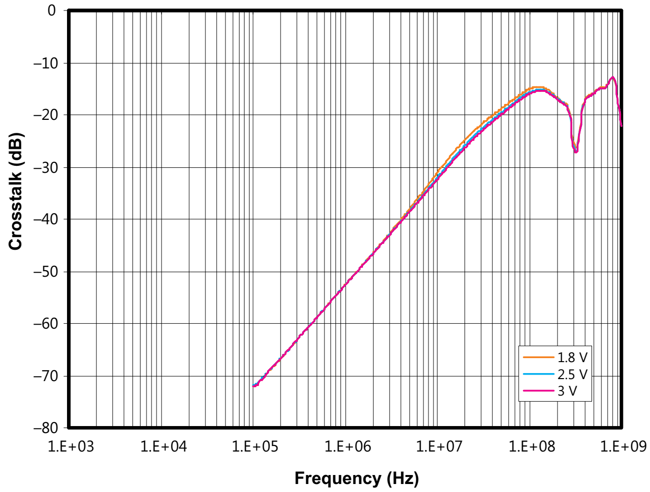


Figure 8. Crosstalk

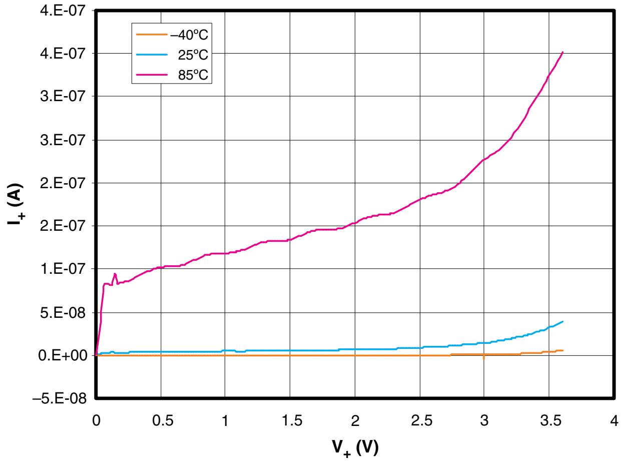


Figure 9. Power-Supply Current vs V_{CC}

7 Parameter Measurement Information

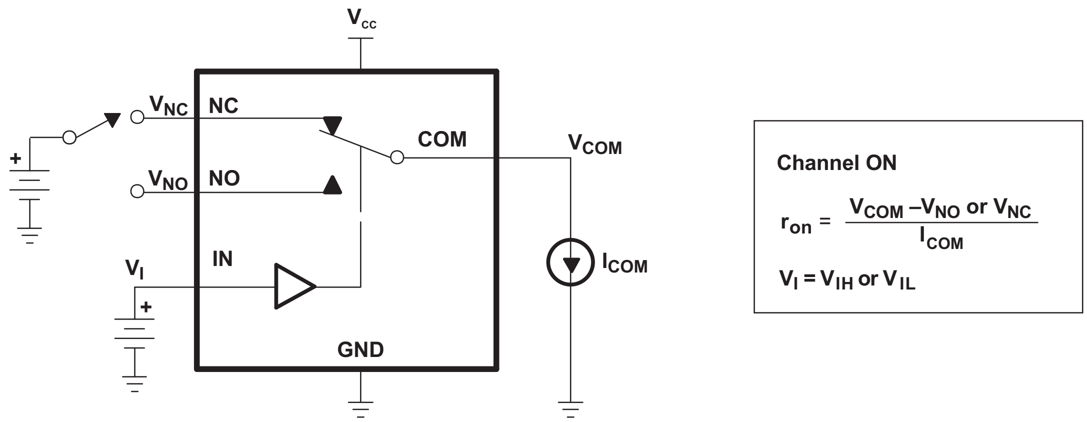
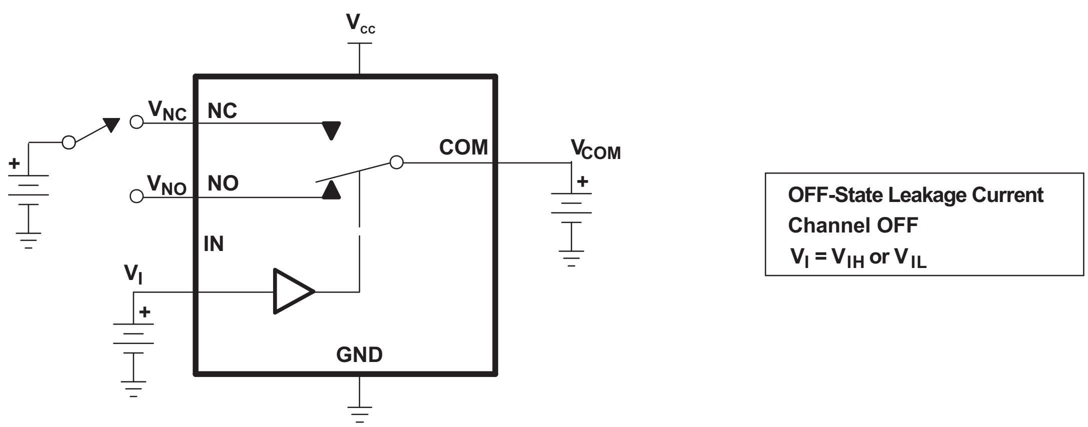
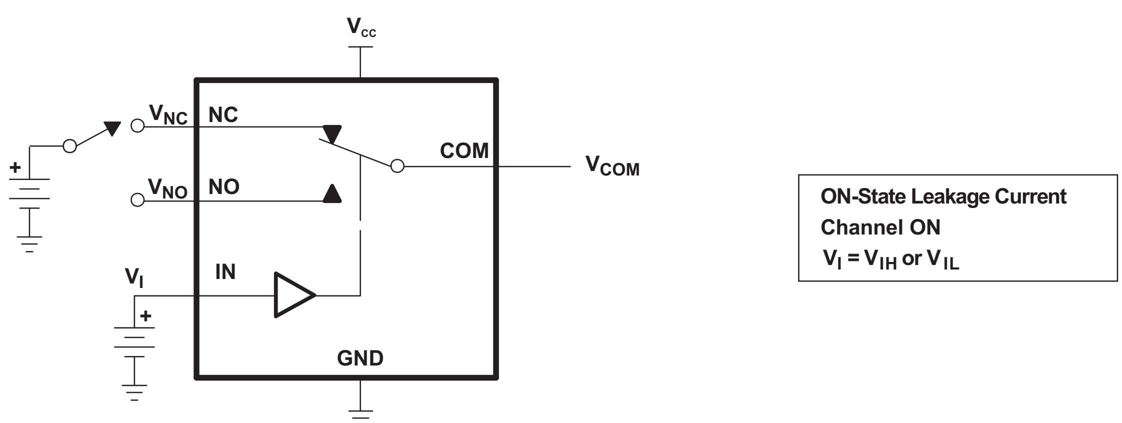


Figure 10. ON-State Resistance



$I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$

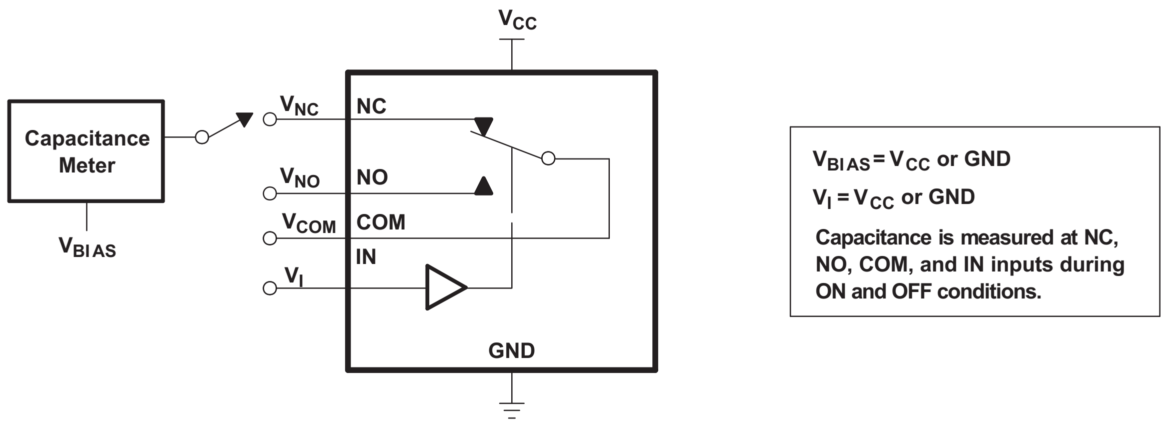
Figure 11. OFF-State Leakage Current



$I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$

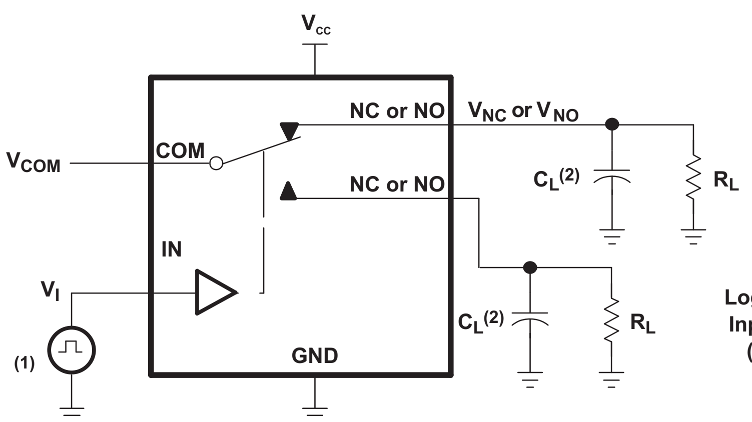
Figure 12. ON-State Leakage Current

Parameter Measurement Information (continued)

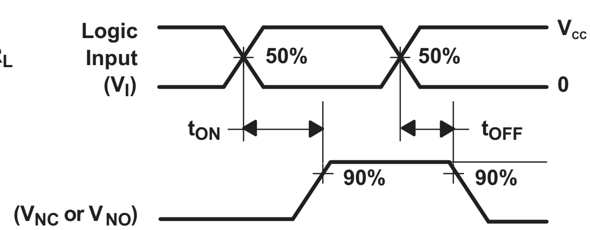


C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$

Figure 13. Capacitance



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{cc}
t_{OFF}	50 Ω	35 pF	V_{cc}

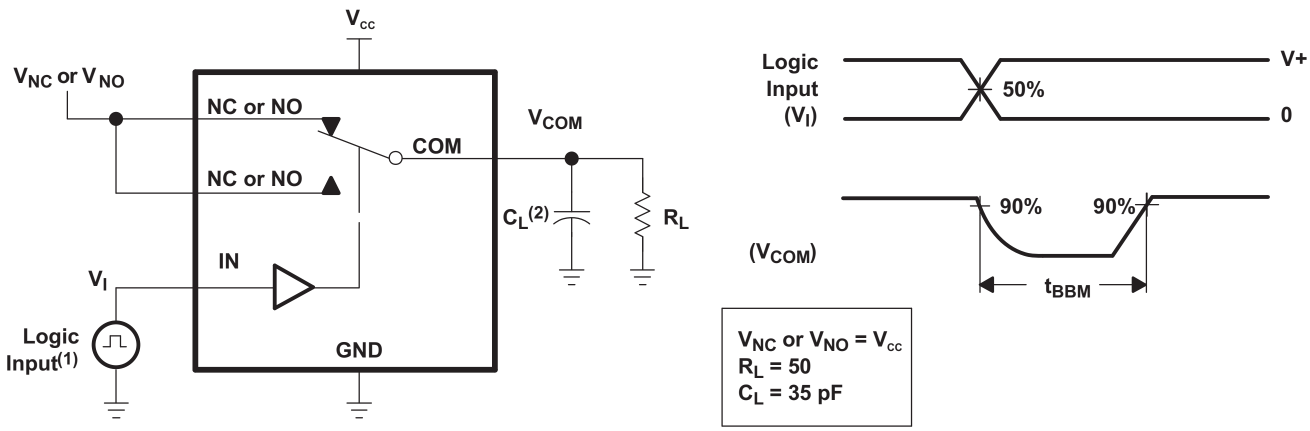


(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 14. Turnon and Turnoff Time

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics:

- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

A. C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time

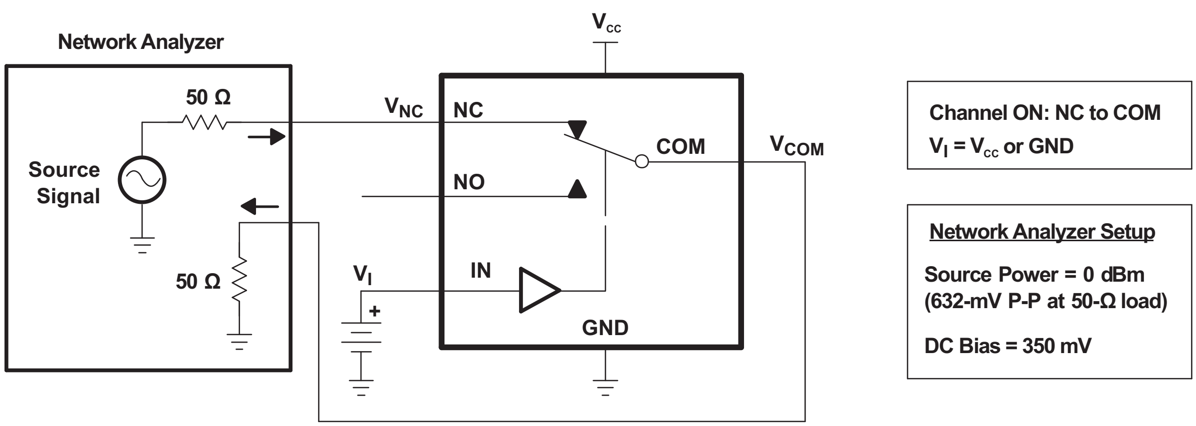


Figure 16. Bandwidth

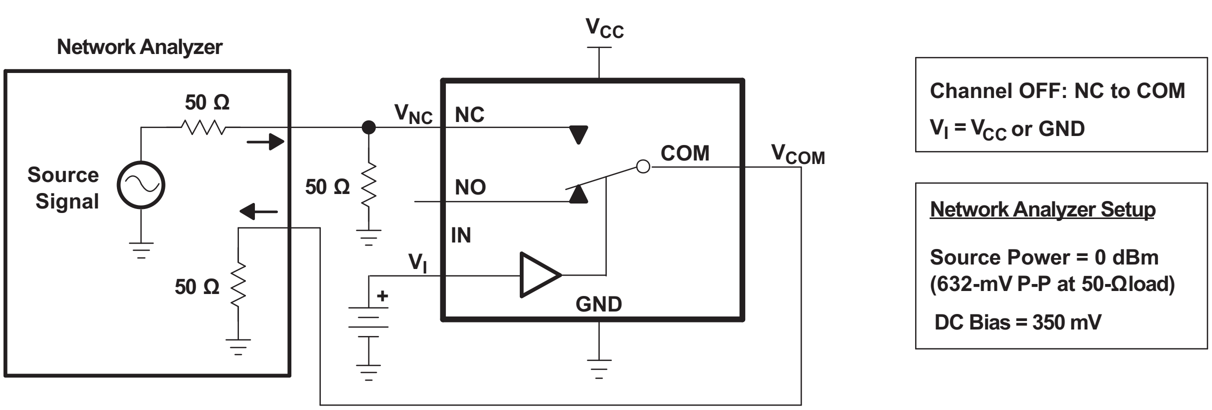


Figure 17. OFF Isolation

Parameter Measurement Information (continued)

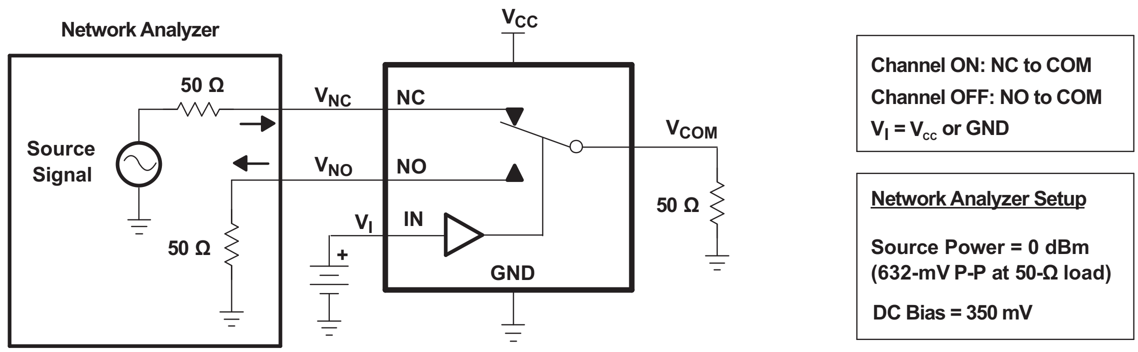
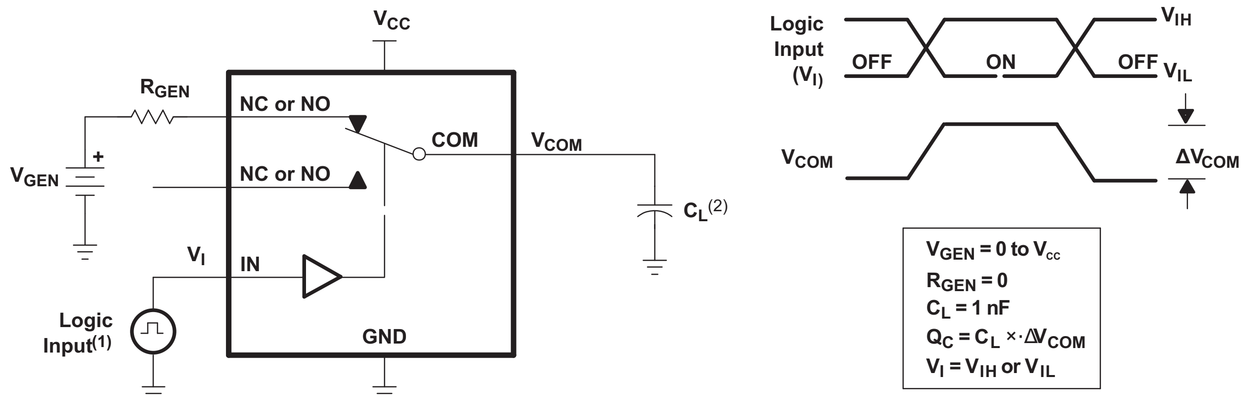


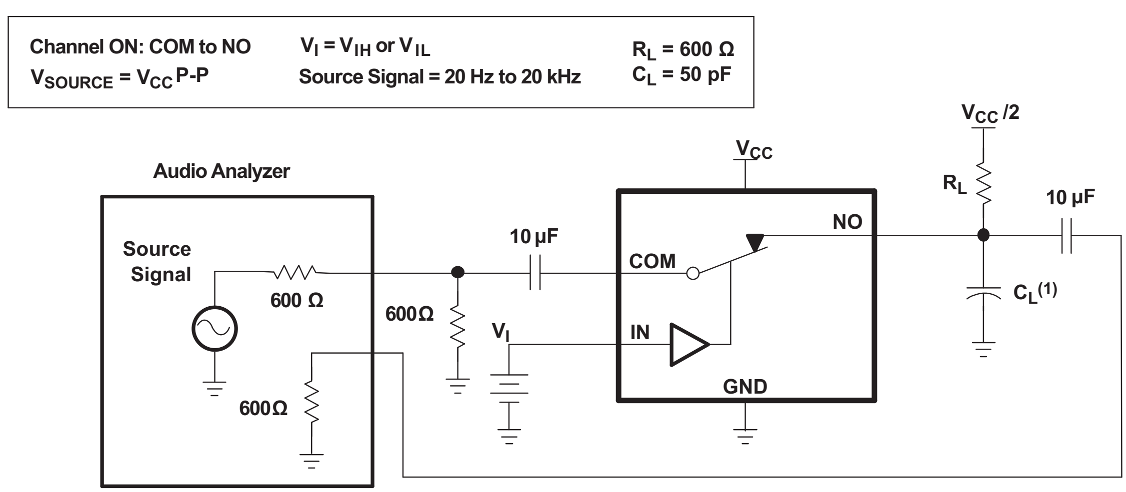
Figure 18. Crosstalk



(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 19. Charge Injection



(1) C_L includes probe and jig capacitance.

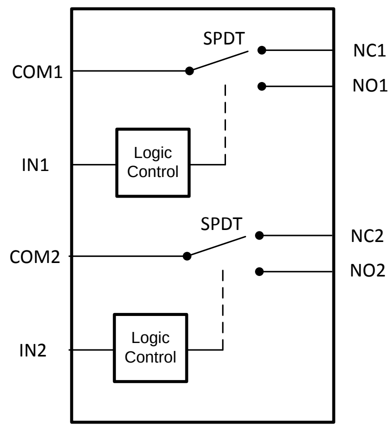
Figure 20. Total Harmonic Distortion

8 Detailed Description

8.1 Overview

The TS3A24157 is a bidirectional, 2-channel, single-pole double-throw (SPDT) analog switch. This switch offers low ON-state resistance and excellent THD performance which makes it great for interfacing with an ADC.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3A24157 is a bidirectional device that has two single-pole, double-throw switches. The two channels of the switch are controlled independently by two digital signals; one digital control for each single-pole, doublethrow switch.

8.4 Device Functional Modes

To allow signals to pass between the NC and COM pins you must set the digital control IN pin *Low*

To allow signals to pass between the NO and COM pins you must set the digital control IN pin *High*

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

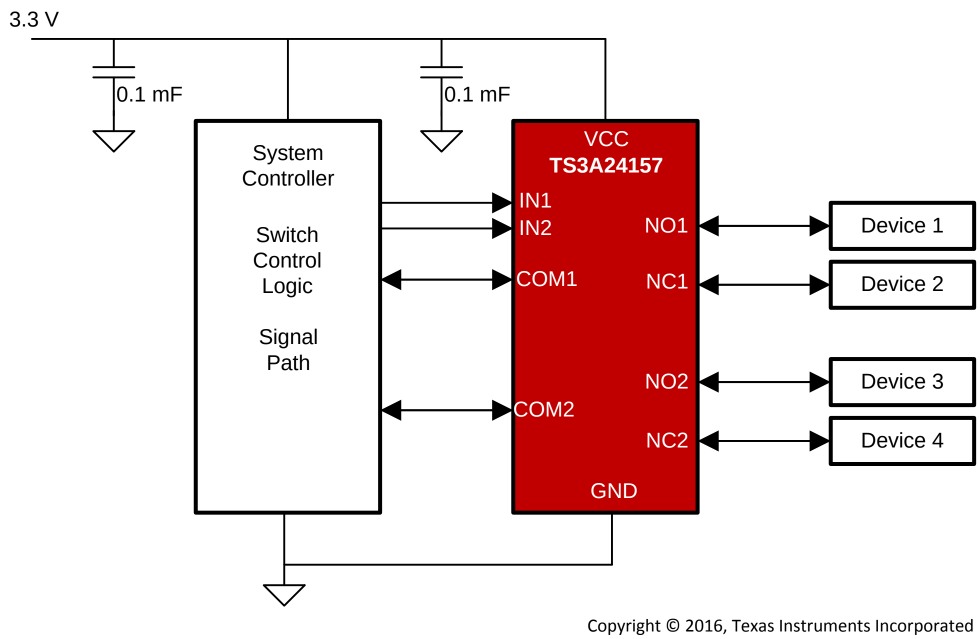


Figure 21. Typical Application Schematic

9.2.1 Design Requirements

The TS3A24157 can be properly operated without any external components.

When unused, pins COM, NC, and NO may be left floating.

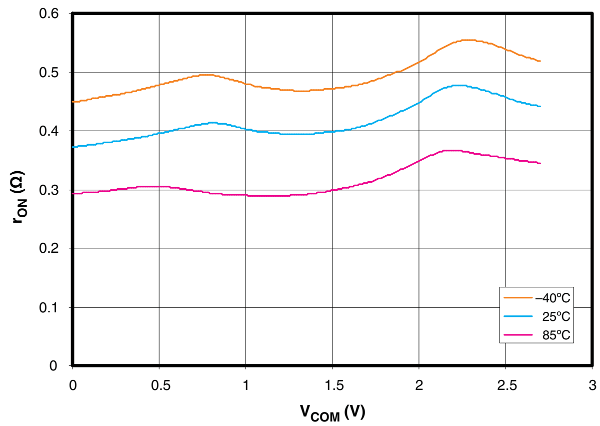
Digital control pins IN must be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

Ensure that all of the signals passing through the switch are within the ranges specified in *Recommended Operating Conditions* to ensure proper performance.

Typical Application (continued)

9.2.3 Application Curves



V_{CC} = 2.7 V

Figure 22. r_{ON} vs V_{COM}

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute-maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{CC} on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are placed as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

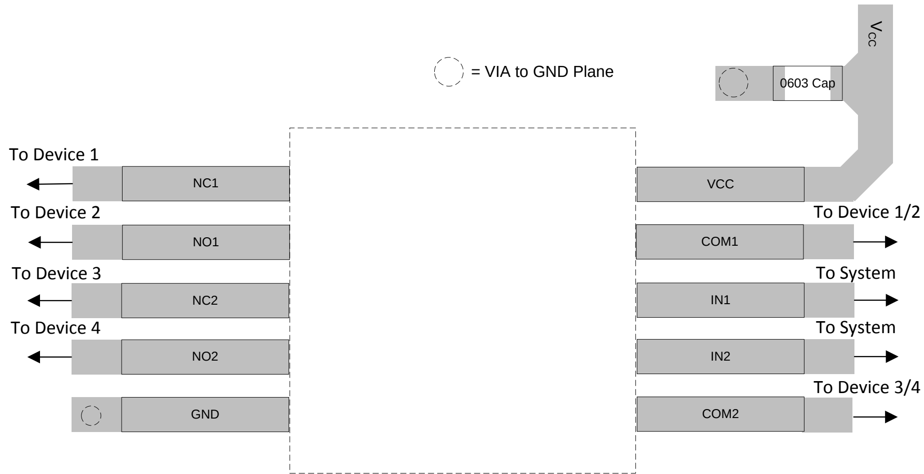


Figure 23. TS3A24157 Example Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

V_{COM} Voltage at COM.

V_{NC} Voltage at NC.

V_{NO} Voltage at NO.

r_{ON} Resistance between COM and NC or COM and NO ports when the channel is ON.

r_{PEAK} Peak ON-state resistance over a specified voltage range.

Δr_{ON} Difference of r_{ON} between channels in a specific device.

$r_{ON(FLAT)}$ Difference between the maximum and minimum value of r_{ON} in a channel over the specified range of conditions.

$I_{NC(OFF)}$ Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.

$I_{NC(PWROFF)}$ Leakage current measured at the NC port during the power-down condition (V_{CC} = 0).

$I_{NO(OFF)}$ Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions.

$I_{NO(PWROFF)}$ Leakage current measured at the NO port during the power-down condition (V_{CC} = 0).

$I_{NC(ON)}$ Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.

$I_{NO(ON)}$ Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open.

$I_{COM(ON)}$ Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open.

$I_{COM(PWROFF)}$ Leakage current measured at the COM port during the power-down condition (V_{CC} = 0).

V_{IH} Minimum input voltage for logic high for the control input (IN).

V_{IL} Maximum input voltage for logic low for the control input (IN).

V_I Voltage at the control input (IN).

I_{IH}, I_{IL} Leakage current measured at the control input (IN).

t_{ON} Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.

t_{OFF} Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.

t_{BBM} Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.

Q_C Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.

$C_{NC(OFF)}$ Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.

$C_{NO(OFF)}$ Capacitance at the NO port when the corresponding channel (NO to COM) is OFF.

Device Support (continued)

$C_{NC(ON)}$ Capacitance at the NC port when the corresponding channel (NC to COM) is ON.

$C_{NO(ON)}$ Capacitance at the NO port when the corresponding channel (NO to COM) is ON.

$C_{COM(ON)}$ Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON.

C_I Capacitance of control input (IN).

O_{ISO} OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.

X_{TALK} Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

BW Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.

THD Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.

I_{CC} Static power-supply current with the control (IN) pin at V_{CC} or GND.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A24157DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JZO, JZR)
TS3A24157DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JZO, JZR)
TS3A24157DGSRG4.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TS3A24157RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JZO
TS3A24157RSER.B	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JZO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

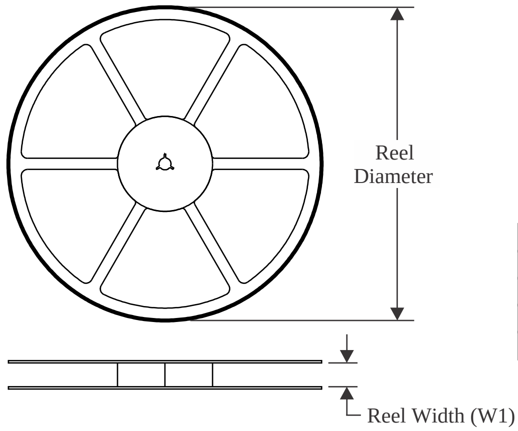
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

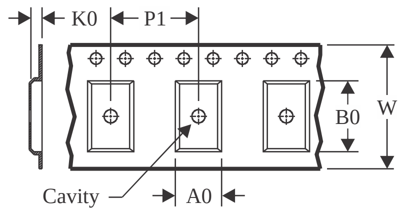
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

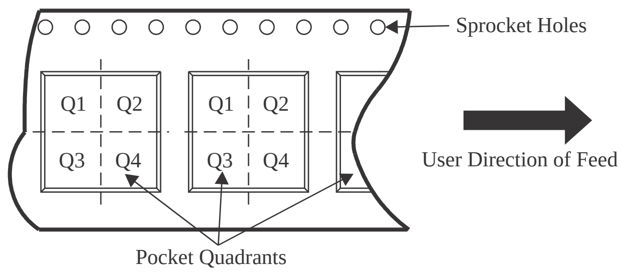


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

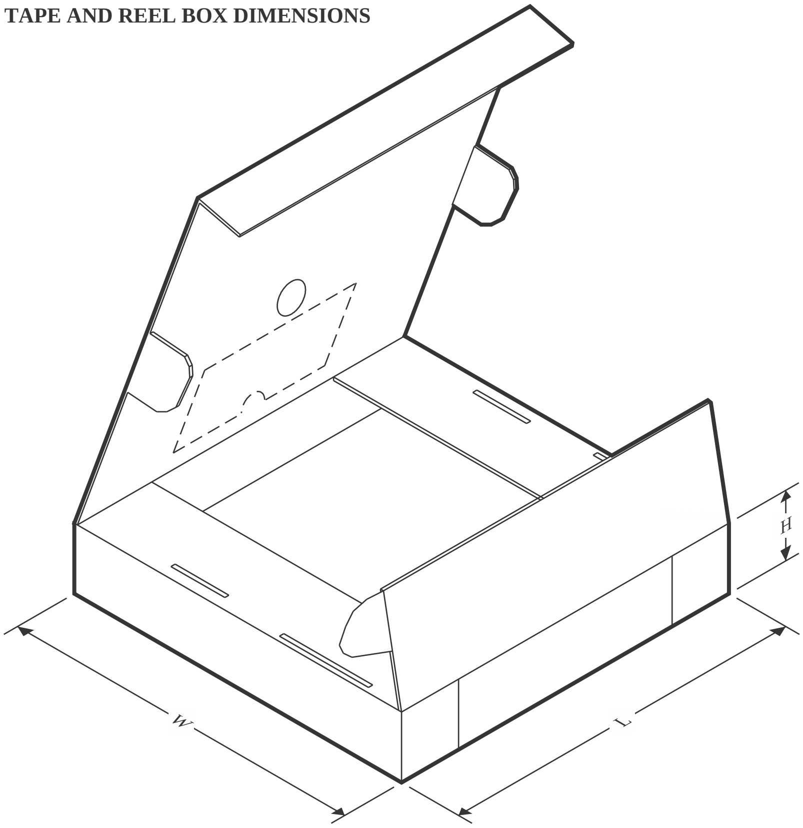
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

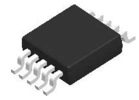
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TS3A24157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

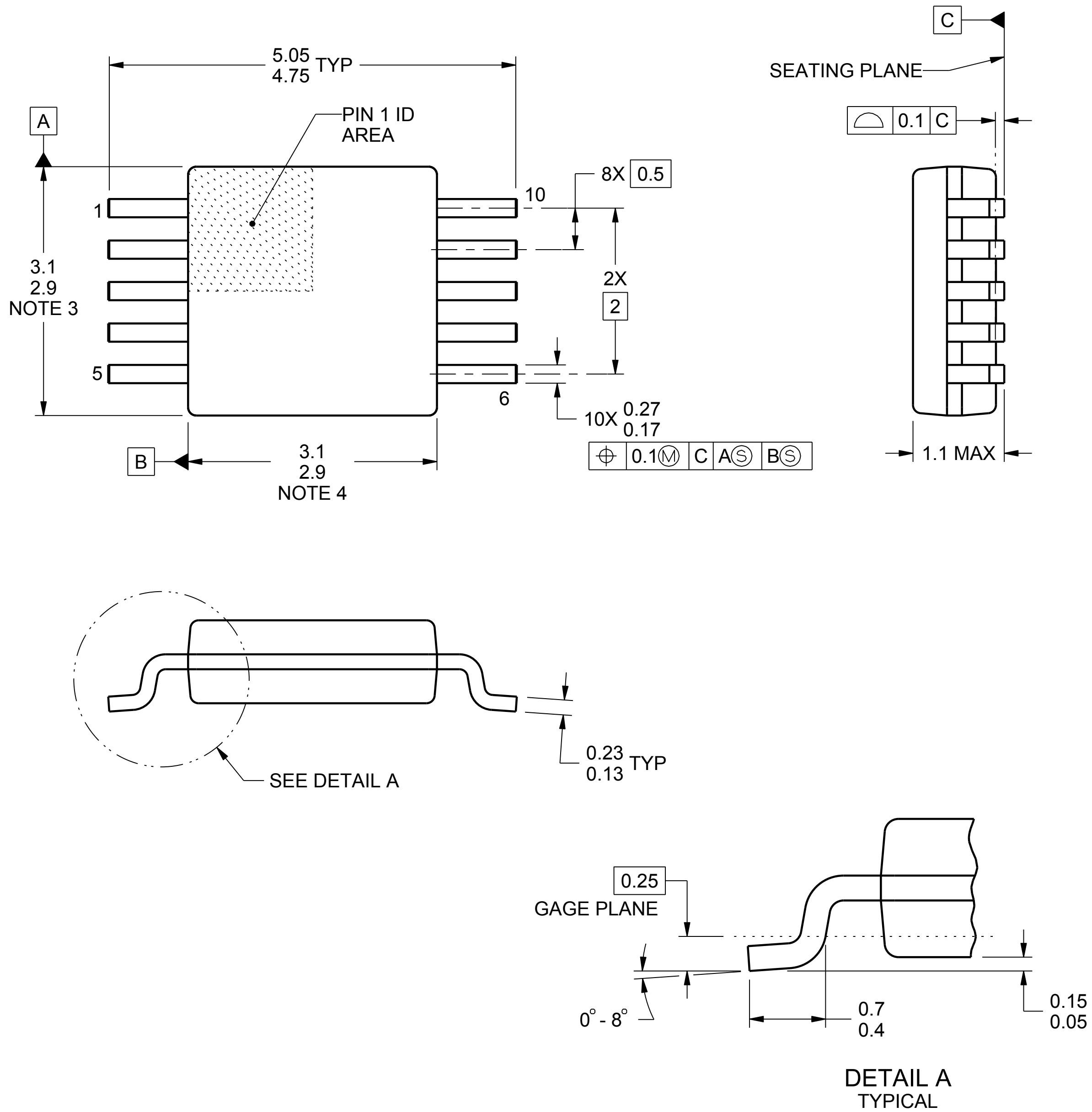
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24157DGSR	VSSOP	DGS	10	2500	346.0	346.0	35.0
TS3A24157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0



DGS0010A

VSSOP - 1.1 mm max height

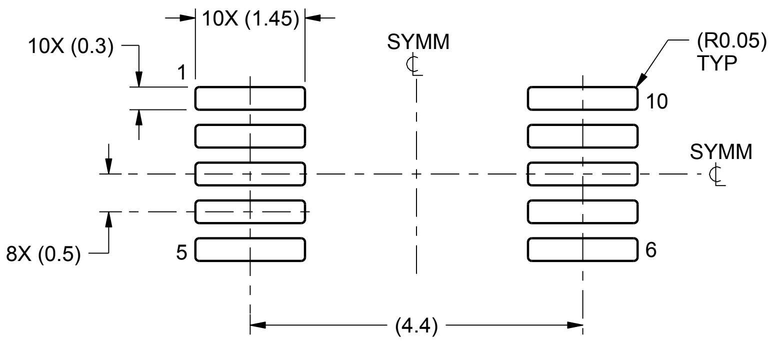
SMALL OUTLINE PACKAGE



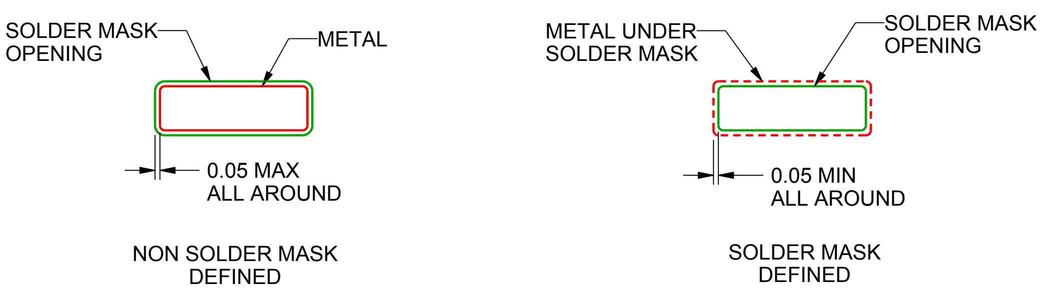
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

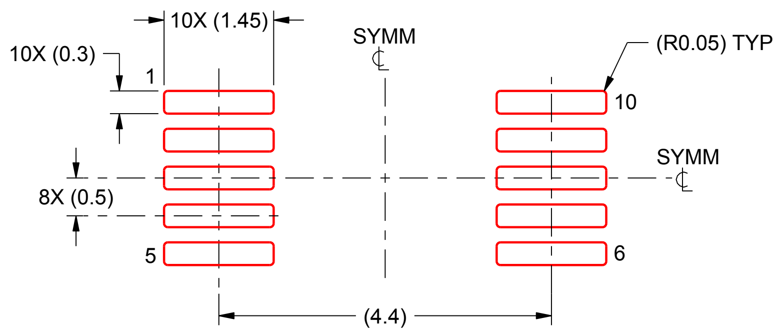


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

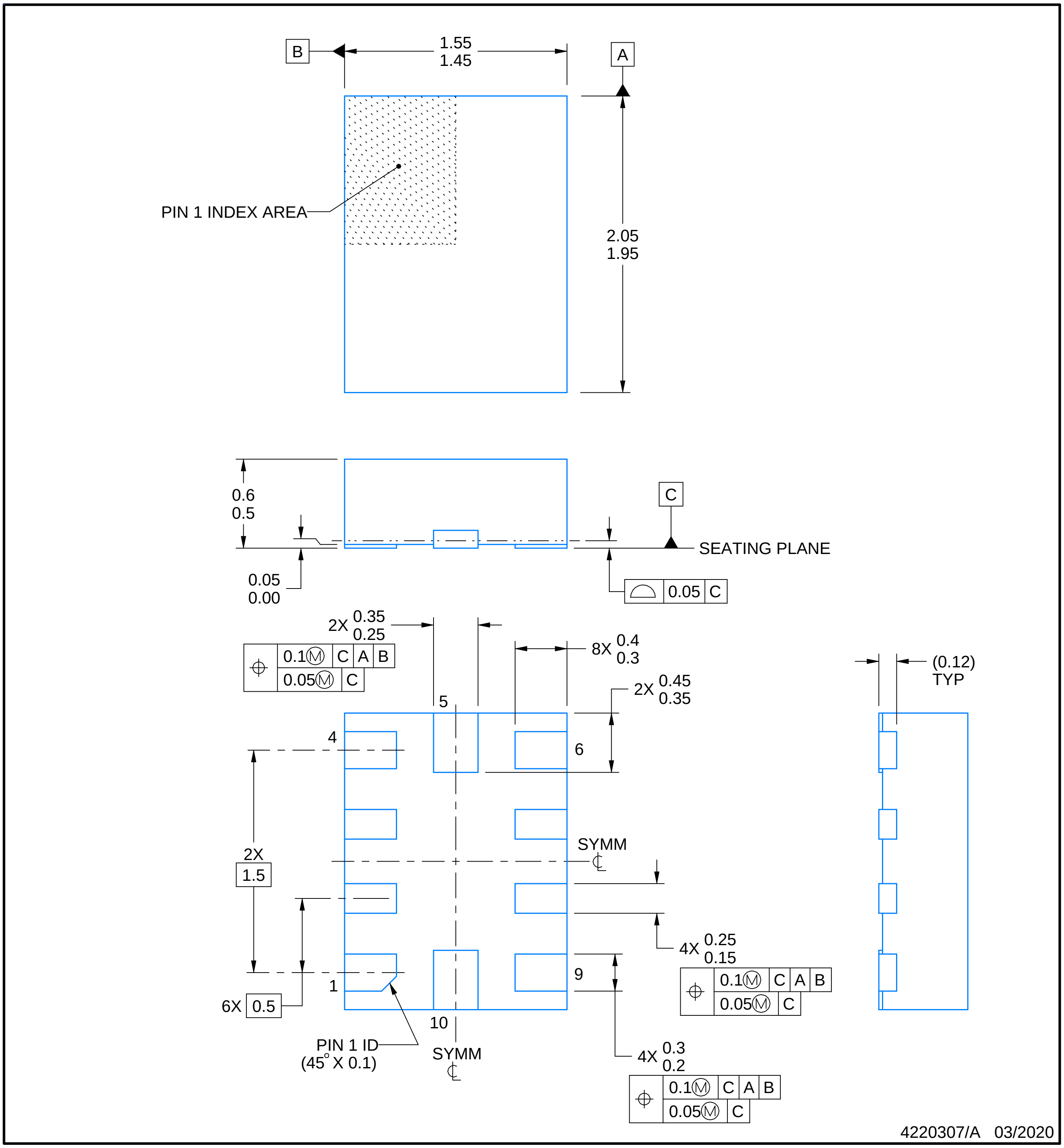
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

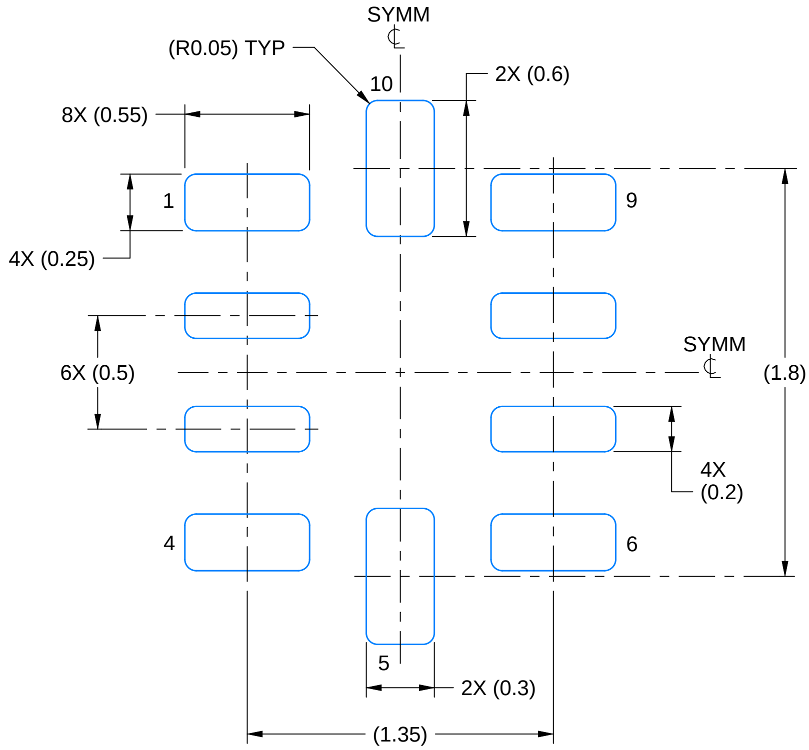
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

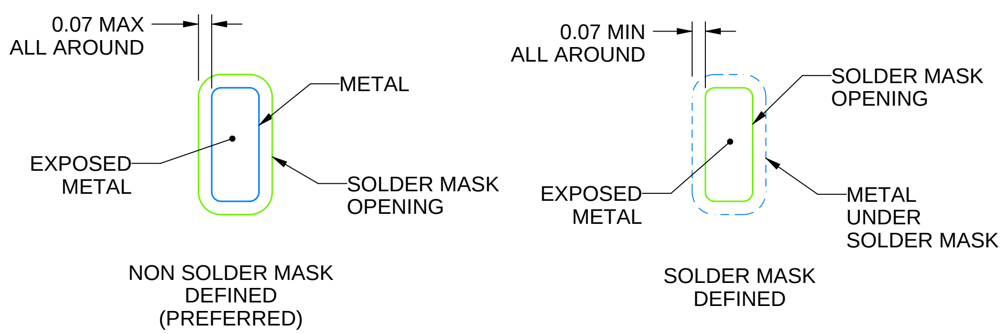


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

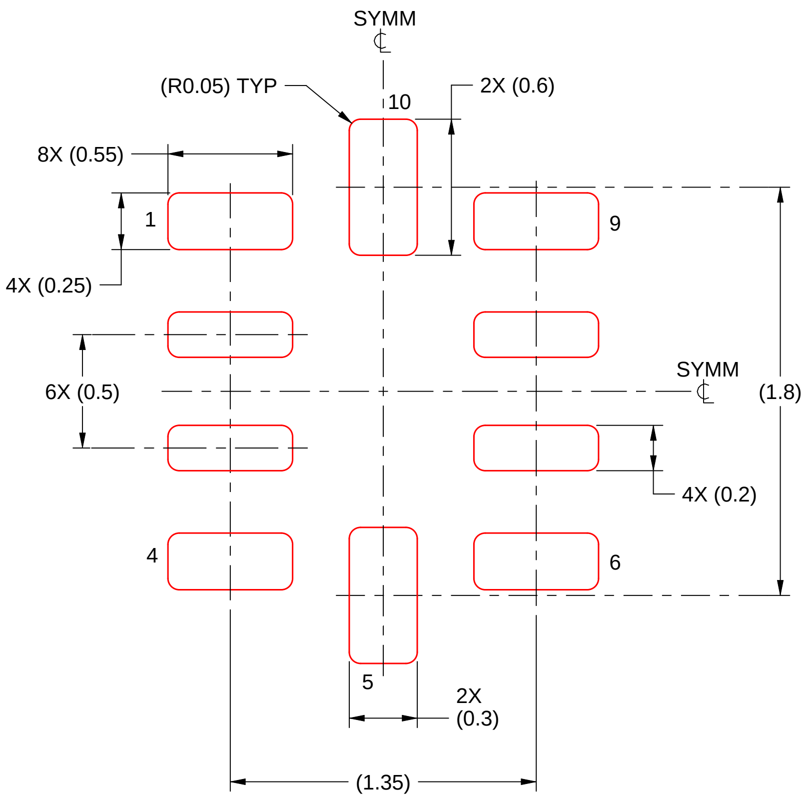


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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