

TRS232E デュアル RS-232 ドライバ / レシーバ、IEC61000-4-2 保護機能搭載

1 特長

- TIA/RS-232-F および ITU 勧告 V.28 適合またはそれを上回る性能
- 1 μ F チャージポンプコンデンサを使用して 5V 単一電源で動作
- 最大 250kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- ± 30 V の入力レベル
- 低い消費電流: 8mA (代表値)
- RS-232 バスピン用 ESD 保護機能
 - ± 15 kV 人体モデル (HBM)
 - ± 8 kV IEC 61000-4-2、接触放電
 - ± 15 kV IEC 61000-4-2、気中放電

2 アプリケーション

- TIA/RS-232-F
- [バッテリー駆動システム](#)
- 端末
- モデム
- コンピュータ

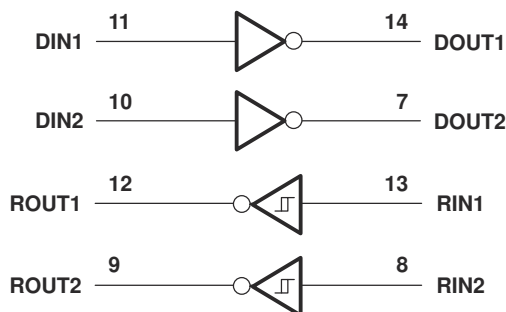
3 概要

TRS232E は、5V 単一電源から TIA/RS-232-F の電圧レベルを供給する容量性電圧発生器を内蔵したデュアルドライバ / レシーバです。各レシーバは、TIA/RS-232-F の入力を 5V の TTL/CMOS レベルに変換します。このレシーバは、標準スレッショルドが 1.3V、標準ヒステリシスが 0.5V で、 ± 30 V の入力を受け入れます。各ドライバは、TTL/CMOS 入力レベルを TIA/RS-232-F レベルに変換します。ドライバ、レシーバ、電圧発生器は、いずれもテキサス・インスツルメンツの LinASIC™ ライブラリのセルとして利用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TRS232E	SOIC (D, 16)	9.9mm × 6mm
	SOIC (DW, 16)	10.4mm × 10.3mm
	PDIP (N, 16)	19.3mm × 9.4mm
	TSSOP (PW, 16)	5mm × 6.4mm

- (1) 詳細については、[セクション 11](#) を参照してください。
 (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)



Table of Contents

1 特長	1	6 Parameter Measurement Information	7
2 アプリケーション	1	7 Detailed Description	8
3 概要	1	7.1 Device Functional Modes.....	8
4 Pin Configuration and Functions	3	8 Application and Implementation	9
5 Specifications	4	8.1 Application Information.....	10
5.1 Absolute Maximum Ratings.....	4	9 Device Documentation and Support	11
5.2 ESD Ratings.....	4	9.1 ドキュメントの更新通知を受け取る方法.....	11
5.3 Recommended Operating Conditions.....	4	9.2 サポート・リソース.....	11
5.4 Thermal Information.....	5	9.3 商標.....	11
5.5 Electrical Characteristics.....	5	9.4 静電気放電に関する注意事項.....	11
5.6 Driver Section: Electrical Characteristics.....	5	9.5 用語集.....	11
5.7 Switching Characteristics.....	5	10 Revision History	11
5.8 Receiver Section: Electrical Characteristics.....	6	11 Mechanical, Packaging, and Orderable Information	11
5.9 Switching Characteristics.....	6		

4 Pin Configuration and Functions

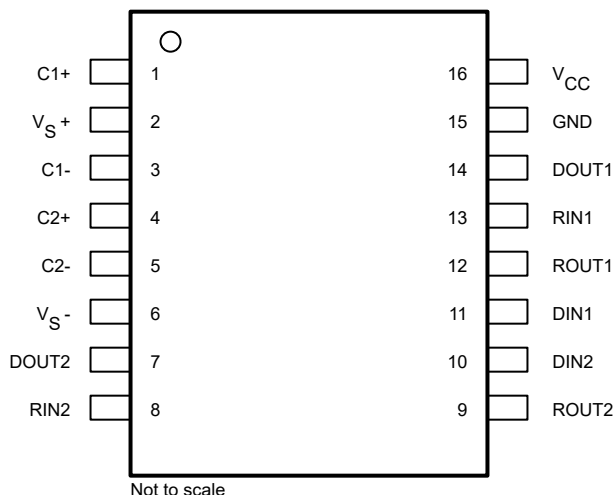


図 4-1. D, DW, N, NS or PW Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
VCC	16	—	Supply Voltage, Connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Input supply voltage range ⁽²⁾		–0.3	6	V
V _{S+}	Positive output supply voltage range		V _{CC} – 0.3	15	V
V _{S–}	Negative output supply voltage range		–0.3	–15	V
V _I	Input voltage range	Driver	–0.3	V _{CC} + 0.3	V
		Receiver		±30	
V _O	Output voltage range	DOUT	V _{S–} – 0.3	V _{S+} + 0.3	V
		ROUT	–0.3	V _{CC} + 0.3	
	Short-circuit duration	DOUT		Unlimited	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

PARAMETER	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage (DIN1, DIN2)		2			V
V _{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
T _A	Operating free-air temperature	TRS232EC	0		70	°C
		TRS232EI	–40		85	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	84.6	71.7	60.6	107.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	38.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.2	36.8	40.6	53.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	10.4	13.	27.5	3.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see ⁽¹⁾ and [8-1](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC} Supply current	V _{CC} = 5.5V, All outputs open, T _A = 25°C		8	10	mA

(1) Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.6 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	DOUT R _L = 3kΩ to GND	5	7		V
V _{OL} Low-level output voltage ⁽³⁾	DOUT R _L = 3kΩ to GND		–7	–5	V
r _o Output resistance	DOUT V _{S+} = V _{S–} = 0, V _O = ±2V	300			Ω
I _{OS} ⁽⁴⁾ Short-circuit output current	DOUT V _{CC} = 5.5V, V _O = 0		±10		mA
I _{IS} Short-circuit input current	DIN V _I = 0			200	μA

(1) Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

(4) Not more than one output should be shorted at a time.

5.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see ⁽¹⁾)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Driver slew rate	R _L = 3kΩ to 7kΩ, See 6-2			30	V/μs
SR(t) Driver transition region slew rate	See 6-3		3		V/μs
Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

5.8 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	ROUT	I _{OH} = –1mA	3.5		V
V _{OL}	Low-level output voltage ⁽³⁾	ROUT	I _{OL} = 3.2mA		0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	RIN	V _{CC} = 5V, T _A = 25°C	1.7	2.4	V
V _{IT–}	Receiver negative-going input threshold voltage	RIN	V _{CC} = 5V, T _A = 25°C	0.8	1.2	V
V _{hys}	Input hysteresis voltage	RIN	V _{CC} = 5V	0.2	0.5	V
r _i	Receiver input resistance	RIN	V _{CC} = 5V, T _A = 25°C	3	5	kΩ

(1) Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

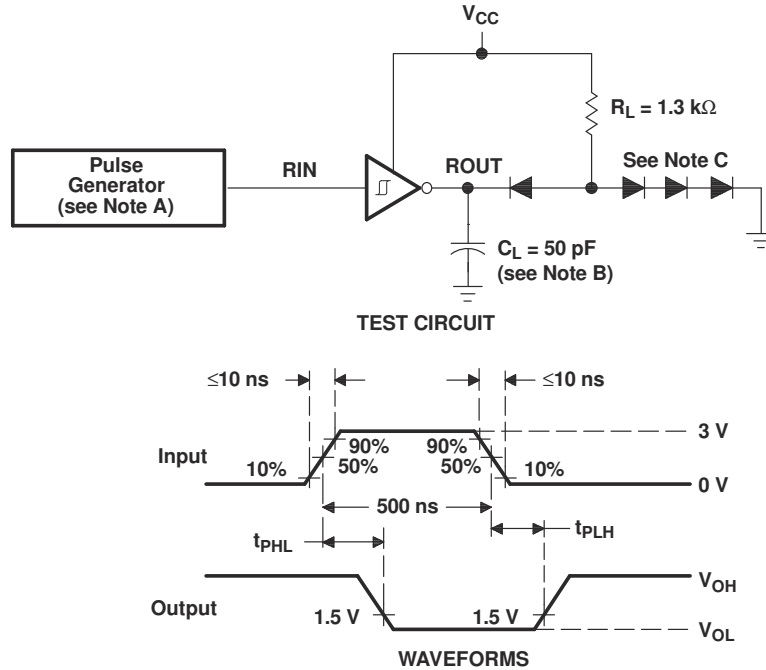
5.9 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see ⁽¹⁾ and [Figure 6-1](#))

PARAMETER		TYP	UNIT
t _{PLH(R)}	Receiver propagation delay time, low- to high-level output	500	ns
t _{PHL(R)}	Receiver propagation delay time, high- to low-level output	500	ns

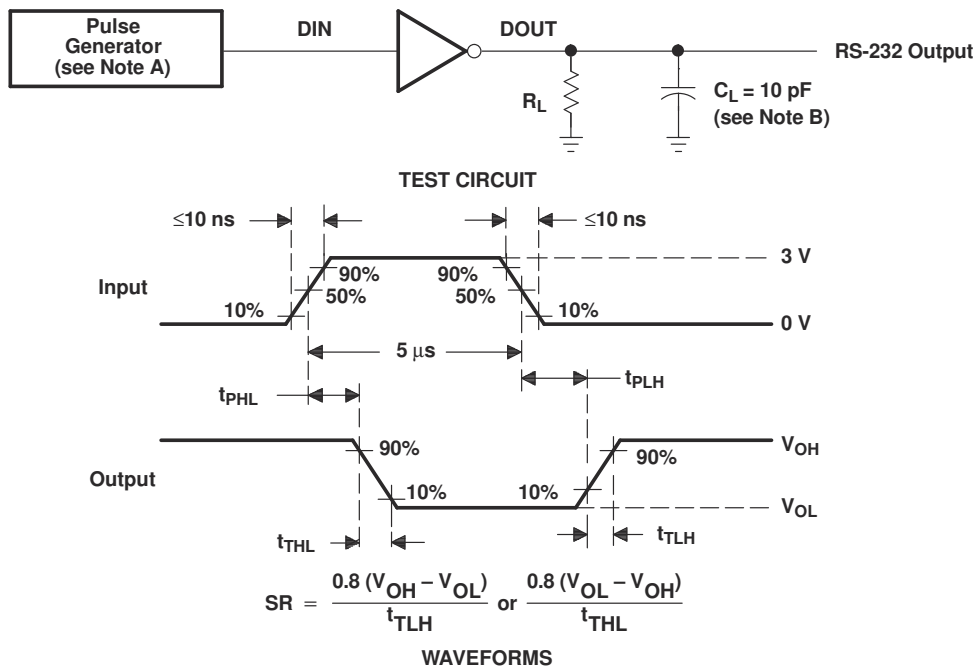
(1) Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

6 Parameter Measurement Information



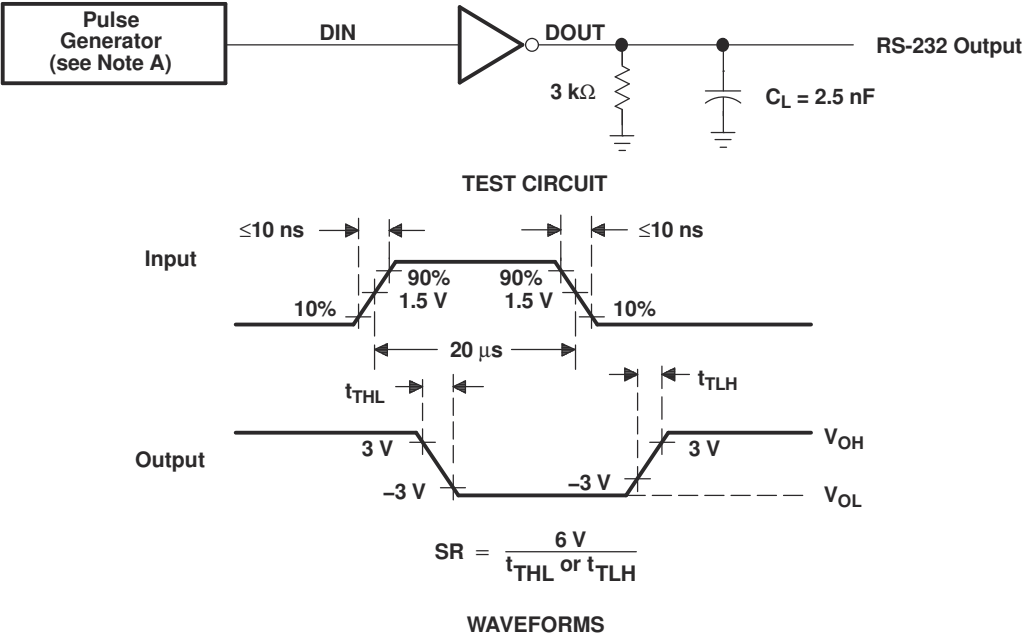
- A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

图 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



- A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.

图 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5 μs Input)



A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.

図 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20μs Input)

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Tables: Each Driver

INPUT ⁽¹⁾ DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 7-2. Each Receiver

INPUT ⁽¹⁾ RIN	OUTPUT ROUT
L	H
H	L

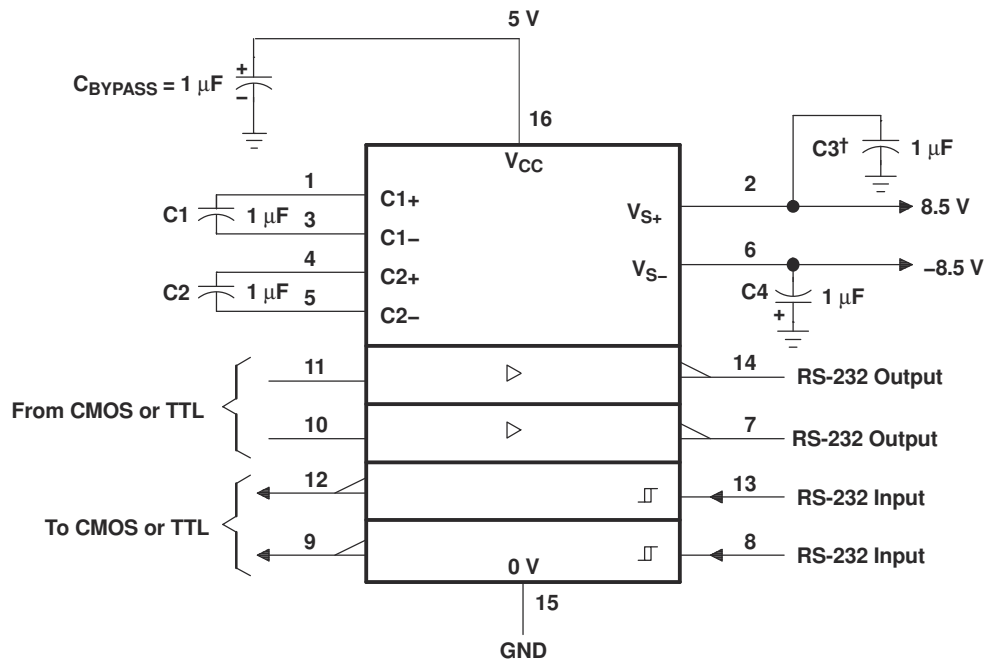
(1) H = high level, L = low level

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information



† C3 can be connected to V_{CC} or GND.

- Resistor values shown are nominal.
- Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the $1\mu\text{F}$ capacitors shown, the TRS202E can operate with $0.1\mu\text{F}$ capacitors.

图 8-1. Typical Operating Circuit

9 Device Documentation and Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

9.3 商標

LinASIC™ and TI E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (March 2021) to Revision E (February 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1

Changes from Revision C (September 2008) to Revision D (March 2021)	Page
「論理図」をページ 1 に移動	1
「注文情報」表を削除	1
「パッケージ情報」表を削除追加	1
「パッケージ情報」表を変更	1
Moved the <i>Function Tables</i> to the <i>Parameter Measurement Information</i> section.....	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS232ECD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECDR	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECDWR	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECPWR	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	0 to 70	RU32EC
TRS232EID	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	TRS232EI
TRS232EIDR	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	TRS232EI
TRS232EIDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI
TRS232EIDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI
TRS232EIN	Obsolete	Production	PDIP (N) 16	-	-	Call TI	Call TI	-40 to 85	TRS232EIN
TRS232EIPWR	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	RU32EI

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

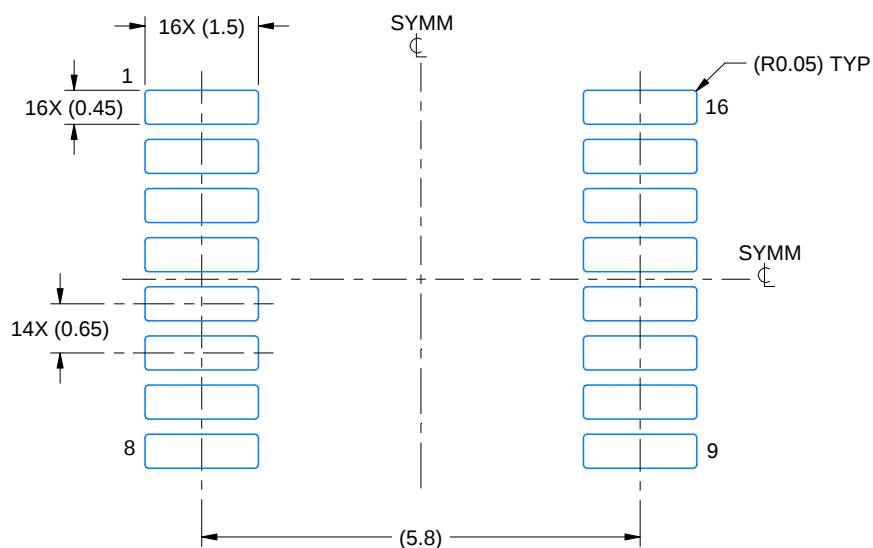
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

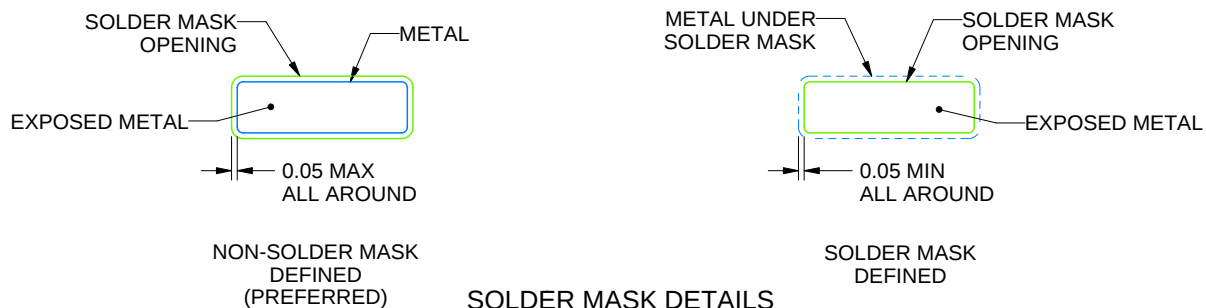
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

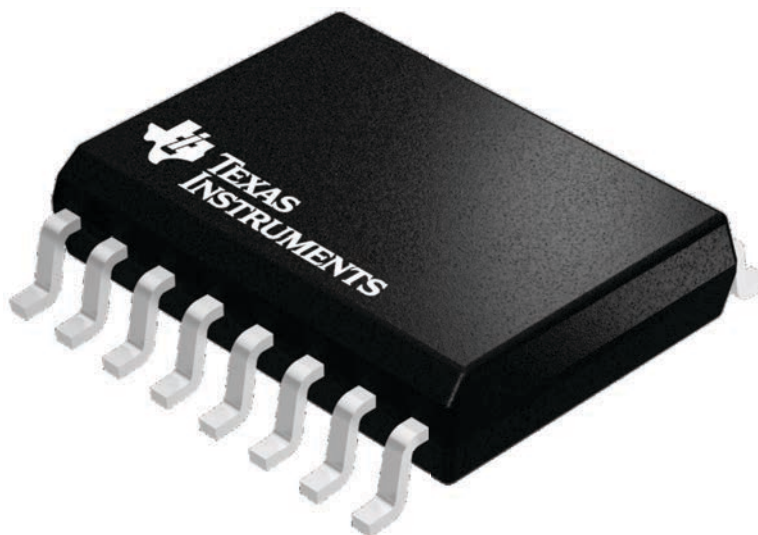
DW 16

SOIC - 2.65 mm max height

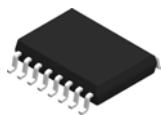
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

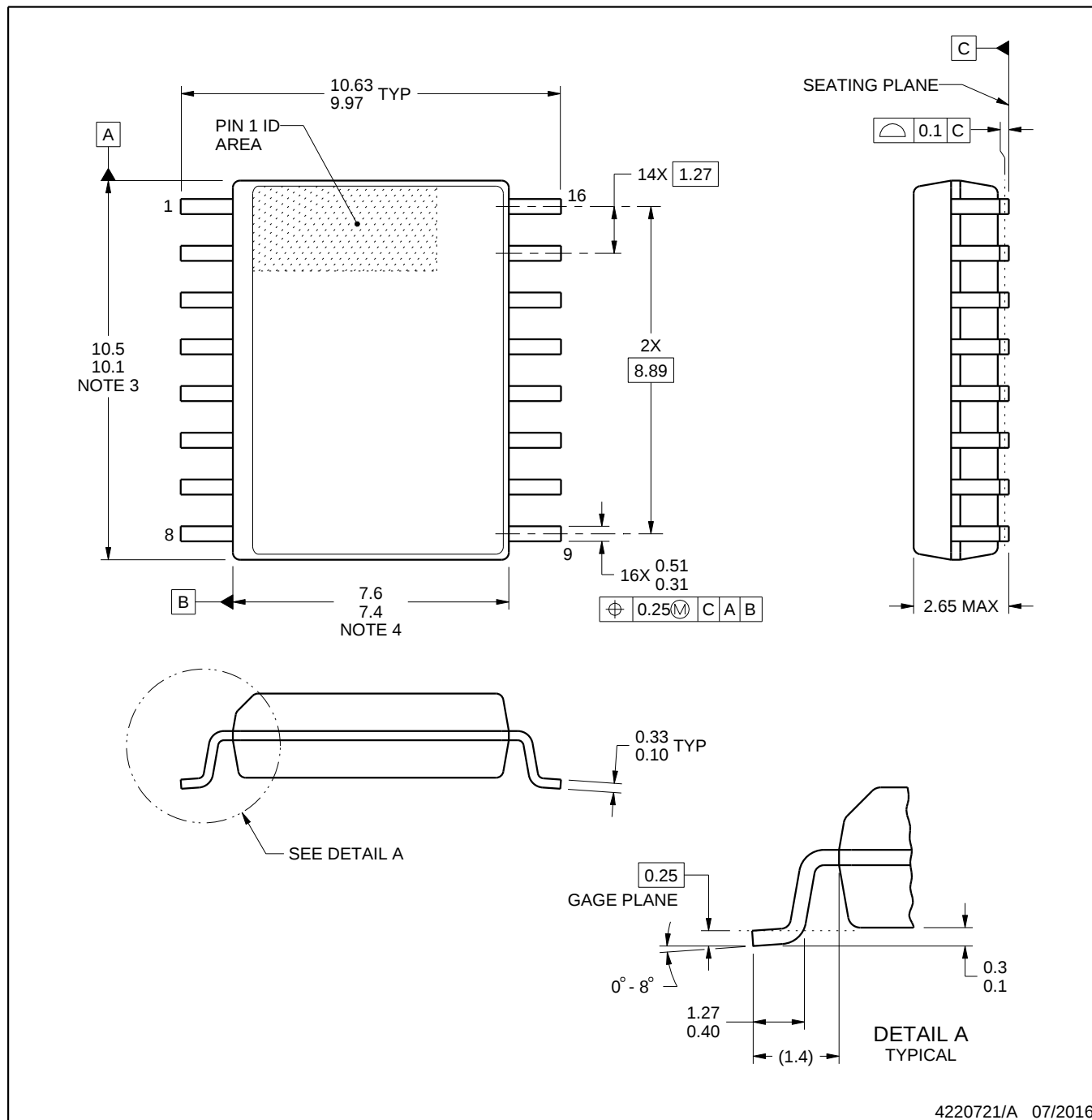


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

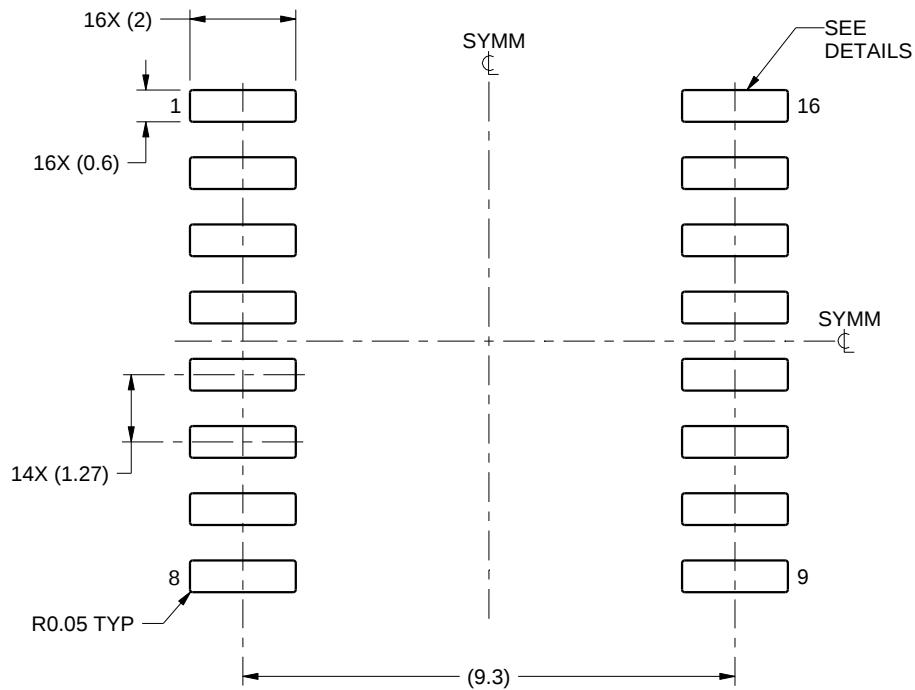
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

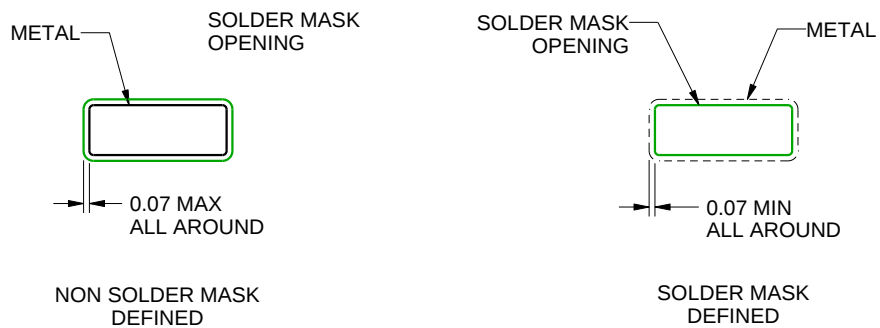
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

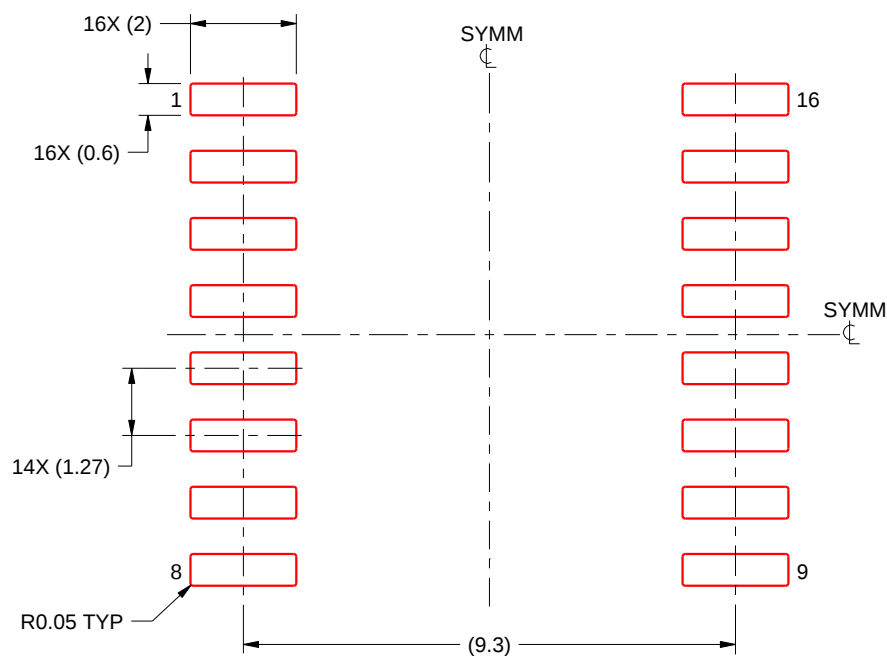
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated