

TRF1305B2 デュアルチャネル、DC から 6.5GHz 超、3dB 帯域幅、完全差動アンプ

1 特長

- 性能が最適化された 3 つのパワー ゲインのバリエーション：
 - 5dB (TRF1305A2)
 - 10dB (TRF1305B2)
 - 15dB (TRF1305C2)
- プリセット ゲインは外付け抵抗で低減可能
- 高い大信号帯域幅：
 - TRF1305B2：7GHz (3dB)、6.5GHz (1dB)
- OP1dB (差動 100Ω 負荷)：
 - 16dBm (2GHz)、12.5dBm (4 GHz)
- OIP3：34dBm (2GHz)、24dBm (4 GHz)
- ノイズ フィギュア：10.2dB (2GHz)、12dB (4 GHz)
- スルーレート：25kV/μs
- 広い入力 (±1V) および出力 (±0.5V) の同相電圧範囲
- 柔軟な構成とモード：
 - シングルエンド入力、差動出力 (S2D)
 - 差動入力、差動出力 (D2D)
 - シングルエンド出力 (性能に制限あり)
 - AC 結合または DC 結合の入出力
 - 調整可能な出力同相電圧
 - 同相入力範囲拡張モード
- 5V、柔軟な単一または分割電源をサポート
- アクティブな消費電力：チャンネルあたり 500mW
- 各チャンネルのパワーダウン

2 アプリケーション

- RF サンプリングまたは GSPS ADC ドライバ
- 試験および測定機器
- ワイヤレス通信テスト
- 高速データ アクイジション
- オシロスコープ (DSO)
- 高速デジタイザ
- スペクトル アナライザ
- ベクトル信号トランシーバ (VST)
- 同相モード レベル シフト
- RF アクティブ バラン
- I/Q ミキサ インターフェイス

3 概要

TRF1305B2 は、非常に高性能な閉ループのデュアル チャネル RF アンプで、真の DC から 6.5GHz を超える動作帯域幅を持ちます。このデバイスは、[ADC12DJ5200RF](#) や [ADC32RF5x](#) などの高速で高性能な ADC を、DC 結合または AC 結合のインターフェイスで駆動する優れた性能を備えています。このアンプは、RF、ゼロ IF、複素 IF、および高速の時間領域アプリケーションでの使用に最適化されています。このデバイスは、プリセットされたゲイン構成での性能に最適化されています。プリセットよりも低いゲインが必要な場合は、外付け抵抗を使用します。

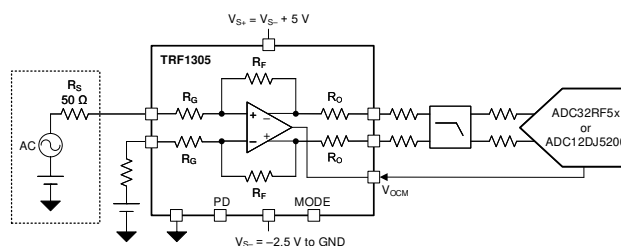
TRF1305B2 は、異なる出力同相電圧と入力同相電圧を設定できる VOCM ピンを備えています (たとえば、レベルシフトや、異なる DC 同相電圧を持つほとんどの IQ 降圧コンバータの ADC インターフェイスアプリケーション用)。フローティング 2 レールの分割電源または単一電源のオプション、および入力同相範囲をより電源に近い範囲へと拡張できる MODE ピン。チャンネル間の絶縁能力が高いため、信号の完全性を損なうことなく、複雑な IQ 送受信信号チェーンで使用することができます。

TRF1305B2 には、各チャンネルを個別にパワーダウンする機能があります。このデバイスは、テキサス・インスツルメンツ独自の高度な BiCMOS プロセスで製造されており、省スペースの 2.5mm × 3.0mm、16 ピンの WQFN-FCRLF パッケージで供給されます。

製品情報

部品番号 ⁽¹⁾	D2D パワー ゲイン	パッケージ ⁽²⁾
TRF1305A2 ⁽³⁾	5dB	RYP (WQFN-FCRLF、16)
TRF1305B2	10dB	
TRF1305C2 ⁽³⁾	15dB	

- (1) 製品比較表を参照してください。
- (2) 詳細については、[セクション 11](#) を参照してください。
- (3) プレビュー情報 (量産データではありません)。



TRF1305 で高速 ADC を駆動



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4 Device Comparison

DEVICE	CHANNEL COUNT	GAIN	PACKAGE
TRF1305A1	1	15 dB	RPV (WQFN, 12)
TRF1305B1	1	10 dB	RPV (WQFN, 12)
TRF1305C1	1	5 dB	RPV (WQFN, 12)
TRF1305A2	2	15 dB	RYP (WQFN, 16)
TRF1305B2	2	10 dB	RYP (WQFN, 16)
TRF1305C2	2	5 dB	RYP (WQFN, 16)

5 Pin Configuration and Functions

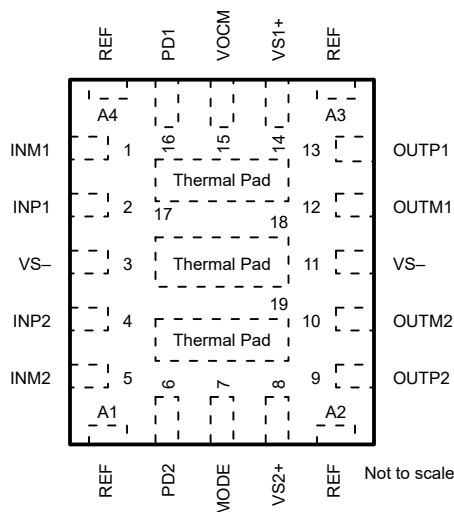


図 5-1. RYP Package (Dual-Channel), 16-Pin WQFN-FCRLF (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
INM1	1	I	Negative side of differential input signal for Channel 1 (Ch1).
INM2	5	I	Negative side of differential input signal for Channel 2 (Ch2).
INP1	2	I	Positive side of differential input signal for Channel 1 (Ch1).
INP2	4	I	Positive side of differential input signal for Channel 2 (Ch2).
MODE	7	I	Mode selection pin. For details, see セクション 7.4.1 .
OUTM1	12	O	Negative side of differential output signals for Ch1.
OUTM2	10	O	Negative side of differential output signals for Ch2.
OUTP1	13	O	Positive side of differential output signals for Ch1.
OUTP2	9	O	Positive side of differential output signals for Ch2.
PD1	16	I	Power-down signal for Ch1, referenced to thermal pad. Supports both 1.8-V and 3.3-V logic. Logic 0 or open = channel enabled. Logic 1 = channel powered down.
PD2	6	I	Power-down signal for Ch2, referenced to thermal pad. Supports both 1.8-V and 3.3-V Logic. Logic 0 or open = channel enabled. Logic 1 = channel powered down.
REF	A1, A2, A3, A4	–	Reference for RF signals and PD control voltage. Connect to same potential as the thermal pad.
VOCM	15	I	Output common-mode voltage input pin. Common for both channels. Floating the pin sets the output common-mode voltage to $V_{S-} + 2.5$ V.
VS-	3, 11	P	Negative supply pin. Common for both channels.
VS1+	14	P	Positive supply pin for Ch1. V_{S1+} must be equal to V_{S2+} .
VS2+	8	P	Positive supply pin for Ch2. V_{S1+} must be equal to V_{S2+} .
Thermal Pad	17, 18, 19	–	PAD. Reference for RF signals and PD control voltage. Also serves as thermal pads. Connect to heat-dissipating V_{S-} (recommended) or GND plane on the board.

(1) I = input, P = power, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{S-}	Negative supply voltage, referenced to thermal pad	–3	3	V
V_{S1+} , V_{S2+}	Positive supply voltage	–0.3	$V_{S-} + 5.5$	V
V_S	Total supply voltage, $V_S = V_{S+} - V_{S-}$	–0.3	5.5	V
P_{IN}	Input RF power		20	dBm
V_{PD}	PD pin voltage, referenced to thermal pad, $V_{S+} \geq 3.3$ V	–0.3	3.6	V
	PD pin voltage, referenced to thermal pad, $V_{S+} < 3.3$ V	–0.3	$V_{S+} + 0.3$	V
V_{OCM}	VOCM pin voltage	$V_{S-} + 1$	$V_{S-} + 4$	V
V_{MODE}	MODE pin voltage	$V_{S-} - 0.3$	$V_{S-} + 3.3$	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Positive supply voltage	2.5		5	V
V_{S-}	Negative supply voltage	–2.5		0	V
V_S	Total supply voltage, $V_S = V_{S+} - V_{S-}$		5		V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TRF1305x2	UNIT
		RYP (WQFN-FCRLF)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	51.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	24.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	14.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	10.7	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics - TRF1305B2

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output with differential source impedance (Z_S) = 100 Ω , differential output load (Z_L) = 100 Ω , external input resistor network (see [8-3](#)), and resistor network included as part of DUT specifications (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal 3-dB bandwidth	$P_{IN} = -20\text{ dBm}$ at each input		7.6		GHz
	Small-signal 1-dB bandwidth			6.5		
LSBW	Large-signal 3-dB bandwidth	Differential $P_{IN} = -3\text{ dBm}$		7		GHz
	Large-signal 1-dB bandwidth			6.5		
S21	Power gain	$f = 4\text{ GHz}$		9.8		dB
	Gain variation over temperature	$f = 4\text{ GHz}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		0.7		
S11	Input return loss	$f = 10\text{ MHz}$ to 7.5 GHz		-10		dB
S12	Reverse isolation	$f < 10\text{ GHz}$ (when enabled)		-20		dB
G_{IMB}	Differential gain imbalance	$f < 5\text{ GHz}$, S2D, $P_{IN} = -20\text{ dBm}$ with 50- Ω source impedance		± 0.2		dB
PH_{IMB}	Differential phase imbalance			± 2		°
OP1dB	Output 1-dB compression point	$f = 500\text{ MHz}$		15.7		dBm
		$f = 1\text{ GHz}$		16		
		$f = 2\text{ GHz}$		16		
		$f = 3\text{ GHz}$		15		
		$f = 4\text{ GHz}$		12.5		
		$f = 5\text{ GHz}$		11.3		
HD2	Second-order harmonic distortion	$f = 500\text{ MHz}$, $V_O = 2\text{ V}_{PP}$		-73		dBc
		$f = 1\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-70		
		$f = 2\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-60		
		$f = 3\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-55		
		$f = 4\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-46		
HD3	Third-order harmonic distortion	$f = 500\text{ MHz}$, $V_O = 2\text{ V}_{PP}$		-68		dBc
		$f = 1\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-60		
		$f = 2\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-55		
		$f = 3\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-53		
		$f = 4\text{ GHz}$, $V_O = 2\text{ V}_{PP}$		-47		
OIP2	Output second-order intercept point	$f = 500\text{ MHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		75		dBm
		$f = 1\text{ GHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		72		
		$f = 2\text{ GHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		60		
		$f = 3\text{ GHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		53		
		$f = 4\text{ GHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		45		
		$f = 5\text{ GHz}$, $P_O = 1\text{ dBm}$ per tone, 2-MHz spacing		49		

6.5 Electrical Characteristics - TRF1305B2 (続き)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{mid supply}$, D2D ac-coupled input/output with differential source impedance (Z_S) = 100 Ω , differential output load (Z_L) = 100 Ω , external input resistor network (see [8-3](#)), and resistor network included as part of DUT specifications (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	f = 500 MHz, P _O = 1 dBm per tone, 2-MHz spacing		43.5		dBm
		f = 1 GHz, P _O = 1 dBm per tone, 2-MHz spacing		39.2		
		f = 2 GHz, P _O = 1 dBm per tone, 2-MHz spacing		34		
		f = 3 GHz, P _O = 1 dBm per tone, 2-MHz spacing		30.5		
		f = 4 GHz, P _O = 1 dBm per tone, 2-MHz spacing		24		
		f = 5 GHz, P _O = 1 dBm per tone, 2-MHz spacing		21		
NF	Noise figure	f = 500 MHz		8.4		dB
		f = 1 GHz		8.8		
		f = 2 GHz		10.2		
		f = 4 GHz		12		
		f = 5 GHz		12.4		
NSD	Output noise spectral density	f = 500 MHz		−155.6		dBm/Hz
		f = 1 GHz		−155.2		
		f = 2 GHz		−153.8		
		f = 4 GHz		−152		
		f = 5 GHz		−151.6		
DC PERFORMANCE						
V _{OD-MAX}	Max differential output voltage	f = 1 GHz		4		V _{PP}
	Slew rate	2-V V _O step, S2D configuration, V _{S+} = 2.5 V, V _{S−} = −2.5 V		25		kV/μs
	Output differential offset voltage			±3		mV
	Overdrive recovery time	From 2 × overdrive of each SE output to each output voltage settling to < ±50 mV		6		ns
COMMON-MODE						
V _{ICM}	Input common-mode voltage	Default range ⁽¹⁾	V _{S−} + 1.5	V _{S−} + 3.5		V
V _{OCM}	Output common-mode voltage		V _{S−} + 2	V _{S−} + 3		V
	Output common-mode offset voltage from V _{OCM} voltage			±10		mV
IMPEDANCE						
Z _{in-SE}	Single ended input impedance	At INPx pin with appropriate termination on INMx pin		47		Ω
Z _{O-DIFF}	Differential output impedance	f = near dc		8		Ω

6.5 Electrical Characteristics - TRF1305B2 (続き)

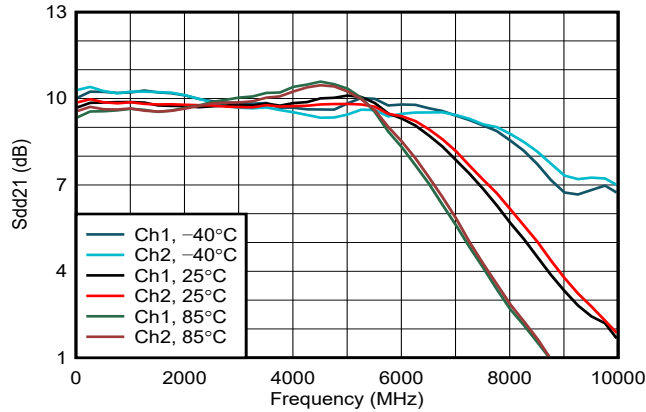
at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating V_{OCM}, PD_x, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output with differential source impedance (Z_S) = 100 Ω , differential output load (Z_L) = 100 Ω , external input resistor network (see [図 8-3](#)), and resistor network included as part of DUT specifications (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHANNEL-TO-CHANNEL PERFORMANCE						
	Channel-to-channel amplitude matching	f < 2 GHz	0.05			dB
		f < 5 GHz	0.3			
	Isolation	f < 2 GHz	−55			dB
		f < 5 GHz	−50			
POWER SUPPLY						
I _{QA}	Active quiescent current	Both channels active	180			mA
		One channel active, other is powered down	102			
I _{QPD}	Power-down quiescent current	Both channels powered down	25			mA
POWER DOWN						
V _{PD_Hi}	PD pin logic high	Referenced to PAD, see セクション 6.1	1.35			V
V _{PD_Lo}	PD pin logic low	Referenced to PAD, see セクション 6.1			0.3	V
I _{PD_Bias}	PD bias current (current on PD pin)	PD = high (1.8-V logic)	15			μA
		PD = high (3.3-V logic)	30			
t _{ON}	Turn-on time	From 50% V _{PD} transition to 90% RF out	25			ns
t _{OFF}	Turn-off time	From 50% V _{PD} transition to 10% RF out	20			ns

(1) V_{ICM} range can be extended closer to V_{S+} or V_{S-} in D2D configuration. See [セクション 7.4.1](#) for more details.

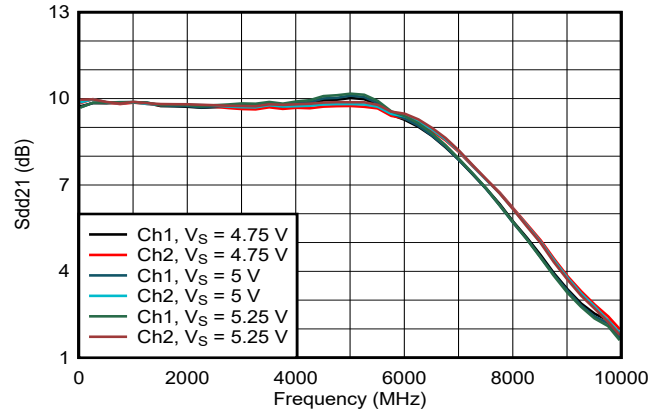
6.6 Typical Characteristics - TRF1305B2

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



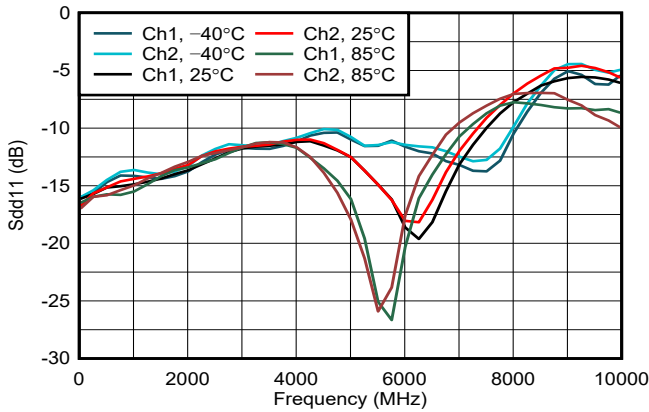
$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-1. Power Gain (S21) Across Temperature



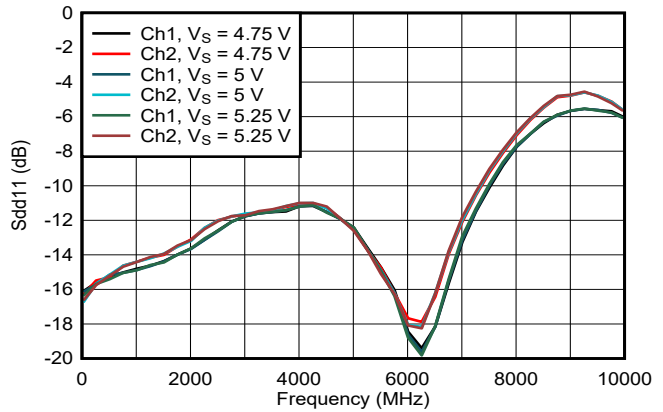
$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-2. Power Gain (S21) Across Supply Voltage



$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-3. Input Return Loss (S11) Across Temperature

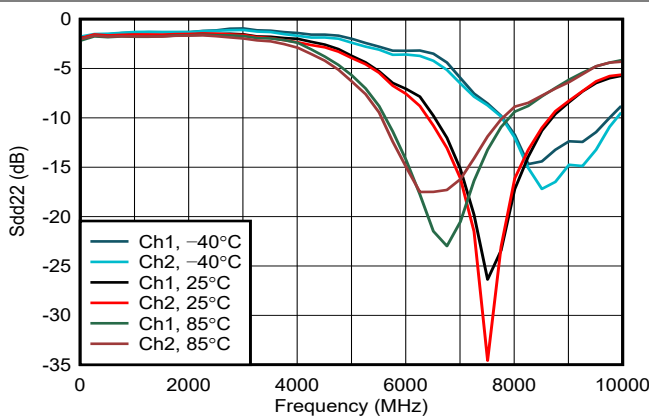


$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-4. Input Return Loss (S11) Across Supply Voltage

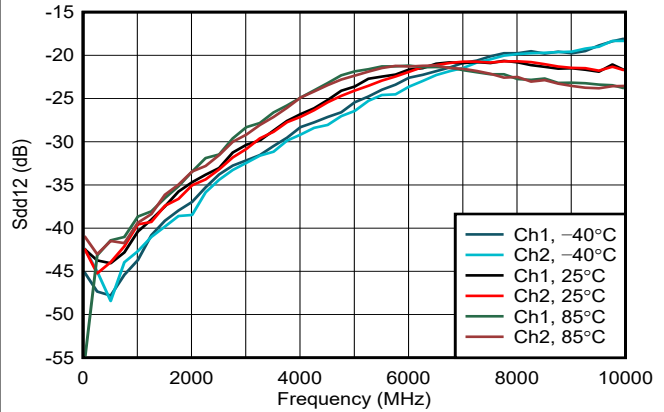
6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



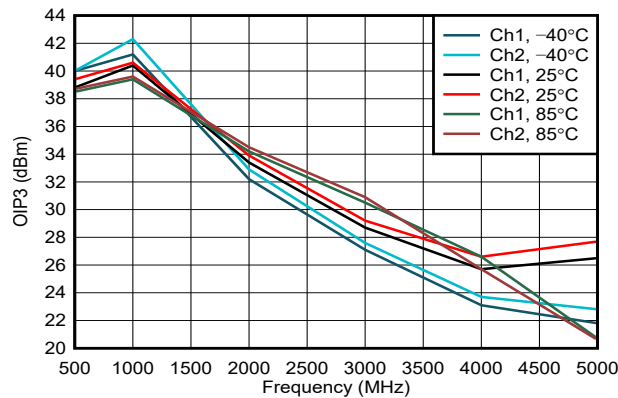
$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-5. Output Return Loss (S22) Across Temperature



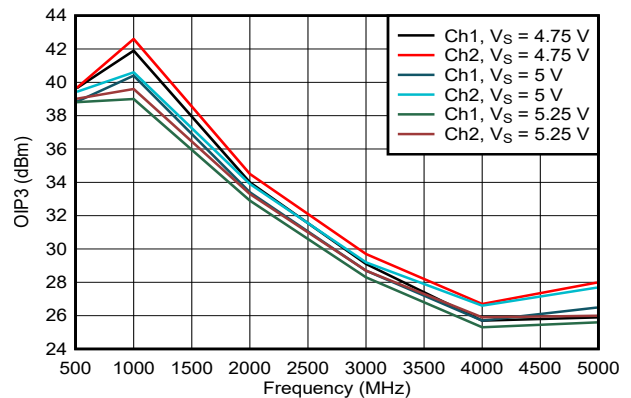
$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-6. Reverse Isolation (S12) Across Temperature



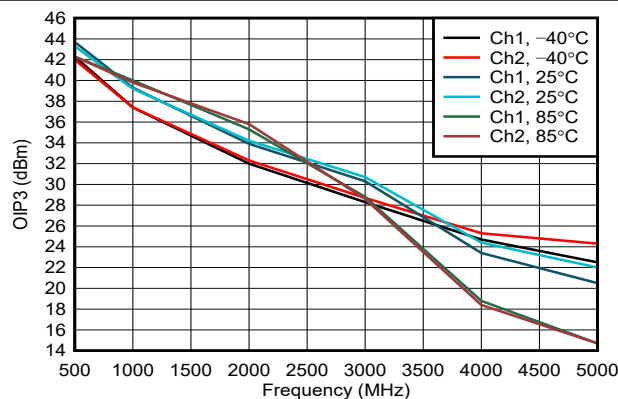
$P_{O}/\text{tone} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-7. OIP3 Across Temperature



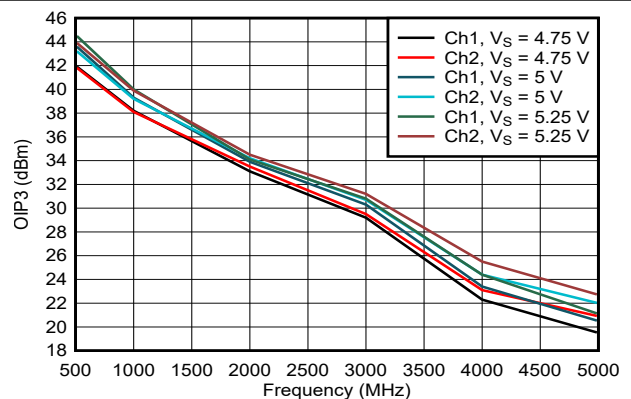
$P_{O}/\text{tone} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-8. OIP3 Across Supply Voltage



$P_{O}/\text{tone} = 1\text{ dBm}$, 2-MHz tone spacing

Figure 6-9. OIP3 Across Temperature

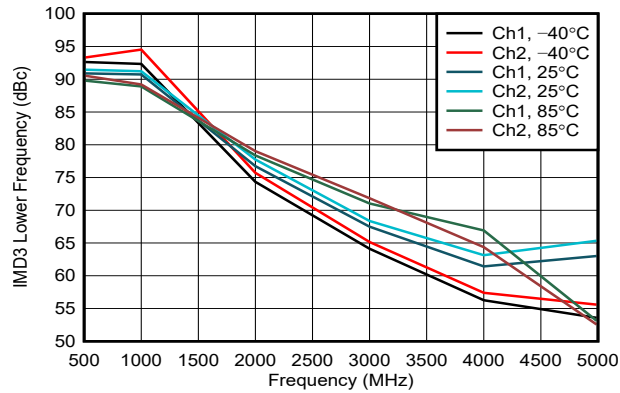


$P_{O}/\text{tone} = 1\text{ dBm}$, 2-MHz tone spacing

Figure 6-10. OIP3 Across Supply Voltage

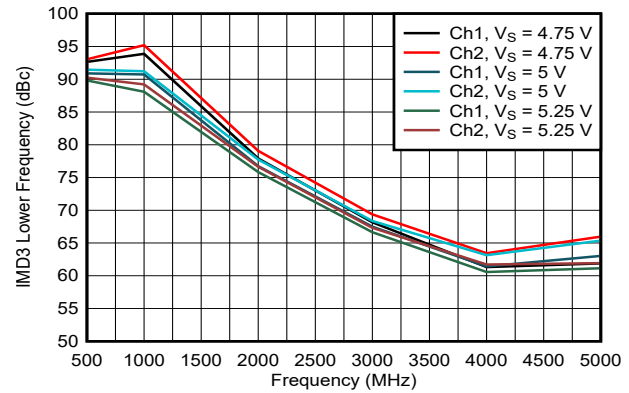
6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



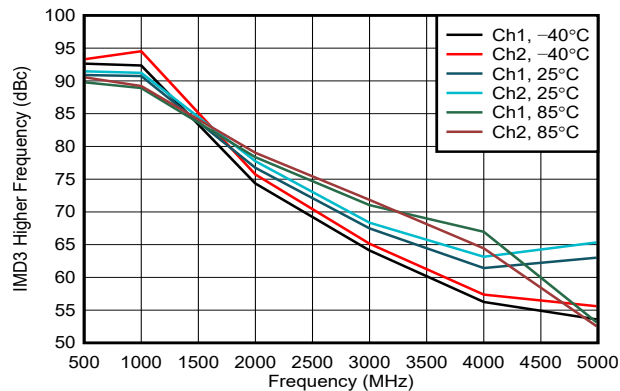
At $(2f_1 - f_2)$ frequency where $f_1 < f_2$,
 $P_{O/\text{tone}} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-11. IMD3 Lower Across Temperature



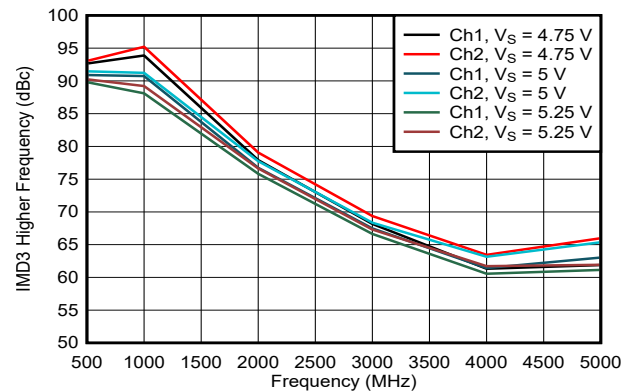
At $(2f_1 - f_2)$ frequency where $f_1 < f_2$,
 $P_{O/\text{tone}} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-12. IMD3 Lower Across Supply Voltage



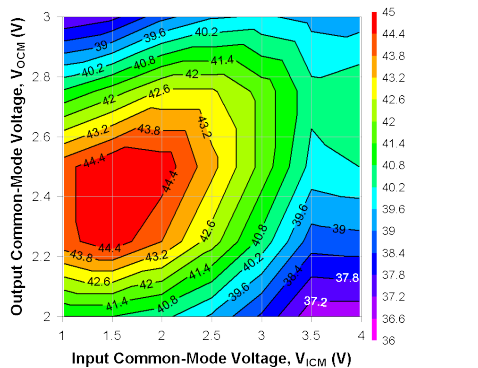
At $(2f_2 - f_1)$ frequency where $f_1 < f_2$,
 $P_{O/\text{tone}} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-13. IMD3 Higher Across Temperature



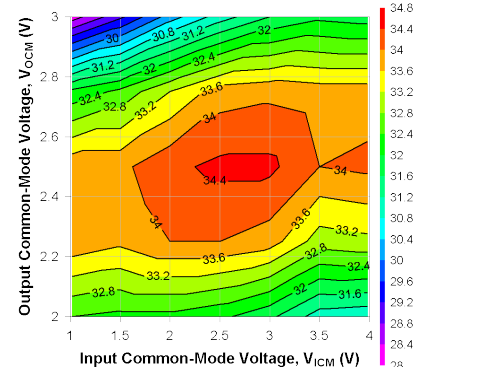
At $(2f_2 - f_1)$ frequency where $f_1 < f_2$,
 $P_{O/\text{tone}} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-14. IMD3 Higher Across Supply Voltage



$P_{O/\text{tone}} = 1\text{ dBm}$, 2-MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-15. OIP3 Across V_{ICM} and V_{OCM} at 500 MHz

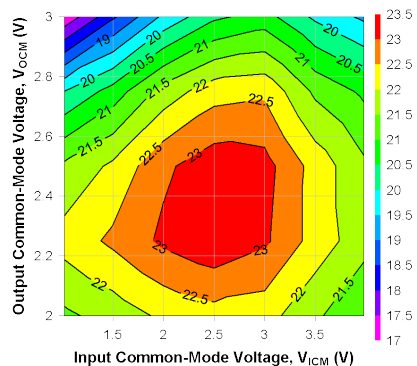


$P_{O/\text{tone}} = 1\text{ dBm}$, 2-MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-16. OIP3 Across V_{ICM} and V_{OCM} at 2 GHz

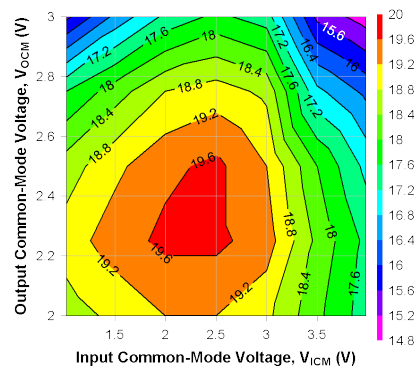
6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VO_{CM}, PD_x, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



$P_{O/\text{tone}} = 1\text{ dBm}$, 2-MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-17. OIP3 Across V_{ICM} and V_{OCM} at 4 GHz



$P_{O/\text{tone}} = 1\text{ dBm}$, 2-MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-18. OIP3 Across V_{ICM} and V_{OCM} at 5 GHz

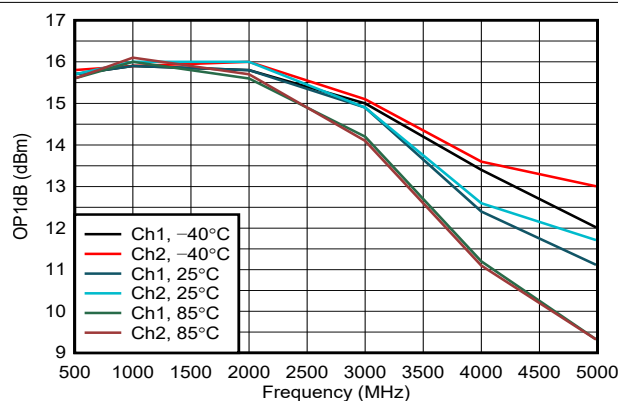


Figure 6-19. OP1dB Across Temperature

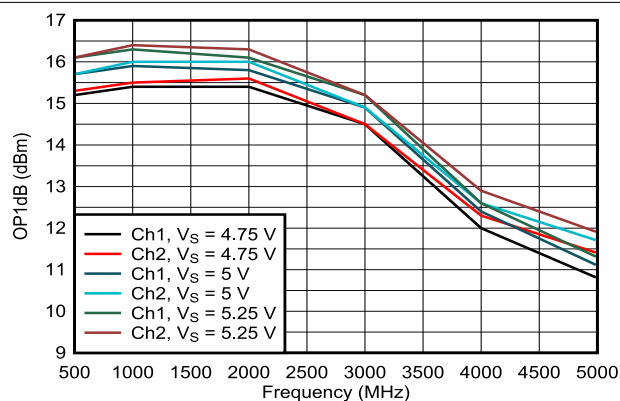


Figure 6-20. OP1dB Across Supply Voltage

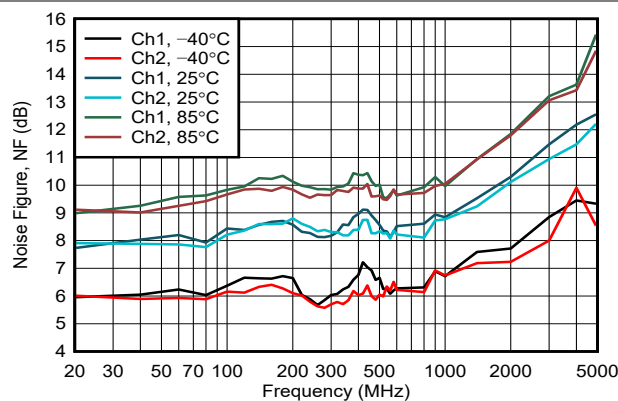


Figure 6-21. Noise Figure Across Temperature

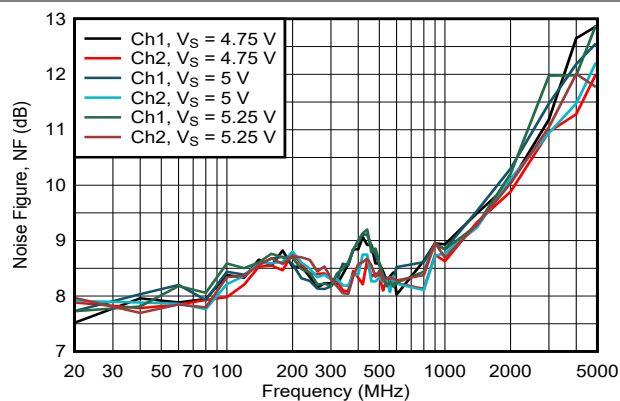
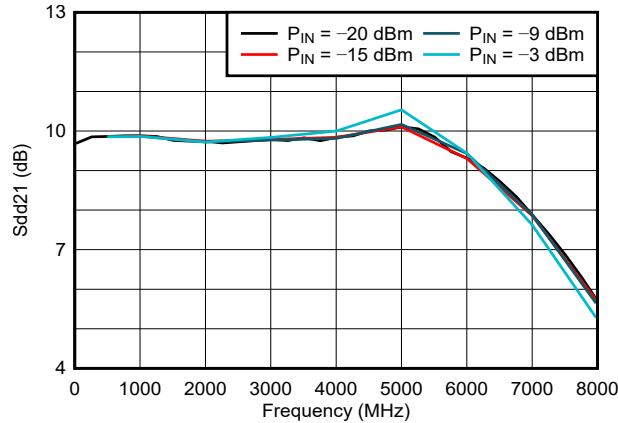


Figure 6-22. Noise Figure Across Supply Voltage

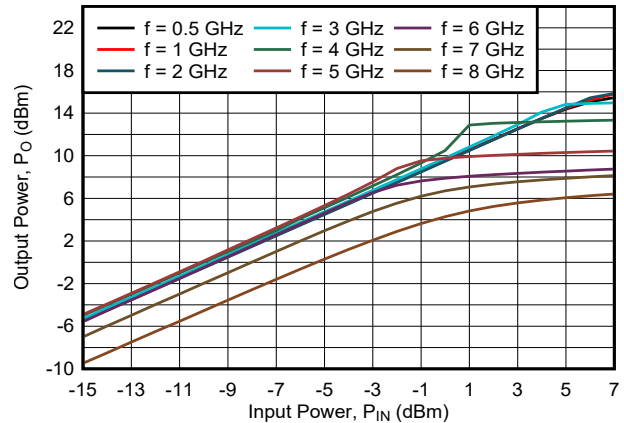
6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



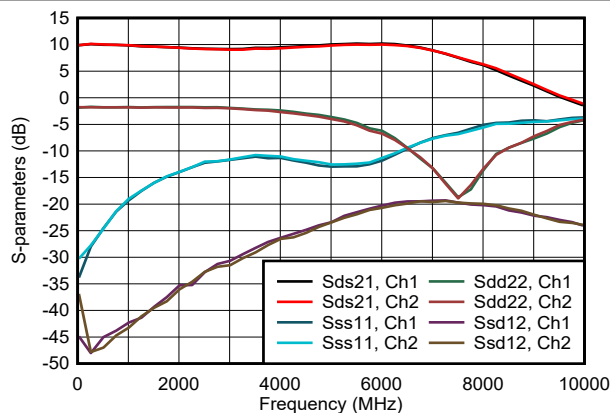
Channel 1, P_{IN} at each input pin with 50- Ω source

Figure 6-23. Power Gain (S21) Across Input Power Levels



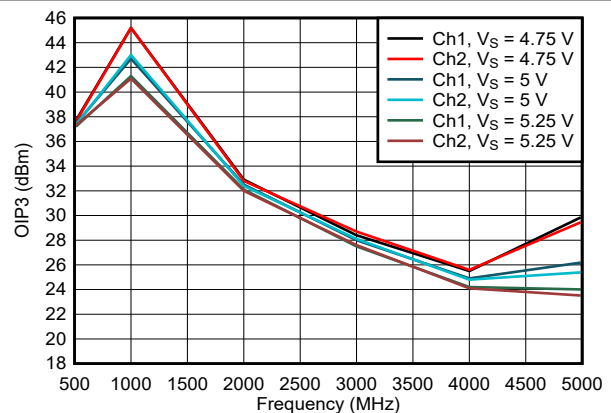
Channel 1, D2D configuration

Figure 6-24. Input Power vs. Output Power



S2D, $P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-25. S-Parameters in S2D Configuration

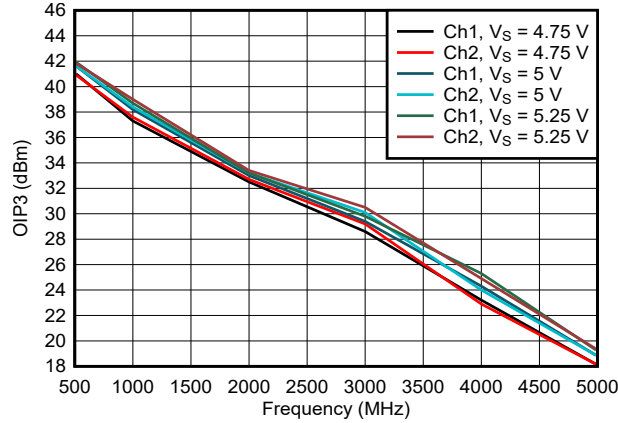


S2D, $P_O/\text{tone} = -5\text{ dBm}$, 2-MHz tone spacing

Figure 6-26. OIP3 Across Supply Voltage in S2D Configuration

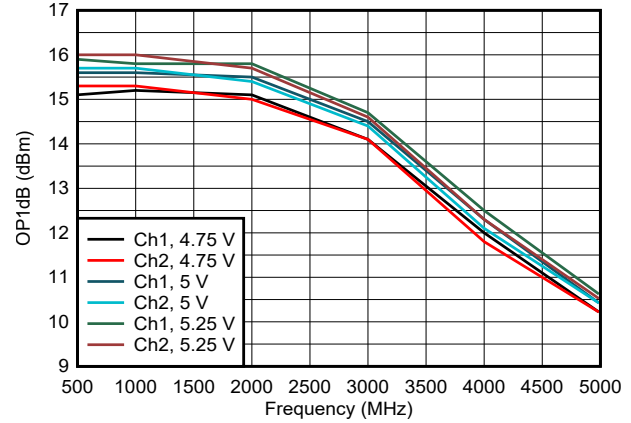
6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



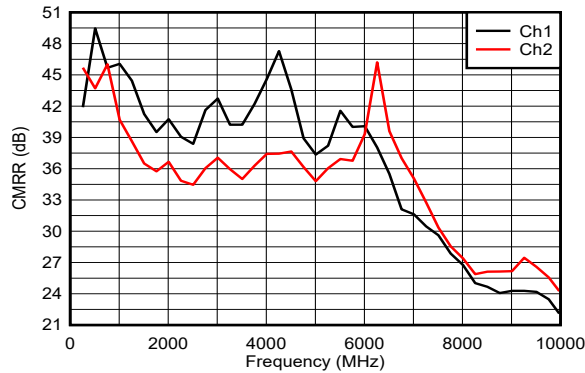
S2D configuration, $P_{O}/\text{tone} = 1\text{ dBm}$, 2-MHz tone spacing

Figure 6-27. OIP3 Across Supply Voltage



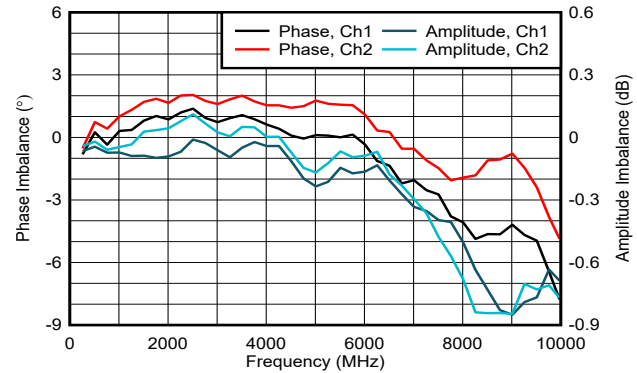
S2D configuration

Figure 6-28. OP1dB Across Supply Voltage



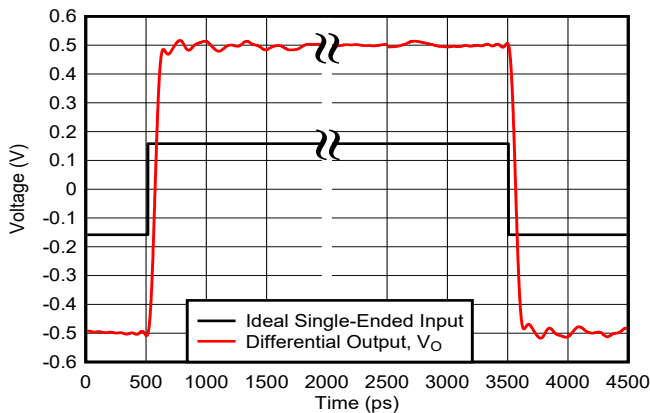
S2D, $P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-29. CMRR in S2D Configuration



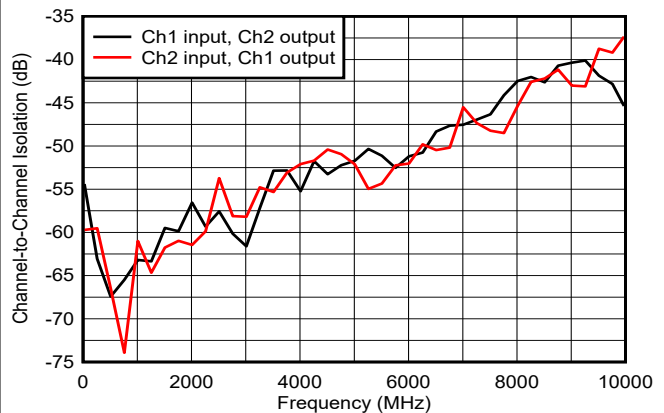
S2D, $P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-30. Gain and Phase Imbalance in S2D Configuration



S2D configuration, $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$

Figure 6-31. Step Response

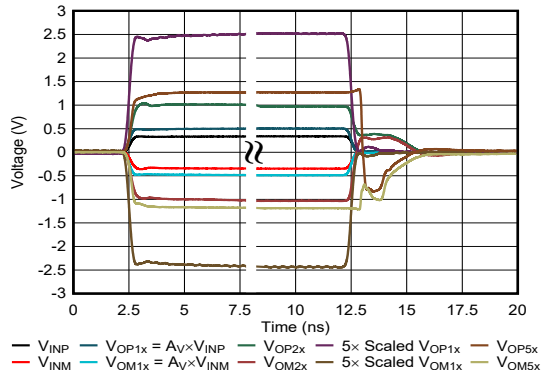


$P_{IN} = -20\text{ dBm}$ at each input pin with 50- Ω source

Figure 6-32. Channel-to-Channel Isolation

6.6 Typical Characteristics - TRF1305B2 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, floating VOCM, PDx, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\ \Omega$, $Z_L = 100\ \Omega$, external input resistor network (see [Figure 8-3](#)), ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



Voltage gain (A_V) $\approx 1.5\text{ V/V}$,

$V_{OZYX} = Y \times V_{OP1x}$, where $Z = \text{P or M}$ and $Y = 2 \text{ or } 5$

Figure 6-33. Overload Recovery Response and Timing

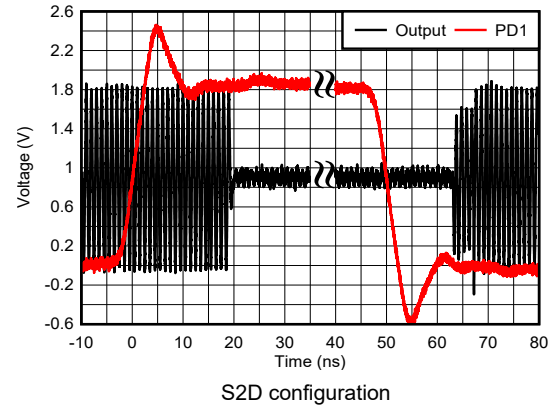


Figure 6-34. Power Up and Power Down Timing

7 Detailed Description

7.1 Overview

The TRF1305A2 TRF1305B2 TRF1305C2 (TRF1305x2) devices are dual-channel, high-performance fully differential amplifiers optimized for very wideband signals from dc to > 6.5 GHz. This device family is primarily designed to interface with high-speed and RF data converters that often require differential input (ADCs) and output (DACs) signaling. The TRF1305x2 can be dc or ac coupled, and configured as single-ended input and differential output (S2D) or differential input and differential output (D2D). The devices feature an output common-mode pin (VOCM) that allows the flexibility to set a desired common-mode output voltage. The VOCM pin sets the same output common-mode voltage for both shared channels. The amplifier allows the data converters to interface with a dc-coupled IQ demodulator or modulator if used in a direct conversion system. The TRF1305x2 family comes in three preset power gain variants (15 dB, 10 dB, and 5 dB), and has a closed-loop feedback-amplifier architecture.

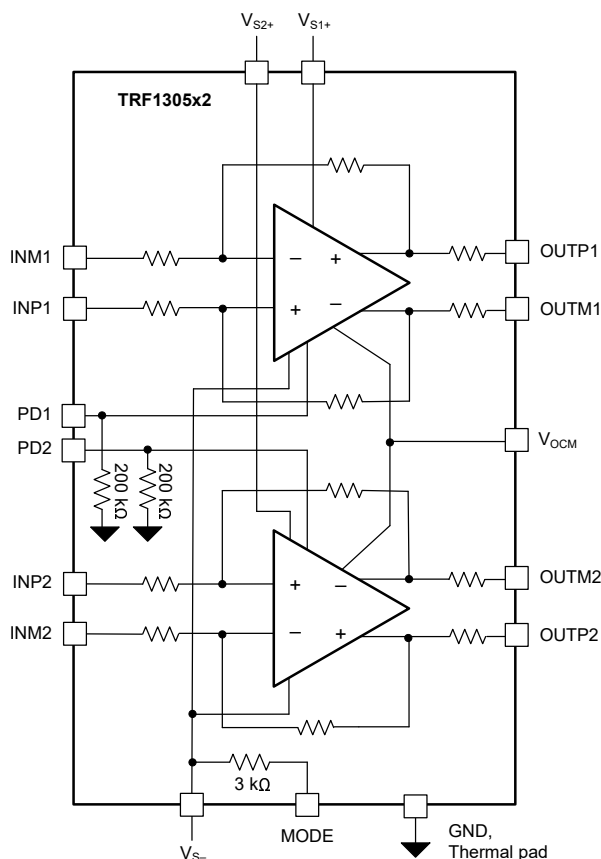
The devices are powered using two-rail supplies with a typical differential voltage of 5 V between the positive and negative supplies, and usable in split- or single-supply configurations. A power-down feature is also available that allows each amplifier channel to be powered down individually.

The output of the amplifiers is low impedance. Appropriate external series termination can be used to match to an arbitrary impedance.

7.2 Functional Block Diagram

This section shows the functional block diagram of the dual-channel TRF1305x2. The output common-mode control pin is common for both channels.

There are certain common internal circuits that are powered by both VS1+ and VS2+. Therefore, short both VS1+ and VS2+ on the board and supply both with a voltage even if only one channel is used. The negative supply, VS-, is shared by both the channels.



7.3 Feature Description

The TRF1305x2 includes the following key features:

- Two-rail floating supply with supply-independent thermal pads
 - Connect thermal pads to V_{S-} or GND
 - For best performance in the S2D configuration, connect the thermal pads to V_{S-}
 - RF signals and PDx pins referenced to thermal pads
- Single-supply or split-supply operation
- Supports single-ended and differential input configurations
- Performance-optimized preset fixed-gain variants
- Output common-mode control
- Input common-mode range selection by pullup resistor
- MODE pin: V_{ICM} range extension closer to V_{S+} or V_{S-} modes
- Digital-logic-controllable power-down option

7.3.1 Fully Differential Amplifier

The TRF1305x2 is a voltage-feedback fully differential amplifier (FDA) with wide bandwidth. The amplifier is designed for a differential power gain of 15 dB, 10 dB, or 5 dB depending on the device variant. This amplifier has excellent time-domain specifications with high slew rate, high input and output common-mode ranges, and fast transient settling time.

The output average voltage (common-mode) of the FDA device is controlled by a separate common-mode loop. The target output common-mode voltage is set by the V_{OCM} input pin.

7.3.2 Output Common-Mode Control

Figure 7-1 shows a functional diagram of the output common-mode control. Internally the V_{OCM} pin sees an LDO output voltage that is equal to $V_{S-} + 2.5$ V connected through a 2.5-k Ω resistor.

Floating the V_{OCM} pin is allowed. The output common-mode voltage at the output pins, OUTP_x and OUTM_x, defaults to the LDO output voltage of $V_{S-} + 2.5$ V when V_{OCM} pin is floated. Floating the V_{OCM} pin results in a V_{OCM} voltage equal to midsupply when $V_S = 5$ V. If the V_{OCM} pin is driven, then drive the pin from a low-impedance source. Limit the value of R_{OCM} to less than 25 Ω for accurate reflection of the forced V_{OCM} voltage at the device outputs.

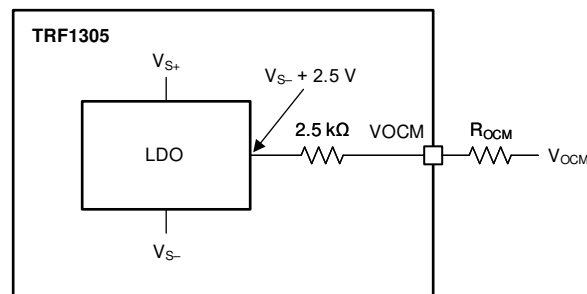


Figure 7-1. Output Common-Mode Control

7.3.3 Internal Resistor Configuration

図 7-2 shows the internal resistor configurations of TRF1305x2. 表 7-1 provides the values of these resistors for different gain variants.

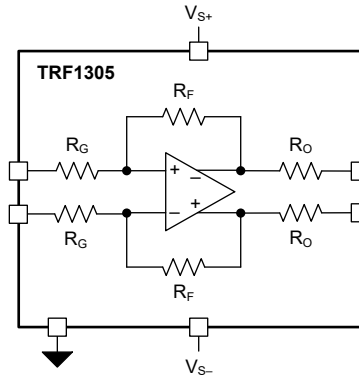


図 7-2. TRF1305x2 Internal Resistor Configuration

表 7-1. Resistor Values

DEVICE NAME	GAIN (dB)	R_G (Ω)	R_F (Ω)	R_O (Ω)
TRF1305A2	15	6.25	258	4
TRF1305B2	10	12.5	161	4
TRF1305C2	5	17	97	4

7.4 Device Functional Modes

7.4.1 MODE Pin

The TRF1305x2 have additional useful features that can be configured using the MODE pin. To select the device mode, either connect a $\pm 2\%$ maximum tolerance pullup resistor between the MODE pin and VS2+, or force a voltage on the MODE pin. Internally, the MODE pin is referenced to VS- through a 3-k Ω resistor (see セクション 7.2). The selected mode applies to both channels.

表 7-2 provides the value of the pullup resistor for each mode, the expected voltage, V_{MODE} , at the MODE pin when the pullup resistor is used or the necessary V_{MODE} voltage to set the device mode, and the mode configurations. The V_{MODE} voltage thresholds are approximately midway between the adjacent modes typical V_{MODE} voltage. If the mode functionality is used, use a decoupling capacitor on the MODE pin.

表 7-2. MODE Pin Configuration

MODE NUMBER	TRF1305x2: PULLUP RESISTOR TO VS2+ ($\pm 2\%$ MAXIMUM TOLERANCE)	MODE PIN VOLTAGE, V_{MODE} (V)	V_{ICM} RANGE EXTENSION ⁽¹⁾
0	OPEN	V_{S-}	Default V_{ICM} range
1	25.6 k Ω	$V_{S-} + 0.5$ V	Low side, extends V_{ICM} range closer to V_{S-}
2	12.8 k Ω	$V_{S-} + 0.95$ V	High side, extends V_{ICM} range closer to V_{S+}
N/A	Do not use pullup resistor < 10 k Ω or set $V_{MODE} > V_{S-} + 1.15$ V		

To switch the mode without turning the supplies off, use a switch or MUX connected between the pullup resistor options and VS2+, or force a mode-appropriate V_{MODE} voltage. However, powering down the device using the power-down feature between mode changes is preferred. The low-side and high-side V_{ICM} range extension modes source and sink currents, respectively (see also セクション 7.4.1.1). Ensure that the external circuitry is ready to sink or source these currents before the device is put in the active mode from the powered-down state.

7.4.1.1 Input Common-Mode Extension

The TRF1305x2 supports a V_{ICM} voltage closer to either V_{S+} or V_{S-} voltage than the default specified input common-mode range in [セクション 6.5](#), when configured in one of the V_{ICM} extension modes. The V_{ICM} extension mode can only be used in D2D configuration.

When configured in the low-side V_{ICM} extension mode, TRF1305B2 supports a 450 mV lower input common-mode voltage than the default option. For example, the lower limit of V_{ICM} voltage range extends from a default value of $V_{S-} + 1.5$ V to $V_{S-} + 1.05$ V for the TRF1305B2 variant, and the higher limit also shifts lower from a default value of $V_{S-} + 3.5$ V to $V_{S-} + 3.05$ V. At the lowest V_{ICM} voltage, approximately 15 mA current must be sunk by the external circuitry connected to the INPx and INMx pins.

When configured in the high-side V_{ICM} extension mode, TRF1305B2 supports a 450 mV higher input common-mode voltage than the default option. For example, the higher limit of V_{ICM} voltage range extends from a default value of $V_{S-} + 3.5$ V to $V_{S-} + 3.95$ V for the TRF1305B2 variant, and the lower limit also shifts up from a default of $V_{S-} + 1.5$ V to $V_{S-} + 1.95$ V. At the highest V_{ICM} voltage, approximately 15 mA current must be sourced by the external circuitry connected to the INPx and INMx pins.

Either resistors connected to supplies or external current sources can be used to sink or source the currents flowing out or into the INPx and INMx pins during the low-side or high-side V_{ICM} extension modes, respectively.

7.4.2 Power-Down Mode

The TRF1305x2 have two bias modes, active and power-down, that are controlled by the voltage on the PD pin. The PD pin is referenced to thermal pad through a 200-k Ω resistor; see also [セクション 7.2](#). If the $V_{S+} \geq 3.3$ V configuration is used, ensure that the PD voltage does not exceed the [Absolute Maximum Ratings](#) in case the high PD voltage is derived from V_{S+} .

With PD1 and PD2, control each channel independently, and individually power down each channel. Both 1.8-V and 3.3-V digital logic is supported for power down control.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Input and Output Interface Considerations

8.1.1.1 Single-Ended Input

In the single-ended input configuration, one of the amplifier input pins is driven from a source while the other input is terminated with an external resistor. [図 8-1](#) shows an ac-coupled, single-ended input configuration driven from and matched to a 50-Ω source. [図 8-1](#) shows how the non-driven INM pin is terminated with a 50-Ω external resistor to match to a source with the same 50-Ω impedance at the INP pin. The shown configuration works for all gain versions of TRF1305x2.

To configure the design in [図 8-1](#) for single-ended, dc-coupled input, replace the ac-coupling capacitors with shorts, and externally bias both INP and INM pins to a voltage close to the mid-supply or within the common-mode limits of the amplifier.

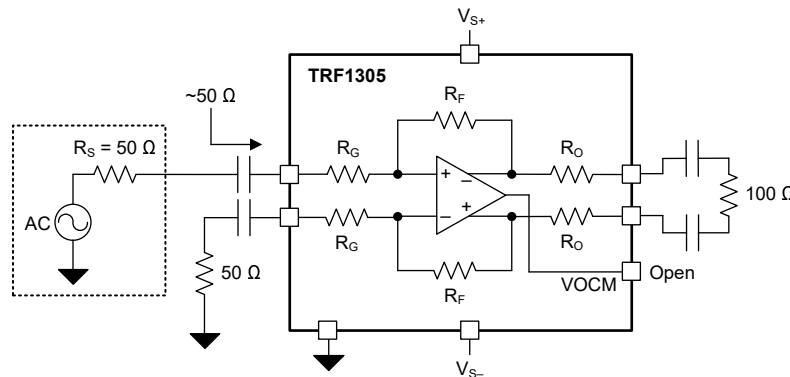


図 8-1. AC-Coupled, Single-Ended Input Matched to a 50 Ω Source

8.1.1.2 Differential Input

[図 8-2](#) shows how a simple network consisting of three resistors is used to match the differential input to a 100-Ω differential source. Though the 1-kΩ shunt resistor, R_{IN_SH} , does not have any impact at dc to low frequencies, the resistor is necessary to get the full wideband performance from TRF1305x2. [図 8-3](#) shows the configuration for ac-coupled differential input designs. The resistors values shown in [図 8-2](#) and [図 8-3](#) work for all gain versions of the TRF1305x2 for an 100-Ω input match to a 100-Ω differential source.

Use small foot-print resistors (0201 preferred), and RF quality for high frequency matching.

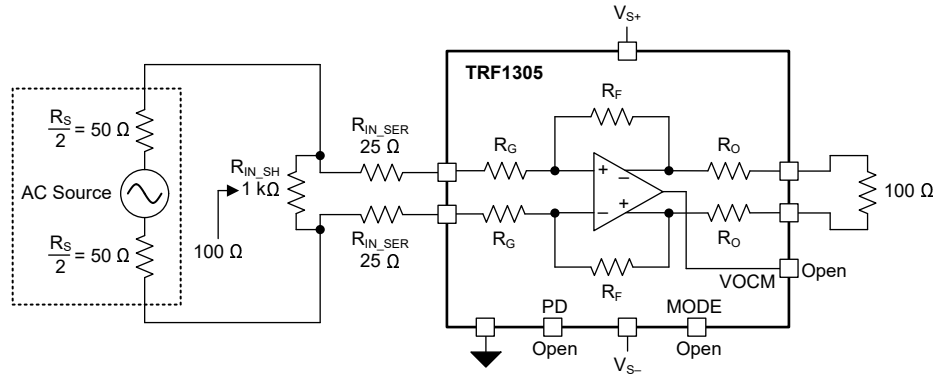


図 8-2. DC-Coupled Differential Input Matched to a 100-Ω Differential Source

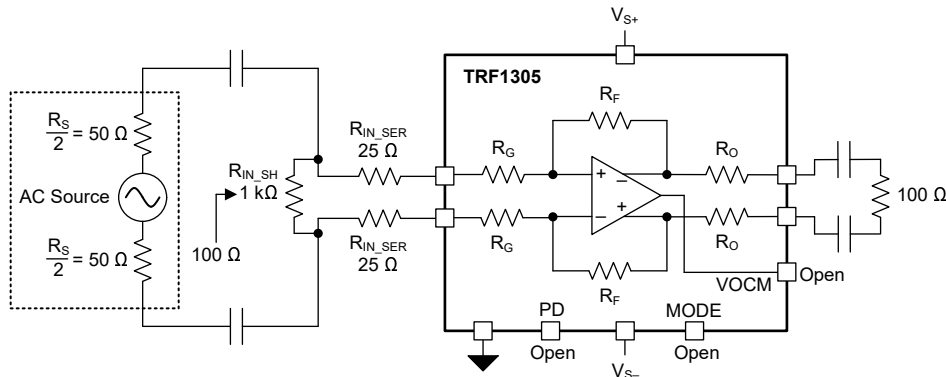


図 8-3. AC-Coupled Differential Input Matched to a 100-Ω Differential Source

8.1.1.3 DC Coupling Considerations

The TRF1305x2 accepts a wide range of input dc common-mode (CM) voltages. Take into consideration the dc current loading of the source when the TRF1305x2 is dc-coupled at the input. 図 8-4 shows that when the input CM voltage, V_{ICM} , is different than the output CM voltage, V_{OCM} , a net dc current flow from or to the source occurs. 式 1 shows the relationship that the source or sink current, I_{CM} , has with the input and output CM voltages:

$$I_{CM} = \frac{(V_{OCM} - V_{ICM})}{(R_F + R_G)} \quad (1)$$

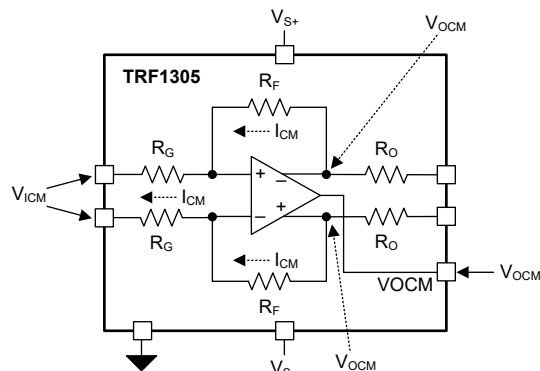


図 8-4. Net DC Current Flow When Input and Output Common-Mode Voltages are not Equal

8.1.2 Gain Adjustment With External Resistors in a Differential Input Configuration

The TRF1305x2 allow minor gain adjustments by configuring the input external resistive network that is part of the differential input configuration. 図 8-5 shows the external input network that comprises of a shunt resistor, R_{IN_SH} , and two series input resistors, R_{IN_SER} , connected to the input pins of the amplifier.

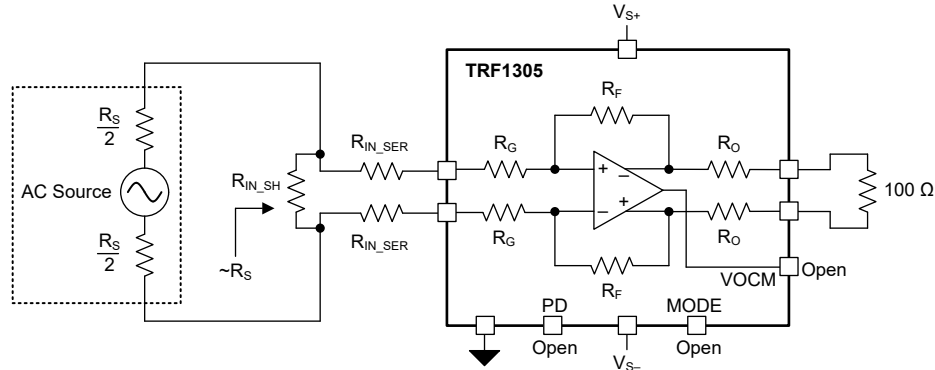


図 8-5. Gain Adjustment With External Resistor Network

表 8-1 provides resistor configurations for a 100- Ω differential source impedance.

表 8-1. Resistor Table for $R_S = 100 \Omega$

TRF1305B2		
POWER GAIN (dB)	$R_{IN_SH} (\Omega)$	$R_{IN_SER} (\Omega)$
10	1000	25
9	408	30
8	267	35
7	204	41
6	169	47
5	146	54

Use external resistive attenuation network only for small gain adjustments because there is a dB-to-dB noise figure degradation with the resistive attenuators. Use an amplifier version that requires minimal attenuation for achieving the overall gain.

For example, to realize 10-dB overall gain with $R_S = 100\text{-}\Omega$ differential, the two options are:

1. TRF1305B2 with $R_{IN_SH} = 1000 \Omega$ and $R_{IN_SER} = 25\text{-}\Omega$ resistors
2. TRF1305A2 with $R_{IN_SH} = 125 \Omega$ and $R_{IN_SER} = 49\text{-}\Omega$ resistors

Option 1 is recommended because the NF is better by approximately 3 dB compared to option 2.

図 8-7 shows how $V_{MIDSUPPLY}$ is chosen to be 0.8 V, so that the amplifier input has a CM offset from $V_{MIDSUPPLY}$ of 0.8 V and output has a CM offset from $V_{MIDSUPPLY}$ of 0.4 V ($1.2 \text{ V} - 0.8 \text{ V}$). The CM offsets are within the valid common-mode range of the amplifier, so the supplies of the TRF1305B2 are chosen to be $V_{S+} = 3.3 \text{ V}$ ($0.8 \text{ V} + 2.5 \text{ V}$) and $V_{S-} = -1.7 \text{ V}$ ($0.8 \text{ V} - 2.5 \text{ V}$). Further optimization in the choice of supply is possible by selecting the input and output CM voltages for the best OIP3 performance. セクション 8.2.1.3 has contour graphs that show OIP3 across input and output common-mode voltages.

The output CM is greater than the input CM; therefore, a net 6.9-mA $((1.2 \text{ V} - 0 \text{ V}) / (161 \Omega + 12.5 \Omega))$ dc current flows from the output to input through the internal feedback resistors. Depending on the choice of the passive mixer, this current can required to be sunk outside the mixer so that the bias conditions of the mixer are not disturbed. A 250- Ω pulldown resistor connected to the INP pin to -1.7 V supply is adequate. If the 6.9-mA dc current is sourced entirely from the amplifier, then the output headroom can be affected. Therefore, source the current externally from the supply using a pair of pullup resistors connected to the amplifier outputs. 300- Ω pullup resistors from OUTP and OUTM to 3.3 V are adequate.

The I-channel mixer output has a 50- Ω port and is connected to the amplifier INP pin through a small (4.7 Ω) series resistor. The INM pin is terminated to ground through a 55- Ω resistor and to -1.7 V through a 250- Ω resistor. This configuration makes sure that the impedance the amplifier sees at the input pins is the same at both INP and INM pins. The impedance of the mixer is close to 43 Ω and provides better than a -20-dB return loss (theoretically). Be aware that there is some drop in the gain due to these resistor networks. Also, the values of the resistors chosen in 図 8-6 are a good starting point; in practice, some adjustment is often needed to simultaneously meet the dc conditions and the RF performance.

At the amplifier output, 50- Ω series resistors are used to match to the antialiasing filter with 100- Ω differential input impedance. The filter output is connected to ADC with appropriate matching. 図 8-6 only shows the I-channel; the Q-channel has an identical configuration.

8.2.1.3 Application Curves

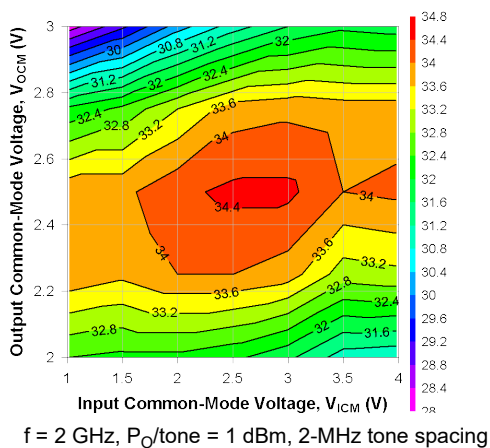


図 8-8. OIP3 Across Input and Output Common-Mode Voltage

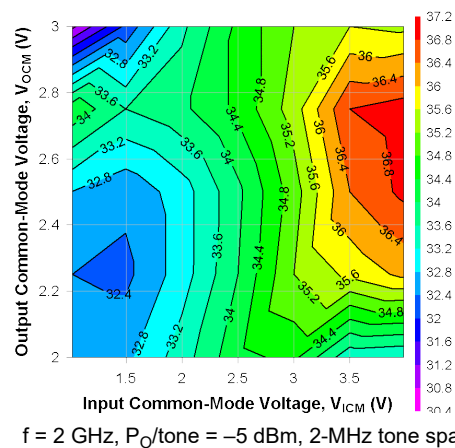


図 8-9. OIP3 Across Input and Output Common-Mode Voltage

8.3 Power Supply Recommendations

8.3.1 Supply Voltages

For the TRF1305x2, short both the VS1+ and VS2+ supply pins together to the same voltage for proper device operation. The typical differential supply between VS+ and VS– is 5 V. The VS+ and VS– supply pins can be floated with respect to the thermal pad within the specified range listed in [セクション 6.1](#) and [セクション 6.3](#).

8.3.2 Single-Supply Operation

The VS– pin is connected to GND in the single-supply configuration. Single-supply operation is most convenient in ac-coupled configurations because the dc common-mode voltages of the source at the inputs and the driven circuit at the outputs are inherently decoupled.

8.3.3 Split-Supply Operation

In split-supply configuration, choose the V_{S+} and V_{S-} voltages to be within the ranges specified in [セクション 6.1](#) and [セクション 6.3](#). The TRF1305x2 allows choosing negative voltages for the V_{S-} supply, thereby allowing the flexibility to choose input and output common-mode voltages according to the input network and output network requirements.

8.3.4 Supply Decoupling

The VS+ and VS– supply pins are decoupled individually to GND using external capacitors. For the TRF1305x2, VS+ decoupling can be split between VS1+ to GND and VS2+ to GND separately for ease of board layout. Place the decoupling capacitors close to the device supply pins.

8.4 Layout

8.4.1 Layout Guidelines

The TRF1305x2 devices are wideband closed-loop feedback amplifiers. When designing with wideband RF amplifiers that have high gain, take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal integrity, power integrity, and thermal performance.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. Ground pins are the reference for the RF signals. Ensure that the second layer of the PCB has a continuous ground layer without any ground cutouts in the vicinity of the amplifier. To minimize phase imbalance, match the length of the output differential lines of both channels. Length matching the input traces is also important, especially if the input configuration is differential. Use small-footprint, passive components wherever possible.

For good heat dissipation, connect the device thermal pad to the board ground planes using thermal vias under the device. For improved heat dissipation, connect the device thermal pad to the top layer ground plane of the board.

8.4.1.1 Thermal Considerations

The TRF1305x2 are packaged in a WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pads underneath the devices to the thermally dissipative ground plane on the board. For good thermal design, use thermal vias to connect the thermal pad plane on the top layer of the PCB to the ground planes in the inner layers.

Limit the total power dissipation to keep the device junction temperature less than 150°C for instantaneous power, and less than 125°C for continuous power.

8.4.2 Layout Example

図 8-10 shows an example layout for TRF1305x2 with a differential input configuration. Key area are highlighted in the figure.

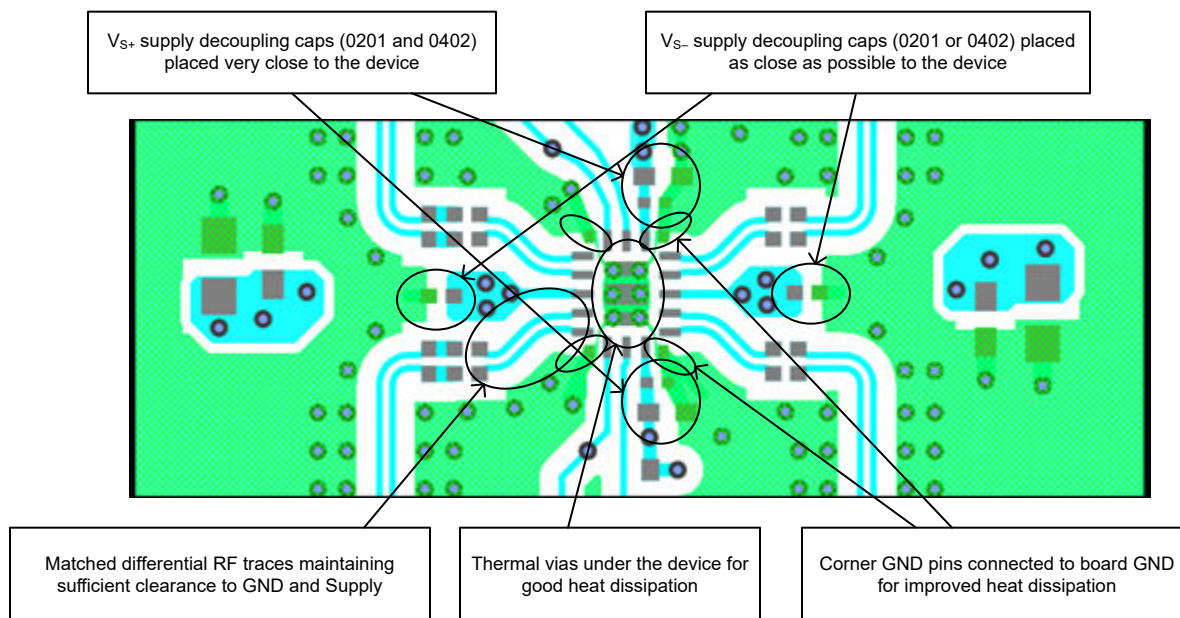


図 8-10. Layout Example: TRF1305x2 With Differential Input

The TRF1305x2 can be evaluated using EVM boards that can be ordered from the [TRF1305B2](#) product folder. For more information about the evaluation board construction and test setup, see the [TRF1305 EVM User's Guide](#).

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRF1305B2RYPR	Active	Production	VQFN-FCRLF (RYP) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1305B2
TRF1305B2RYPR.A	Active	Production	VQFN-FCRLF (RYP) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1305B2

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

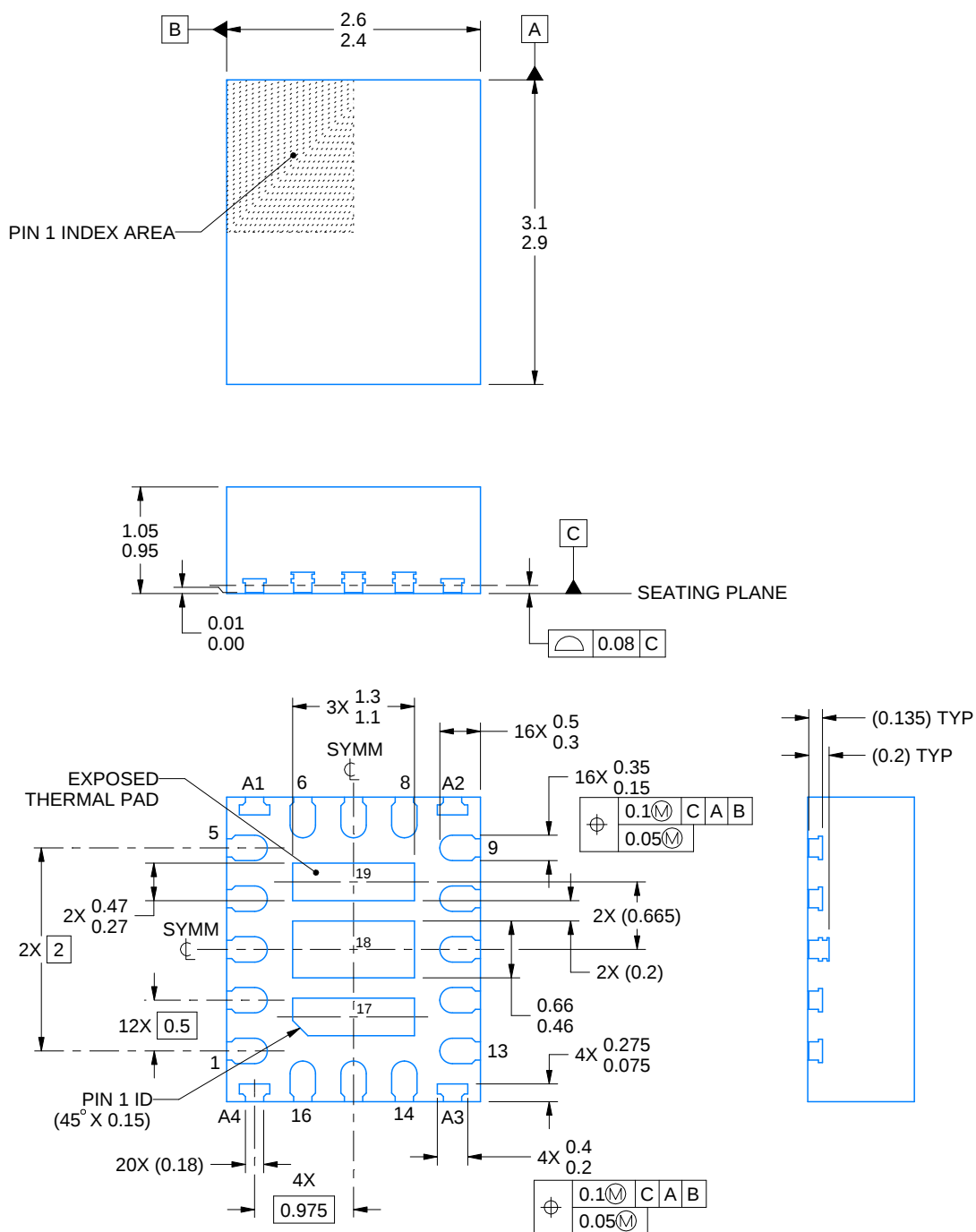
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4226528/D 04/2024

NOTES:

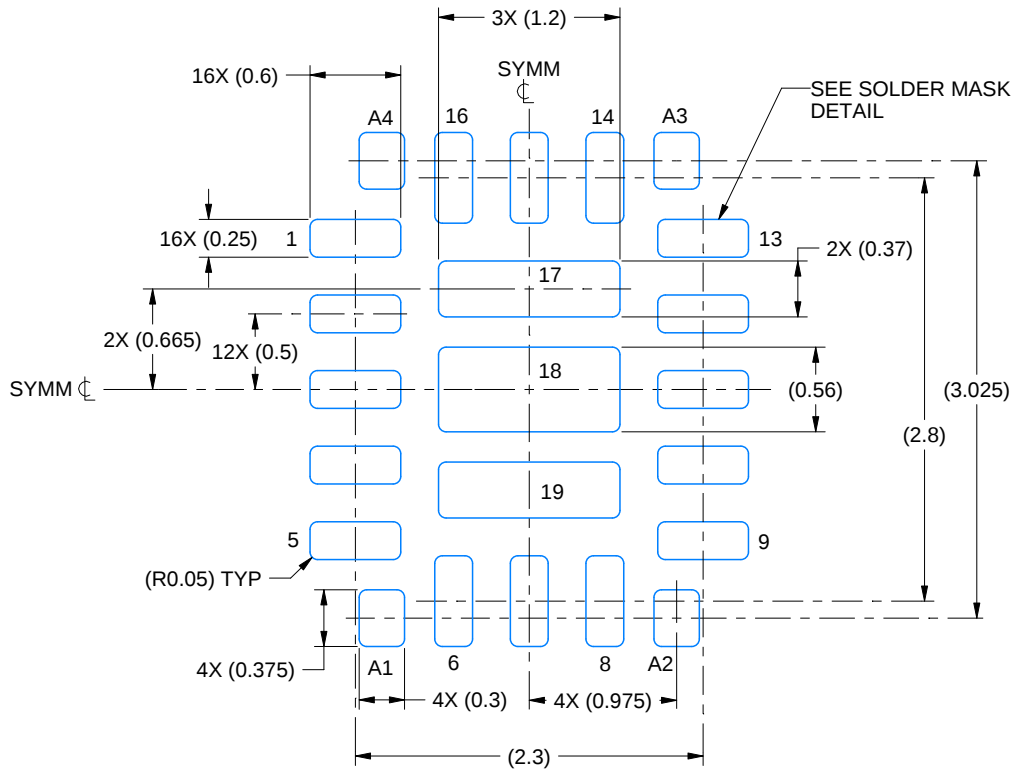
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

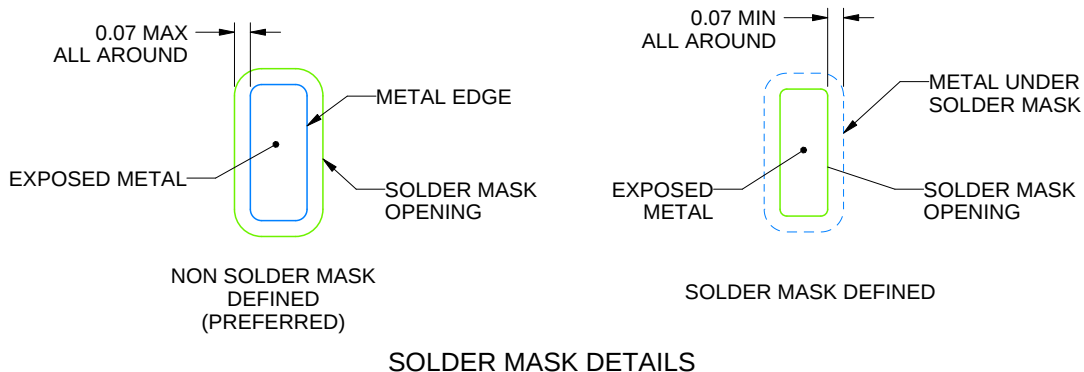
RYP0016A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

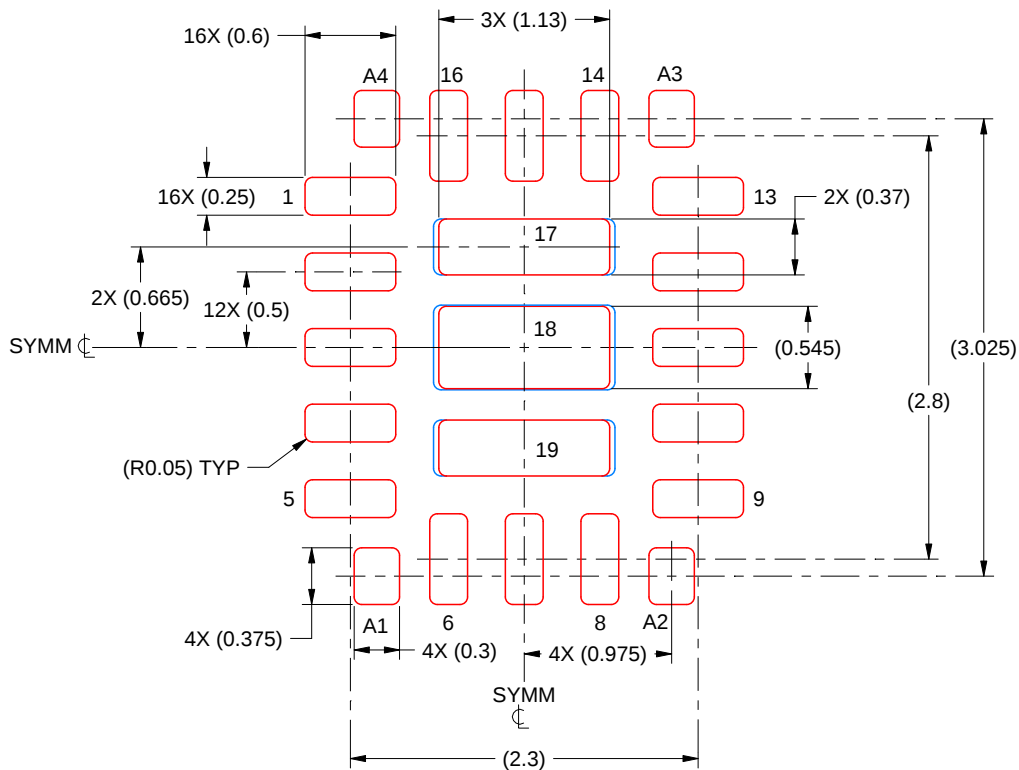
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RYP0016A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 17 & 19: 94%
PAD 18: 92%

4226528/D 04/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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