TPSM84203、TPSM84205、TPSM84212 1.5A、28V入力、TO-220パワー・モジュール

1 特長

- 完全に統合された電源ソリューション
- 3ピンTO-220の外形
- 最高95%の効率
- 固定出力電圧オプション:
  3.3V、5V、12V
- 400kHzのスイッチング周波数
- 高度なEco-mode™パルス・スキップ
- プリバイアス出力によるスタートアップ
- 過電流保護
- 出力過電圧保護
- サーマル・シャットダウン
- 動作時の接合部温度範囲: -40℃～+125℃
- 動作時周囲温度範囲: -40℃～+85℃
- EN55022 Class Bの放射規格に準拠
- WEBENCH® Power Designerにより、TPSM84203を使用するカスタム設計を作成

2 アプリケーション

- 12V、24Vの分散パワー・バス電源
- 業務用白物家電
- コンシューマ
  - オーディオ
  - STB、DTV
  - プリンタ

3 概要

TPSM842xxパワー・モジュールは使いやすい統合電源ソリューションで、1.5AのDC/DCコンバータとパワーMOSFET、インダクタ、受動部品を、3ピンのスルーホール・パッケージに搭載した製品です。この総合的な電源ソリューションは、入力と出力のコンデンサを追加するだけで動作し、設計プロセスでループ補償や磁気部品の選択が不要になります。

標準のTO-220ピン配置なので、この業界標準サイズにパッケージされているリニア・レギュレータを置き換えることで、性能を大きく向上させることができます。TPSM842xxデバイスははるかに効率が高く、ヒートシンクを必要としません。

製品情報(1)

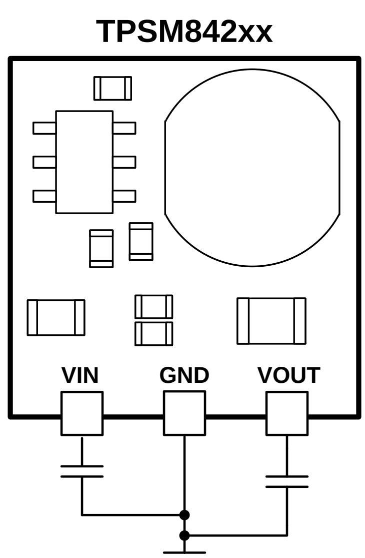
型番	パッケージ	本体サイズ(公称)
TPSM84203	EAB	10mm×11mm
TPSM84205		
TPSM84212		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイスの比較

型番	出力電圧
TPSM84203	3.3V
TPSM84205	5.0V
TPSM84212	12.0V

アプリケーション概略図



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4 改訂履歴

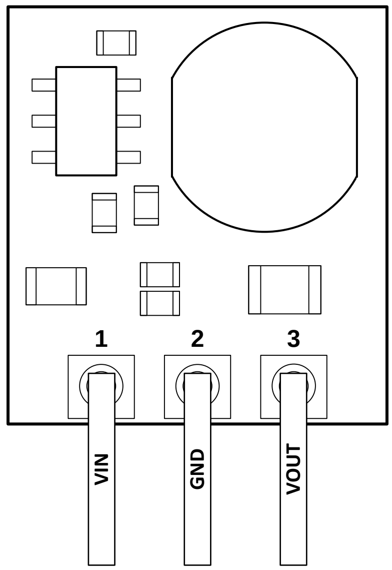
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年7月発行のものから更新 **Page**

- 「*特長*」に、EN55022 Class Bの放射規格を満たすことを追記 ... 1
- Added the *EMI* section ... 16

5 Pin Configuration and Functions

EAB Package
3-Pin Through-Hole
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2		Ground. This is the return current path for the power stage of the device. Connect this pin to the bypass capacitors associated with VIN and VOUT.
VIN	1	I	Input Voltage. This pin supplies voltage to the control circuitry and power switches of the converter. Connect external bypass capacitors between this pin and GND.
VOUT	3	O	Output Voltage. This pin is connected to the internal output inductor. Connect this pin to the output load and connect external bypass capacitors between this pin and GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		MIN	MAX	UNIT
Input Voltage		–0.3	30	V
Output Voltage	TPSM84203	–0.3	3.9	V
	TPSM84205	–0.3	5.7	V
	TPSM84212	–0.3	13.0	V
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		10	G
Operating IC Junction Temperature range, T_J [2]		–40	125	°C
Operating Ambient Temperature range, T_A [2]		–40	85	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
V_{IN}	Input voltage	TPSM84203	4.5	28	V
		TPSM84205	7	28	V
		TPSM84212	14.5	28	V
I_{OUT}	Output current		0	1.5	A
T_A	Operating ambient temperature range[1]		–40	85	°C
T_J	Operating junction temperature range[1]		–40	125	°C

(1) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC[1]		TPSM842xx EAB 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter [3]	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter [4]	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics paper.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 50 mm × 50 mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the controller IC.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the module board 1 mm from the controller IC.

6.5 Electrical Characteristics

Over -40°C to +85°C free-air temperature range, V_{IN} = 24 V, I_{OUT} = I_{OUT} max, F_{SW} = 400 kHz, C_{IN} = 0.1µF, 50V ceramic; 10µF, 50V ceramic; 100µF, 35V electrolytic, and C_{OUT} = 2 x 47µF, 16V 1210 ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)							
V_{IN}	Input voltage range	Over V_{OUT} range	TPSM84203	4.5[1]		28	V
			TPSM84205	7[1]		28	V
			TPSM84212	14.5[1]		28	V
V_{IN_UVLO}	V_{IN} under voltage lock out	V_{IN} increasing			4.1	4.4	V
		V_{IN} decreasing		3.3	3.6		V
OUTPUT VOLTAGE (VOUT)							
V_{OUT}	Output voltage	Over I_{OUT} range	TPSM84203		3.3		V
			TPSM84205		5.0		V
			TPSM84212		12.0		V
	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0 A		–3%		+3%	
	Temperature variation[2]	–40°C ≤ T_A ≤ 85°C, I_{OUT} = 0 A			0.4%		
	Line regulation	Over V_{IN} range, I_{OUT} = 1 A			0.4%		
	Load regulation	Over I_{OUT} range			0.5%		
	Output voltage ripple	20 MHz bandwidth, peak-to-peak, I_{OUT} > 500 mA			15		mV
OUTPUT CURRENT							
I_{OUT}	Output current	See SOA graph for derating over temperature.		0		1.5	A
	Overcurrent threshold				3.1		A
PERFORMANCE							
η	Efficiency[3]	V_{IN} = 5 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		92%		
		V_{IN} = 12 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		91%		
			V_{OUT} = 5.0 V		92%		
		V_{IN} = 24 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		87%		
			V_{OUT} = 5.0 V		90%		
			V_{OUT} = 12.0 V		94%		
	Transient response[2]	1 A/µs load step, 25% to 75% IOUT(max), COUT= 94 µF	V_{OUT} over/undershoot		4%		V_{OUT}
			Recovery time		100		µs

(1) The minimum input voltage is the lowest ensured voltage that will produce the nominal output voltage. See the Drop-Out Voltage section for information on drop-out voltage.
(2) Specified by design. Not production tested.
(3) See the efficiency graphs in the Typical Characteristics section for efficiency over the entire load range.

Electrical Characteristics (continued)

Over -40°C to +85°C free-air temperature range, V_{IN} = 24 V, I_{OUT} = I_{OUT} max, F_{SW} = 400 kHz, C_{IN} = 0.1µF, 50V ceramic; 10µF, 50V ceramic; 100µF, 35V electrolytic, and C_{OUT} = 2 x 47µF, 16V 1210 ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SOFT START							
T_{SS}	Internal soft start time(2)				5		ms
THERMAL SHUTDOWN							
	Rising threshold(2)				165		°C
	Hysteresis(2)				10		°C
CAPACITANCE							
C_{IN}	External input capacitance	Ceramic type		10			µF
		Non-ceramic type		0	100		µF
C_{OUT}	External output capacitance	Ceramic type	TPSM84203	94		470	µF
			TPSM84205				
			TPSM84212	47		470	µF
		Total output capacitance		0		500(4)	µF
		Equivalent series resistance (ESR)				35	mΩ

(4) The maximum output capacitance of 500 µF includes the combination of both ceramic and non-ceramic capacitors.

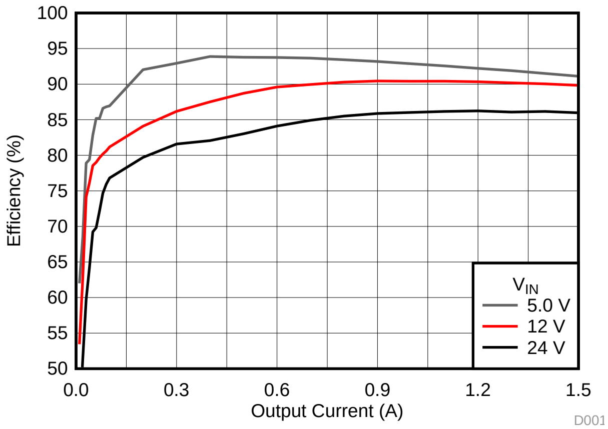
6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW}	Switching frequency		290	400	510	kHz

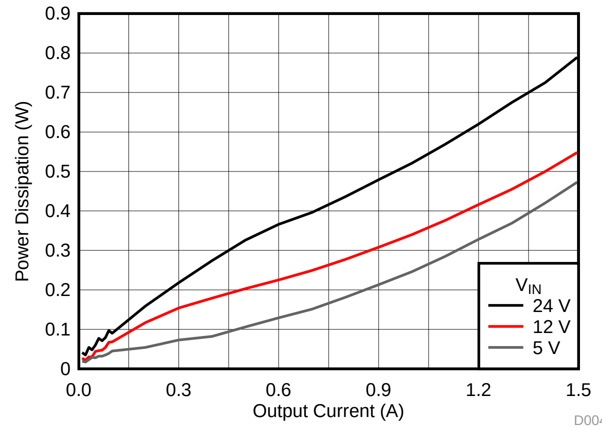
6.7 Typical Characteristics (V_{OUT} = 3.3 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



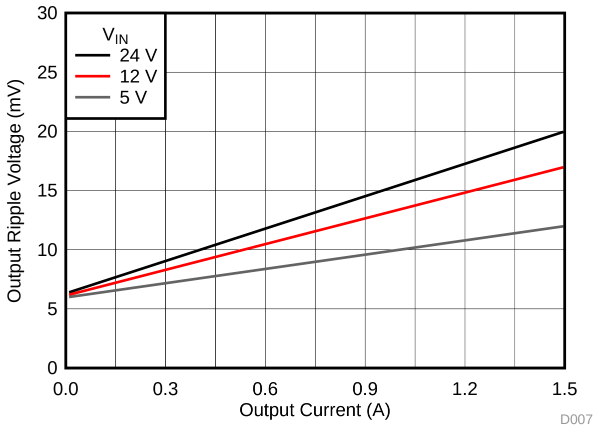
V_{OUT} = 3.3 V

図 1. Efficiency vs Output Current



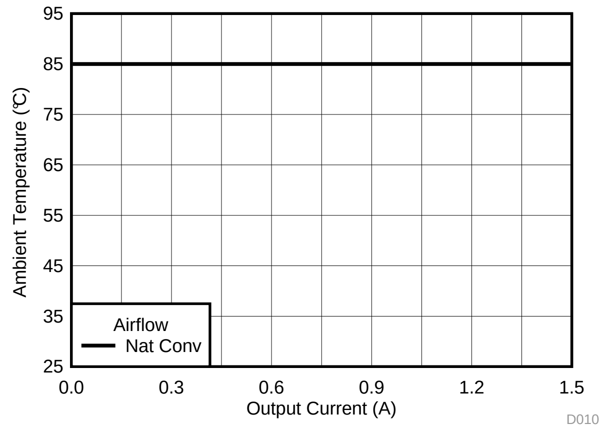
V_{OUT} = 3.3 V

図 2. Power Dissipation vs Output Current



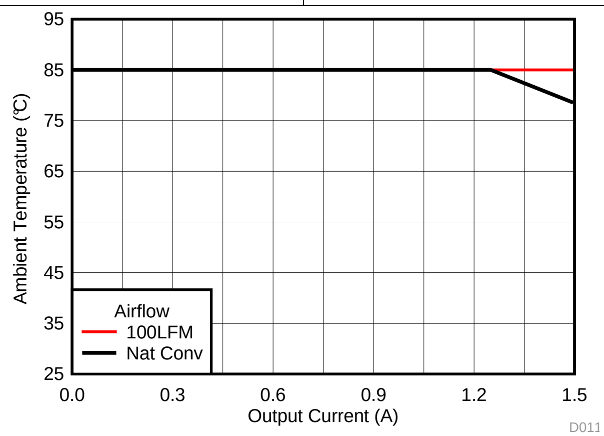
V_{OUT} = 3.3 V C_{OUT} = 2x 47 µF

図 3. Ripple Voltage vs Output Current



V_{OUT} = 3.3 V V_{IN} ≤ 15 V

図 4. Safe Operating Area

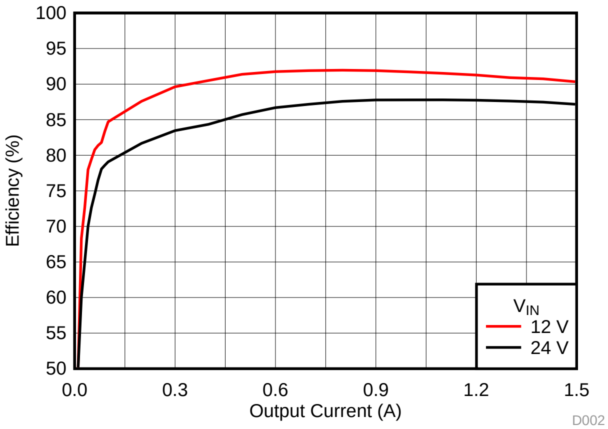


V_{OUT} = 3.3 V V_{IN} = 24 V

図 5. Safe Operating Area

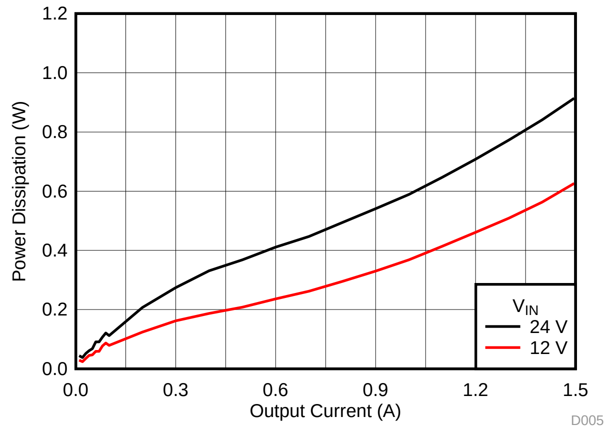
6.8 Typical Characteristics (V_{OUT} = 5 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



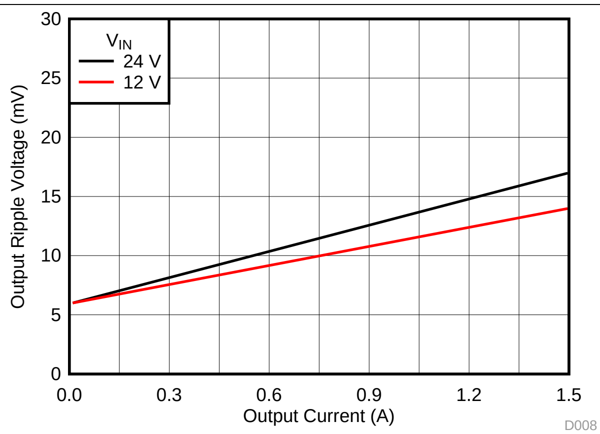
V_{OUT} = 5 V

図 6. Efficiency vs Output Current



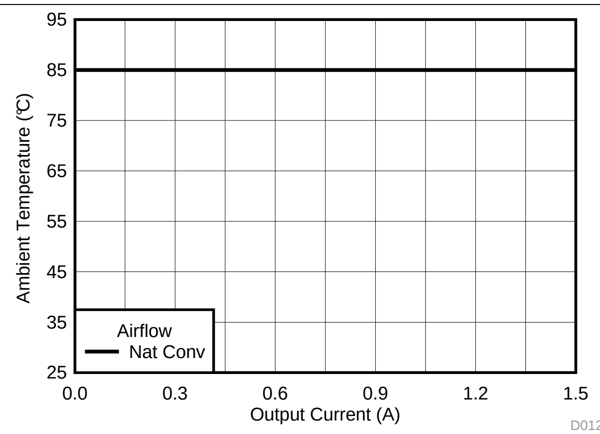
V_{OUT} = 5 V

図 7. Power Dissipation vs Output Current



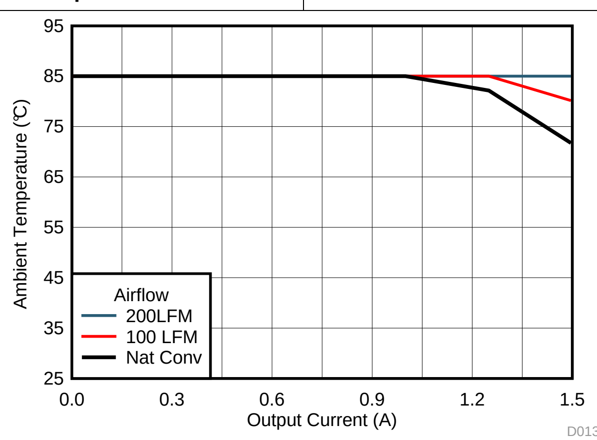
V_{OUT} = 5 V C_{OUT} = 2x 47 µF

図 8. Ripple Voltage vs Output Current



V_{OUT} = 5 V V_{IN} ≤ 15 V

図 9. Safe Operating Area

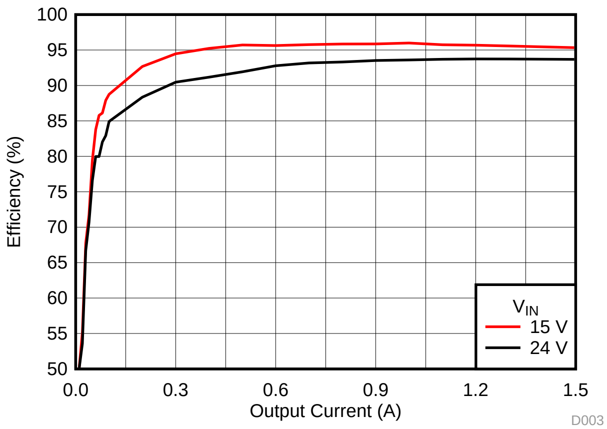


V_{OUT} = 5 V V_{IN} = 24 V

図 10. Safe Operating Area

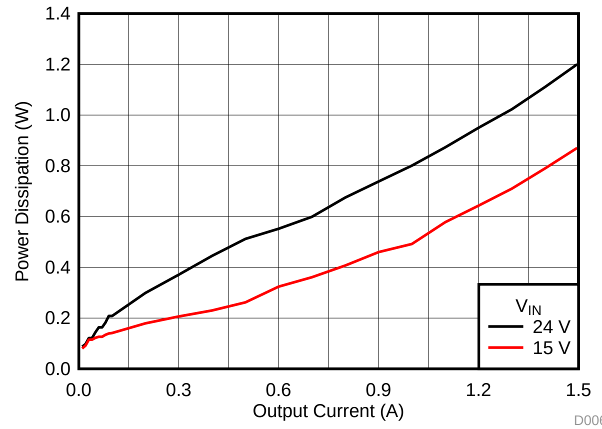
6.9 Typical Characteristics (V_{OUT} = 12 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



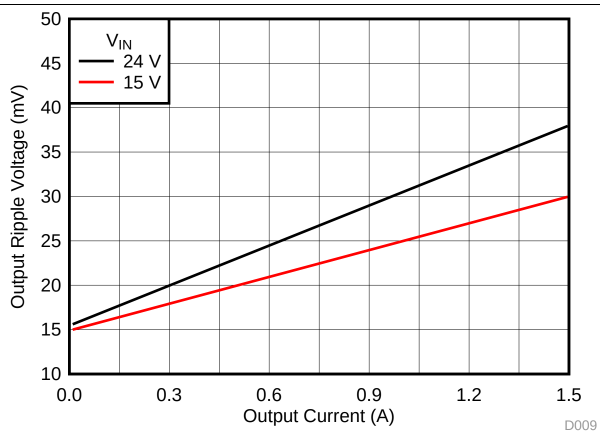
V_{OUT} = 12 V

図 11. Efficiency vs Output Current



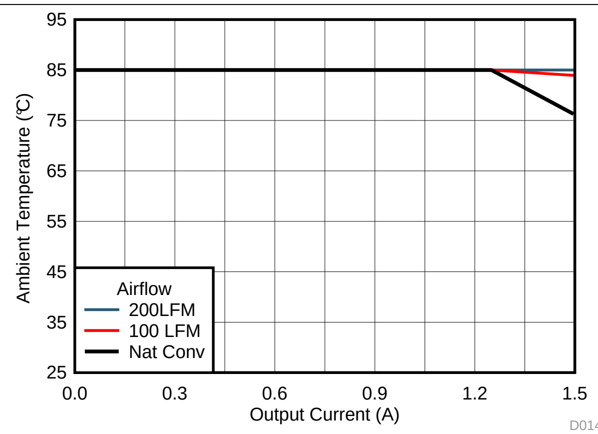
V_{OUT} = 12 V

図 12. Power Dissipation vs Output Current



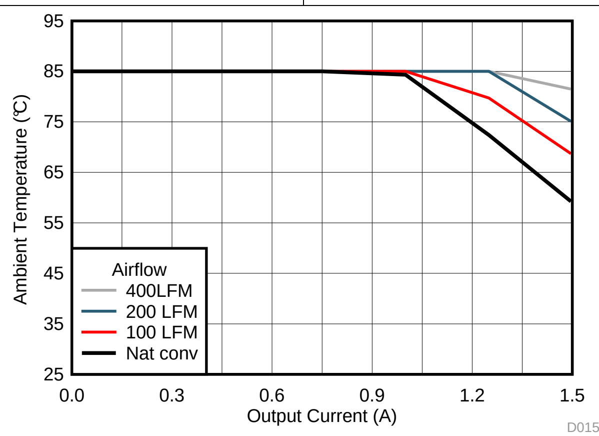
V_{OUT} = 12 V C_{OUT} = 1x 47 µF

図 13. Ripple Voltage vs Output Current



V_{OUT} = 12 V $V_{IN} \leq 15$ V

図 14. Safe Operating Area



V_{OUT} = 12 V V_{IN} = 24 V

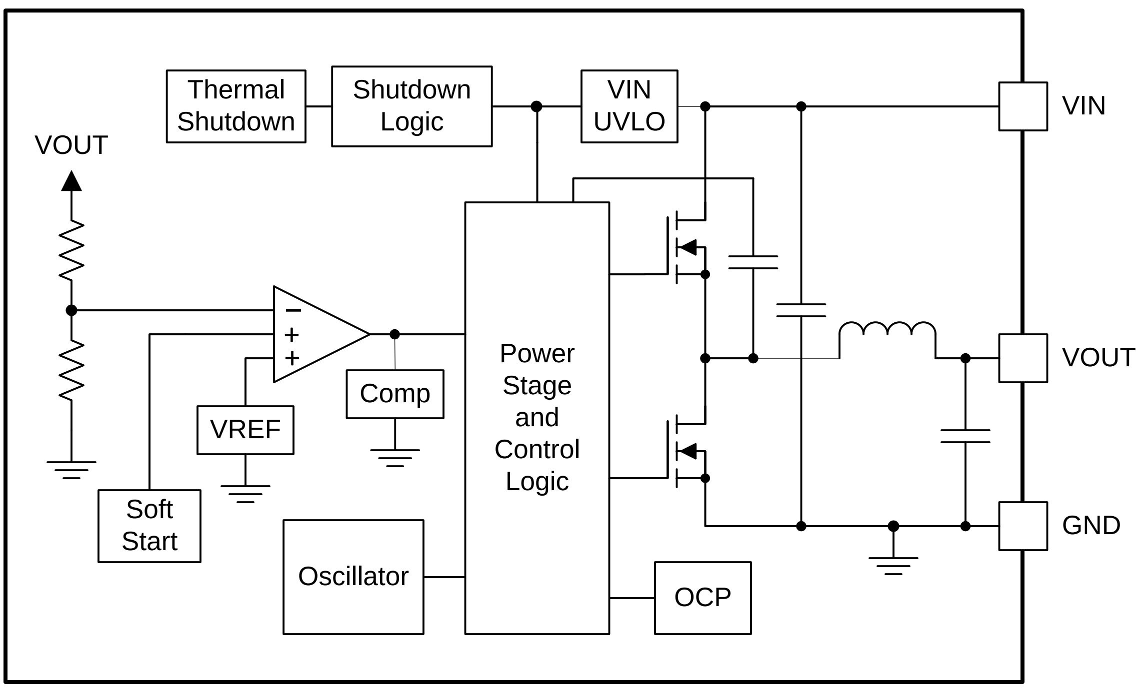
図 15. Safe Operating Area

7 Detailed Description

7.1 Overview

The TPSM84203, TPSM84205, and TPSM84212 devices are 28 V input, 1.5 A, synchronous step down converters with PWM, MOSFETs, inductor, and control circuitry integrated into a TO-220 footprint package. The device integration enables small designs, while improving efficiency over a traditional linear regulator design. The TPSM842xx family provides fixed output voltages of 3.3 V, 5.0 V and 12.0 V. The fixed 400 kHz (typ) switching frequency allows small size and low output voltage ripple. Under light load conditions, these devices are designed to operate in high-efficiency pulse-skipping mode. These devices provide accurate voltage regulation for a variety of loads by using a precision internal voltage reference. These devices have been designed to safely start up into a pre-biased output voltage. Thermal shutdown and current limit features protect the device during an overload condition. The 3-pin, TO-220 footprint package offers improved performance over traditional linear regulators packaged in the standard footprint.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Capacitors

The TPSM842xx devices require a minimum input capacitance of 10 μF of ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 μF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

表 1. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (μF)	ESR(3) (mΩ)
Murata	X7R	GRM32ER71H475KA88L	50	4.7	2
TDK	X5R	C3225X5R1H106K250AB	50	10	3
Murata	X7R	GRM32ER71H106KA12	50	10	2
TDK	X7R	C3225X7R1H106M250AB	50	10	3
Panasonic	ZA	EEHZA1H101P	50	100	28

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Standard capacitance values
(3) Maximum ESR @ 100kHz, 25°C.

7.3.2 Output Capacitors

The TPSM84203 and TPSM84205 devices require a minimum output capacitance of 94 μF (2x 47 μF) of ceramic type. The TPSM84212 device requires a minimum output capacitance of 47 μF of ceramic type. High-quality X5R or X7R ceramic capacitors with sufficient voltage rating are recommended. Additional output capacitance is recommended for applications with transient load requirements. The voltage rating of output capacitors must be greater than the maximum output voltage.

表 2. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (μF)	ESR(3) (mΩ)
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12
Panasonic	POSCAP	6TPF330M9L	6.3	330	9
Panasonic	POSCAP	16TQC47MYFD	16	47	55

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Standard capacitance values.
(3) Maximum ESR @ 100kHz, 25°C.

7.3.3 Drop-Out Voltage

The drop-out voltage of a voltage regulator is the difference between the input voltage and the output voltage that is required to maintain regulation. 図 16 and 図 17 show typical drop-out voltage graphs for TPSM84205 at ambient temperatures of 25°C and 85°C. 図 18 and 図 19 show typical drop-out voltage graphs for TPSM84212 at ambient temperatures of 25°C and 85°C.

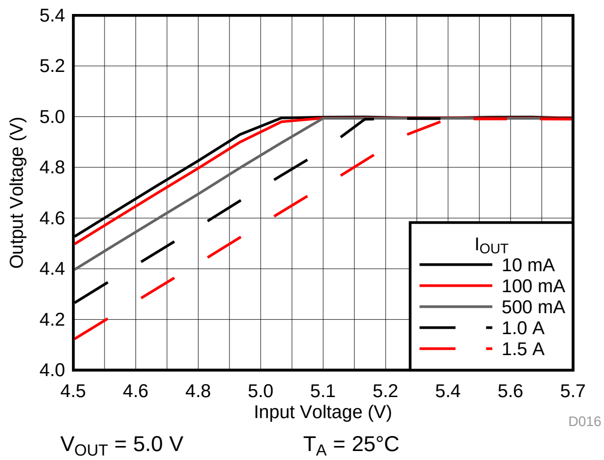


図 16. Drop-Out Voltage

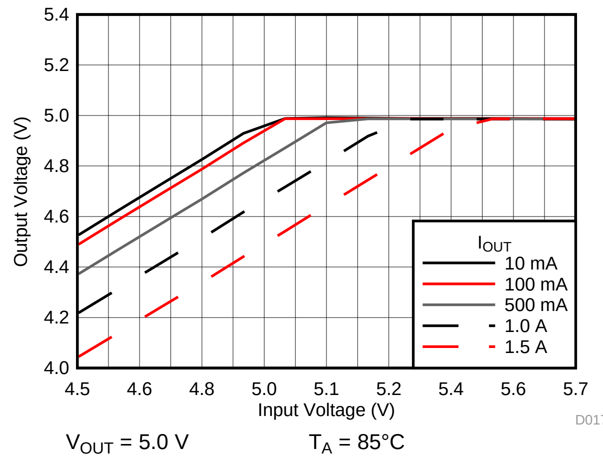


図 17. Drop-Out Voltage

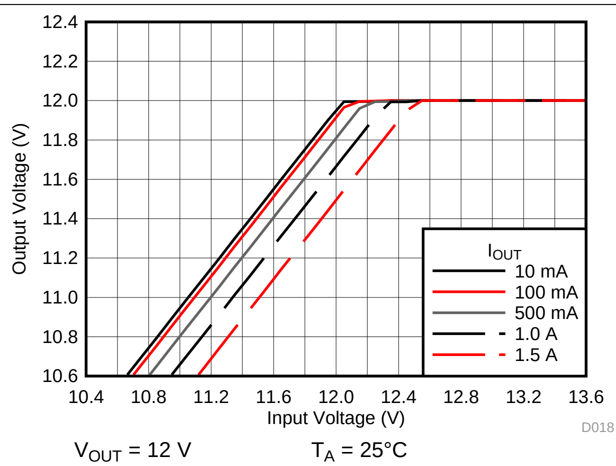


図 18. Drop-Out Voltage

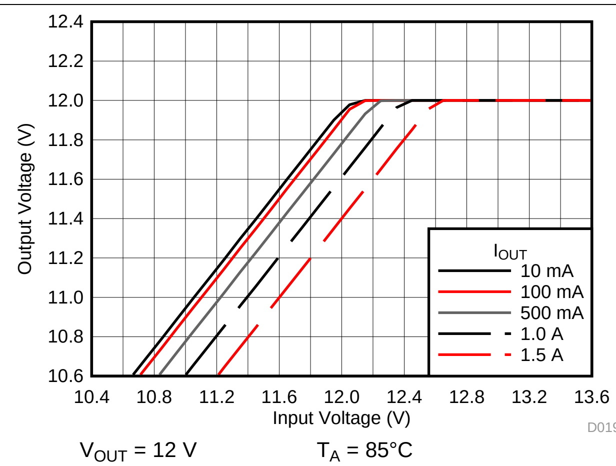


図 19. Drop-Out Voltage

7.3.4 Internal Soft-Start

The device starts up under control of the internal soft-start function. The internal soft start time is set to 5 ms typically.

7.3.5 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than the internal feedback voltage.

7.3.6 Over-Current Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting. If an output overload condition occurs for more than 1.28 ms, the device shuts down and restarts after approximately 40 ms. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.7 Output Over-Voltage Protection

An output over voltage protection circuit is incorporated to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. When the output voltage goes above 108% × V_{OUT}, the high-side MOSFET is forced off. When the output voltage falls below 104% × V_{OUT}, the high-side MOSFET is enabled again.

7.3.8 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 155°C typically.

7.4 Device Functional Modes

7.4.1 Normal Operation

The TPSM842xx devices operate in Normal operation mode when the input voltage is above the minimum input voltage. In Normal operation mode, the device operates in continuous conduction mode (CCM) which occurs when inductor peak current is above 840 mA typically. In CCM, the TPSM842xx devices operate at a fixed frequency of 400 kHz (typ). In addition, to reduce EMI, the devices introduce frequency spread spectrum. The jittering frequency range is ±6% of the switching frequency with a 780 Hz modulation rate.

7.4.2 Eco-mode™ Operation

The TPSM842xx devices operate in Eco-mode operation in light load conditions. Eco-mode is a high-efficiency, pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 840 mA typically. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The device takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM842xx devices are step down DC-DC power modules. They convert a higher DC voltage to a lower DC voltage of 3.3 V, 5 V, or 12 V with a maximum output current of 1.5 A. The following design procedure can be used to select components for the TPSM842xx devices. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. Please visit www.ti.com/WEBENCH for more details.

8.2 Typical Application

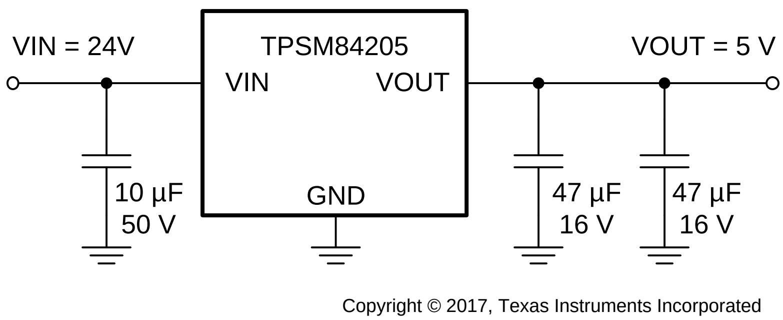


図 20. Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 and follow the design procedures below.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input Voltage V_{IN}	24-V typical
Output Voltage V_{OUT}	5.0 V
Output Current Rating	1.5 A
Key care-abouts	TO-220 footprint, high efficiency

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM84203 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

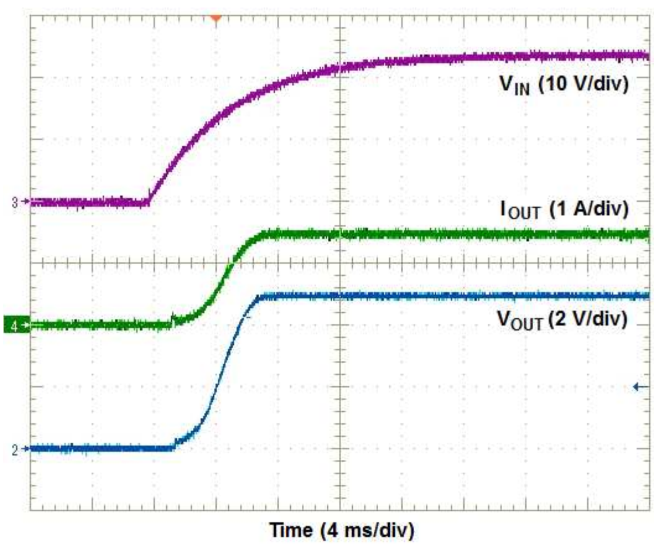
Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Input and Output Capacitors

The TPSM842xx devices require both input and output capacitance for proper operation. The minimum required input capacitance for all of the TPSM842xx devices is 10 µF of ceramic capacitance placed directly at the device pins. The minimum required output capacitance for the TPSM84203 and TPSM84205 is 2× 47 µF of ceramic type. The TPSM84212 requires only one 47 µF ceramic output capacitor. Additional capacitance can be added to improve ripple or transient response.

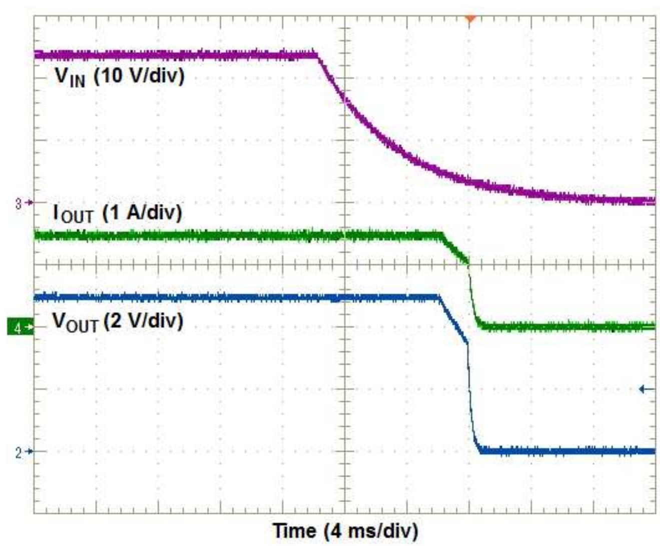
For this application, the minimum required input capacitance of 10 µF, ceramic was added and 2× 47 µF ceramic capacitance was added to the output.

8.2.3 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 1.5 A

図 21. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 1.5 A

図 22. Shut-down Waveforms

8.2.3.1 EMI

The TPSM842xx devices are all compliant with EN55022 Class B radiated emissions. 図 23 to 図 27 show typical examples of radiated emissions plots for the TPSM842xx devices. The EMI plots were taken using a web-orderable EVM with a resistive load. Input power was provided using a lead acid battery. All graphs show plots of the antenna in the horizontal and vertical positions.

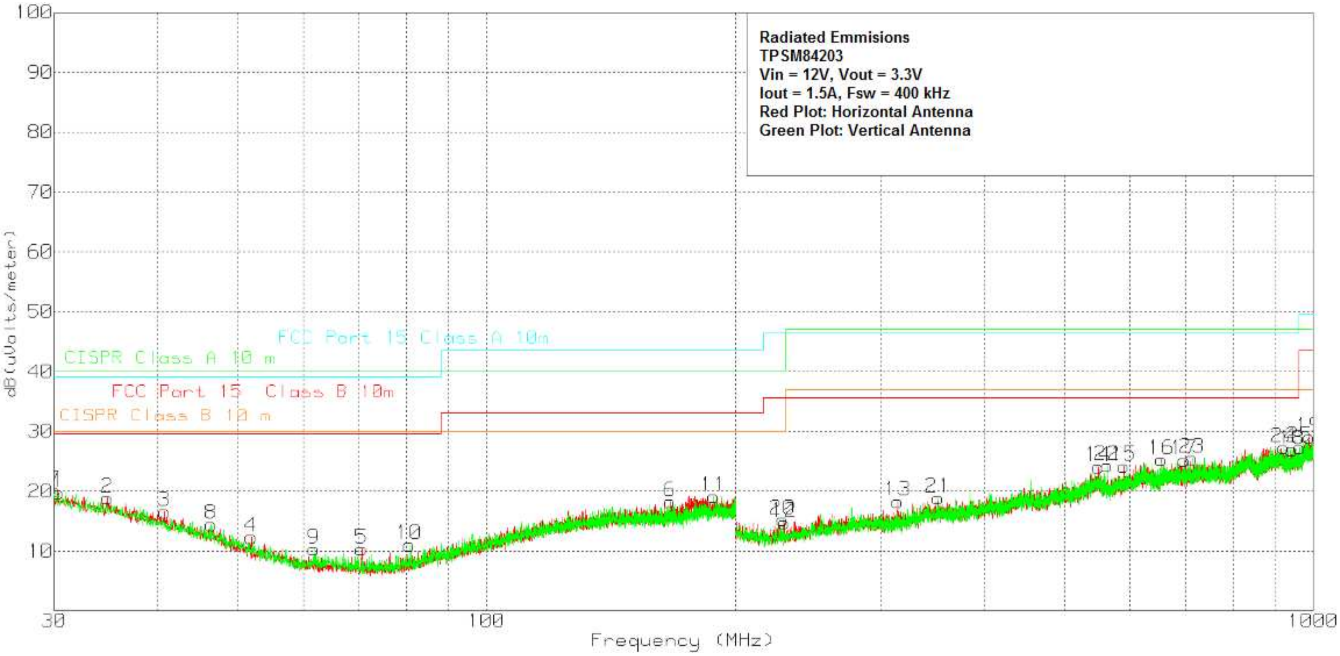


図 23. Radiated Emissions 12-V Input, 3.3-V Output, 1.5-A Load, Horizontal and Vertical Antenna

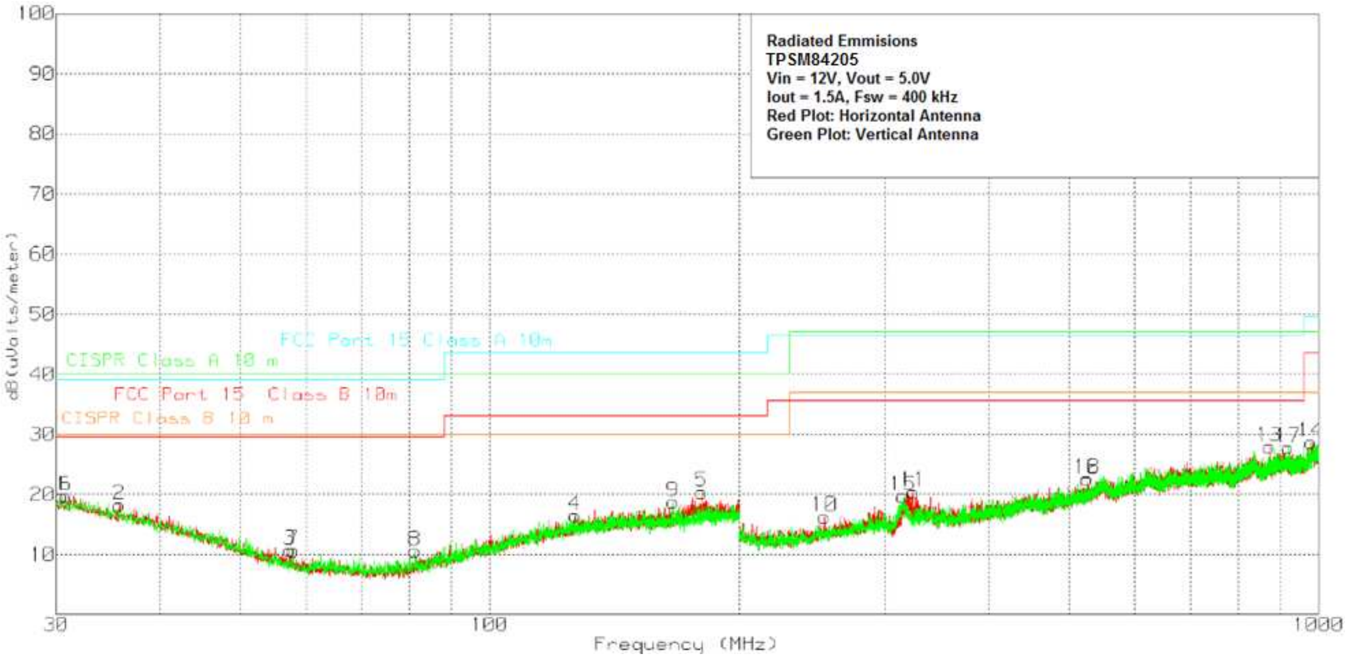


図 24. Radiated Emissions 12-V Input, 5.0-V Output, 1.5-A Load, Horizontal and Vertical Antenna

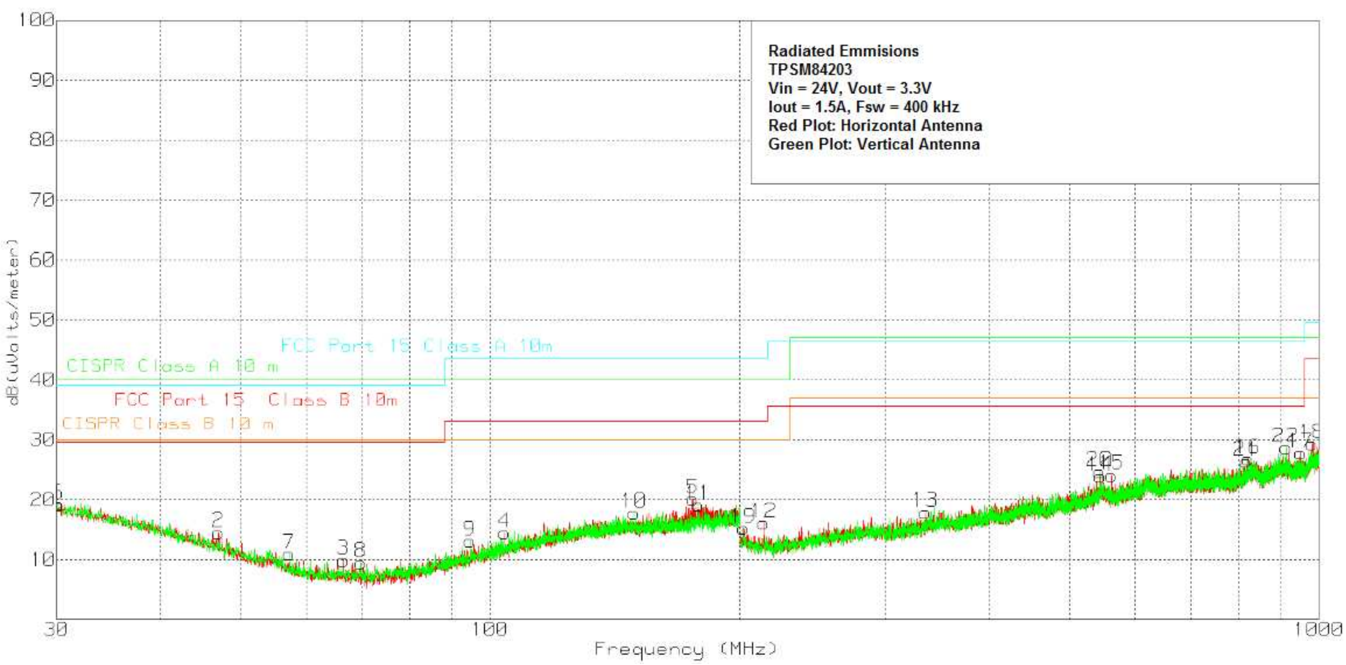


図 25. Radiated Emissions 24-V Input, 3.3-V Output, 1.5-A Load, Horizontal and Vertical Antenna

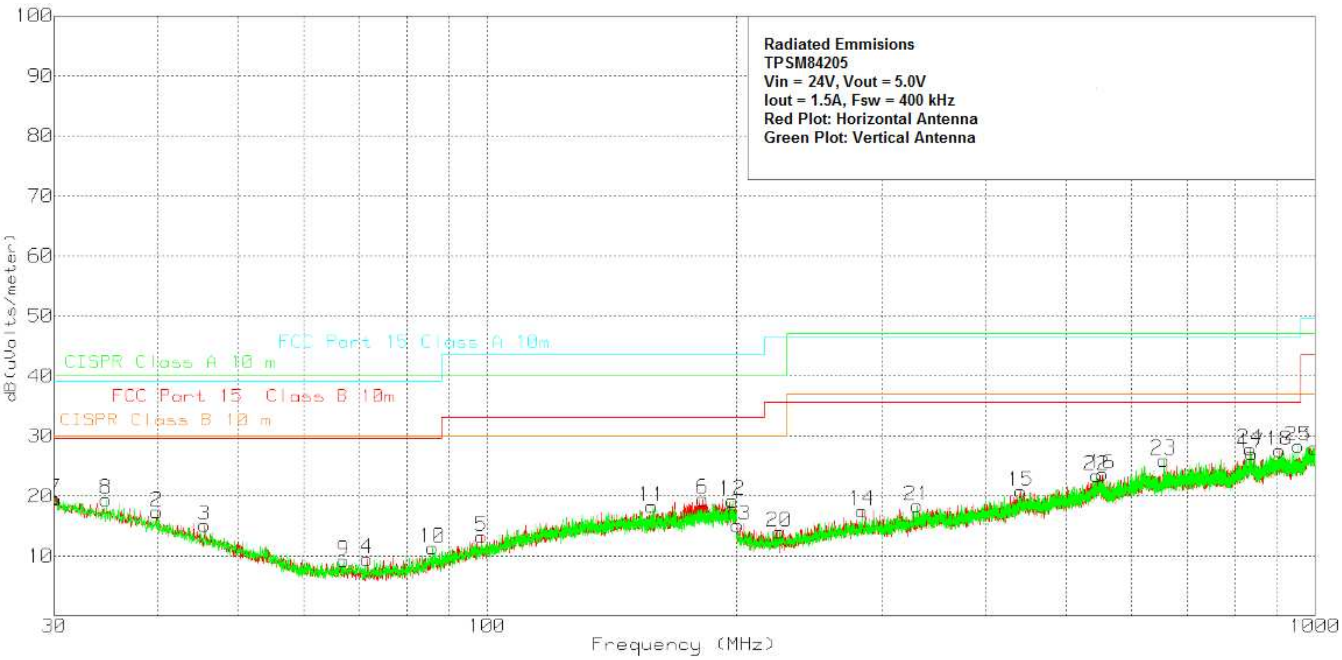


図 26. Radiated Emissions 12-V Input, 5.0-V Output, 1.5-A Load, Horizontal and Vertical Antenna

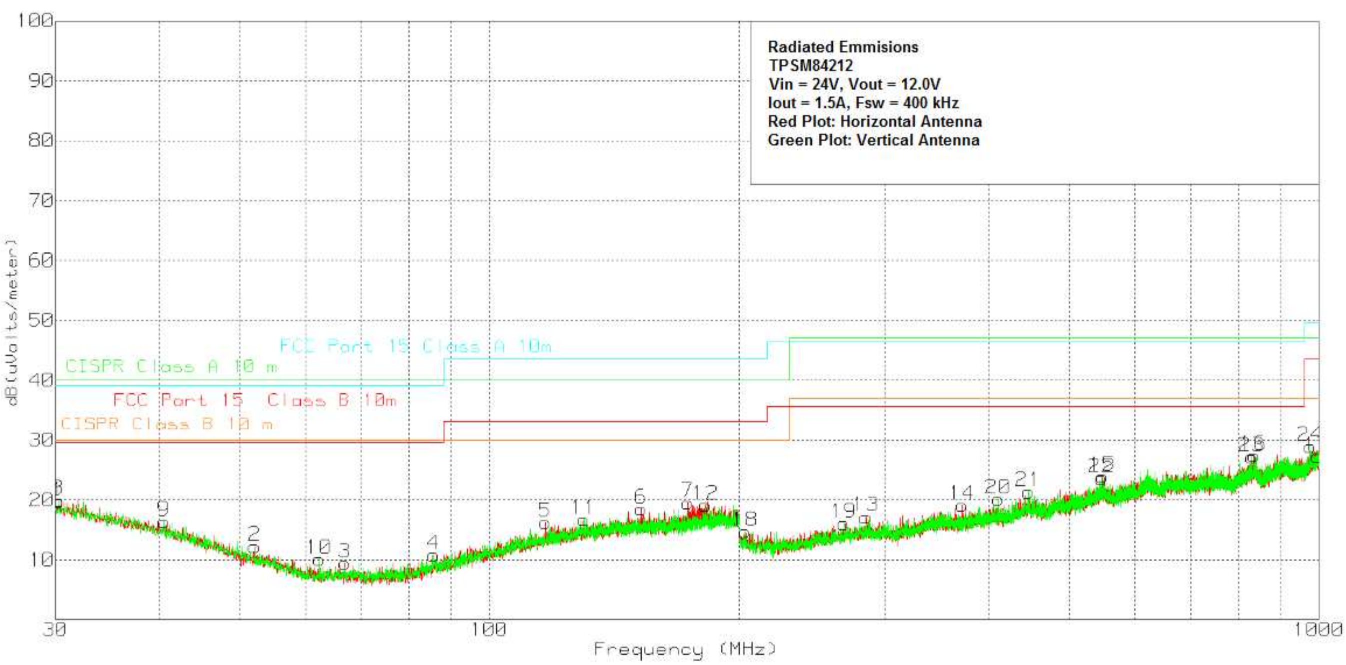


図 27. Radiated Emissions 24-V Input, 12-V Output, 1.5-A Load, Horizontal and Vertical Antenna

9 Power Supply Recommendations

The TPSM842xx devices are designed to operate from an input voltage supply between 4.5 V and 28 V. This supply must be well regulated. Proper bypassing of input supply is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the Layout section.

10 Layout

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 28 shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

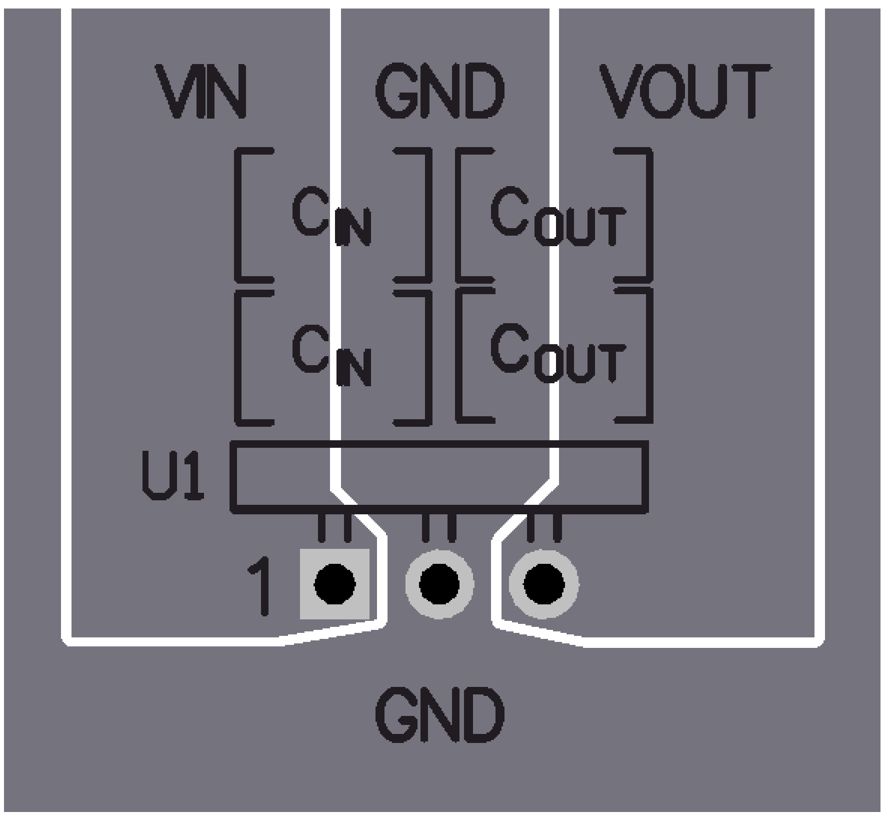


図 28.

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPSM84203デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPSM84203	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPSM84205	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPSM84212	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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11.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM84203EAB	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	
TPSM84203EAB.B	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	
TPSM84205EAB	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	
TPSM84205EAB.B	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	
TPSM84212EAB	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	
TPSM84212EAB.B	Active	Production	SIP MODULE (EAB) | 3	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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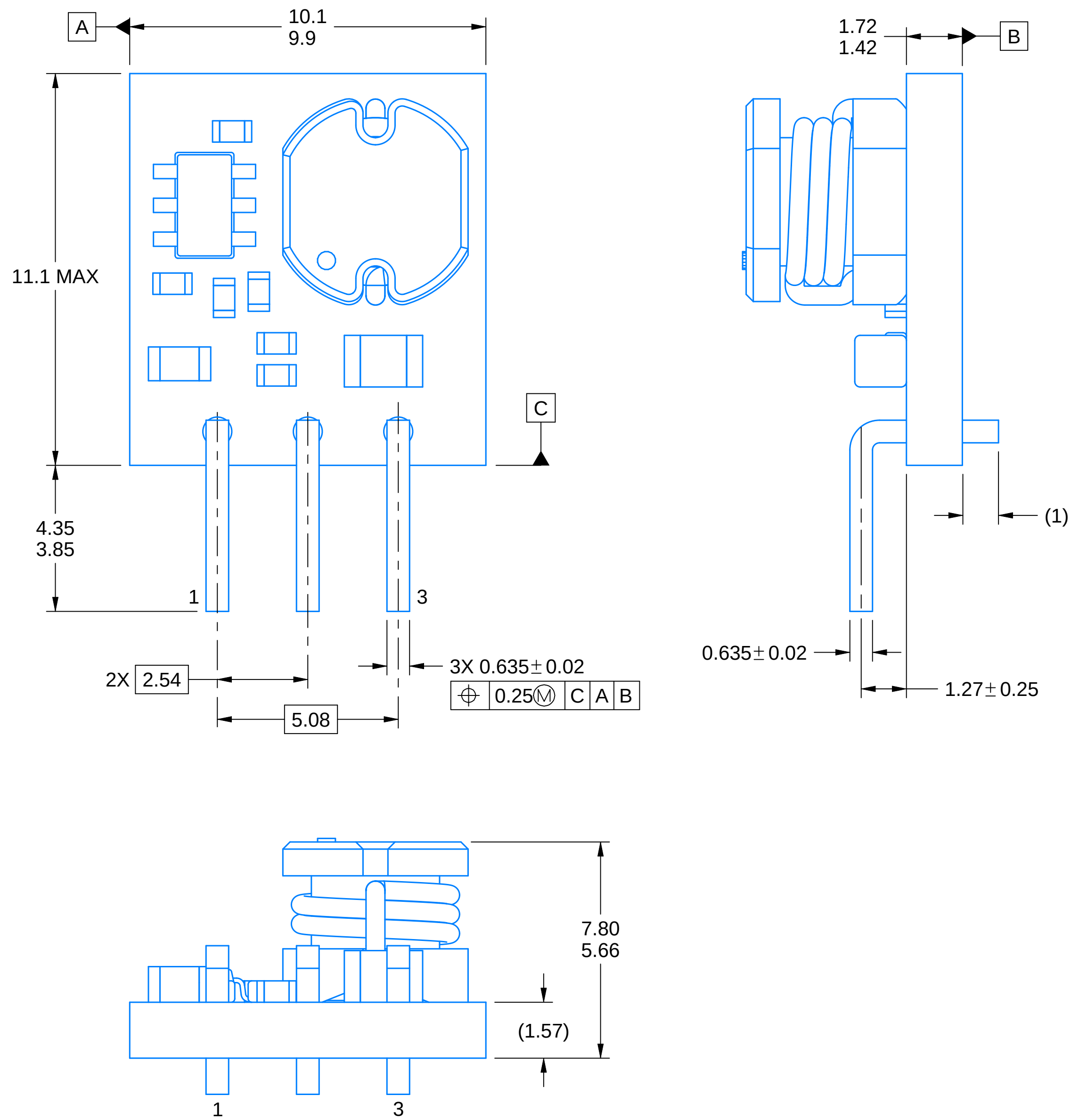
EAB0003A

SIPMODULE - 11.1 mm max height

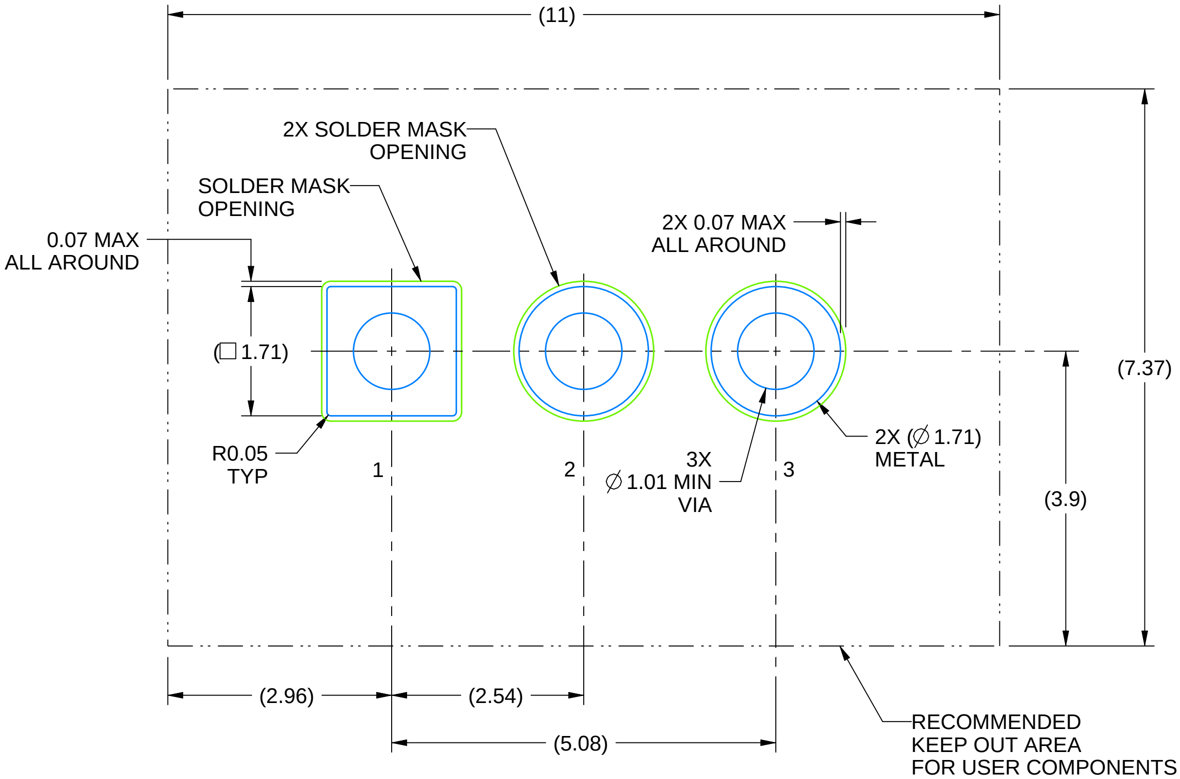
SYSTEM IN PACKAGE MODULE



4223521/D 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Location, size and quantity of each component are for reference only and may vary.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:10X

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2163130	02/07/2017	V. PAKU / T. LEQUANG
B	SIDE VIEW: ADD PIN CENTER TO PCB DIMENSION; REMOVE PIN EDGE TO PCB DIMENSION	2167747	08/14/2017	V. PAKU / K. SINCERBOX
C	4.35/3.85 WAS 4.1/3.5	2169958	11/20/2017	C. FERNANDEZ / K. SINCERBOX
D	1.27± 0.25 WAS 1.27± 0.025;	2208237	04/18/2024	A. VAZQUEZ / K. SINCERBOX

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