TPSI3100-Q1 車載対応、 17V ゲート ドライバ、統合型バイアス電源、デュアル絶縁型コンパレータ内蔵、絶縁型スイッチドライバ

1 特長

- 外部パワー スイッチ (MOSFET、IGBT、SiC FET、SCR) を駆動
- バイアス電源を内蔵し、絶縁型の二次電源は不要
- 1.5/2.5A ピークのソースおよびシンク電流の 17V ゲートドライブ
- 5 kV_{RMS} 強化基本絶縁
- 外部補助回路に対して最大 25mW、5V の電力を供給
- ±1.5% の精度の電圧リファレンスを内蔵したデュアル絶縁型高速コンパレータ
- フォルトおよびアラーム インジケータ用のオープン ドレイン出力
- 車載アプリケーション用に AEC Q-100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 安全関連認証
  - 予定:DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:7070V_{PK}
  - 予定:UL 1577 に準拠した絶縁耐圧:5kV_{RMS} (1 分間)

2 アプリケーション

- ソリッド ステート リレー
- バッテリ マネージメント システム
- オンボード チャージャ
- ハイブリッド / 電気自動車およびパワートレイン システム
- ビル オートメーション
- ファクトリ オートメーション / 制御

3 概要

TPSI3100-Q1 は、統合型の絶縁スイッチ ドライバで、外部パワー スイッチと組み合わせることにより、完全な絶縁型ソリッド ステート リレー ソリューションを形成します。ゲート駆動電圧 17V、ピーク ソース電流 / ピーク シンク電流 1.5A/2.5A という性能を備えているため、さまざまなパワースイッチを使用して多くのアプリケーションのニーズに対応できます。TPSI3100-Q1 は、1 次側で供給された電源によって独自の 2 次バイアス電源を生成するので、絶縁型の 2 次側電源バイアスは不要です。TPSI3100-Q1 は、電流および電圧監視やリモート温度検出などの各種機能を実行するために補助回路で使用する追加電力を公称 5V のレール (VDDM) 経由で供給します。TPSI3100-Q1 の絶縁は非常に堅牢で、従来の機械式リレーやフォトカプラに比べて高信頼性、低消費電力で、温度範囲が広くなっています。

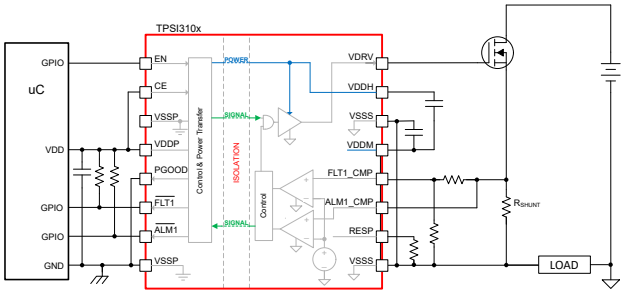
TPSI3100-Q1 には通信バックチャネルが内蔵されており、オープン ドレイン出力の PGOOD (パワー グッド)、$\overline{\text{FLT1}}$ (フォルト 1)、$\overline{\text{ALM1}}$ (アラーム 1) を通じて 2 次側から 1 次側にステータス情報を転送します。$\overline{\text{FLT1}}$ および $\overline{\text{ALM1}}$ のアサートには、共有の電圧リファレンスを内蔵したデュアル高速コンパレータが使用されます。コンパレータ入力 FLT1_CMP が電圧リファレンスを超えると、ドライバが即座に Low にアサートされると共に $\overline{\text{FLT1}}$ も Low に駆動され、フォルトが発生したことがシステムに示されます。これは、過電流検出などの重大なイベントが発生したときに、短いレイテンシで外部スイッチを無効にするのに便利です。コンパレータ入力 ALM1_CMP が電圧リファレンスを超えると、$\overline{\text{ALM1}}$ 信号が Low にアサートされますが、ドライバでは何も行われません。これは、過熱や過電圧のイベントに対するアラームまたは警告インジケータとして役立ちます。

TPSI310xL-Q1 シリーズは、ラッチ ベースのフォルト インジケータを備えています。フォルトが検出されると、ドライバとフォルト インジケータが Low にアサートされ、EN が Low にアサートされるまでラッチされた状態を維持します。TPSI310x-Q1 シリーズには、ラッチなしのフォルト インジケータがあります。フォルト イベントが解消されると、$\overline{\text{FLT1}}$ がデアサートされ、ドライバは指定された回復期間の後で EN ピンの状態に従います。それでもフォルト イベントが解消されない場合、フォルト インジケータとドライバの両方が Low にアサートされたままになります。

製品情報

部品番号	REF (2)	コンパレータ(2)	パッケージ (1)
TPSI3100-Q1	0.31 V	フォルト 1、アラーム 1	DVX (SSOP、16)
TPSI3100L-Q1	0.31 V	ラッチ フォルト 1、アラーム 1	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) 製品比較表を参照してください。



TPSI3100-Q1 の概略回路図

Table of Contents

4 Device Comparison Table

VARIANT	REF	COMPARATORS	LATCHED FAULT
TPSI3100-Q1	0.31V	1 fault, 1 alarm	No
TPSI3103-Q1 (3)	1.23V		
TPSI3100L-Q1	0.31V		Yes
TPSI3103L-Q1 (3)	1.23V		
TPSI3110-Q1 (3)	0.31V	2 faults	No
TPSI3113-Q1 (3)	1.23V		
TPSI3110L-Q1 (3)	0.31V		Yes
TPSI3113L-Q1 (3)	1.23V		
TPSI3120-Q1 (3)	0.31V	2 alarms	N/A(2)
TPSI3123-Q1 (3)	1.23V		
TPSI3133-Q1 (3)	1.23V	1 fault(1), 1 alarm	No

(1) FLT1_CMP input is actively pulled down when EN is low. These devices are useful for overcurrent detection using DESAT techniques primarily with IGBT power transistors.
(2) Non-applicable.
(3) Product preview.

5 Pin Configuration and Functions

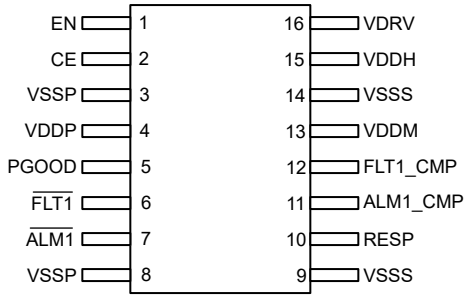


図 5-1. TPSI310x-Q1 and TPSI310xL-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable. Internal 500kΩ pull-down to VSSP.
2	CE	I	—	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500kΩ pull-down to VSSP.
3	VSSP	—	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	—	P	Power supply for the primary side.
5	PGOOD	O	—	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	—	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM1}}$	O	—	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	—	GND	Ground supply for the primary side. All VSSP must be connected to the primary side ground.
9	VSSS	—	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	—	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM1_CMP	I	—	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I	—	Analog comparator input. When FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	—	P	Generated mid-supply, nominal 5V.
14	VSSS	—	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	—	P	Generated high supply, nominal 17V.
16	VDRV	O	—	Active high driver output.

(1) P = power, GND = ground, NC = no connect

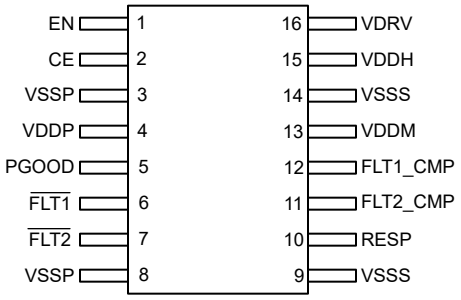


図 5-2. TPSI311x-Q1 and TPSI311xL-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable. Internal 500kΩ pull-down to VSSP.
2	CE	I	—	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500kΩ pull-down to VSSP.
3	VSSP	—	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	—	P	Power supply for the primary side.
5	PGOOD	O	—	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	—	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{FLT2}}$	O	—	Fault 2 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	—	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	—	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	—	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	FLT2_CMP	I	—	Analog comparator input. When FLT2_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT2}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I	—	Analog comparator input. When FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	—	P	Generated mid-supply, nominal 5V.
14	VSSS	—	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	—	P	Generated high supply, nominal 17V.
16	VDRV	O	—	Active high driver output.

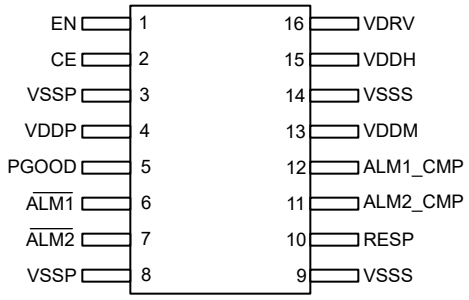


図 5-3. TPSI312x-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable. Internal 500kΩ pull-down to VSSP.
2	CE	I	—	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500kΩ pull-down to VSSP.
3	VSSP	—	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	—	P	Power supply for the primary side.
5	PGOOD	O	—	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{ALM1}}$	O	—	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM2}}$	O	—	Alarm 2 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	—	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	—	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	—	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM2_CMP	I	—	Analog comparator input. When ALM2_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM2}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	ALM1_CMP	I	—	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	—	P	Generated mid-supply, nominal 5V.
14	VSSS	—	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	—	P	Generated high supply, nominal 17V.
16	VDRV	O	—	Active high driver output.

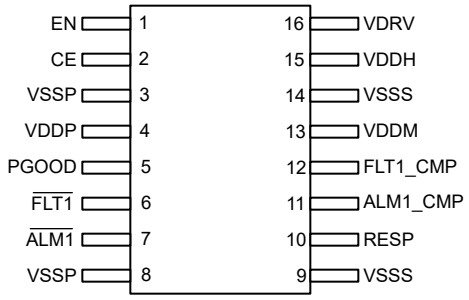


図 5-4. TPSI3133-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable. Internal 500kΩ pull-down to VSSP.
2	CE	I	—	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500kΩ pull-down to VSSP.
3	VSSP	—	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	—	P	Power supply for the primary side.
5	PGOOD	O	—	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	—	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM1}}$	O	—	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	—	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	—	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	—	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM1_CMP	I	—	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I/O	—	Analog comparator input/output. When EN state is low, FLT1_CMP is actively pulled low. If EN state is high and FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 2.8MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	—	P	Generated mid-supply, nominal 5V.
14	VSSS	—	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	—	P	Generated high supply, nominal 17V.
16	VDRV	O	—	Active high driver output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary side supply(2)	VDDP, EN, CE, PGOOD, $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI3133), $\overline{FLT2}$ (TPSI311x), $\overline{ALM1}$ (TPSI310x, TPSI312x, TPSI3133), $\overline{ALM2}$ (TPSI312x)	–0.3	6	V
Secondary side supply(3)	FLT1_CMP (TPSI310x, TPSI311x, TPSI3133), FLT2_CMP (TPSI311x), ALM1_CMP (TPSI310x, TPSI312x, TPSI3133), ALM2_CMP (TPSI312x)	–3	6	V
Secondary side supply(3)	VDRV	–0.3	18	V
	VDDH	–0.3	18	V
	VDDM	–0.3	6	V
	VDDH-VDDM	–0.3	13	V
Secondary side supply(3)	RESP	–0.3	6	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP. Not all signals listed may be present pending device variant.
(3) All voltage values are with respect to VSSS. Not all signals listed may be present pending device variant.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage(1)	4.5		5.5	V
EN	Enable VDRV(1) (1)	0		5.5	V
CE	Chip enable(1)	0		5.5	V
PGOOD	Power good indicator(4) (1)	0		5.5	V
$\overline{FLTn}$	Fault indicator(s).(4) (1) $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI3133) $\overline{FLT2}$ (TPSI311x)	0		5.5	V
$\overline{ALMn}$	Alarm indicator(s).(4) (1) $\overline{ALM1}$ (TPSI310x, TPSI311x, TPSI3133) $\overline{ALM2}$ (TPSI312x)	0		5.5	V
C_{VDDP}	Decoupling capacitance on VDDP and VSSP(3)	1		20	µF

6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.003		15	µF
C_{DIV2} (2)	Decoupling capacitance across VDDM and VSSS(3)	0.1		40	µF
Q_{TOTAL}	Total charge to be driven by VDRV.			2500	nC
R_{RESP}	Comparator response resistor from RESP to VSSS.	0		1000	kΩ
I_{AUX}	Auxiliary current sourced from VDDM.	0		5	mA
T_A	Ambient operating temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geq 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.
(4) Open-drain fail-safe output. When being used, an external pull-up resistor greater than 20kΩ to VDDP is recommended. When not being used, float pin or connect to VSSP.

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE DVX (SSOP) 16 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	82.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	T_A = 25°C, V_{VDDP} = 5.0V, f_{EN} = 1kHz square wave, C_{VDRV} = 1nF			250	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	

6.6 Insulation Specifications (続き)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1200	V_{RMS}
		DC voltage	1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$; t = 1s (100% production test)	8484	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air; 1.2/50µs waveform per IEC 62638-1	9230	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil (qualification test); 1.2/50µs waveform per IEC 62638-1	12000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2036V_{PK}$, t_m = 10s.	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2715V_{PK}$, t_m = 10s.	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3139V_{PK}$, t_m = 1s.	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	3	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500V at T_S =150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the intrinsic surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, $7070V_{PK}$; Maximum repetitive peak isolation voltage, $1697V_{PK}$; Maximum surge isolation voltage, $12000V_{PK}$	Single protection, $5000V_{RMS}$
Certificate planned	Certificate planned

6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 82.5°C/W, V_{VDDP} = 5.5V, T_J = 150°C, T_A = 25°C			275	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ =82.5°C/W, T_J = 150°C, T_A = 25°C			1.52	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
CMTI	Common-mode transient immunity, static.	$\|V_{CM}\|$ = 1000V, V_{EN} = 0V or V_{EN} = 5V.	100			V/ns
TSD	Temperature shutdown	V_{VDDP} = 5V		173		℃
TSDH	Temperature shutdown hysteresis	V_{VDDP} = 5V		32		℃
SUPPLY						
I_{VDDP_STBY}	VDDP current in standby	V_{VDDP} = 5V, EN = 0V, CE = 0V. Measure average current.		25	45	µA
I_{VDDP_LOW}	VDDP average current in steady state	V_{VDDP} = 5V, EN = CE = 5V. Fault and alarm inputs tied to VSSP (device specific). I_{AUX} = 0mA. Lowest power regulation. V_{VDDH} in steady state, measure I_{VDDP}.		5.3		mA
I_{VDDP_HIGH}	VDDP average current in steady state	V_{VDDP} = 5V, EN = CE = 5V. Fault and alarm inputs tied to VSSS (device specific). Highest power regulation. V_{VDDH} in steady state, measure I_{VDDP}.		37		mA
V_{VDDH}	VDDH output voltage	V_{VDDP} = 5V, EN = CE = 5V. Fault and alarm inputs tied to VSSS (device specific).	16	17	18	V
V_{VDDM}	Average VDDM voltage when not sourcing current.	V_{VDDP} = 5V, EN = CE = 5V. Fault and alarm inputs tied to VSSS (device specific).	4.8	5.0	5.2	V
I_{VDDH_STBY}	Average standby current of VDDH supply.	V_{VDDP} = 5V, EN = 0V, CE = 5V. Fault and alarm inputs tied to VSSS (device specific).		48		µA
I_{VDDM_STBY}	Average standby current of VDDM supply.	V_{VDDP} = 5V, EN = 0V, CE = 5V. Fault and alarm inputs tied to VSSS (device specific).		105		µA
P_{OUT_VDDH}	Maximum power transfer to VDDH.	V_{VDDP} = 5V, EN = 0V, CE = 5V.	42	72.8		mW

6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5V, EN = 0V, steady state. Fault and alarm inputs tied to VSSS (device specific). Source I_{AUX} = 5mA from VDDM, measure V_{VDDM}. C_{DIV2} = 1µF	4.7		5.5	V
SUPERVISORY						
$V_{VDDP\_UV\_R}$	VDDP undervoltage threshold rising	VDDP rising.	3.9	4.1	4.35	V
$V_{VDDP\_UV\_F}$	VDDP undervoltage threshold falling	VDDP falling	3.8	3.9	4.25	V
$V_{VDDP\_UV\_HYS}$	VDDP undervoltage threshold hysteresis			170		mV
$V_{VDDH\_UV\_R}$	VDDH undervoltage threshold rising	VDDH rising.	11.9	13	14.2	V
$V_{VDDH\_UV\_F}$	VDDH undervoltage threshold falling.	VDDH falling.	9.6	10.4	11.5	V
$V_{VDDH\_UV\_HYS}$	VDDH undervoltage threshold hysteresis.			2.5		V
$V_{VDDM\_UV\_R}$	VDDM undervoltage threshold rising	VDDM rising.	3.4	3.7	3.9	V
$V_{VDDM\_UV\_F}$	VDDM undervoltage threshold falling.	VDDM falling.	3.1	3.4	3.7	V
$V_{VDDM\_UV\_HYS}$	VDDM undervoltage threshold hysteresis.			0.3		V
DRIVER						
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 5V, EN = 5V. V_{VDDH} in steady state, no DC loading. Fault and alarm inputs tied to VSSS (device specific).	16	17	18	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 5V, EN = 0V, V_{VDDH} in steady state, VDRV sinking 10mA. Fault and alarm inputs tied to VSSS (device specific).			0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 5V, EN = 0V → 5V, V_{VDDH} in steady state, measure peak current. Fault and alarm inputs tied to VSSS (device specific).		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 5V, EN = 5V → 0V, V_{VDDH} in steady state, measure peak current. Fault and alarm inputs tied to VSSS (device specific).		2.5		A

6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_VDRV}	Driver on resistance in low state.	Fault and alarm inputs tied to VSSS (device specific).		1.5		Ω
	Driver on resistance in high state.	Fault and alarm inputs tied to VSSS (device specific).		3.5		Ω
V_{ACT_CLAMP}	Active clamp voltage when engaged.	V_{VDDP} = 0V. Sink I_{VDRV} = 300mA. Measure VDRV.		1.9	2.5	V
DIGITAL INPUT/OUTPUT						
$V_{IT\_+(EN)}$	Input threshold voltage rising on EN.	V_{VDDP} = 5V	2.3	2.5	2.7	V
$V_{IT\_-(EN)}$	Input threshold voltage falling on EN.	V_{VDDP} = 5V	1.7	1.9	2.0	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.	V_{VDDP} = 5V		0.5		V
$V_{IT\_+(CE)}$	Input threshold voltage rising on CE.	V_{VDDP} = 5V	2.3	2.5	2.7	V
$V_{IT\_-(CE)}$	Input threshold voltage falling on CE.	V_{VDDP} = 5V	1.7	1.9	2.0	V
$V_{IT\_HYS(CE)}$	Input threshold voltage hysteresis on CE.	V_{VDDP} = 5V		0.5		V
V_{OL}	Low level output voltage. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI3133) $\overline{FLT2}$ (TPSI311x) $\overline{ALM1}$ (TPSI310x, TPSI312x, TPSI3133) $\overline{ALM2}$ (TPSI32x)	V_{VDDP} = 4.5V to 5.5V, I_{OL} = 2mA. Outputs enabled.			0.4	V
I_{OL}	Low level output current. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI3133) $\overline{FLT2}$ (TPSI311x) $\overline{ALM1}$ (TPSI310x, TPSI312x, TPSI3133) $\overline{ALM2}$ (TPSI312x)	V_{VDDP} = 4.5V to 5.5V, V_{OL} = 0.4V. Outputs enabled.	-2			mA
$V_{OL\_FLT\_CMP}$	Open-drain output, low level output voltage. FLT_CMP1 (TPSI3133)	V_{VDDP} = 4.5V to 5.5V, I_{OL} = 2mA, CE = 1, EN = 0.			0.1	V
$I_{OL\_FLT\_CMP}$	Open-drain output, low level output current. FLT_CMP1 (TPSI3133)	V_{VDDP} = 4.5V to 5.5V, V_{OL} = 0.4V, CE = 1, EN = 0.	-2			mA
I_{LKG}	Leakage current. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI3133) $\overline{FLT2}$ (TPSI311x) $\overline{ALM1}$ (TPSI310x, TPSI312x, TPSI3133) $\overline{ALM2}$ (TPSI312x)	V_{VDDP} = 4.5V to 5.5V, Outputs disabled.			2	µA
$R_{EN\_PULLDOWN}$	Internal resistor pull-down on EN.	V_{VDDP} = 5V	390	500	640	kΩ
$R_{CE\_PULLDOWN}$	Internal resistor pull-down on CE.	V_{VDDP} = 5V	390	500	640	kΩ

6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF}	Internal reference voltage. TPSI3100, TPSI3110, TPSI3120 devices.	T_A = 25°C		0.31		V
	Internal reference voltage. TPSI3103, TPSI3113, TPSI3123, TPSI3133 devices.	T_A = 25°C		1.23		V
V_{REF_TOL}	Internal reference voltage tolerance.		-1.5		1.5	%
COMPARATORS						
$R_{CMP\_PULLDOWN}$	Internal resistor pull-down. FLT1_CMP, ALM1_CMP (TPSI310x, TPS3133) FLT1_CMP, FLT2_CMP (TPSI311x) ALM1_CMP. ALM2_CMP (TPSI312x)		1.3	2.8	3.8	MΩ

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER and DRIVER						
t_{LO_CE}	Low time of CE.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{LO_EN}	Low time of EN.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{PER_EN}	Period of EN.	V_{VDDH}, V_{VDDM} = steady state.	10			µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0V, V_{VDDP} = 0V → 5V at 1V/µs, V_{VDDH} = 7.5V.		145		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 0V → 5V, V_{VDRV} = 13.5V.		3	4.5	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 5V → 0V, V_{VDRV} = 1.5V.		2.5	3.0	µs
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 5V, V_{VDDP} = 5V → 0V at -1V/µs, V_{VDRV} = 1.5V.		140	210	µs
$t_{LH\_VDRV\_CE}$	Propagation delay time from CE rising to VDRV at 10% level	V_{VDDP} = 5V, VDDH and VDDM fully discharged. EN = CE = 0V → 5V, V_{VDRV} = 1.5V.		185		µs
$t_{HL\_VDRV\_CE}$	Propagation delay time from CE falling to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 5V, CE= 5V → 0V, V_{VDRV} = 1.5V.		3	4	µs

6.10 Switching Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF, I_{AUX} = 0mA. 50kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 0V → 5V, V_{VDRV} = 2.25V to 12.75V.		10		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = xV, V_{VDDH}, V_{VDDM} = steady state, EN = xV → 0V, V_{VDRV} = 12.75V to 2.25V.		10		ns
t_{REC_VDRV} (1)	Time VDRV remains low upon detection of a fault condition.	V_{VDDP} = 5V, V_{VDDH} and V_{VDRV} in steady state, EN = 5V, FLTn_CMP positive-pulse of 3V, 50µs pulse-width. Measure from FLTn_CMP going low (1.5V) to V_{VDRV} = 7.5V.		165	270	µs
COMPARATORS						
$t_{PD\_CMP\_VDRV\_DIS}$	Propagation delay time, fault comparator output rising to VDRV asserted low.	EN = CE = VDDP R_{RESP} ≤ 10kΩ V_{UD} = 100mV V_{OD} = 30mV Measure V_{FLT_CMP} crossing V_{REF} to 50% V_{VDRV}.	320	385	460	ns
		EN = CE = VDDP R_{RESP} = 100kΩ. V_{UD} = 100mV V_{OD} = 30mV Measure V_{FLT_CMP} crossing V_{REF} to 50% V_{VDRV}.	630	715	830	ns
		EN = CE = VDDP R_{RESP} = 300kΩ. V_{UD} = 100mV V_{OD} = 30mV Measure V_{FLT_CMP} crossing V_{REF} to 50% V_{VDRV}.	890	1375	1970	ns
		EN = CE = VDDP R_{RESP} = 500kΩ. V_{UD} = 100mV V_{OD} = 30mV Measure V_{FLT_CMP} crossing V_{REF} to 50% V_{VDRV}.	1275	2020	2950	ns
$t_{DEGLITCH\_CMP\_F}$	Fault comparator falling output de-glitch.		4.2	5.7	8	µs
$t_{FLT\_LATENCY}$	Delay from rising or falling event detected by fault comparator and indicated on $\overline{FLT1}$ output.	EN = CE = VDDP R_{RESP} = 500kΩ. V_{UD} = 100mV V_{OD} = 30mV Measure V_{FLT1_CMP} rising or falling and crossing V_{REF} to 50% $\overline{FLT1}$.			30	µs
$t_{ALM\_LATENCY}$	Delay from rising or falling event detected by alarm comparator and indicated on $\overline{ALM1}$ output.	EN = CE = VDDP R_{RESP} = 500kΩ. V_{UD} = 100mV V_{OD} = 30mV Measure V_{ALM1_CMP} rising or falling and crossing V_{REF} to 50% $\overline{ALM1}$.			30	µs

(1) On latched based devices, recovery timer is still in effect even though VDRV is latched low. If the fault condition is removed and EN is asserted low and then high to clear the fault, VDRV will remain asserted low until the recovery timer has elapsed.

6.11 Insulation Characteristic Curves

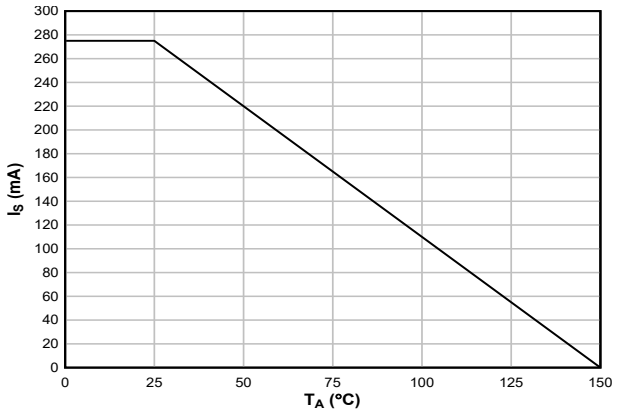


図 6-1. Thermal Derating Curve for Limiting Current per VDE and IEC

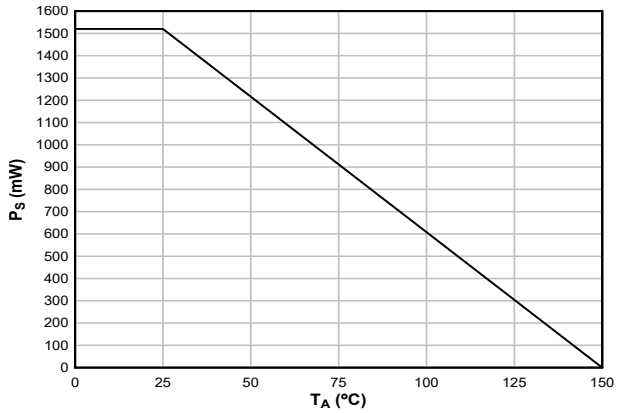
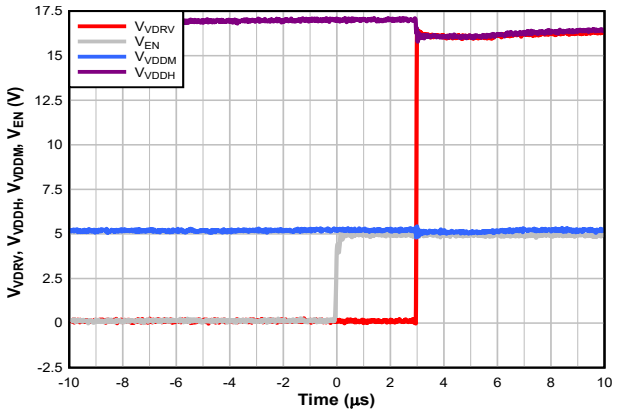


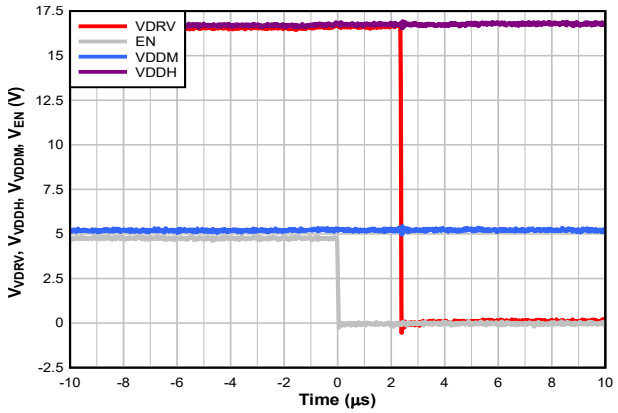
図 6-2. Thermal Derating Curve for Limiting Power per VDE and IEC

6.12 Typical Characteristics



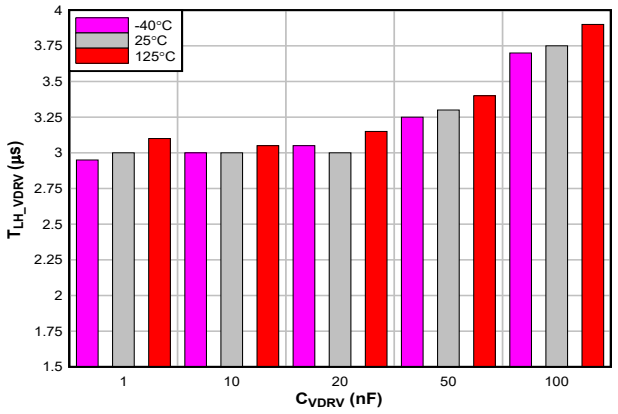
VDDP = 5.0V T_A = 25°C
C_{DIV1} = 47nF C_{DIV2} = 220nF C_{VDRV} = 1nF

図 6-3. t_{LH_VDRV}



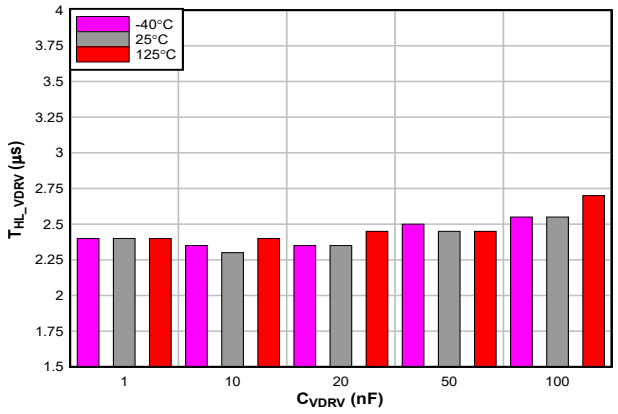
VDDP = 5.0V T_A = 25°C
C_{DIV1} = 47nF C_{DIV2} = 220nF C_{VDRV} = 1nF

図 6-4. t_{HL_VDRV}



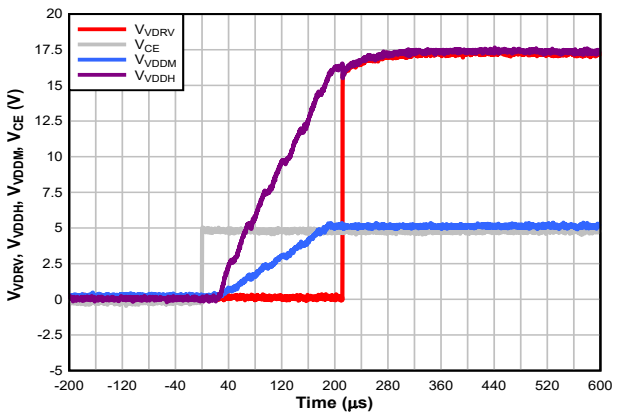
VDDP = 5.0V
C_{DIV1} = 3.3µF C_{DIV2} = 10µF

図 6-5. t_{LH_VDRV} versus C_{VDRV}



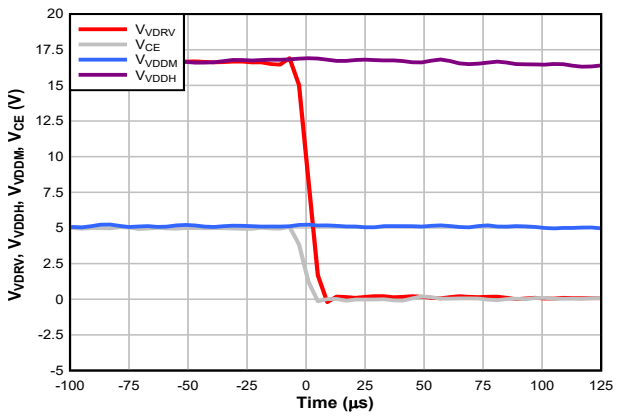
VDDP = 5.0V
C_{DIV1} = 3.3µF C_{DIV2} = 10µF

図 6-6. t_{HL_VDRV} versus C_{VDRV}



VDDP = 5.0V T_A = 25°C R_{RESP} = 100kΩ
C_{DIV1} = 47nF C_{DIV2} = 220nF C_{VDRV} = 1nF

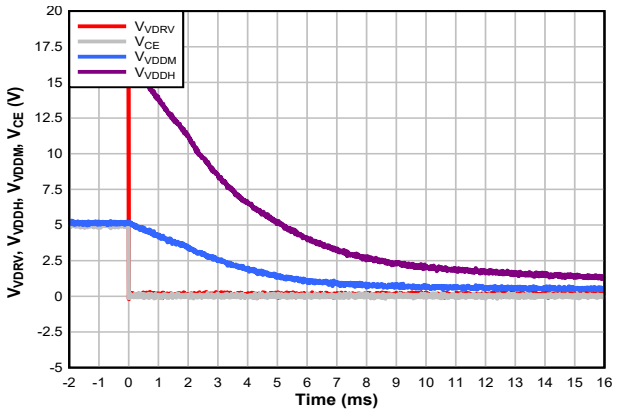
図 6-7. $t_{LH\_VDRV\_CE}$



VDDP = 5.0V T_A = 25°C R_{RESP} = 100kΩ
C_{DIV1} = 47nF C_{DIV2} = 220nF C_{VDRV} = 1nF

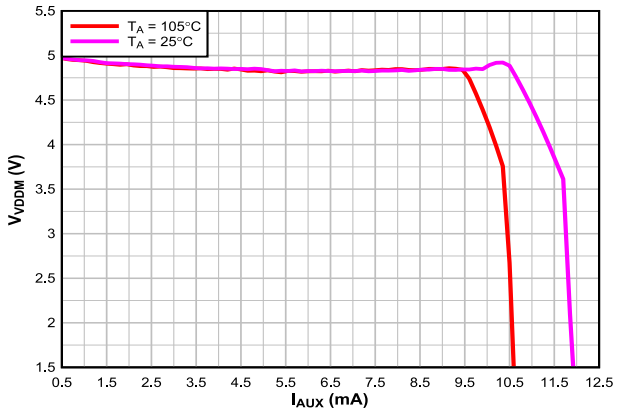
図 6-8. $t_{HL\_VDRV\_CE}$(zoomed in)

6.12 Typical Characteristics (continued)



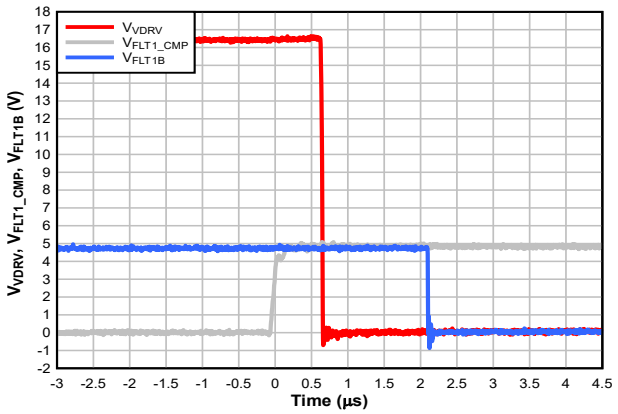
VDDP = 5.0V | T_A = 25°C | R_{RESP} = 100kΩ
C_{DIV1} = 47nF | C_{DIV2} = 220nF | C_{VDRV} = 1nF

図 6-9. $t_{HL\_VDRV\_CE}$(zoomed out)



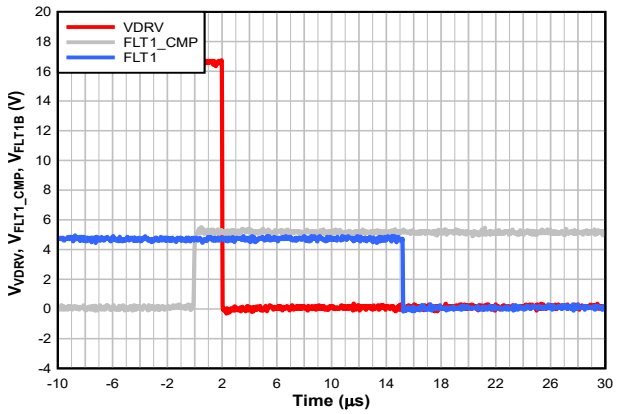
VDDP = 5.0V | C_{DIV1} = 47nF | C_{DIV2} = 220nF

図 6-10. V_{VDDM} versus I_{AUX}



VDDP = 5.0V | T_A = 25°C | R_{RESP} = 100kΩ
C_{DIV1} = 47nF | C_{DIV2} = 220nF | C_{VDRV} = 1nF

図 6-11. $t_{PD\_CMP\_VDRV\_DIS}$, $t_{FLT\_LATENCY}$



VDDP = 5.0V | T_A = 25°C | R_{RESP} = 500kΩ
C_{DIV1} = 47nF | C_{DIV2} = 220nF | C_{VDRV} = 1nF

図 6-12. $t_{PD\_CMP\_VDRV\_DIS}$, $t_{FLT\_LATENCY}$

7 Parameter Measurement Information

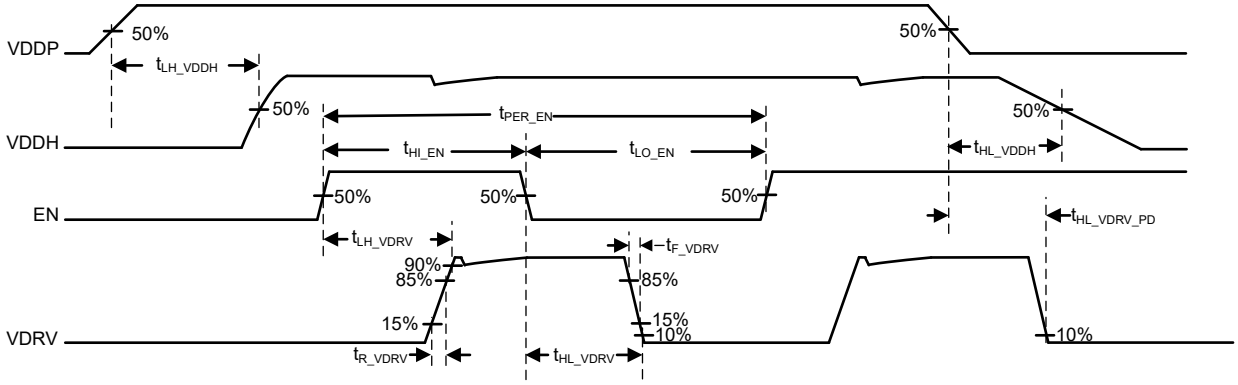


図 7-1. VDRV Timing, (CE = 1 or CE = VDDP, FLTn_CMP = ALMn_CMP = 0)

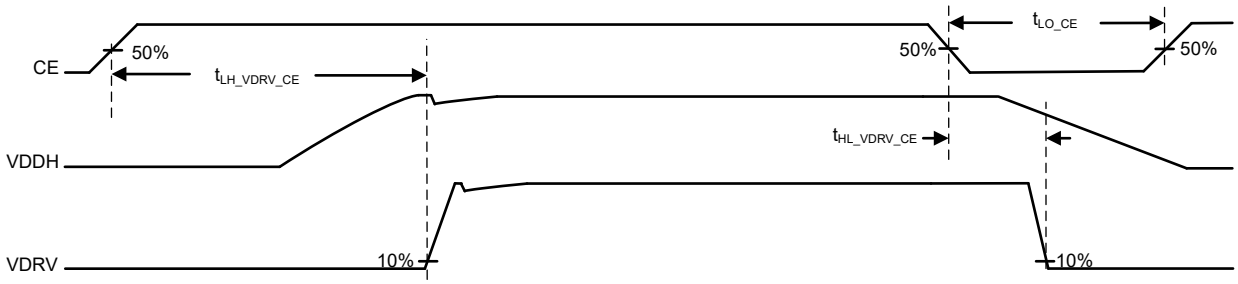


図 7-2. VDRV Timing, (VDDP present, FLTn_CMP = ALMn_CMP = 0)

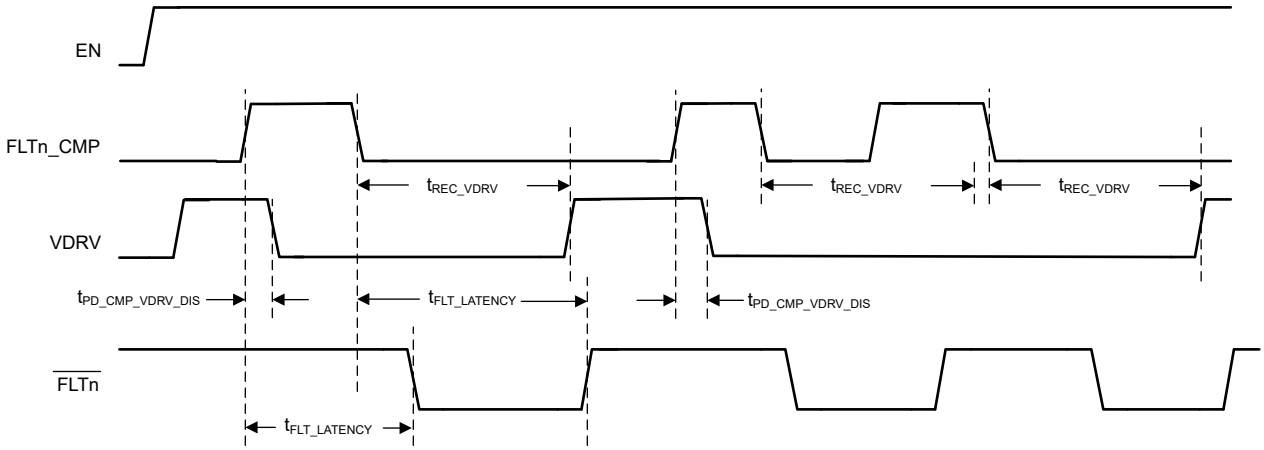


図 7-3. VDRV Auto-Recovery Timing (CE = 1 or CE = VDDP)

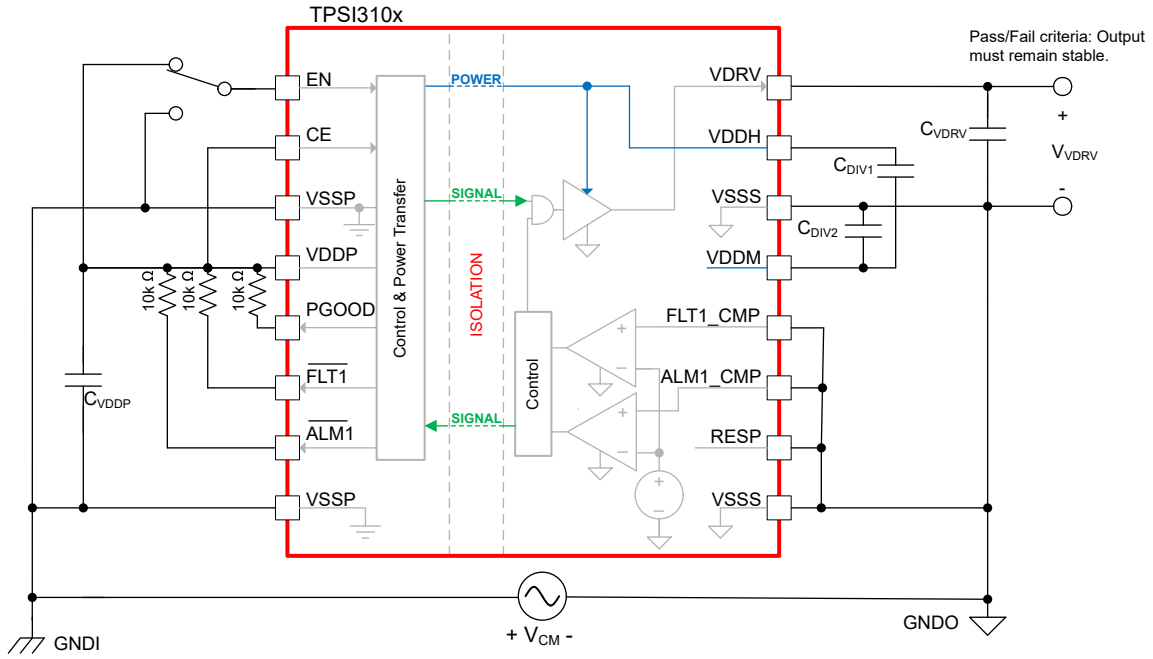


図 7-4. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The TPSI3100-Q1 is a fully integrated isolated switch driver, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a gate drive voltage of 17V with 1.5 and 2.5A peak source and sink current, a large availability of power switches can be used to meet many application needs. The TPSI3100-Q1 generates its own secondary bias supply from power received on its primary side, so no isolated secondary supply bias is required. The TPSI3100-Q1 provides additional power via the nominal 5V rail (VDDM) for use by auxiliary circuits to perform various function such as current and voltage monitoring or remote temperature detection. The TPSI3100-Q1 isolation is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The TPSI3100-Q1 integrates a communication back-channel that transfers status information from the secondary side to the primary side via open-drain outputs, PGOOD (Power Good), $\overline{\text{FLT1}}$ (Fault 1), and $\overline{\text{ALM1}}$ (Alarm 1). Dual high-speed comparators with an integrated shared voltage reference are used to assert $\overline{\text{FLT1}}$ and $\overline{\text{ALM1}}$. When the comparator input, FLT1_CMP, exceeds the voltage reference, the driver is immediately asserted low and $\overline{\text{FLT1}}$ is also driven low, indicating to the system that a fault has occurred. This is useful for disabling the external switch with low latency on critical events, such as overcurrent detection. When the comparator input, ALM1_CMP, exceeds the voltage reference, $\overline{\text{ALM1}}$ signal is asserted low, but no action is taken by the driver. This may be useful as an alarm or warning indicator for overtemperature or overvoltage events.

The TPSI310xL-Q1 series offers a latch based fault indicator. When a fault is detected, the driver and the fault indicator are asserted low and remain latched, until EN is asserted low. The TPSI310x-Q1 series has a non-latched fault indicator. If the fault event is no longer present, $\overline{\text{FLT1}}$ deasserts and the driver, after a specified recovery period, follows the state of the EN pin. If the fault event still remains, both the fault indicator and the driver remain asserted low.

The TPSI310x-Q1 and TPSI310xL-Q1 device family has two voltage options for the integrated reference to meet a wide range of application needs.

The Functional Block Diagram shows the primary side includes a transmitter that drives an alternating current into the primary winding of an integrated transformer which transfers power from the primary side to the secondary side. The transmitter operates at high frequency (80MHz, nominal) to optimally drive the transformer to its peak efficiency. In addition, the transmitter utilizes spread spectrum techniques to greatly improve EMI performance allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information is transferred to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer, is rectified and multiplied, and is regulated to the voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low, respective of the logic state of the EN pin.

During each transfer of power from the primary side to the secondary side, back-channel state information is automatically sampled, encoded, and sent from the secondary side back to the primary side where it is decoded.

8.2 Functional Block Diagram

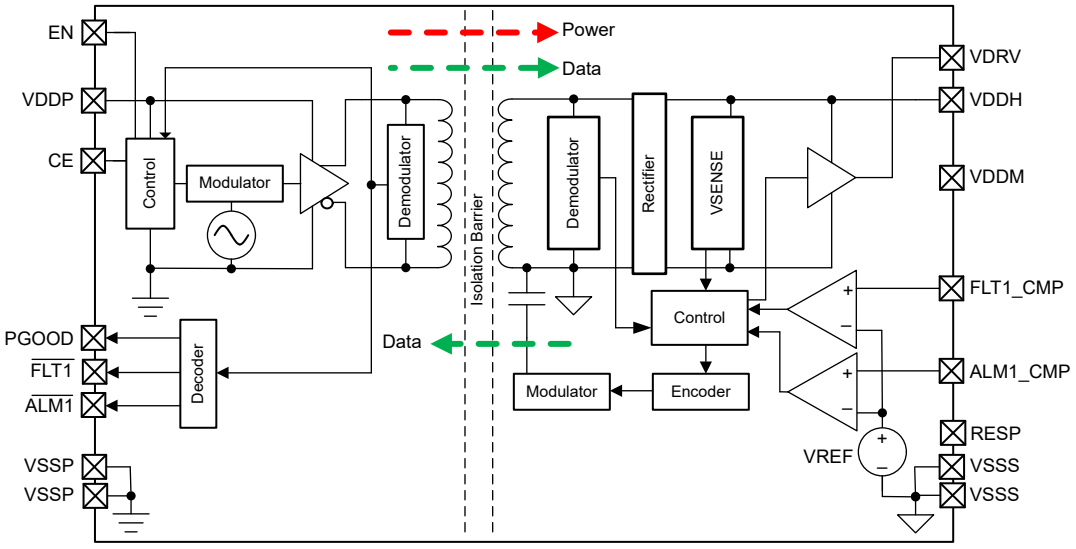


図 8-1. TPSI310x-Q1, TPSI310xL-Q1

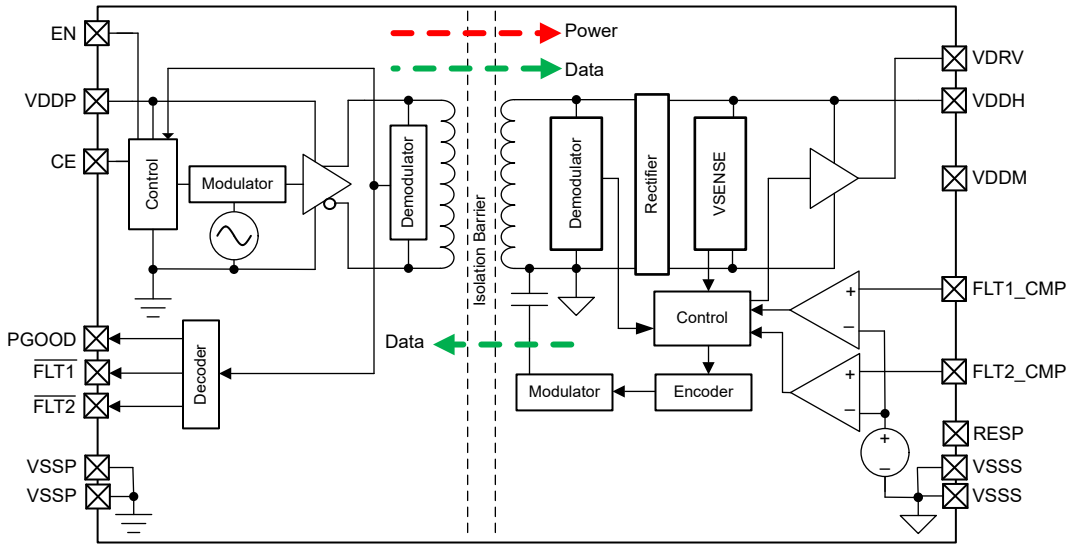


図 8-2. TPSI311x-Q1, TPSI311xL-Q1

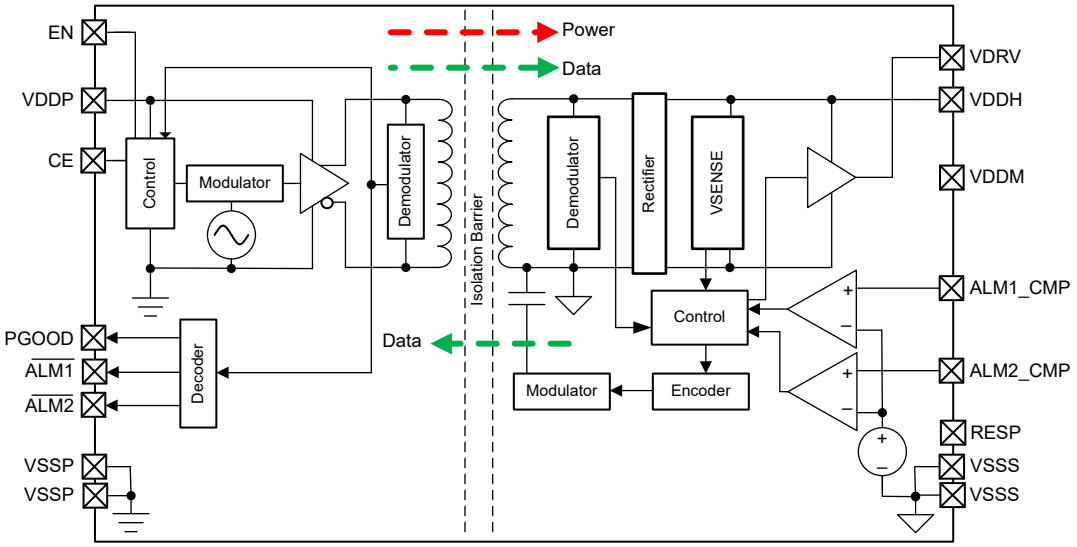


図 8-3. TPSI312x-Q1

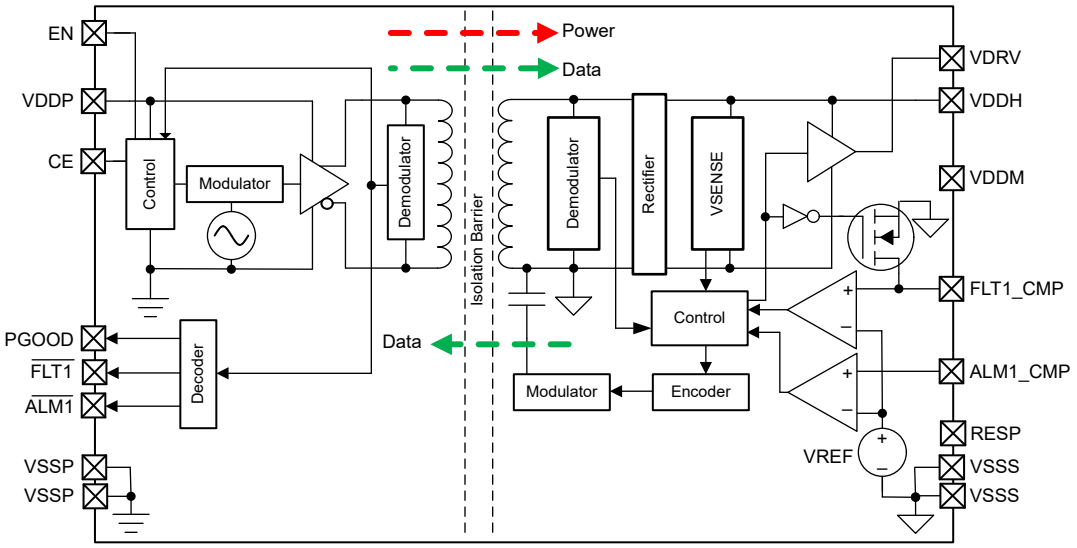


図 8-4. TPSI3133-Q1

8.3 Feature Description

8.3.1 Transmission of the Enable State

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ uses a modulation scheme to transmit the switch enable (EN) state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier, and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low based on the state information received.

8.3.2 Power Transmission

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ does not utilize a secondary side isolated bias supply for its power. The secondary side power is obtained by the transferring of the primary side input power from VDDP across the isolation transformer. The modulation scheme uses spread spectrum techniques to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

8.3.3 Gate Driver

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ has an integrated gate driver that provides a nominal 17V with 1.5 and 2.5A peak source and sink current sufficient for driving many power transistors. When driving external power transistors, TI recommends bypass capacitors ($C_{DIV2} \geq 3 * C_{DIV1}$) from VDDH to VDDM and VDDM to VSSS with an equivalent series capacitance of minimum of 30 times the equivalent gate capacitance. If optional auxiliary circuitry requires power, additional capacitance may be required.

8.3.4 Chip Enable (CE)

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ has an active high chip enable, CE. When CE is asserted high and VDDP is present, the device enters its active mode of operation and power transfer occurs from the primary side to the secondary side. When CE is asserted low while VDDP is present, the device enters standby and no power transfer occurs from primary side to the secondary side and VDRV will be asserted low. Over time, VDDH and VDDM fully discharge depending on the amount of loading present on these rails.

8.3.5 Comparators

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ devices include two identical isolated comparators. A simplified block diagram is shown in 図 8-5. The function of the comparator, fault or alarm, depends on the device orderable in the family. The positive inputs (FLTn_CMP or ALMn_CMP) of each comparator monitor the voltage on these inputs referenced to VSSS. Both comparators share a single integrated voltage reference, VREF, with an accuracy of ±1.5% over voltage and temperature and is connected internally to the negative inputs of each comparator. The reference voltage is internal to the device and not available externally. The reference voltage level depends on the device orderable in the family.

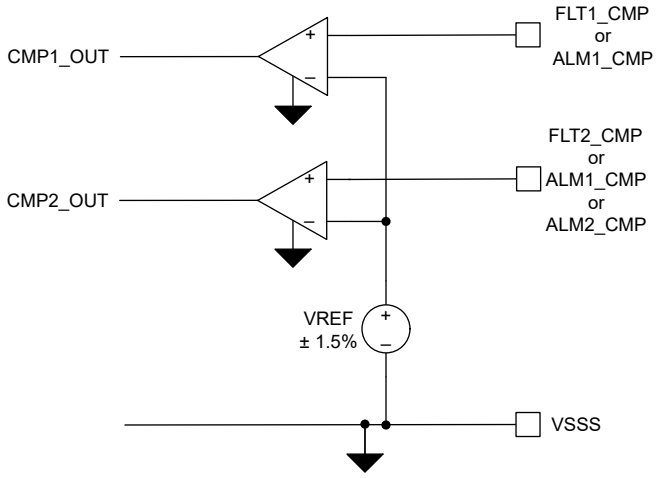


図 8-5. Comparator Block Diagram

8.3.5.1 Fault Comparator

The TPSI310x-Q1 and TPSI3133-Q1 devices include one fault comparator that is used to quickly assert the output driver, VDRV, low to allow for the fastest disable time of the external power switch. This is useful for critical events such as overcurrent protection (OCP) to protect the external power switch and downstream circuitry. The block diagram of the fault comparator is shown in 図 8-6. The TPSI311x-Q1 devices have two fault comparators. This can be useful for applications such as bi-directional OCP or whenever there are two independent critical events required to protect the external power switch. The TPSI312x-Q1 device does not support any fault comparators, only alarm comparators.

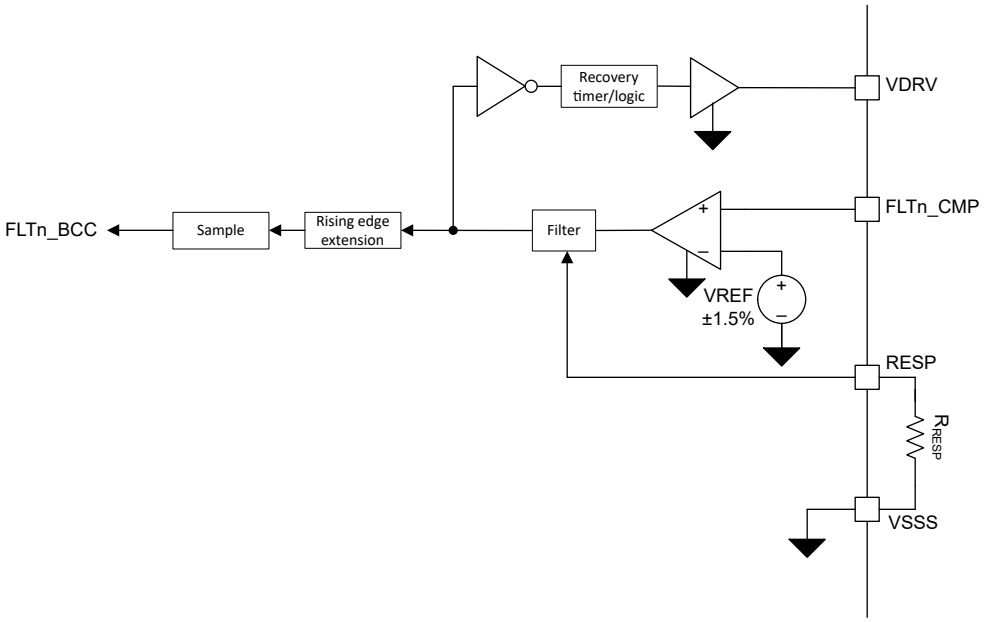


図 8-6. Fault Comparator Block Diagram

If the input voltage of the fault comparator, FLTn_CMP, exceeds the internal reference voltage, VREF, the comparator output asserts high. The comparator output is filtered and is adjustable via an external 1% resistor, R_{RESP}, connected from RESP to VSSS. The filtering of low-to-high transitions of the comparator output is adjustable by R_{RESP}. High-to-low transitions of the comparator output are filtered at a fixed setting. Filtering the comparator output allows for flexibility and application tradeoffs to help minimize false trigger events while still providing adequate protection. The filtered comparator output is then fed into the driver logic. If the comparator output low-to-high event passes through the filter, VDRV is immediately asserted low regardless of the state of EN. The TPSI310x-Q1, TPSI311x-Q1, and TPSI3133-Q1 fault comparators are not latched. Upon a fault condition, VDRV has a recovery timer that keeps VDRV low for a minimum time, t_{REC_VDRV}. If a fault condition is removed (FLTn_CMP voltage falls below the internal reference voltage and passes through the filter), VDRV is held low until the recovery timer has elapsed. Once the recovery timer has elapsed, VDRV follows the state of EN. If a fault condition occurs before the recovery timer has elapsed, the recovery timer is restarted.

The comparator output information is transferred to the primary side of the device via back-channel communication (BCC) over the isolation barrier. As shown in 図 8-6, any low-to-high transition of the comparator output (fault event) that passes through the filter is extended to make sure the event is captured by the sample logic. Any high-to-low transition of the comparator output (recovery event) that passes through the filter are not extended. A recovery event can be missed by the sample logic if the event does not last longer than the sample period. Therefore, priority is given to fault events over recovery events. $\overline{\text{FLTn}}$ open-drain output is asserted low upon the fault event. If a recovery event occurs and is captured by the sample logic, $\overline{\text{FLTn}}$ open-drain output is set to high-impedance, but VDRV remains asserted low until the recovery timer elapses.

The TPSI310xL-Q1 and TPSI311xL-Q1 devices have latched fault comparators as shown in 図 8-7. Fault events are latched and held until EN is asserted low. Upon a fault event, VDRV asserts low and is held until EN is asserted low and the recovery timer elapses. $\overline{\text{FLTn}}$ is also asserted low and held until EN is asserted low. If the fault event has recovered, $\overline{\text{FLTn}}$ is asserted high even if the recovery timer has not elapsed.

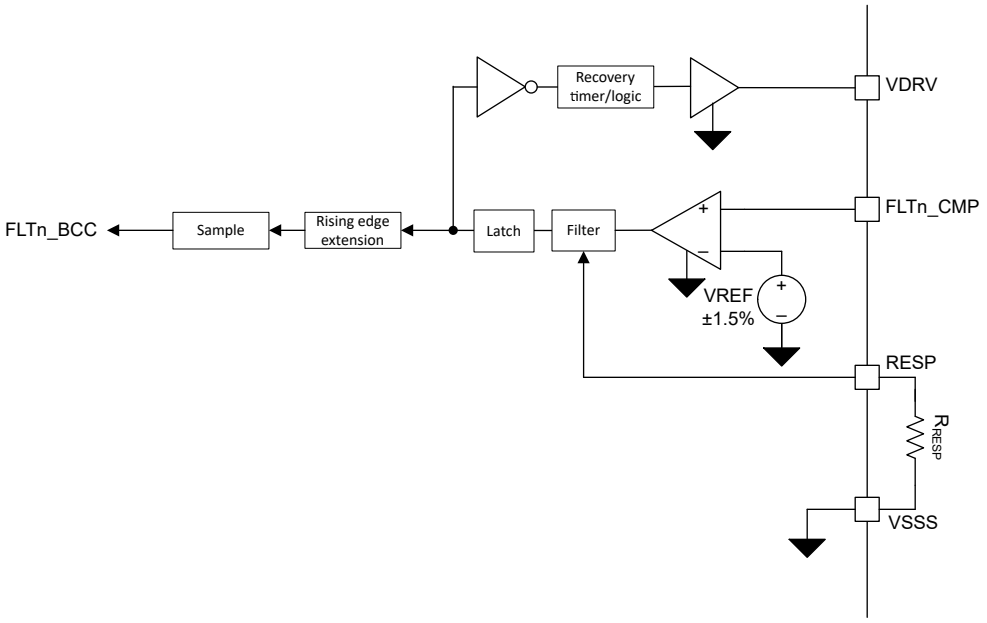


図 8-7. Latched Fault Comparator Block Diagram

8.3.5.2 Alarm Comparator

The TPSI310x-Q1 and TPSI3133-Q1 devices include one alarm comparator. The TPSI312x-Q1 devices include two alarm comparators. An alarm comparator differs from the fault comparator in that the output state of the comparator has no direct control of the VDRV output driver. The block diagram of the alarm comparator is shown in 図 8-8.

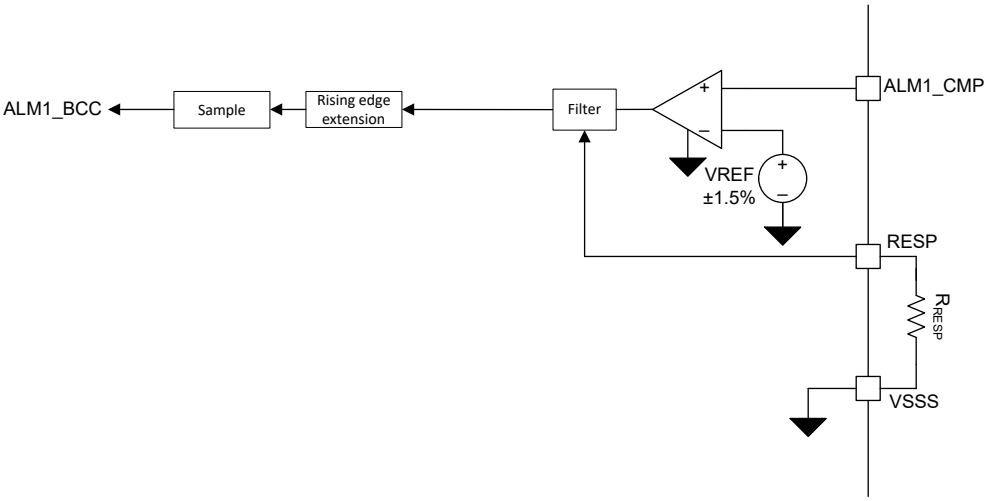


図 8-8. Alarm Comparator Block Diagram

If the input voltage of the alarm comparator, ALM1_CMP, exceeds the internal reference voltage, VREF, the comparator output asserts high. The comparator output is filtered and is adjustable via an external 1% resistor, R_{RESP}, connected from RESP to VSSS. The filtering of low-to-high transitions of the comparator output is adjustable by R_{RESP}. High-to-low transitions of the comparator output are filtered at a fixed setting. The filter setting is shared by both the fault and alarm comparators and cannot be set independently. In addition, the alarm comparator is not latched.

Similar to the fault comparator, the alarm comparator output information is transferred to the primary side of the device via back-channel communication (BCC) over the isolation barrier. As shown in 図 8-8, any low-to-high transition of the comparator output (alarm event) that passes through the filter is extended to make sure the event is captured by the sample logic. Any high-to-low transition of the comparator output (recovery event) that passes through the filter are not extended. A recovery event can be missed by the sample logic if the event does not last longer than the sample period. Therefore, priority is given to alarm events over recovery events. $\overline{\text{ALM1}}$ open-drain output is asserted low upon the alarm event. If a recovery event occurs and is captured by the sample logic, $\overline{\text{ALM1}}$ open-drain output is set to high-impedance.

8.3.5.3 Comparator De-glitch

For many applications, there is a tradeoff between detecting critical events and the false triggering of a non-critical events. The RESP pin allows for adjustment of the response time of the comparator based on the application needs. Selection of a 1% resistor from the RESP pin to VSSS allows for filtering of the comparator response. The amount of typical de-glitch, $t_{DEGLITCH\_CMP\_R}$, on the comparator output high assertion is estimated using 式 1, where $t_{DEGLITCH\_CMP\_R}$ units is nanoseconds and R_{RESP} units is kilo-ohm.

$$t_{DEGLITCH\_CMP\_R\,(ns)} = max\left[\left(3.55 \times R_{RESP\,(k\Omega)} + 153\right),\ 235\right] \quad (1)$$

If the comparator output high assertion exceeds the duration of $t_{DEGLITCH\_R}$, the comparator output is propagated. Comparator output low assertions are filtered at a fixed setting, $t_{DEGLITCH\_CMP\_F}$.

8.3.6 VDDP, VDDH, and VDDM Undervoltage Lockout (UVLO)

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ implements an internal UVLO protection feature for both input (VDDP) and output power supplies (VDDM and VDDH). The device remains disabled until VDDP exceeds its rising UVLO threshold. When the VDDP supply voltage falls below its falling threshold voltage, the device attempts to send data information to quickly assert VDRV low, regardless of the state of EN. This depends on the rate of VDDP loss. If VDDP collapses too fast to send the information, a timeout mechanism ensures VDRV is asserted low within $t_{HL\_VDRV\_PD}$. A VDDP ULVO event causes PGOOD, $\overline{\text{FLT1}}$, and $\overline{\text{ALM1}}$ to assert low.

VDDH and VDDM UVLO circuits monitor the voltage on VDDH and VDDM, respectively. VDRV is only asserted high if both the VDDH and VDDM UVLO rising thresholds are surpassed. If either VDDH or VDDM fall below their respective UVLO falling thresholds, VDRV is immediately asserted low. The UVLO protection blocks feature hysteresis, which helps to improve immunity of VDRV to noise present on the VDDM and VDDH rails. During turn on and turn off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH and VDDM power supplies. The UVLO protection circuits ignores the associated noise during these normal switching transients.

8.3.7 Keep-Off Circuitry

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ contains keep-off circuitry on the output driver. The purpose of the keep-off circuitry is to clamp the gate voltage below an acceptable level to prevent the external power switch from turning on when no power is present on the secondary rails. The keep-off circuitry can be used to replace or greatly reduce the requirements of an external bleed-off resistor on the external power switch.

図 8-9 shows a simplified schematic of the keep-off circuitry. Transistors MP1 and MN1 form the driver that provides the gate current to drive the external power switch (M1). When no power is available on the secondary, the 1MΩ resistor, is connected from the drain to gate of MN1, forming an NMOS diode configuration. Any external coupling into the VDRV signal, via the M1 parasitic gate-to-drain and gate-to-source capacitances, can cause the VDRV signal to rise. The diode configuration of MN1 sinks this current to keep VDRV from rising too high, clamping VDRV to V_{ACT_CLAMP} . This is sufficient to keep most power switches off. If desired, an additional resistance can also be placed (on the order of 250kΩ or higher) across the gate-to-source of M1. Note that any resistance applied requires power from the secondary supply in normal operation and must be accounted for in the overall power budget.

In addition to the MN1 diode clamp, the body diode of MP1 can also help absorb any coupling into VDRV. The equivalent capacitance, C_{eq}, which is the series combination of C_{DIV1} and C_{DIV2} is typically on the order of hundreds of nanofarads for most applications. If power transfer has ceased for some time, this capacitance is fully discharged to VSSS and clamps VDRV a diode above VSSS via the body diode of MP1 connected to VDDH. Any external coupling into the VDRV signal, via the M1 parasitic gate-to-drain and gate-to-source capacitances, is absorbed by C_{eq}, minimizing the voltage rise on VDRV.

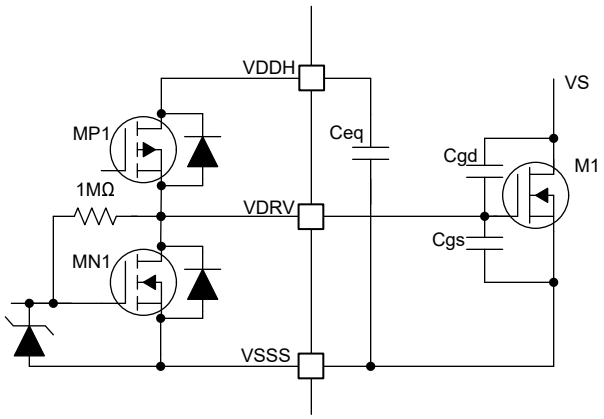


図 8-9. Keep-Off Circuitry

8.3.8 Thermal Shutdown

The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ has an integrated temperature sensor. The sensor monitors its local temperature. When the sensor reaches its threshold, it automatically disables power transfer from the primary side to the secondary side, and sends data information to disable the driver, VDRV. The power transfer is disabled and VDRV is asserted low until the local temperature reduces enough to re-engage.

8.4 Device Operation

VDDP must be supplied independently by a low impedance external supply that can deliver the required power. When VDDP power is present and CE is a logic high, power transfers from the primary side to the secondary side. Setting the EN pin logic high or low asserts or deasserts VDRV, thereby enabling or disabling the external switch, respectively. 図 8-10 shows the basic set-up required for proper operation which requires EN, VDDP, and VSSP signals. EN may be driven up to 5.5V which is normally driven from circuitry on the same rail as VDDP. In this example, the TPSI310x-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. Driving back-to-back MOSFETs is required for AC switching applications or DC switching where reverse blocking is required. C_{VDDP} provides the required decoupling capacitance for the VDDP supply. C_{DIV1} and C_{DIV2} provide the required decoupling capacitance of the VDDH/VDDM supply rails to provide peak current to drive the external MOSFETs.

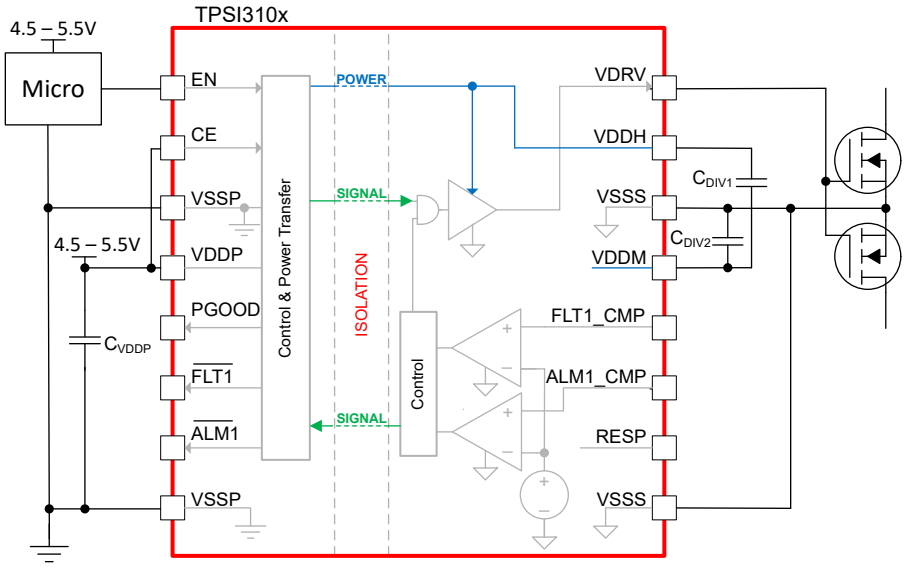


図 8-10. Simplified Schematic

図 8-11 shows the basic operation from start up to steady state conditions.

- At T1: VDDP powers up the device. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are asserted low.
- At T2 and T3: TPSI310x-Q1 begins to transfer power from VDDP to the secondary side for a fixed burst period (25µs typical), which begins to charge up the VDDH and VDDM secondary side rails. Power transfer continues as long as VDDP is present (and CE remains high). The time required to fully charge VDDH depends on several factors including the values of VDDP, C_{DIV1}, C_{DIV2}, the amount of auxiliary load drawn from VDDM, and the overall power transfer efficiency.
- At T4, T5, and T6: After four burst periods, the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are released and begin to reflect their respective status. PGOOD asserts high if VDDM and VDDH are both above their UVLO thresholds, otherwise remains asserted low. $\overline{\text{FLTn}}$ and $\overline{\text{ALMn}}$ indicate the status of their comparator outputs. In this example, since FLTn_CMP and ALMn_CMP are tied to VSSS, $\overline{\text{FLTn}}$ and $\overline{\text{ALMn}}$ assert high. The status indicators are always transferred sequentially in the order of $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD with a delay of approximately 400ns between each indicator.
- At T7 and T8: EN is asserted high and VDRV asserts high. Note that VDRV will not assert high until VDDH and VDDM are both above their UVLO thresholds. Due to latency of the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD indicators, it is possible that VDRV asserts high prior to PGOOD asserting high.

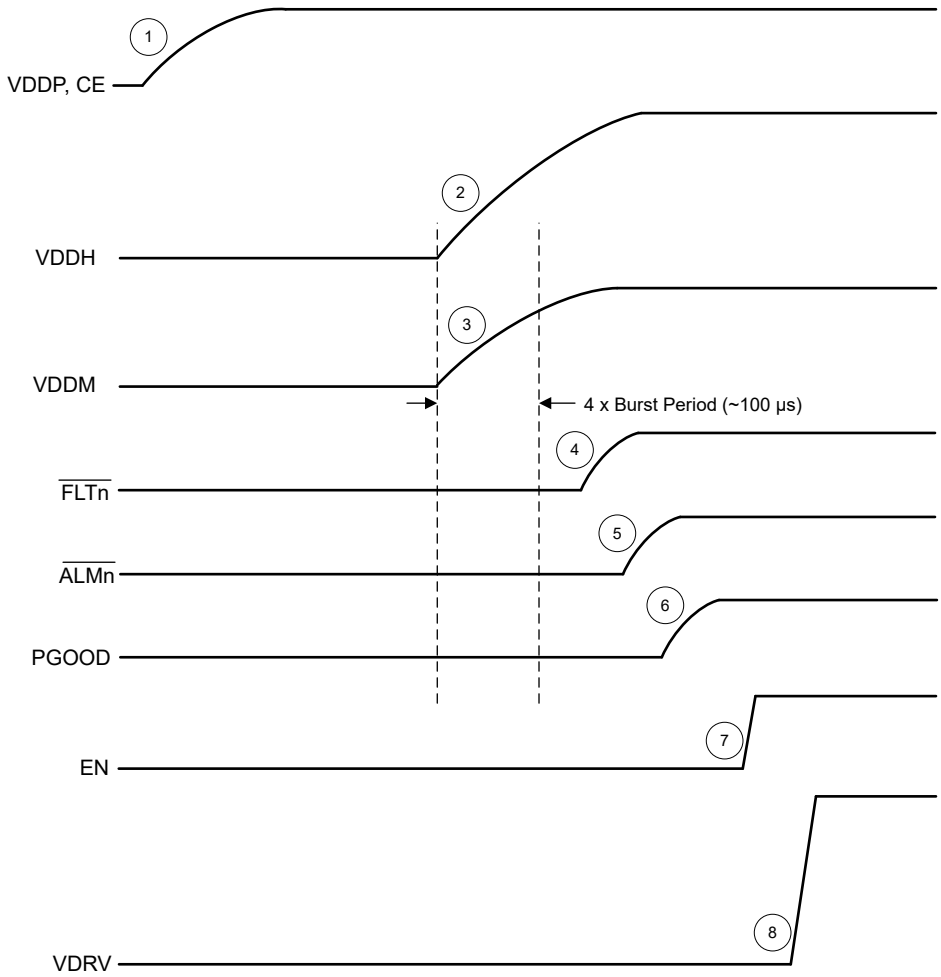


図 8-11. TPSI310x-Q1 Typical Start-up (CE = VDDP, FLTn_CMP = 0, ALMn_CMP = 0)

図 8-12 shows start up sequence where VDDP, CE, and EN signals are tied together.

- At T1: VDDP powers up the device. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are asserted low.
- At T2 and T3: TPSI310x-Q1 begins to transfer power from VDDP to the secondary side for a fixed burst period (25µs typical), which begins to charge up the VDDH and VDDM secondary side rails.
- At T4: VDRV asserts high when both VDDH and VDDM are above their UVLO thresholds.
- At T5, T6, and T7: After four burst periods, the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are released and begin to reflect their respective status. In this specific example, it is assumed that VDDH and VDDM rails have charged up beyond their UVLO thresholds under the four burst periods (100µs). In this case, due to the PGOOD latency, PGOOD is asserted high after VDRV is asserted high.

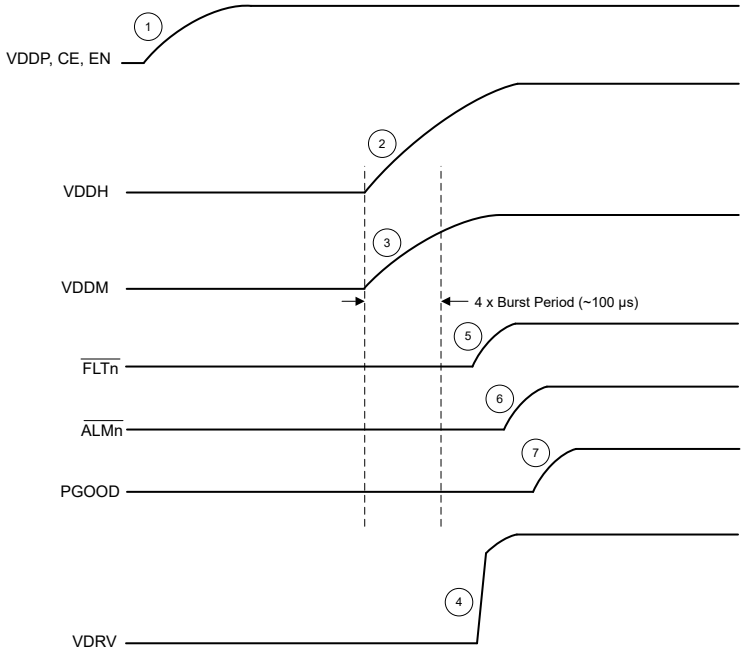


図 8-12. TPSI310x-Q1 Typical Start-up (CE = EN = VDDP, FLTn_CMP = 0, ALMn_CMP = 0)

To reduce average power, the TPSI310x-Q1 transfers power from the primary side to the secondary side in a burst fashion. The period of the burst is fixed while the burst on time is determined internally by the control loop regulating the VDDM voltage. The burst on time is automatically adjusted thereby optimizing power transfer for a given load condition. During power up, the device operates at the highest power setting which helps to quickly charge up the VDDM and VDDH rails.

8.5 Device Functional Modes

表 8-1 summarizes the functional modes for the TPSI310x-Q1 and TPSI310xL-Q1.

表 8-1. TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ, Functional Modes (1) (2)

CE	VDDP	VDDH, VDDM	EN	VDRV	PGOOD	COMMENTS
X	Powered Down(4)	Powered Down(6)	X	L	Hi-Z	Powered Down: VDRV output disabled, keep off circuitry applied.
L	Powered Up(3)	Powered Down(6)	X	L	L	Disabled Operation: When CE is asserted low, power transfer to the secondary ceases. VDDH and VDDM rails discharge pending loading. VDRV output disabled, keep off circuitry applied.
H	Powered Up(3)	Powered Up(5)	L	L	H	Normal Operation: VDRV output state follows logic state of EN logic state.
			H	H	H	
X	Powered Down(4)	Powered Up(5)	X	L	L	Disabled Operation: When VDDP is powered down, output driver is disabled automatically. If sufficient VDDP power is available, VDRV is disabled within the propagation delay, otherwise after the timeout duration. Keep off circuitry applied.

(1) No alarm or fault conditions present (FLTn_CMP = ALMn_CMP = 0).
(2) X: do-not-care.
(3) V_{VDDP} ≥ VDDP_UVLO threshold.
(4) V_{VDDP} < VDDP_UVLO threshold.
(5) V_{VDDH} ≥ VDDH_UVLO threshold and V_{VDDM} ≥ VDDM_UVLO threshold.
(6) V_{VDDH} <VDDH_UVLO threshold or V_{VDDM} < VDDM_UVLO threshold.

表 8-2 summarizes fault and comparator functional behavior.

表 8-2. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$ Functional Behavior (1)

CE(2)	FLTn_CMP(3)	ALMn_CMP(4)	$\overline{\text{FLTn}}$ (5)	$\overline{\text{ALMn}}$ (5)	COMMENTS
L	X	X	L	L	VDRV output disabled, keep off circuitry applied.
H	L	L	Hi-Z	Hi-Z	VDRV output follows state of EN pin.
H	L	H	Hi-Z	L	Fault detected. VDRV output asserted low until recovery timer elapses. On latched fault devices, VDRV asserts low and remains low until EN asserts low then high and recovery timer elapses.
H	H	L	L	Hi-Z	Alarm detected. VDRV output unchanged.
H	H	H	L	L	Fault and alarm detected. VDRV output asserted low until recovery timer elapses. On latched fault devices, VDRV asserts low and remains low until EN asserts low then high and recovery timer elapses.

(1) Assumes V_{VDDP} ≥ VDDP_UVLO threshold and device is fully powered in steady state conditions.
(2) L: $V_{CE} < V_{IT\_-(CE)}$, H: $V_{CE} \geq V_{IT\_+(CE)}$.
(3) L: $V_{FLTn\_CMP} < V_{REF}$, H: $V_{FLTn\_CMP} \geq V_{REF}$.
(4) L: $V_{ALMn\_CMP} < V_{REF}$, H: $V_{ALMn\_CMP} \geq V_{REF}$.
(5) Hi-Z: Open-drain output disabled, L: Open-drain output enabled.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPSI310x-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a nominal gate drive voltage of 17V with 1.5A and 3.0A peak source and sink current, a large variety of external power switches such as MOSFETs, IGBTs, or SCRs can be chosen to meet a wide range of applications. The TPSI310x-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The secondary side provides a regulated, floating supply rail of 17V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI310x-Q1 can support driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI310x-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The TPSI310x-Q1 integrates a communication back-channel that transfers various status information from the secondary side to the primary side via open-drain outputs, PGOOD (Power Good), $\overline{\text{FLT1}}$ (Fault 1), and $\overline{\text{ALM1}}$ (Alarm 1). Two high-speed comparators with an integrated shared voltage reference are used to assert $\overline{\text{FLT1}}$ and $\overline{\text{ALM1}}$. When the comparator input, FLT1_CMP, exceeds the voltage reference, the driver is immediately asserted low and $\overline{\text{FLT1}}$ on the primary side is driven low after some latency, indicating a fault has occurred. This is useful for directly disabling the external switch from the secondary on critical events with low latency, such as short circuit detection. When the comparator input, ALM1_CMP, exceeds the voltage reference, $\overline{\text{ALM1}}$ signal is asserted low on the primary side, but no action is taken by the driver. This may be useful as an alarm or warning indicator.

The various devices offered in the family can be used in a broad range of applications, with just some examples shown here. 図 9-1 shows a simplified schematic of a shunt based overcurrent protection for DC applications. As the voltage increases across R_{SHUNT}, an alarm event is triggered upon crossing the VREF threshold of the alarm comparator and $\overline{\text{ALM1}}$ asserts low notifying the system of the event. As the voltage increases further, a fault event is triggered upon crossing the VREF threshold of the fault comparator, which immediately asserts VDRV low to protect the FET and the downstream load. $\overline{\text{FLT1}}$ asserts low notifying the system of the event.

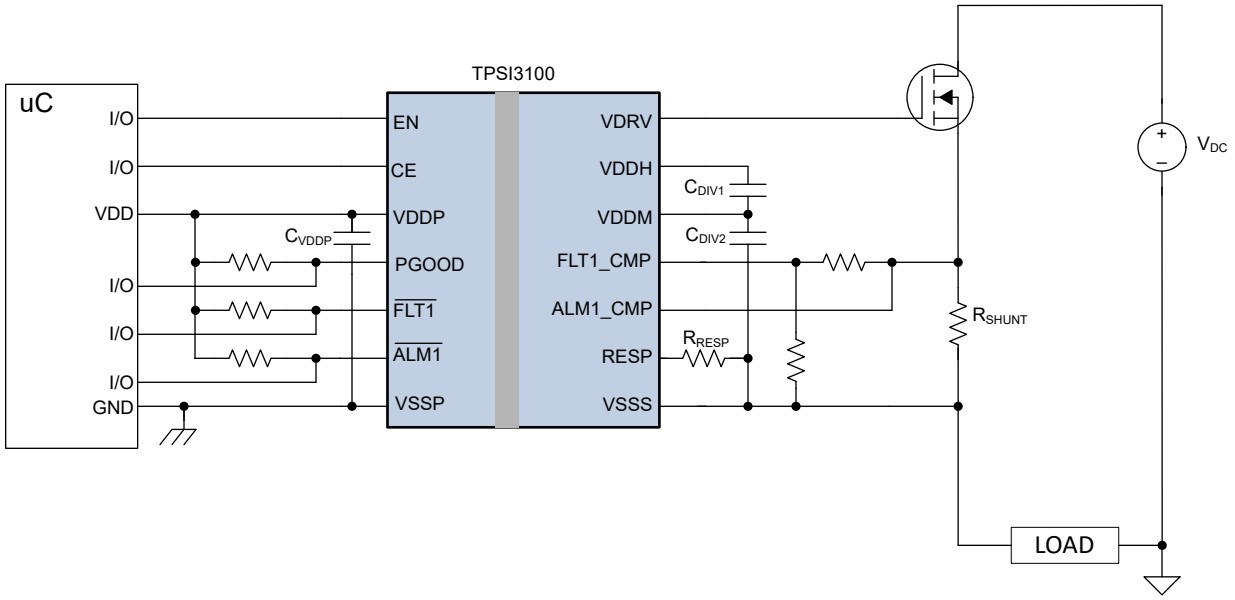


図 9-1. TPSI3100-Q1 overcurrent protection with fault and alarm indicators

図 9-2 shows a simplified schematic of a shunt based overcurrent protection using a current sense amplifier for DC applications. The current sense amplifier, with its low input offset, allows for using smaller value R_{SHUNT} values for lower power losses for larger current ranges. As the voltage increases across R_{SHUNT}, after being amplified by the current sense amplifier, an alarm event is triggered upon crossing the VREF threshold of the alarm comparator and $\overline{ALM1}$ asserts low notifying the system of the event. As the voltage increases further, a fault event is triggered upon crossing the VREF threshold of the fault comparator, which immediately asserts VDRV low to protect the FET and the downstream load. $\overline{FLT1}$ asserts low notifying the system of the event.

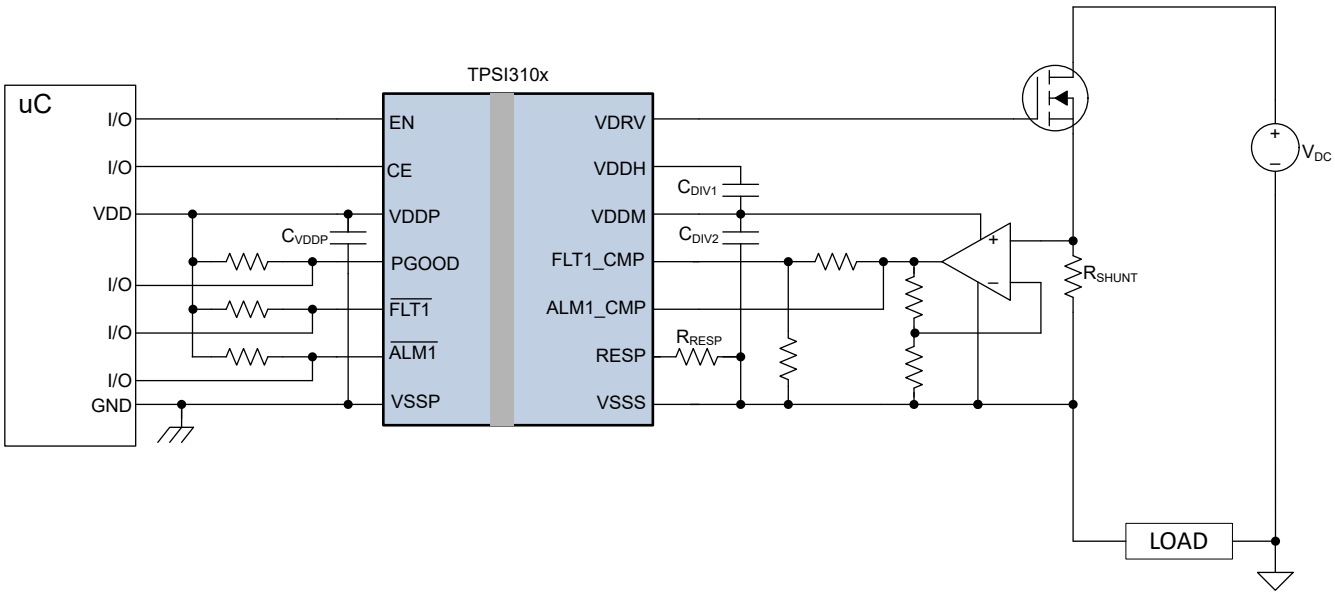


図 9-2. TPSI310x-Q1 overcurrent protection with current sense amplifier, fault and alarm indicators

図 9-3 shows a simplified schematic of a shunt based overcurrent protection for AC applications. As the positive AC voltage increases across R_{SHUNT1}, a fault event is triggered upon crossing the VREF threshold of the first fault comparator, which immediately asserts VDRV low to protect the back-to-back FETs and the downstream load. $\overline{FLT1}$ asserts low notifying the system of the event. Similarly, as the negative AC voltage increases across

R_{SHUNT2}, a fault event is triggered upon crossing the VREF threshold of the second fault comparator, which immediately asserts VDRV low. $\overline{FLT2}$ asserts low notifying the system of the event.

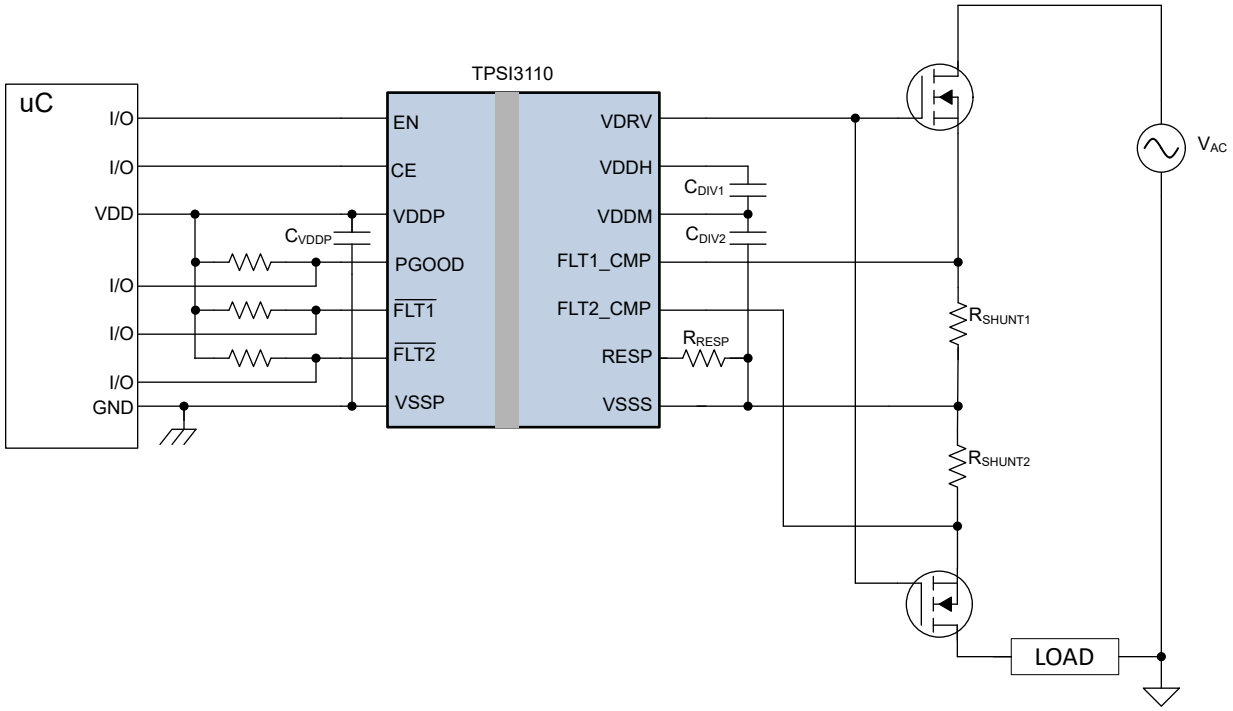


図 9-3. TPSI3110-Q1 Bi-directional overcurrent protection with fault indicators

図 9-4 shows a simplified schematic of a shunt based overcurrent protection using dual current sense amplifiers for AC applications. In this topology, a single shunt resistor is used. The top current sense amplifier connects its IN+ and IN- pins across R_{SHUNT}, where the second current sense amplifier reverses its input connections. As the positive AC voltage increases across R_{SHUNT}, after being amplified by the top current sense amplifier, a fault event is triggered upon crossing the VREF threshold of the first fault comparator, which immediately asserts VDRV low to protect the back-to-back FETs and the downstream load. $\overline{FLT1}$ asserts low notifying the system of the event. Similarly, as the negative AC voltage increases across R_{SHUNT}, a fault event is triggered upon crossing the VREF threshold of the second fault comparator, which immediately asserts VDRV low. $\overline{FLT2}$ asserts low notifying the system of the event.

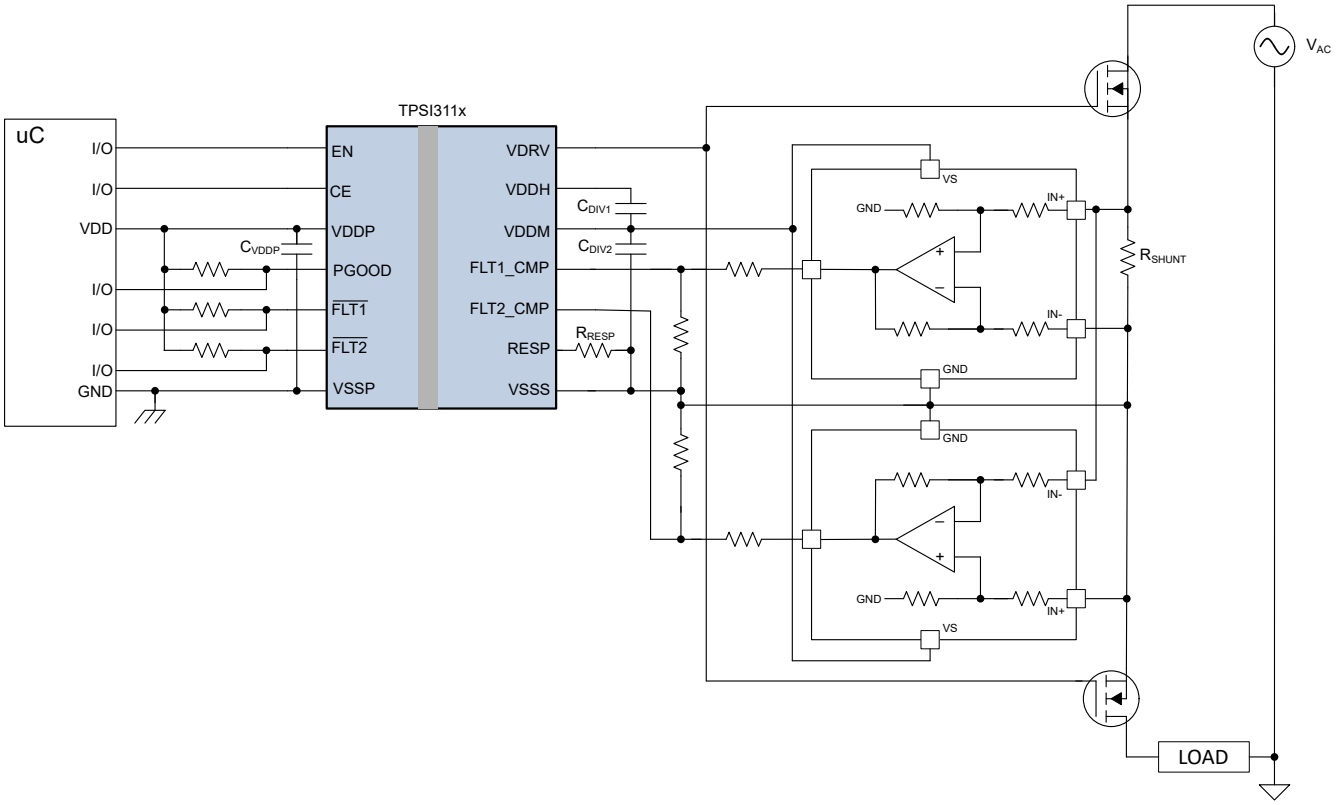


図 9-4. TPSI311x-Q1 Bi-directional overcurrent protection with current sense amplifiers, fault indicators

図 9-5 shows a simplified schematic of overcurrent protection using DESAT protection for DC applications. This method is commonly used with IGBT power transistors. When the IGBT is off, FLT1_CMP is driven low internally by the TPSI3133-Q1. When the driver is being enabled, the voltage on FLT1_CMP begins to rise. As the IGBT turns on, under normal load conditions, its V_{CE} drops quickly which causes the voltage on FLT1_CMP to remain below the fault comparator threshold. The time for when FLT1_CMP is released and V_{CE} has dropped enough to keep a false fault event from being detected, is known as the blanking time. Adjusting RESP value can help increase the required blanking time or some capacitance may be added to FLT1_CMP. If overcurrent conditions occur, V_{CE} begins to rise until the voltage on FLT1_CMP reaches the VREF threshold of the fault comparator. VDRV is asserted low to protect the IGBT and the downstream load. $\overline{FLT1}$ asserts low notifying the system of the event.

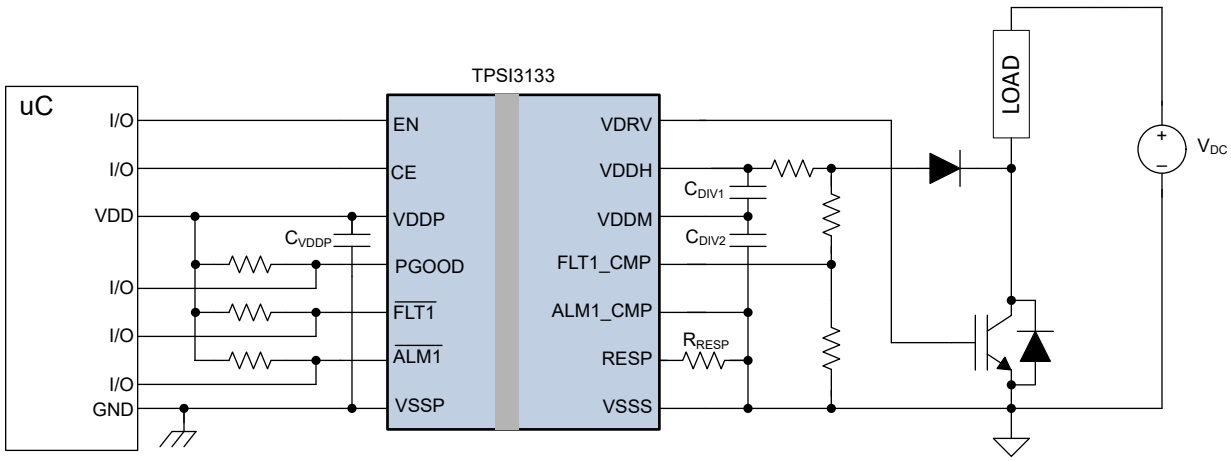


図 9-5. TPSI3133-Q1 DESAT protection with fault indicator

9.2 Typical Application

The simplified circuit diagram shown in 図 9-6 is a typical overcurrent protection application using the TPSI3100-Q1. The circuit uses the alarm comparator to signal a warning to the system via the $\overline{ALM1}$ status indicator. The current is sensed by the voltage formed across the shunt resistor, R_{SHUNT}, during load conditions. $\overline{ALM1}$ asserts low when the alarm threshold is exceeded. The fault comparator is used to detect an overcurrent event and disables the driver at the set overcurrent threshold. The system is notified via the $\overline{FLT1}$ status indicator asserting low.

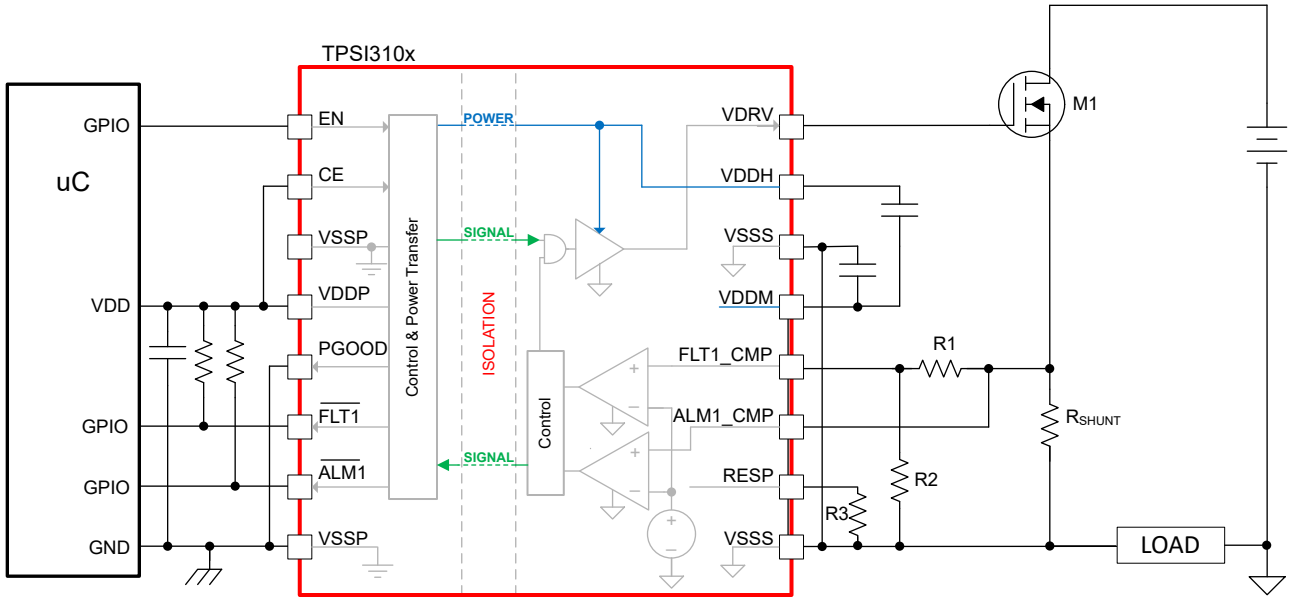


図 9-6. Typical Overcurrent Protection Application

9.2.1 Design Requirements

表 9-1 lists the design requirements of the TPSI310x-Q1 gate driver. The application requires driving external FETs. It includes circuitry for a two-level overcurrent protection that sends an alarm when the load current exceeds its threshold, and a fault when the load current exceeds its overcurrent threshold. Upon a fault, the driver is immediately disabled to protect the external FET and load. The TPSI3100-Q1 used in this example includes a 0.31V voltage reference.

表 9-1. TPSI310x-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	120nC
FET turn-off time upon fault detection	< 0.5µs
Supply voltage (VDDP)	5V ±5%
Overcurrent fault	8A ±10%
Overcurrent alarm	4A ±10%
Shunt resistor tolerance	±1%

9.2.2 Detailed Design Procedure

9.2.2.1 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitors required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the C_{DIV1} and C_{DIV2} capacitors is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of C_{DIV1} and C_{DIV2} be

sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5V drop of the VDDH supply rail that is used to supply power to the VDRV signal. 式 2 and 式 3 can be to used to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (2)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (3)$$

where

- n is a real number greater than or equal to 3.0.
- C_{DIV1} is the external capacitor from VDDH to VDDM.
- C_{DIV2} is the external capacitor from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

注

C_{DIV1} and C_{DIV2} represent absolute capacitor and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitance.

Larger values of ΔV can be used in the application, but excessive droop can cause the VDDH undervoltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitance increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming n = 3 and ΔV = 0.5V, then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120nC}{0.5V} = 320nF \quad (4)$$

$$C_{DIV2} = 3 \times 320nF = 960nF \quad (5)$$

9.2.2.2 Start-up Time and Recovery Time

As described in the *セクション 9.2.2.1* section, the start-up time of the fully discharged VDDH and VDDM rails depends on the amount of capacitance present on the VDDH and VDDM pins, as well as, power being used from VDDM for any auxiliary circuitry. The rate at which this capacitance is charged depends on the amount of power transferred from the primary side to the secondary side. At start up, the power regulation loop transfers more power until the VDDH and VDDM rails reach their steady state values.

9.2.2.3 R_{SHUNT}, R1, and R2 Selection

The TPSI3100-Q1 has an internal nominal voltage reference (V_{REF}) of 0.31V. This reference is shared by the fault and alarm comparator negative inputs.

The alarm event should be detected when the load current, I_{LOAD}, reaches 4A nominal. The required shunt resistor can be computed as:

$$R_{SHUNT} = \frac{V_{REF}}{I_{LOAD}} = \frac{0.31V}{4A} = 77.5m\Omega \quad (6)$$

For this design, R_{SHUNT} = 75mΩ, is used. From this, the nominal alarm current, I_{ALM}, detected can be computed:

$$I_{ALM} = \frac{V_{REF}}{R_{SHUNT}} = \frac{0.31V}{75m\Omega} = 4.13A \quad (7)$$

The fault event should be detected when the load current, I_{LOAD}, reaches 8A nominal. This corresponds to a voltage drop across the shunt resistor of V_{SENSE_FLT}:

$$V_{SENSE\_FLT} = R_{SHUNT} \times I_{OCP} = 75m\Omega \times 8A = 600mV \quad (8)$$

Since the fault comparator threshold of the TPSI3100-Q1 is also the nominal voltage reference (V_{REF}) of 0.31V, a resistor divider is required to scale the V_{SENSE_FLT} voltage to the comparator input threshold (V_{REF}). The divider ratio (DIV) required can be calculated from:

$$DIV = \frac{V_{REF}}{V_{SENSE\_FLT}} = \frac{0.31V}{0.6V} = 0.517 \quad (9)$$

$$DIV = \frac{R2}{R1 + R2} \quad (10)$$

For this design, the divider (DIV) was selected as 0.5. Therefore, R1 = R2. This leads to a nominal overcurrent of:

$$I_{OCP} = \frac{V_{REF}}{DIV \times R_{SHUNT}} = \frac{0.31V}{0.5 \times 75m\Omega} = 8.27A \quad (11)$$

The power dissipated in the shunt resistor while remaining at the alarm condition can be computed as:

$$P_{SHUNT\_ALM} = {I_{ALM}}^2 \times R_{SHUNT} = (4.13A)^2 \times 75m\Omega = 1.28W \quad (12)$$

Similarly, the power dissipated in the shunt resistor at the overcurrent condition can be computed as:

$$P_{SHUNT\_OCP} = {I_{OCP}}^2 \times R_{SHUNT} = (8.27A)^2 \times 75m\Omega = 5.13W \quad (13)$$

A power rating for the shunt resistor should be chosen that is sufficient to handle these power conditions compared to those experienced during normal loading. If the system can take necessary action in a timely manner upon an alarm condition, a 2W power rated resistor is deemed sufficient. An overcurrent event causes the driver to be disabled quickly by the TPSI3100-Q1, and the overload current exists for short duration. A more conservative approach is to select a 5W power rated resistor.

9.2.2.4 Overcurrent Fault Error

There are several sources of error that contribute to total error in the overcurrent detection accuracy. These include:

1. Voltage reference tolerance (includes comparator offset)
2. Shunt resistor tolerance
3. Divider resistor tolerances

For this design, an overcurrent protection accuracy of ±10% is required. The voltage reference tolerance of the TPSI3100-Q1 can be found in the *Electrical Characteristics* section of the data sheet and includes the comparator offset error.

The resistor tolerances of the resistor divider are chosen as 1%. The reference voltage tolerance is ±1.5%. Lastly, the selected shunt resistor tolerance is ±1%.

It is assumed that all error contributors are independent variables, so that the total expected error adds in a root mean squared fashion as follows:

$$\%Err_{OCP\_TOTAL} = \left[{\%Err_{VREF}}^2 + {\%Err_{R1}}^2 + {\%Err_{R2}}^2 + {\%Err_{RSHUNT}}^2 \right]^{0.5} \quad (14)$$

$$\%Err_{OCP\_TOTAL} = \left[(1.5\%)^2 + (1\%)^2 + (1\%)^2 + (1\%)^2 \right]^{0.5} = 2.3\% \quad (15)$$

9.2.2.5 Overcurrent Alarm Error

The total error for the alarm or warning indicator is similar to the overcurrent protection total error except the error contribution due to the resistor divider does not affect the total error. As before, it is assumed that all error contributors are independent variables, so that the total expected error adds in a root mean squared fashion as follows:

$$\%Err_{ALM\_TOTAL} = \left[\%Err_{VREF}{}^{2} + \%Err_{RSHUNT}{}^{2}\right]^{0.5} \quad (16)$$

$$\%Err_{ALM\_TOTAL} = \left[(1.5\%)^{2} + (1\%)^{2}\right]^{0.5} = 1.8\% \quad (17)$$

9.2.2.6 VDDP Capacitance, C_{VDDP}

For this design, 1µF in parallel with 100nF is used.

9.2.3 Application Curves

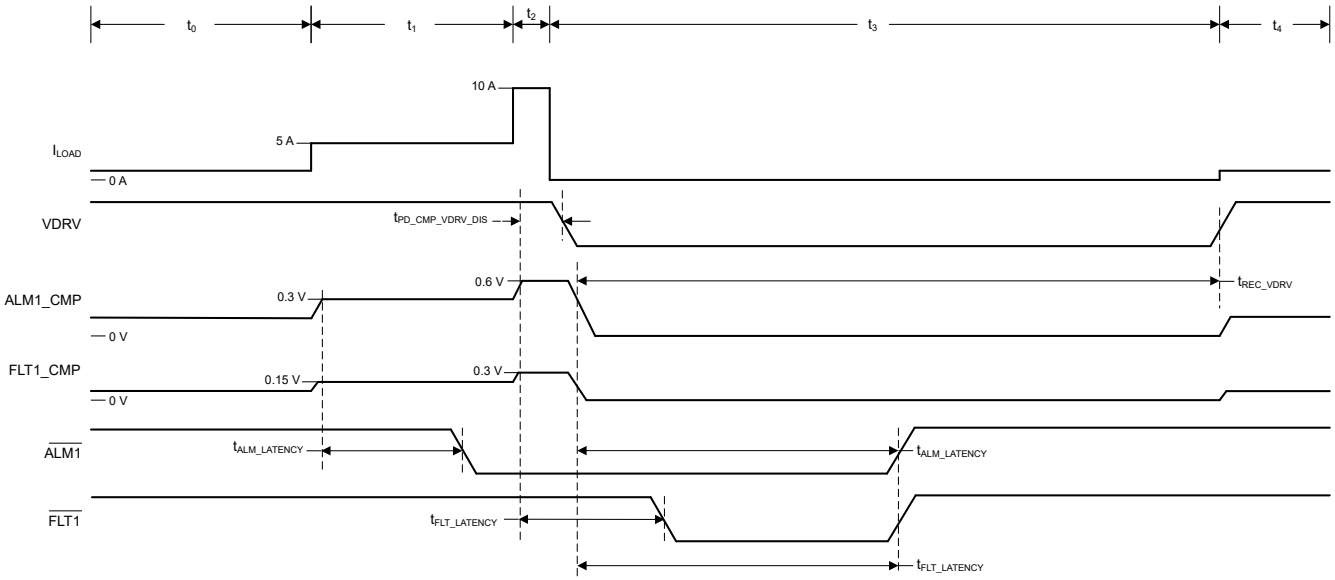


図 9-7. Overcurrent Protection Typical Timing and Behavior

- At t_0: VDRV is asserted high and the external FETs are supplying load current, I_{LOAD}. I_{LOAD} is in its normal operating range and is below the alarm level setting of 4A, nominal. ALM1_CMP and FLT1_CMP comparator input voltages are below the comparator threshold set by VREF of the TPSI3100-Q1 of 0.31V,nominal). $\overline{ALM1}$ and $\overline{FLT1}$ faults are asserted high pulled-up by external resistor pull-ups to VDDP.
- At t_1: I_{LOAD} current increases and reaches the alarm level setting of 4A, nominal. ALM1_CMP comparator input voltage reaches its threshold of 0.31V and $\overline{ALM1}$ asserts low within $t_{ALM\_LATENCY}$. VDRV remains asserted high since the FLT1_CMP comparator input threshold has not been reached. $\overline{FLT1}$ remains asserted high pulled-up by the external resistor pull-up to VDDP.
- At t_2: I_{LOAD} current continues to increases and reaches the fault level setting of 8A, nominal. FLT1_CMP comparator input voltage reaches its threshold of 0.31V and VDRV is quickly asserted low to disable the external FETs. $\overline{FLT1}$ asserts low within $t_{FLT\_LATENCY}$. $\overline{ALM1}$ remains asserted low since the ALM1_CMP comparator input exceeds its threshold.
- At t_3: Since the FETs have been turned off, I_{LOAD}, is removed. FLT1_CMP and ALM1_CMP comparator inputs drop below their thresholds, settling to VSSS. VDRV remains asserted low keeping the external FETs off for t_{REC_VDRV}. $\overline{FLT1}$ and $\overline{ALM1}$ assert high within $t_{FLT\_LATENCY}$ and $t_{ALM\_LATENCY}$, respectively indicating to the system that fault and alarm conditions have been removed.
- At t_4: VDRV asserts high again since EN remains high, t_{REC_VDRV} time has elapsed, and the fault condition is no longer present. The external FETs are enabled and supply I_{LOAD} in its normal operating range.

図 9-8 shows a typical waveform capture. At time 0µs, a load current (I_{LOAD}) pulse of over 5A is applied. Since this is above the alarm comparator threshold of 4.13A, $\overline{ALM1}$ indicator is asserted low within $t_{ALM\_LATENCY}$, in this case, near time 5µs. Approximately at time 15µs, a load current pulse of over 10A is applied. Since this is above the fault comparator threshold of 8.27A, VDRV is quickly asserted low to protect the power FET, and I_{LOAD} drops to 0A. $\overline{FLT1}$ is asserted low within $t_{FLT\_LATENCY}$, in this case, near time 30µs. Both the fault and alarm comparator thresholds are exceeded on the second load current pulse. After I_{LOAD} falls below both the fault and alarm comparator thresholds, $\overline{ALM1}$ and $\overline{FLT1}$ assert high near time 55µs, indicating no alarm or fault is present. VDRV remains asserted low until t_{REC_VDRV} time elapses, near time 180µs.

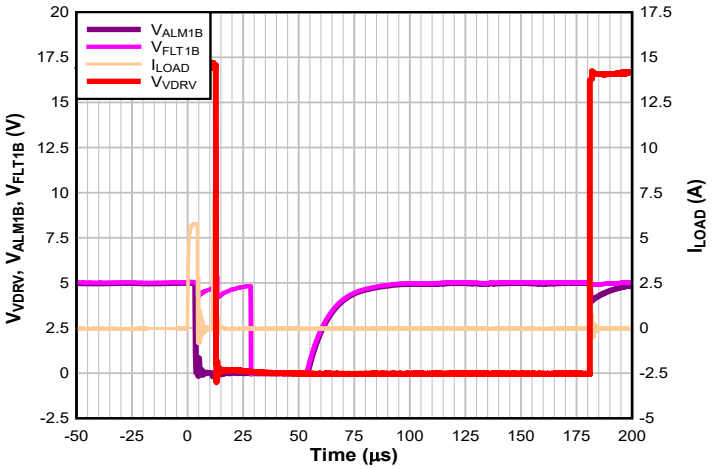


図 9-8. Overcurrent Protection and VDRV Auto-recovery

9.3 Power Supply Recommendations

To help ensure a reliable supply voltage, TI recommends that the C_{VDDP} capacitance from VDDP to VSSP consists of a 0.1µF bypass capacitor for high frequency decoupling in parallel with a 1µF for low frequency decoupling. Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

9.4 Layout

9.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitance on the RESP pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.

- EMI considerations:

  The TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ employs spread spectrum modulation (SSM) for optimized EMI performance. Depending on the system requirements and safety preferences of the system designer, additional measures to minimize EMI can be takes as follows:

  – Inductive components: A pair of ferrite beads or a common mode choke can be placed in series with VDDP supply and VSSP ground to increase the common mode loop impedance.
  – Capacitive components: Most designs already employ discrete Y capacitors or include parasitic Y capacitance between the high voltage and low voltage domains. Incorporating this Y capacitance on the same board as the TPSI310x-Q1、TPSI311x-Q1、TPSI312x-Q1、TPSI3133-Q1 ファミリ, provides a capacitive return path from the secondary side to the primary side.
- High-voltage considerations:
  – To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  – Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  – If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

9.4.2 Layout Example

図 9-9 shows a PCB layout example with the signals and key components labeled.

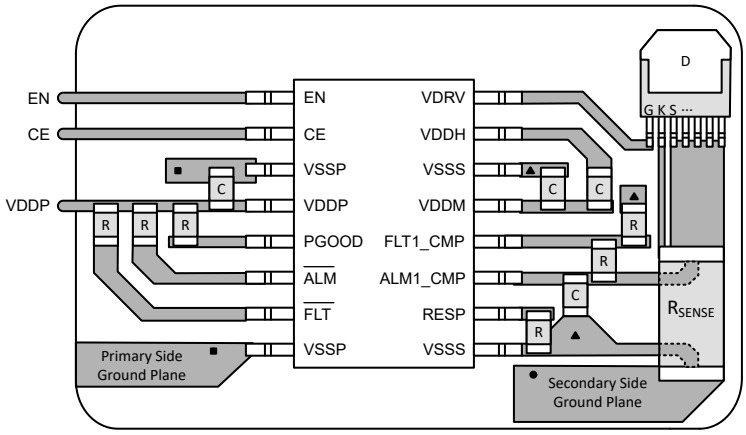


図 9-9. Layout example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary*

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.4 Trademarks

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10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2023) to Revision A (November 2024)	Page
• ドキュメントのステータスを「事前情報」から「*量産データ*」	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPSI3100LQDVXRQ1.A	Active	Preproduction	SO-MOD (DVX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPSI3100LQDVXRQ1.B	Active	Preproduction	SO-MOD (DVX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSI3100LQDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3100LQ
TPSI3100QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3100Q
TPSI3100QDVXRQ1.A	Active	Production	SO-MOD (DVX) | 16	1000 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3100Q
TPSI3100QDVXRQ1.B	Active	Production	SO-MOD (DVX) | 16	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPSI3103LQDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3103LQ
TPSI3103QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3103Q
TPSI3110LQDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3110LQ
TPSI3110QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3110Q
TPSI3113LQDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3113LQ
TPSI3113QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3113Q
TPSI3120QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3120Q
TPSI3123QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3123Q
TPSI3133QDVXRQ1	Active	Production	SO-MOD (DVX) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TI3133Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPSI3100-Q1 :

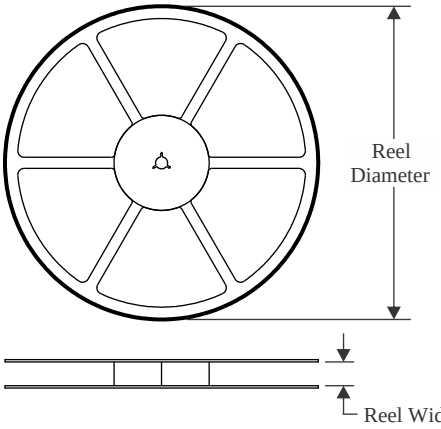
- Catalog : TPSI3100

NOTE: Qualified Version Definitions:

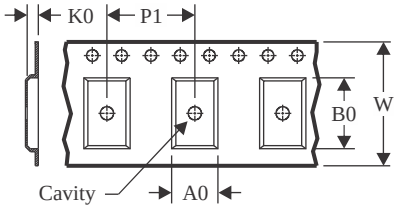
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

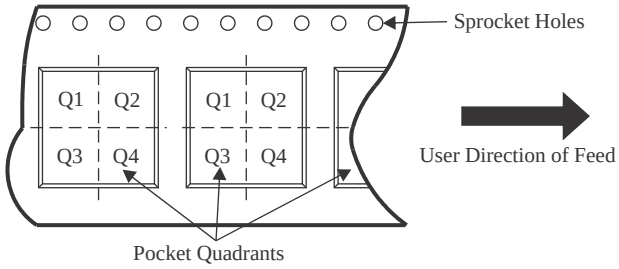


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

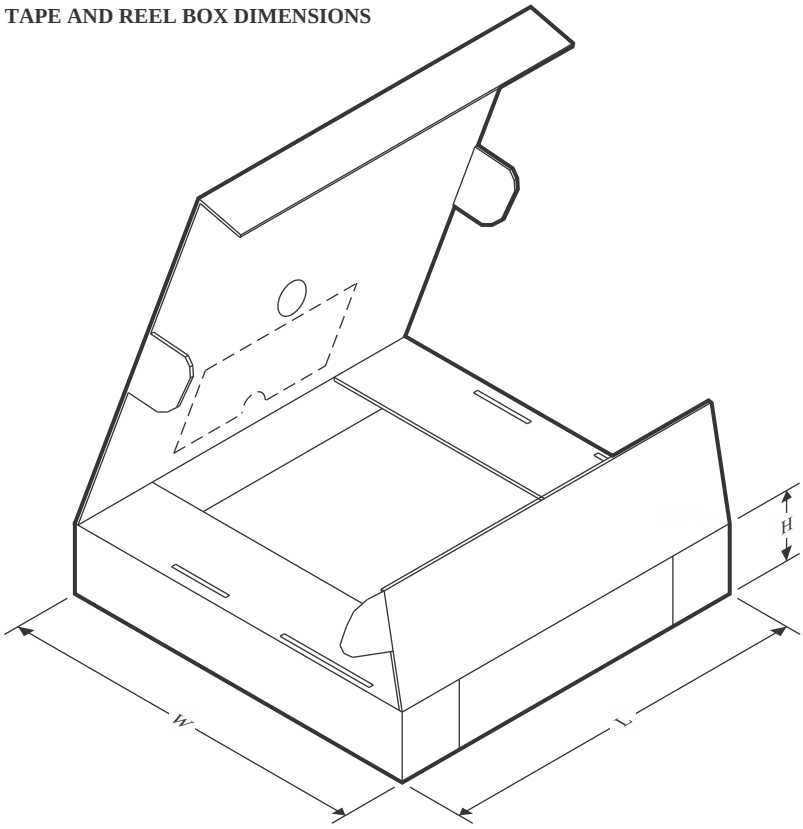
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSI3100LQDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3100QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3103LQDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3103QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3110LQDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3110QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3113LQDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3113QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3120QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3123QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3133QDVXRQ1	SO-MOD	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSI3100LQDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3100QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3103LQDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3103QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3110LQDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3110QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3113LQDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3113QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3120QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3123QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0
TPSI3133QDVXRQ1	SO-MOD	DVX	16	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

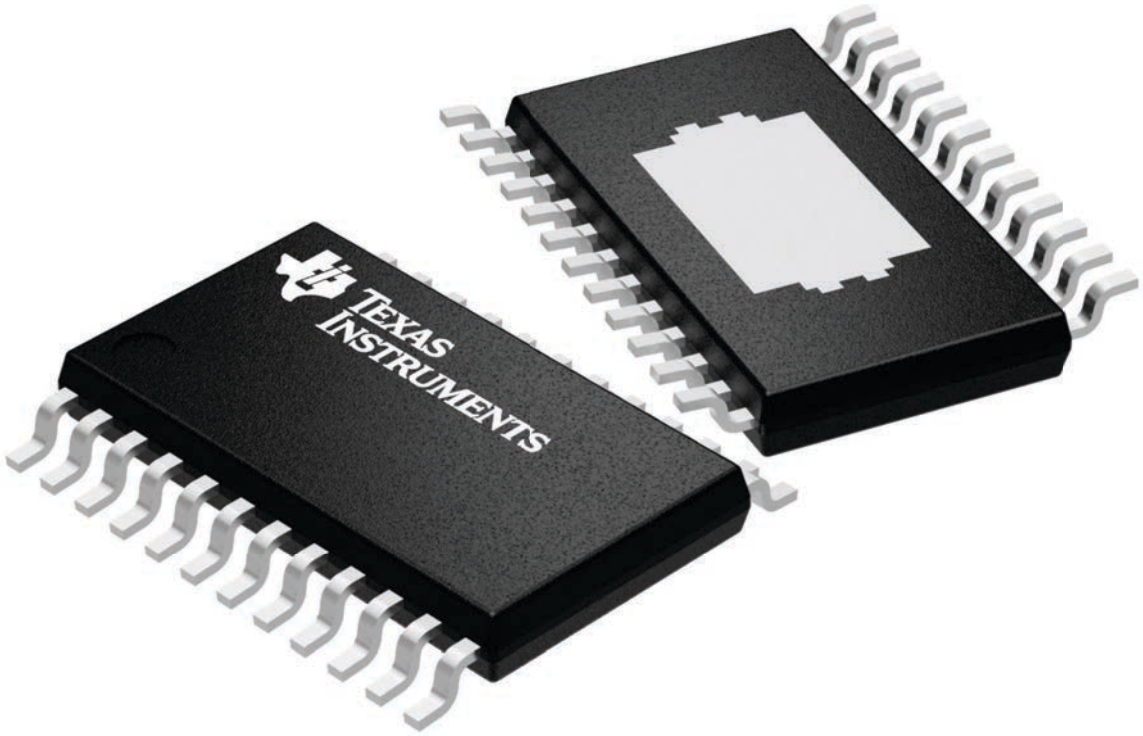
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



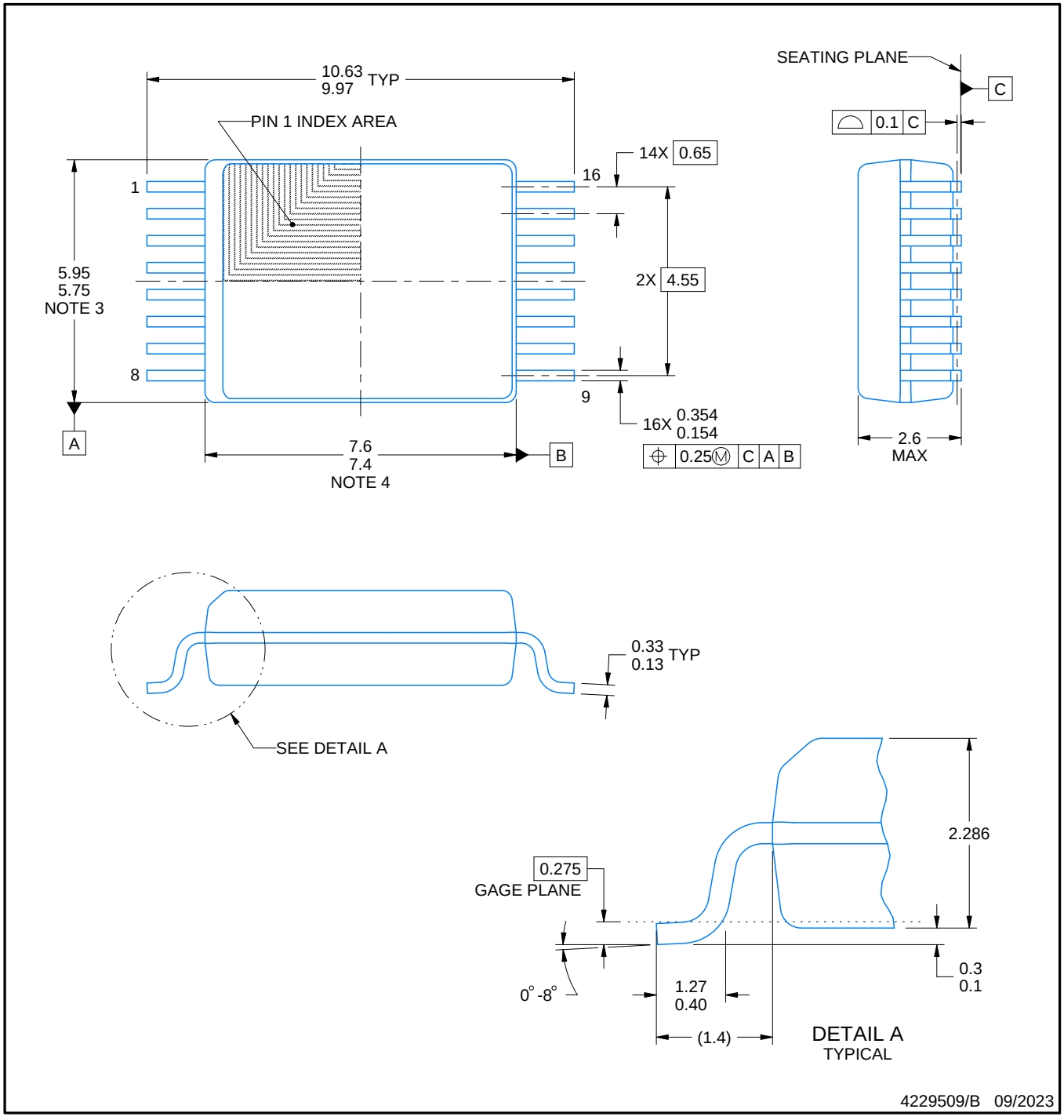
4224742/B

PACKAGE OUTLINE

DVX0016A

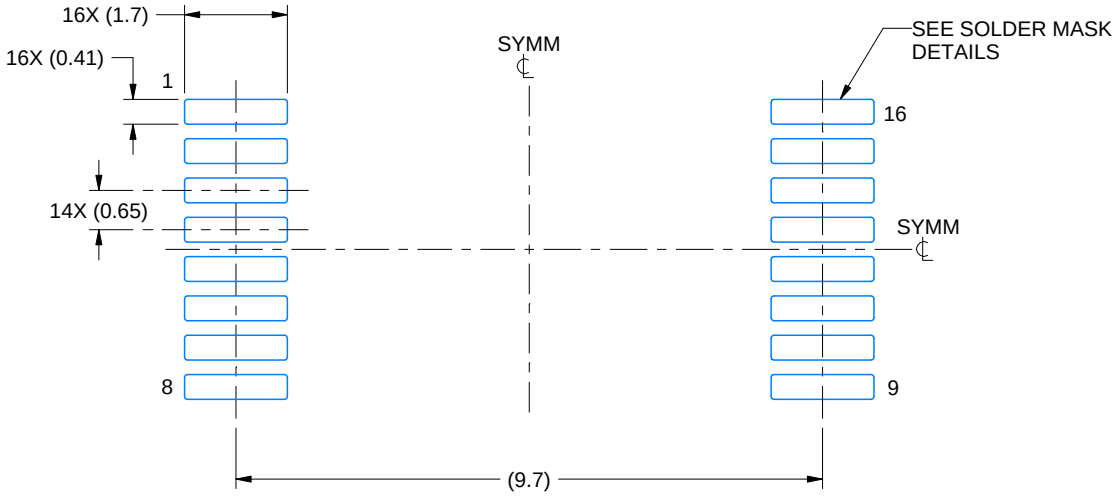
SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE

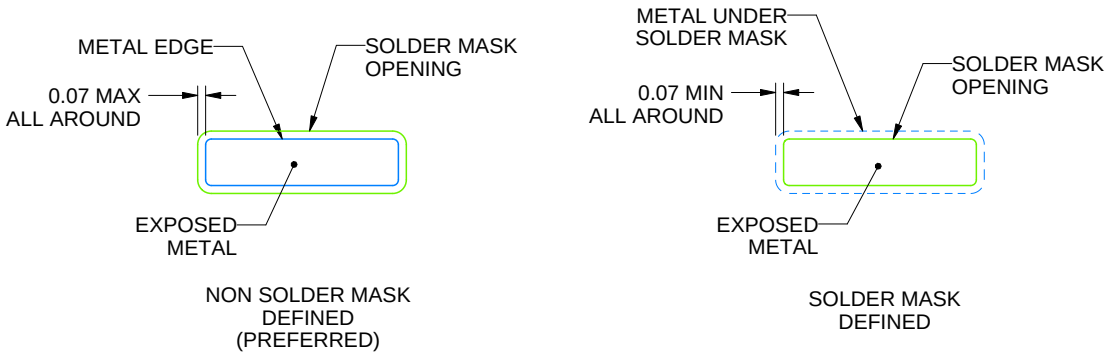


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4229509/B 09/2023

NOTES: (continued)

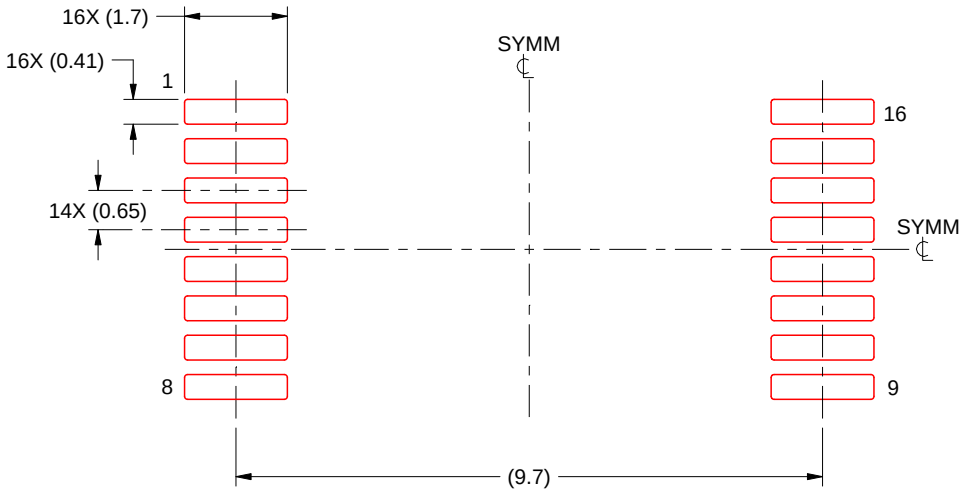
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

DWG_NO:3/REV:3 MM_YYYY:3

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月