TPS82084 (2A) / TPS82085 (3A) インダクタ内蔵の高効率降圧コンバータ MicroSiP™モジュール

1 特長

- 低プロファイルの MicroSiP™電源モジュール
- DCS-Control トポロジ
- 最大 95% の効率
- 動作時の静止電流 17µA
- -40℃～125℃の動作温度範囲
- ヒカップ短絡保護機能
- 入力電圧範囲：2.5V～6V
- 出力電圧は 0.8V～V_{IN} まで可変
- パワー・セーブ・モードにより軽負荷時の効率を向上
- 100% デューティ·サイクル動作によりドロップアウト電圧が最小限
- 出力放電機能
- パワー・グッド出力
- ソフト・スタートアップを内蔵し、プリバイアス・スタートアップをサポート
- 過熱保護
- CISPR11 Class B 準拠
- 2.8mm x 3.0mm x 1.3mm、8 ピンの µSiL パッケージ

2 アプリケーション

- 光学モジュール
- シングル・ボード・コンピュータ
- ソリッド・ステート・ドライブ (SSD)
- 都市部データ・センター
- オーディオ/ビデオ制御システム
- レーダー

3 概要

TPS82084/5 は 2A/3A の降圧コンバータ MicroSiP™モジュールで、小型で高効率のソリューション用に最適化されています。この電源モジュールには同期整流降圧型コンバータとインダクタが組み込まれているため、設計を簡素化し、外付けコンポーネントを減らして、PCB 面積を削減できます。薄く小型のソリューションなので、標準の表面実装機による自動組み立てに適しています。

製品情報(1)

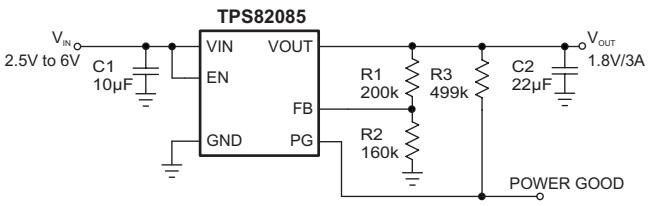
型番	パッケージ	本体サイズ(公称)
TPS82085	µSiL (8)	2.8mm×3.0mm
TPS82084	µSiL (8)	2.8mm×3.0mm

デバイスの比較

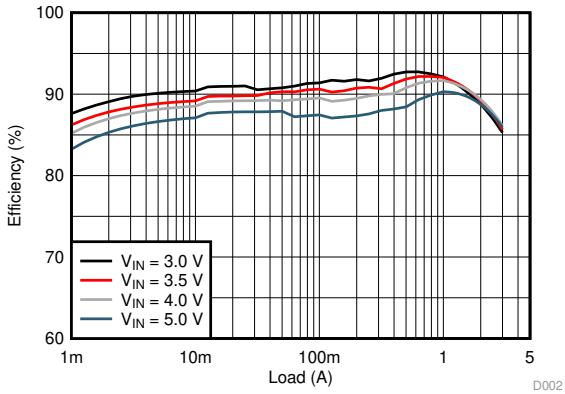
型番	出力電流
TPS82084	2A
TPS82085	3A

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

1.8V 出力のアプリケーション



1.8V 出力の効率



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4 改訂履歴

Revision C (September 2018) から **Revision D** に変更 **Page**

- タイトルの型番を訂正 ... 1
- Add the input voltage range for the output voltage discharge feature in Enable and Disable. ... 10

Revision B (April 2015) から **Revision C** に変更 **Page**

- データシートに TPS82084 デバイスを 追加 ... 1
- Changed from –40 ºC to –55 ºC for storage temperature range ... 4
- Added thermal information for TPS82085EVM-672. Updated thermal metric value. ... 5
- 追加 power save mode waveform diagram to Power Save Mode (PSM) ... 9
- 追加 typical value of the EN pin high/low level input voltage in Enable and Disable ... 10
- 追加 pg pin logic table in Power Good Output ... 10
- 追加 integrated inductor information in Application Information ... 11
- 追加 additional efficiency curves and a reference hyperlink to the BOM, 表 3 ... 13
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Revision A (April 2015) から **Revision B** に変更 **Page**

- Changed the *ESD Ratings* Charged device model (CDM) From: ±500 V To: ±1000 V ... 4

2014年10月 発行のものから更新 **Page**

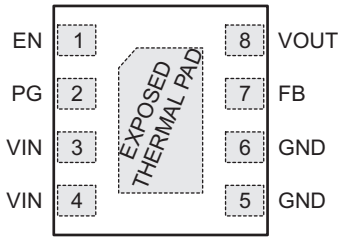
- データシートを 3 ページの製品プレビューから量産データに変更 ... 1

5 概要（続き）

最大の効率を実現するため、このコンバータは公称スイッチング周波数 2.4MHz の PWM モードで動作し、負荷電流が小さいときには自動的にパワー・セービング・モードの動作に移行します。パワー・セービング・モードでは、デバイスは標準 17µA の静止電流で動作します。このデバイスは DCS-Control トポロジを使用して、非常に優れた負荷過渡性能と、出力電圧の正確なレギュレーションを実現しています。EN および PG ピンはシーケンシング構成をサポートするため、柔軟なシステム設計が可能です。内蔵のソフト・スタートアップにより、入力電源からの突入電流が減少します。過熱保護およびヒカップ短絡保護機能により、堅牢で信頼性が高いソリューションを実現できます。

6 Pin Configuration and Functions

µSiL Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400 kΩ when the device is disabled.
PG	2	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
VIN	3,4	PWR	Input voltage pin.
GND	5,6		Ground pin.
FB	7	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
VOUT	8	PWR	Output voltage pin.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	EN, PG, VIN, FB, VOUT	-0.3	7	V
Sink current	PG		1.0	mA
Module operating temperature range		-40	125	°C
Storage temperature range		–55	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.5	6	V
V_{PG}	Power good pull-up resistor voltage		6	V

Recommend Operating Conditions (continued)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{OUT}	Output voltage range	0.8	V_{IN}	V
I_{OUT}	Output current range, TPS82084 (1)	0	2	A
	Output current range, TPS82085 (1)	0	3	A
T_J	Module operating temperature range (1)	-40	125	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated.

7.4 Thermal Information

THERMAL METRIC (1)		TPS82084/5SIL (JEDEC 51-5)	TPS82085EVM-672	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.6	46.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.1	n/a (2)	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	n/a (2)	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	
ψ_{JB}	Junction-to-board characterization parameter	23.3	24.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.2	15.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953
(2) Not applicable to an EVM

7.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 2.5V to 6V. Typical values are at T_J = 25°C and V_{IN} = 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_Q	Quiescent current into VIN	No load, device not switching T_J = -40°C to 85°C, V_{IN} = 2.5 V to 5.5 V		17	25	µA
I_{SD}	Shutdown current into VIN	EN = Low, T_J = -40°C to 85°C, V_{IN} = 2.5 V to 5.5 V		0.7	5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
		V_{IN} rising	2.3	2.4	2.5	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage		1.0			V
V_{IL}	Low-level input voltage				0.4	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High		0.01	0.16	µA
R_{PD}	Pull-down resistance at EN pin	EN = Low		400		kΩ
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		0.8		ms
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	93%	95%	98%	
		V_{OUT} falling, referenced to V_{OUT} nominal	88%	90%	93%	
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1mA			0.4	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 5V		0.01	0.16	µA

Electrical Characteristics (continued)

T_J = -40°C to 125°C and V_{IN} = 2.5V to 6V. Typical values are at T_J = 25°C and V_{IN} = 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Output voltage range		0.8		V_{IN}	V
V_{FB}	Feedback regulation voltage	PWM mode	792	800	808	mV
		PSM mode, C_{OUT} = 22 µF	792	800	817	
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.8 V		0.01	0.1	µA
R_{DIS}	Output discharge resistor	EN = Low, V_{OUT} = 1.8 V		260		Ω
	Line regulation	I_{OUT} = 1 A, V_{IN} = 2.5 V to 6 V		0.02		%/V
	Load regulation	I_{OUT} = 0.5 A to 3 A		0.16		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500 mA		31	56	mΩ
	Low-side FET on-resistance	I_{SW} = 500 mA		23	45	mΩ
R_{DP}	Dropout resistance	100% mode		69		mΩ
I_{LIMF}	High-side FET switch current limit	TPS82085	3.7	4.6	5.5	A
		TPS82084		3.6		
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		2.4		MHz

7.6 Typical Characteristics

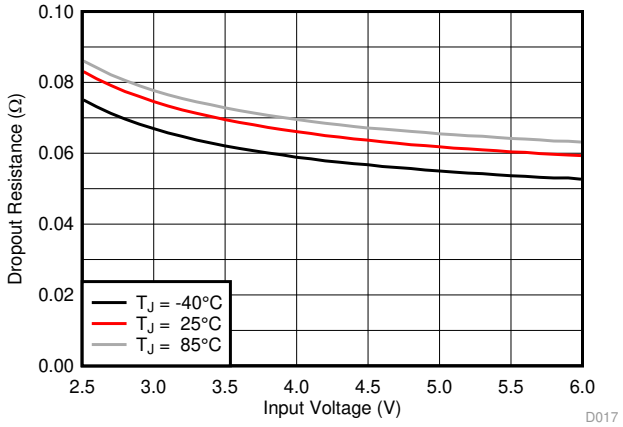


図 1. Dropout Resistance

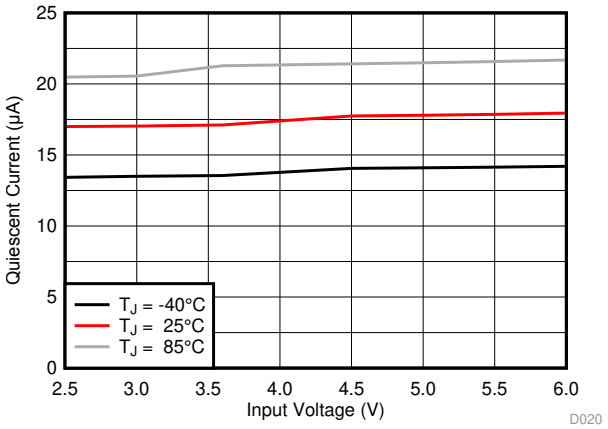


図 2. Quiescent Current

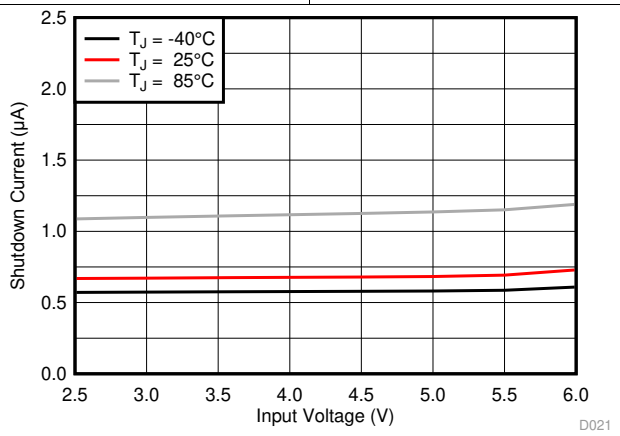


図 3. Shutdown Current

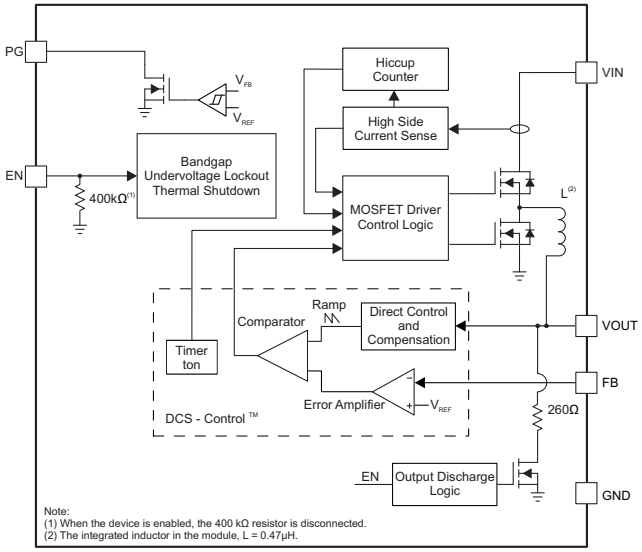
8 Detailed Description

8.1 Overview

The TPS82084/5 synchronous step-down converter power modules are based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage and current mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power Save Mode) at light load currents. In PWM, the converter operates with its nominal switching frequency of 2.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The device offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Save Mode (PSM)

The device includes a fixed on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 420\ ns \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^{2} \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

To maintain high efficiency at light loads, the device enters Power Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with a reduced switching frequency and with a minimum quiescent current to maintain high efficiency. The on time in PSM is also based on the same t_{ON} circuitry. The switching frequency in PSM is shown in 式 1.

Feature Description (continued)

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

During PAUSE period in PSM (shown in 図 4), the device does not change the PG pin state nor does it detect an UVLO event, in order to achieve a minimum quiescent current and maintain high efficiency at light loads.

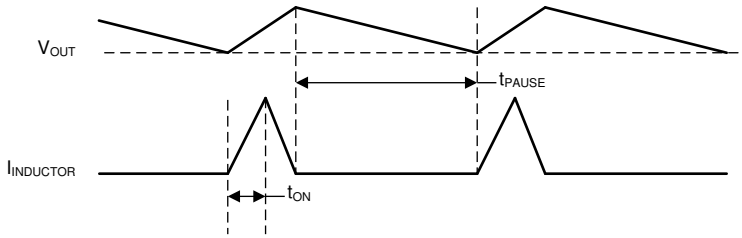


図 4. Power Save Mode Waveform Diagram

8.3.2 Low Dropout Operation (100% Duty Cycle)

The device offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (2)$$

Where

R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor.

$V_{OUT(min)}$ = Minimum output voltage the load can accept.

8.3.3 Soft Startup

The device has an internal soft start circuit which ramps up the output voltage to the nominal voltage during a soft start time of typically 0.8ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to monotonically start into a pre-biased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Short Circuit Protection (Hiccup-Mode)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current. Once this switch current limits is triggered 32 times, the devices stop switching and enables the output discharge. The devices then automatically start a new startup after a typical delay time of 66µs has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears.

8.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic High (typical 0.8 V). Accordingly, shutdown mode is forced if the EN pin is pulled Low (typical 0.7 V) with a shutdown current of typically 0.7 μA. An internal resistor of 260 Ω discharges the output via the VOUT pin smoothly when the device is disabled. The output discharge function also works when thermal shutdown, undervoltage lockout or short circuit protection are triggered. The output discharge function stops working when the input voltage has decreased to around 0.5V.

An internal pull-down resistor of 400 kΩ is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

8.4.2 Power Good Output

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. 表 1 shows the PG pin logic.

表 1. PG Pin Logic

	DEVICE CONDITIONS	LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} < V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.5\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 0.5\ V$	√	

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS82084/5 are synchronous step-down converter power modules whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

The required power inductor is integrated inside the TPS82084/5. The inductor is shielded and has an inductance of 0.47 µH with approximately a +/- 20% tolerance. The TPS82084 and TPS82085 are pin-to-pin and BOM-to-BOM compatible, differing only in their rated output current.

9.2 Typical Applications

9.2.1 1.2-V Output Application

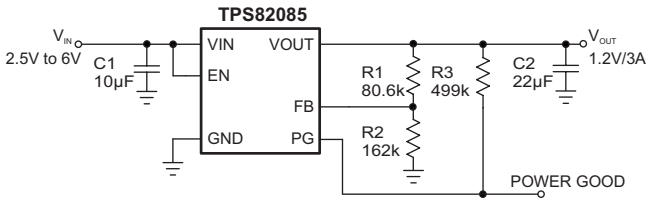


図 5. 1.2-V Output Application

9.2.1.1 Design Requirements

For this design example, use the input parameters shown in 表 2.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage	1.2 V
Output ripple voltage	< 20 mV
Output current rating	3 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A106KE51	Murata
C2	22µF, Ceramic Capacitor, 6.3V, X7R, size 0805, CL21B226MQQNNNE or 22µF, Ceramic Capacitor, 6.3V, X7S, size 0805, C2012X7S1A226M125AC	Samsung or TDK
R1	Depending on the output voltage, 1% accuracy	Std
R2	162kΩ, 1% accuracy	Std
R3	499kΩ, 1% accuracy	Std

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

R2 should not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. 図 5 shows a recommended external resistor divider value for a 1.2-V output. Choose appropriate resistor values for other output voltages.

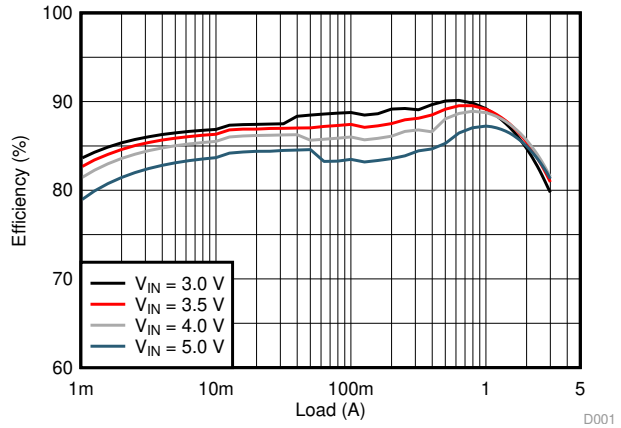
9.2.1.2.2 Input and Output Capacitor Selection

For best output and input voltage filtering, ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22 µF up to more than 150 µF. The recommended typical output capacitor value is 22µF. Values over 150 µF may be possible with a reduced load during startup in order to avoid triggering the Hiccup short circuit protection. A feed forward capacitor is not required for proper operation.

Ceramic capacitor has a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least 5µF and the output effective capacitance is at least 8µF.

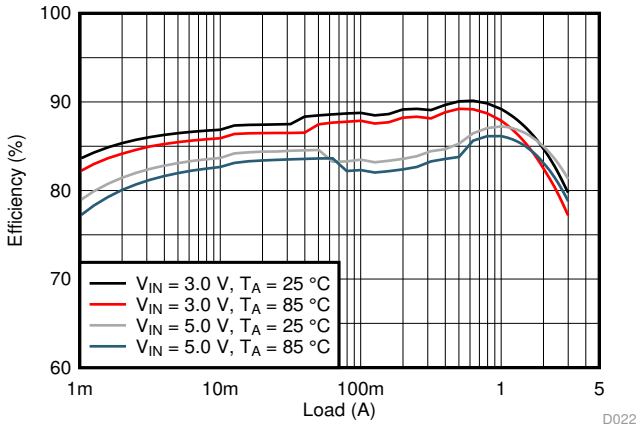
9.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, BOM = 表 3 unless otherwise noted.



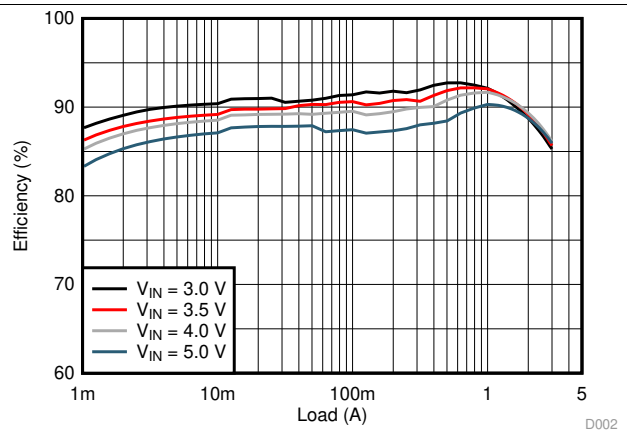
V_{OUT} = 1.2 V

図 6. Efficiency



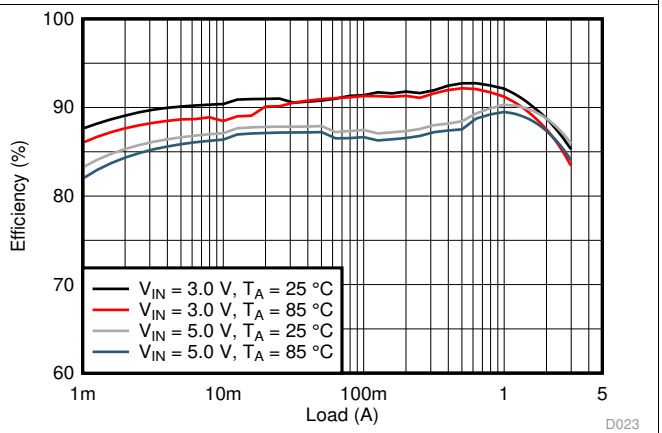
V_{OUT} = 1.2 V

図 7. Efficiency



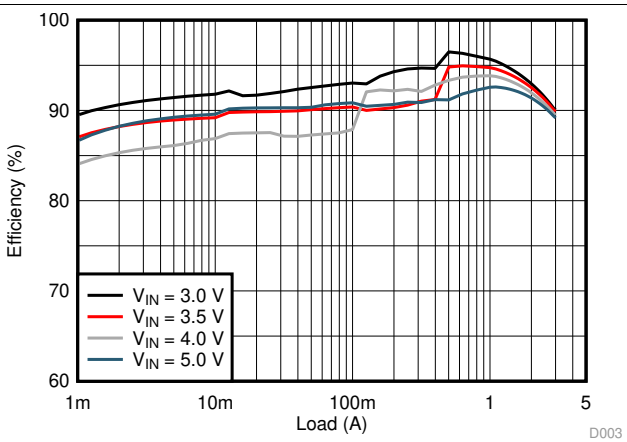
V_{OUT} = 1.8 V

図 8. Efficiency



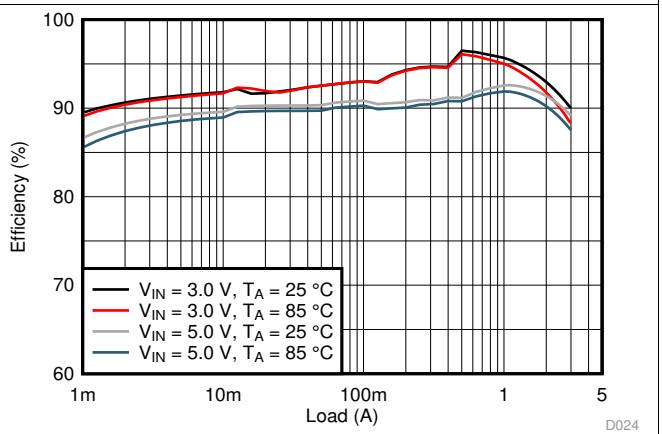
V_{OUT} = 1.8 V

図 9. Efficiency



V_{OUT} = 2.6 V

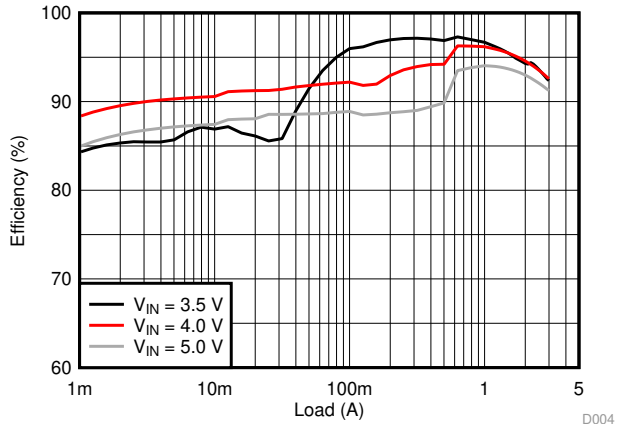
図 10. Efficiency



V_{OUT} = 2.6 V

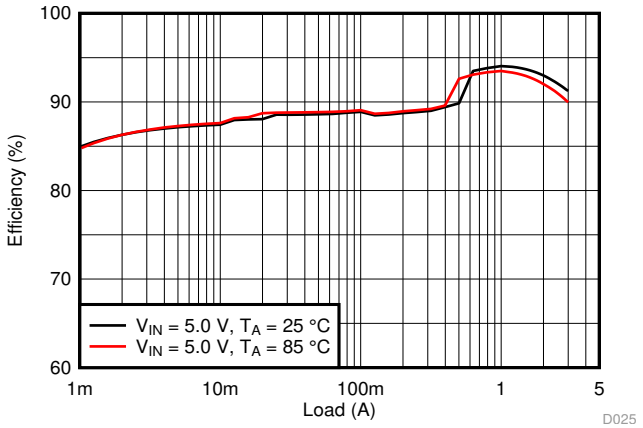
図 11. Efficiency

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, BOM = 表 3 unless otherwise noted.



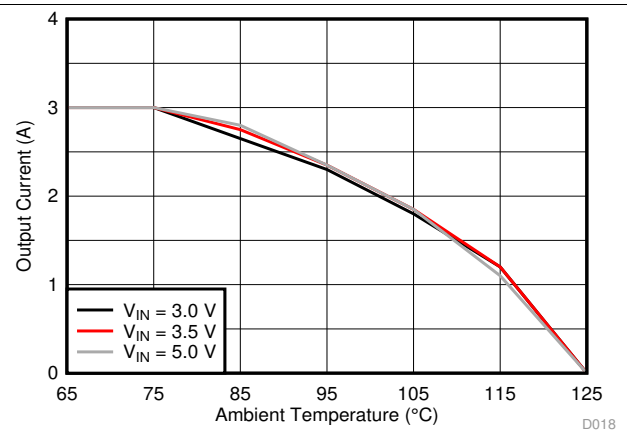
V_{OUT} = 3.3 V

図 12. Efficiency



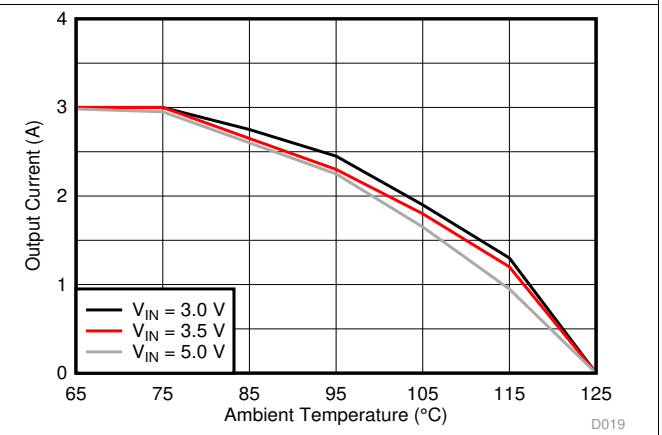
V_{OUT} = 3.3 V

図 13. Efficiency



V_{OUT} = 1.2 V θ_{JA} = 46.6°C/W

図 14. Thermal Derating



V_{OUT} = 2.6 V θ_{JA} = 46.6°C/W

図 15. Thermal Derating

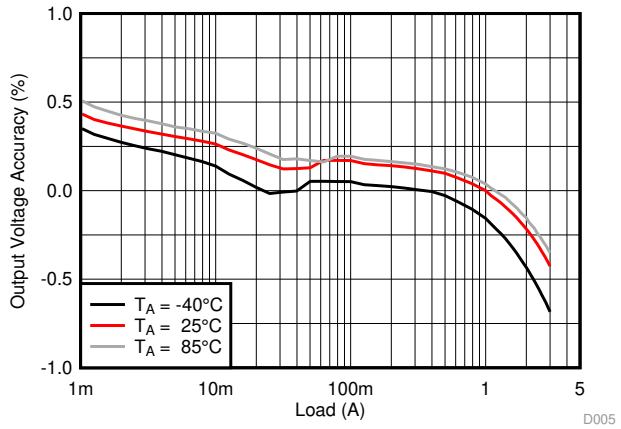
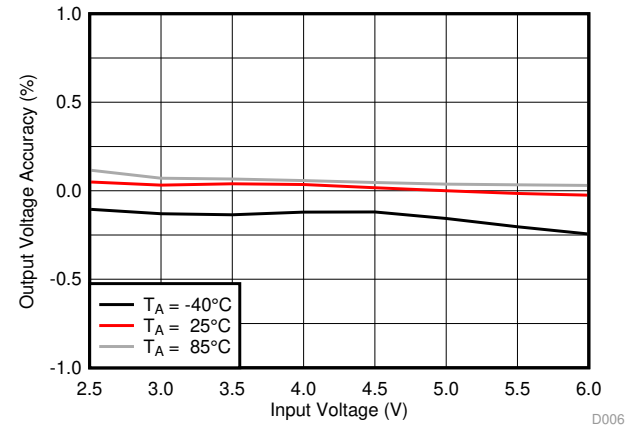


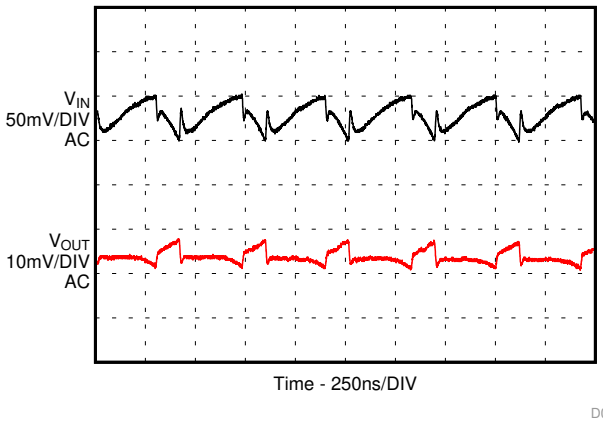
図 16. Load Regulation



I_{OUT} = 1 A

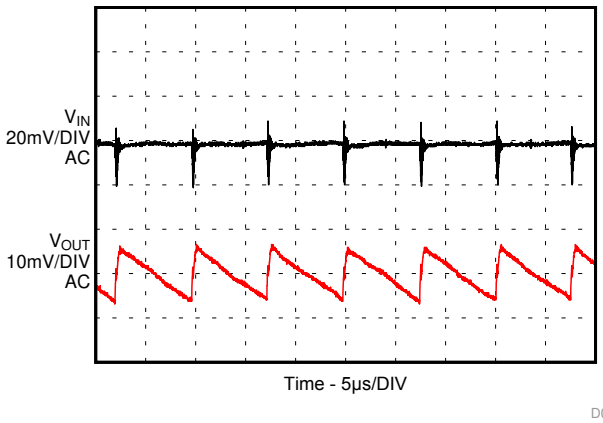
図 17. Line Regulation

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, BOM = 表 3 unless otherwise noted.



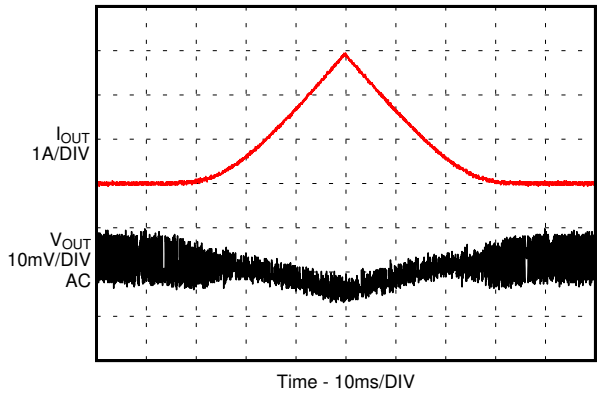
I_{OUT} = 2 A

図 18. Input and Output Ripple in PWM Mode



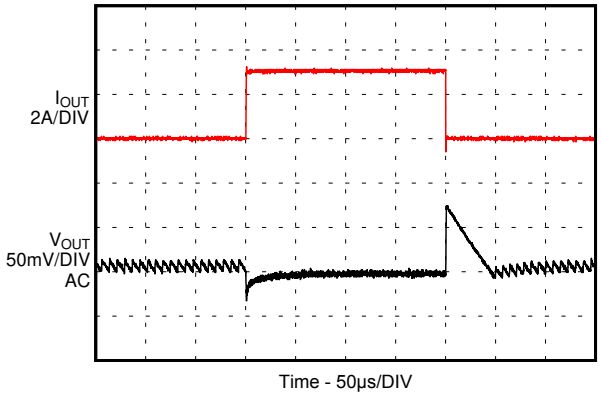
I_{OUT} = 25 mA

図 19. Input and Output Ripple in PSM Mode



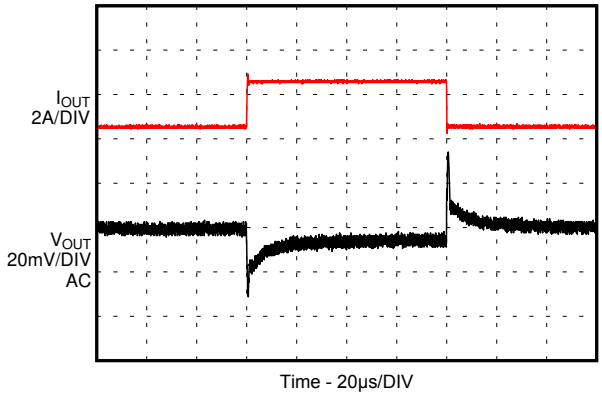
I_{OUT} = 25 mA to 3 A

図 20. Load Sweep



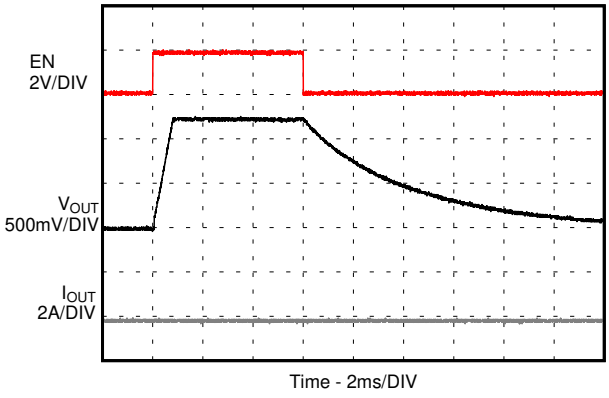
I_{OUT} = 25 mA to 3 A

図 21. Load Transient



I_{OUT} = 0.5 A to 2.5 A

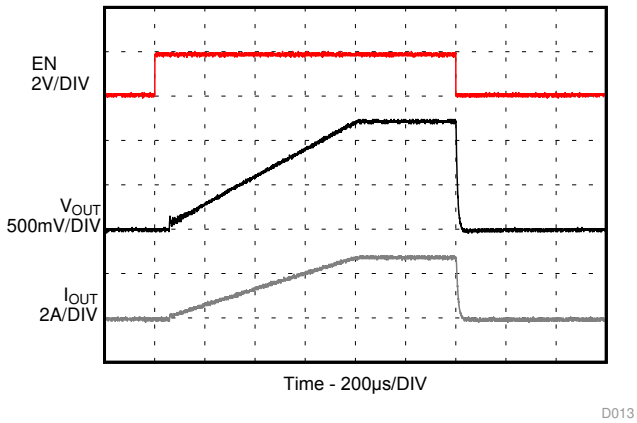
図 22. Load Transient



I_{OUT} = no load

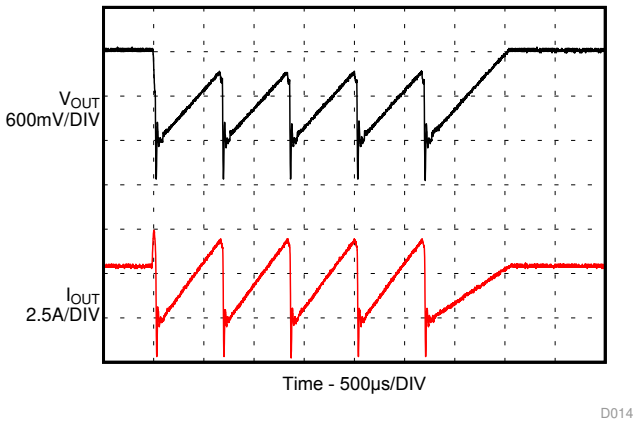
図 23. Startup / Shutdown without Load

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, BOM = 表 3 unless otherwise noted.



Load = 0.4 Ω

図 24. Startup / Shutdown with Resistive Load



I_{OUT} = 3 A

図 25. Short Circuit, HICCUP Protection Entry / Exit

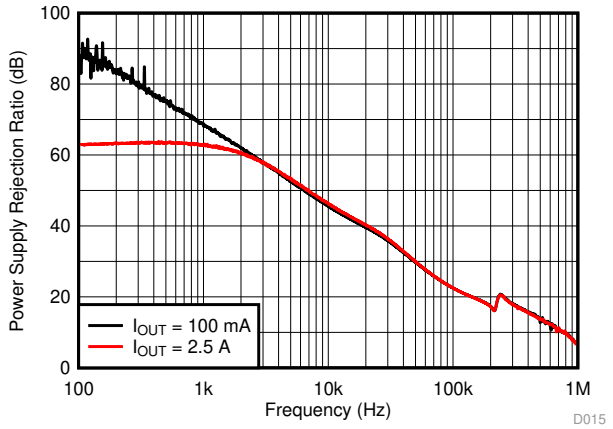


図 26. Power Supply Rejection Ratio (PSRR)

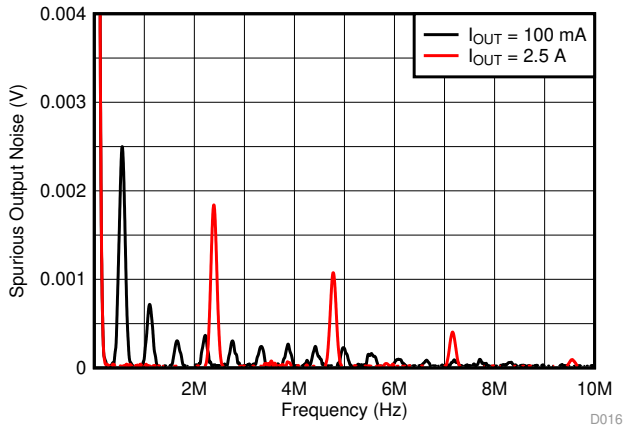
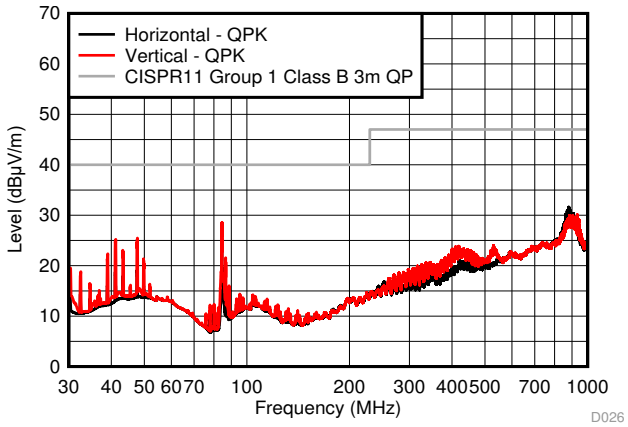
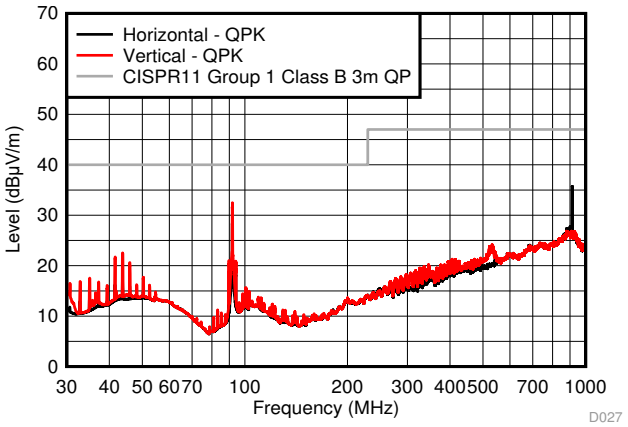


図 27. Spurious Output Noise



R_{LOAD} = 0.47 Ω, V_{IN} = 5 V (battery supply), V_{OUT} = 1.2 V, EMI test board without filters

図 28. TPS82085 Radiated Emission



R_{LOAD} = 0.68 Ω, V_{IN} = 5 V (battery supply), V_{OUT} = 1.2 V, EMI test board without filters

図 29. TPS82084 Radiated Emission

10 Power Supply Recommendations

The devices are designed to operate from an input supply voltage range between 2.5 V and 6 V. The average input current of the TPS82084/5 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (4)$$

Ensure that the power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

- It is recommended to place all components as close as possible to the IC. Specially, the input capacitor placement must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to 図 30 for an example of component placement, routing and thermal design.
- The recommended land pattern for the TPS82084/5 is shown at the end of this data sheet. For best manufacturing results, it is important to create the pads as solder mask defined (SMD). This keeps each pad the same size and avoids solder pulling the device during reflow.

11.2 Layout Example

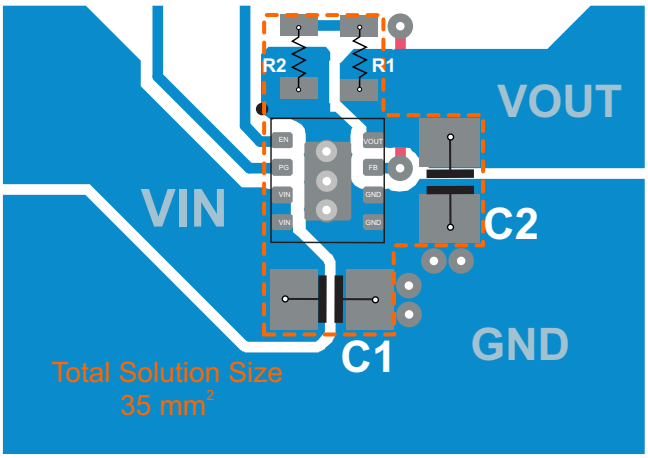


図 30. TPS82084/5 PCB Layout

11.3 Thermal Consideration

The TPS82084/5's output current needs to be derated when the device operates in a high ambient temperature or deliver high output power. The amount of current derated is dependent upon the input voltage, output power, PCB layout design and environmental thermal condition.

The TPS82084/5 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82084/5, apply the typical efficiency stated in this datasheet to the desired application condition for the module power dissipation, then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS82085	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS82084	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

MicroSiP, DCS-Control, E2E are trademarks of Texas Instruments.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

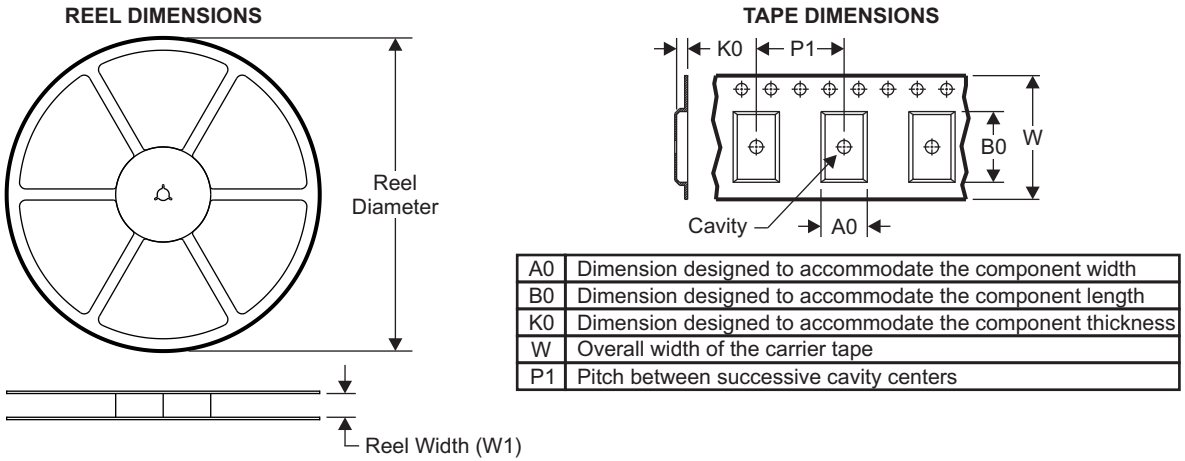
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

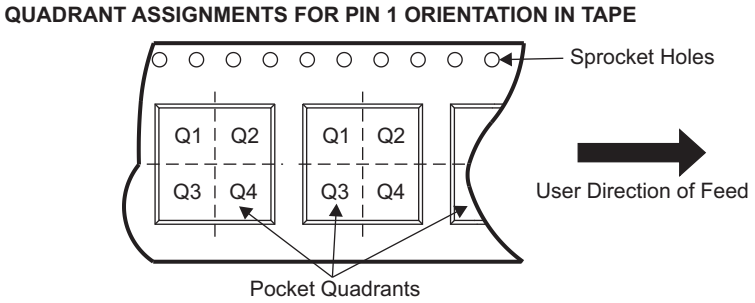
13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

13.1 Tape and Reel Information

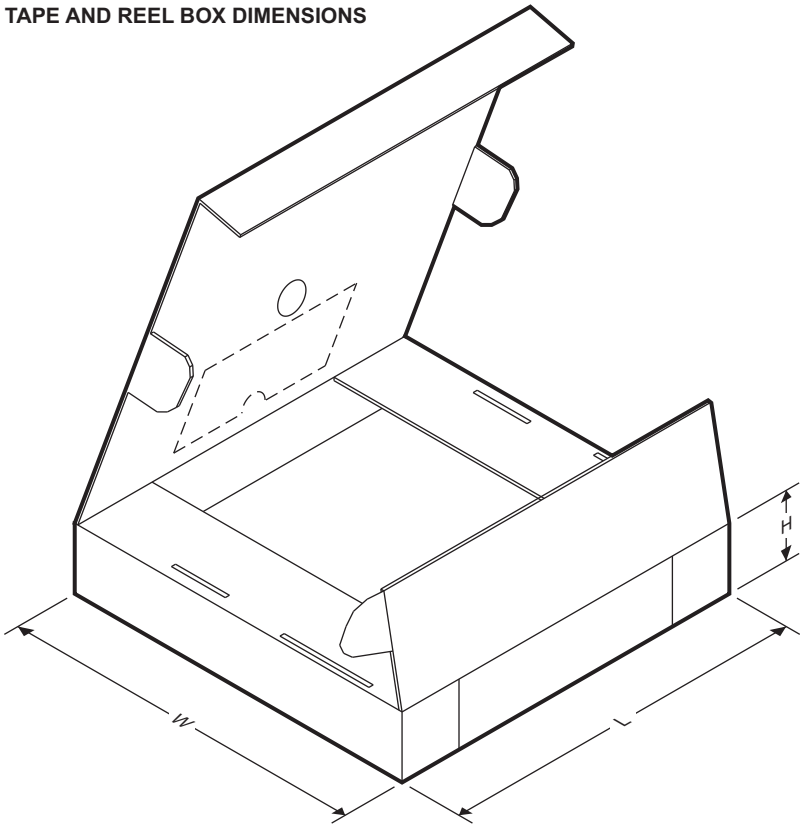


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82084SILR	uSiP	SIL	8	3000	330.0	12.4	3.0	3.2	1.45	4.0	12.0	Q1
TPS82084SILT	uSiP	SIL	8	250	178.0	13.2	3.0	3.2	1.45	4.0	12.0	Q1
TPS82085SILR	uSiP	SIL	8	3000	330.0	12.4	3.0	3.2	1.45	4.0	12.0	Q1
TPS82085SILT	uSiP	SIL	8	250	178.0	13.2	3.0	3.2	1.45	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



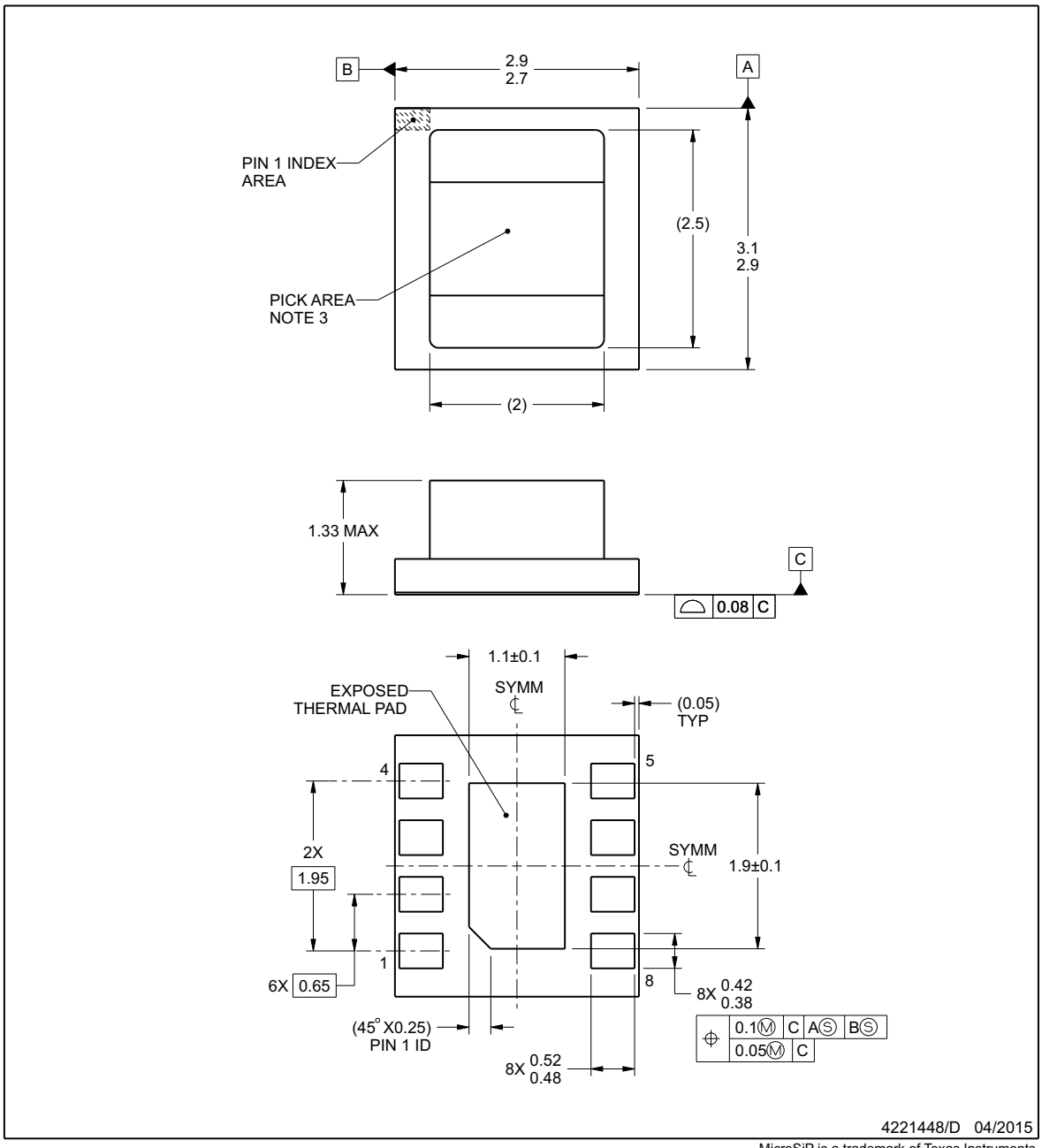
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82084SILR	uSiP	SIL	8	3000	383	353	58
TPS82084SILT	uSiP	SIL	8	250	223	194	35
TPS82085SILR	uSiP	SIL	8	3000	383	353	58
TPS82085SILT	uSiP	SIL	8	250	223	194	35

PACKAGE OUTLINE

SIL0008C

MicroSiP™ - 1.33 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

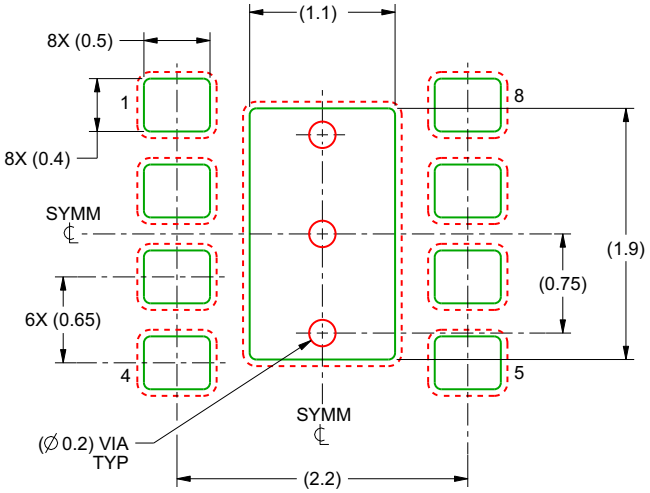
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

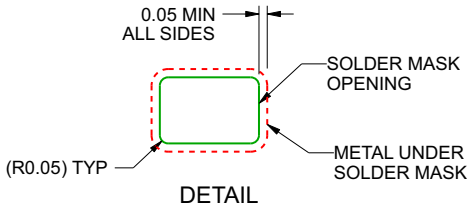
SIL0008C

MicroSiP ™ - 1.33 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

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NOTES: (continued)

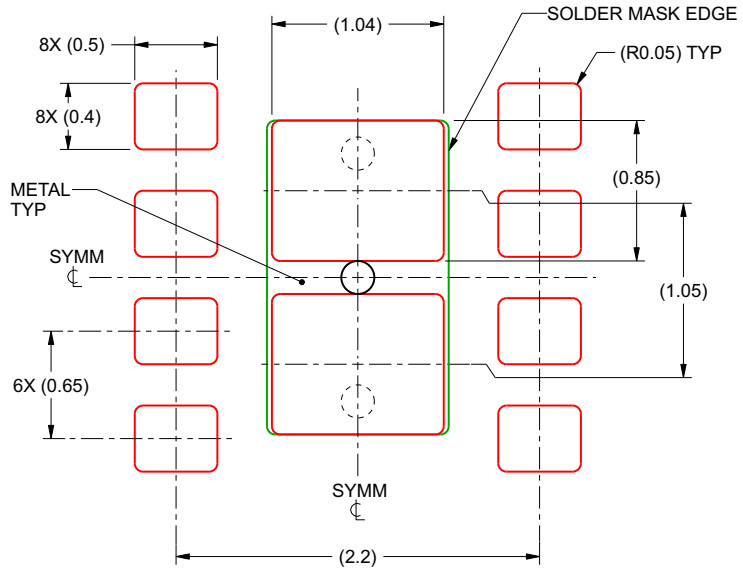
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIL0008C

MicroSiP ™ - 1.33 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS82084SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	1D
TPS82084SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	1D
TPS82084SILR.B	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS82084SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1D
TPS82084SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1D
TPS82084SILT.B	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS82085SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	GE
TPS82085SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	GE
TPS82085SILR.B	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS82085SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	GE
TPS82085SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	GE
TPS82085SILT.B	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265