TPS7H1210-SEP -16.5V、1A、負リニア・レギュレータ、宇宙用強化プラスチック

1 特長

- VID (Vendor Item Drawing) V62/21616 が利用可能
- 総照射線量 (TID) 耐性 = 30krad (Si)
  - すべてのウェハー・ロットについて、20krad(Si) までの TID RLAT (放射線ロット受け入れテスト)
- シングルイベント効果 (SEE) の特性
  - シングルイベント・ラッチアップ (SEL)、シングルイベント・バーンアウト (SEB)、シングルイベント・ゲート・ラプチャー (SEGR) の、線エネルギー付与 (LET) に対する耐性 = 43MeV-cm^2/mg
  - シングルイベント機能割り込み (SEFI) およびシングルイベント過渡 (SET) の LET に対する耐性 = 43MeV-cm^2/mg
- 低ノイズ:13.7μV_{RMS} (標準値、10Hz～100kHz)
- 高い電源除去比、PSRR (V_{IN} = -6V、V_{OUT} = -5V、I_{OUT} = 1A での標準値):
  - 100Hz 時に 61dB
  - 100kHz 時に 61dB
  - 1MHz 時に 41dB
- 入力電圧範囲:-3V～-16.5V
- 調整可能な出力:-1.2V～-15.5V
- 最大 1A の出力電流
- 10μF 以上のセラミック出力コンデンサで安定動作
- 電流制限とサーマル・シャットダウン保護機能を内蔵
- 宇宙向け強化プラスチック (SEP)
  - 管理されたベースライン
  - 金ボンド・ワイヤ
  - NiPdAu リード仕上げ
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 軍用温度範囲:-55℃～125℃
  - 長い製品ライフ・サイクル
  - 製品変更通知期間 (PCN) の延長
  - 製品のトレーサビリティ
  - モールド・コンパウンドの改良による低いガス放出

2 アプリケーション

- 低軌道 (LEO) 衛星用途のサポート
- 衛星用電源システム (EPS)
- アナログ回路の電源
  - データ・コンバータ:ADC と DAC (A/D コンバータと D/A コンバータ)
  - オペアンプ (演算増幅器)
  - イメージング・センサ
- DC-DC コンバータのポスト・レギュレーションおよびリップル・フィルタ処理
- 耐放射線が強化された、制約のある宇宙分野向けの超クリーンなアナログ電源

3 概要

TPS7H1210-SEP 負電圧リニア・レギュレータは、1A の最大負荷を供給できる低ノイズ、高 PSRR のレギュレータです。

このレギュレータには、CMOS ロジックレベル互換のイネーブル・ピン (EN) が搭載されており、ユーザーがカスタマイズ可能なパワー・マネージメント方式を実現できます。その他の機能として、電流制限機能とサーマル・シャットダウン機能が内蔵されており、障害状態時にデバイスとシステムが保護されます。

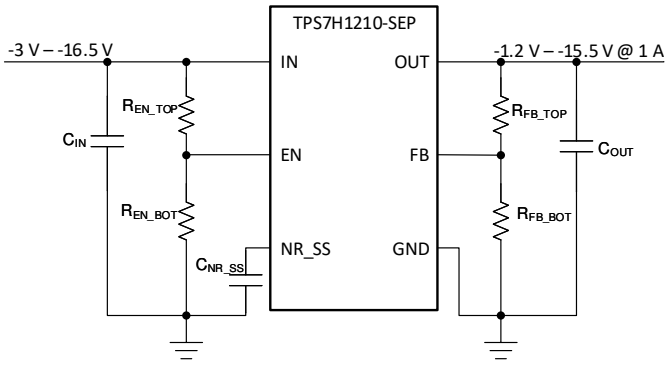
TPS7H1210-SEP デバイスは、システム性能を最大限に高めるためにクリーンな電源レールが決定的に重要な、高精度、低ノイズのアプリケーションを主な対象として、バイポーラ・テクノロジで設計されています。したがって、オペアンプ、ADC、DAC、その他の高性能アナログ回路への電力供給に理想的です。

そのほか、TPS7H1210-SEP デバイスは、DC/DC コンバータのポスト・レギュレーションに適しています。DC/DC スイッチング変換に本質的に付随する出力電圧リップルをフィルタ処理し、影響を受けやすいデバイスや RF アプリケーションにおいて、最大のシステム性能が保証されます。

デバイス情報

部品番号 (1)	グレード	パッケージ (2)
TPS7H1210MRGWSEP	20krad(Si) RLAT、30krad(Si) 特性	VQFN (20) 5.00mm × 5.00mm 質量 = 83.6mg
TPS7H1210EVM	評価ボード	EVM

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) 寸法と質量は公称値です。



代表的なアプリケーション回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2021	*	Initial Release

5 Pin Configuration and Functions

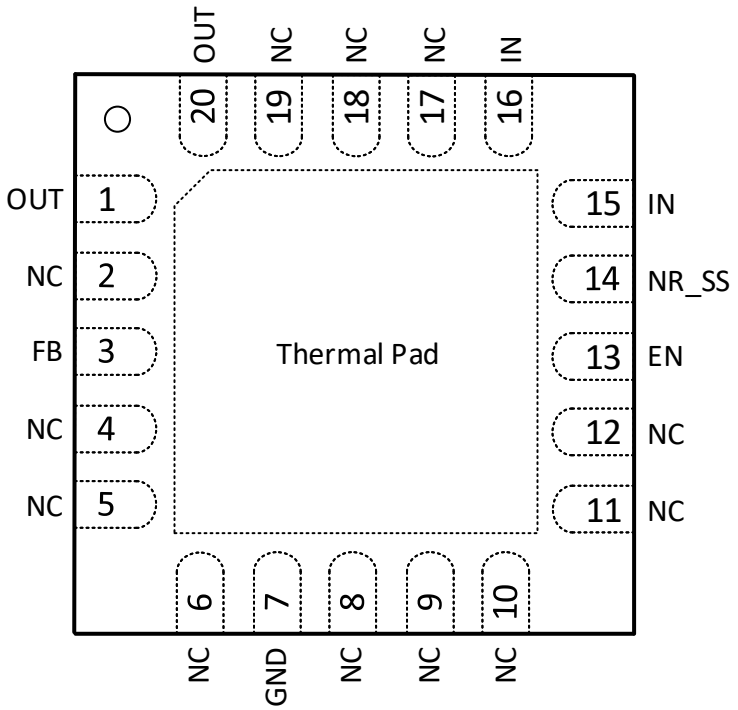


図 5-1. RGW Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	13	I	Enable. This dual-polarity pin turns the regulator on when $\|V_{EN}\| \geq 2$ V. The EN pin can be connected to IN if not used. If V_{EN} is negative polarity, then keep $\|V_{EN}\| \leq \|V_{IN}\|$.
FB	3	I	Feedback. This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device and is normally equal to V_{REF} (–1.182 V, typical) during operation.
GND	7	—	Ground.
IN	15, 16	I	Input supply. It is recommended to connect a 10-µF capacitor from IN to GND (as close to the device as possible).
NC	2, 4–6, 8–12, 17–19	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
NR_SS	14	—	Noise reduction and soft start. A capacitor connected from this pin to GND controls the soft-start function and allows RMS noise to be reduced to very low levels. TI recommends connecting a 100-nF capacitor from NR_SS to GND (as close to the device as possible) to filter the noise generated by the internal band gap and maximize AC performance.
OUT	1, 20	O	Output of the regulator. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to ensure stability. TI recommends connecting a 47-µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize AC performance.
Thermal Pad	—	—	Connect the thermal pad to a large-area ground plane. The thermal pad is not internally grounded and it must be externally tied to GND for proper operation.

(1) I = Input, O = Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN to GND	–35	0.3	V
	FB to GND	–2	0.3	V
	FB to IN	–0.3	35	V
	EN to GND	–35	10	V
	NR_SS to IN	–0.3	35	V
	NR_SS to GND	–2	0.3	V
Output voltage	OUT to GND	–33	0.3	V
	OUT to IN	–0.3	35	V
Output current	Peak output	Internally limited		
Operating virtual junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	IN	–16.5		–3	V
	EN	V_{IN}		10	
Output voltage	OUT(1)	–15.5		V_{REF}	V
Output current	OUT(2)	0		1	A
R_{FB_BOT} (3)	R_{FB_BOT} is the lower feedback resistor			240	kΩ
Input capacitance	C_{IN}	10			µF
Output capacitance	C_{OUT}	10	47		µF
C_{NR_SS}	Noise reduction and soft start capacitor		100		nF
Operating junction temperature	T_J	–55		125	°C

(1) The minimum dropout voltage must also be met.
(2) To ensure stability at no load conditions, a current from the feedback resistive network greater than or equal to 5 µA is required.
(3) This condition helps ensure stability at no load.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H1210-SEP RQW (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
V_{UVLO}	Undervoltage lockout threshold				–2		V
$\|V_{DO}\|$	Dropout voltage	V_{IN} = –4.6 V, $V_{OUT(set)}$ = –5 V, $\|V_{DO}\| = \|V_{IN} - V_{OUT(measured)}\|$, C_{IN} = 30 µF	I_{OUT} = 0.5 A		224	325	mV
			I_{OUT} = 1 A		363	500	
			I_{OUT} = 1 A, T_J = 25°C		363	450	
I_{CL}	Current limit	V_{IN} = –6 V, $V_{OUT(SET)}$ = –5 V, $V_{OUT(forced)}$ = –4.5 V			2.9		A
I_Q	Quiescent current	V_{EN} = 3 V, I_{OUT} = 0 A			210	350	µA
I_{GND}	Ground current(2)	V_{EN} = 3 V, I_{OUT} = 0.5 A			5	10	mA
$\|I_{SHDN}\|$	Shutdown current	V_{EN} = 0.4 V			1	3	µA
		V_{EN} = –0.4 V			1	3	
$I_{FB(LKG)}$	Feedback leakage current(3)				14	75	nA
ACCURACY							
V_{REF}	Reference voltage	$V_{FB} = V_{REF}$		–1.199	–1.182	–1.164	V
V_{ACC}	Output voltage accuracy	$\|V_{IN}\|$ = 3 V, 1 mA ≤ I_{OUT} ≤ 1 A		–2%	±1%	2%	
		$\|V_{IN}\|$ = 16.5 V, 1 mA ≤ I_{OUT} ≤ 100 mA		–2%	±1%	2%	
		$\|V_{IN}\|$ = 16.5 V, $\|V_{OUT}\|$ = 15.5 V, I_{OUT} = 1 A		–2%	±1%	2%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	3 V ≤ $\|V_{IN}\|$ ≤ 16.5 V			–0.007%		V_{OUT}/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	1 mA ≤ I_{OUT} ≤ 1 A			–0.5%		V_{OUT}/A
ENABLE							
$V_{EN(+HI)}$	Enable turn-on (positive logic)			2		10	V
$V_{EN(–HI)}$	Enable turn-on (negative logic)	V_{IN} = –16.5 V		V_{IN}		-2	
$V_{EN(+LO)}$	Enable turn-off (positive logic)			0		0.4	
$V_{EN(–LO)}$	Enable turn-off (negative logic)			–0.4		0	
$\|I_{EN}\|$	Enable current	$V_{IN} = V_{EN}$ = –3 V			0.48	1	µA
		$V_{IN} = V_{EN}$ = –16.5 V			0.51	1	
		V_{IN} = –16.5 V, V_{EN} = 10 V			0.5	1	
$T_{SD(enter)}$	Thermal shutdown enter temperature				178		°C
$T_{SD(exit)}$	Thermal shutdown exit temperature				152		
NOISE AND PSRR							
PSRR	Power-supply rejection ratio	V_{IN} = –6 V, V_{OUT} = –5 V, C_{OUT} = 50.11 µF, I_{OUT} = 1 A, C_{NR_SS} = 100 nF(4)	f = 100 Hz		61		dB
			f = 100 kHz		61		
			f = 1 MHz		41		
V_N	Output noise rms voltage (bandwidth from 10 Hz to 100 kHz)	V_{IN} = –3 V, $V_{OUT(nom)} = V_{REF}$, C_{IN} = 11.1 µF, C_{OUT} = 50.11 µF, C_{NR_SS} = 100 nF, I_{OUT} = 1 A			13.7		μV_{RMS}

(1) At operating conditions, $V_{IN} \le 0$ V, $V_{OUT(nom)} \le V_{REF} \le 0$ V; at regulation, $V_{IN} \le V_{OUT(nom)} - |V_{DO}|$; $I_{OUT} > 0$ flows from OUT to IN.
(2) $I_{GND} = I_{IN} - I_{OUT}$
(3) $I_{FB} > 0$ flows into the device.
(4) C_{IN} is removed as part of PSRR testing. During normal operation, follow the recommended operating condition of $C_{IN} \ge 10$ µF.

6.6 Typical Characteristics

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, T_A = 25°C, unless otherwise noted.

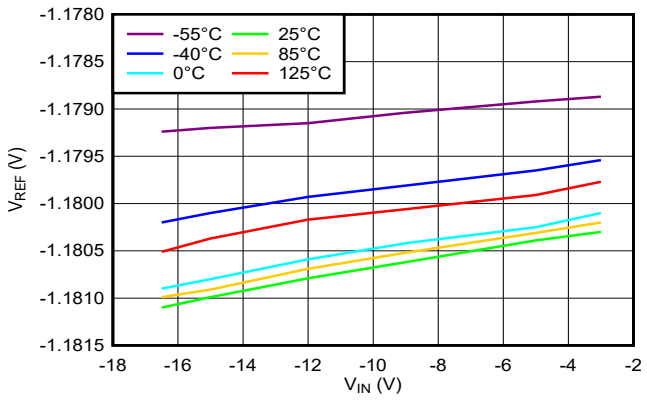
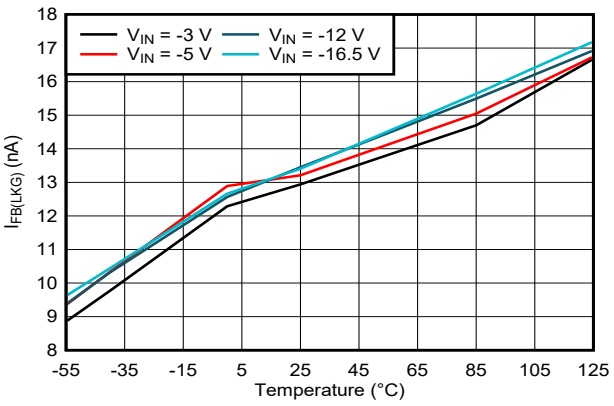


図 6-1. Reference Voltage vs Input Voltage Across Temperature



I_{FB} > 0 flows into the device

図 6-2. Feedback Leakage Current vs Temperature Across Input Voltage

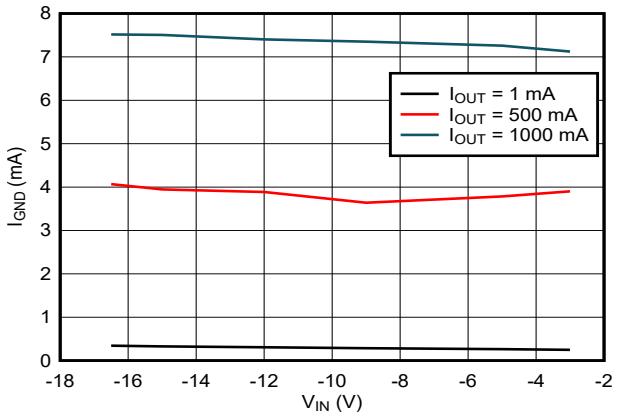
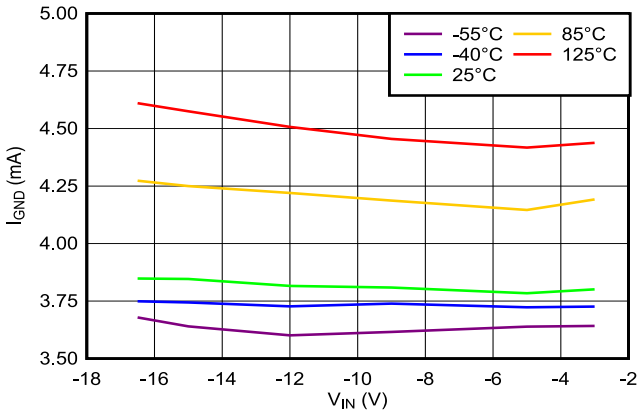


図 6-3. Ground Current vs Input Voltage Across Output Current



I_{OUT} = 500 mA

図 6-4. Ground Current vs Input Voltage Across Temperature

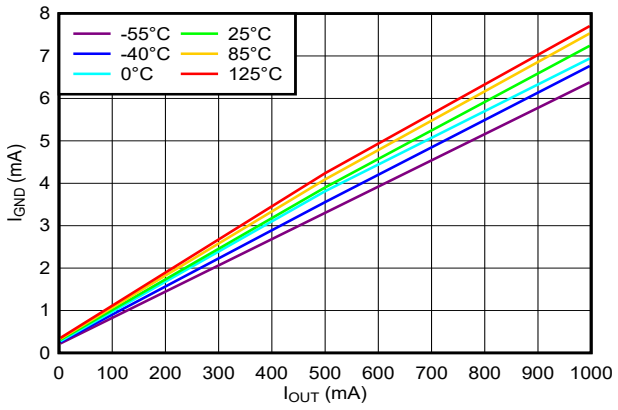


図 6-5. Ground Current vs Output Current Across Temperature

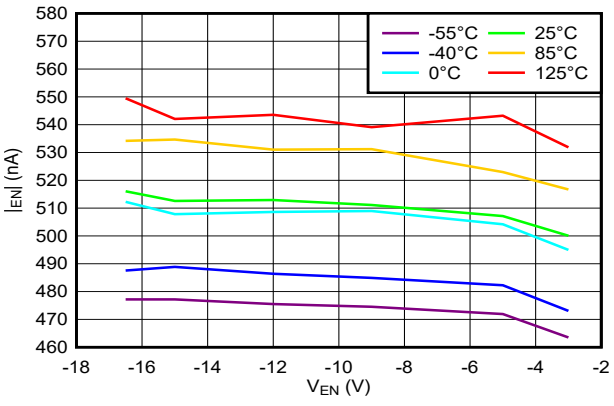
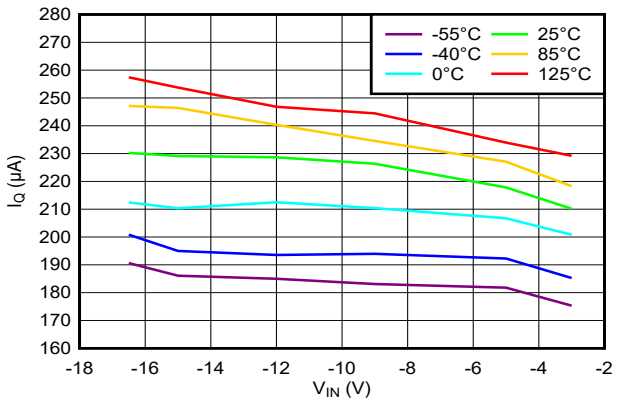


図 6-6. Enable Current vs Enable Voltage Across Temperature

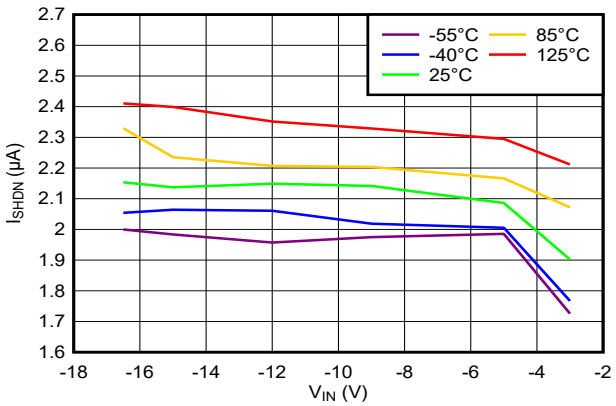
6.6 Typical Characteristics (continued)

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, T_A = 25°C, unless otherwise noted.



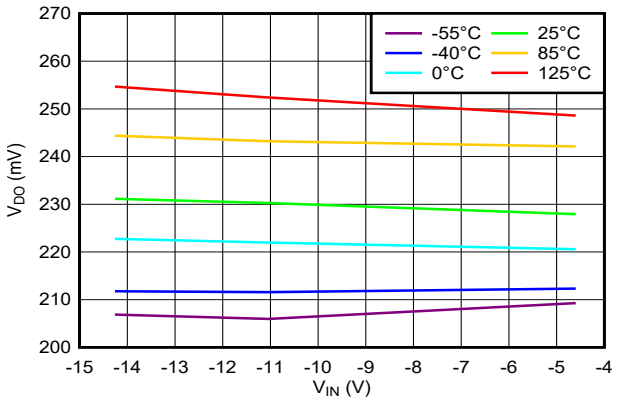
I_{OUT} = 0 mA

図 6-7. Quiescent Current vs Input Voltage Across Temperature



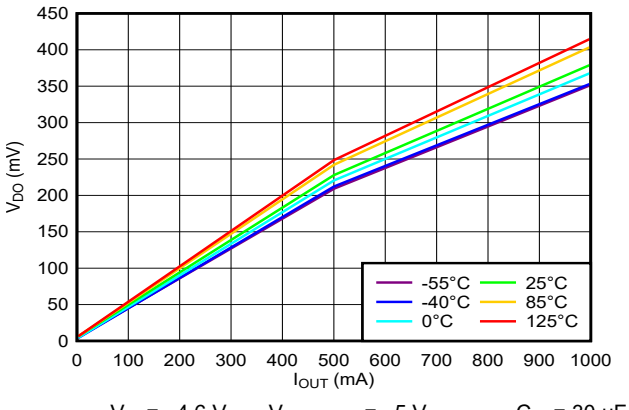
V_{EN} = 0.4 V

図 6-8. Shutdown Current vs Input Voltage Across Temperature



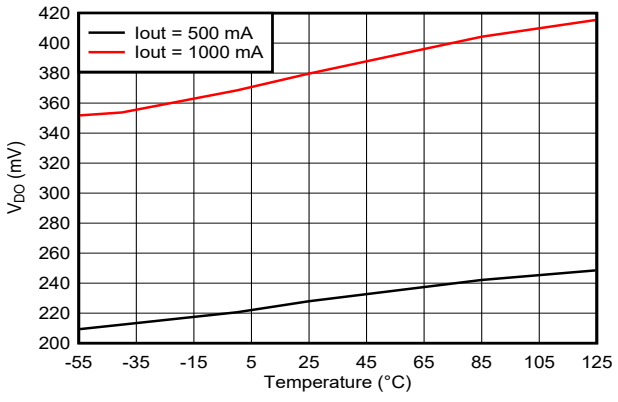
I_{OUT} = 500 mA C_{IN} = 30 µF

図 6-9. Dropout Voltage vs Input Voltage Across Temperature



V_{IN} = –4.6 V $V_{OUT(SET)}$ = –5 V C_{IN} = 30 µF

図 6-10. Dropout Voltage vs Output Current Across Temperature



V_{IN} = –4.6 V $V_{OUT(SET)}$ = –5 V C_{IN} = 30 µF

図 6-11. Dropout Voltage vs Temperature Across Output Current

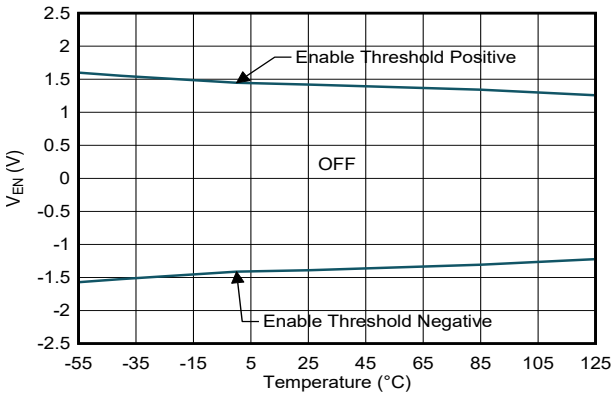
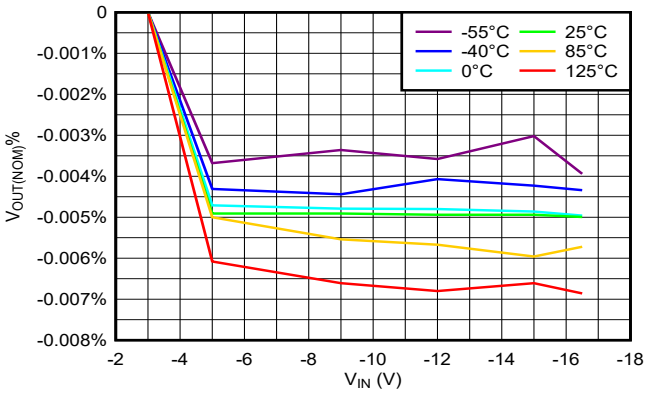


図 6-12. Enable Threshold Voltage vs Temperature

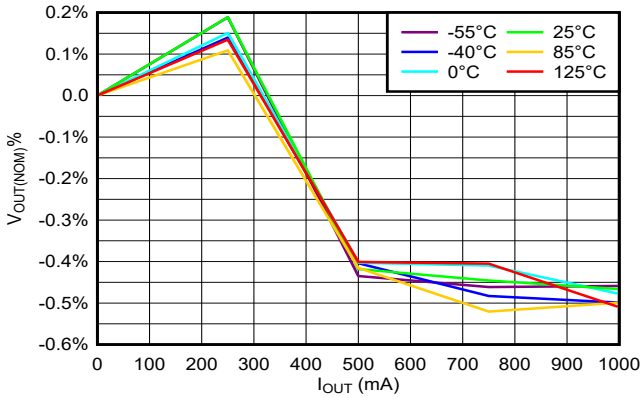
6.6 Typical Characteristics (continued)

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, T_A = 25°C, unless otherwise noted.



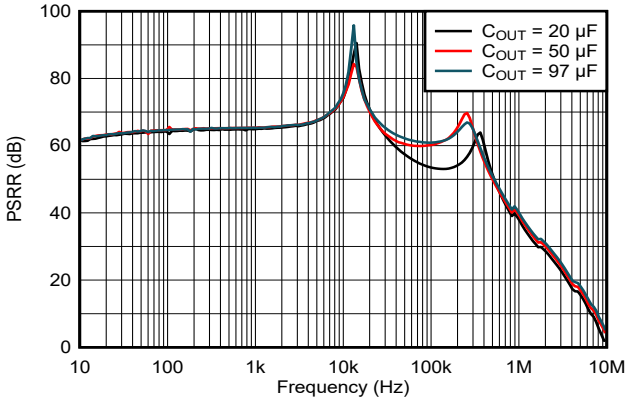
Each individual curve is normalized to 0% at V_{IN} = –3 V

図 6-13. Line Regulation vs Input Voltage Across Temperature



Each individual curve is normalized to 0% at I_{OUT} = 0 mA

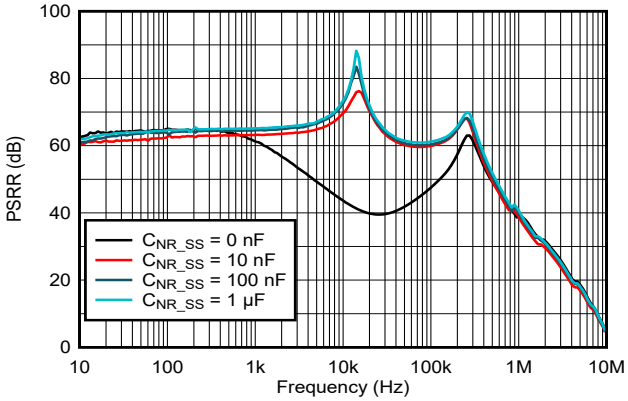
図 6-14. Load Regulation vs Output Current Across Temperature



C_{NR_SS} = 100 nF I_{OUT} = 1 A C_{IN} = 0 µF(A)

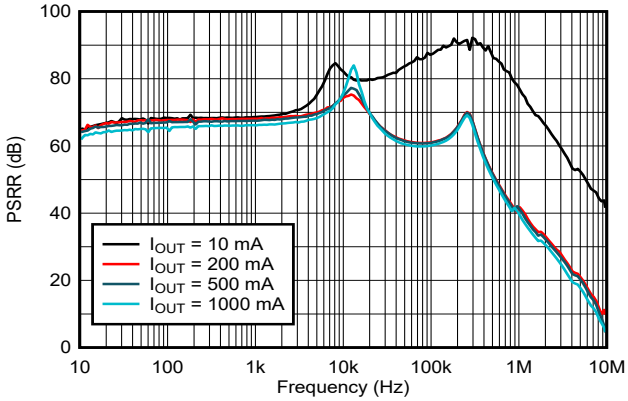
All curves have 100-nF and 10-nF capacitor on V_{OUT}

図 6-15. Power-Supply Rejection Ratio vs Frequency Across C_{OUT}



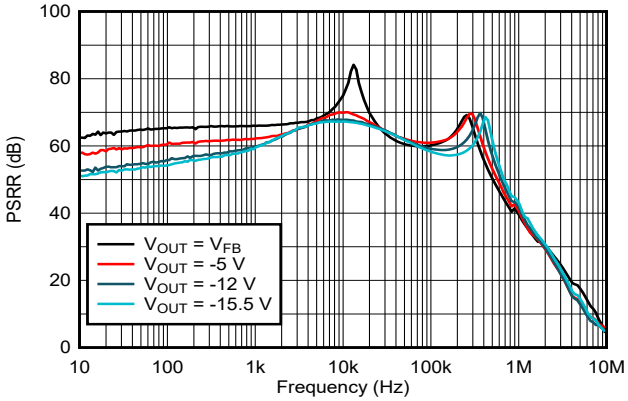
C_{OUT} = 50.11 µF I_{OUT} = 1 A C_{IN} = 0 µF(A)

図 6-16. Power-Supply Rejection Ratio vs Frequency Across C_{NR_SS}



C_{OUT} = 50.11 µF C_{NR_SS} = 100 nF C_{IN} = 0 µF(A)

図 6-17. Power-Supply Rejection Ratio vs Frequency Across Output Current



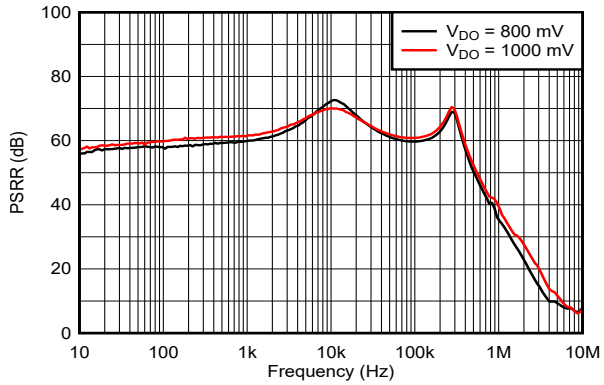
C_{OUT} = 50.11 µF C_{NR_SS} = 100 nF C_{IN} = 0 µF(A)

I_{OUT} = 1 A $|V_{IN}| = |V_{OUT}$ + 1 V|, 3-V minimum

図 6-18. Power-Supply Rejection Ratio vs Frequency Across Output Voltage

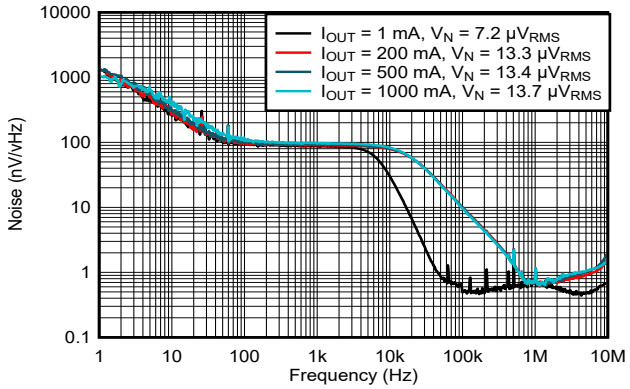
6.6 Typical Characteristics (continued)

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, T_A = 25°C, unless otherwise noted.



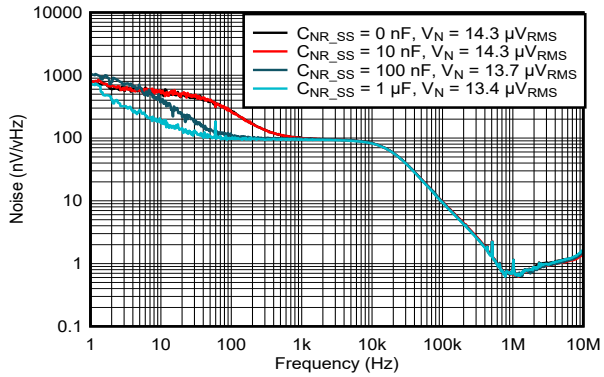
C_{OUT} = 50.11 µF C_{NR_SS} = 100 nF C_{IN} = 0 µF(A)
I_{OUT} = 1 A V_{OUT} = –5 V
$|V_{IN}| = |V_{OUT} + V_{DO}|$, 3-V minimum

図 6-19. Power-Supply Rejection Ratio vs Frequency Across Dropout Voltage



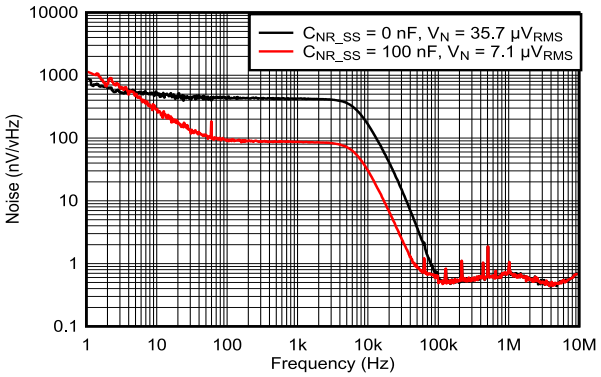
C_{OUT} = 50.11 µF C_{NR_SS} = 100 nF C_{IN} = 11.1 µF
V_N = output noise RMS voltage (10-Hz to 100-kHz bandwidth)

図 6-20. Output Noise vs Frequency Across Output Current (Noise Spectral Density)



C_{OUT} = 50.11 µF I_{OUT} = 1 A C_{IN} = 11.1 µF
V_N = output noise RMS voltage (10-Hz to 100-kHz bandwidth)

図 6-21. Output Noise vs Frequency Across C_{NR_SS} (Noise Spectral Density)

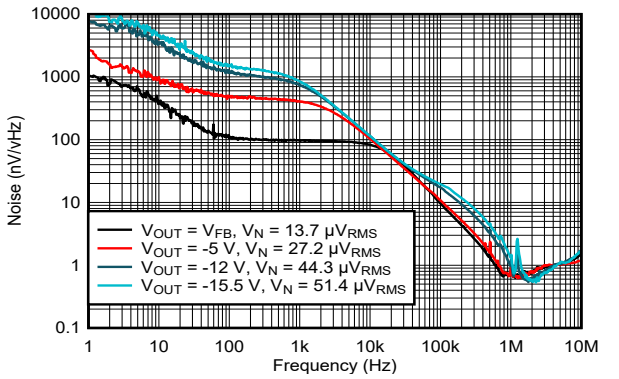


C_{OUT} = 50.11 µF I_{OUT} = 1 mA C_{IN} = 11.1 µF
V_N = output noise RMS voltage (10-Hz to 100-kHz bandwidth)

図 6-22. Output Noise vs Frequency Across C_{NR_SS} (Noise Spectral Density)

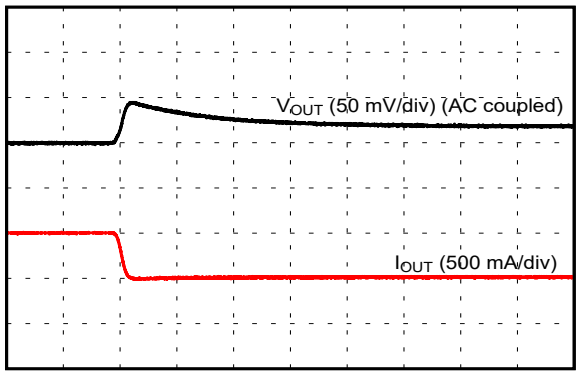
6.6 Typical Characteristics (continued)

Over $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN, T_A = 25°C, unless otherwise noted.



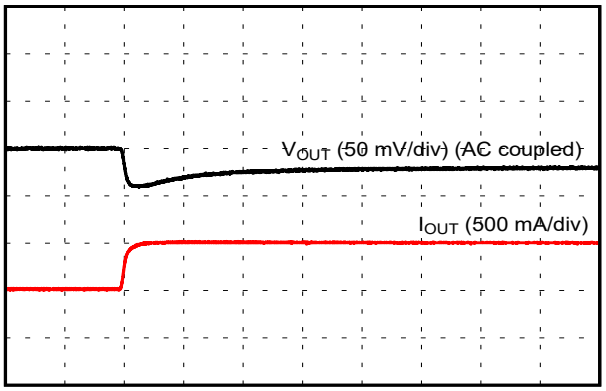
C_{OUT} = 50.11 µF I_{OUT} = 1 A C_{IN} = 11.1 µF
$|V_{IN}| = |V_{OUT} + V_{DO}|$, 3-V minimum
V_N = output noise RMS voltage (10-Hz to 100-kHz bandwidth)

図 6-23. Output Noise vs Frequency Across Output Voltage (Noise Spectral Density)



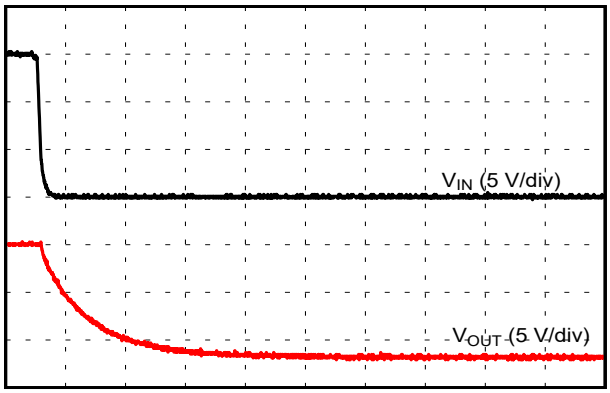
Time (100 µs/div)
V_{IN} = –15 V V_{OUT} = –12 V $I_{OUT\ (slew)}$ = 1 A / 10 µs
C_{IN} = 11.1 µF C_{OUT} = 50 µF C_{NR_SS} = 100 nF

図 6-24. Load Step: 1 mA to 500 mA



Time (100 µs/div)
V_{IN} = –15 V V_{OUT} = –12 V $I_{OUT\ (slew)}$ = 1 A / 10 µs
C_{IN} = 11.1 µF C_{OUT} = 50 µF C_{NR_SS} = 100 nF

図 6-25. Load Step: 500 mA to 1 mA



Time (50 ms/div)
$V_{IN(SET)}$ = –15 V $V_{OUT(SET)}$ = –12 V C_{IN} = 11.1 µF
C_{OUT} = 50 µF C_{NR_SS} = 100 nF

図 6-26. Start-up with Soft-Start

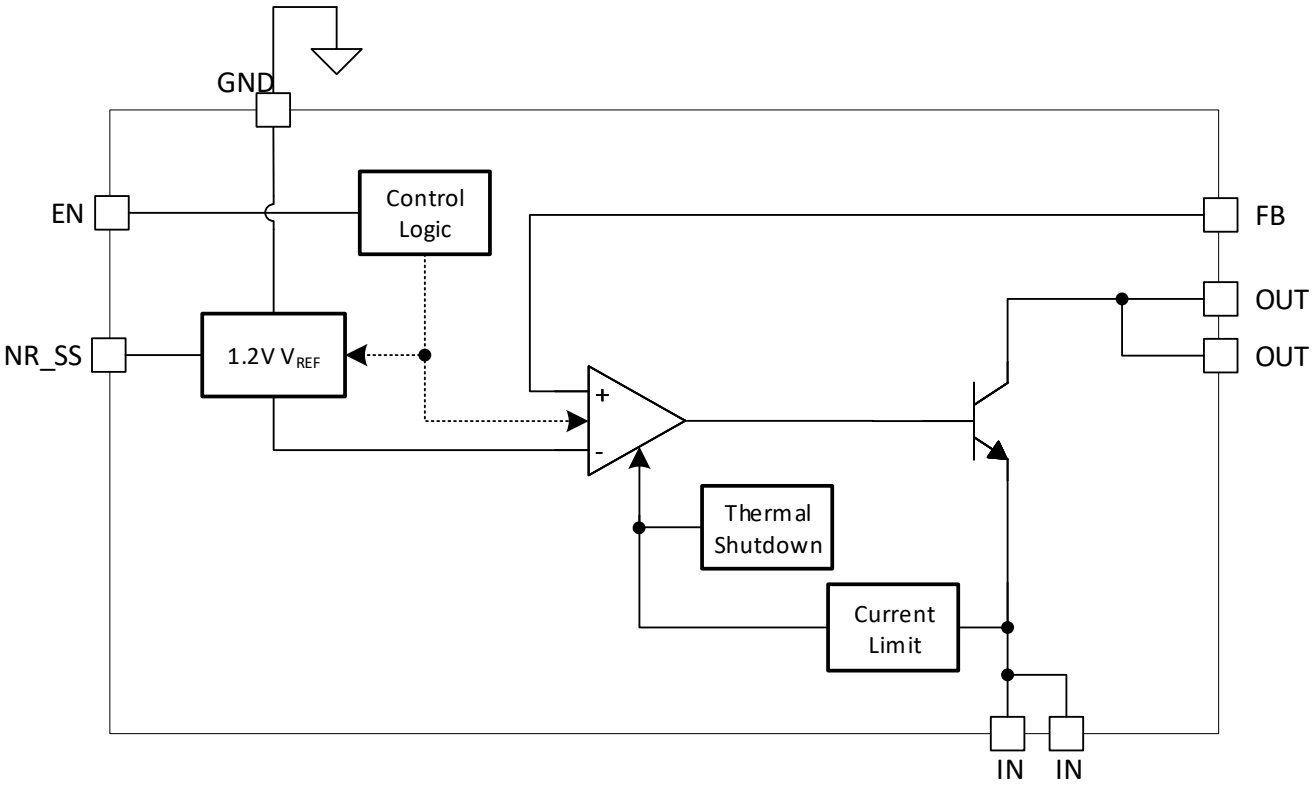
A. C_{IN} is removed as part of PSRR testing. During normal operation, follow the recommended operating condition of C_{IN} ≥ 10 µF.

7 Detailed Description

7.1 Overview

The TPS7H1210-SEP negative voltage linear regulator uses a bipolar process to achieve very low noise and very high PSRR levels at a wide input voltage and current range. These features, plus its radiation tolerance, make this device ideal for high-performance analog applications in satellites.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The fixed internal current limit of the TPS7H1210-SEP device helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (2.9 A, typical), and it is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

7.3.2 Enable Pin Operation

The TPS7H1210-SEP provides a dual-polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2$ V, whether the voltage is positive or negative, as shown in 図 7-1. Specifically, if $V_{EN} \geq V_{EN(+HI)}$ or $V_{EN} \leq V_{EN(-HI)}$, the regulator is enabled. If $V_{EN(+LO)} \geq V_{EN} \geq V_{EN(-LO)}$, the regulator is disabled.

This functionality allows for different system power management topologies; for example:

- Connecting the EN pin directly to a negative voltage, such as V_{IN}.
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.
- Connecting the EN pin to a resistor divider from V_{IN} to GND to turn-on at a specific input voltage level (programmable turn-on voltage).

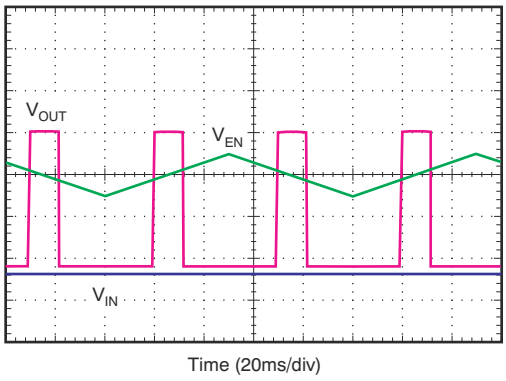


図 7-1. Enable Pin Positive and Negative Threshold

7.3.3 Programmable Soft-Start

The NR_SS capacitor acts as a noise reduction capacitor and a soft-start capacitor to slow down the rise time of the output. The output rise time, when using an NR_SS capacitor, is approximated by 式 1.

$$t_{SS}\ (\text{ms}) = 1.2 \times C_{NR\_SS}\ (\text{nF}) \quad (1)$$

In 式 1, t_{SS} is the soft-start time in milliseconds and C_{NR_SS} is the capacitance at the NR_SS pin in nanofarads.

図 7-2 shows the start-up voltage waveforms versus C_{NR_SS}.

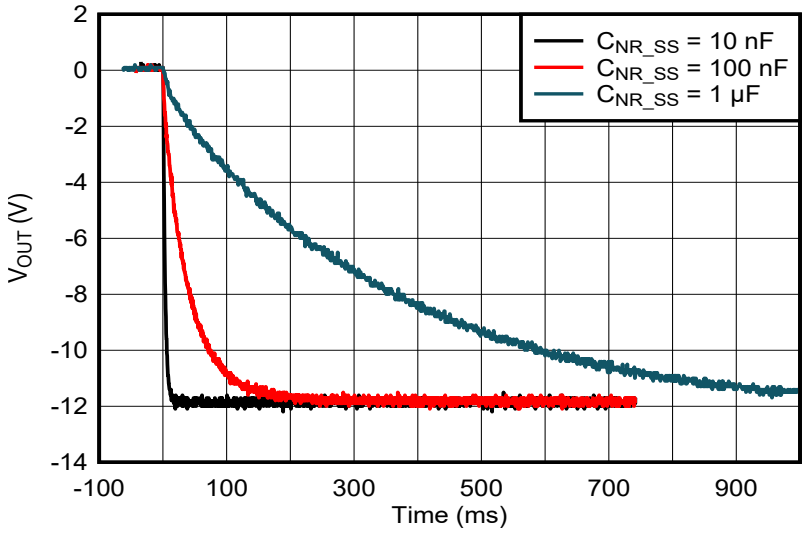


図 7-2. Start-Up Waveforms vs C_{NR_SS}

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 178°C, allowing the device to cool. When the junction temperature cools to approximately 152°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, mitigating damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit the junction temperature to a maximum of 125°C.

The internal protection circuitry of the TPS7H1210-SEP has been designed to protect against overload conditions. It was not intended to replace proper thermal management. Continuously running the TPS7H1210-SEP into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under all of the following conditions:

- The input voltage magnitude has previously exceeded the UVLO rising voltage magnitude and has not decreased below the UVLO falling threshold magnitude.
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage magnitude.
- $|V_{EN}| > |V_{(HI)}|$
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified recommended operating conditions junction temperature.

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the magnitude of the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under any of the following conditions:

- $|V_{EN}| < |V_{(HI)}|$
- The device junction temperature is greater than the thermal shutdown temperature.

表 7-1 shows the conditions that lead to the different modes of operation.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$\|V_{IN}\| > \{ \|V_{OUT(nom)}\| + \|V_{DO}\|, \|V_{IN(min)}\| \}$	$\|V_{EN}\| > \|V_{(HI)}\|$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$\|V_{IN(min)}\| < \|V_{IN}\| < \|V_{OUT(nom)}\| + \|V_{DO}\|$	$\|V_{EN}\| > \|V_{(HI)}\|$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$\|V_{IN}\| \le \|V_{UVLO}\|$	$\|V_{EN}\| < \|V_{(HI)}\|$	—	$T_J > ~178°C$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Operation

The TPS7H1210-SEP has an output voltage range of V_{REF} to –15.5 V. The nominal output voltage of the device is set by two external resistors, as shown in 図 8-2.

R_{FB_TOP} and R_{FB_BOT} can be calculated for any output voltage range using 式 2. To ensure stability under no-load conditions at $|V_{OUT}| > |V_{REF}|$, this resistive network must provide a current equal to or greater than 5 µA.

$$R_{FB\_TOP} = R_{FB\_BOT} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right), \text{ where } \frac{|V_{REF}|}{R_{FB\_BOT}} > 5\ \mu A \quad (2)$$

表 8-1 shows the resistor combinations to achieve a few of the most common rails using commercially available, 1%-tolerance resistors. If greater voltage accuracy is required, consider the output voltage offset contributions because of the feedback pin current and use 0.1%-tolerance resistors.

表 8-1. Example 1% Tolerance Resistors for Common Voltage Rails

V_{OUT} (V)	R_{FB_TOP} (kΩ)	R_{FB_BOT} (kΩ)	RESISTOR NETWORK BIAS CURRENT (µA)	RESISTOR ERROR CONTRIBUTION(1)
–1.182	0	∞	N/A	N/A
–1.8	7.32	14	84.4	+0.001%
–2.5	11.3	10.2	115.9	+0.341%
–3.3	19.1	10.7	110.5	–0.245%
–5	34	10.5	112.6	–0.189%
–9	115	17.4	67.9	+0.066%
–10	445	15.4	76.8	–0.086%
–12	137	15	78.8	+0.187%
–15	133	11.3	104.6	–0.627%

(1) This is the error contribution due to the mismatch between the ideal resistor ratio and the actual resistor ratio (using the indicated resistor values). It does not include the error contribution due to the resistor tolerance itself. More accurate ratios are possible by using 0.1% tolerance resistors.

8.1.2 Capacitor Recommendations

It is recommended to use low equivalent series resistance (ESR) capacitors for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with an X7R dielectric is preferred. This dielectric offers stable characteristics over temperature.

注

High-ESR capacitors may degrade PSRR and affect stability.

The TPS7H1210-SEP negative linear regulator achieves stability with a minimum input and output capacitance of 10 µF. TI recommends using a 10-µF capacitor at the input. A larger capacitor is recommended at the output. Specifically, TI recommends using a 47-µF capacitor (or multiple capacitors to reach ~47 µF) at the output to improve single event transient (SET) performance.

8.1.3 Noise Reduction and Feed-Forward Capacitor Requirements

Although the noise-reduction (C_{NR_SS}) capacitor is not needed to achieve stability, TI highly recommends using a 100-nF noise-reduction capacitor to minimize noise and maximize AC performance. The noise-reduction capacitor is especially important at low currents as shown in 図 6-22.

It is generally recommended to not use a feed-forward capacitor. While a feed-forward capacitor can provide some improvements in PSRR at certain frequencies, it also has additional risks. See *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* for additional information.

注意

Using a feed-forward capacitor with the TPS7H1210-SEP can cause the FB pin to go too positive during shutdown, thus damaging the device.

図 8-1 shows the different PSRR performance of the device with and without a feed-forward capacitor with V_{IN} = –13 V, V_{OUT} = –12 V, I_{OUT} = 1 A, C_{NR_SS} = 100 nF, and C_{OUT} = 50 µF.

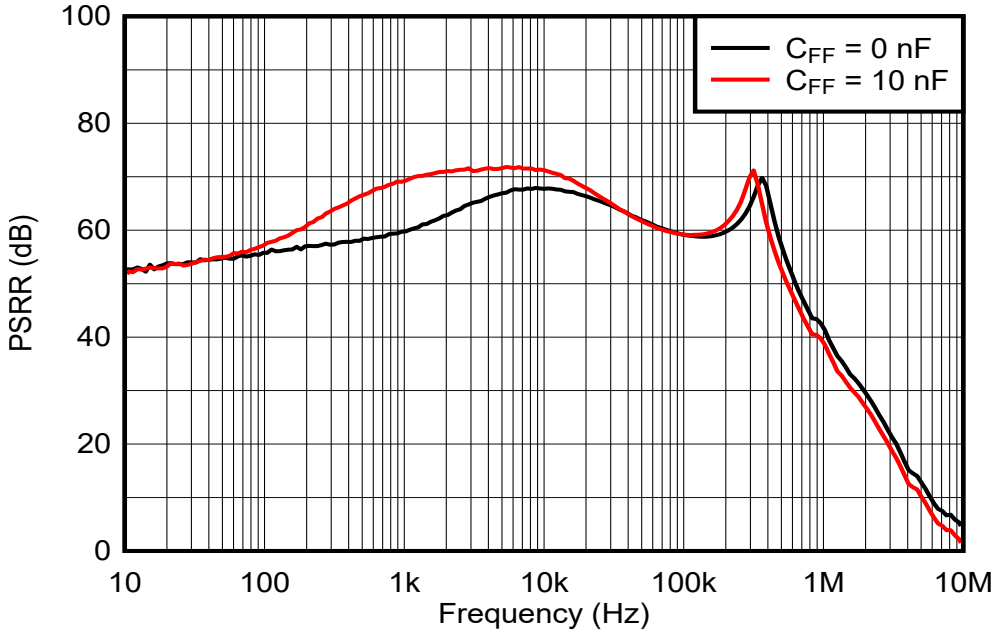


図 8-1. Power-Supply Rejection Ratio vs Frequency Across C_{FF}

8.1.4 Power-Supply Rejection Ratio (PSRR)

Using a noise-reduction capacitor (C_{NR_SS}) of at least 10-nF greatly improves TPS7H1210-SEP power-supply rejection ratio. If the C_{NR_SS} capacitor is omitted, the PSRR can be 10 dB lower or worse across a wide range of frequencies. A 100-nF capacitor is generally recommended.

Additionally, TI recommends using at least a 47-µF output capacitor for both single event transient (SET) and to achieve great AC performance. A 10-µF input capacitor is generally sufficient for good device performance; however, a 47-µF input capacitor or larger may be ideal if the input rail is extremely noisy.

The high power-supply rejection of the TPS7H1210-SEP makes it a good choice for powering high-performance analog circuitry.

8.1.5 Output Noise

The TPS7H1210-SEP provides low output noise when a noise-reduction capacitor (C_{NR_SS}) is used.

The noise-reduction capacitor serves as a filter for the internal reference. By using at a 100-nF noise reduction capacitor (C_{NR_SS}), the output noise can be reduced by approximately 80% (from 35.7 μV_{RMS} to 7.1 μV_{RMS}). See 図 6-22 for additional information. The benefit is less pronounced at higher currents (see 図 6-21).

The TPS7H1210-SEP low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

8.1.6 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.1.7 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are generally the preferred solution to stepping up or down a voltage rail when current consumption is not negligible. These devices offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the DC output signal.

If not filtered properly, this high-frequency component degrades analog circuitry performance, and reduces overall system accuracy and precision.

The TPS7H1210-SEP offers a wide-bandwidth, very-high power-supply rejection ratio (PSRR). This specification makes it ideal for post DC-DC converter filtering. TI recommends using a schematic like the one shown in 図 8-2 for high performance. Also, verify that the TPS7H1210-SEP regulator PSRR is still high within the fundamental frequency (and its first harmonic, if possible) of the switching regulator.

8.1.8 Power for Precision Analog

One of the primary TPS7H1210-SEP applications is to provide very low noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision. This includes powering operational amplifiers, ADCs, DACs, and RF amplifiers.

Because of the low noise levels at high voltages, the TPS7H1210-SP can directly power high performance analog circuitry with high-voltage input supply requriements.

8.2 Typical Application

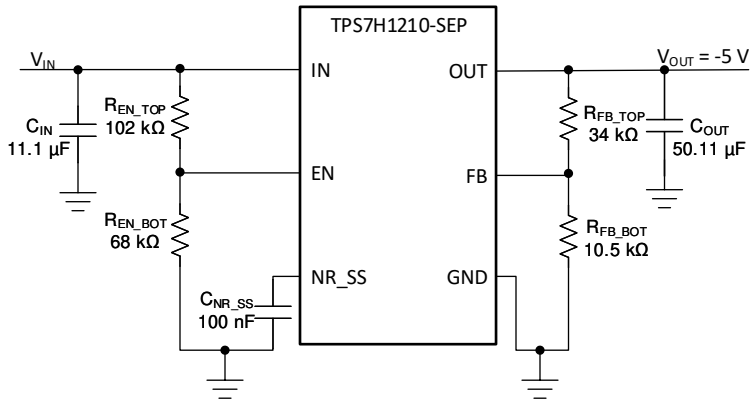


図 8-2. Adjustable Operation for Optimized AC and Radiation Performance

8.2.1 Design Requirements

The design goals for this example are V_{IN} = –6 V, V_{OUT} = –5 V, and I_{OUT} = 1-A maximum. The design must optimize transient response, and the input supply comes from a supply on the same printed-circuit board (PCB).

8.2.2 Detailed Design Procedure

The design consists of C_{IN}, C_{OUT}, C_{NR_SS}, R_{FB_TOP}, R_{FB_BOT}, R_{EN_TOP}, R_{EN_BOT}, and the circuit shown in 図 8-2.

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements can be met. At 1 A, the input dropout voltage of the TPS7H1210-SEP device is a maximum of 500 mV over temperature; thus, the dropout headroom is sufficient for operation over both input and output voltage accuracy. Keep in mind that operating an LDO close to the dropout limit reduces AC performance, but has the benefit of reducing the power dissipation across the LDO.

The maximum power dissipated in the linear regulator is the maximum voltage drop across the pass element from the input to the output multiplied by the maximum load current (plus a small amount of quiescent power). In this example, the maximum voltage drop across in the pass element is (–6 V) – (–5 V), giving us a V_{DROP} = 1 V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is approximately 1 W.

To ensure an accurate output voltage, R_{FB_TOP} and R_{FB_BOT} must also be found, and the current through these resistors must be greater than 5 µA to ensure stability. For this design, R_{FB_TOP} is set to 34 kΩ, to achieve reasonable leakage current leakage while continuing to hold it well above 5 µA. Then 式 3 is used to calculate the proper value for R_{FB_BOT}.

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times V_{REF}}{V_{OUT} - V_{REF}} = 10.5\ k\Omega \text{ and } I_{DIVIDER} = \frac{|V_{REF}|}{R_{FB\_BOT}} = 112.6\ \mu A \quad (3)$$

Next, for C_{IN} a 10 µF, 1 µF, and 0.1-µF ceramic capacitor are selected. This provides margin over the 10-µF minimum input capacitance and reduces the impedance across a wider range of frequencies than a single 10-µF capacitor.

For C_{OUT}, 5 × 10-µF, 1 × 100-nF, and 1 × 10-nF ceramic capacitors are selected. The multiple ceramic capacitors reduce ESR (equivalent series resistance) and ESL (equivalent series inductance) to aid in good AC performance. Additionally, better SET (single-event-transient) performance is generally achieved by choosing a larger output capacitance than the minimum of 10 µF.

Next, C_{NR_SS} is set at 100 nF for optimal noise performance along with maximized AC performance while keeping reasonable soft-start times.

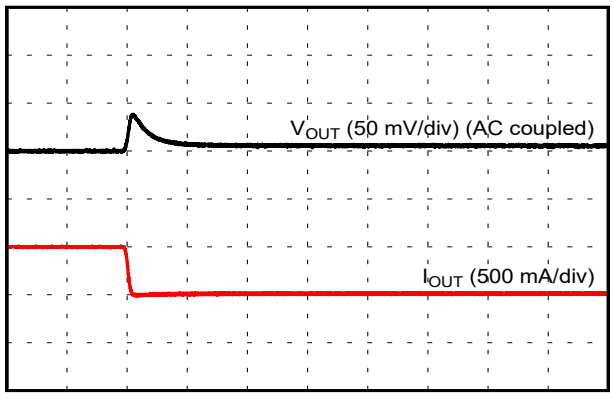
To have a configurable turn-on voltage, feed the EN pin by a resistor divider from V_{IN} to GND. Since the TPS7H1210-SEP is commanded to turn-on when EN is less than –2 V (see $V_{EN(-HI)}$ in セクション 6.5), 式 4 can be used to determine the resistors to select for a desired turn-on voltage, $V_{IN(turn-on)}$.

$$R_{EN\_BOT} = \frac{R_{EN\_TOP} \times 2\ V}{V_{IN(turn-on)} - 2\ V} \quad (4)$$

For this design R_{EN_TOP} = 102 kΩ and R_{EN_BOT} = 68 kΩ, which results in $V_{IN(turn-on)}$ = –5 V. This means that as V_{IN} is ramping from 0 V to its final value of –6 V during start-up, the regulator will turn-on when V_{IN} reaches –5 V.

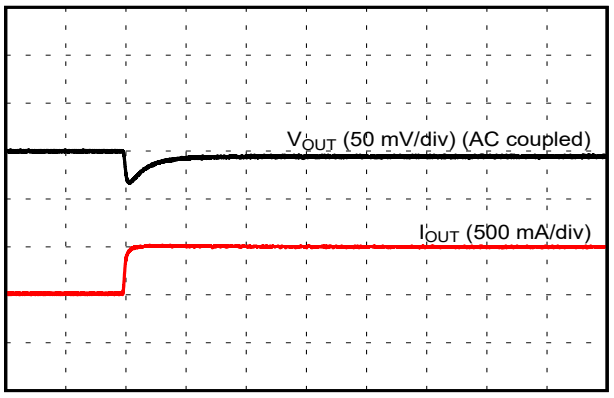
8.2.3 Application Curves

図 8-3 and 図 8-4 show a 1-mA to 500-mA load step and 500-mA to 1-mA load step respectively using the values described within this section.



V_{IN} = –6 V　V_{OUT} = –5 V　$I_{OUT\ (slew)}$ = 1 A / 10 µs
C_{IN} = 11.1 µF　C_{OUT} = 50.11 µF　C_{NR_SS} = 100 nF

図 8-3. Load Step: 1 mA to 500 mA



V_{IN} = –6 V　V_{OUT} = –5 V　$I_{OUT\ (slew)}$ = 1 A / 10 µs
C_{IN} = 11.1 µF　C_{OUT} = 50.11 µF　C_{NR_SS} = 100 nF

図 8-4. Load Step: 500 mA to 1 mA

8.3 Do's and Don'ts

Place at least one low ESR 10-µF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the EN pin.

Do not resistively or inductively load the NR_SS pin.

9 Power Supply Recommendations

The input supply for the LDO must be within its recommended operating conditions, of –16.5 V to –3 V. The input voltage must provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

Layout is a critical part of good power-supply design. Several signal paths that conduct fast-changing currents or voltages can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low ESR ceramic bypass capacitor with an X7R dielectric.

10.1 Layout Guidelines

10.1.1 Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate planes for IN, OUT, and GND. The IN and OUT planes should be isolated from each other by a GND plane section. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{NR_SS}, and C_{FF} if used) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

10.2 Layout Example

It may be possible to obtain acceptable performance with alternative PCB layouts.

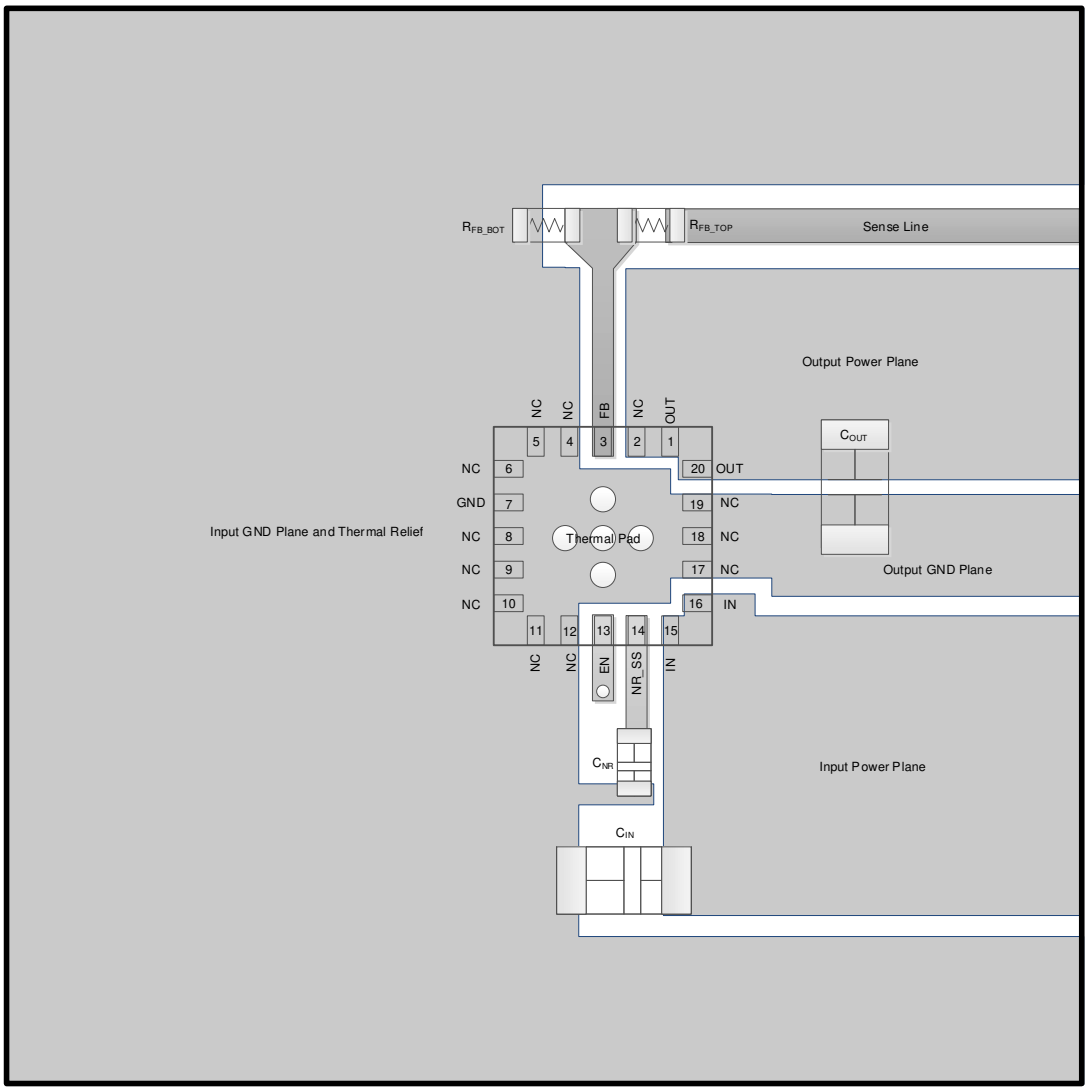


図 10-1. TPS7H1210-SEP Layout Guideline

10.3 Thermal Performance

The high-current and high-voltage characteristics of the TPS7H1210-SEP means that, often enough, high power (heat) is dissipated from the device itself. This heat, if dissipated into the PCB, creates a temperature gradient in the surrounding area that causes nearby components to react to this temperature change (drift). In high-performance systems, such drift may degrade overall system accuracy and precision.

The heat generated by the device is a result of the power dissipation, which depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by calculating the product of the output current times the voltage drop across the output pass element, as shown in 式 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Be sure the PCB is able to effectively dissipate the heat resulting from the power dissipation.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A PSpice model for the TPS7H1210-SEP is available through the product folder under the *Design & Development* section.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instrument, *TPS7H1210-SEP Total Ionizing Dose (TID)* radiation report
- Texas Instrument, *TPS7H1210-SEP Single-Event Effects (SEE)* radiation report
- Texas Instrument, *TPS7H1210-SEP Evaluation Module (EVM)* user's guide
- Texas Instrument, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report
- Vendor item drawing available, VID V62/21616

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.5 Trademarks

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11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7H1210MRGWSEP	Active	Production	VQFN (RGW) | 20	70 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H1210
TPS7H1210MRGWTSEP	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H1210
V62/21616-01XE	Active	Production	VQFN (RGW) | 20	70 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H1210MRGWSEP	7H1210
V62/21616-01XE-T	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H1210MRGWTSEP	7H1210

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

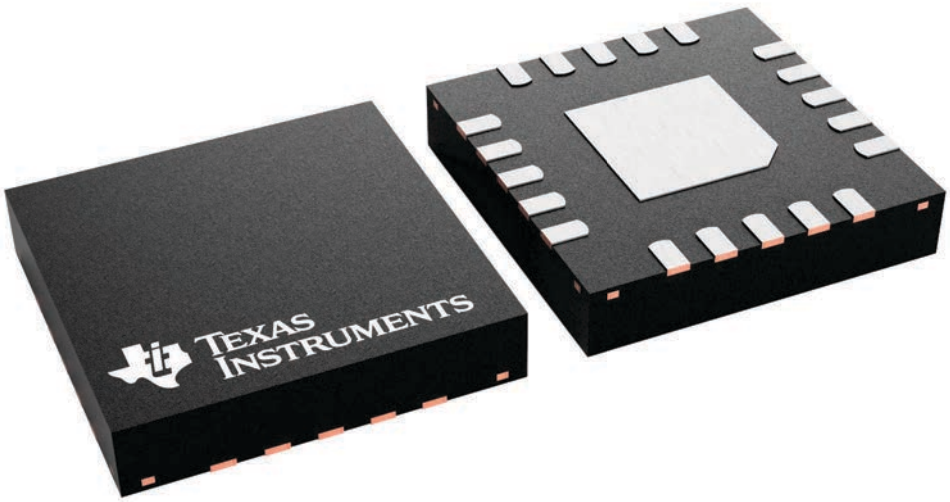
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



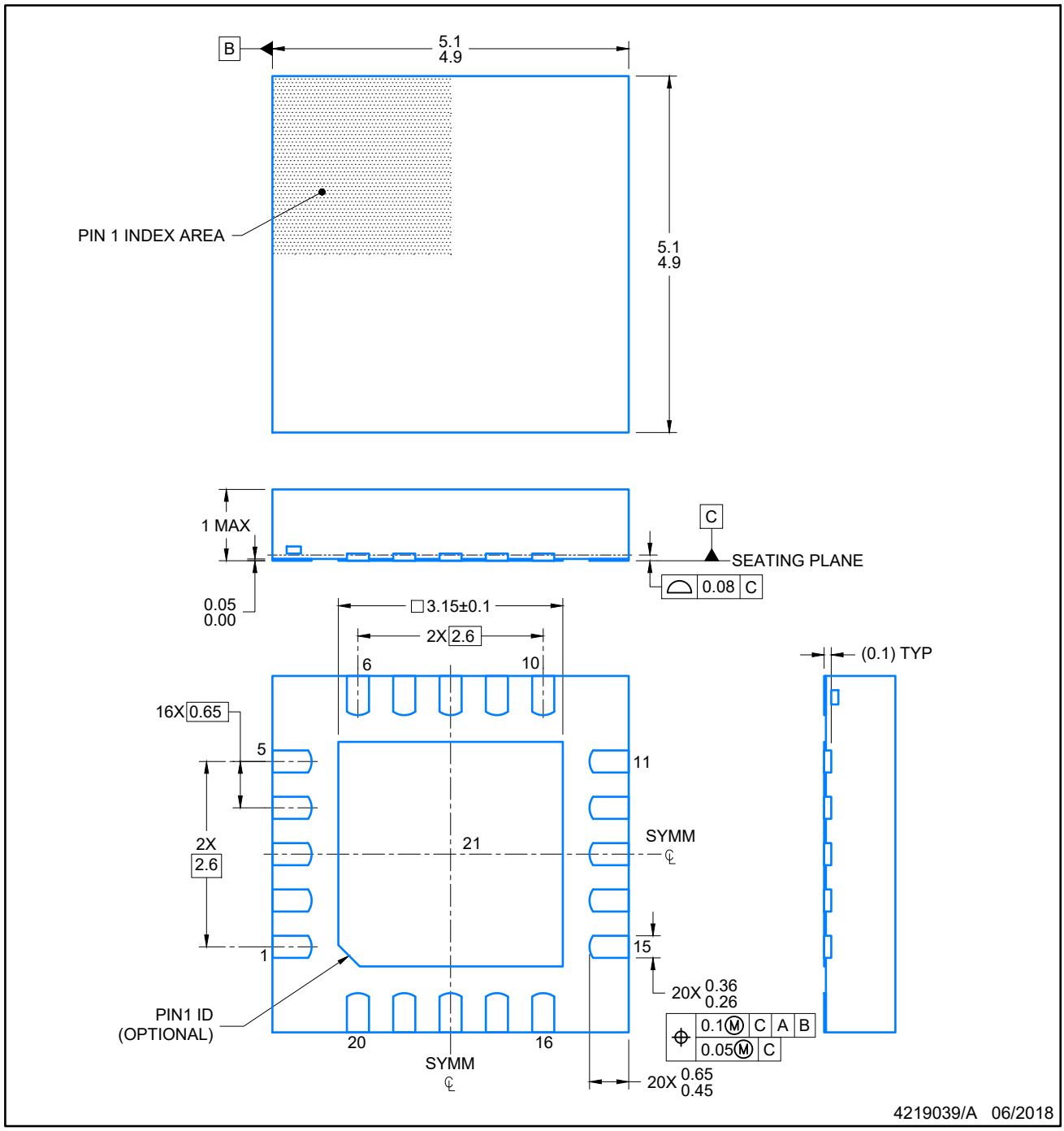
4227157/A

PACKAGE OUTLINE

RGW0020A

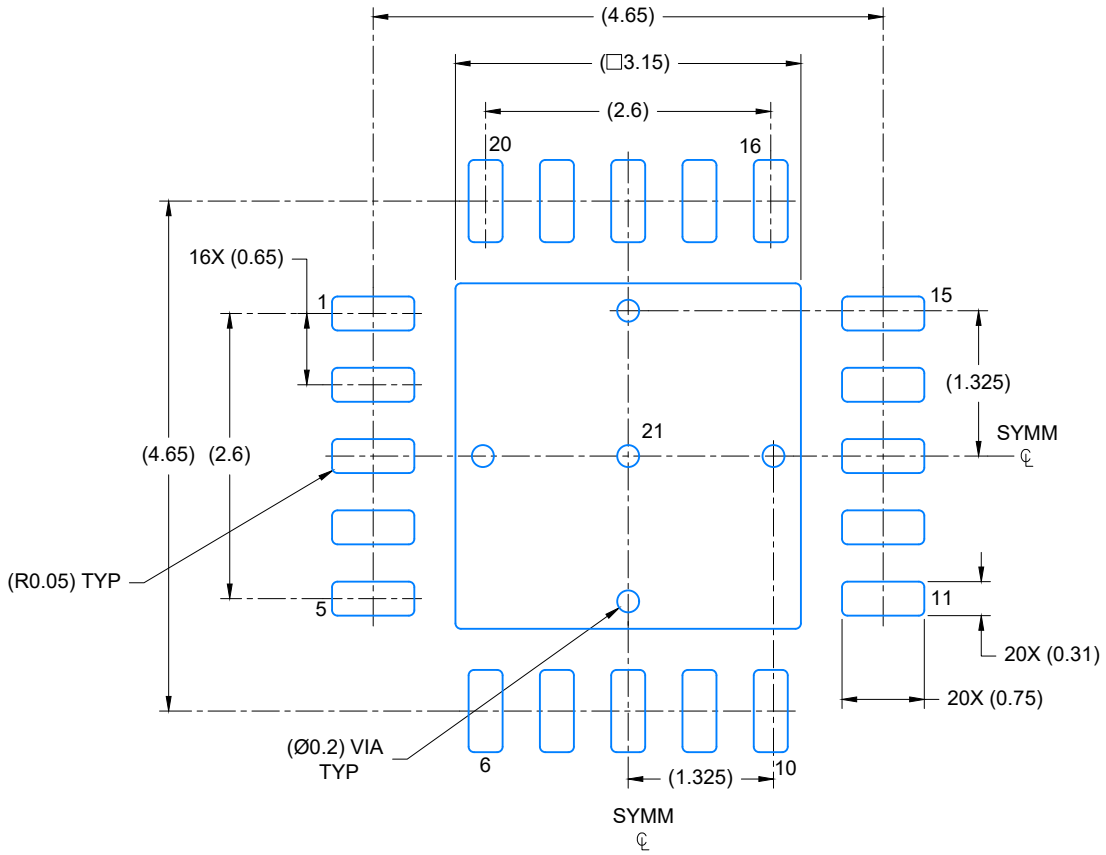
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



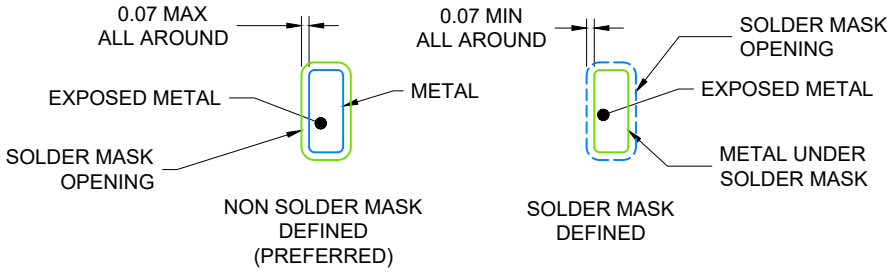
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

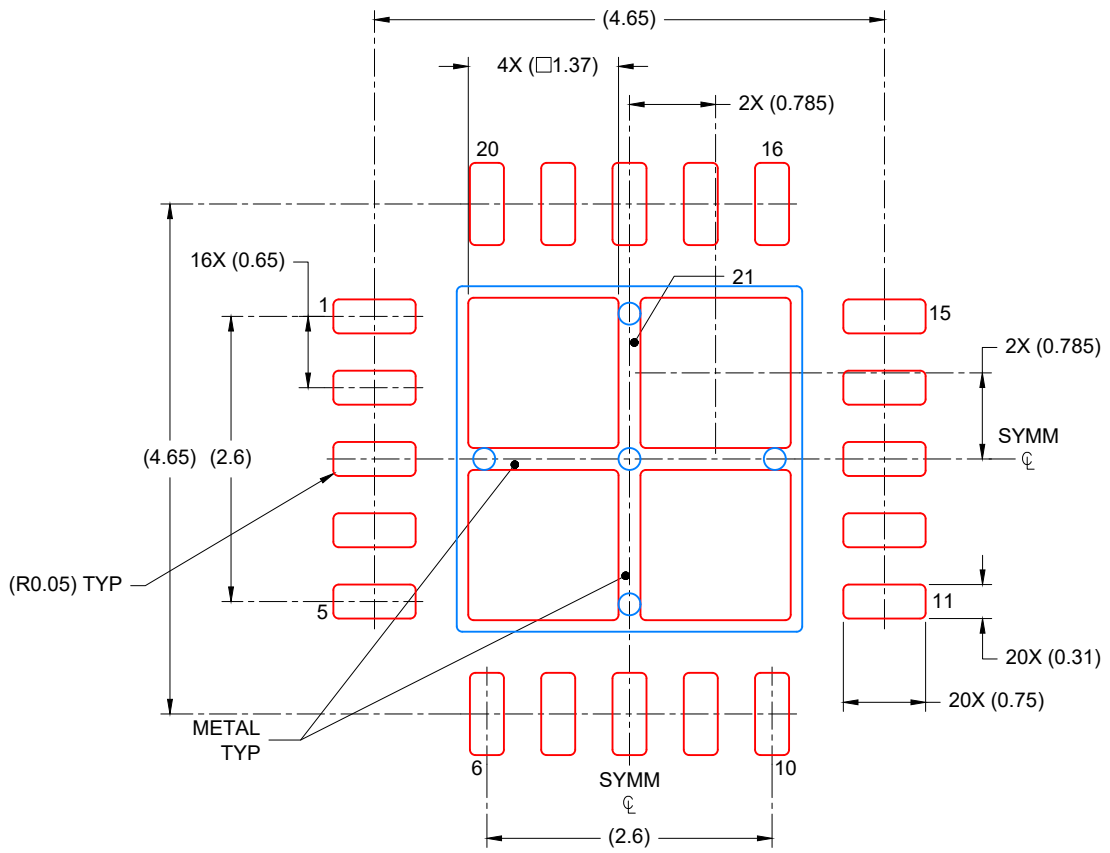


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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