

TPS7B81-Q1 車載用、150mA、バッテリー直結型、超低 I_Q (3 μ A)、低ドロップアウトレギュレータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: -40°C ~ 125°C, T_A
- デバイス接合部温度範囲: -40°C ~ 150°C
- 3V ~ 40V の広い V_{IN} 入力電圧範囲、最大 45V の過渡電圧に対応
- 最大出力電流: 150mA
- 小さい静止電流 (I_Q):
 - EN = LOW (シャットダウン モード) 時: 300nA (標準値)
 - 軽負荷時標準値: 2.7 μ A
 - 軽負荷時最大値: 4.5 μ A
- ライン、負荷、温度の全範囲にわたって 1.5% の出力電圧精度
- 最大ドロップアウト電圧: 固定 5V 出力バージョンで、負荷電流 150mA 時に 540mV
- 低 ESR (0.001 Ω ~ 5 Ω) のセラミック出力安定化コンデンサ (1 μ F ~ 200 μ F) で安定動作
- 5V、3.3V、2.5V の固定出力電圧
- フォルト保護機能を搭載:
 - サーマル シャットダウン
 - 短絡保護と過電流保護
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- パッケージ:
 - DGN (8 ピン HVSSOP)、 $R_{\theta JA} = 63.9^\circ\text{C/W}$
 - DRV (6 ピン WSON)、 $R_{\theta JA} = 72.8^\circ\text{C/W}$
 - KVU (5 ピン TO-252)、 $R_{\theta JA} = 38.8^\circ\text{C/W}$

2 アプリケーション

- 車載ヘッドユニット
- ヘッドライト
- バッテリー管理システム (BMS)
- インバータおよびモータ制御

3 説明

車載用のバッテリー接続アプリケーションでは、エネルギーを削減し、バッテリー駆動時間を延長するため、静止電流 (I_Q) が低いことが重要です。常時オンのシステムでは、車両のエンジンが停止しているときも継続して動作できるようにするため、拡張温度範囲にわたって非常に低い I_Q が要求されます。

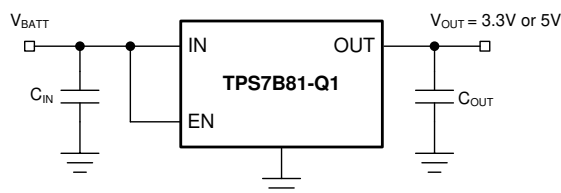
TPS7B81-Q1 は、 V_{IN} が 40V までのアプリケーション用に設計された低ドロップアウト (LDO) リニアレギュレータです。このデバイスは、軽負荷時の静止電流がわずか 2.7 μ A (標準値) であるため、スタンバイシステム内のマイコンや CAN/LIN (コントローラエリアネットワーク/ローカル相互接続ネットワーク) トランシーバへの給電に最適のソリューションです。

このデバイスには、短絡および過電流保護機能が内蔵されています。このデバイスは -40°C ~ +125°C の周囲温度、-40°C ~ +150°C の接合部温度で動作します。また、サイズや熱伝導率が異なる複数のパッケージで使用できます。小型の WSON パッケージを使用すると、最も小型の PCB を容易に設計でき、TO-252 パッケージを使用すると、デバイス全体で大きな放熱が発生する場合でも連続動作が可能です。これらの特長により、このデバイスは各種のバッテリー接続車載アプリケーションの電源として適しています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TPS7B81-Q1	DGN (HVSSOP, 8)	3mm × 3mm
	DRV (WSON, 6)	2mm × 2mm
	KVU (TO-252, 5)	6.1mm × 6.6mm

- 詳細については、[メカニカル](#)、[パッケージ](#)、および[注文情報](#)をご覧ください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンを含みます。



代表的なアプリケーション回路図



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4 Pin Configuration and Functions

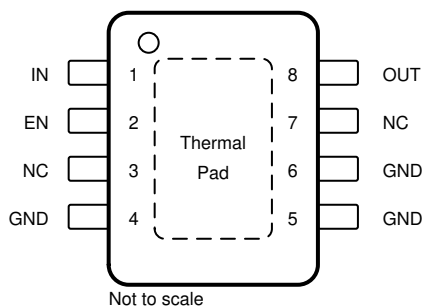


図 4-1. DGN Package, 8-Pin HVSSOP PowerPAD™ (Top View)

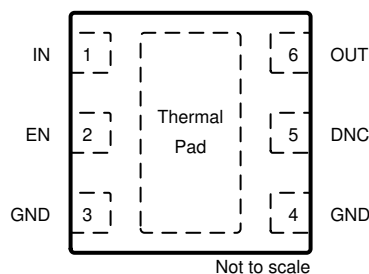


図 4-2. DRV Package, 6-Pin WSON PowerPAD™ (Top View)

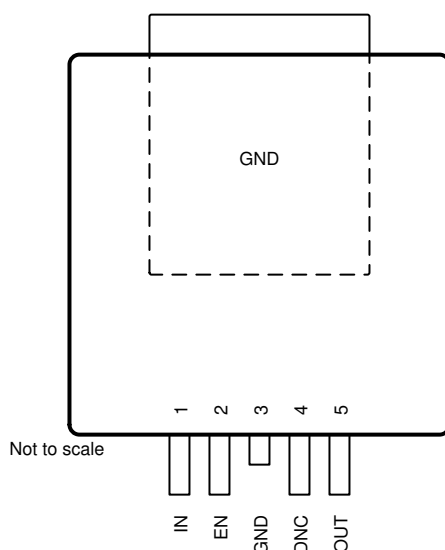


図 4-3. KVV Package, 5-Pin TO-252 (Top View)

表 4-1. Pin Functions

NAME	PIN NO.			I/O	DESCRIPTION
	DGN	DRV	KVV		
DNC	—	5	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	I	Enable input pin. Drive EN greater than V_{IH} to turn on the regulator. Drive EN less than V_{IL} to put the low-dropout (LDO) into shutdown mode.
GND	4, 5, 6	3, 4	3, TAB	—	Ground reference
IN	1	1	1	I	Input power-supply pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input Capacitor section. Place the input capacitor as close to the output of the device as possible.
NC	3, 7	—	—	—	Not internally connected

表 4-1. Pin Functions (続き)

PIN				I/O	DESCRIPTION
NAME	NO.				
	DGN	DRV	KVU		
OUT	8	6	5	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <i>Recommended Operating Conditions</i> table and the <i>Output Capacitor</i> section. Place the output capacitor as close to output of the device as possible.
Thermal pad				—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Unregulated input ⁽³⁾	−0.3	45	V
V _{EN}	Enable input ⁽³⁾	−0.3	V _{IN}	V
V _{OUT}	Regulated output	−0.3	7	V
T _J	Junction temperature range	−40	150	°C
T _{stg}	Storage temperature range	−40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute maximum voltage, can withstand 45 V for 200 ms.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
		Corner pins	±500	
		Other pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	3	40	V
V _{EN}	Enable input voltage	0	V _{IN}	V
C _{OUT}	Output capacitor requirements ⁽¹⁾	1	200	μF
ESR	Output capacitor ESR requirements ⁽²⁾	0.001	5	Ω
T _A	Ambient temperature range	−40	125	°C
T _J	Junction temperature range	−40	150	°C

- (1) The output capacitance range specified in the table is the effective value.
- (2) Relevant ESR value at f = 10 kHz

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7B81-Q1			UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

5.5 Electrical Characteristics

over operating ambient temperature range, $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, and $10\text{-}\mu\text{F}$ ceramic output capacitor (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V _{IN}	Input voltage			V _{OUT(Nom)} + V _(Dropout)		40	V
I _(SD)	Shutdown current	EN = 0 V		0.3		1	µA
I _(Q)	Quiescent current	V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0 mA		1.9		3.5	µA
		V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0.2 mA	DGN package	2.7		6.5	
			DRV and KVVU packages	2.7		4.5	
V _(IN, UVLO)	V _{IN} undervoltage detection	Ramp V _{IN} down until the output turns off				2.7	V
		Hysteresis				200	mV
ENABLE INPUT (EN)							
V _{IL}	Logic-input low level					0.7	V
V _{IH}	Logic-input high level			2			V
I _{EN}	Enable current			10			nA
REGULATED OUTPUT (OUT)							
V _{OUT}	Regulated output	V _{IN} = V _{OUT} + V _(Dropout) to 40 V, I _{OUT} = 1 mA to 150 mA		–1.5%		1.5%	
V _(Line-Reg)	Line regulation	V _{IN} = 6 V to 40 V, I _{OUT} = 10 mA				10	mV
V _(Load-Reg)	Load regulation	V _{IN} = 14 V, I _{OUT} = 1 mA to 150 mA	DGN package			20	mV
			DRV and KVVU packages			10	

5.5 Electrical Characteristics (続き)

over operating ambient temperature range, $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, and $10\text{-}\mu\text{F}$ ceramic output capacitor (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _(Dropout)	Dropout voltage ⁽¹⁾	V _{OUT} = 5 V	I _{OUT} = 150 mA	DGN package		270	540	mV
				DRV and KVVU packages		325	585	
			I _{OUT} = 100 mA	DGN package		180	350	
				DRV and KVVU packages		200	390	
		V _{OUT} = 3.3 V	I _{OUT} = 150 mA	DGN package		650		
				DRV and KVVU packages		345	675	
			I _{OUT} = 100 mA			255	450	
I _{OUT}	Output current	V _{OUT} in regulation, V _{IN} = 7 V for the fixed 5-V option, V _{IN} = 5.8 V for the fixed 3.3-V option			0		150	mA
I _(CL)	Output current limit	V _{OUT} short to 90% × V _{OUT}			180	510	690	mA
PSRR	Power-supply ripple rejection	V _(Ripple) = 0.5 V _{PP} , I _{OUT} = 10 mA, frequency = 100 Hz, C _{OUT} = 2.2 μF				60		dB
OPERATING TEMPERATURE RANGE								
T _(SD)	Junction shutdown temperature					175		°C
T _(HYST)	Hysteresis of thermal shutdown					20		°C

(1) Dropout is not valid for the 2.5-V output because of the minimum input voltage limits.

5.6 Typical Characteristics

at $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, and $V_{EN} \geq 2\text{ V}$ (unless otherwise noted)

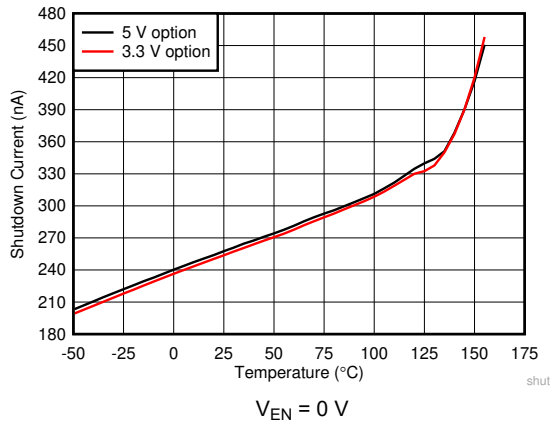


Figure 5-1. Shutdown Current vs Ambient Temperature

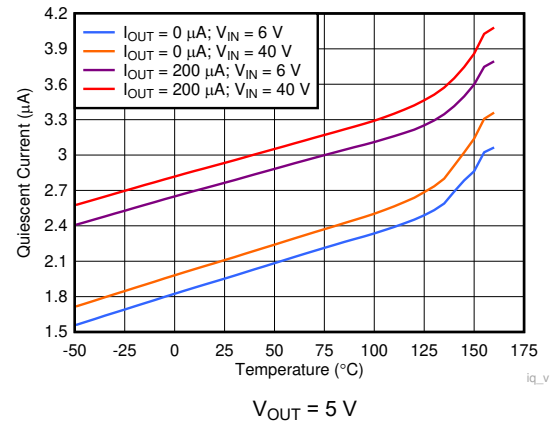


Figure 5-2. Quiescent Current vs Ambient Temperature

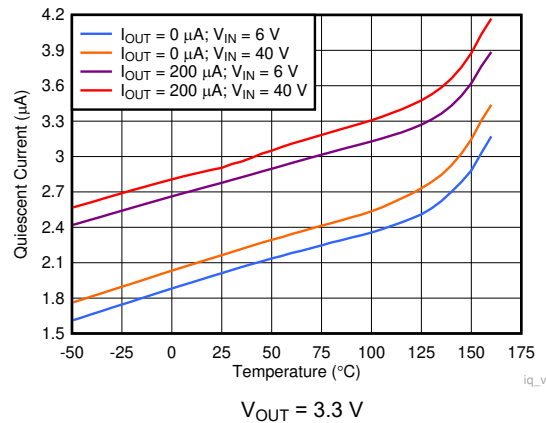


Figure 5-3. Quiescent Current vs Ambient Temperature

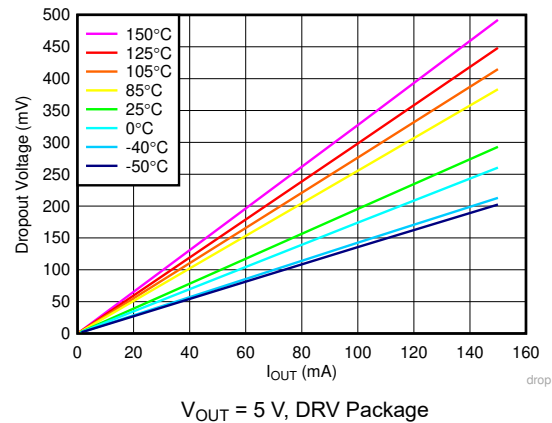


Figure 5-4. Dropout Voltage vs Output Current

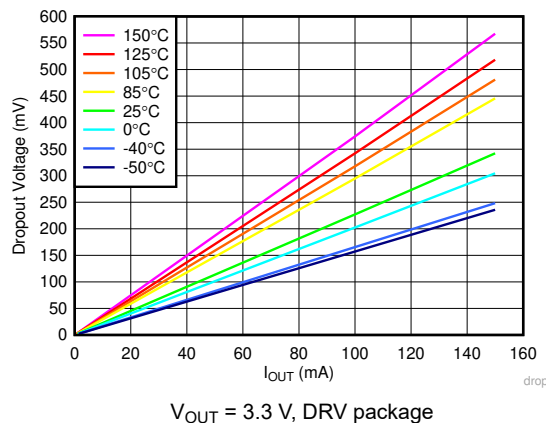


Figure 5-5. Dropout Voltage vs Output Current

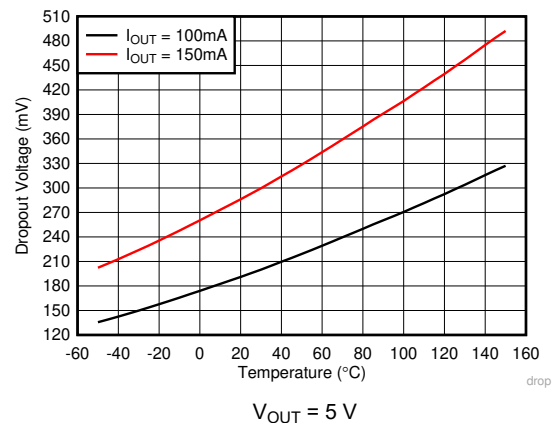


Figure 5-6. Dropout Voltage vs Ambient Temperature

5.6 Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{\text{IN}} = 14\text{ V}$, and $V_{\text{EN}} \geq 2\text{ V}$ (unless otherwise noted)

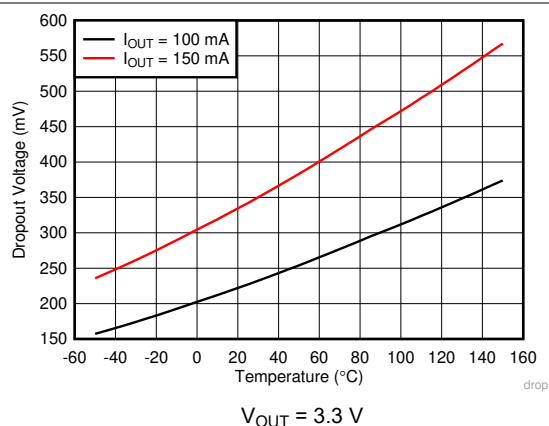


FIG 5-7. Dropout Voltage vs Ambient Temperature

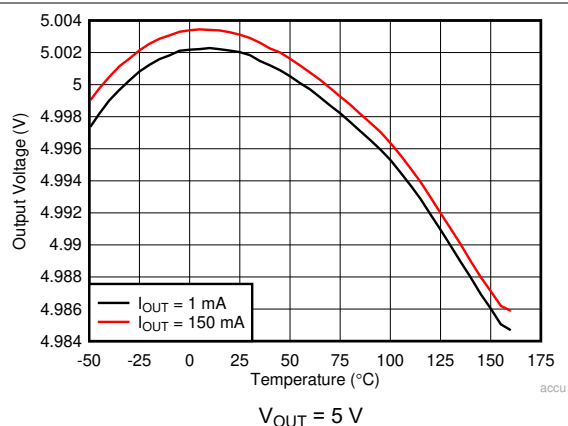


FIG 5-8. Output Voltage vs Ambient Temperature

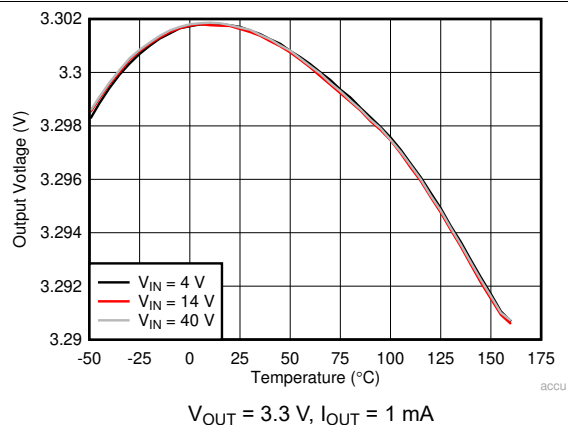


FIG 5-9. Output Voltage vs Ambient Temperature

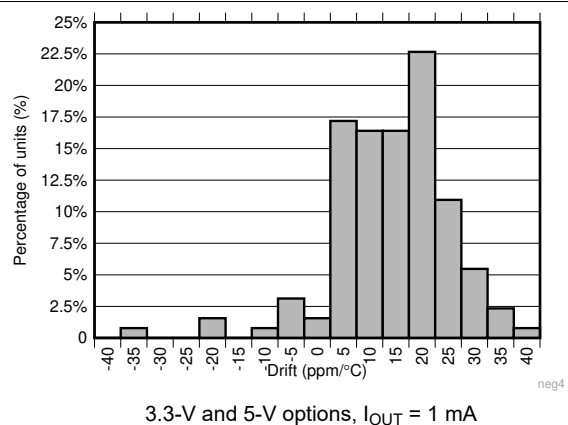


FIG 5-10. Temperature Drift Histogram (-40°C to $+25^{\circ}\text{C}$)

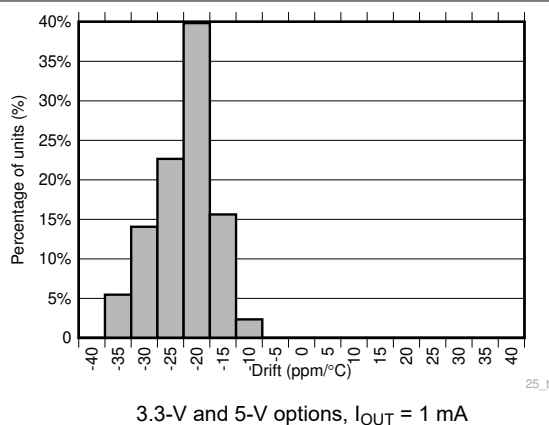


FIG 5-11. Temperature Drift Histogram (25°C to 150°C)

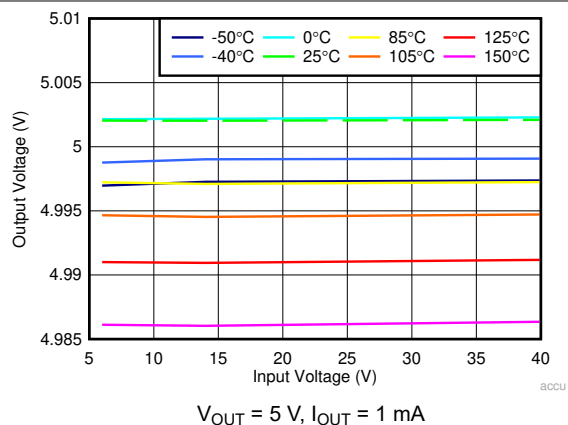


FIG 5-12. Output Voltage vs Input Voltage

5.6 Typical Characteristics (continued)

at $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, $V_{IN} = 14\text{ V}$, and $V_{EN} \geq 2\text{ V}$ (unless otherwise noted)

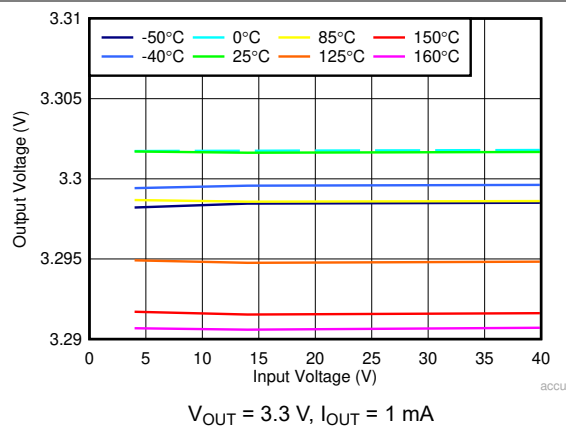


図 5-13. Output Voltage vs Input Voltage

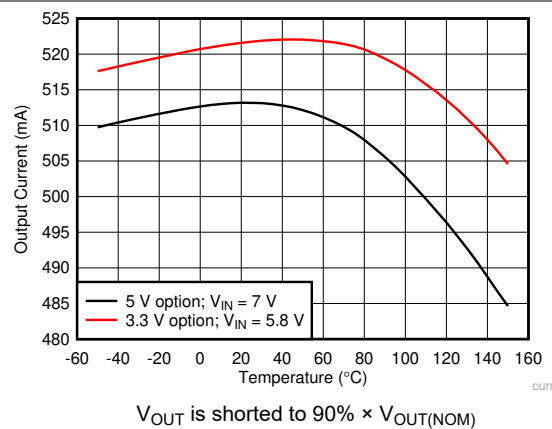
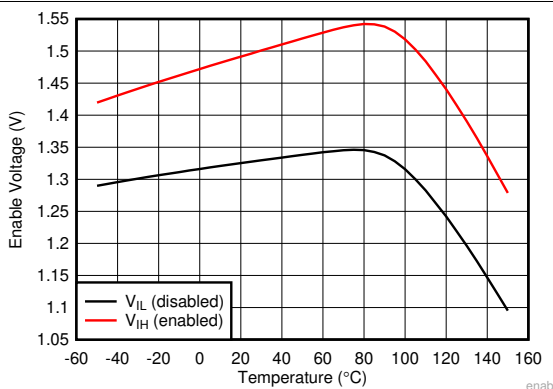
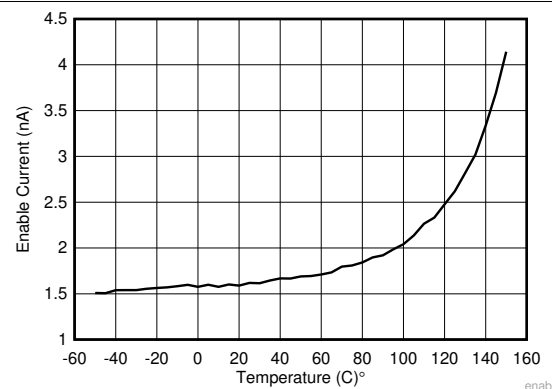


図 5-14. Output Current Limit vs Ambient Temperature



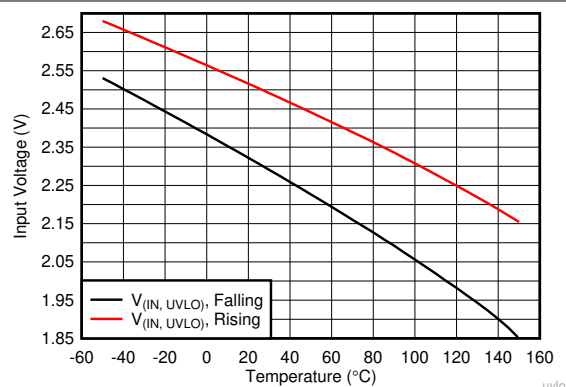
A.

図 5-15. Enable Voltage vs Ambient Temperature



A.

図 5-16. Enable Current vs Ambient Temperature



A.

図 5-17. UVLO vs Ambient Temperature

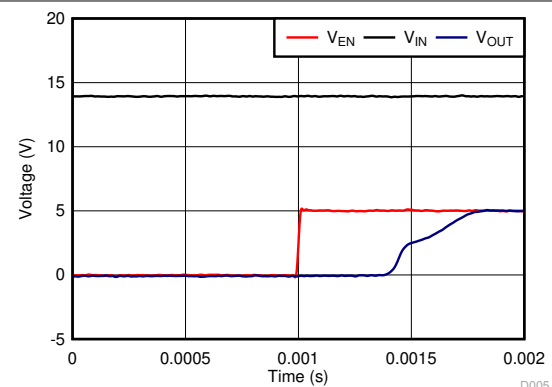


図 5-18. Startup With Enable

5.6 Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, and $V_{EN} \geq 2\text{ V}$ (unless otherwise noted)

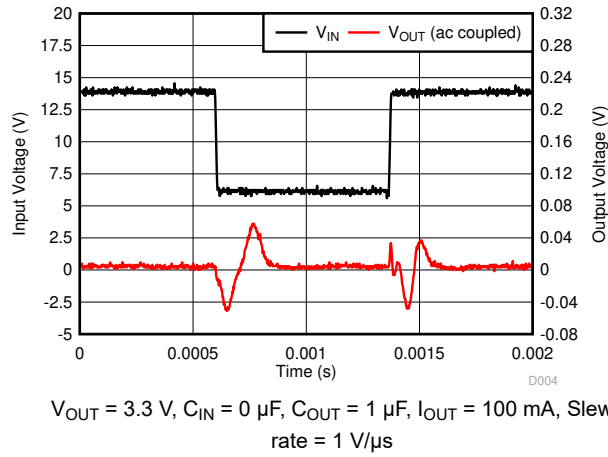


Figure 5-19. Line Transient

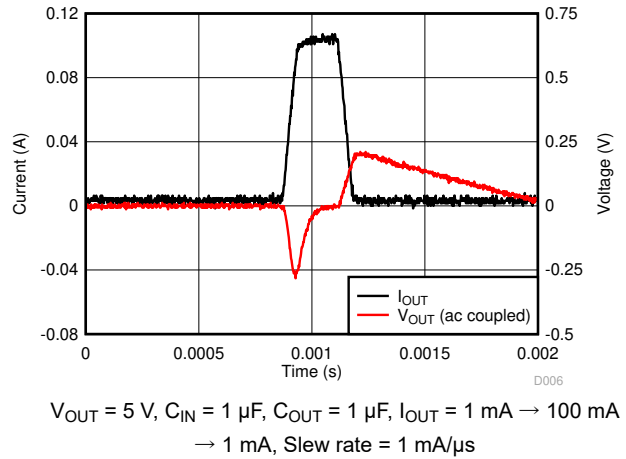


Figure 5-20. Load Transient

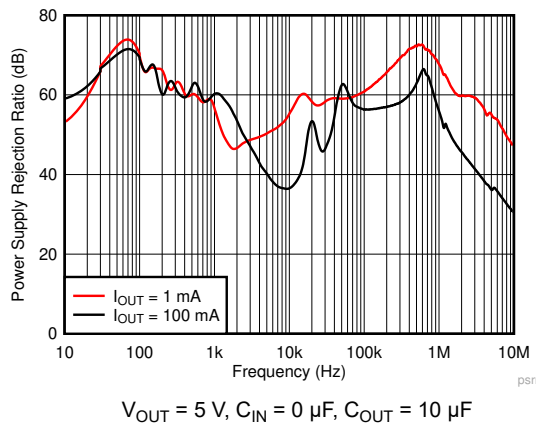


Figure 5-21. PSRR vs Frequency

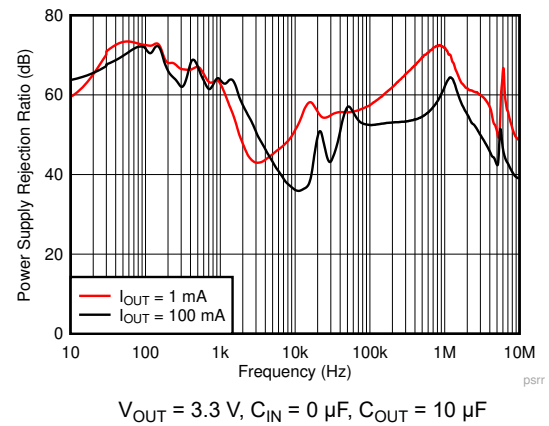


Figure 5-22. PSRR vs Frequency

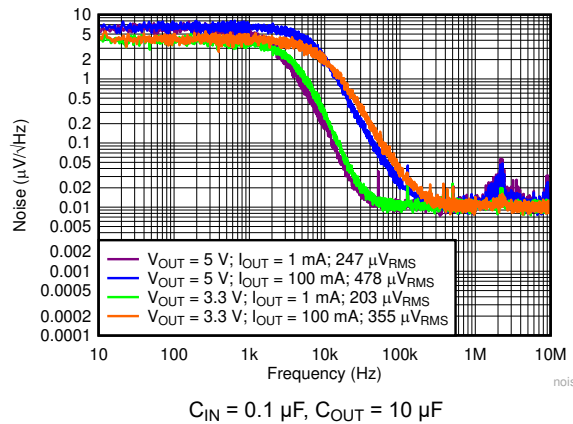


Figure 5-23. Noise vs Frequency

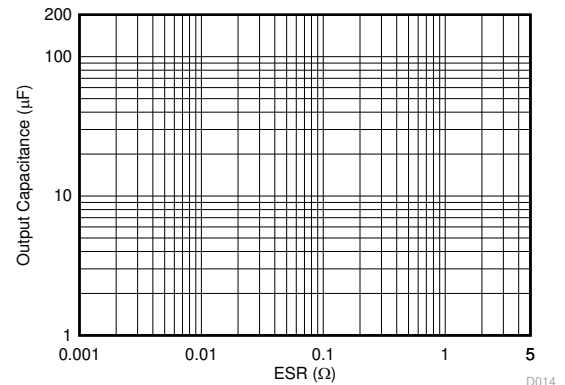


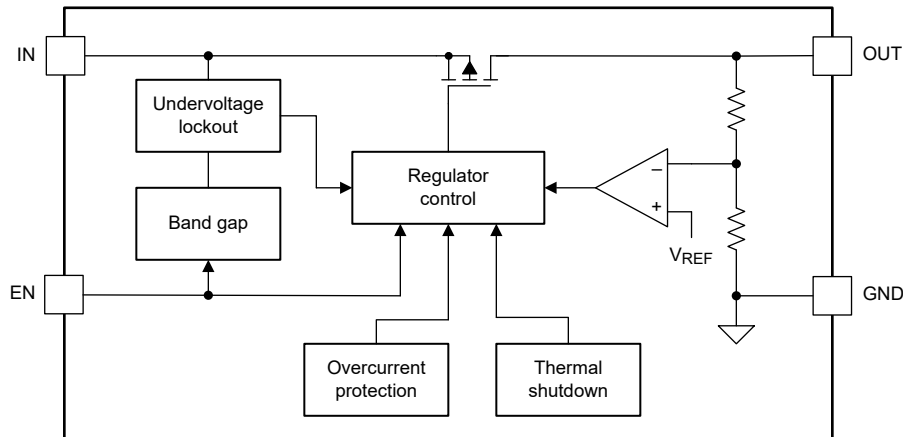
Figure 5-24. Output Capacitance vs ESR Stability

6 Detailed Description

6.1 Overview

The TPS7B81-Q1 is a 40-V, 150-mA, low-dropout (LDO) linear regulator with ultralow quiescent current. This voltage regulator consumes only 3 μ A of quiescent current at light load, and is quite suitable for the automotive always-on application.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation on. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

6.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold (V_{UVLO}). This feature ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

6.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

6.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the thermal shutdown hysteresis, the output turns on again.

6.4 Device Functional Modes

6.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. The device does not operate at input voltages below the actual UVLO voltage.

6.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{(Dropout)}$ and $V_{IN} \geq 3\text{ V}$	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160^\circ\text{C}$
Dropout mode	$3\text{ V} \leq V_{IN} < V_{OUT(nom)} + V_{(Dropout)}$	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160^\circ\text{C}$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{(IN, UVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > 160^\circ\text{C}$

7 Application and Implementation

注

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7.1 Application Information

The TPS7B81-Q1 is a 150-mA, 40-V, low-dropout (LDO) linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

7.1.1 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be approximated using 式 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A), according to 式 2. The equation is rearranged for output current in 式 3.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (2)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the v table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCBot}$) plus the thermal resistance contribution by the PCB copper.

図 7-1 through 図 7-6 show the functions of $R_{\theta JA}$ and ψ_{JB} vs. copper area and thickness. These plots are generated with a 101.6 mm x 101.6 mm x 1.6mm PCB of two and four layers. For the four layer board, inner planes use 1 oz copper thickness. Outer layers are simulated with both 1 oz and 2 oz copper thickness. A 2 x 1 array of thermal vias of 300 μ m drill diameter and 25 μ m Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

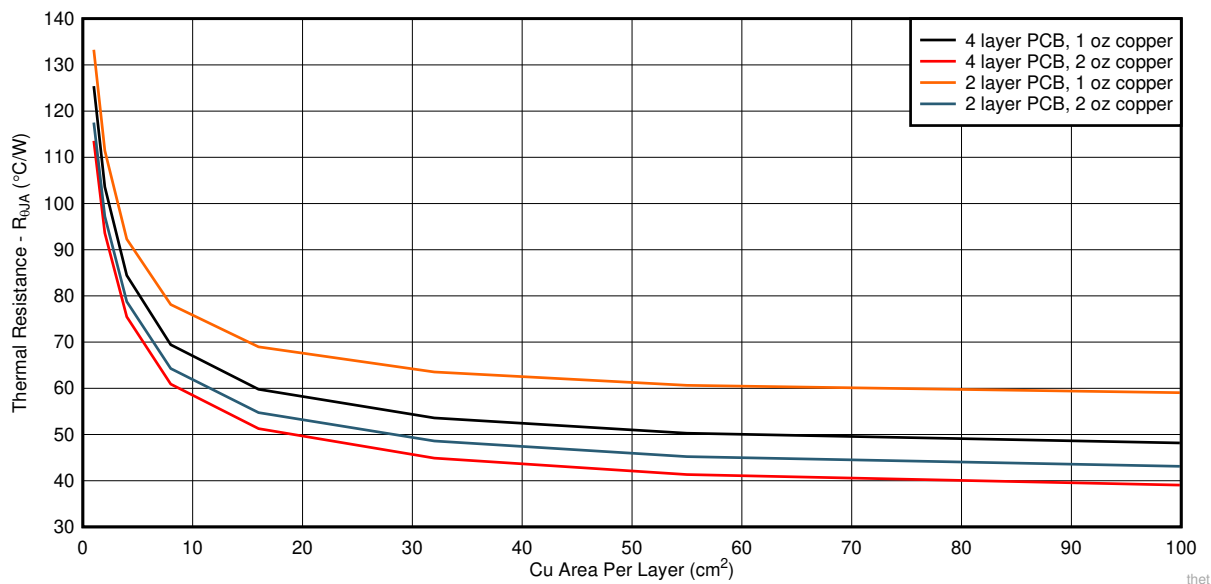


図 7-1. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package

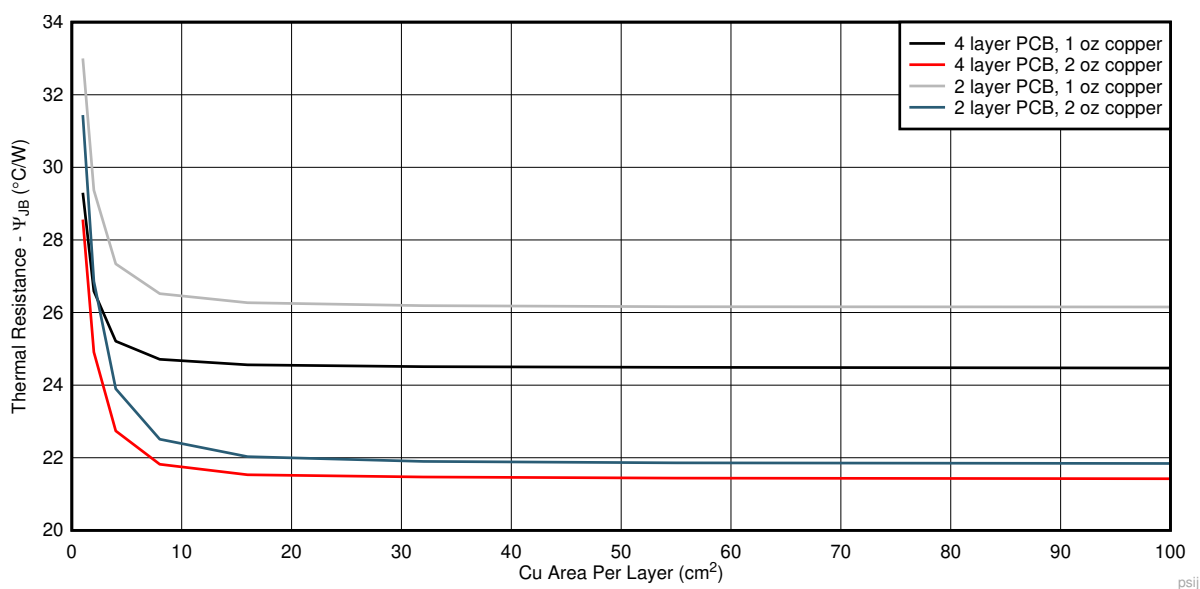


図 7-2. ψ_{JB} versus Cu Area for the WSON (DRV) Package

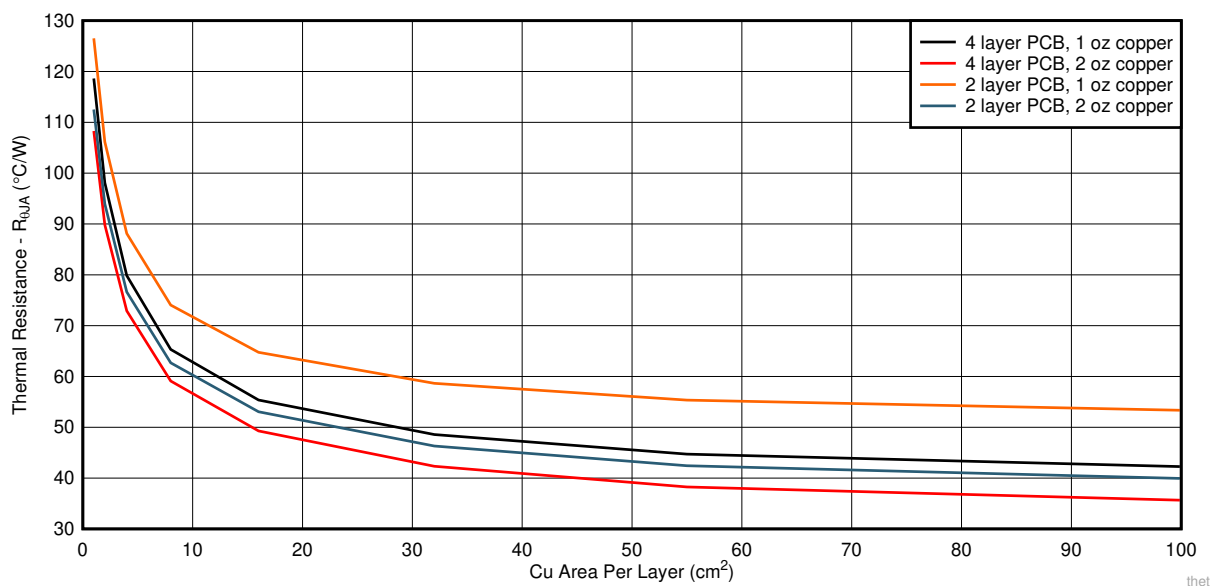


図 7-3. $R_{\theta JA}$ versus Cu Area for the HVSSOP (DGN) Package

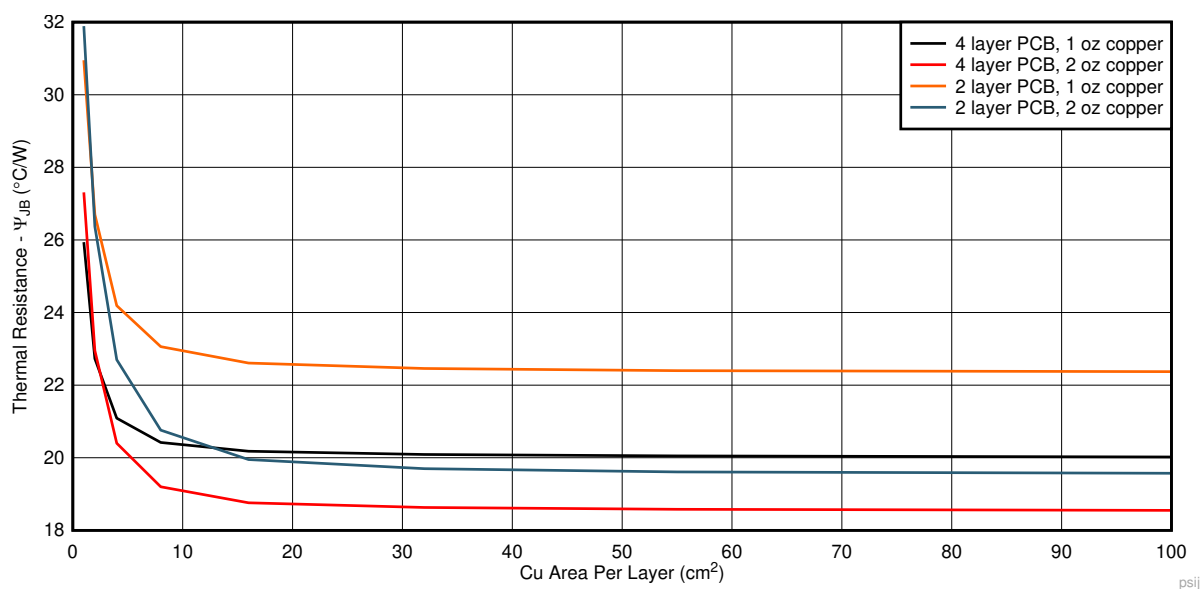


図 7-4. ψ_{JB} versus Cu Area for the HVSSOP (DGN) Package

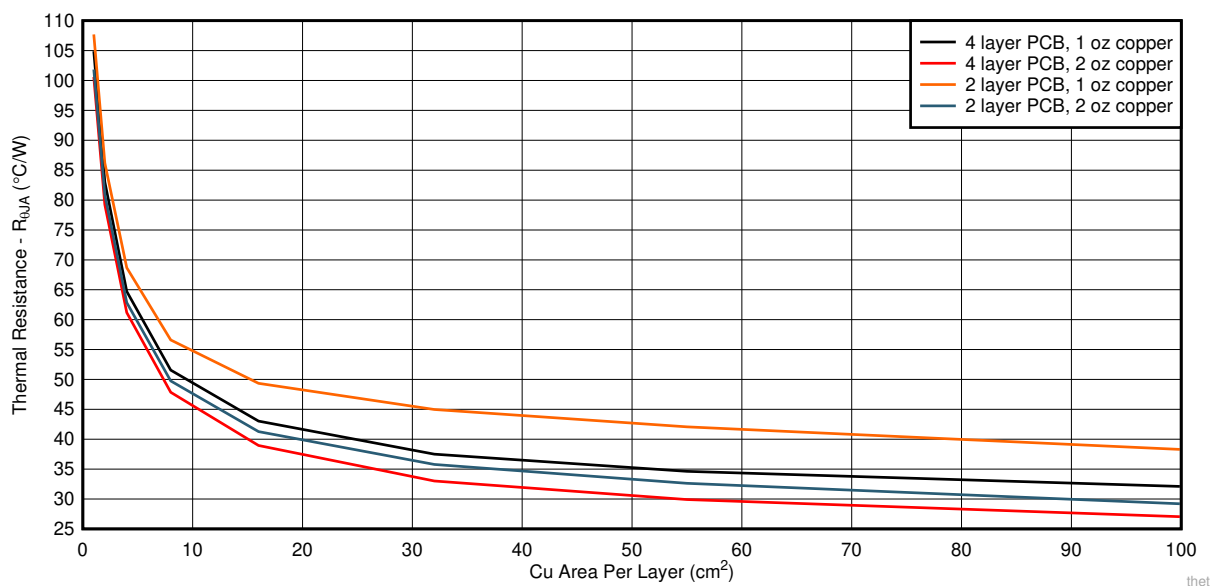


図 7-5. $R_{\theta JA}$ versus Cu Area for the TO-252 (KVU) Package

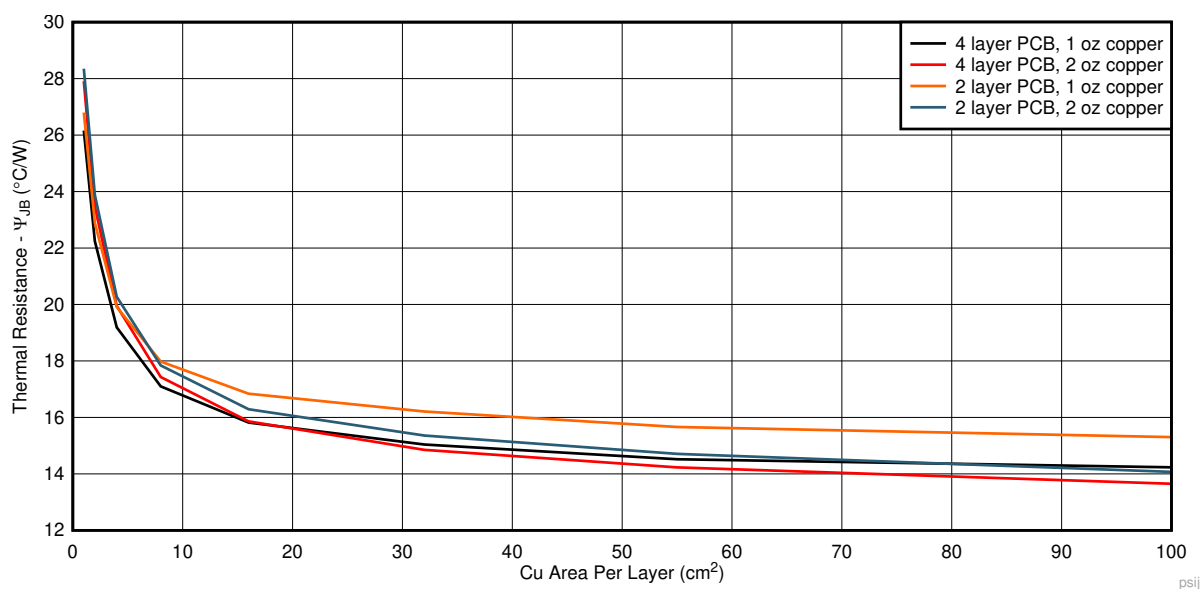


図 7-6. ψ_{JB} versus Cu Area for the TO-252 (KVU) Package

7.1.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the [セクション 5.4](#) table and are used in accordance with [式 4](#).

$$\begin{aligned}\Psi_{JT}: T_J &= T_T + \Psi_{JT} \times P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \times P_D\end{aligned}\tag{4}$$

where:

- P_D is the power dissipated as explained in [式 1](#)
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

7.2 Typical Application

[図 7-7](#) shows a typical application circuit for the TPS7B81-Q1. Different external component values can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric.

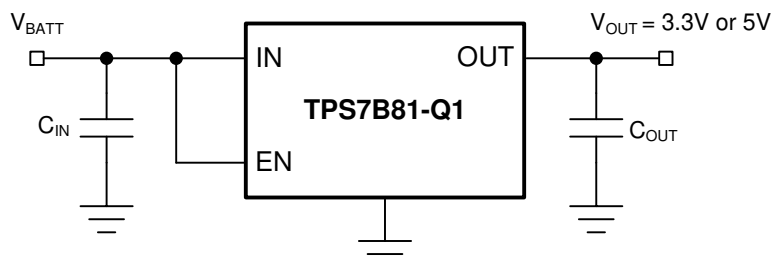


図 7-7. TPS7B81-Q1 Typical Application Schematic

7.2.1 Design Requirements

Use the parameters listed in [表 7-1](#) for this design example.

表 7-1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	150 mA maximum

7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

7.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10- μ F to 22- μ F capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

To ensure the stability of the TPS7B81-Q1, the device requires an output capacitor with a value in the range from 1 μ F to 200 μ F and with an ESR range between 0.001 Ω and 5 Ω . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

7.2.3 Application Curve

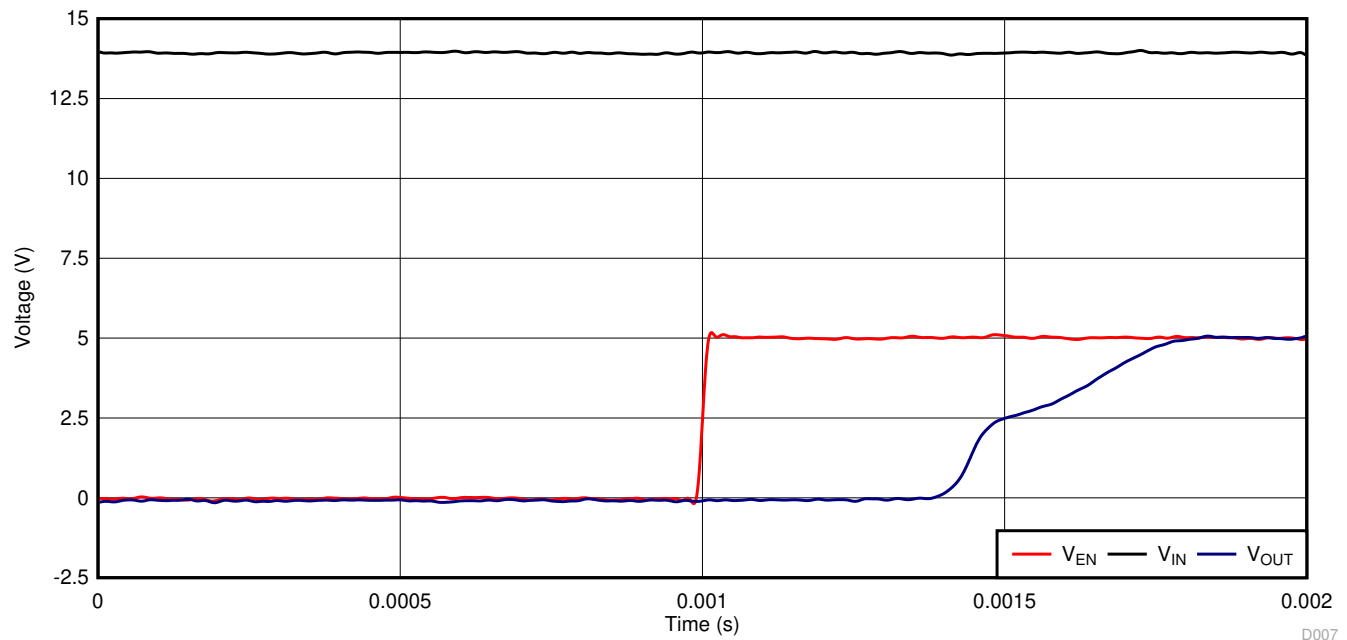


図 7-8. TPS7B81-Q1 Power-Up Waveform (5 V)

7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3 V to 40 V. The input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B81-Q1, TI recommends adding a capacitor with a value greater than or equal to 10 μ F with a 0.1- μ F bypass capacitor in parallel at the input.

7.4 Layout

7.4.1 Layout Guidelines

Layout is an important step for LDO power supplies, especially for high-voltage and large-output-current supplies. If the layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitations. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and put enough thermal vias on the copper under the thermal pad. 図 7-9 shows an example layout.

7.4.2 Layout Example

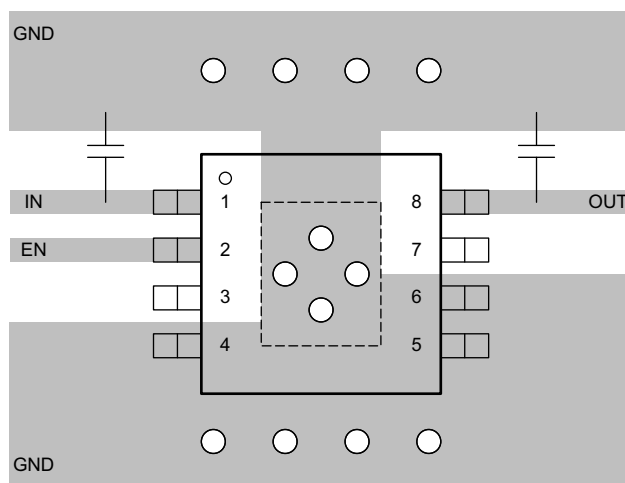


図 7-9. TPSB81-Q1 Example Layout Diagram

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (June 2020) to Revision E (June 2025)	Page
・ 「特長」セクションに機能安全の箇条書き項目を追加.....	1
・ Changed power FET from NMOS to PMOS in <i>Functional Block Diagram</i>	12

Changes from Revision C (April 2020) to Revision D (June 2020)	Page
・ ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1
・ Added footnote and deleted $V_{OUT} = 2.5\text{ V}$ rows from <i>Dropout voltage</i> parameter.....	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7B8133QWDRVRQ1	Active	Preproduction	WSON (DRV) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 150	
TPS7B8125QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	26GX
TPS7B8125QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	26GX
TPS7B8133QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VTX
TPS7B8133QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VTX
TPS7B8133QDRVRQ1	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1X2H
TPS7B8133QDRVRQ1.A	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1X2H
TPS7B8133QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8133Q1
TPS7B8133QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8133Q1
TPS7B8133QWDRVRQ1	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3NGH
TPS7B8150QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VUX
TPS7B8150QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VUX
TPS7B8150QDRVRQ1	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1WNH
TPS7B8150QDRVRQ1.A	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1WNH
TPS7B8150QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8150Q1
TPS7B8150QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8150Q1
TPS7B8150QWDRVRQ1	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3NHH

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS7B81-Q1 :

- Catalog : [TPS7B81](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

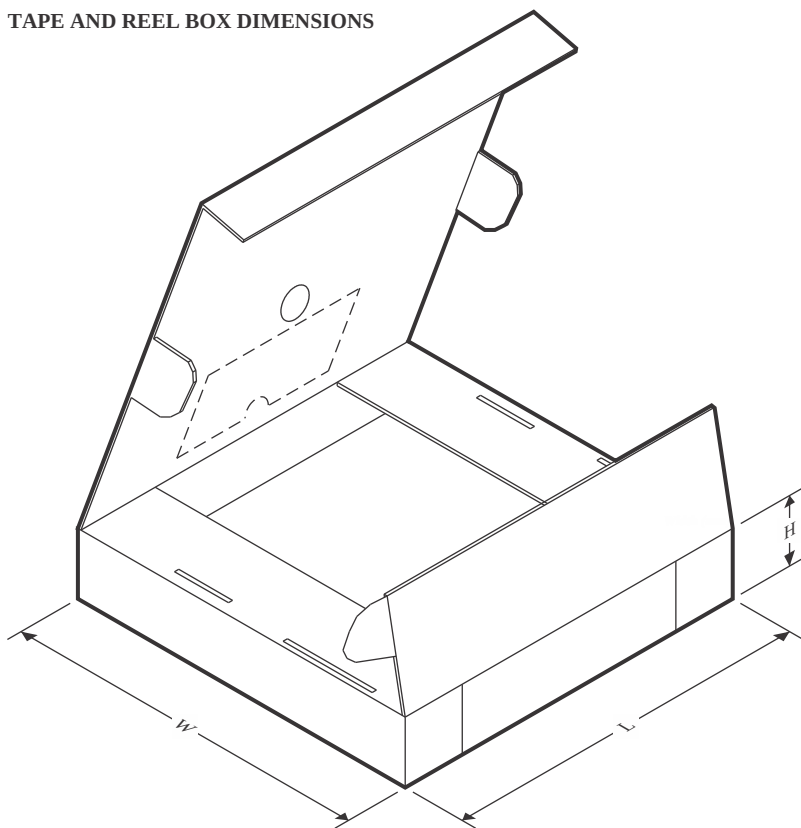
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8125QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8133QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8133QDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8133QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8133QWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8150QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8150QDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8150QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8150QWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8125QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8133QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8133QDRVRQ1	WSO	DRV	6	3000	210.0	185.0	35.0
TPS7B8133QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8133QWDRVRQ1	WSO	DRV	6	3000	210.0	185.0	35.0
TPS7B8150QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8150QDRVRQ1	WSO	DRV	6	3000	210.0	185.0	35.0
TPS7B8150QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8150QWDRVRQ1	WSO	DRV	6	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

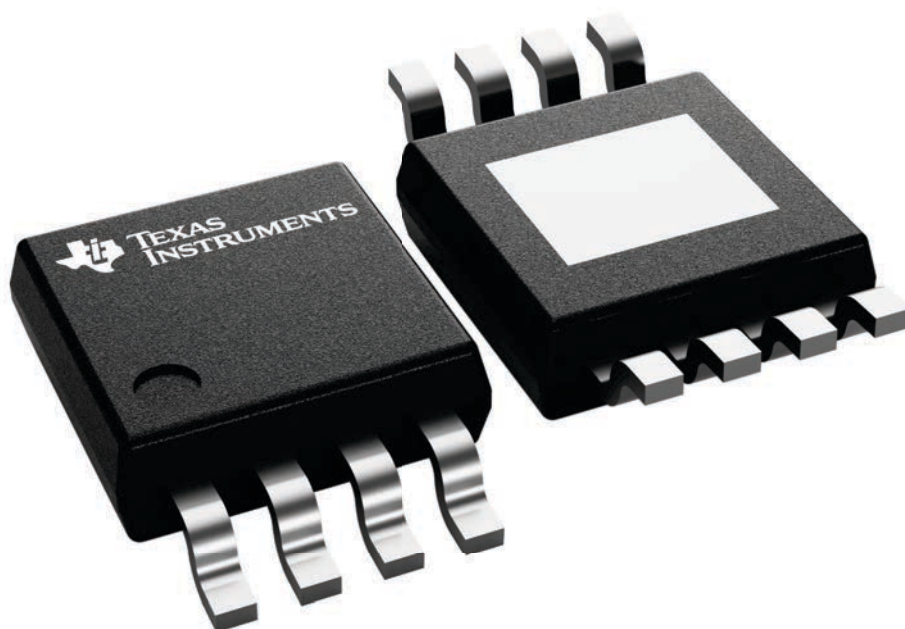
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

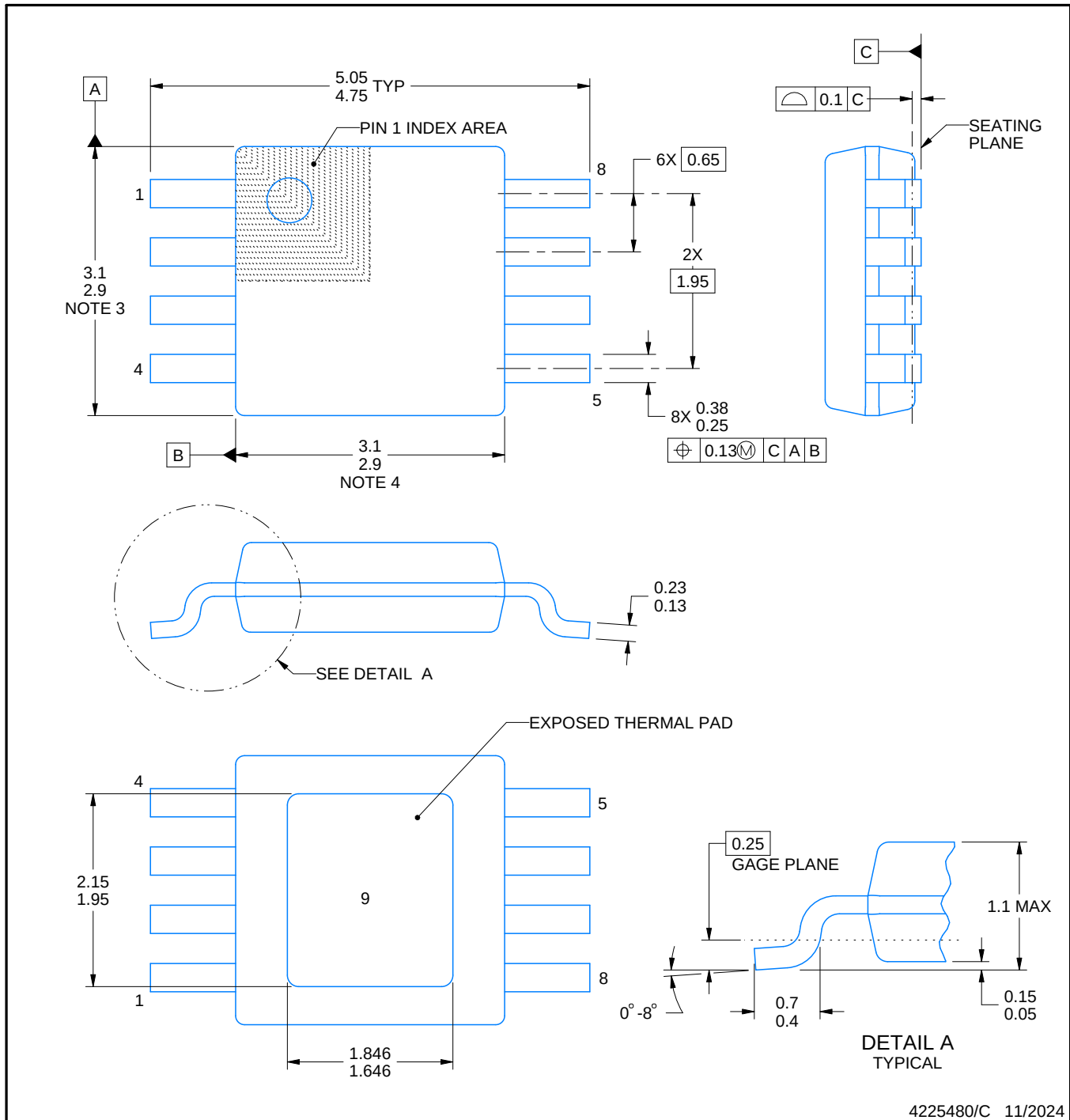
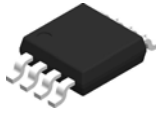
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225480/C 11/2024

NOTES:

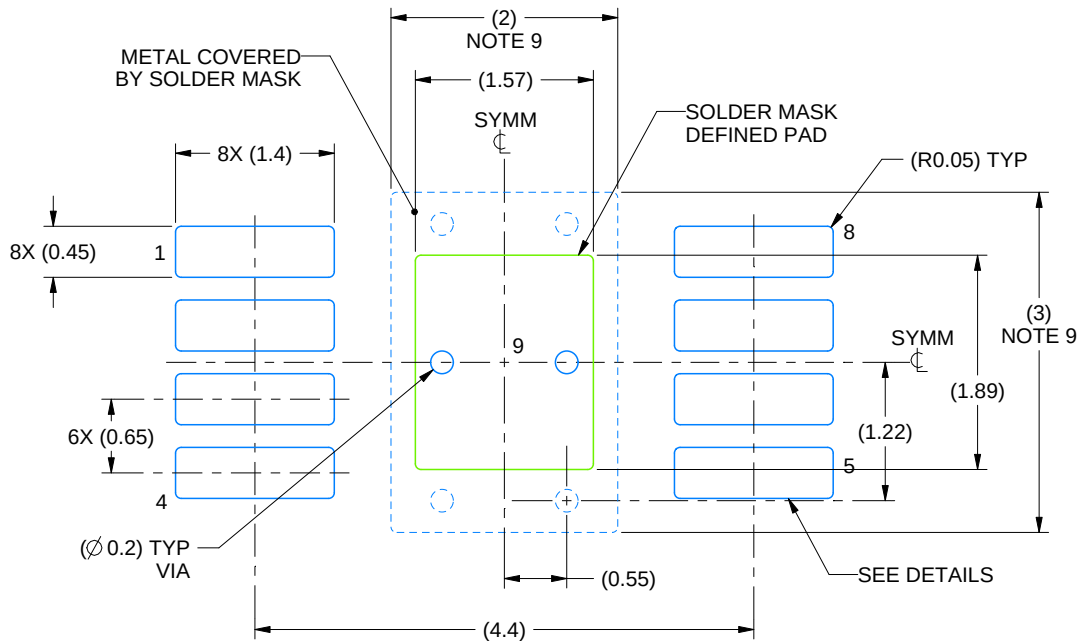
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

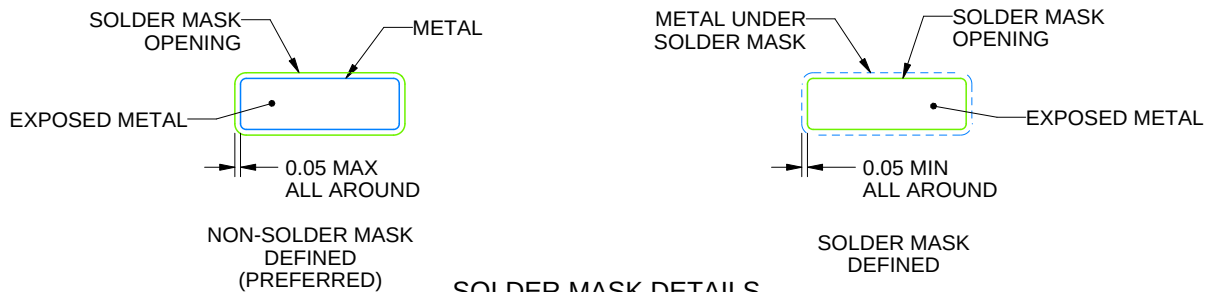
DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

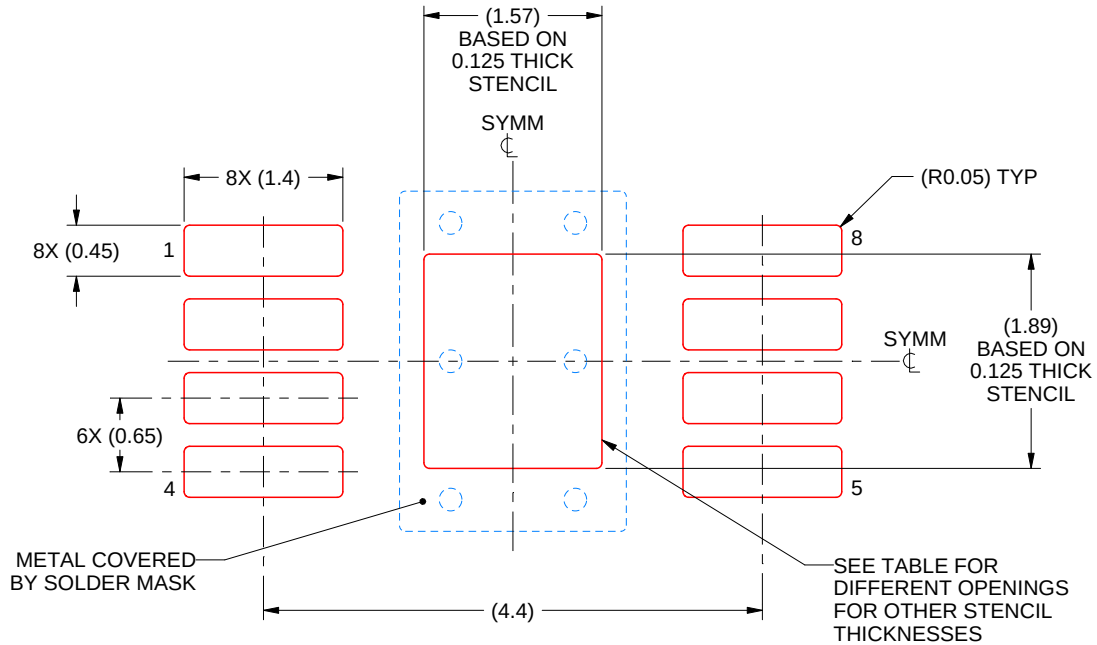
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



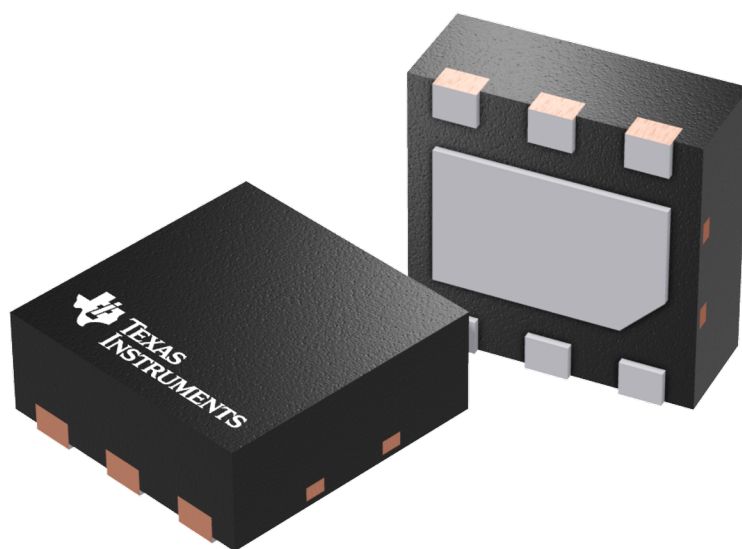
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

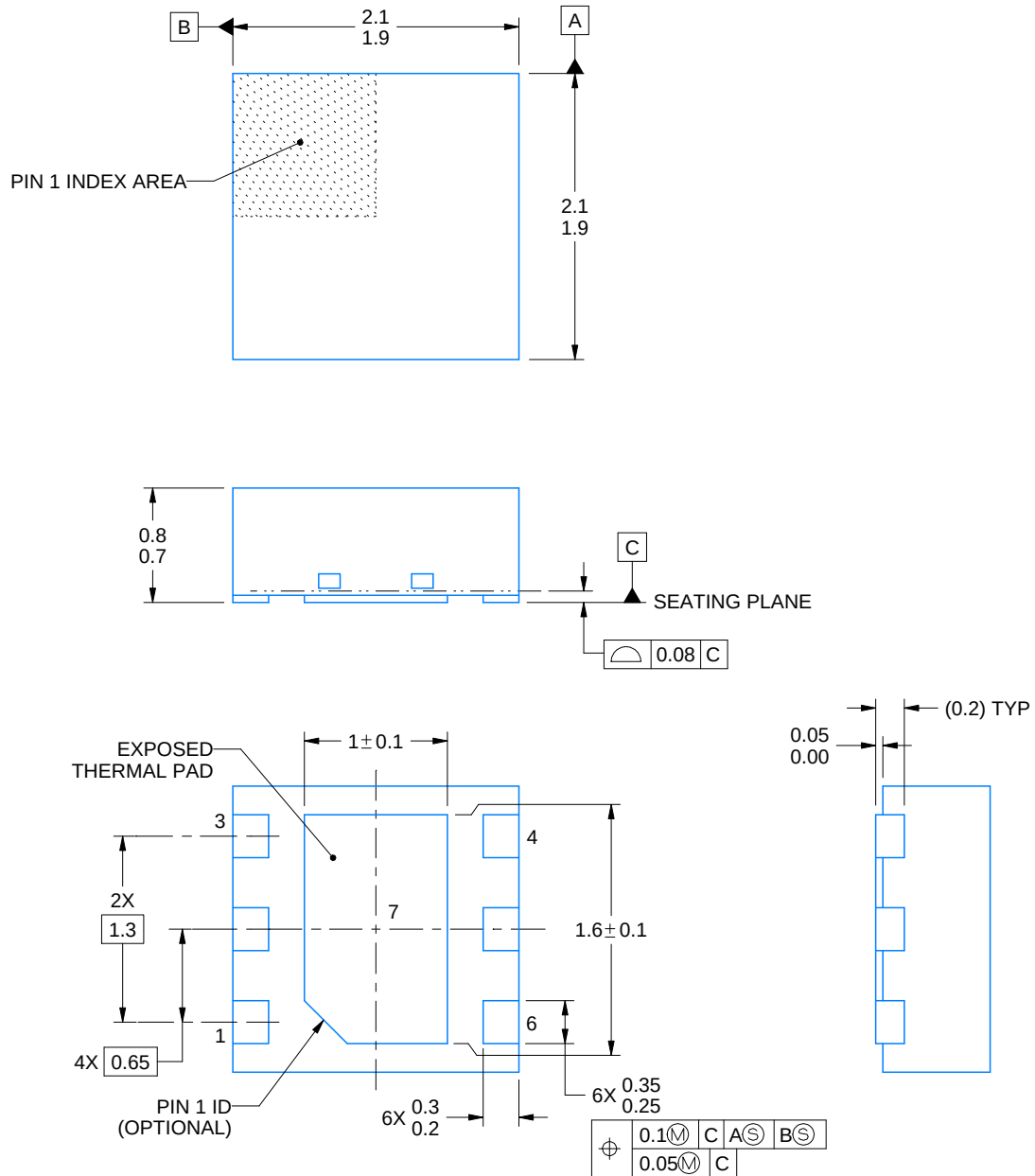
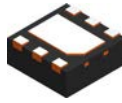
4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4222173/B 04/2018

NOTES:

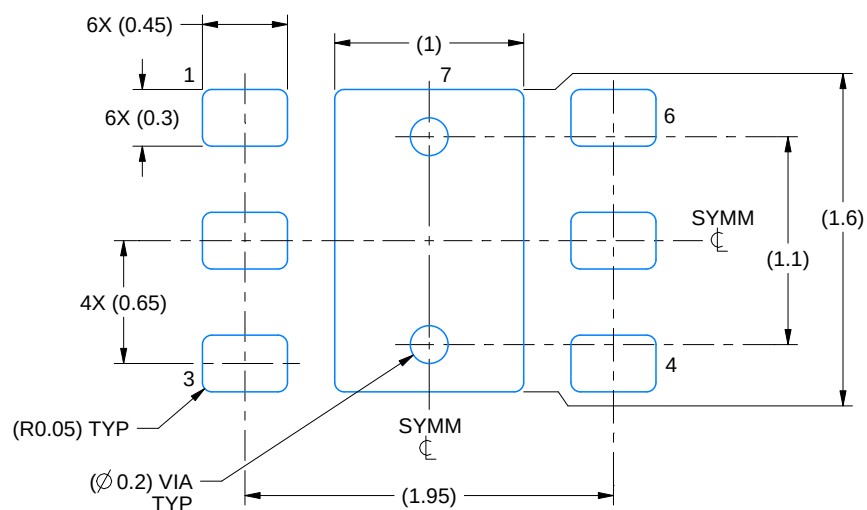
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

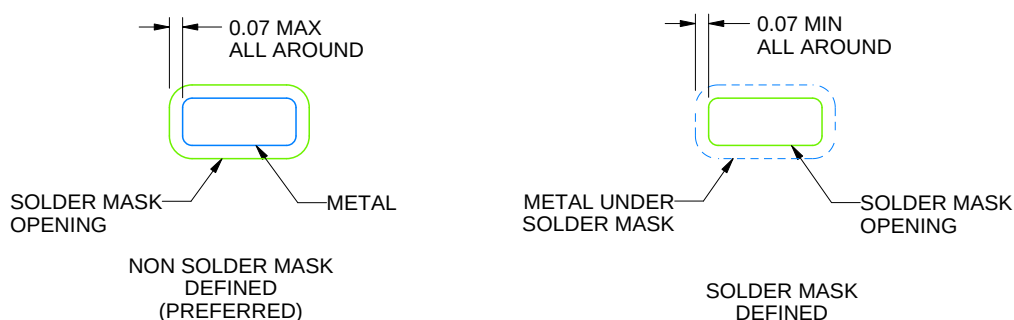
DRV0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

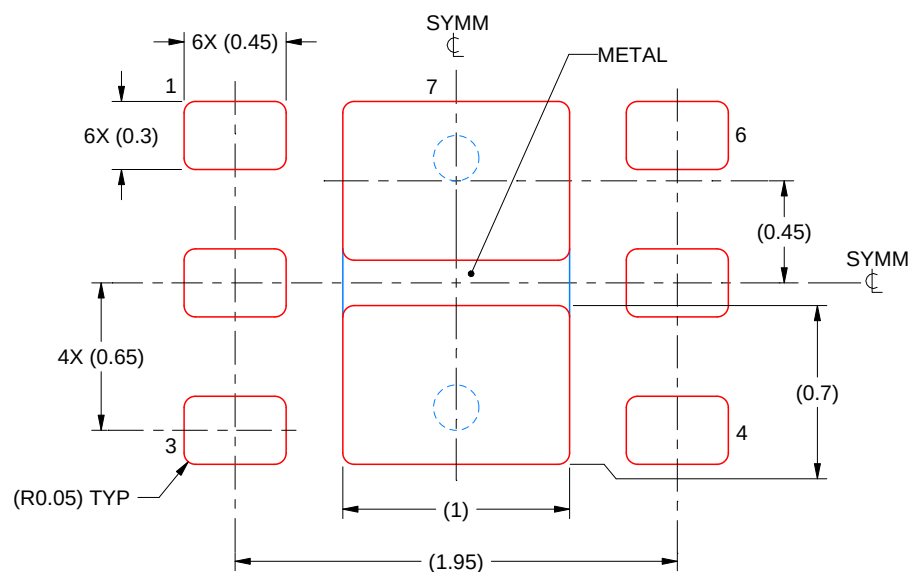
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

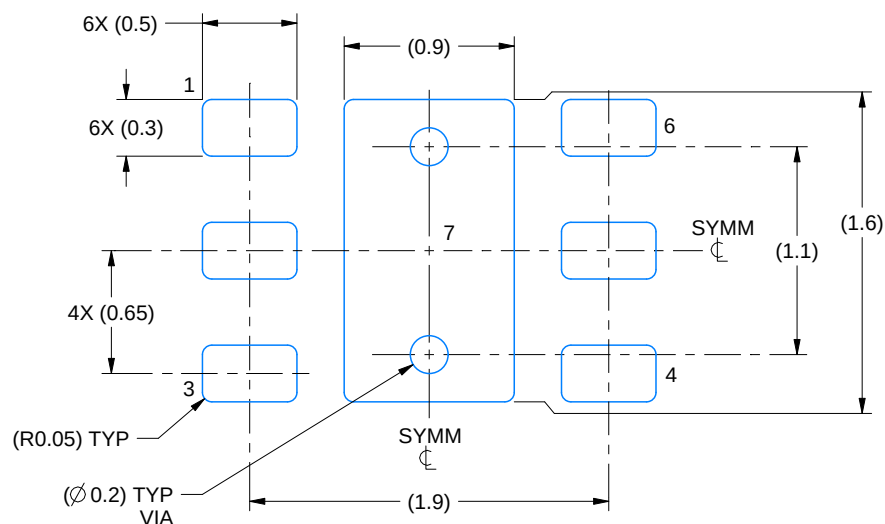
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

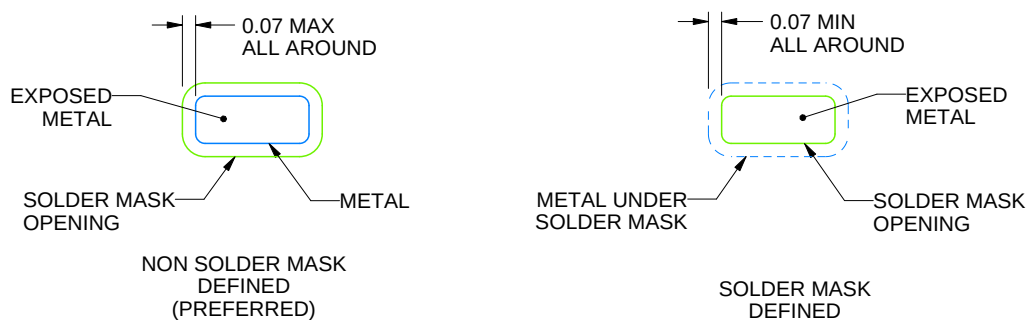
DRV0006C

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4223939/A 09/2017

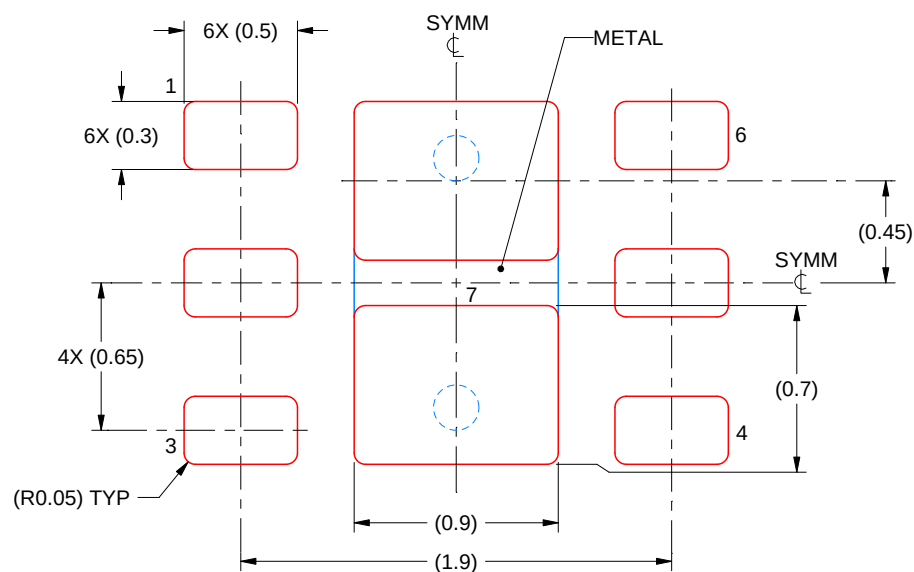
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4223939/A 09/2017

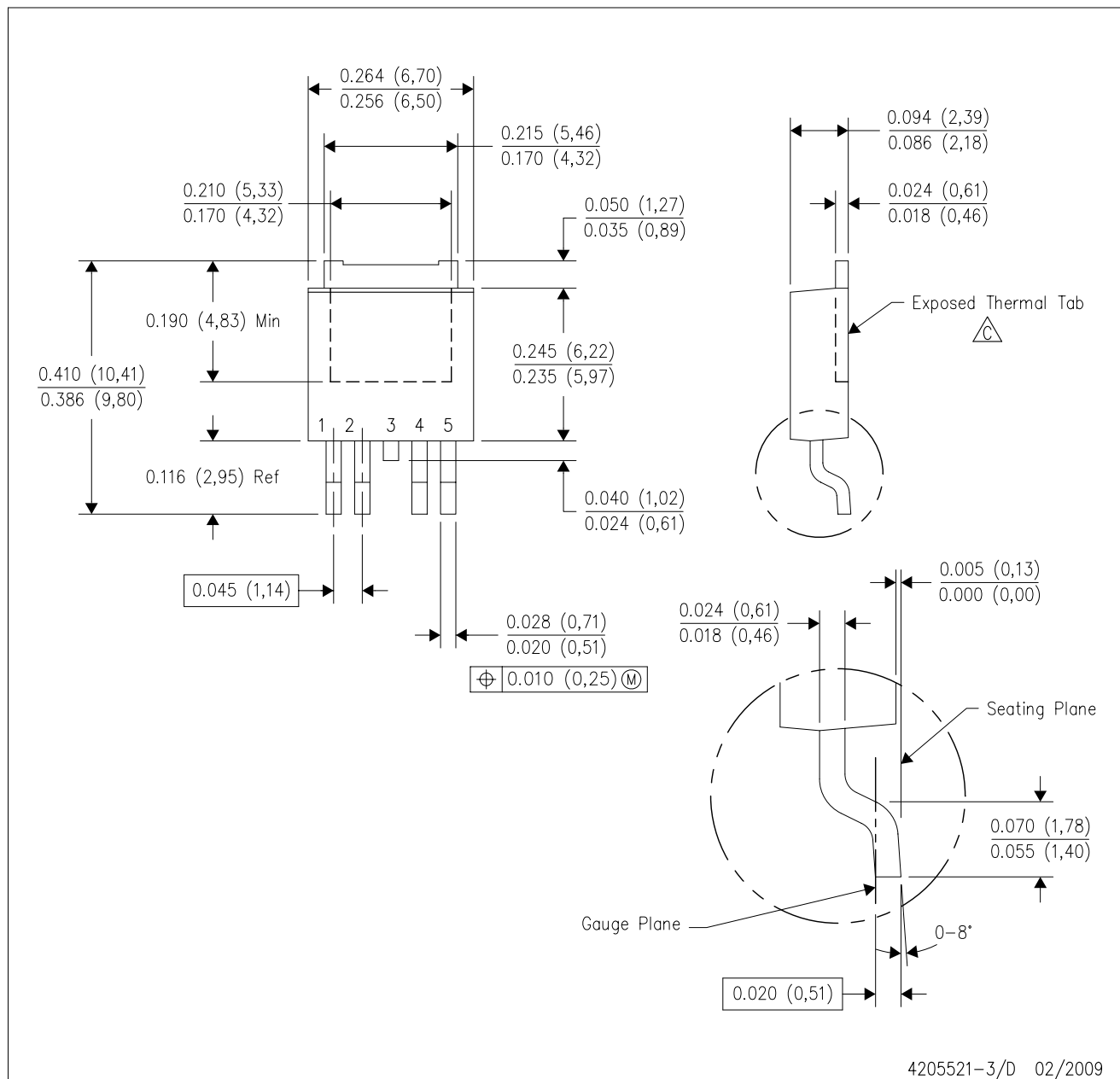
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

KVU (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

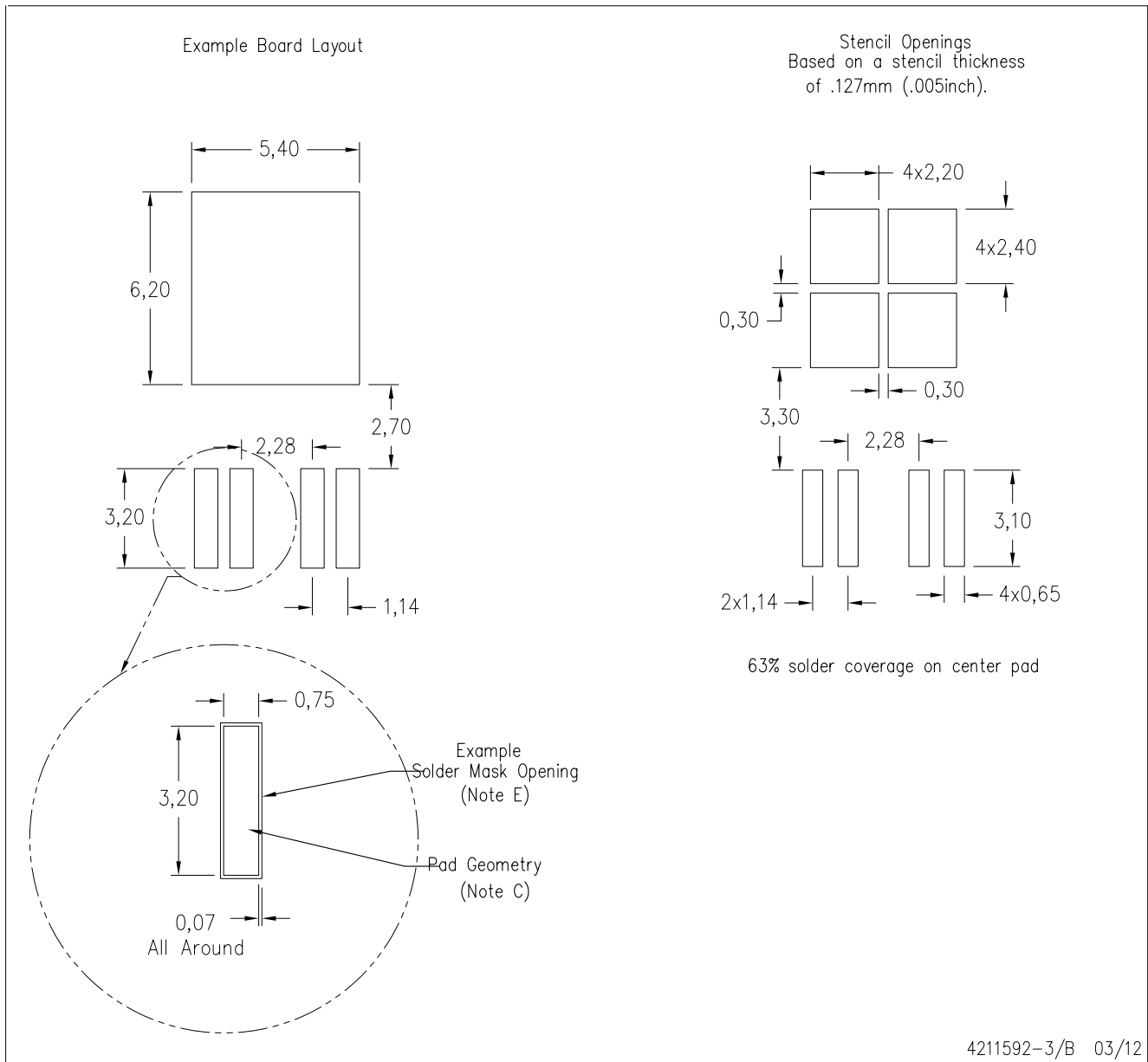


NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO-252 variation AD.

KVU (R-PSFM-G5)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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