

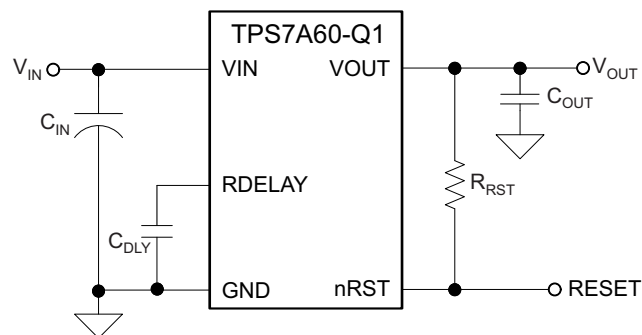
TPS7A6x-Q1 300mA、40V、静止電流25 μ Aの低ドロップアウト・レギュレータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
 - 温度グレード 1: -40°C ~ 125°C, T_A
 - 接合部温度: -40°C ~ 150°C, T_J
- 低いドロップアウト電圧:
 - $I_{OUT} = 150mA$ で 300mV
- 7V ~ 40V の広い入力電圧範囲、最大 45V の過渡電圧に対応
- 最大出力電流: 300mA
- 非常に低い静止電流
 - 軽負荷時に $I_{QUIESCENT} = 25\mu A$ (標準値)
 - ENABLE = LOW のとき $I_{SLEEP} < 2\mu A$
- 3.3V ~ 5V の固定出力電圧
- 低 ESR のセラミック出力安定コンデンサ
- パワーオン・リセット機能を搭載
 - 遅延をプログラム可能
 - オープン・ドレイン・リセット出力
- フォルト保護機能を搭載
 - 短絡保護と過電流保護
 - サーマル・シャットダウン
- 低い入力電圧のトラッキング
- 熱的に強化された Power パッケージ
 - 5ピン TO-263 (KTT, D2PAK)
 - 5ピン TO-252 (KVU, DPAK)

2 アプリケーション

- 車載用ヘッド・ユニット
- 車載センター情報ディスプレイ
- ハイブリッド・インストルメント・クラス
プログラム可能なリセット遅延オプション



3 概要

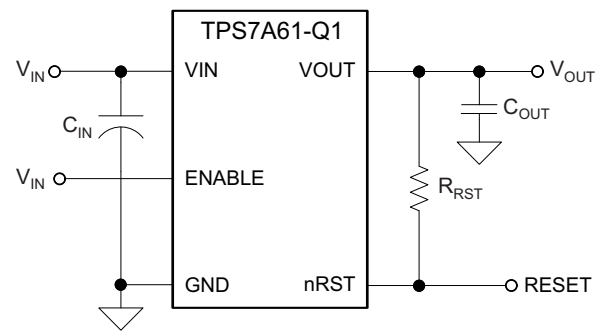
TPS7A60-Q1およびTPS7A61-Q1は、低ドロップアウトのリニア電圧レギュレータのファミリーで、消費電力が低く、軽負荷アプリケーションで静止電流が25 μ A未満に設計されています。これらのデバイスには過電流保護機能が搭載されており、低ESRのセラミック・コンデンサでも安定して動作するように設計されています。パワー・オン・リセット遅延が実装されており、デバイスのスタートアップ時に出力電圧が安定し、レギュレートされていることを示します。パワー・オン・リセット遅延は固定(標準値250 μ s)で、外付けコンデンサによってプログラムすることもできます。低電圧トラッキング機能により、小型の入力コンデンサを使用でき、コールド・クランク状況では多くの場合に昇圧コンバータが不要になります。これらの機能から、これらのデバイスは各種の車載アプリケーション用の電源に最適です。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS7A6033-Q1	TO-263 (5)	10.16mm×9.15mm
	TO-252 (5)	6.10mm×6.60mm
TPS7A6050-Q1	TO-263 (5)	10.16mm×9.15mm
	TO-252 (5)	6.10mm×6.60mm
TPS7A6133-Q1	TO-252 (5)	6.10mm×6.60mm
TPS7A6150-Q1	TO-252 (5)	6.10mm×6.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

イネーブル・オプション



目次

1	特長	1	8.3	Feature Description	13
2	アプリケーション	1	8.4	Device Functional Modes	17
3	概要	1	9	Application and Implementation	18
4	改訂履歴	2	9.1	Application Information	18
5	Device Comparison Table	4	9.2	Typical Applications	18
6	Pin Configuration and Functions	5	10	Power Supply Recommendations	22
7	Specifications	6	11	Layout	22
7.1	Absolute Maximum Ratings	6	11.1	Layout Guidelines	22
7.2	ESD Ratings	6	11.2	Layout Examples	25
7.3	Recommended Operating Conditions	6	12	デバイスおよびドキュメントのサポート	27
7.4	Thermal Information	7	12.1	関連リンク	27
7.5	Electrical Characteristics	7	12.2	ドキュメントの更新通知を受け取る方法	27
7.6	Switching Characteristics	8	12.3	コミュニティ・リソース	27
7.7	Typical Characteristics	9	12.4	商標	27
8	Detailed Description	12	12.5	静電気放電に関する注意事項	27
8.1	Overview	12	12.6	Glossary	27
8.2	Functional Block Diagrams	12	13	メカニカル、パッケージ、および注文情報	27

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision I (May 2018) から Revision J に変更	Page
• AEC-Q100 の「特長」項目を新標準に合わせて 変更	1
• ドキュメント全体で入力電圧範囲を 11V から 7V に 変更	1
• 「アプリケーション」セクションを 変更	1
• Added footnote to V_{IN} row in <i>Recommended Operating Conditions</i> table	6
• Added footnote to V_{IN} row in <i>Electrical Characteristics</i> table	7

Revision H (March 2016) から Revision I に変更	Page
• デバイス名を TPS7A6033-Q1、TPS7A6050-Q1、TPS7A6133-Q1、TPS7A6150-Q1 から TPS7A60-Q1 および TPS7A61-Q1 に 変更	1
• 4 番目の「特長」項目で 4V を 11V に 変更	1
• Changed V_{IN} minimum specification from 4 V to 11 V in <i>Recommended Operating Conditions</i> table	6
• Changed V_{IN} and V_{ENABLE} parameters to be separate rows, changed V_{ENABLE} description to <i>Enable pin voltage</i>	6
• Changed V_{IN} parameter: condensed test conditions to one row and changed minimum specification from 5.3 V to 11 V ...	7
• Changed 4 V (3.3-V version) or 5.3 V (5-V version) to 11 V in <i>Regulation Mode</i> section	17
• Changed <i>Input voltage range</i> parameter example value in <i>TPS7A60-Q1 Design Parameters</i> table	18
• Changed <i>Input voltage range</i> parameter example value in <i>TPS7A61-Q1 Design Parameters</i> table	20

Revision G (April 2012) から Revision H に変更	Page
• 「特長」一覧の最初に新項目を追加	1
• データシート全体を通して、多くの場所で型番に「-Q1」を追加	1
• 「ESD 定格」表、「スイッチング特性」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• Added MIN values for V_{IN} , R_{DELAY} , and V_{OUT} in <i>Absolute Maximum Ratings</i> table	6
• Deleted two graphs from the <i>Typical Characteristics</i> section	9

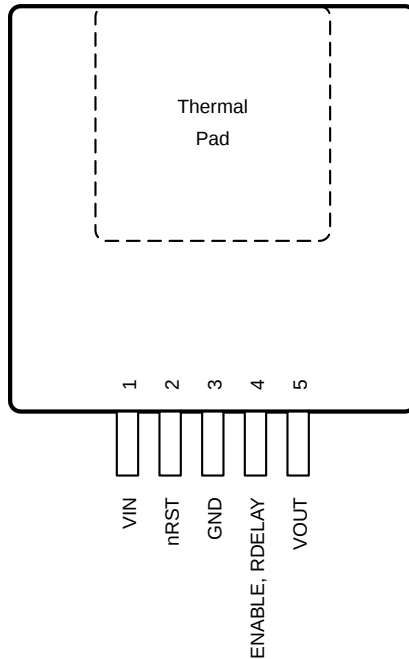
• Updated Typical Application Schematic for the TPS7A61xx-Q1 Device image.	20
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5 Device Comparison Table

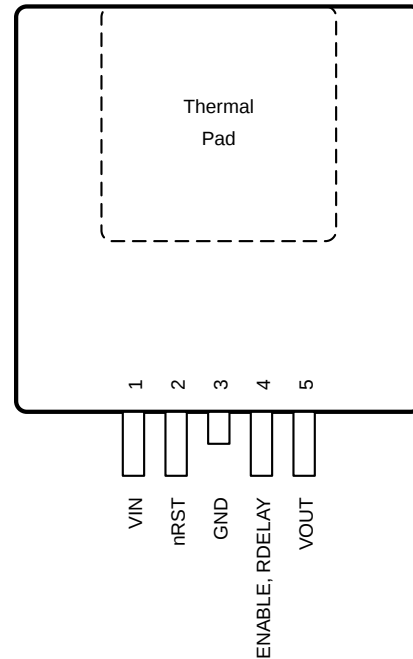
PART NUMBER	OUTPUT VOLTAGE	ENABLE	RESET	PROGRAMMABLE RESET DELAY
TPS7A6033-Q1	3.3 V	No	Yes	Yes
		No	Yes	Yes
TPS7A6050-Q1	5 V	No	Yes	Yes
		No	Yes	Yes
TPS7A6133-Q1	3.3 V	Yes	Yes	No
TPS7A6150-Q1	5 V	Yes	Yes	No

6 Pin Configuration and Functions

KTTPackage
5-Pin TO-263 With Exposed Thermal Pad
Top View



KVUPackage
5-Pin TO-252 With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ENABLE	4	I	Enable pin (for TPS7A61-Q1 only): This is a high-voltage-tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. This input can be connected to the VIN pin for self-bias applications. If this pin is not connected, the device stays disabled.
GND	3	I/O	Ground pin: This is the signal-ground pin of the IC.
nRST	2	O	Reset pin: This is an output pin with an external pullup resistor connected to the VOUT pin.
RDELAY	4	O	Reset delay timer pin (for TPS7A60-Q1 only): This pin is used to program the reset delay timer using an external capacitor (C_{DLV}) to ground.
VIN	1	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between the VIN pin and the GND pin to dampen input line transients.
VOUT	5	O	Regulated output-voltage pin: This is a regulated voltage output ($V_{OUT} = 3.3\text{ V}$ or 5 V , as applicable) pin with a limitation on maximum output current. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and the GND pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Unregulated inputs ⁽²⁾	VIN, ENABLE	–0.3	45	V
Regulated output	VOUT	–0.3	7	V
Open-drain reset output	nRST	–0.3	7	V
Output to charge an external capacitor	RDELAY	–0.3	7	V
Operating ambient temperature, T _J		–40	150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum voltage for duration less than 480 ms

7.2 ESD Ratings

			VALUE	UNIT
TPS7A60-Q1 and TPS7A61-Q1 Devices in KVV Package				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
TPS7A60-Q1 Device in KTT Package				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	7 ⁽¹⁾	40	V
V _{ENABLE}	Enable pin voltage ⁽²⁾	4	40	V
V _{nRST} , V _{RDELAY}	Low-voltage output range ⁽³⁾	0	5.25	V
I _{OUT}	Output current	0	300	mA
T _A	Operating ambient temperature	–40	150	°C

- (1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.
- (2) Applicable for the TPS7A61-Q1 only.
- (3) Applicable for the TPS7A60-Q1 only.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS7A60-Q1, TPS7A61-Q1	TPS7A60-Q1	UNIT
		KVU (TO-252)	KTT (TO-263)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	26.9	24.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	32.2	38.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	6.5	7.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	2.5	3.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	6.5	7.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.8	1.5	°C/W

- (1) The thermal data is based on JEDEC standard high K profile JESD 51-5. The copper pad is soldered to the thermal land pattern. The correct attachment procedure must be incorporated.
- (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

V_{IN} = 14 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN PIN)						
V _{IN}	Input voltage	Fixed 5-V or 3.3-V output, I _{OUT} = 1 mA	7 ⁽¹⁾		40	V
I _{QUIESCENT}	Quiescent current	V _{IN} = 8.2 V to 18 V, V _{ENABLE} ⁽²⁾ = 5 V, I _{OUT} = 0.01 mA to 0.75 mA		25	40	μA
I _{SLEEP} ⁽²⁾	Sleep or shutdown current	V _{IN} = 8.2 V to 18 V, V _{ENABLE} ⁽²⁾ < 0.8 V, I _{OUT} = 0 mA (no load), T _A = 125°C			3	μA
V _{IN-UVLO}	Undervoltage lockout voltage	Ramp V _{IN} down until output is turned OFF		3.16		V
V _{IN(POWERUP)}	Power-up voltage	Ramp V _{IN} up until output is turned ON		3.45		V
ENABLE INPUT (ENABLE PIN)						
V _{IL} ⁽²⁾	Logic input low level		0		0.8	V
V _{IH} ⁽²⁾	Logic input high level		2.5		40	V
REGULATED OUTPUT VOLTAGE (VOUT PIN)						
V _{OUT}	Regulated output voltage	Fixed V _{OUT} value (3.3 V or 5 V as applicable), I _{OUT} = 10 mA to 300 mA, V _{IN} = V _{OUT} + 1 V to 16 V	–2%		2%	
ΔV _{LINE-REG}	Line regulation	V _{IN} = 6 V to 28 V, I _{OUT} = 10 mA, V _{OUT} = 5 V			15	mV
		V _{IN} = 6 V to 28 V, I _{OUT} = 10 mA, V _{OUT} = 3.3 V			20	mV
ΔV _{LOAD-REG}	Load regulation	I _{OUT} = 10 mA to 300 mA, V _{IN} = 14 V, V _{OUT} = 5 V			25	mV
		I _{OUT} = 10 mA to 300 mA, V _{IN} = 14 V, V _{OUT} = 3.3 V			35	mV
V _{DROPOUT} ⁽³⁾	Dropout voltage (V _{IN} – V _{OUT})	I _{OUT} = 250 mA			500	mV
		I _{OUT} = 150 mA			300	mV
R _{SW}	Switch resistance	V _{IN} to V _{OUT} resistance			2	Ω
I _{CL}	Output current limit	V _{OUT} = 0 V (V _{OUT} pin is shorted to ground)	350		1000	mA
PSRR	Power supply ripple rejection	V _{IN-RIPPLE} = 0.5 V _{pp} , I _{OUT} = 300 mA, frequency = 100 Hz, V _{OUT} = 5 V and V _{OUT} = 3.3 V		60		dB
		V _{IN-RIPPLE} = 0.5 V _{pp} , I _{OUT} = 300 mA, frequency = 150 kHz, V _{OUT} = 5 V and V _{OUT} = 3.3 V		30		
RESET (nRST PIN)						
V _{OL}	Reset pulled low	I _{OL} = 5 mA			0.4	V
I _{OH}	Leakage current	Reset pulled to V _{OUT} through 5-kΩ resistor			1	μA

- (1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.
- (2) Applicable for the TPS7A61-Q1 only.
- (3) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (3.3 V or 5 V) drops by 100 mV at specified loads.

Electrical Characteristics (continued)

 $V_{IN} = 14\text{ V}$, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{TH(POR)}	Power-on-reset threshold	V _{OUT} power up above internally set tolerance, V _{OUT} = 5 V	4.5	4.65	4.77	V
		V _{OUT} power up above internally set tolerance, V _{OUT} = 3.3 V		3.07		
UV _{THRES}	Reset threshold	V _{OUT} falling below internally set tolerance, V _{OUT} = 5 V	4.5	4.65	4.77	V
		V _{OUT} falling below internally set tolerance, V _{OUT} = 3.3 V		3.07		
RESET DELAY (RDELAY PIN)						
V _{TH(RDELAY)} ⁽⁴⁾	Threshold to release nRST high	Voltage at RDELAY pin is ramped up.		3	3.3	V
I _{DLY} ⁽⁴⁾	Delay capacitor charging current		0.75	1	1.25	μA
I _{OL} ⁽⁴⁾	Delay capacitor discharging current	Voltage at RDELAY pin = 1 V	5			mA
OPERATING TEMPERATURE RANGE						
T _J	Operating junction temperature		−40		150	°C
T _{SHUTDOWN}	Thermal shutdown trip point			165		°C
T _{HYST}	Thermal shutdown hysteresis			10		°C

(4) Applicable for the TPS7A60-Q1 only.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET (nRST PIN)						
t_{POR}	Power-on-reset delay	$C_{DLY} = 100\text{ pF}$		300		μs
		$C_{DLY} = 100\text{ nF}$		300		ms
$t_{POR-PRESET}$	Internally preset power-on-reset delay	C_{DLY} not connected in TPS7A60xx or not available in TPS7A61xx, $V_{OUT} = 5\text{ V}$ and $V_{OUT} = 3.3\text{ V}$		250		μs
$t_{DEGLITCH}$	Reset deglitch time			5.5		μs

7.7 Typical Characteristics

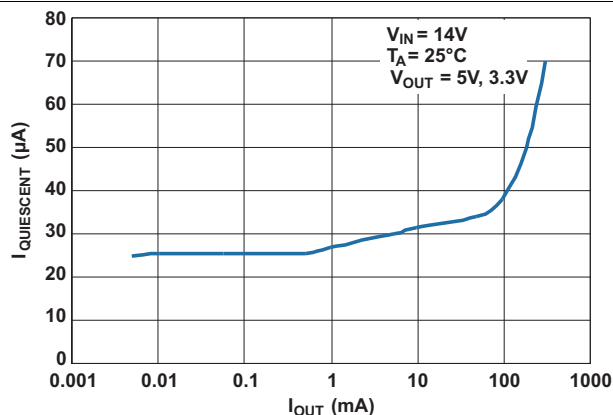


Figure 1. Quiescent Current vs Load Current

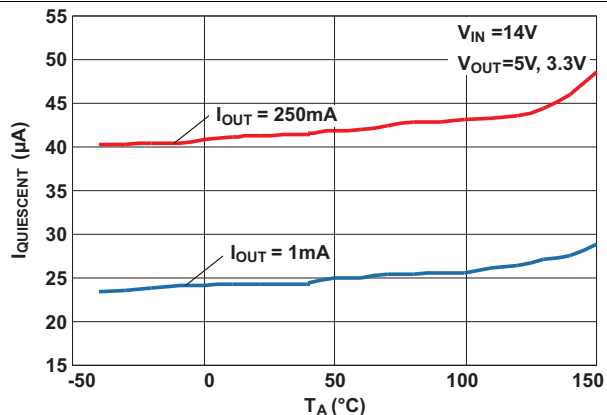


Figure 2. Quiescent Current vs Ambient Air Temperature

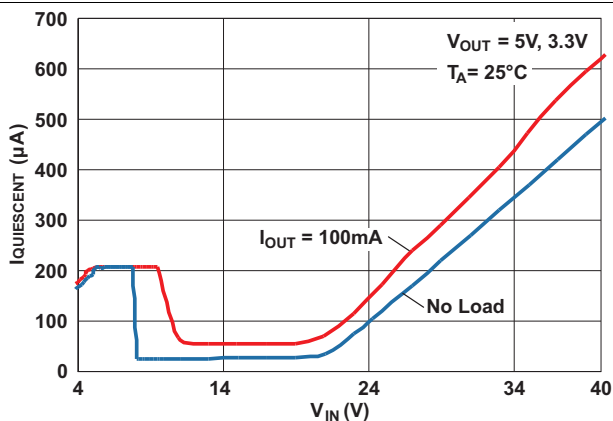


Figure 3. Quiescent Current vs Input Voltage

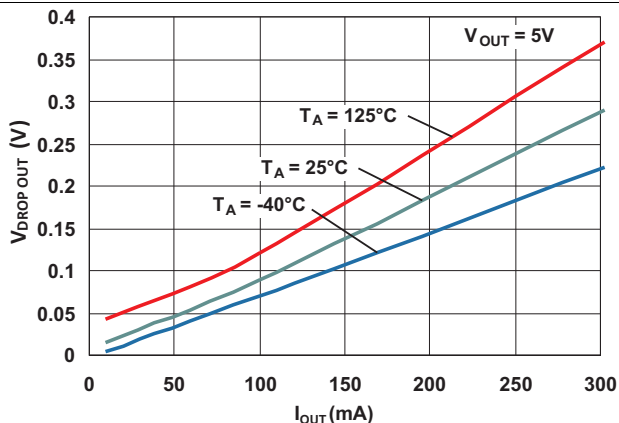


Figure 4. Dropout Voltage ⁽¹⁾ vs Load Current

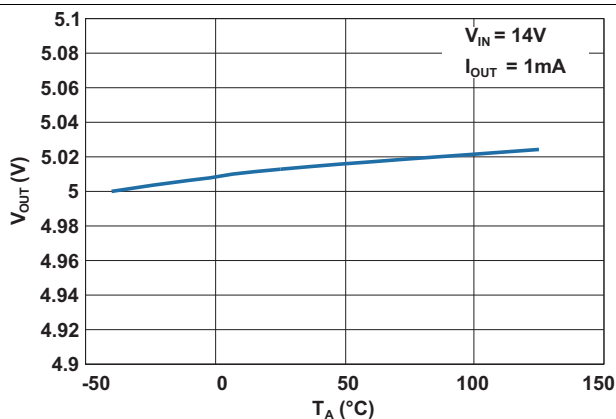


Figure 5. Output Voltage vs Ambient Air Temperature

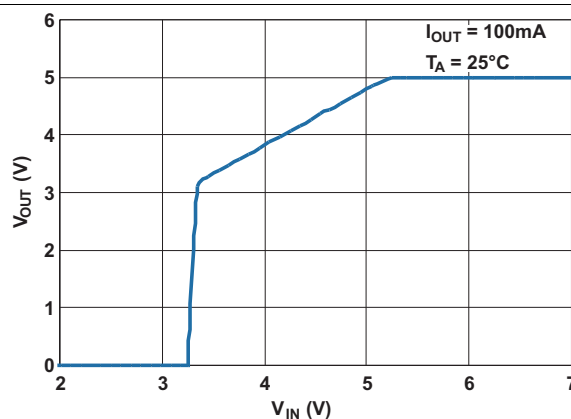


Figure 6. Output Voltage vs Input Voltage

(1) Dropout voltage is measured when the output voltage drops by 100 mV from the regulated output voltage level. (For example, dropout voltage for the TPS7A6050-Q1 is measured when the output voltage drops down to 4.9 V from 5 V.)

Typical Characteristics (continued)

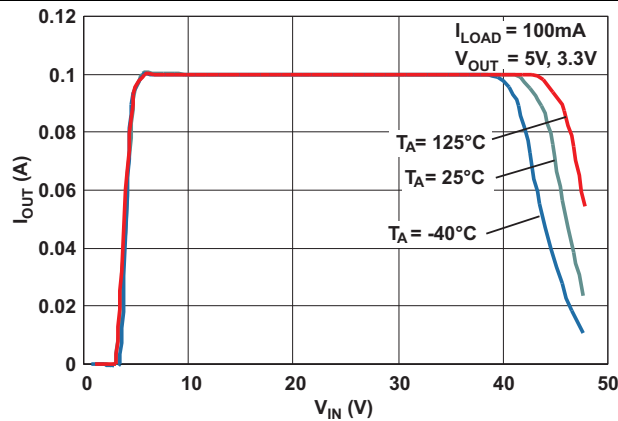


Figure 7. Output Voltage vs Input Voltage

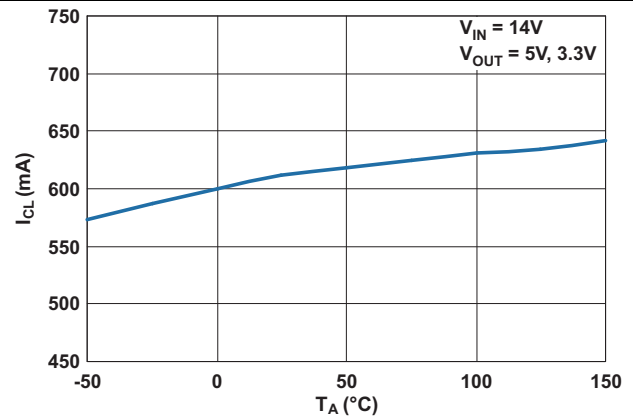


Figure 8. Output Current Limit vs Ambient Air Temperature

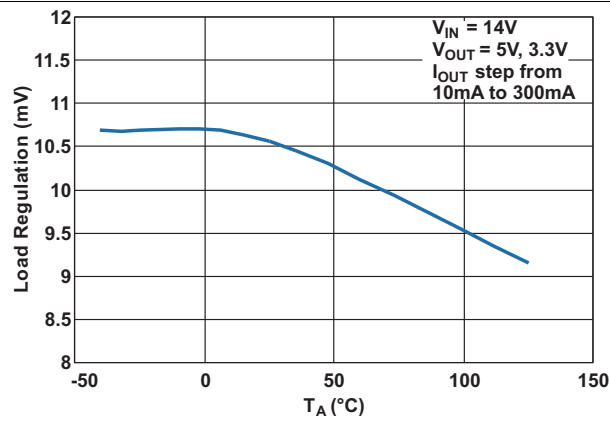


Figure 9. Load Regulation vs Ambient Air Temperature

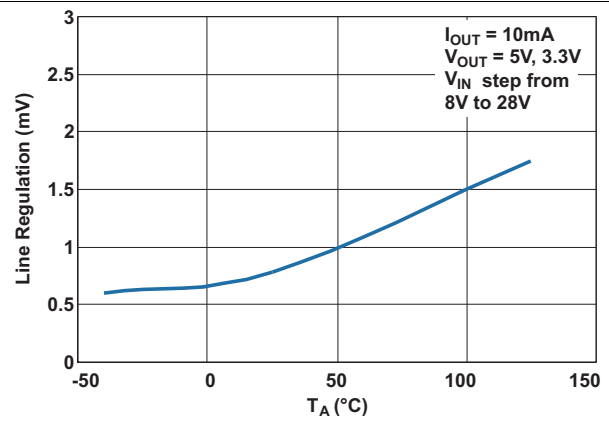


Figure 10. Line Regulation vs Ambient Air Temperature

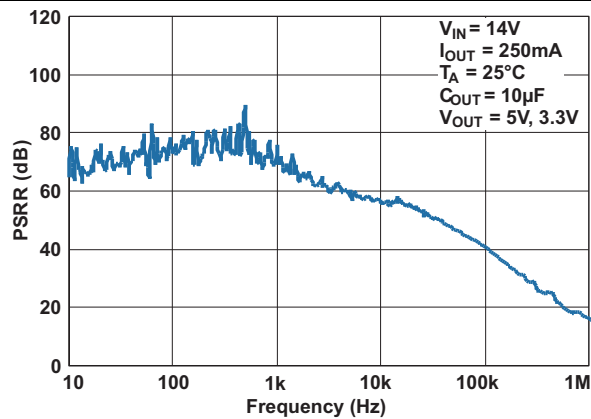


Figure 11. PSRR at Heavy Load Current

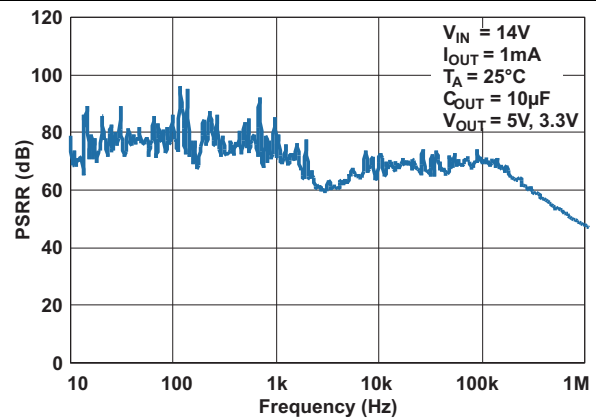
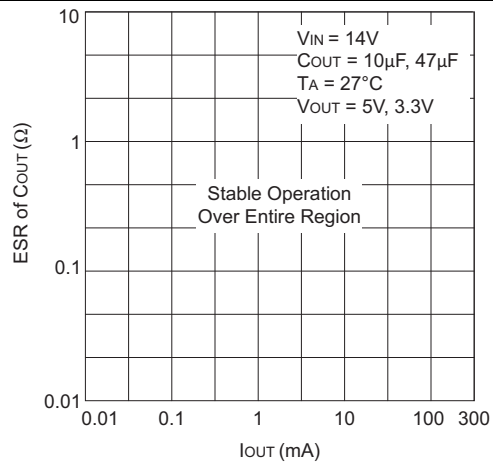


Figure 12. PSRR at Light Load Current

Typical Characteristics (continued)



**Figure 13. ESR Stability vs Load Current
for TPS7A60-Q1 and TPS7A61-Q1**

Functional Block Diagrams (continued)

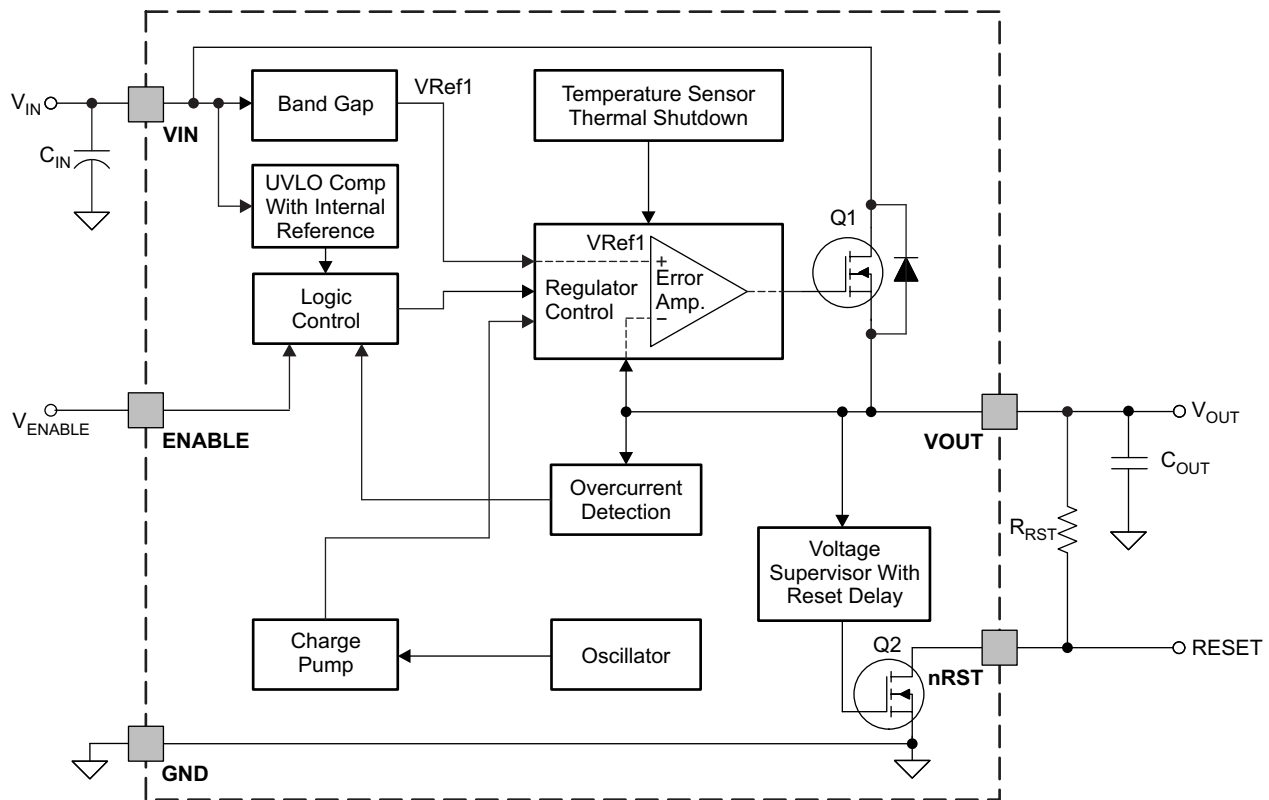


Figure 15. TPS7A61-Q1 Functional Block Diagram

8.3 Feature Description

The following section describes the features of TPS7A60-Q1 and TPS7A61-Q1 voltage regulators in detail.

8.3.1 Reset Delay and Reset Output

Reset delay is implemented when the device starts up to indicate that output voltage is stable and in regulation, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration. The reset-delay timer is initialized when the voltage at the output (V_{OUT}) exceeds 93% of the regulated output voltage (3.3 V or 5 V, as applicable). The reset output ($nRST$) is asserted high after the power-on-reset delay (t_{POR}) has elapsed. If the regulated output voltage falls below 93% of the set level, $nRST$ is asserted low after a short de-glitch time of approximately 5.5 μs (typical).

For TPS7A60-Q1 devices, the reset-delay time can be programmed by connecting an external capacitor (C_{DLY}) to the RDELAY pin. The delay time is given by Equation 1:

$$t_{POR} = \frac{C_{DLY} \times 3}{1 \times 10^{-6}}$$

where

- t_{POR} = reset delay time in seconds
- C_{DLY} = reset delay capacitor value in farads, 100 pF to 100 nF

In TPS7A61xx devices, there is no RDELAY pin, and the reset-delay time is preset internally (250 μs typical).

Feature Description (continued)

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{IN(POWERUP)}$) level, the output voltage begins to ramp as shown in Figure 16 and Figure 17. When the output voltage reaches the power-on-reset threshold ($V_{TH(POR)}$) level, a constant output current charges an external capacitor (C_{DLY}) to an internal threshold ($V_{TH(RDELAY)}$) voltage level. Then, $nRST$ is asserted high and C_{DLY} is discharged through an internal load. This allows C_{DLY} to charge from approximately 0 V during the next power cycle. If no external capacitor is connected, the delay time is preset internally. This is shown in Figure 16.

In TPS7A60-Q1 devices, if the C_{DLY} capacitor is not connected to the RDELAY pin, the reset-delay time is set internally. This is shown in Figure 17.

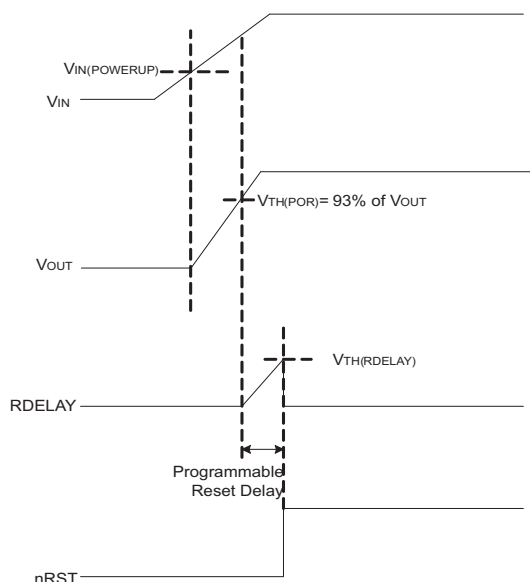


Figure 16. Power Up and Reset-Delay Function With the C_{DLY} Capacitor Connected to the RDELAY Pin for TPS7A60-Q1

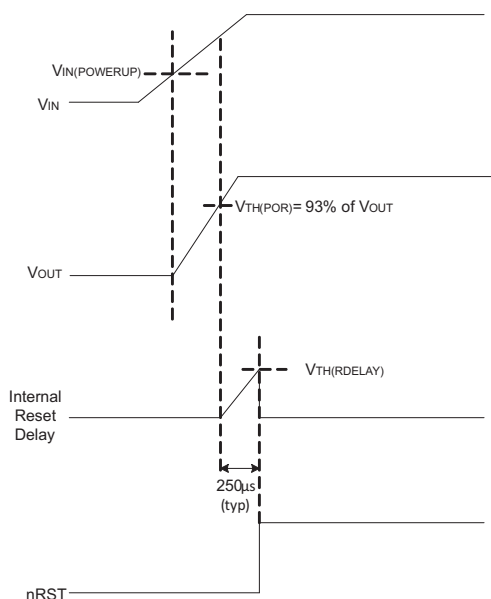


Figure 17. Power Up and Reset Delay Function With the C_{DLY} Capacitor Not Connected or Available in TPS7A60-Q1 and TPS7A61-Q1, Respectively

Feature Description (continued)

In case of negative transients in the input voltage (V_{IN}), the reset signal is asserted low only if the output (V_{OUT}) drops and stays below the reset threshold level ($V_{TH(POR)}$) for more than the de-glitch time ($t_{DEGLITCH}$). This is shown in Figure 18.

While $nRST$ is low, if the input voltage returns to the nominal operating voltage, the normal power-up sequence is followed. $nRST$ is asserted high, only if the output voltage exceeds the reset-threshold voltage ($V_{TH(POR)}$) and the reset-delay time (t_{POR}) has elapsed. This is shown in the shaded region of Figure 18.

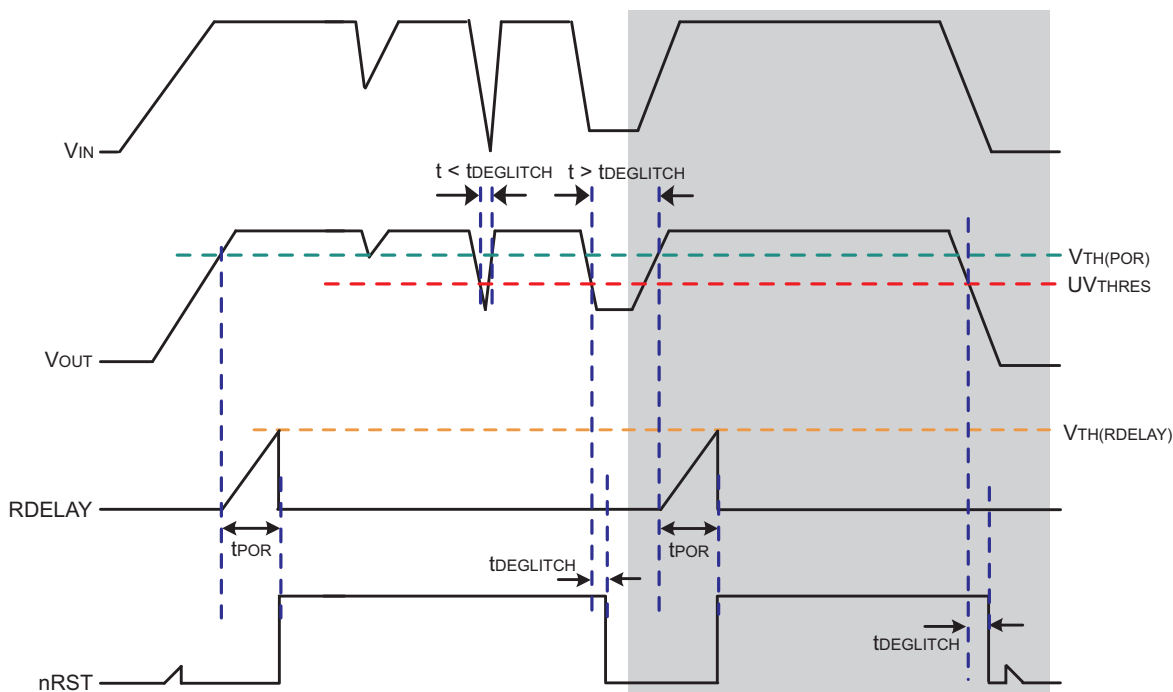


Figure 18. Conditions for Activation of Reset

8.3.2 Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge-pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input-voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge-pump switching thresholds are hysteretic. Figure 19 and Figure 20 show typical switching thresholds for the charge pump at light ($I_{OUT} < \text{approximately } 2 \text{ mA}$) and heavy ($I_{OUT} > \text{approximately } 2 \text{ mA}$) loads, respectively.

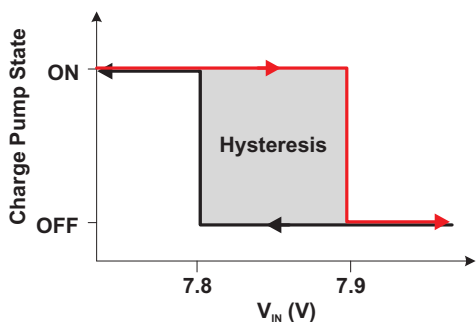


Figure 19. Charge Pump Operation at Light Loads

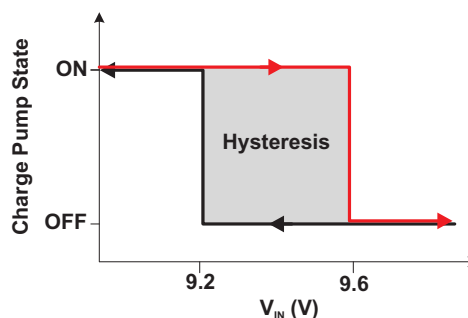


Figure 20. Charge Pump Operation at Heavy Loads

Feature Description (continued)

8.3.3 Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$). This ensures that the regulator is not latched into an unknown state during low-input-voltage conditions. The regulator powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ level.

8.3.4 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks the input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

8.3.5 Integrated Fault Protection

These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to keep them in a safe area of operation during certain fault conditions, internal current-limit protection and current-limit foldback are used to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output, current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

8.3.6 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output is turned off. When the junction temperature falls below the TSD trip point, the output is turned on again. This is shown in [Figure 21](#).

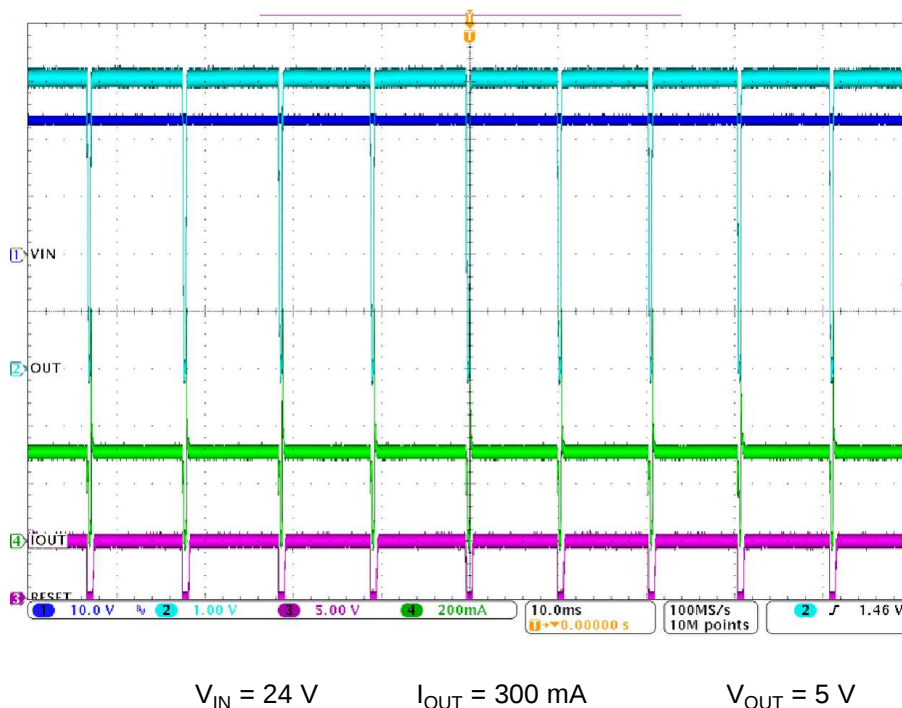


Figure 21. Thermal Cycling Waveform for the TPS7A6150-Q1

8.4 Device Functional Modes

8.4.1 Low-Power Mode

At light loads and high input voltages ($V_{IN} >$ approximately 8 V such that charge pump is off), the device operates in low-power mode and the quiescent current consumption is reduced to 25 μ A (typical) as shown in [Table 1](#).

Table 1. Typical Quiescent Current Consumption

I_{OUT}	CHARGE PUMP ON	CHARGE PUMP OFF
$I_{OUT} <$ approximately 2 mA (light load)	250 μ A	25 μ A (low-power mode)
$I_{OUT} >$ approximately 2 mA (heavy load)	280 μ A	70 μ A

8.4.2 Sleep Mode (TPS7A61-Q1 Only)

The enable falling edge is 0.8 V (minimum). The device operates in the sleep mode by holding the ENABLE pin below that voltage, and the quiescent current consumption is reduced to 3 μ A (maximum) as shown in [Electrical Characteristics](#).

8.4.3 Regulation Mode

When the input voltage is above 7 V, with the ENABLE pin pulled higher than 2.5 V, the device operates in regulation mode and outputs the nominal voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A60-Q1 and TPS7A61-Q1 devices are 300-mA low-dropout linear regulators designed for up to 40-V V_{IN} operation with only 25- μ A quiescent current at no load. There are specific EVMs designed for these devices to enable evaluation of all the functions of the devices. Both the EVM and its user guide are available on the product folder as well.

9.2 Typical Applications

Figure 22 and Figure 24 show typical application circuits for the TPS7A60-Q1 and TPS7A61-Q1, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

9.2.1 TPS7A60-Q1 Typical Application

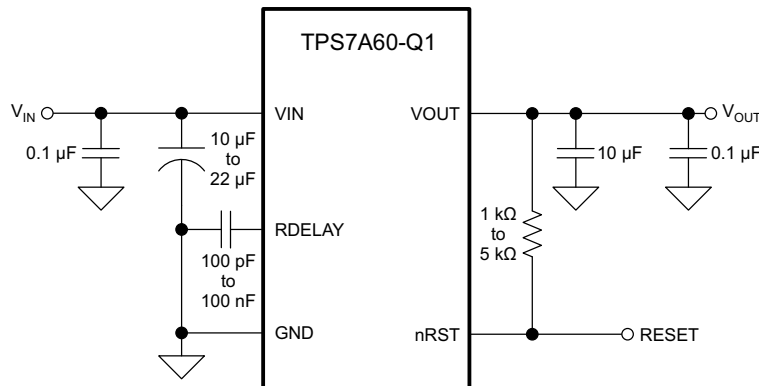


Figure 22. Typical Application Schematic for the TPS7A60-Q1 Device

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. TPS7A60-Q1 Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7 V to 40 V
Output voltage	3.3 V (for TPS7A6033-Q1) or 5 V (for TPS7A6050-Q1)
Output current rating	300 mA
Output capacitor range	10 μ F to 47 μ F
Output-capacitor ESR range	10 m Ω to 10 Ω
RESET-delay capacitor range	100 pF to 100 nF

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

9.2.1.2.1 Input Capacitor

The device requires an input bypass capacitor, the value of which depends on the application. The typical recommended value for the bypass capacitor is 10 μ F. The voltage rating must be greater than the maximum input voltage.

9.2.1.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. TI recommends selecting a capacitor between 10 μ F and 47 μ F with ESR range from 10 m Ω to 10 Ω .

9.2.1.3 Application Curve

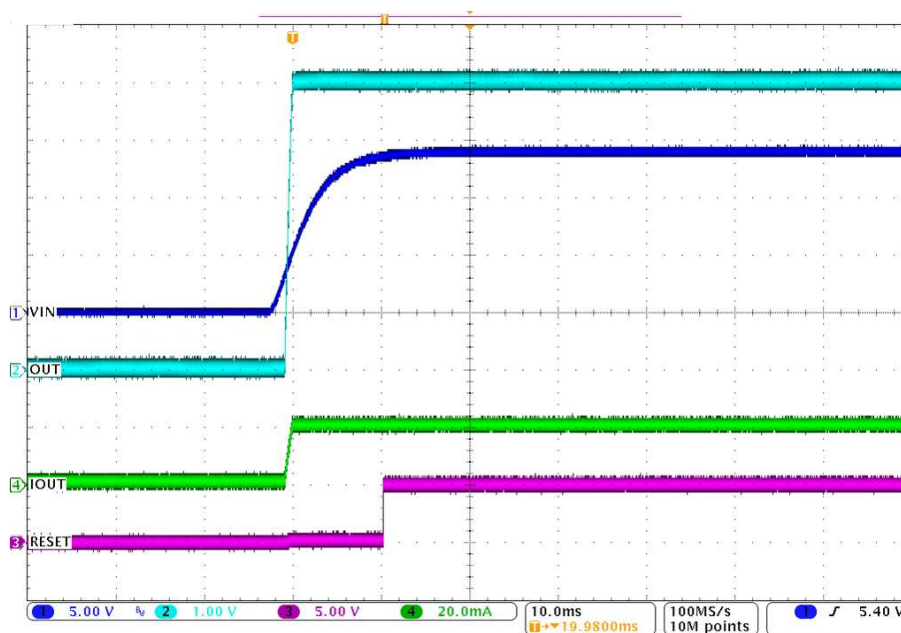


Figure 23. Power Up ($V_{OUT} = 5$ V) With 10-ms RESET Delay, 10 ms/div, $I_L = 20$ mA

9.2.2 TPS7A61-Q1 Typical Application

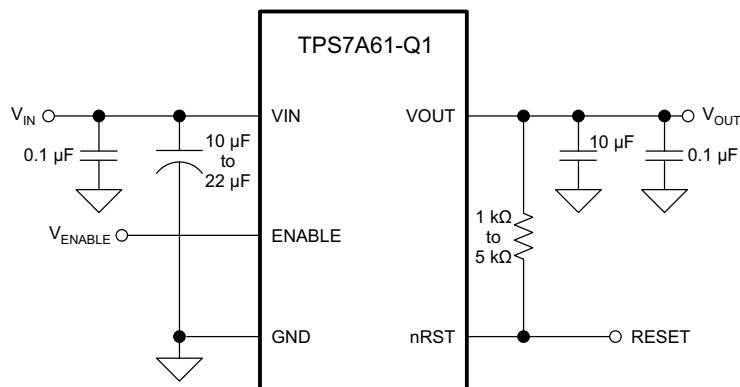


Figure 24. Typical Application Schematic for the TPS7A61-Q1 Device

9.2.2.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#).

Table 3. TPS7A61-Q1 Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7 V to 40 V
Output voltage	3.3 V (for TPS7A6133-Q1) or 5 V (for TPS7A6150-Q1)
Output current rating	300 mA
Output capacitor range	10 μF to 47 μF
Output-capacitor ESR range	10 mΩ to 10 Ω

9.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

9.2.2.3 Application Curve

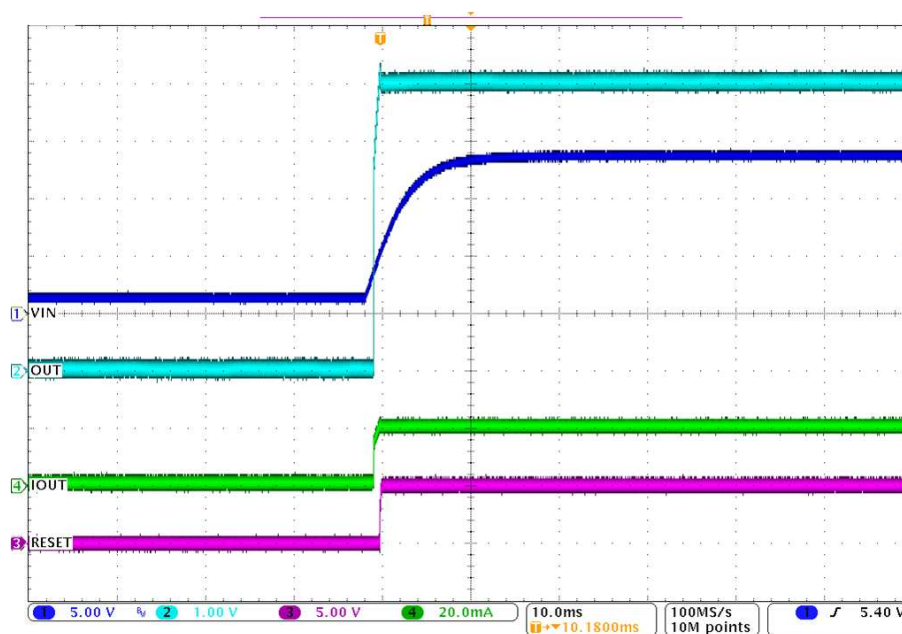


Figure 25. Power Up ($V_{OUT} = 5\text{ V}$), 10 ms/div, $I_L = 20\text{ mA}$

10 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A60-Q1 or TPS7A61-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 μ F and a ceramic bypass capacitor at the input.

11 Layout

11.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, it is recommended to spread the thermal pad as large as possible and put enough thermal vias on the thermal pad. [Figure 29](#) and [Figure 30](#) show an example layout.

11.1.1 Power Dissipation and Thermal Considerations

Power dissipated in the device can be calculated using [Equation 2](#).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN}$$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage
- $I_{QUIESCENT}$ = quiescent current

(2)

As $I_{QUIESCENT} \ll I_{OUT}$, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in [Equation 2](#) can be ignored.

For a device under operation at a given ambient air temperature (T_A), the junction temperature (T_J) can be calculated using [Equation 3](#).

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

- $R_{\theta JA}$ = junction-to-ambient-air thermal impedance

(3)

Layout Guidelines (continued)

The rise in junction temperature due to power dissipation can be calculated using [Equation 4](#).

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (4)$$

For a given maximum junction temperature (T_{J-Max}), the maximum ambient air temperature (T_{A-Max}) at which the device can operate can be calculated using [Equation 5](#).

$$T_{A-Max} = T_{J-Max} - (R_{\theta JA} \times P_D) \quad (5)$$

Example:

If $I_{OUT} = 100 \text{ mA}$, $V_{OUT} = 5 \text{ V}$, $V_{IN} = 14 \text{ V}$, $I_{QUIESCENT} = 250 \text{ }\mu\text{A}$ and $R_{\theta JA} = 30^\circ\text{C/W}$, the continuous power dissipated in the device is 0.9 W . The rise in junction temperature due to power dissipation is 27°C . For a maximum junction temperature of 150°C , maximum ambient air temperature at which the device can operate is 123°C .

For adequate heat dissipation, it is recommended to solder the thermal pad (exposed heat sink) to a thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Power derating curves for the TPS7A60-Q1 and TPS7A61-Q1 family of devices in the KTT (TO-263) and KVU (TO-252) packages are shown in [Figure 26](#).

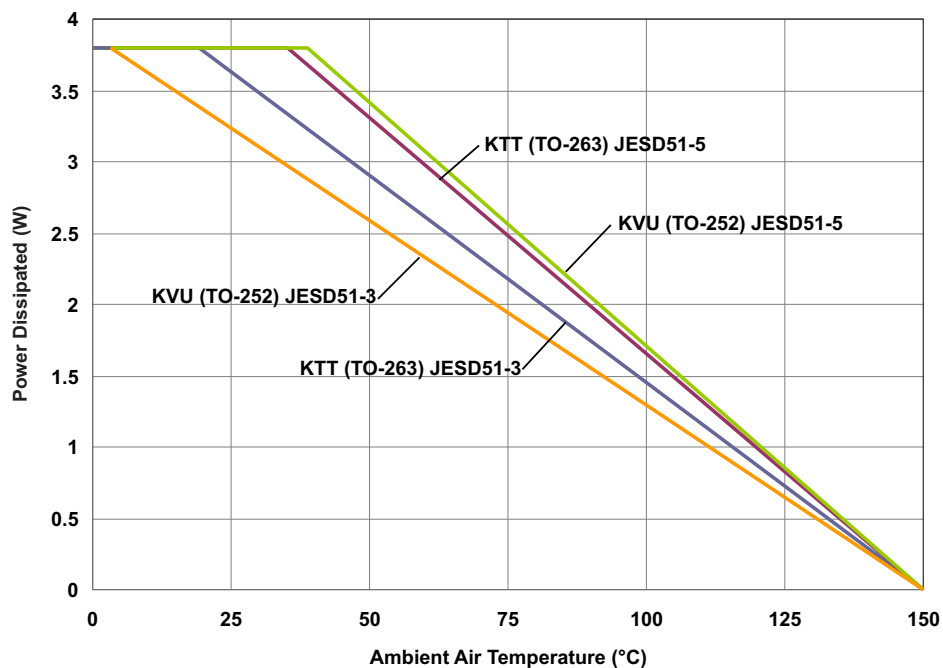


Figure 26. Power Derating Curves

For optimum thermal performance, TI recommends to use a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad. This is shown in [Figure 27](#) (a) and (b). Further, the heat-spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area.

Layout Guidelines (continued)

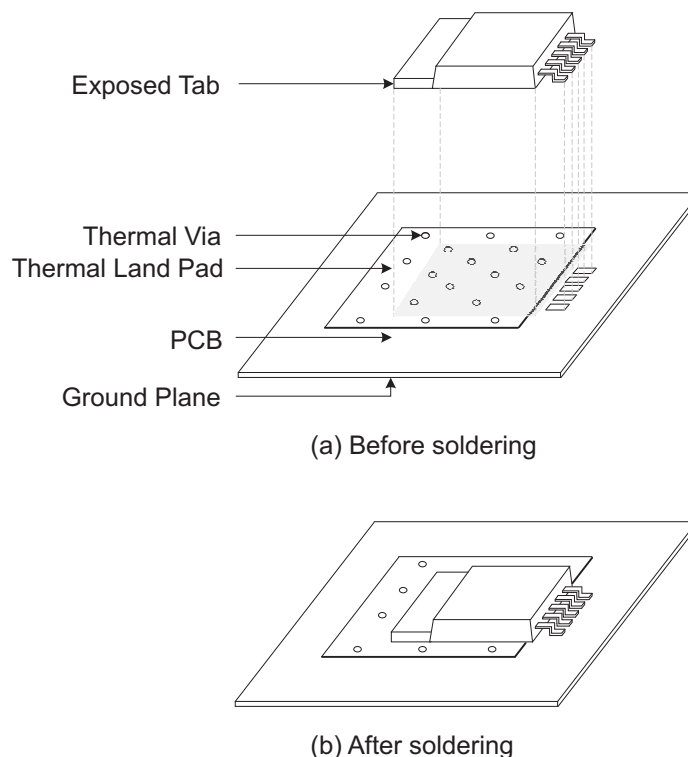


Figure 27. Using Multilayer PCB and Thermal Vias For Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 28 shows the variation of $R_{\theta JA}$ with surface area of the thermal land pad (soldered to the exposed pad) for KTT and KVV packages.

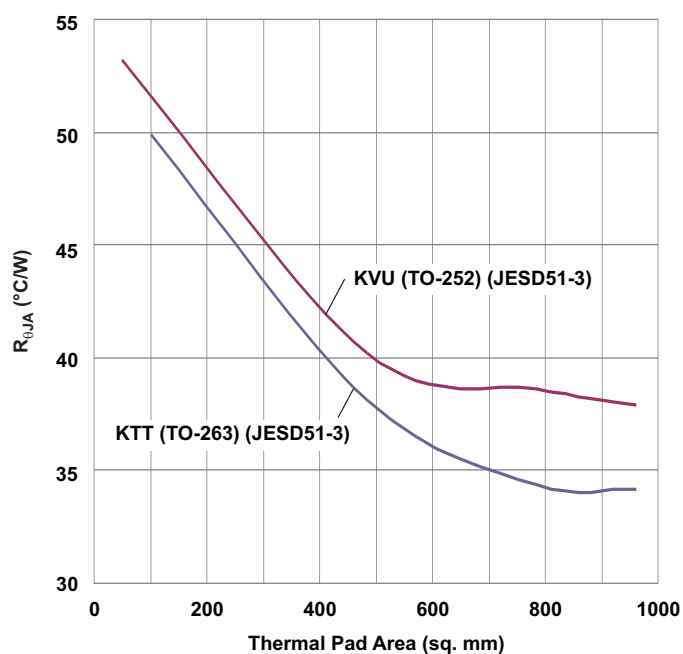


Figure 28. $R_{\theta JA}$ vs Thermal Pad Area

11.2 Layout Examples

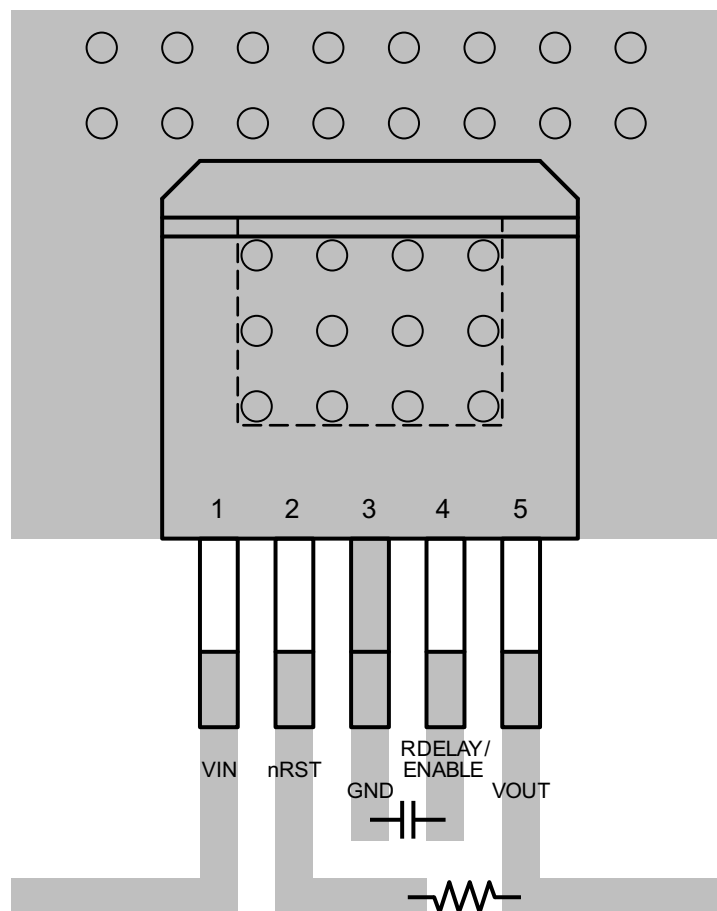


Figure 29. Layout Recommendation for 5-Pin KTT Package

Layout Examples (continued)

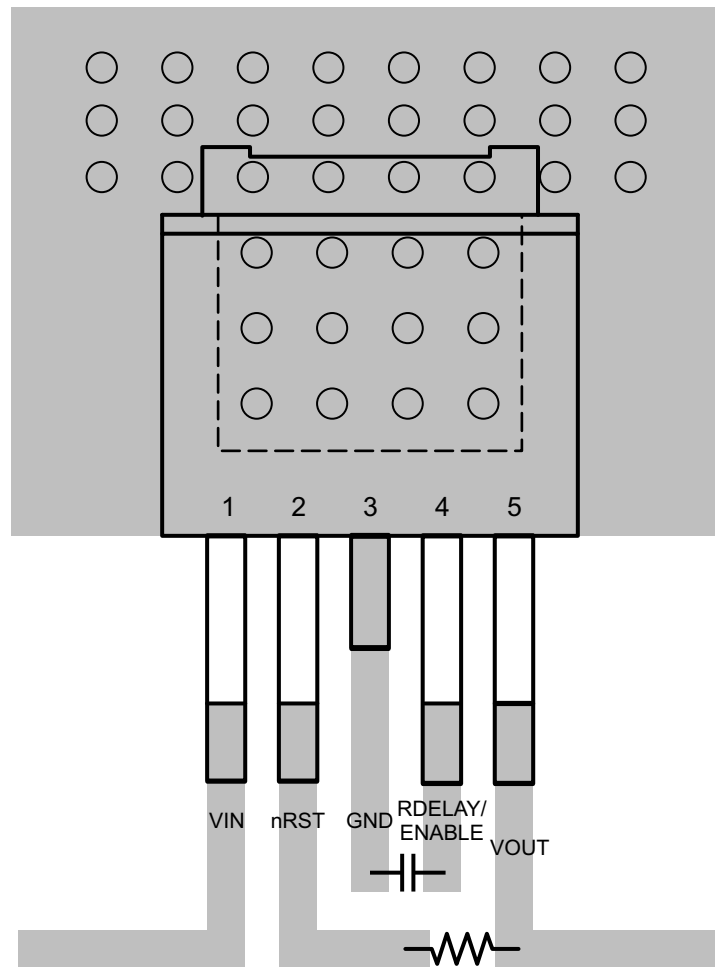


Figure 30. Layout Recommendation for 5-pin KVV package

12 デバイスおよびドキュメントのサポート

12.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS7A60-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS7A61-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6033QKTTRQ1	Active	Production	DDPAK/ TO-263 (KTT) 5	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	7A6033Q1
TPS7A6033QKTTRQ1.A	Active	Production	DDPAK/ TO-263 (KTT) 5	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	7A6033Q1
TPS7A6033QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6033Q1
TPS7A6033QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6033Q1
TPS7A6050QKTTRQ1	Active	Production	DDPAK/ TO-263 (KTT) 5	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	7A6050Q1
TPS7A6050QKTTRQ1.A	Active	Production	DDPAK/ TO-263 (KTT) 5	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	7A6050Q1
TPS7A6050QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6050Q1
TPS7A6050QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6050Q1
TPS7A6133QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6133Q1
TPS7A6133QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6133Q1
TPS7A6150QKVURQ1	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6150Q1
TPS7A6150QKVURQ1.A	Active	Production	TO-252 (KVU) 5	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6150Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6033QKTTRQ1	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A6033QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6050QKTTRQ1	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A6050QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6133QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6150QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

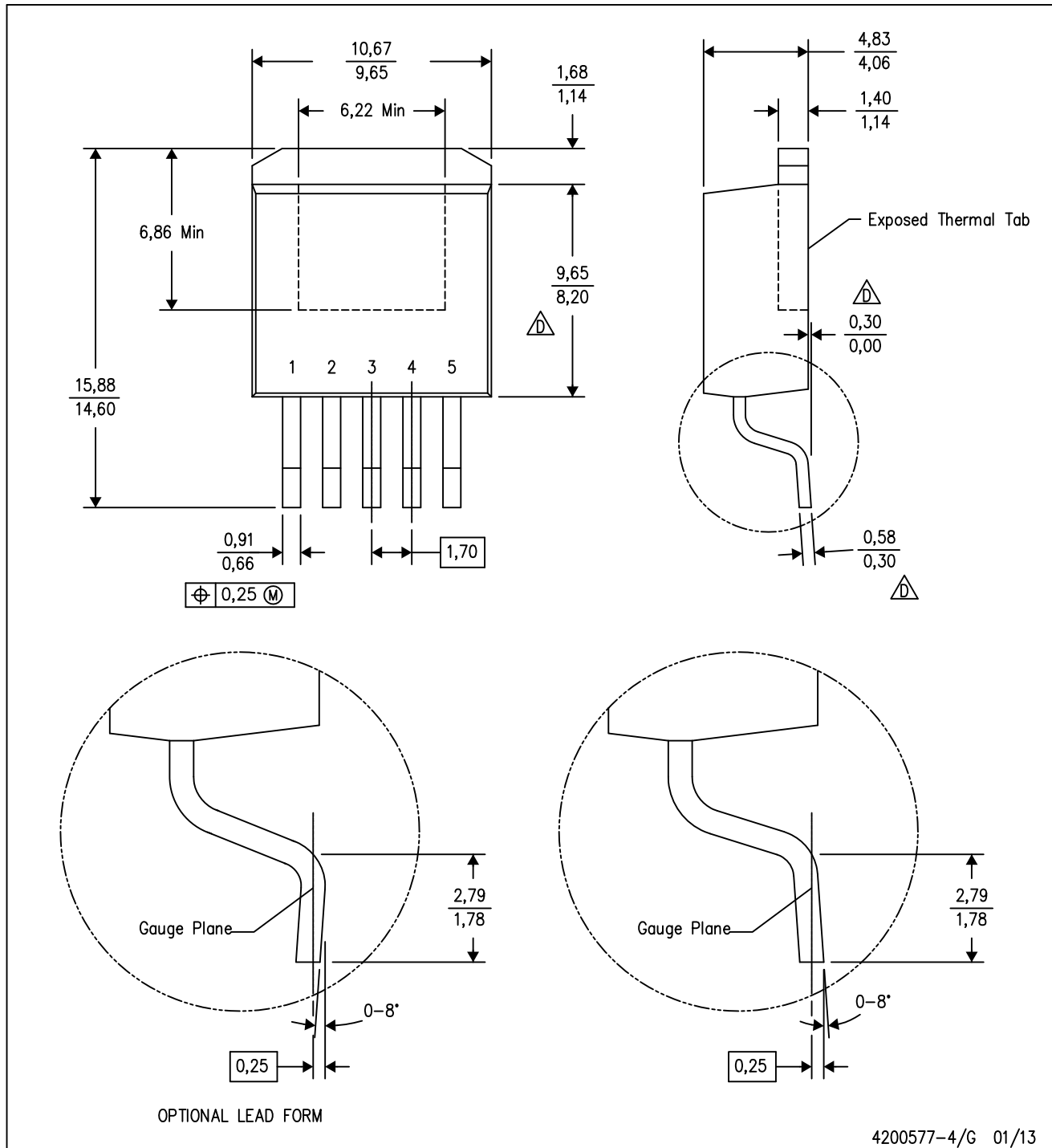


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6033QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A6033QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7A6050QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A6050QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7A6133QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7A6150QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

KTT (R-PSFM-G5)

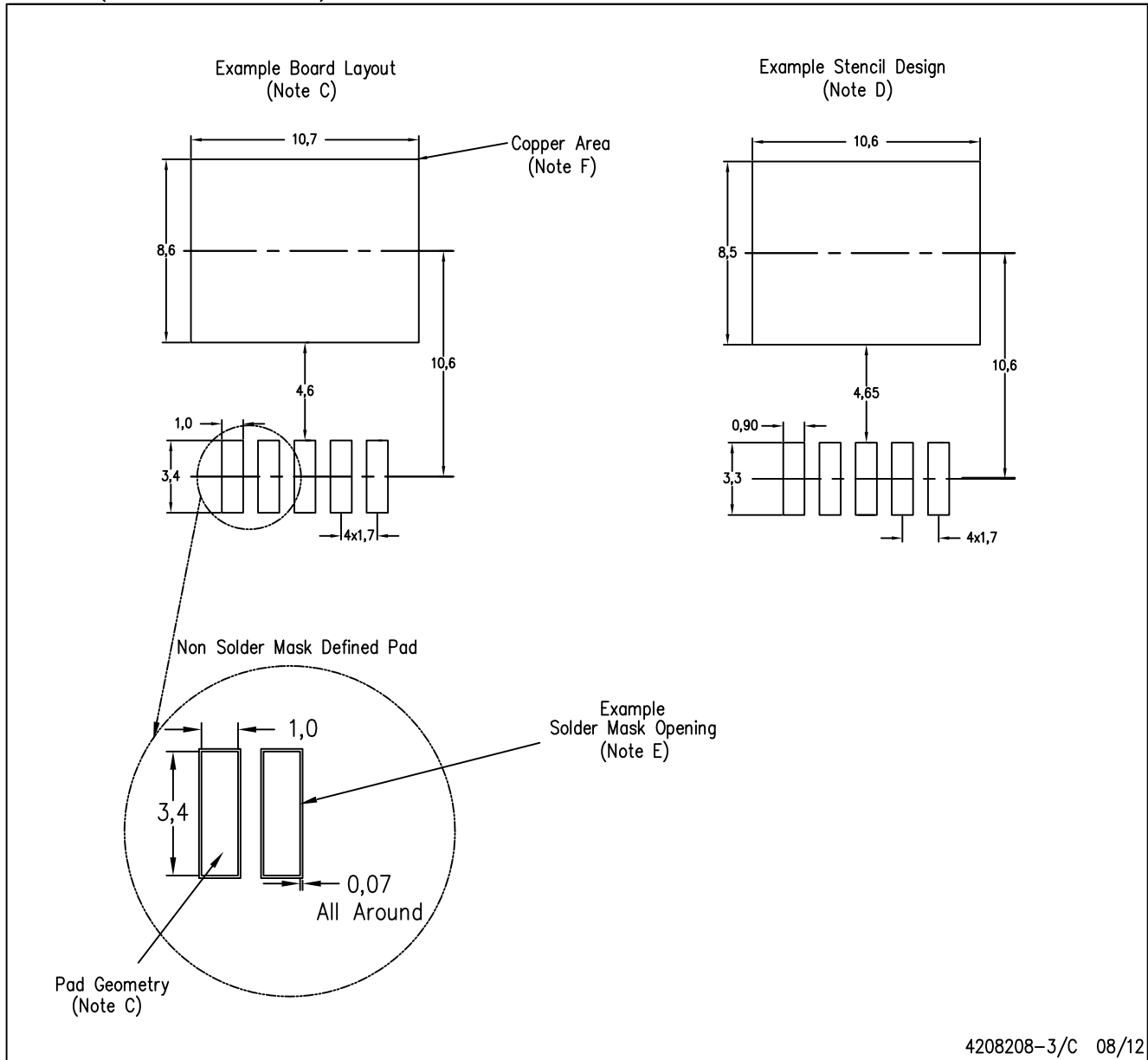
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)

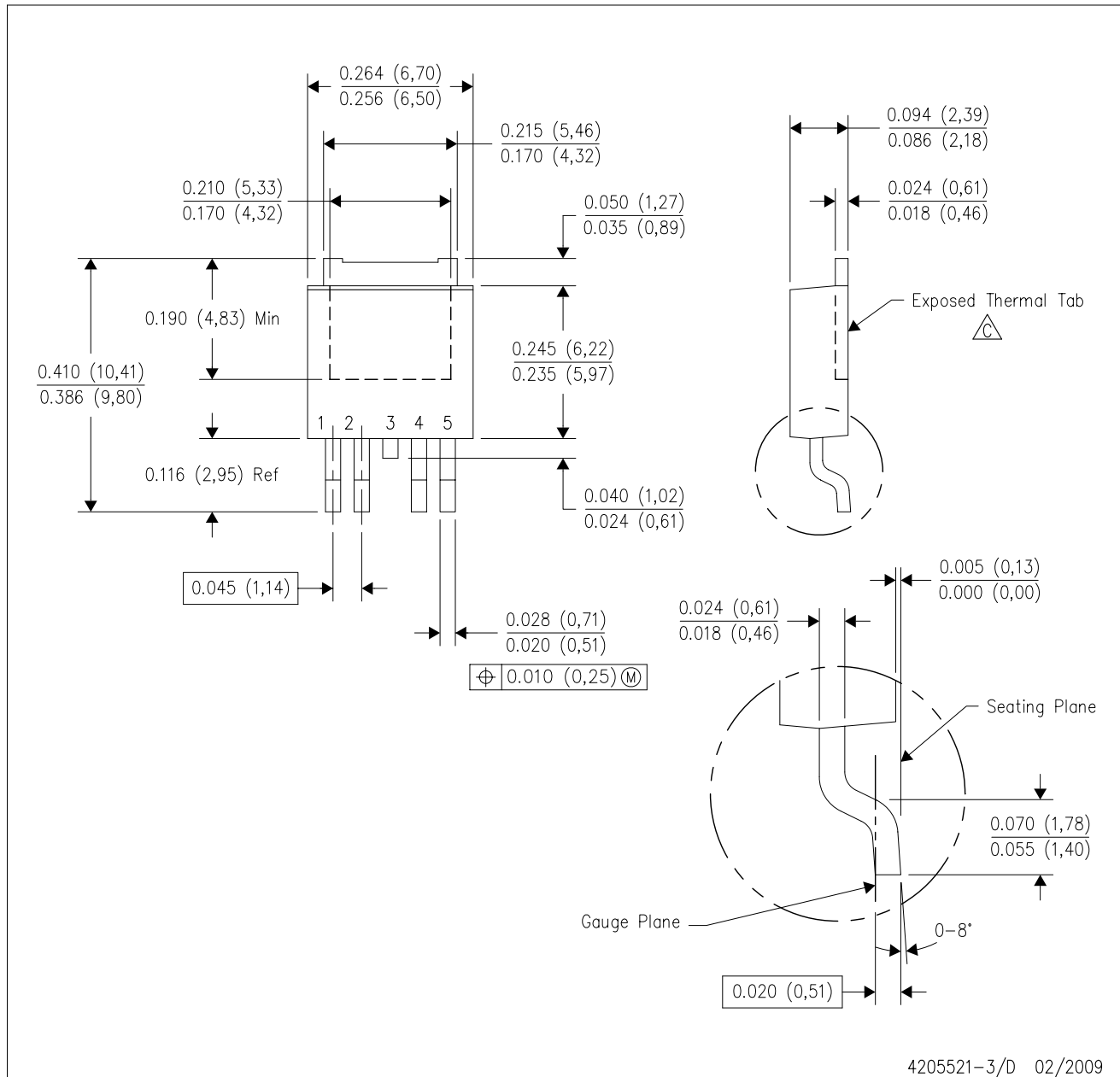
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

KVU (R-PSFM-G5)

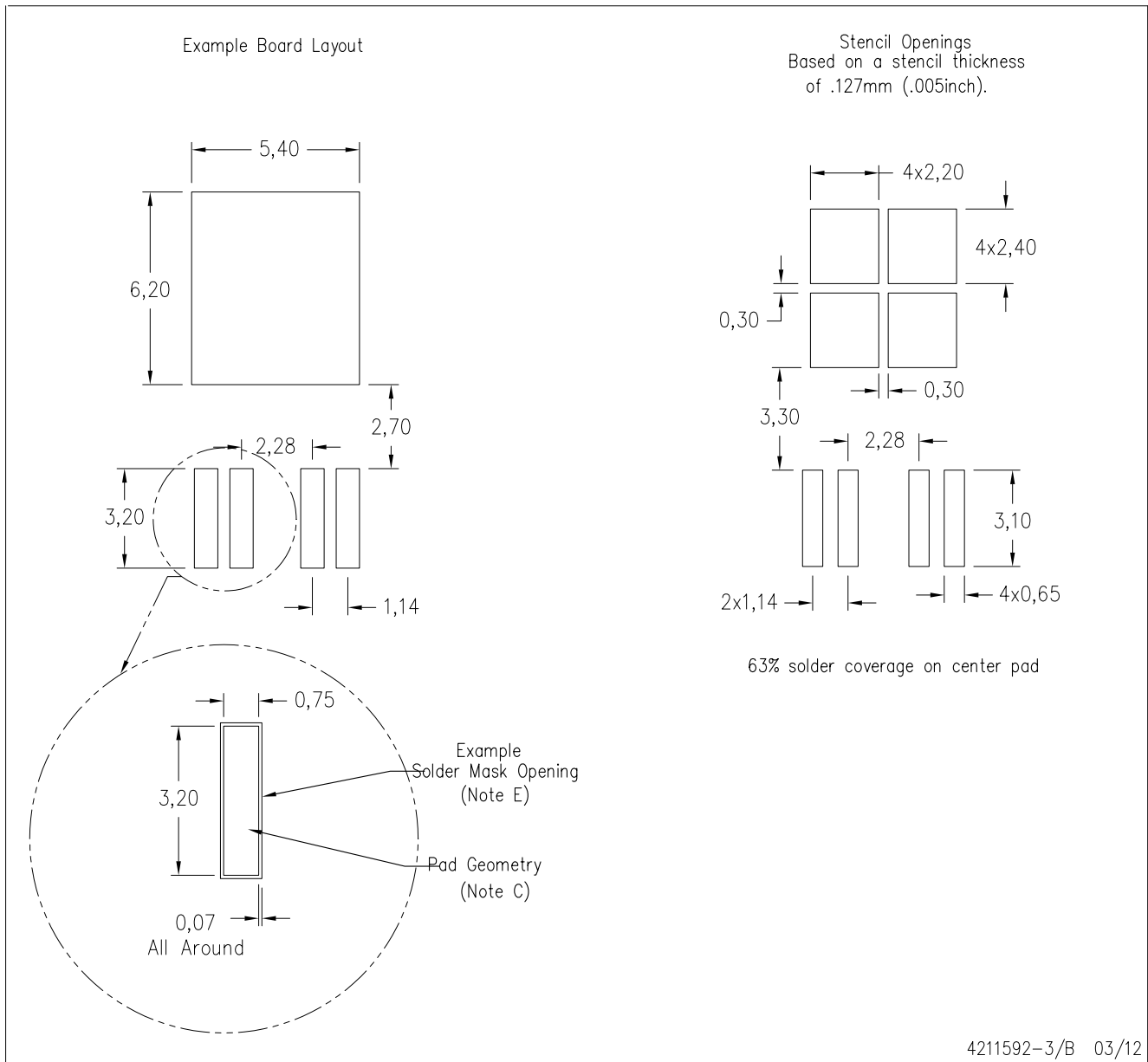
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. The center lead is in electrical contact with the exposed thermal tab.
 - D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
 - E. Falls within JEDEC TO-252 variation AD.

KVU (R-PSFM-G5)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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