TPS7A20U 75mA、低ノイズ、低 IQ、高 PSRR LDO

1 特長

- 低い出力電圧ノイズ:7μV_{RMS}
  - ノイズ バイパス コンデンサが不要
- 高 PSRR:1kHz 時に 89dB
- 超低 I_Q:6.5μA
- 入力電圧範囲:1.6V～6.0V
- 出力電圧範囲:0.8V～5.5V
- 出力電圧許容誤差:±1.5% (最大値)
- 非常に低いドロップアウト:
  - 75mA で 95mV (最大値) (V_{OUT} = 1.5V～5.5V)
- 小さい突入電流
- スマート イネーブルのプルダウン
- 最小 1μF のセラミック出力コンデンサで安定
- 0.616mm × 0.616mm DSBGA パッケージ

2 アプリケーション

- スマートフォンとタブレット
- IP ネットワーク カメラ
- 携帯医療機器
- スマート メータとフィールド トランスミッタ
- モーター ドライブ
- ウェアラブル

3 概要

TPS7A20U は、75mA の出力電流を供給できる超小型の低ドロップアウト (LDO) リニア レギュレータです。TPS7A20U は、低ノイズ、高 PSRR、非常に優れた負荷およびライン過渡性能を実現するよう設計されています。この性能は、RF およびその他の敏感なアナログ回路の要件を満たしています。革新的な設計手法を採用した TPS7A20U は、ノイズ バイパス コンデンサを追加しなくても超低ノイズ性能を発揮します。TPS7A20U は、静止電流が小さいという利点も備えており、バッテリ駆動のアプリケーションに適した設計になっています。1.6V～6.0V の入力電圧範囲と 0.8V～5.5V の出力電圧範囲に対応する TPS7A20U は、さまざまなアプリケーションを柔軟にサポートできます。本デバイスは、負荷、ライン、温度の変化に対して誤差 1.5% 以下の精度を達成するために高精度の基準電圧回路を使用しています。

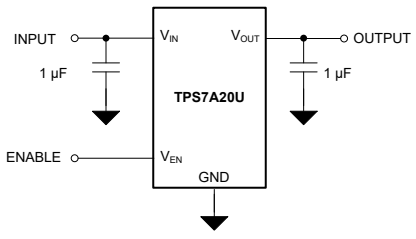
TPS7A20U は、突入電流を低減させるための内部ソフトスタートを備えているため、スタートアップ時の入力電圧の低下を最小限に抑えることができます。このデバイスは小さなセラミック コンデンサでも安定に動作するため、ソリューション全体を小型化できます。

TPS7A20U にはスマート イネーブル入力回路があり、内部で制御されるプルダウン抵抗によって LDO をディセーブル状態に維持できます。EN ピンがフローティングのままであっても LDO はディセーブル状態を維持するので、EN ピンをプルダウンするために使用する外付け部品が不要になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS7A20U	YCK (DSBGA、4)	0.616 mm × 0.616 mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略回路図

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4 Pin Configuration and Functions

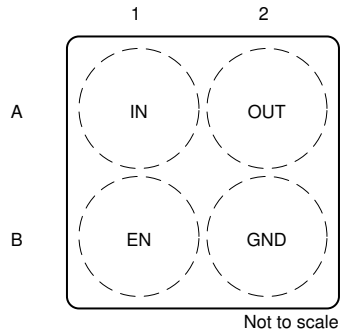


図 4-1. YCK Package, 4-Pin DSBGA (Top View)

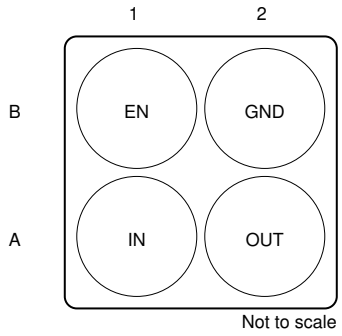


図 4-2. YCK Package, 4-Pin DSBGA (Bottom View)

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	IN	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
A2	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor, as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$).
B1	EN	I	Enable input. A low voltage ($< V_{EN(LOW)}$) on this input turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500kΩ pulldown is disconnected to reduce input current.
B2	GND	—	Common ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{OUT}	–0.3	6.5 or V_{IN} + 0.3 (2)	
	V_{EN}	–0.3	6.5	
Current	Maximum output(4)	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum value of V_{OUT} is the lesser of 6.5V or (V_{IN}+0.3V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.6		6.0	V
V_{EN}	Enable input voltage	0		6.0	V
V_{OUT}	Nominal output voltage range	0.8		5.5	V
I_{OUT}	Output current	0		75	mA
C_{IN}	Input capacitor(2)		1		µF
C_{OUT}	Output capacitance(3)	0.47		10	µF
ESR	Output capacitor effective series resistance			50	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which sometimes causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
(3) To help achieve fast settling and avoid instability, make sure the output capacitance (including tolerance, bias voltage, temperature variations, and so forth) falls within the specified range.

5.4 Thermal Information

THERMAL METRIC[1]		TPS7A20U YCK (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V, whichever is greater, V_{EN} = 1.0V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 6.0V, I_{OUT} = 1 mA to 75 mA	V_{OUT} ≥ 1.85V	–1.5		1.5	%
			V_{OUT} < 1.85V	–30		30	mV
ΔV_{OUT}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 6.0V, I_{OUT} = 1mA			0.03		%/V
ΔV_{OUT}	Load regulation	I_{OUT} = 1mA to 75mA			3		mV
I_{GND}	Quiescent ground current	V_{EN} = V_{IN} = 6V, I_{OUT} = 0mA	T_J = 25°C		6.5	9.5	µA
			T_J = –40°C to 85°C			11	
			T_J = –40°C to 125°C			15	
		V_{EN} = V_{IN} = 6 V, I_{OUT} = 75mA			1500		
I_{SHDN}	Shutdown ground current	V_{EN} = 0V (disabled), V_{IN} = 6.0V	T_J = 25°C		0.07	0.2	µA
			T_J = –40°C to 85°C			2	
			T_J = –40°C to 125°C			10	
$I_{GND(DO)}$	I_{GND} in dropout	V_{IN} ≤ $V_{OUT(NOM)}$, I_{OUT} = 0mA, V_{EN} = V_{IN}			6.5	15	µA
V_{DO}	Dropout voltage	I_{OUT} = 75mA, V_{OUT} = 95% x $V_{OUT(NOM)}$	1.5V ≤ V_{OUT} ≤ 5.5V			95	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.5V	V_{OUT} < 1.5V	95	180	265	mA
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V	V_{OUT} ≥ 1.5V	95	185	265	
PSRR	Power-supply rejection ratio	I_{OUT} = 20mA, V_{IN} = V_{OUT} + 1.0V	f = 100Hz		88		dB
			f = 1kHz		87		
			f = 10kHz		72		
			f = 100kHz		62		
			f = 1MHz		42		
		I_{OUT} = 75mA, V_{IN} = V_{OUT} + 1.0V	f = 100Hz		80		
			f = 1kHz		89		
			f = 10kHz		73		
			f = 100kHz		63		
			f = 1MHz		44		
V_N	Output noise voltage	BW = 10Hz to 100kHz, V_{OUT} = 2.8V	I_{OUT} = 75mA		7		μV_{RMS}
			I_{OUT} = 1mA		8		
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled), V_{IN} = 3.1V			285		Ω
T_{SD}	Thermal shutdown	T_J rising			165		°C
		T_J falling			140		

5.5 Electrical Characteristics (続き)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V, whichever is greater, V_{EN} = 1.0V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(LOW)}$	Low input threshold	V_{IN} = 1.6V to 6.0V, V_{EN} falling until the output is disabled			0.3	V
$V_{EN(HI)}$	High input threshold	V_{IN} = 1.6V to 6.0V V_{EN} rising until the output is enabled	0.9			V
V_{UVLO}	UVLO threshold	V_{IN} rising	1.11	1.35	1.59	V
		V_{IN} falling	1.05	1.3	1.55	
$V_{UVLO(HYST)}$	UVLO hysteresis			47		mV
I_{EN}	EN input leakage current	V_{EN} = 6.0V and V_{IN} = 6.0V		90	250	nA
$R_{EN(PULL-DOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.25V		500		KΩ

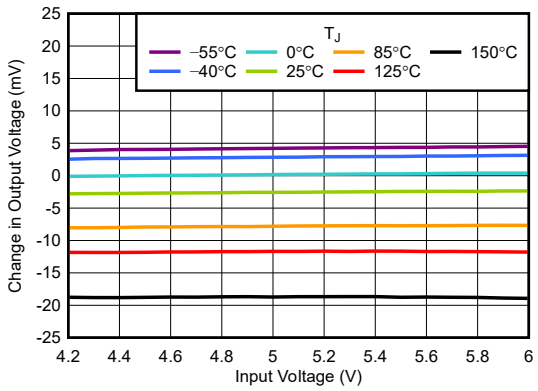
5.6 Switching Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V, whichever is greater, V_{EN} = 1.0V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, C_{OUT} ESL = 300pH, C_{OUT} ESR = 8mΩ, board ESL = 1.5nH, board ESR = 5mΩ (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$		750	1150	µs

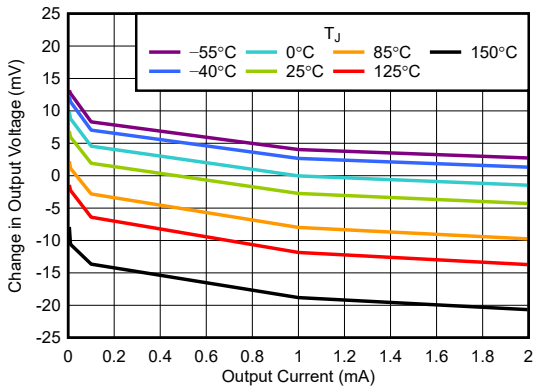
5.7 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



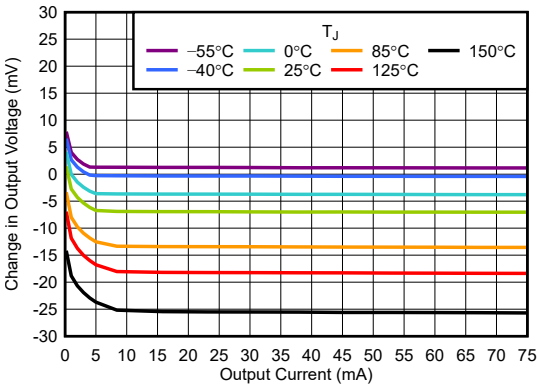
V_{EN} = 1V

図 5-1. Line Regulation vs V_{IN}



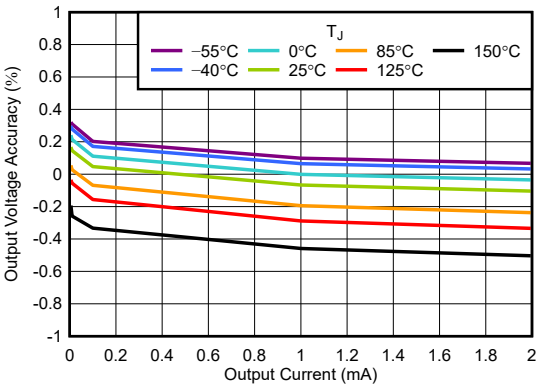
V_{IN} = 4.4V, V_{EN} = 1V

図 5-2. Load Regulation vs I_{OUT}



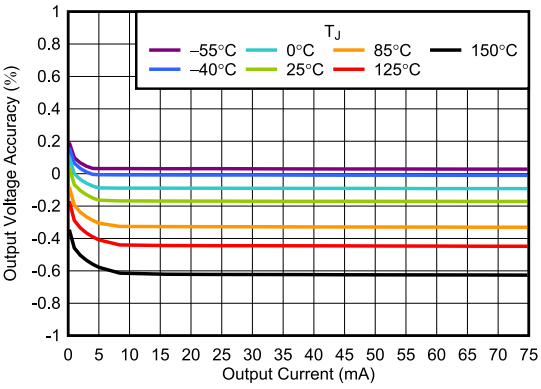
V_{IN} = 4.4V, V_{EN} = 1V

図 5-3. Load Regulation vs I_{OUT}



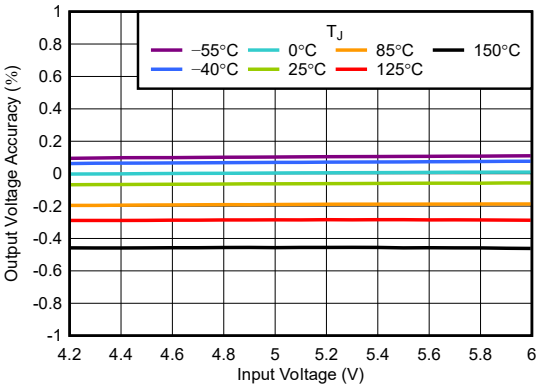
V_{EN} = 1V

図 5-4. Output Voltage Accuracy vs I_{OUT}



V_{EN} = 1V

図 5-5. Output Voltage Accuracy vs I_{OUT}

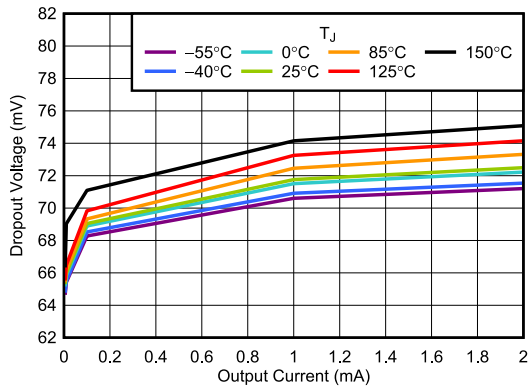


V_{EN} = 1V, I_{OUT} = 1mA

図 5-6. Output Voltage Accuracy vs V_{IN}

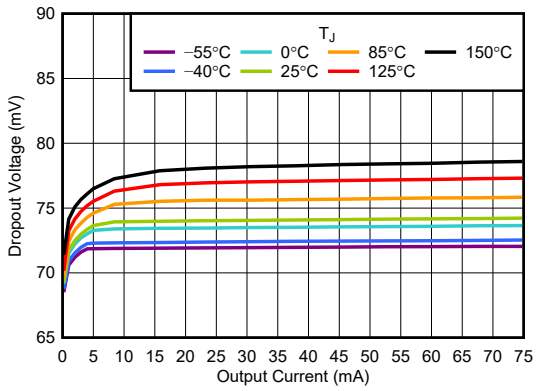
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



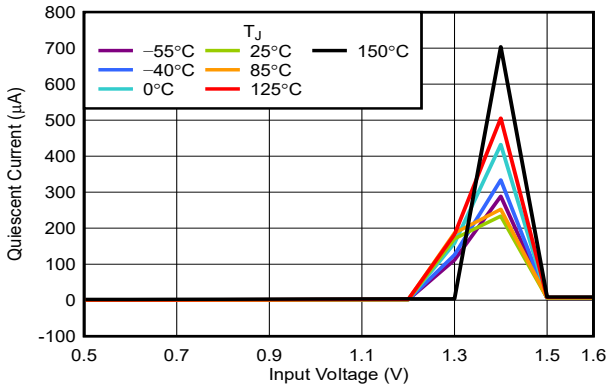
V_{EN} = 1V

図 5-7. Dropout Voltage vs I_{OUT}



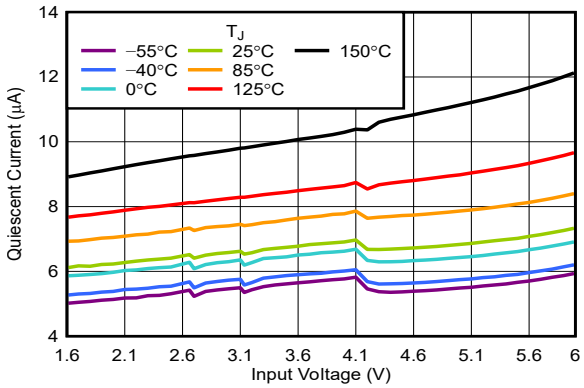
V_{EN} = 1V

図 5-8. Dropout Voltage vs I_{OUT}



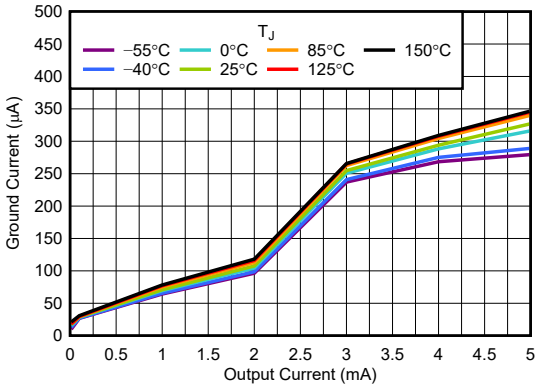
V_{EN} = 1V, I_{OUT} = 0mA

図 5-9. I_{GND} vs V_{IN}



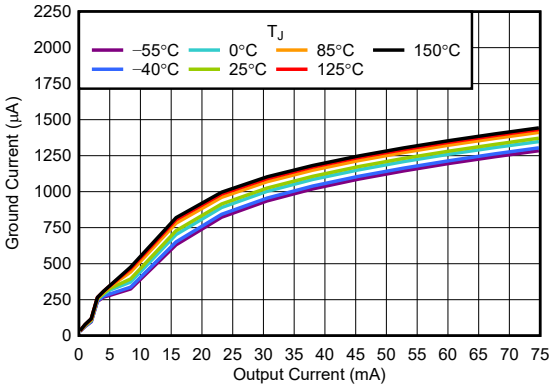
V_{EN} = V_{IN}, I_{OUT} = 0mA

図 5-10. I_{GND} vs V_{IN}



V_{EN} = 1V

図 5-11. I_{GND} vs I_{OUT}

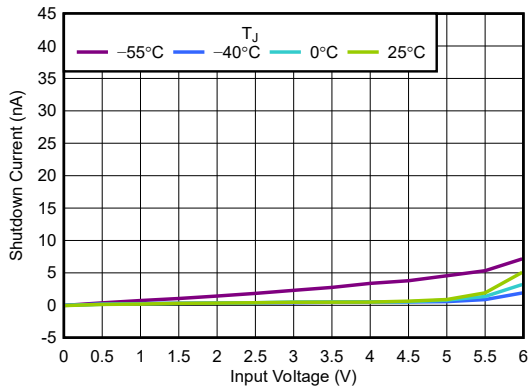


V_{EN} = 1V

図 5-12. I_{GND} vs I_{OUT}

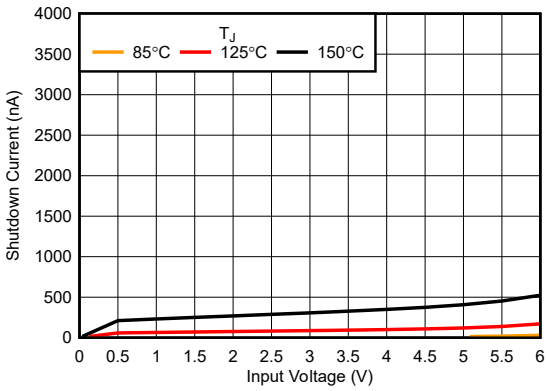
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



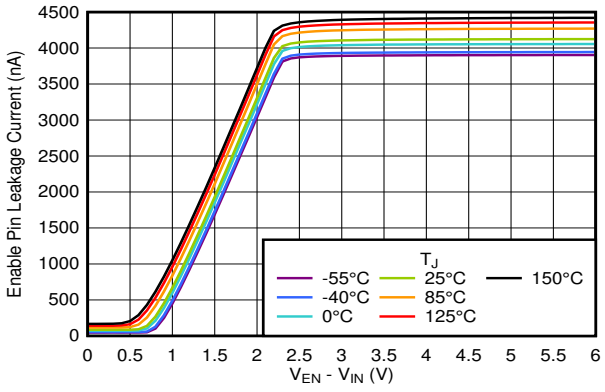
V_{EN} = 1V

図 5-13. Shutdown Current vs V_{IN}



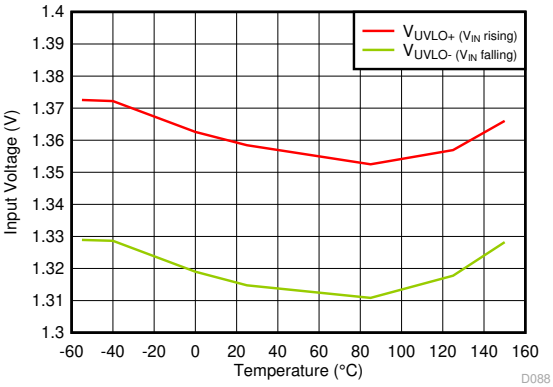
V_{EN} = 0V

図 5-14. Shutdown Current vs V_{IN}



V_{EN} = 6V, I_{OUT} = 0mA

図 5-15. Enable Pin Leakage Current vs V_{EN} – V_{IN}



V_{EN} = 1V

図 5-16. UVLO Threshold vs Temperature

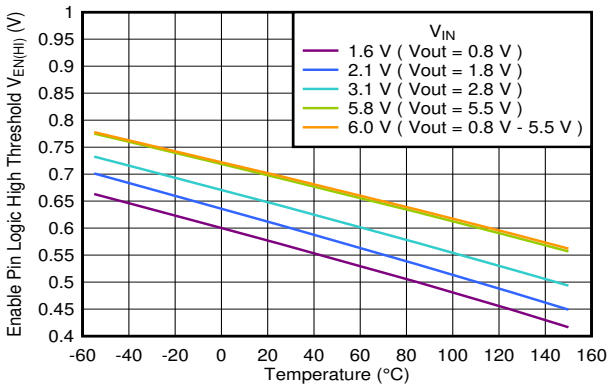


図 5-17. Enable Logic High Threshold vs Temperature

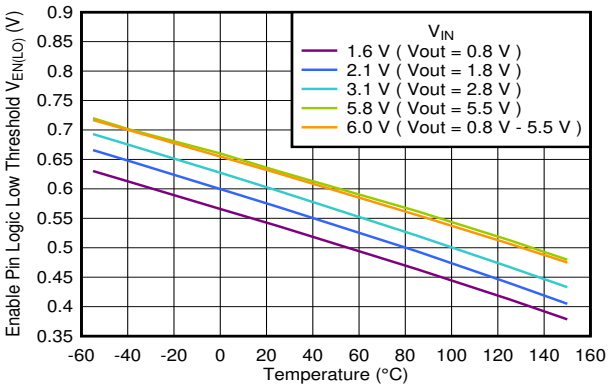
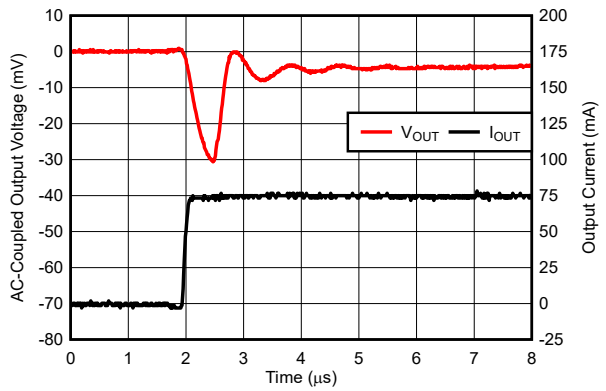


図 5-18. Enable Logic Low Threshold Low vs Temperature

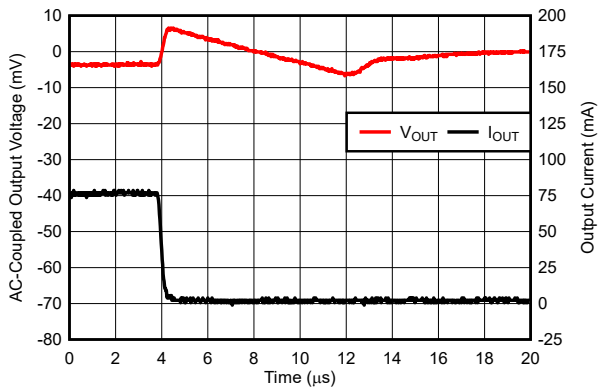
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



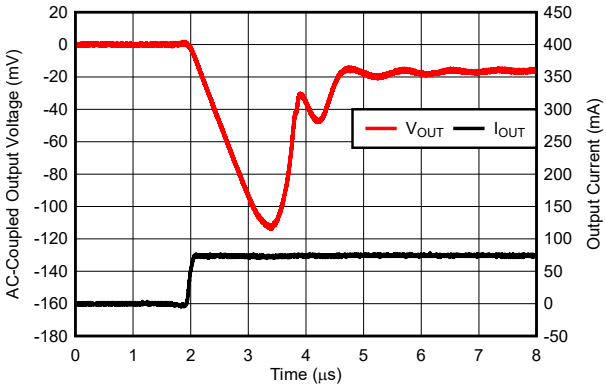
I_{OUT} = 1mA to 75mA, t_{RISING} = 75ns

図 5-19. Load Transient



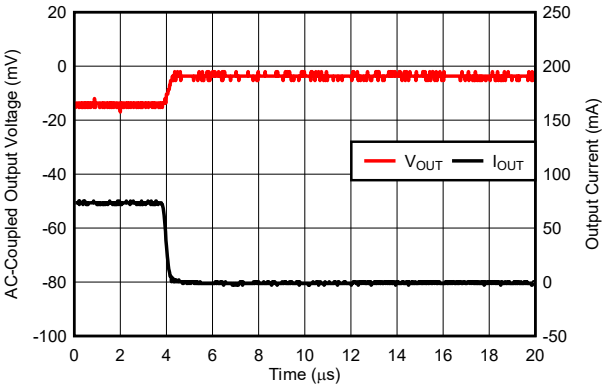
I_{OUT} = 75mA to 1mA, $t_{FALLING}$ = 75ns

図 5-20. Load Transient



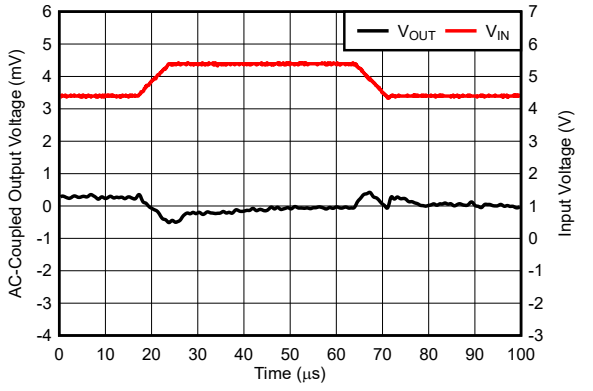
I_{OUT} = 0mA to 75mA, t_{RISING} = 75ns

図 5-21. Load Transient



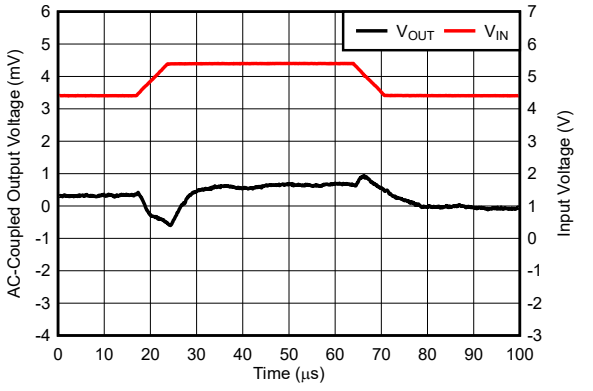
I_{OUT} = 75mA to 0mA, $t_{FALLING}$ = 75ns

図 5-22. Load Transient



V_{IN} = 4.4V → 5.4V → 4.4V, V_{IN} t_{RISING} = 5µs, I_{OUT} = 75mA

図 5-23. Line Transient

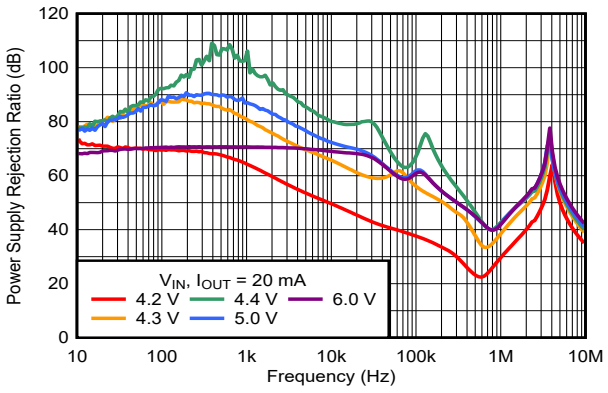


V_{IN} = 4.4V → 5.4V → 4.4V, V_{IN} t_{RISING} = 5µs, I_{OUT} = 1mA

図 5-24. Line Transient

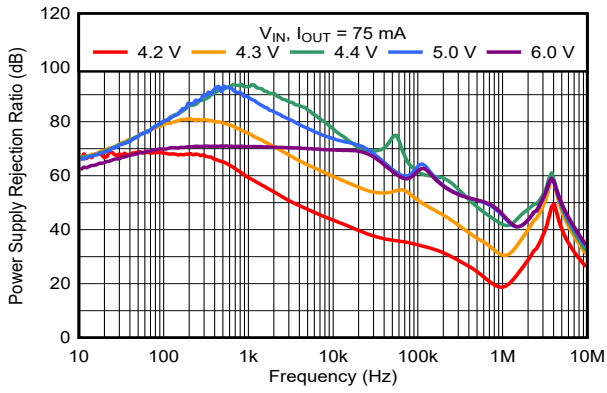
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



I_{OUT} = 20mA

図 5-25. PSRR vs Frequency and V_{IN}



I_{OUT} = 75mA

図 5-26. PSRR vs Frequency and V_{IN}

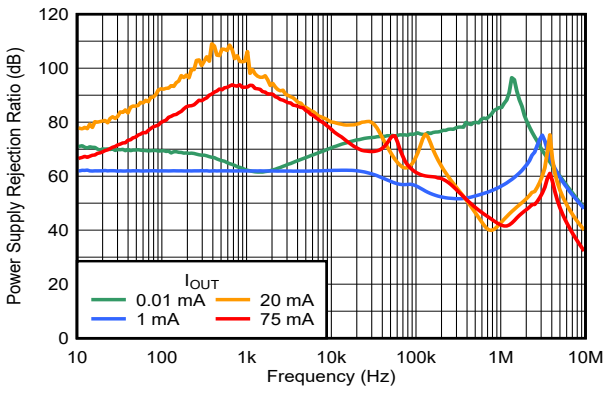
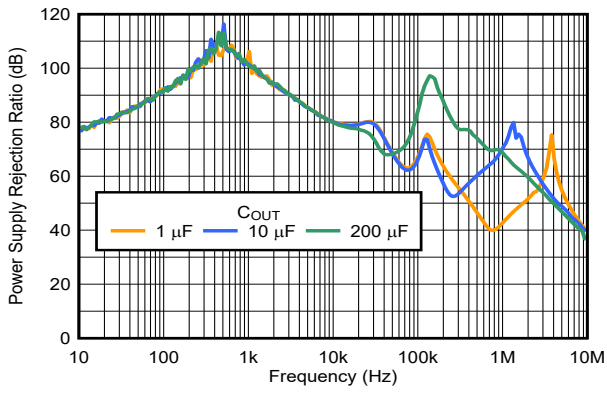
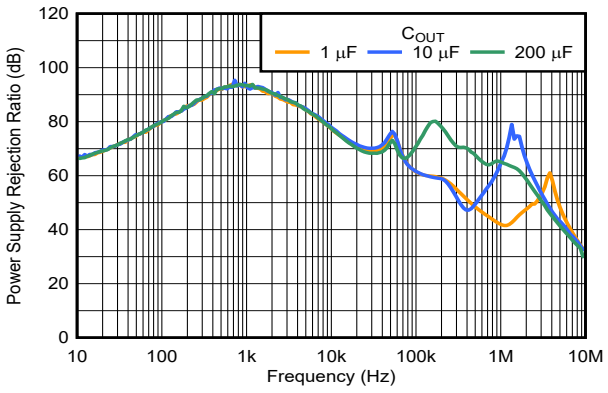


図 5-27. PSRR vs Frequency and I_{OUT}



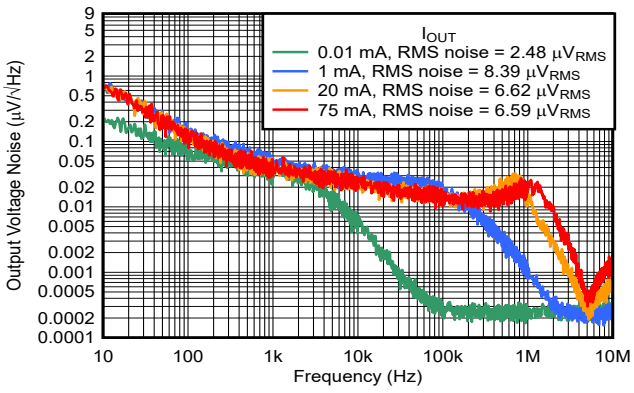
I_{OUT} = 20mA

図 5-28. PSRR vs Frequency and C_{OUT}



I_{OUT} = 75mA

図 5-29. PSRR vs Frequency and C_{OUT}

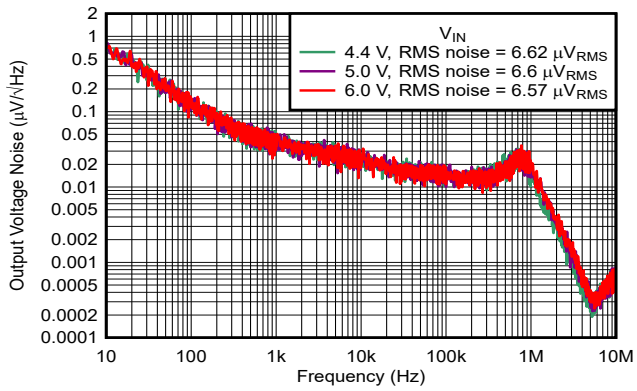


V_{RMS} BW = 10Hz to 100kHz

図 5-30. Noise vs Frequency and I_{OUT}

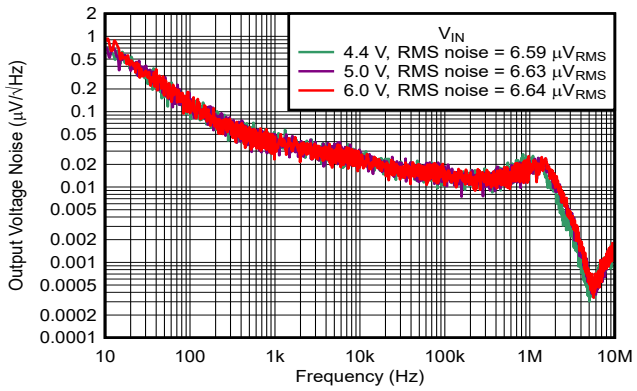
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



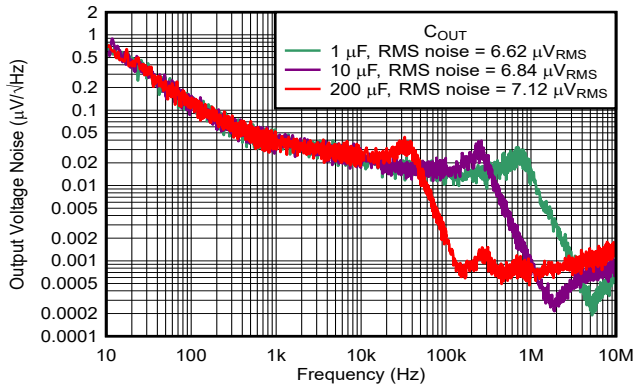
I_{OUT} = 20mA, V_{RMS} BW = 10Hz to 100kHz

図 5-31. Noise vs Frequency and V_{IN}



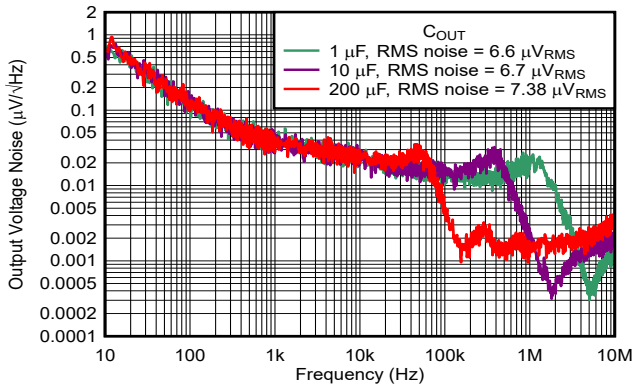
I_{OUT} = 75mA, V_{RMS} BW = 10Hz to 100kHz

図 5-32. Noise vs Frequency and V_{IN}



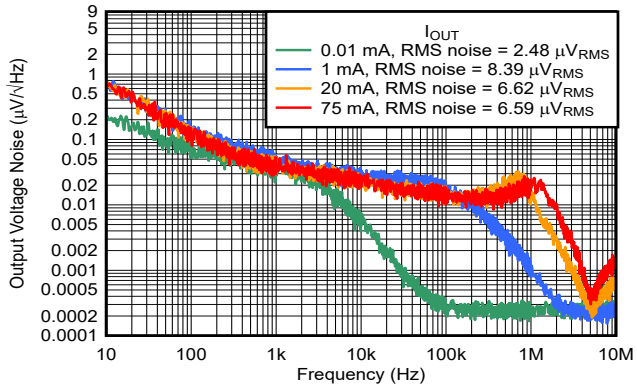
I_{OUT} = 20mA, V_{RMS} BW = 10Hz to 100kHz

図 5-33. Noise vs Frequency and C_{OUT}



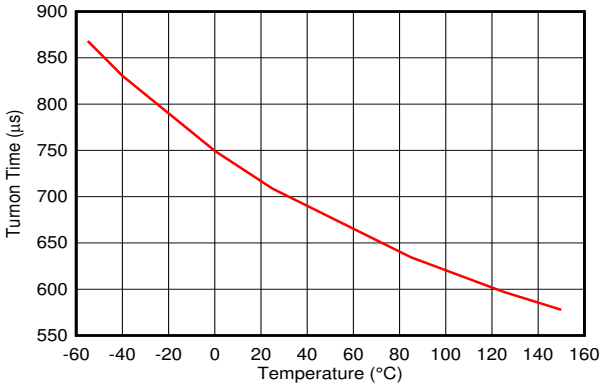
I_{OUT} = 75mA, V_{RMS} BW = 10Hz to 100kHz

図 5-34. Noise vs Frequency and C_{OUT}



V_{RMS} BW = 10Hz to 100kHz

図 5-35. Noise vs Frequency and I_{OUT}

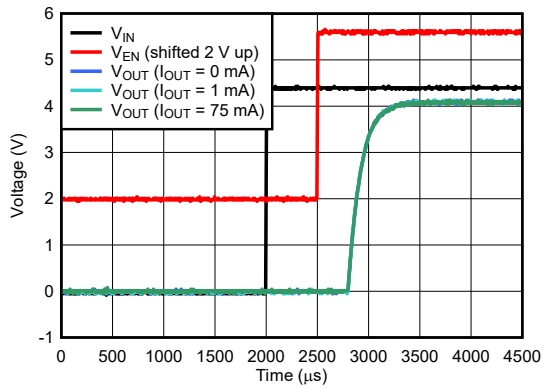


From V_{EN} = $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, I_{OUT} = 0mA

図 5-36. Start-Up Turn-On Time

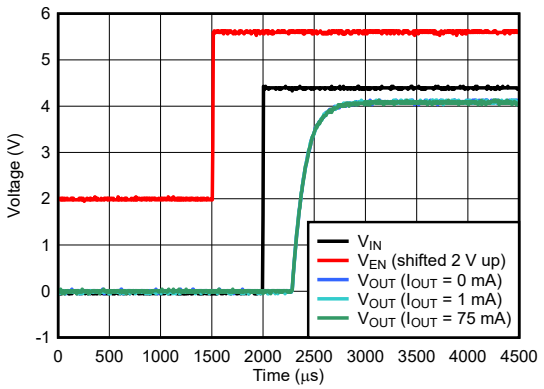
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3V or 1.6V (whichever is greater), V_{OUT} = 4.1V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



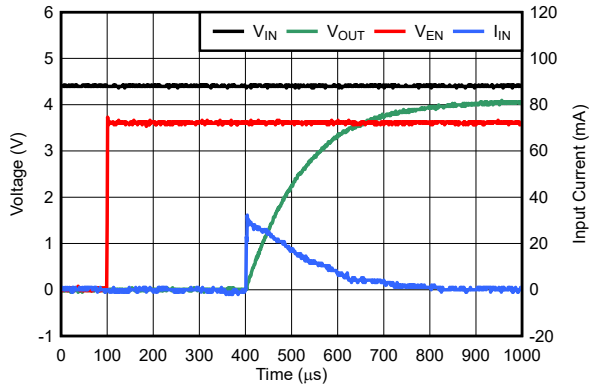
V_{IN} = 0V to 4.4V, V_{EN} = 0V to 3.6V, V_{EN} rises 500µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1V/µs

図 5-37. Start-Up



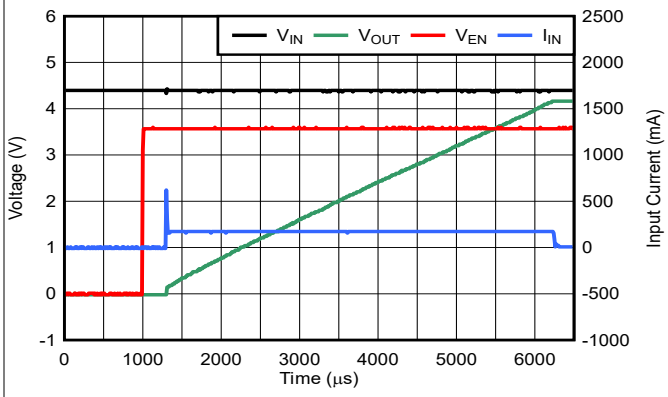
V_{IN} = 0V to 4.4V, V_{EN} = 0V to 3.6V, V_{EN} rises 500µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1V/µs

図 5-38. Start-Up



V_{IN} = 4.4V, V_{EN} = 0V to 3.6V, V_{EN} slew rate = 1V/µs, C_{OUT} = 1µF

図 5-39. Inrush Current



V_{IN} = 4.4V, V_{EN} = 0V to 3.6V, V_{EN} slew rate = 1V/µs, C_{OUT} = 200µF

図 5-40. Inrush Current

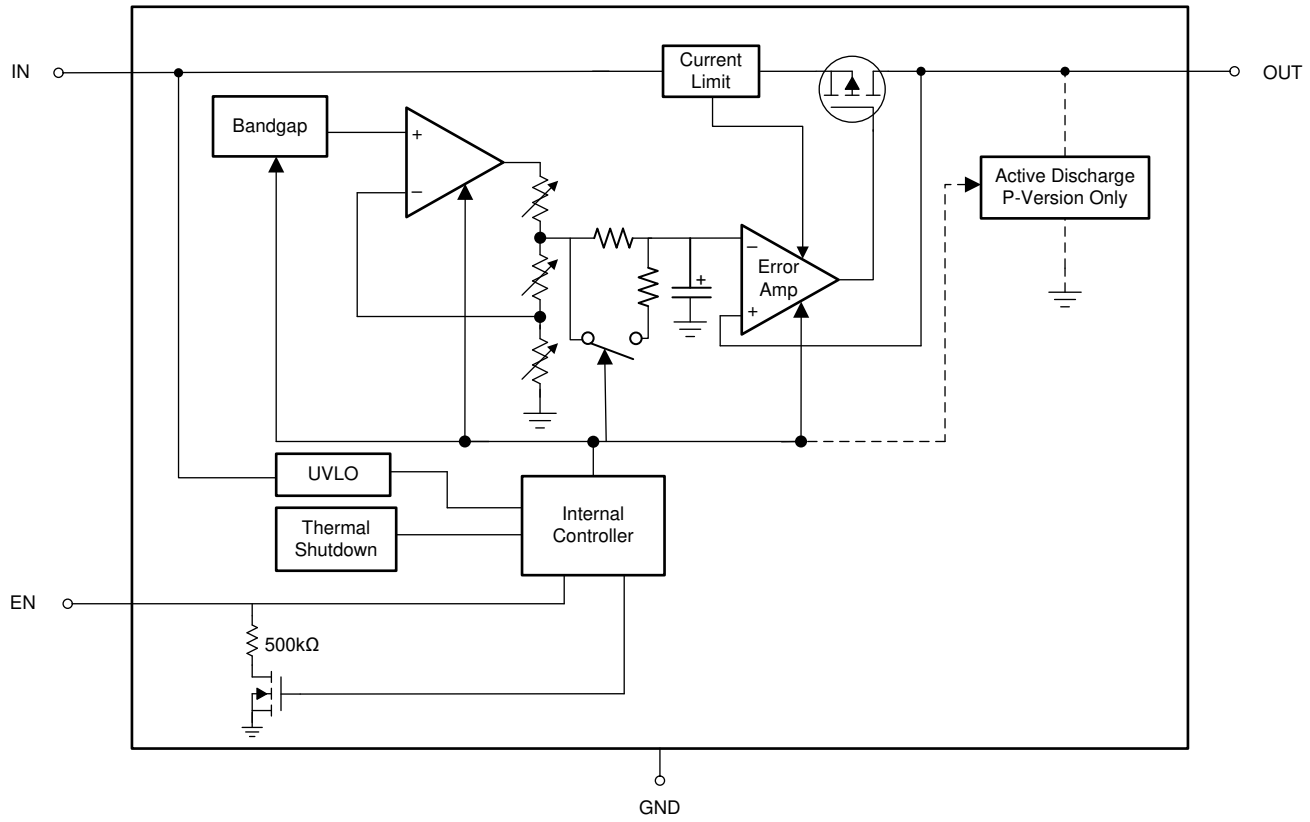
6 Detailed Description

6.1 Overview

the TPS7A20U is designed to meet the needs of sensitive RF and analog circuits. This device provides low noise, high PSRR, low quiescent current, and low line and load transient response figures. Using innovative design techniques, the TPS7A20U offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20U is designed to operate with a single 1µF input capacitor and a single 1µF ceramic output capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Output Noise

Any internal noise at the TPS7A20U reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3dB cut-off frequency of approximately 0.1Hz.

During start-up, the filter resistor is bypassed to reduce output rise time. The filter begins normal operation after the output voltage reaches the correct value.

6.3.2 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the enable input voltage is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the enable pin voltage is driven above $V_{EN(HI)}$, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. See the *Electrical Characteristics* table. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

6.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [(VIN – VOUT) × ICL]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on.

If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the Know Your Limits application note.

6.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows for a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis; see the *Electrical Characteristics* table.

6.3.6 Thermal Shutdown

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal device protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.7 Active Discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. The active discharge circuit is activated by driving EN low or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed. Reverse current potentially flows from the output to the input. This reverse current flow potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.3 Disabled

Shut down the output of the LDO by driving EN to less than $V_{EN(LOW)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shut down. The output voltage is also actively discharged to ground by an internal discharge circuit between OUT and ground.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. Whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors provided in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although the LDO is stable without an input capacitor, good analog design practice is to connect a capacitor from IN to GND. Use a capacitor with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use this capacitor if the source impedance is greater than 0.5Ω. When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system is susceptible to instability. Instability includes ringing, sustained oscillation, and other performance degradation if there is insufficient capacitance between IN and GND. Use a capacitor with a value greater than the minimum if large, fast-rise-time load or line transients are anticipated. Also use a similar capacitor if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps provide stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

7.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: from a light to a heavy load and from a heavy to a light load. The regions shown in 図 7-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

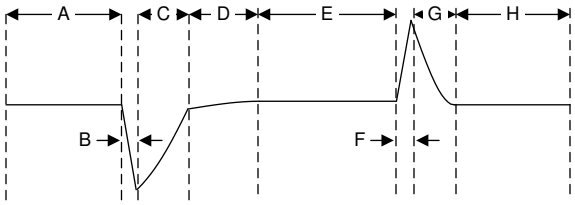


図 7-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to an increased output capacitor charge (region F)
- Recovery from the rise results from the LDO decreasing sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks. The amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure that the device stays disabled before the input supply reaches the minimum operational voltage range. This circuit also makes sure that the device shuts down when the input supply collapses. 図 7-2 shows the UVLO circuit response to various input voltage events. The diagram is separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output potentially falls out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

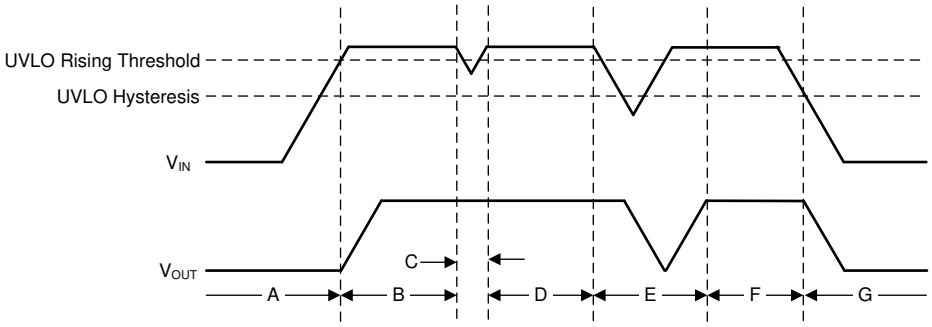


図 7-2. Typical UVLO Operation

7.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, circuit location on the PCB, and correct thermal plane sizing. Make sure the printed circuit board (PCB) area around the regulator is as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20U allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 3, power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. 式 4 rearranges 式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{4}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, this resistance varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area. $R_{\theta JA}$ is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DSBGA $R_{\theta JC(bot)}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JC(bot)}$ is the package junction-to-case (bottom) thermal resistance.

7.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \tag{5}$$

where:

- P_D is the power dissipated as explained in 式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 7-3 and is separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 式 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO. Thus, when $V_{IN} - V_{OUT}$ increases the output current decreases.

- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

図 7-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$, as given in the *Thermal Information* table.

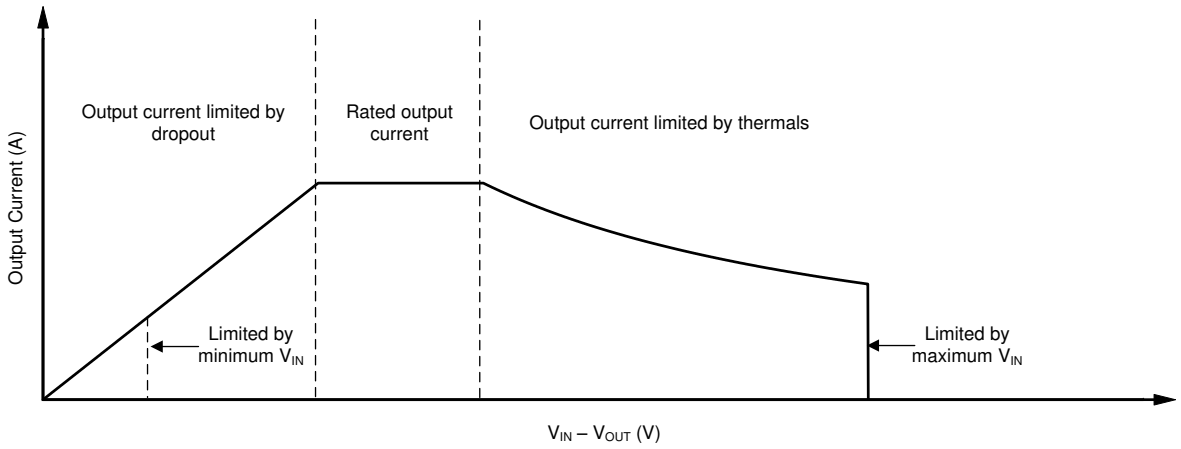


図 7-3. Region Description of Continuous Operation Regime

7.2 Typical Application

図 7-4 shows the typical application circuit for the TPS7A20. If needed, increase the input and output capacitances above the 1µF minimum for some applications.

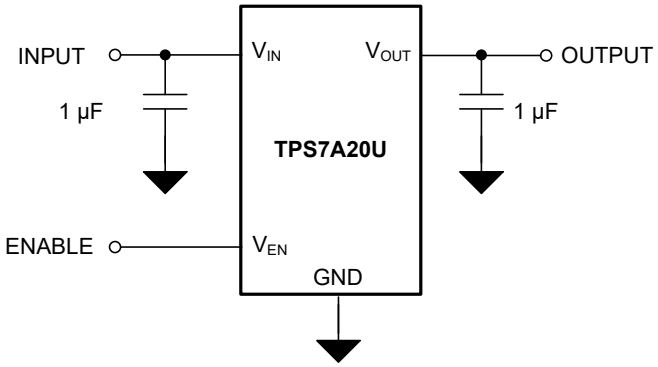


図 7-4. TPS7A20U Typical Application

7.2.1 Design Requirements

表 7-1 summarizes the design requirements for 図 7-4.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.5V to 5.5V
Output voltage	4.1V
Output current	70mA
Maximum ambient temperature	85°C

7.2.2 Detailed Design Procedure

For this design example, the 4.1V output version (TPS7A20U41) is selected. A nominal 5V input supply is assumed. Use a minimum 1.0µF input capacitor to minimize the effect of resistance and inductance between the 5V source and the LDO input. Also use a minimum 1.0µF output capacitor for stability and good load transient response. The dropout voltage (V_{DO}) is less than 95mV maximum at a 4.1V output voltage and 75mA output current. Thus, there are no dropout issues with a minimum 4.5V input voltage and a maximum 75mA output current.

7.2.3 Application Curve

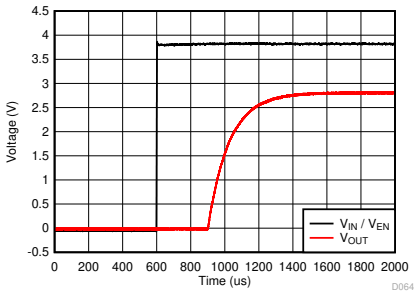


図 7-5. Start-Up

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6V to 6.0V. Make sure the input supply is well regulated and free of spurious noise. Set the input supply to be at least $V_{OUT(nom)}$ + 0.3V or 1.6V, whichever is greater. This setting makes sure that the output voltage is well regulated and dynamic performance is optimum. Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the YCK package. A via wicks solder or solder paste away from the thermal pad joint during the soldering process, thus leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Example

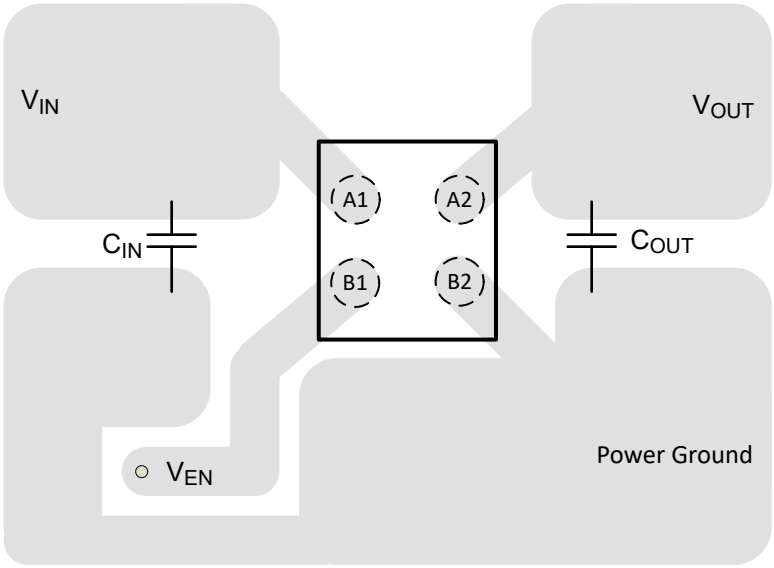


図 7-6. YCK Package (DSBGA) Typical Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT (1) (2)	V_{OUT}
TPS7A20U**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number. Otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V). **P** indicates an active output discharge feature. **yyy** is the package designator. **z** is the package quantity. R is for reel (12000 pieces for YCK).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8V to 5.5V in 25mV increments are available. Contact the factory for details and availability.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (August 2024) to Revision A (September 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A20U18PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V
TPS7A20U18PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V
TPS7A20U25PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
TPS7A20U25PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
TPS7A20U30PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS7A20U30PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS7A20U31PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Y
TPS7A20U31PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Y
TPS7A20U33PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A20U33PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A20U41PYCKR	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U
TPS7A20U41PYCKR.A	Active	Production	DSBGA (YCK) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

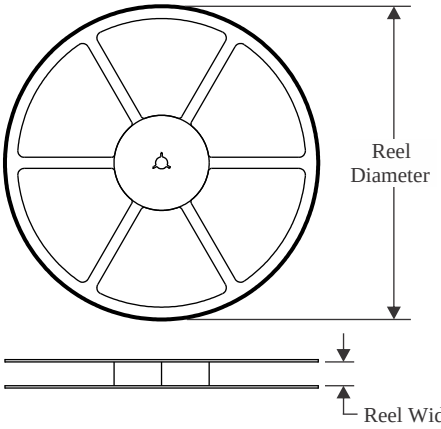
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

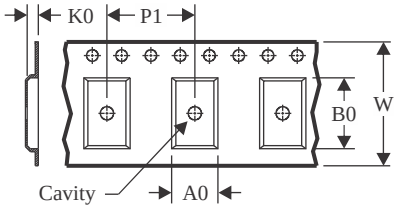
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

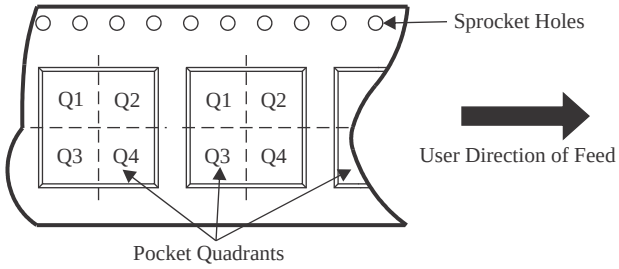


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

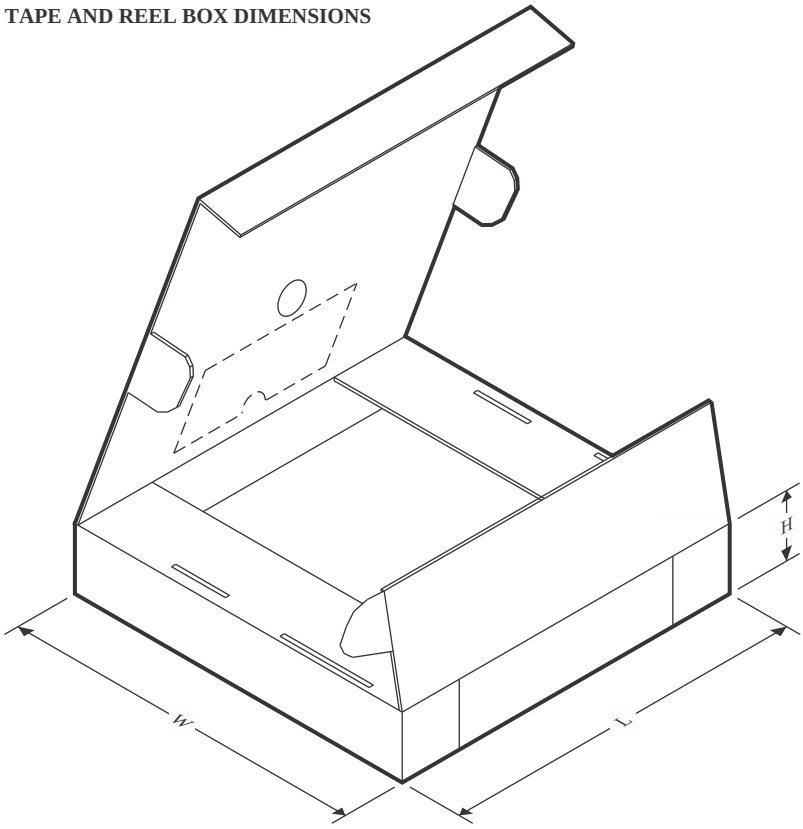
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A20U18PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U18PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U25PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U25PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U30PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U30PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U31PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U31PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U33PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U33PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U41PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20U41PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A20U18PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U18PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U25PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U25PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U30PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U30PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U31PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U31PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U33PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U33PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U41PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A20U41PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0

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