TEXAS INSTRUMENTS
TPS7A20L
JAJSQC0 – JANUARY 2024

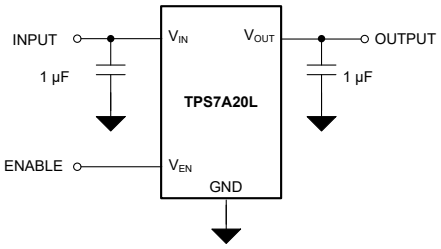
TPS7A20L 300mA、低ノイズ、低静止電流 (I_Q)、高 PSRR LDO 電圧レギュレータ、1.2V ロジック互換イネーブル

1 特長

- 低い出力電圧ノイズ:7μV_{RMS}
  - ノイズ バイパス コンデンサが不要
- 高い PSRR:1kHz 時に 95dB
- 超低 I_Q:6.5µA
- 入力電圧範囲:1.6V～6.0V
- 出力電圧範囲:0.8V～5.5V
- 出力電圧許容誤差:±1.5% (最大値)
- 非常に低いドロップアウト:
  - 300mA で 140mV 以下 (V_{OUT} = 3.3V)
- 小さい突入電流
- スマート イネーブルのプルダウン
- 最小 1µF のセラミック出力コンデンサで安定
- イネーブル入力は 1.2V ロジック互換
- パッケージ:1mm×1mm X2SON

2 アプリケーション

- スマートフォンとタブレット
- IP ネットワーク カメラ
- 携帯医療機器
- スマート メータとフィールド トランスミッタ
- モータ ドライブ
- ウェアラブル



概略回路図

3 概要

TPS7A20L は、300mA の出力電流を供給できる超小型の低ドロップアウト (LDO) リニア レギュレータです。TPS7A20L は、RF やその他の敏感なアナログ回路の要件を満たすため、低ノイズ、高 PSRR、および非常に優れた負荷ライン過渡性能を実現できるよう設計されています。革新的な設計手法を採用した TPS7A20L は、ノイズ バイパス コンデンサを追加しなくても超低ノイズ性能を発揮します。TPS7A20L は、静止電流が小さいという利点も備えているため、バッテリ駆動のアプリケーションに役立ちます。1.6V～6.0V の入力電圧範囲と 0.8V～5.5V の出力電圧範囲を持つ TPS7A20L は幅広いアプリケーションに使用できます。本デバイスは、負荷、ライン、温度の変化に対して誤差 1.5% 以下の精度を達成するために高精度の基準電圧回路を使用しています。

TPS7A20L は、突入電流を低減させるための内部ソフトスタートを備えているため、スタートアップ時の入力電圧降下を最小限に抑えることができます。このデバイスは小さなセラミック コンデンサでも安定に動作するため、ソリューション全体を小型化できます。

TPS7A20L は、内部的に制御されるプルダウン抵抗を持つスマート イネーブル入力回路を備えています。EN ピンをフローティング状態のままにしていても、このプルダウン抵抗が LDO をディセーブル状態に維持するため、EN ピンをプルダウンするために使用する外付け部品は不要です。イネーブル入力ロジック スレッショルドは、1.2V ロジック デバイスの出力レベルと互換性があります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS7A20L	DQN (X2SON、4)	1mm × 1mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

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4 Pin Configuration and Functions

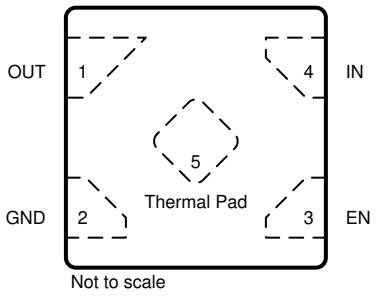


図 4-1. DQN Package, 4-Pin X2SON (Top View)

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	X2SON		
EN	3	I	Enable input. A low voltage (< $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When V_{EN} > $V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current.
GND	2	G	Common ground.
IN	4	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode (V_{EN}< $V_{EN(LOW)}$).
Thermal Pad	5	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

(1) I = Input, O = output, G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{OUT}	–0.3	6.5 or V_{IN} + 0.3 (2)	
	V_{EN}	–0.3	6.5	
Current	Maximum output(4)	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum value of V_{OUT} is the lesser of 6.5 V or (V_{IN} + 0.3 V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.6		6.0	V
V_{EN}	Enable input voltage	0		6.0	V
V_{OUT}	Nominal output voltage range	0.8		5.5	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor(2)		1		µF
C_{OUT}	Output capacitor(3)	1		200	µF
ESR	Output capacitor effective series resistance			100	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
(3) Effective output capacitance of 0.47 µF minimum and 200 µF maximum is required for stability.

5.4 Thermal Information

THERMAL METRIC[1]		TPS7A20L DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	166.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	103.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	98.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA, V_{OUT} ≥ 1.85 V		–1.5		1.5	%
		V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA V_{OUT} < 1.85 V		–30		30	mV
ΔV_{OUT}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA			0.03		%/V
ΔV_{OUT}	Load regulation	I_{OUT} = 1 mA to 300 mA			13		mV
I_{GND}	Quiescent ground current	V_{EN} = V_{IN} = 6 V, I_{OUT} = 0 mA	T_J = 25°C		6.5	8.5	µA
			T_J = –40°C to 85°C			10	
			T_J = –40°C to 125°C			15	
		V_{EN} = V_{IN} = 6 V, I_{OUT} = 300 mA			2000		
I_{SHDN}	Shutdown ground current	V_{EN} = 0 V (disabled), V_{IN} = 6.0 V, T_J = 25°C			0.07	0.2	µA
$I_{GND(DO)}$	I_{GND} in dropout	V_{IN} ≤ $V_{OUT(NOM)}$, I_{OUT} = 0 mA, V_{EN} = V_{IN}			6.5	15	µA
V_{DO}	Dropout voltage	I_{OUT} = 300 mA, V_{OUT} = 95% x $V_{OUT(NOM)}$,	0.8 V ≤ V_{OUT} < 1.0 V[1]			690	mV
			1.0 V ≤ V_{OUT} < 1.2 V[1]			490	
			1.2 V ≤ V_{OUT} < 1.5 V[1]			355	
			1.5 V ≤ V_{OUT} < 2.5 V			200	
			2.5 V ≤ V_{OUT} < 5.5 V			140	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V	V_{OUT} < 1.5 V	360	520	730	mA
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V	V_{OUT} ≥ 1.5 V	360	520	730	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			160		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 20 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		95		dB
			f = 1 kHz		95		
			f = 10 kHz		75		
			f = 100 kHz		75		
			f = 1 MHz		45		
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		65		
			f = 1 kHz		92		
			f = 10 kHz		75		
			f = 100 kHz		60		
			f = 1 MHz		40		

5.5 Electrical Characteristics (続き)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	I_{OUT} = 300 mA		7		μV_{RMS}
			I_{OUT} = 1 mA		10		
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled), V_{IN} = 3.1 V			150		Ω
T_{SD}	Thermal shutdown	T_J rising			165		°C
		T_J falling			140		
$V_{EN(LOW)}$	Low input threshold	V_{IN} = 1.6 V to 6.0 V, V_{EN} falling until the output is disabled				0.43	V
$V_{EN(HI)}$	High input threshold	V_{IN} = 1.6 V to 6.0 V V_{EN} rising until the output is enabled		0.75			V
V_{UVLO}	UVLO threshold	V_{IN} rising		1.17	1.35	1.59	V
		V_{IN} falling		1.11	1.3	1.55	
$V_{UVLO(HYST)}$	UVLO hysteresis				50		mV
I_{EN}	EN input leakage current	V_{EN} = 6.0 V and V_{IN} = 6.0 V			90	250	nA
$R_{EN(PULL-DOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.25 V			500		KΩ

(1) Design simulation data only

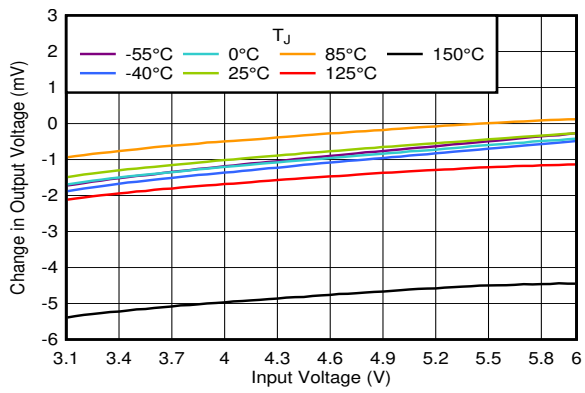
5.6 Switching Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN}= 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$		750	1150	µs

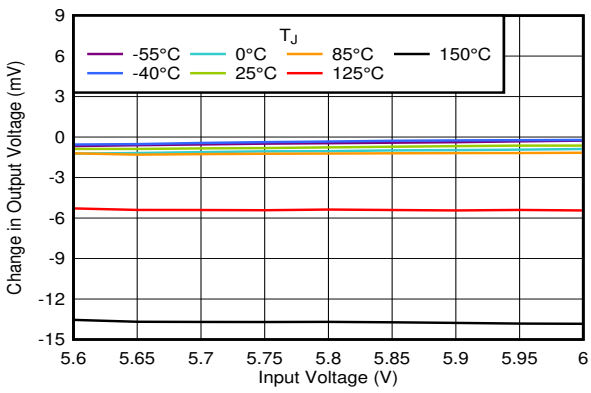
5.7 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



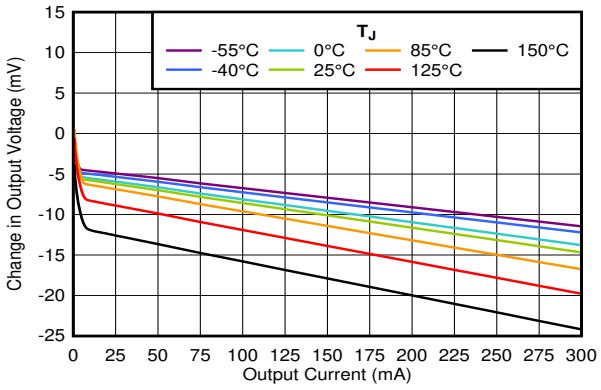
V_{EN} = 1 V

図 5-1. Line Regulation vs V_{IN}



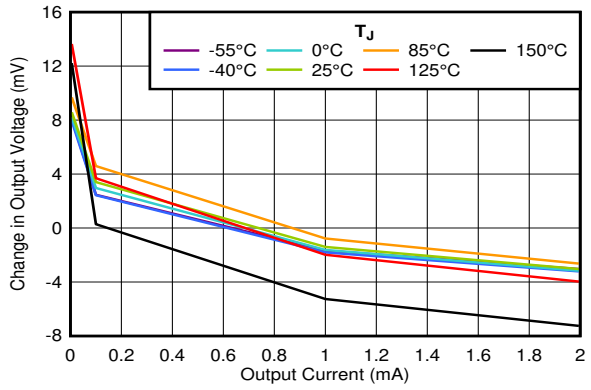
V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-2. Line Regulation vs V_{IN}



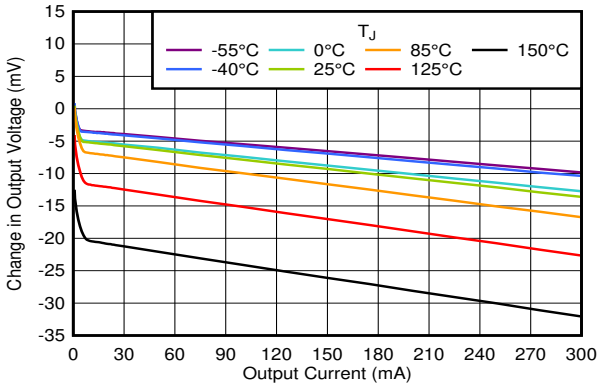
V_{IN} = 3.1 V, V_{EN} = 1 V

図 5-3. Load Regulation vs I_{OUT}



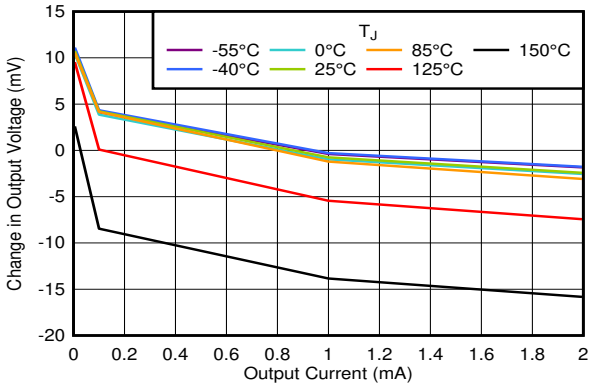
V_{IN} = 3.1 V, V_{EN} = 1 V

図 5-4. Load Regulation vs I_{OUT}



V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-5. Load Regulation vs I_{OUT}

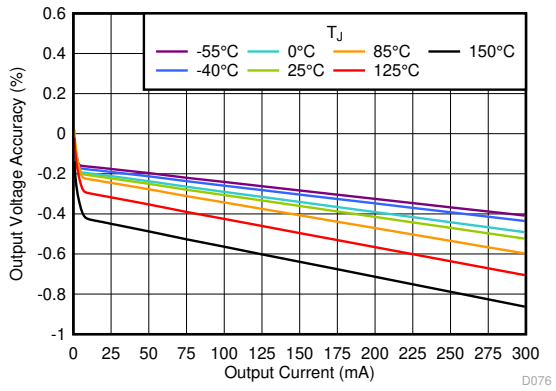


V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-6. Load Regulation vs I_{OUT}

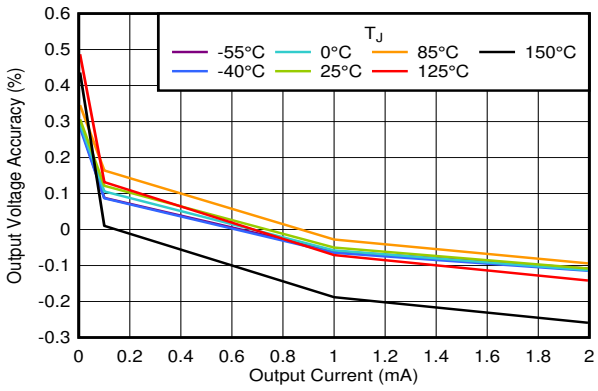
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



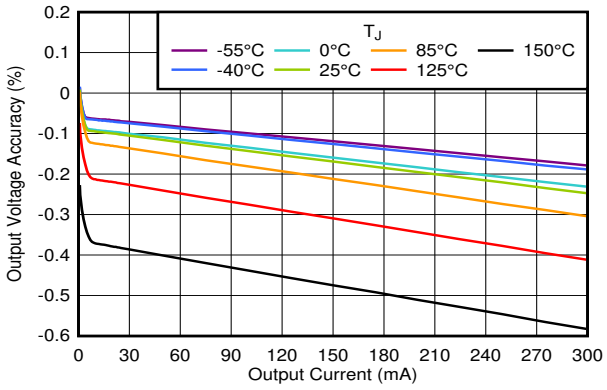
V_{EN} = 1 V

図 5-7. Output Voltage Accuracy vs I_{OUT}



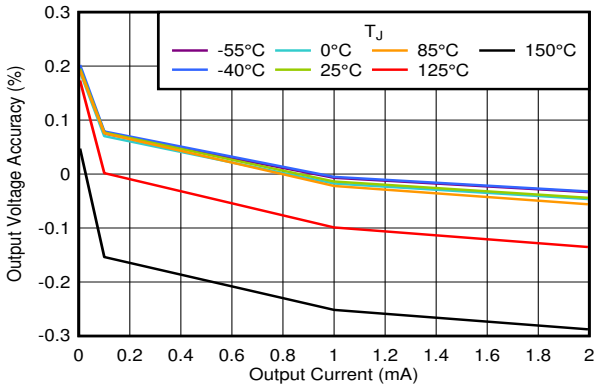
V_{EN} = 1 V

図 5-8. Output Voltage Accuracy vs I_{OUT}



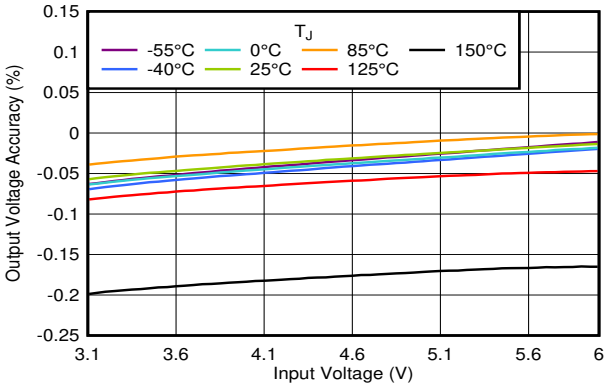
V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-9. Output Voltage Accuracy vs I_{OUT}



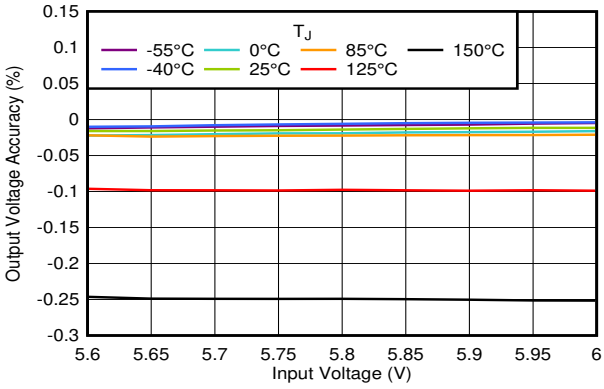
V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-10. Output Voltage Accuracy vs I_{OUT}



V_{EN} = 1 V, I_{OUT} = 1 mA

図 5-11. Output Voltage Accuracy vs V_{IN}

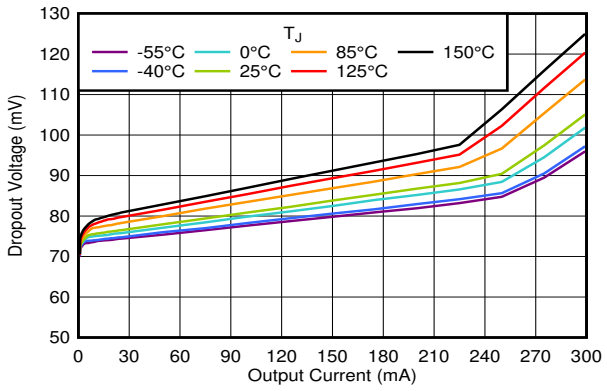


V_{OUT} = 5.5 V, V_{EN} = 1 V

図 5-12. Output Voltage Accuracy vs V_{IN}

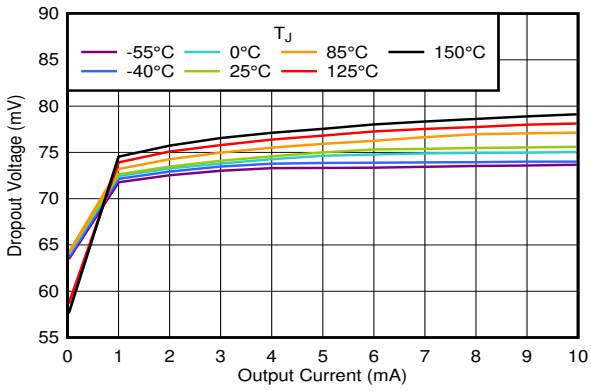
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



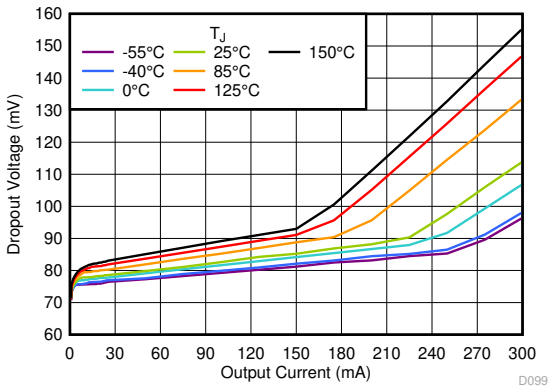
V_{EN} = 1 V

図 5-13. Dropout Voltage vs I_{OUT}



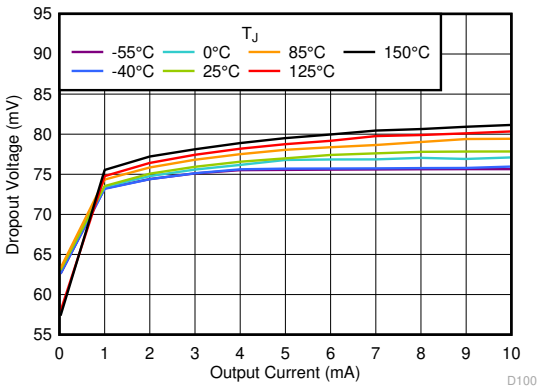
V_{EN} = 1 V

図 5-14. Dropout Voltage vs I_{OUT}



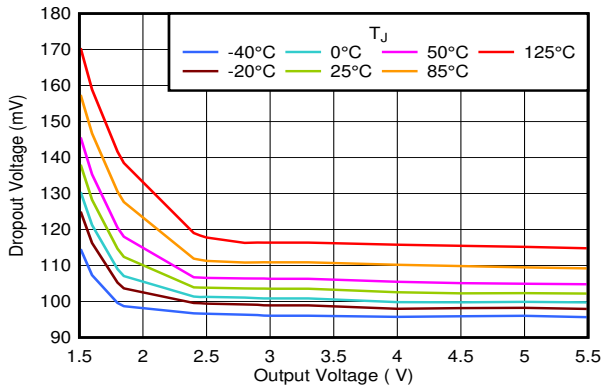
V_{OUT} = 1.8 V, V_{EN} = 1 V

図 5-15. Dropout Voltage vs I_{OUT}



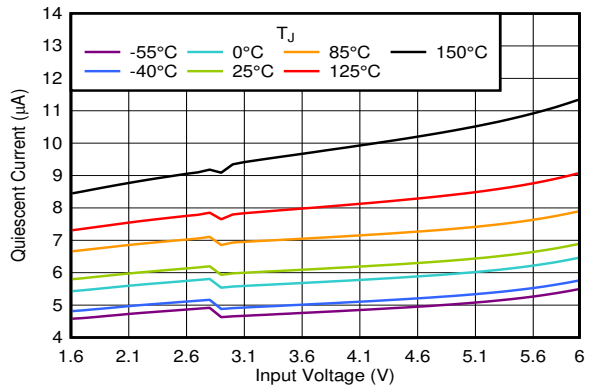
V_{OUT} = 1.8 V, V_{EN} = 1 V

図 5-16. Dropout Voltage vs I_{OUT}



I_{OUT} = 300 mA

図 5-17. Dropout Voltage vs V_{OUT}

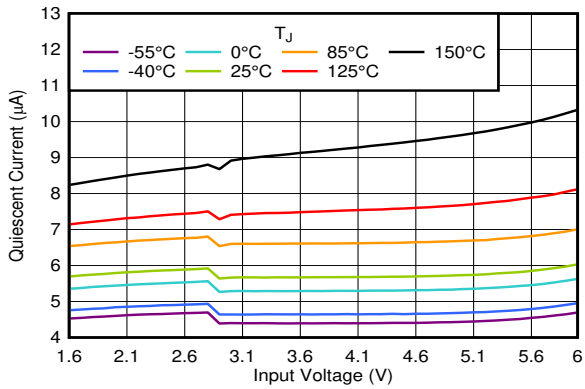


V_{EN} = 1 V, I_{OUT} = 0 mA

図 5-18. I_{GND} vs V_{IN}

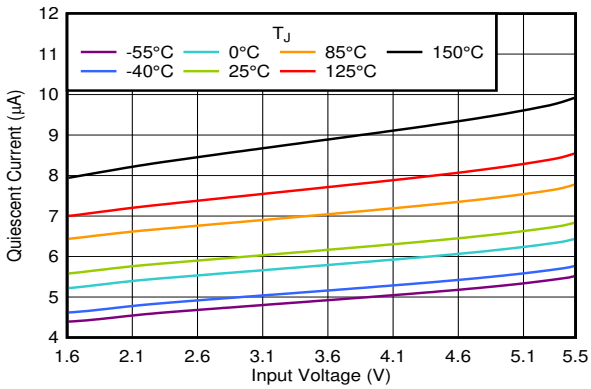
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



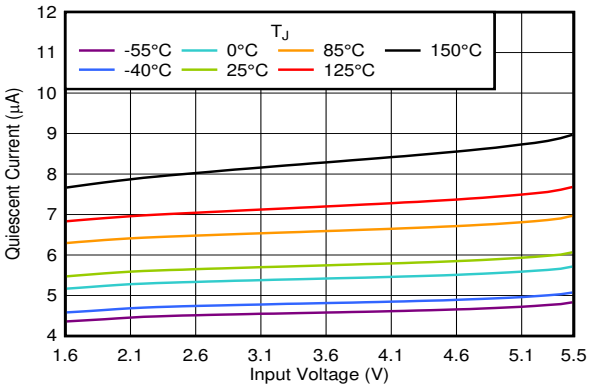
V_{EN} = V_{IN}, I_{OUT} = 0 mA

図 5-19. I_{GND} vs V_{IN}



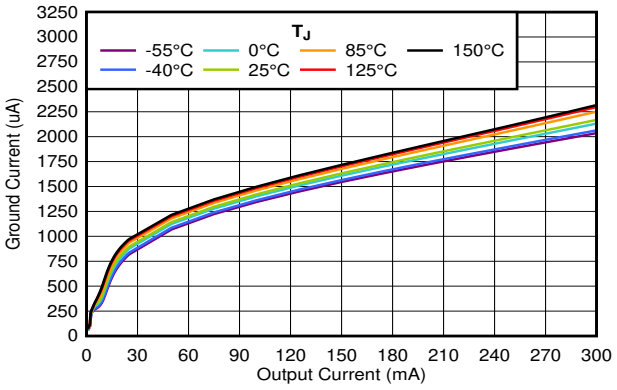
$V_{OUT(NOM)}$ = 5.5 V, V_{EN} = 1 V, I_{OUT} = 0 mA

図 5-20. I_{GND} vs V_{IN} in the Dropout Region



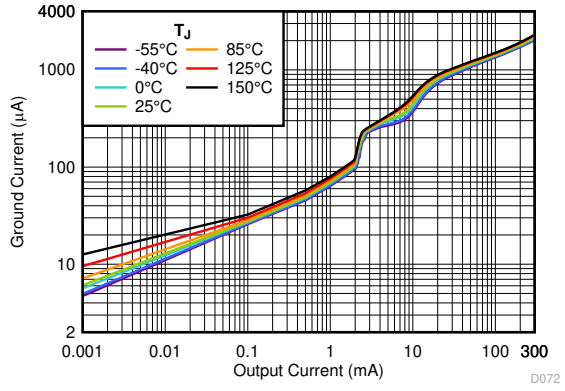
$V_{OUT(NOM)}$ = 5.5 V, V_{EN} = V_{IN}, I_{OUT} = 0 mA

図 5-21. I_{GND} vs V_{IN} in the Dropout Region



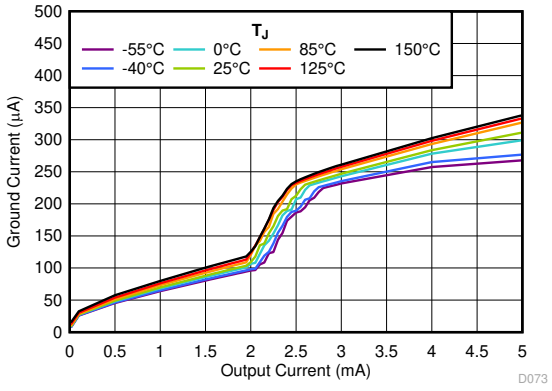
V_{EN} = 1 V

図 5-22. I_{GND} vs I_{OUT}



V_{EN} = 1 V

図 5-23. I_{GND} vs I_{OUT}

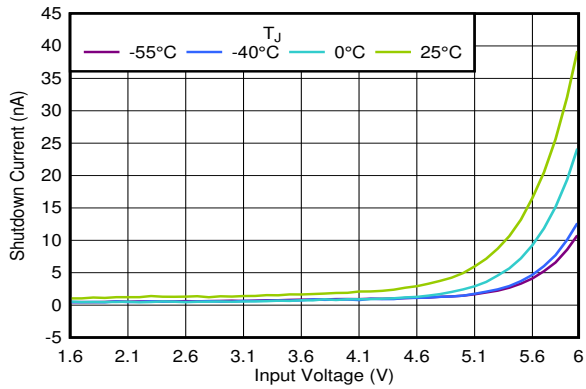


V_{EN} = 1 V

図 5-24. I_{GND} vs I_{OUT}

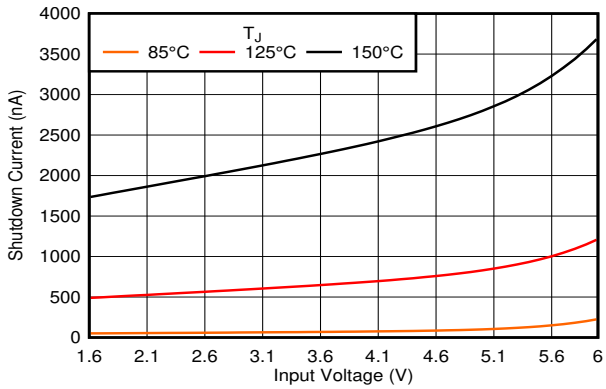
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



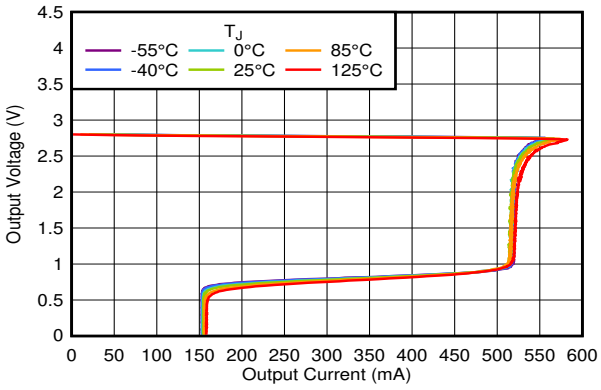
V_{EN} = 0 V

図 5-25. Shutdown Current vs V_{IN}



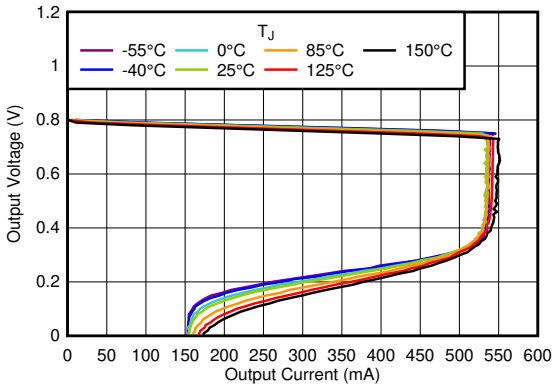
V_{EN} = 0 V

図 5-26. Shutdown Current vs V_{IN}



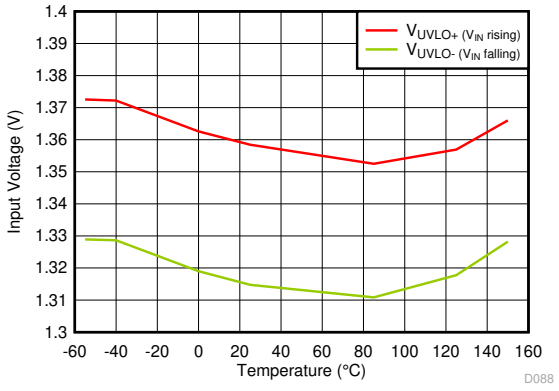
V_{EN} = 1 V

図 5-27. Current Limit



V_{OUT} = 0.8 V, V_{EN} = 1 V

図 5-28. Current Limit



V_{EN} = 1 V

図 5-29. UVLO Threshold vs Temperature

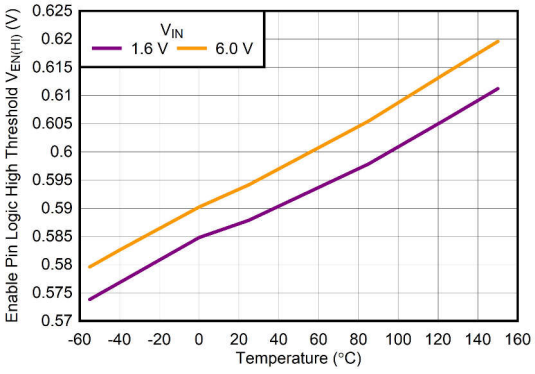


図 5-30. Enable Logic High Threshold vs Temperature

5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)

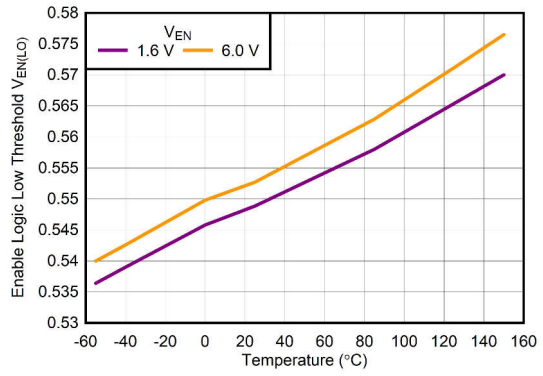
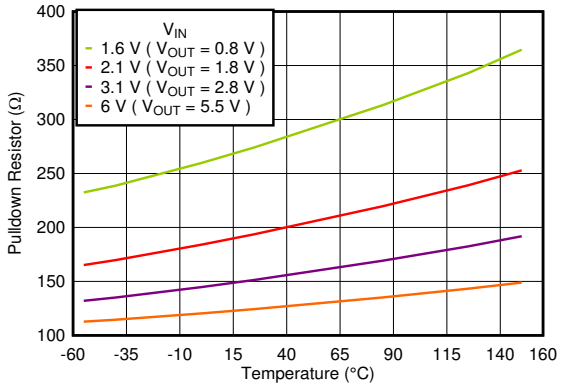
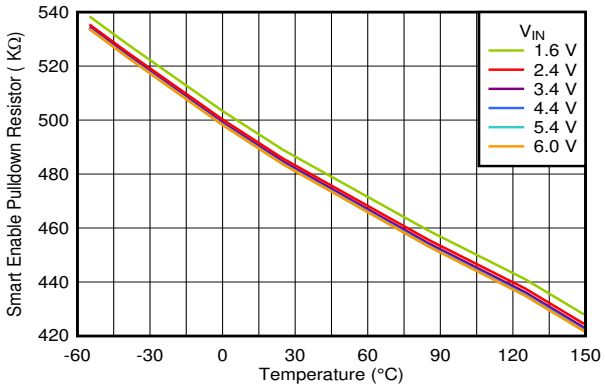


図 5-31. Enable Logic Low Threshold vs Temperature



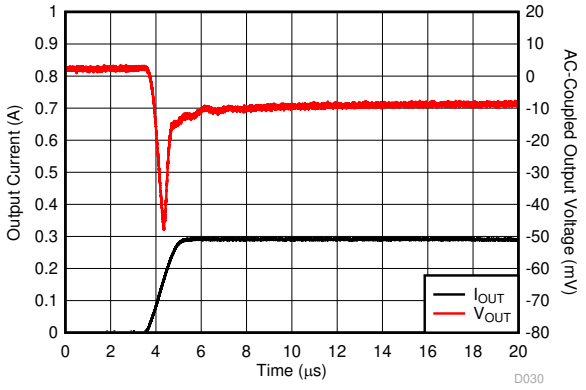
V_{EN} = 0.25 V

図 5-32. Output Pulldown Resistor vs Temperature



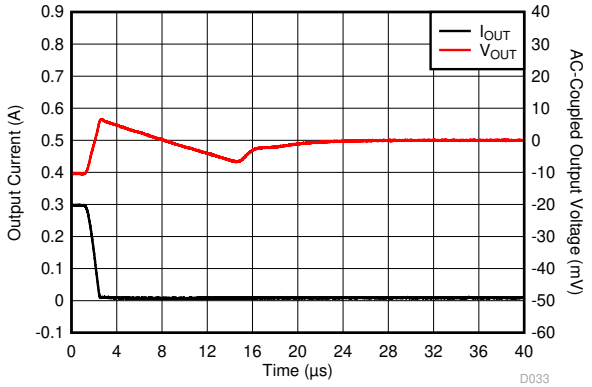
V_{EN} = 0.25 V

図 5-33. Smart Enable Pulldown Resistor vs Temperature and V_{IN}



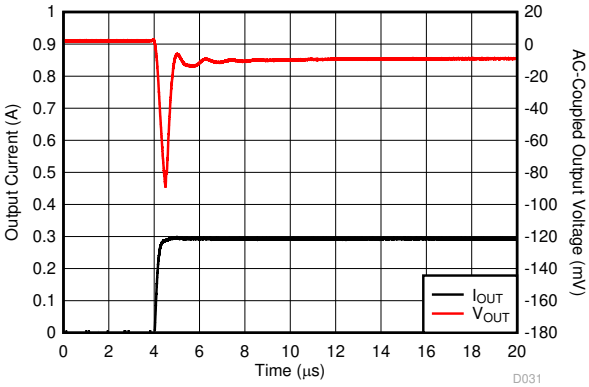
I_{OUT} = 1 mA to 300 mA, t_{RISING} = 1 µs

図 5-34. Load Transient



I_{OUT} = 300 mA to 1 mA, $t_{FALLING}$ = 1 µs

図 5-35. Load Transient

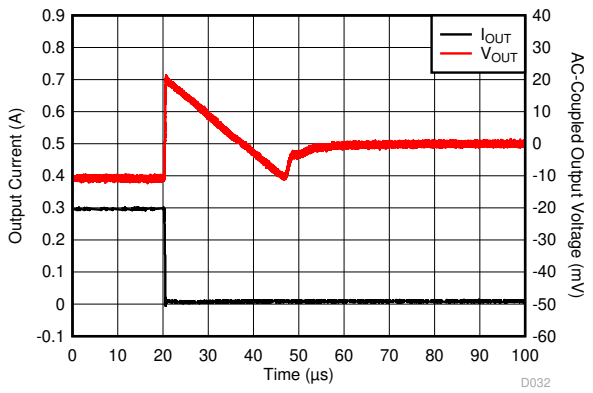


I_{OUT} = 1 mA to 300 mA, t_{RISING} = 200 ns

図 5-36. Load Transient

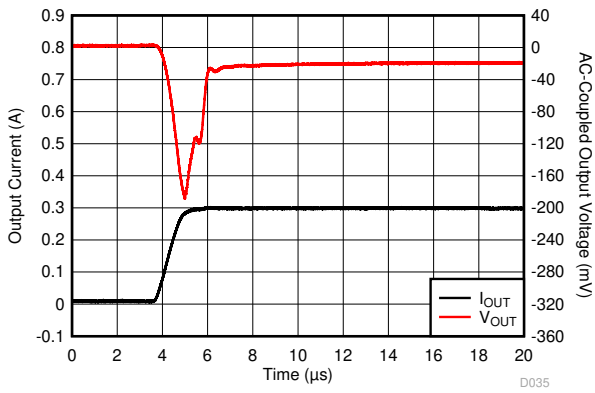
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



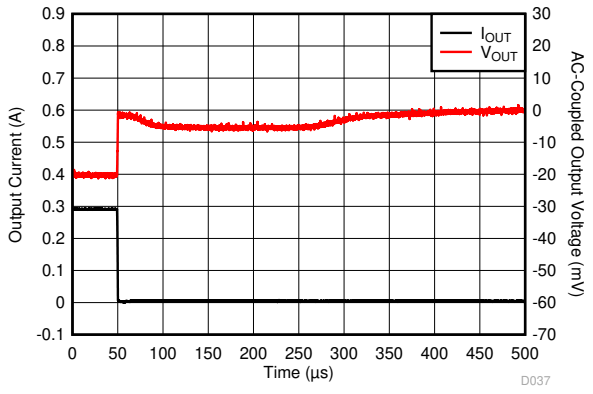
I_{OUT} = 300 mA to 1 mA, $t_{FALLING}$ = 200 ns

図 5-37. Load Transient



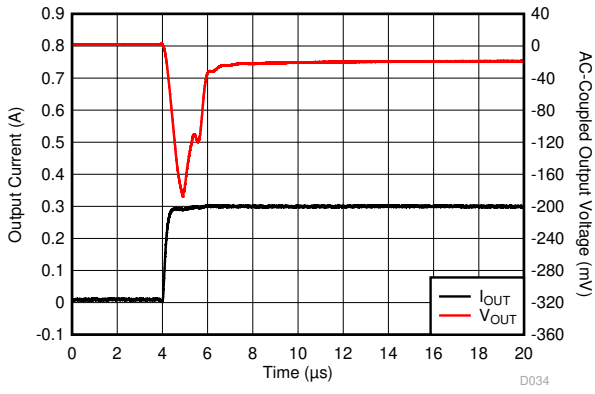
I_{OUT} = 0 mA to 300 mA, t_{RISING} = 1 µs

図 5-38. Load Transient



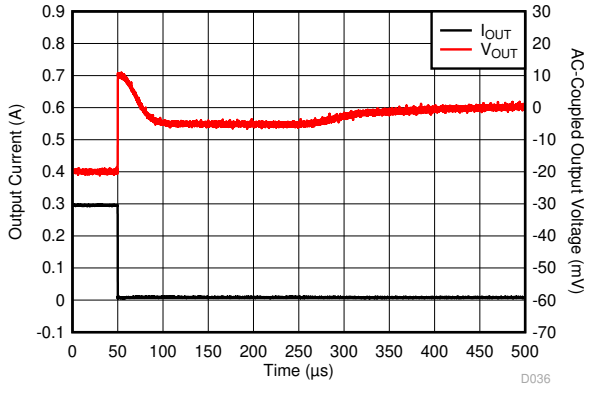
I_{OUT} = 300 mA to 0 mA, $t_{FALLING}$ = 1 µs

図 5-39. Load Transient



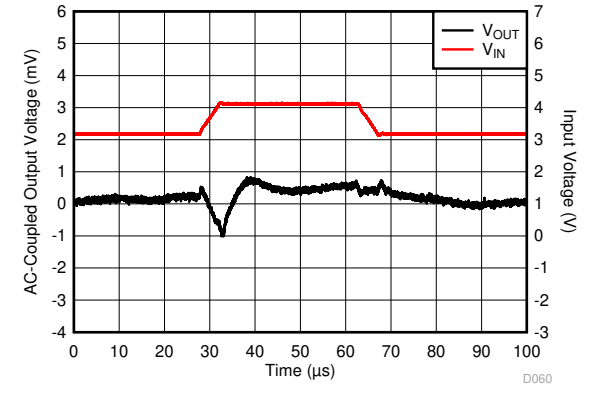
I_{OUT} = 0 mA to 300 mA, t_{RISING} = 200 ns

図 5-40. Load Transient



I_{OUT} = 300 mA to 0 mA, $t_{FALLING}$ = 200 ns

図 5-41. Load Transient

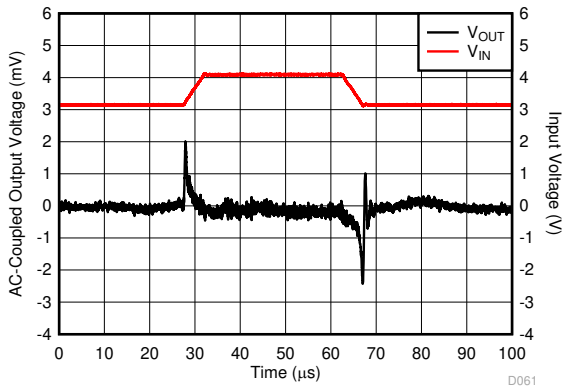


V_{IN} = 3.1 V → 4.1 V → 3.1 V, V_{IN} t_{RISING} = 5 µs, I_{OUT} = 1 mA

図 5-42. Line Transient

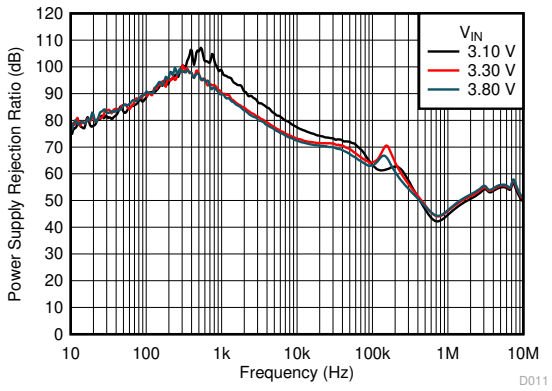
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



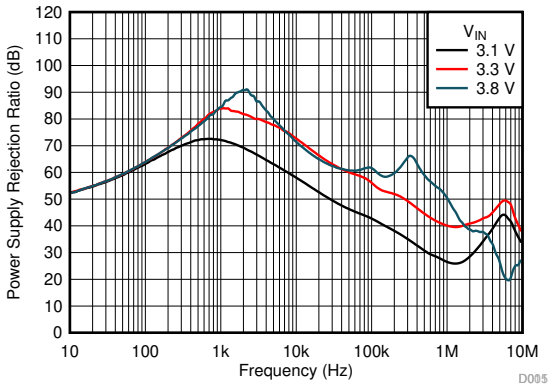
V_{IN} = 3.1 V → 4.1 V → 3.1 V, V_{IN} t_{RISING} = 5 µs,
I_{OUT} = 300 mA

図 5-43. Line Transient



I_{OUT} = 20 mA

図 5-44. PSRR vs V_{IN} vs Frequency and V_{IN}



I_{OUT} = 300 mA

図 5-45. PSRR vs Frequency and V_{IN}

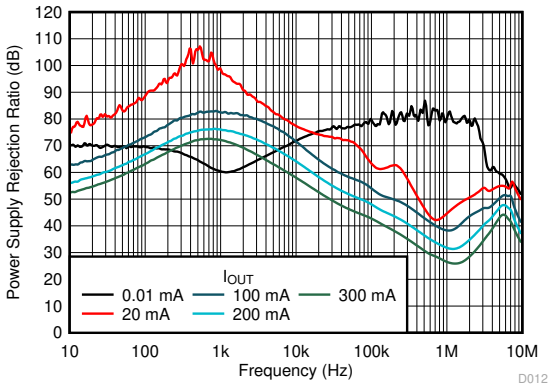
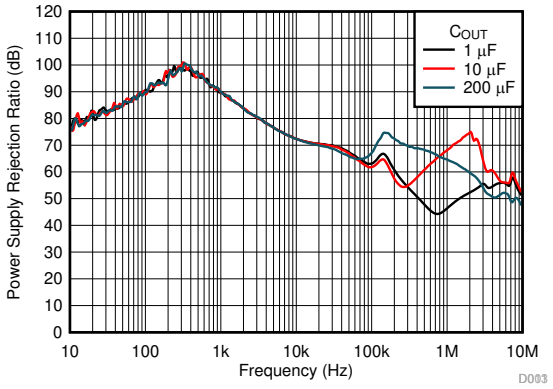
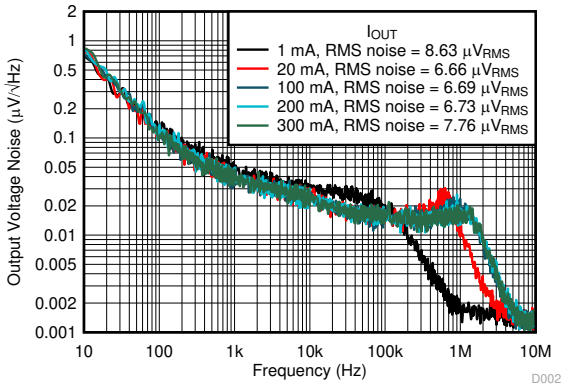


図 5-46. PSRR vs Frequency and I_{OUT}



I_{OUT} = 20 mA

図 5-47. PSRR vs Frequency and C_{OUT}

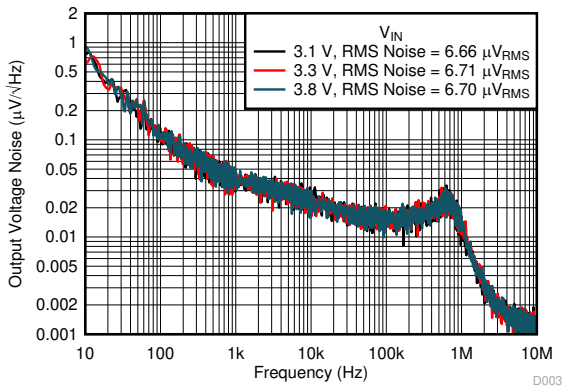


V_{RMS} BW = 10 Hz to 100 kHz

図 5-48. Noise vs Frequency and I_{OUT}

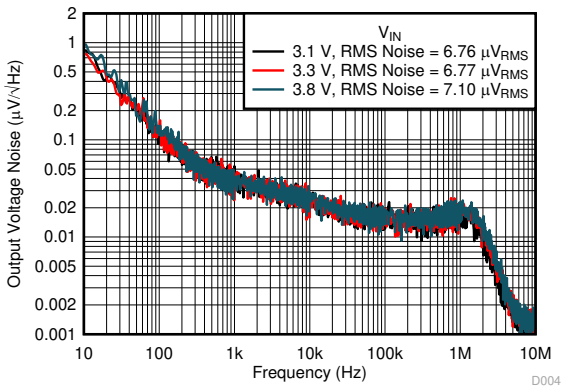
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



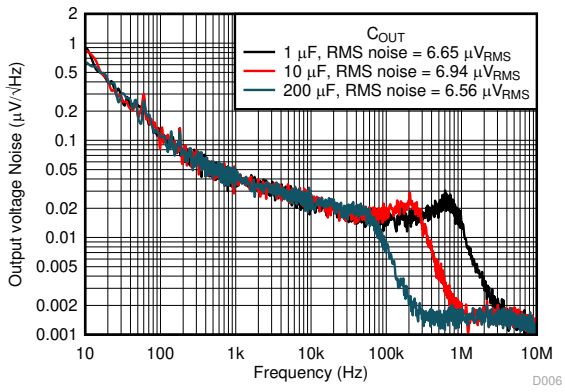
I_{OUT} = 20 mA, V_{RMS} BW = 10 Hz to 100 kHz

図 5-49. Noise vs Frequency and V_{IN}



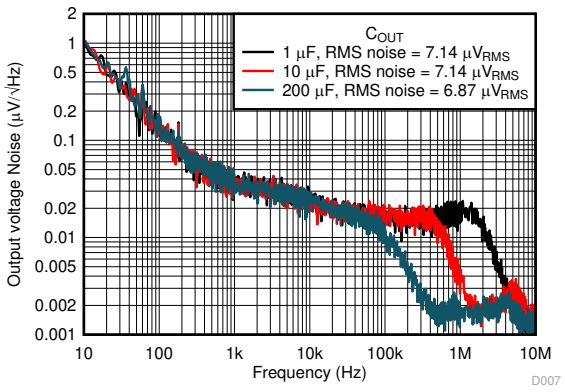
I_{OUT} = 300 mA, V_{RMS} BW = 10 Hz to 100 kHz

図 5-50. Noise vs Frequency and V_{IN}



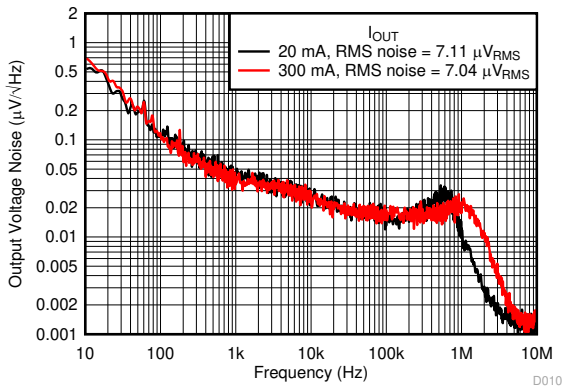
V_{IN} = 3.8 V, I_{OUT} = 20 mA, V_{RMS} BW = 10 Hz to 100 kHz

図 5-51. Noise vs Frequency and C_{OUT}



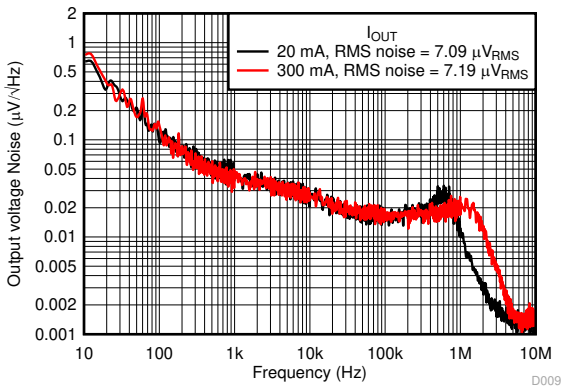
V_{IN} = 3.8 V, I_{OUT} = 300 mA, V_{RMS} BW = 10 Hz to 100 kHz

図 5-52. Noise vs Frequency and C_{OUT}



V_{OUT} = 0.8 V, V_{RMS} BW = 10 Hz to 100 kHz

図 5-53. Noise vs Frequency and I_{OUT}

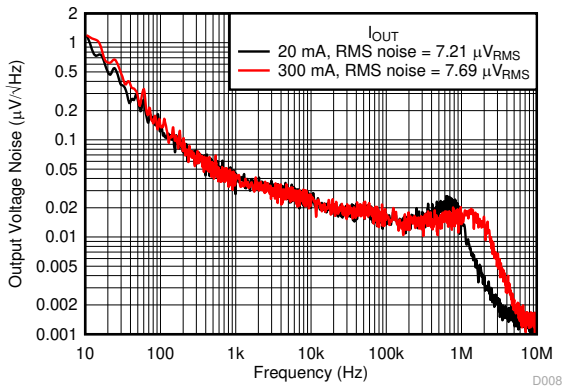


V_{OUT} = 0.8 V, V_{IN} = 1.8 V, V_{RMS} BW = 10 Hz to 100 kHz

図 5-54. Noise vs Frequency and I_{OUT}

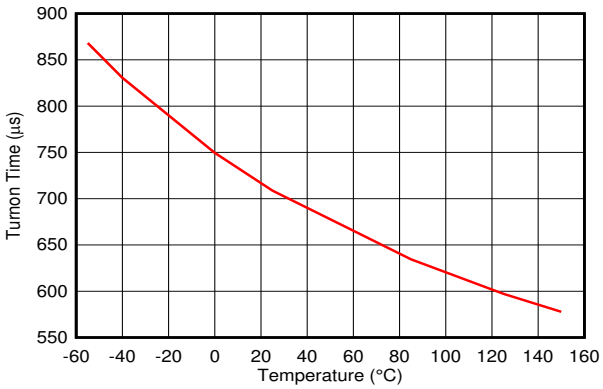
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



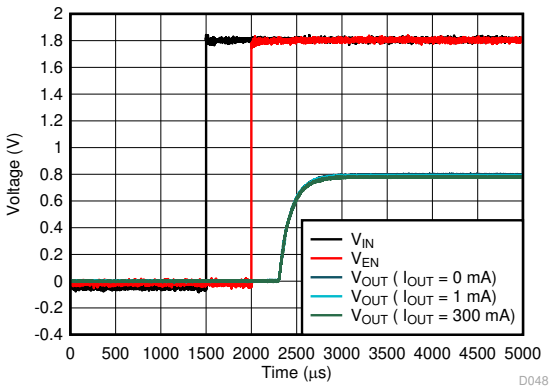
V_{OUT} = 5.5 V, V_{IN} = 6 V, V_{RMS} BW = 10 Hz to 100 kHz

図 5-55. Noise vs Frequency and I_{OUT}



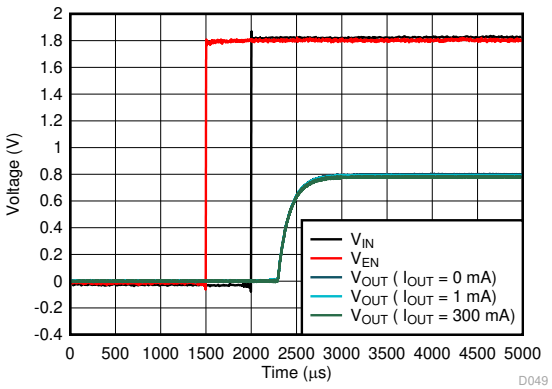
From V_{EN} = $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, I_{OUT} = 0 mA

図 5-56. Start-Up Turn-On Time



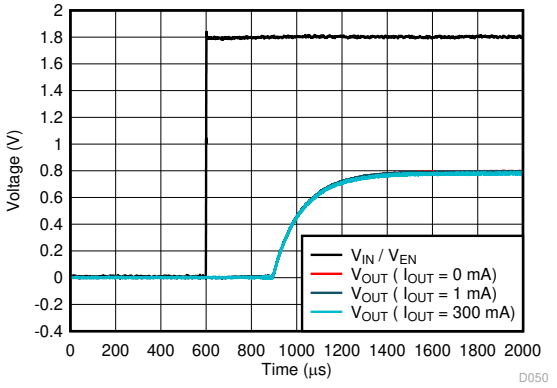
V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} rises 500 µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-57. Start-Up



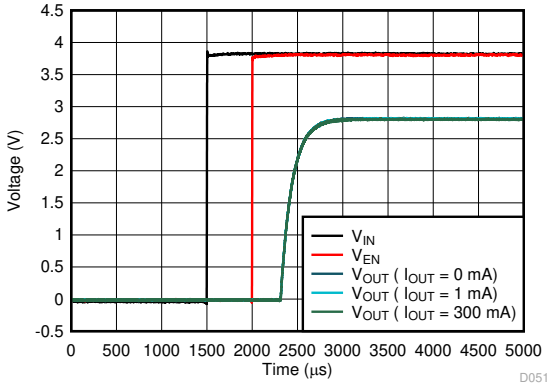
V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} rises 500 µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-58. Start-Up



V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = V_{IN}, V_{IN} slew rate = 1 V/µs

図 5-59. Start-Up

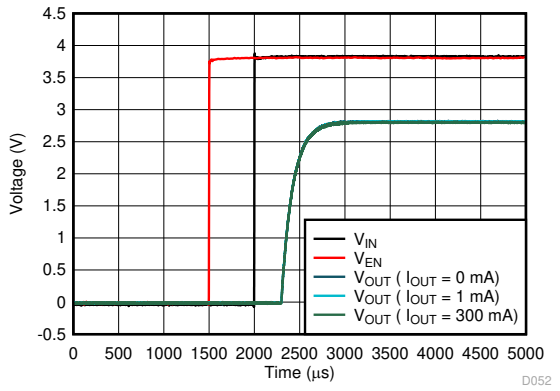


V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} rises 500 µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-60. Start-Up

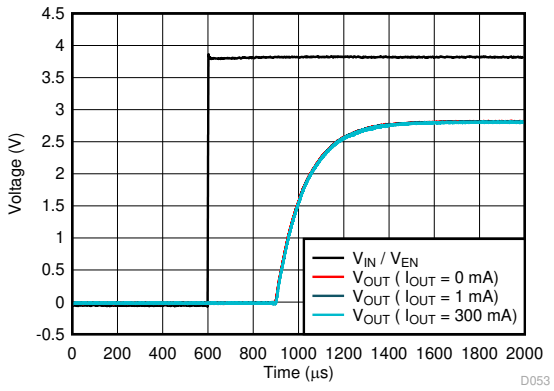
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



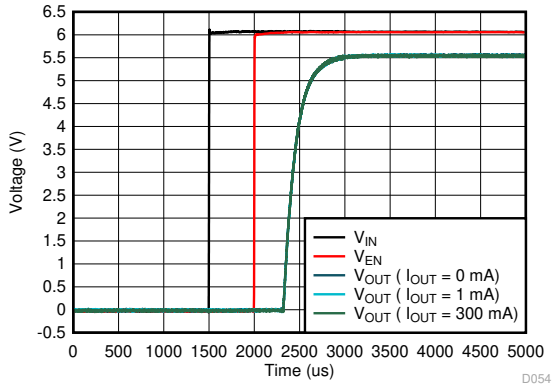
V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} rises 500 µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-61. Start-Up



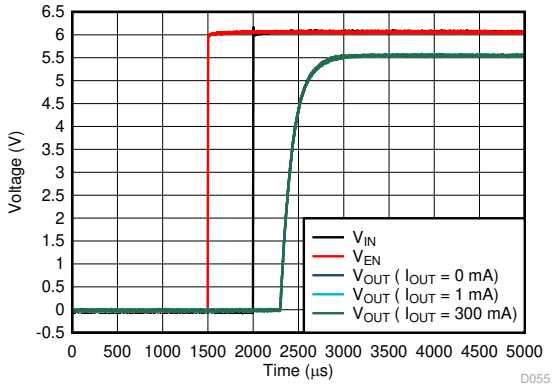
V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} = V_{IN}, V_{IN} and slew rate = 1 V/µs

図 5-62. Start-Up



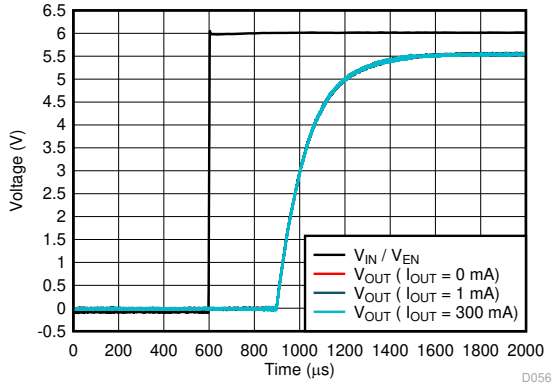
V_{OUT} = 5.5 V, V_{IN} = 0 V to 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} rises 500 µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-63. Start-Up



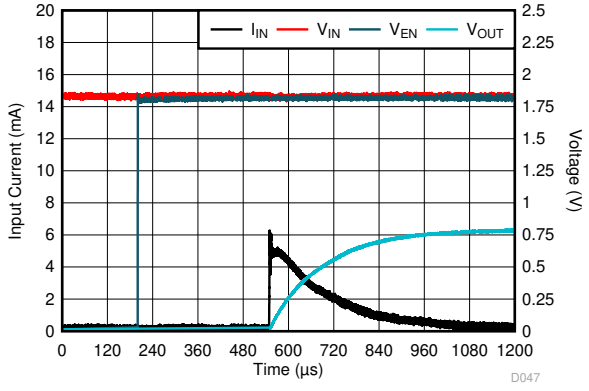
V_{OUT} = 5.5 V, V_{IN} = 0 V to 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} rises 500 µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 5-64. Start-Up



V_{OUT} = 5.5 V, V_{IN} = 0 V to 6 V, V_{EN} = V_{IN}, V_{IN} slew rate = 1 V/µs

図 5-65. Start-Up

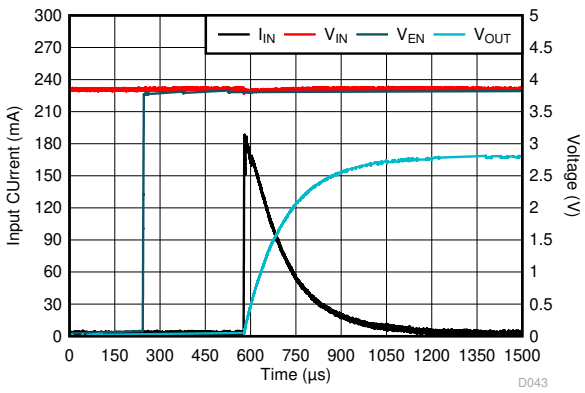


V_{OUT} = 0.8 V, V_{IN} = 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} slew rate = 1 V/µs, C_{OUT} = 10 µF

図 5-66. Inrush Current

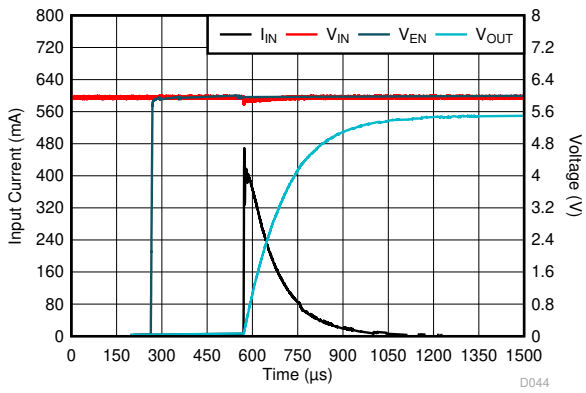
5.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



V_{IN} = 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} slew rate = 1 V/µs, C_{OUT} = 10 µF

図 5-67. Inrush Current



V_{OUT} = 5.5 V, V_{IN} = 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} slew rate = 1 V/µs, C_{OUT} = 10 µF

図 5-68. Inrush Current

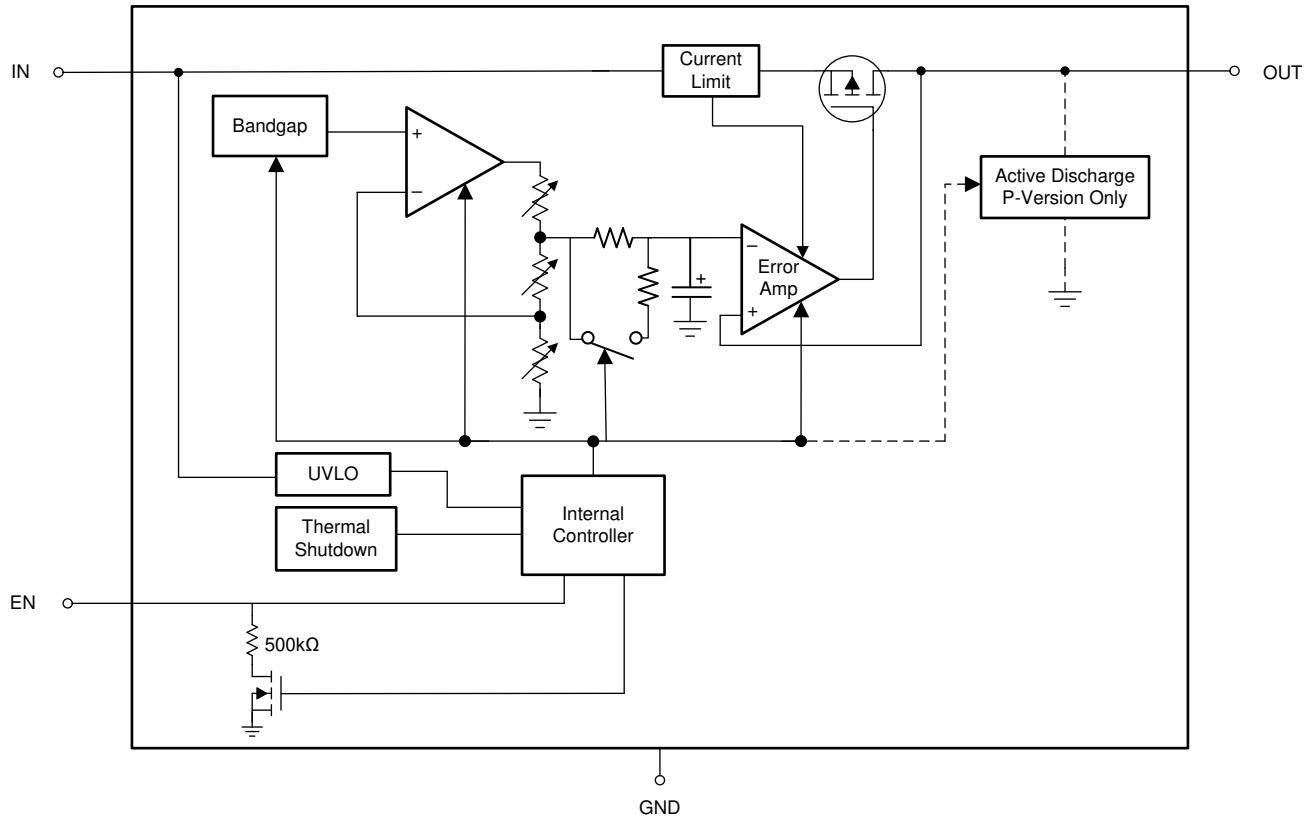
6 Detailed Description

6.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A20L provides low noise, high PSRR, low quiescent current, and low line and load transient response figures. Using innovative design techniques, the TPS7A20L offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20L is designed to operate with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Output Noise

Any internal noise at the TPS7A20L reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cutoff frequency of approximately 0.1 Hz.

During start-up, the filter resistor is bypassed to reduce output rise time; the filter begins normal operation after the output voltage reaches the correct value.

6.3.2 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

6.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the foldback current limit.

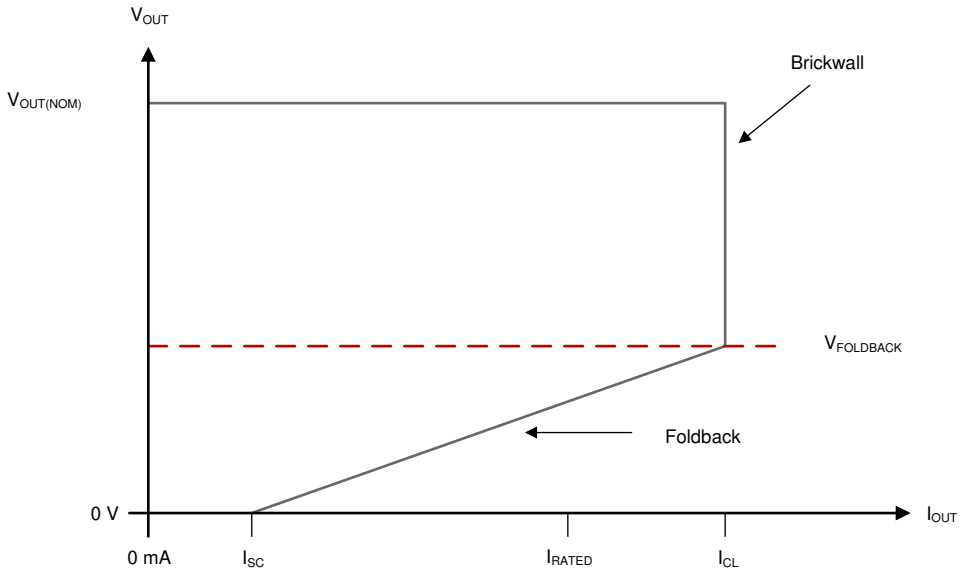


図 6-1. Foldback Current Limit

6.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.6 Thermal Shutdown

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.7 Active Discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. The active discharge circuit is activated by driving EN low or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the LDO can be shut down by driving EN to less than $V_{EN(LOW)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit between OUT and ground.

7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although the LDO is stable without an input capacitor, good analog design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 Ω. When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system can be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum can be necessary if large, fast-rise-time load or line transients are anticipated or if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps provide stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

7.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 図 7-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady state.

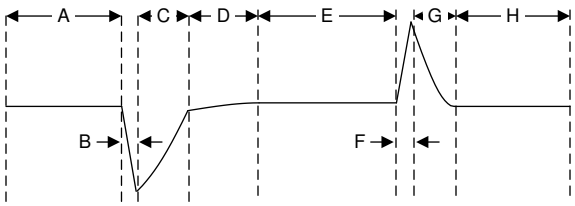

図 7-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure that the device stays disabled before the input supply reaches the minimum operational voltage range, and makes sure that the device shuts down when the input supply collapses. 図 7-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

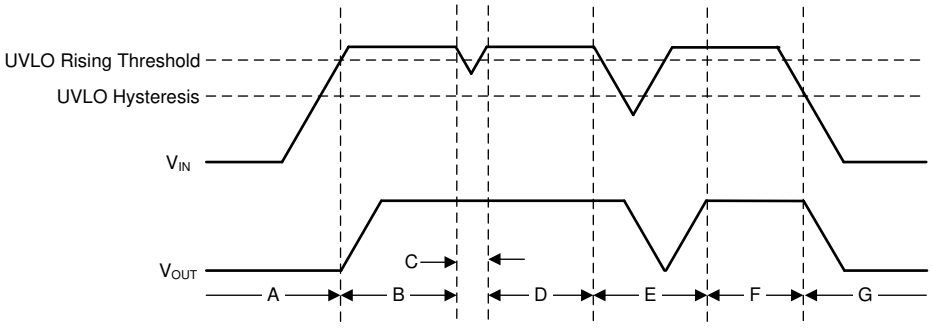

図 7-2. Typical UVLO Operation

7.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 式 4 rearranges 式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

7.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- P_D is the power dissipated as explained in 式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

7.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 7-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 式 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

図 7-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

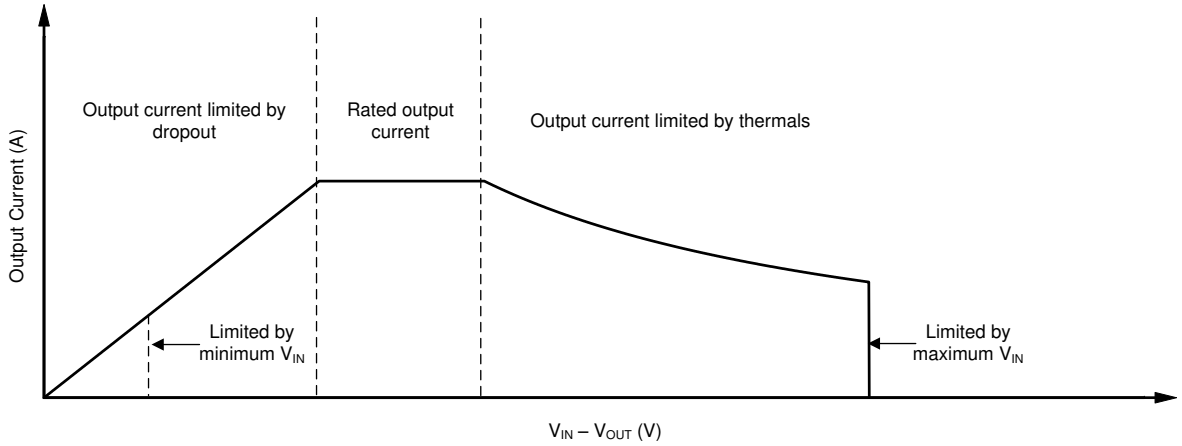

図 7-3. Region Description of Continuous Operation Regime

7.2 Typical Application

図 7-4 shows the typical application circuit for the TPS7A20. If needed, increase the input and output capacitances above the 1-µF minimum.

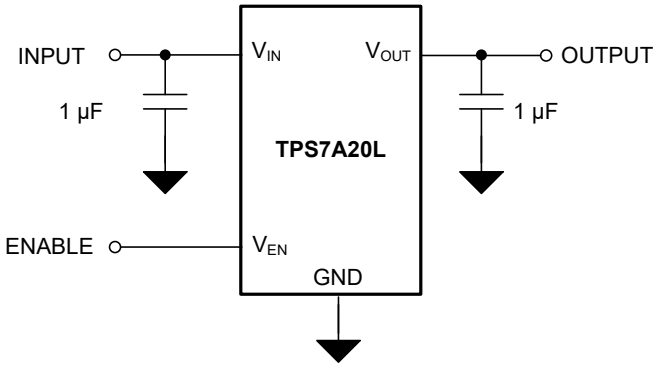

図 7-4. TPS7A20L Typical Application

7.2.1 Design Requirements

表 7-1 summarizes the design requirements for 図 7-4.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.1 V to 3.6 V
Output voltage	2.8 V
Output current	200 mA
Maximum ambient temperature	85°C

7.2.2 Detailed Design Procedure

For this design example, the 2.8-V output version (TPS7A20L28) is selected. A nominal 3.3-V input supply is assumed. Use a minimum 1.0-µF input capacitor to minimize the effect of resistance and inductance between the 3.3-V source and the LDO input. Use a minimum 1.0-µF output capacitor for stability and good load transient response. The dropout voltage (V_{DO}) is less than 140 mV maximum at a 2.8-V output voltage and 300-mA

output current, so there are no dropout issues with a minimum input voltage of 3.0 V and a maximum output current of 200 mA.

7.2.3 Application Curves

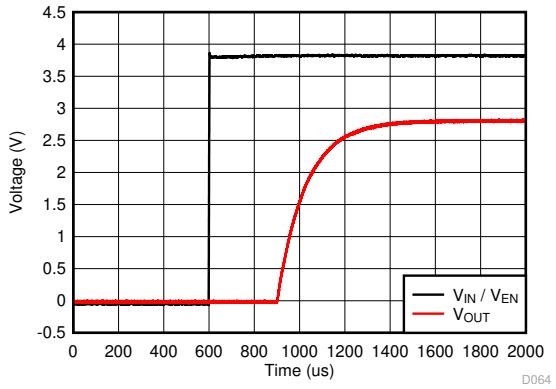

図 7-5. Start-Up

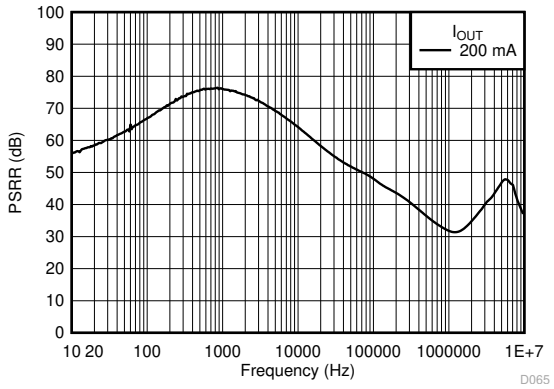

図 7-6. PSRR

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.3 V or 1.6 V, whichever is greater. Use a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Example

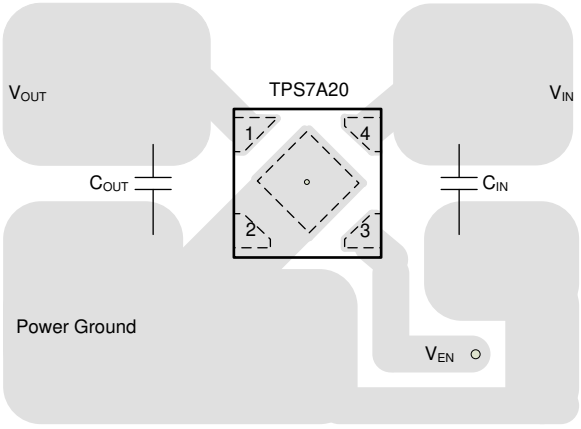

図 7-7. DQN Package (X2SON) Typical Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT (1) (2)	V_{OUT}
TPS7A20L**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TPS7A20L family actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces for DQN).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8 V to 5.5 V in 25-mV increments are available. Contact the factory for details and availability.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Universal Low-Dropout (LDO) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module* user guide
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.5 Trademarks

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8.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A20L10PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OU
TPS7A20L10PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OU
TPS7A20L12PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OV
TPS7A20L12PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OV
TPS7A20L18PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OW
TPS7A20L18PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OW
TPS7A20L28PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OX
TPS7A20L28PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OX
TPS7A20L33PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OZ
TPS7A20L33PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

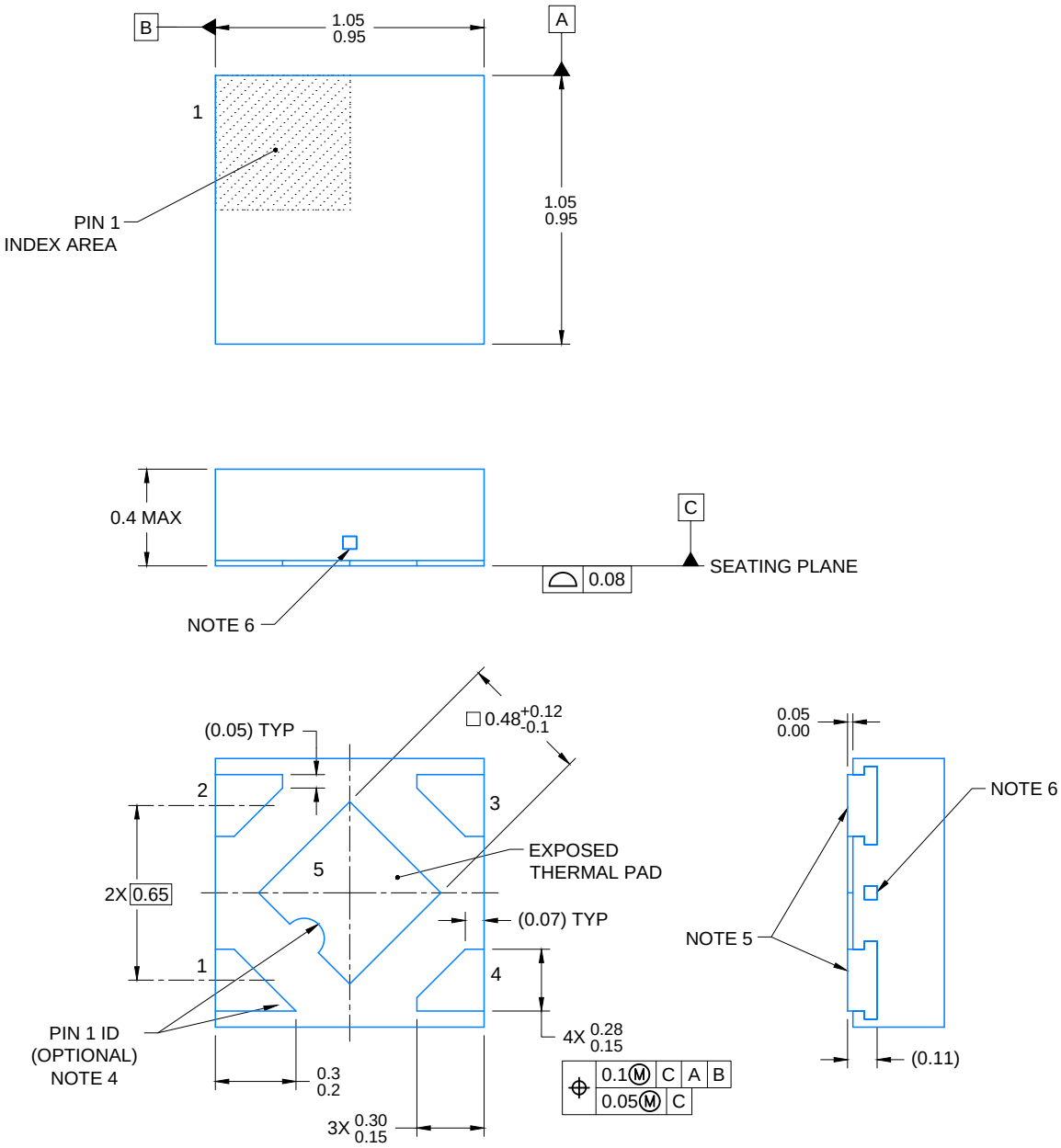
4210367/F

PACKAGE OUTLINE

DQN0004A

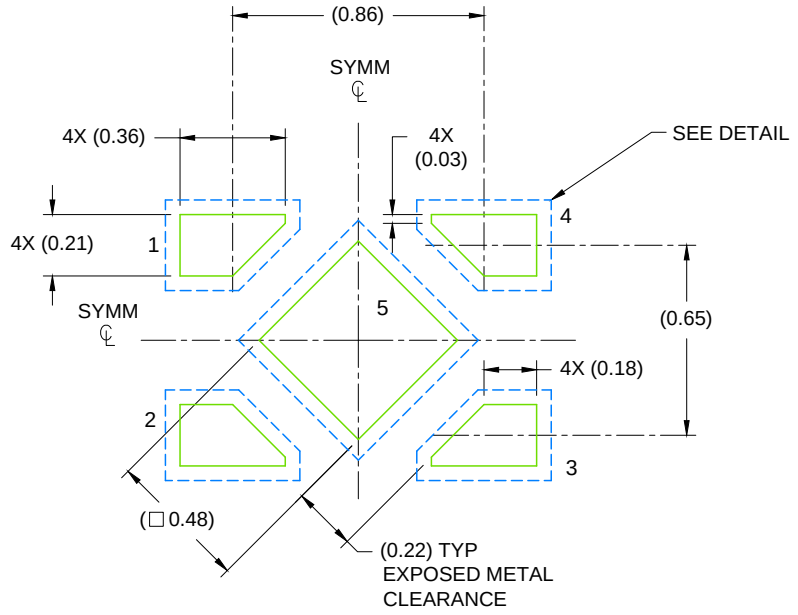
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



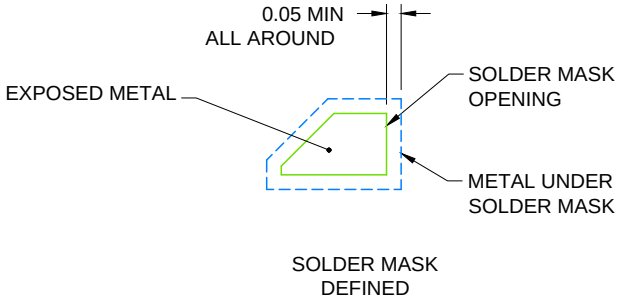
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

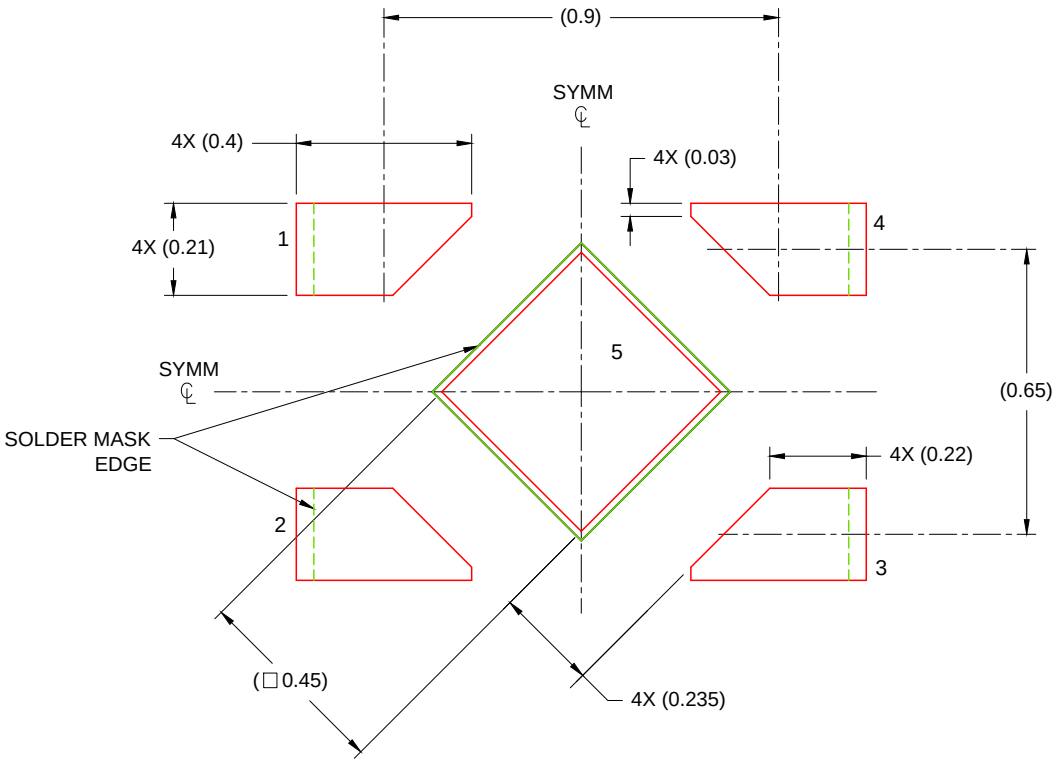


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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