TPS7A10 300mA、低V_{IN}、低V_{OUT}、超低ドロップアウト・レギュレータ

1 特長

- **非常に低い入力電圧範囲**: 0.75V～3.3V
- **非常に低いドロップアウトで最小限の電力損失**
  - 300mA (V_{OUT} > 1.0V)で70mV (最大値)、YKA パッケージ
- **低い静止電流**
  - V_{IN} I_Q = 1.6µA（標準値）
  - V_{BIAS} I_Q = 6µA（標準値）
- **すべての負荷、ライン、温度範囲での精度**: 1.5%
- **高いPSRR**：1kHzにおいて60dB
- **固定出力電圧で利用可能**
  - 0.5V～3.0V (50mV刻み)
- V_{BIAS}**範囲**: 1.7V～5.5V
- **パッケージ**
  - 0.74mm×1.09mm WCSP-5
  - 1.50mm×1.50mm WSON-6
- V_{OUT}**が単調増加するソフトスタートを内蔵**
- **アクティブ出力放電**

2 アプリケーション

- スマートウォッチ、フィットネス・トラッカー
- ワイヤレス・ヘッドホン/イヤホン
- カメラ・モジュール
- スマートフォンおよびタブレット
- ポータブル医療機器

3 概要

TPS7A10は超小型で静止電流が低い、低ドロップアウト・レギュレータ(LDO)であり、300mAを供給可能で、AC特性(負荷、ライン過渡応答)が非常に優れています。入力範囲は0.75V～3.3V、出力範囲は0.5V～3.0Vで、全負荷/ライン/温度範囲で1.5%という非常に高い精度を実現しています。この性能は、最新のMCUやアナログ・センサの低いコア電圧を供給するには理想的です。

主電源路はV_{IN}を経由し、出力電圧+70mVという低い電源に接続できます。V_{BIAS}レールを追加してLDOの内部回路に電力を供給することで、極めて低い入力電圧に対応します。V_{IN}とV_{BIAS}で消費される静止電流は非常に低く、それぞれ1.6µA、6µAです。I_Qが低く、超低ドロップアウトであることから、消費電力が重視される用途でソリューションの効率を高めることができます。例えば、V_{IN}を高効率のDC/DC降圧レギュレータの出力とし、V_{BIAS}ピンを充電式バッテリに接続できます。

また、オフ時に出力を高速放電するアクティブ・プルダウン回路を内蔵しており、既知の起動状態を確保できます。

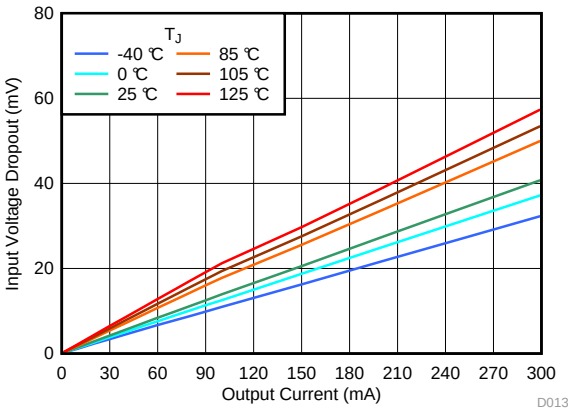
TPS7A10は超小型の5ピンDSBGA (YKA)パッケージで供給されるため、スペースの制約が厳しいアプリケーションに適しています。TPS7A10は6ピンWSON (DSE)パッケージでも供給されます。

製品情報(1)

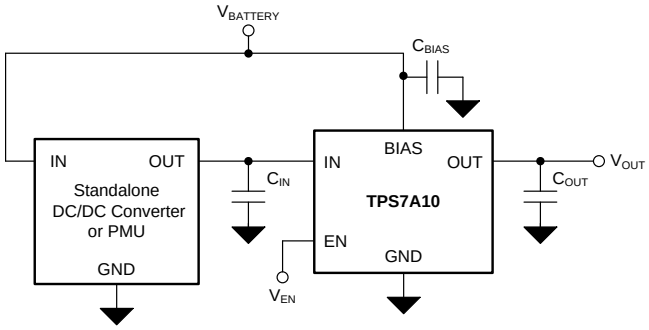
型番	パッケージ	本体サイズ（公称）
TPS7A10	WSON (6)	1.50mm×1.50mm
	DSBGA (5)	0.74mm×1.09mm (0.35mmピッチ)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

ドロップアウト 対 I_{OUT}および温度、YKAパッケージ



代表的なアプリケーション回路



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (June 2018) から Revision B に変更 **Page**

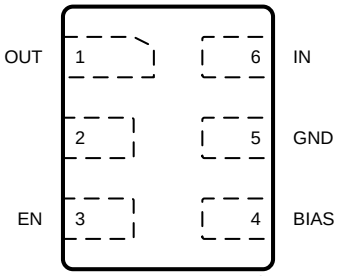
- 「*特長*」の「*非常に低いドロップアウトで最小限の電力損失*」箇条書き項目の副項目に、「*YKA*パッケージ」を 追加 ... 1
- 「*概要*」セクションの最後の文 追加 ... 1
- WSON (DSE)パッケージを事前情報から量産データ(アクティブ)に 変更 ... 1
- 「*ドロップアウト 対 I_{OUT}および温度、YKA*パッケージ」図のタイトルに「*YKA*パッケージ」を 追加 ... 1
- 追加 *YKA Package* to captions of *Output Accuracy Over Temperature, YKA Package* and *Output Accuracy Over Temperature, YKA Package* figures ... 7
- 追加 *Output Accuracy Over Temperature, DSE Package* and *Output Accuracy Over Temperature, DSE Package* figures 7
- 追加 *YKA Package* to caption of *Dropout vs I_{IOUT} and Temperature, YKA Package* figure ... 7
- 追加 *Dropout vs I_{IOUT} and Temperature, DSE Package* figure ... 8

2018年3月発行のものから更新 **Page**

- 事前情報から量産データ(アクティブ)に 変更 ... 1

5 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



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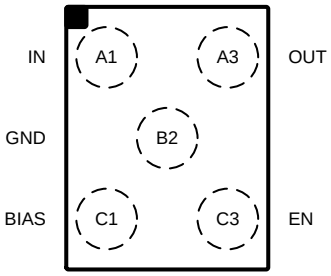
YKA Package
5-Pin DSBGA
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSE	YKA		
IN	6	A1	I	Input pin. For best transient response and to minimize input impedance, use the recommended or larger value ceramic capacitor from IN to ground. as listed in the *Recommended Operation Conditions*. Place the input capacitor as close as possible to input of the device.
OUT	1	A3	O	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use larger than the minimum recommended value ceramic capacitor. Follow the recommended capacitor value as listed in the *Recommended Operation Conditions*. Place the output capacitor as close as possible to output of the device.
GND	5	B2	—	Ground pin. This pin must be connected to ground.
BIAS	4	C1	I	BIAS pin. This pin enables the use of low-input voltage, low-output voltage conditions, (LILO). For best response, use the recommended or larger value ceramic capacitor from BIAS to ground as listed in the *Recommended Operation Conditions*. Place the bias capacitor as close as possible to input of the device.
EN	3	C3	I	Enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS; however, connecting EN to IN is only acceptable if the V_{IN} voltage is greater than 0.9 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	3.6	V
	Enable, V_{EN}	–0.3	6.0	
	Bias, V_{BIAS}	–0.3	6.0	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Current	Maximum output current		Internally limited	A
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is 3.6 or (V_{IN} + 0.3) , whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.75		3.3	V
V_{BIAS}	Bias voltage	1.7		5.5	V
V_{OUT}	Output voltage	0.5		3.0	V
I_{OUT}	Peak output current	0		300	mA
C_{IN}	Input capacitor	2.2			µF
C_{BIAS}	Bias capacitor		0.1		µF
C_{OUT} (1)	Output capacitor	2.2		22	µF
T_J	Operating junction temperature	–40		125	℃

(1) Maximum ESR must be lower than 250 mΩ

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A10		UNIT
		DSE (WSON)	YKA (WSCP)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.8	169.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.9	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.0	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.4	55.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* .

6.5 Electrical Characteristics

over T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Nominal Accuracy	T_J = 25°C	–0.5		0.5	%
	Accuracy over temperature	–20°C ≤ T_J ≤ 85, DSE package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.25		1.25	
		–40°C ≤ T_J ≤ 85, YKA package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.25		1.25	
		–40°C ≤ T_J ≤ 125, DSE and YKA package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.5		1.5	
ΔV_{OUT} / ΔV_{IN}	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V		0.001		%/V
ΔV_{OUT} / ΔV_{BIAS}	V_{BIAS} line regulation	$V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V		0.03		%/V
ΔV_{OUT} / ΔI_{OUT}	Load regulation	0.1 mA ≤ I_{OUT} ≤ 300 mA		0.2		%/A
$I_{Q(BIAS)}$	Bias pin current	T_J = 25°C, I_{OUT} = 0 mA	3	6	8	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			11	
		I_{OUT} = 0 mA			14	
		I_{OUT} = 300 mA			60	
$I_{Q(IN)}$	Input pin current(1)	T_J = 25°C, I_{OUT} = 0 mA		1.6	2.1	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			2.3	
		I_{OUT} = 0 mA			2.6	
		I_{OUT} = 300 mA			9	
$I_{SHDN(BIAS)}$	V_{BIAS} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			400	nA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1200	
$I_{SHDN(IN)}$	V_{IN} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1	µA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			3	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$, YKA package	325	450	600	mA
		V_{OUT} = 0.9 × $V_{OUT(NOM)}$, DSE package	350	450	625	mA
I_{SC}	Short circuit current limit	V_{OUT} = 0 V		150		mA
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 300 mA, YKA package		40	70	mV
		V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 300 mA, DSE package		55	90	
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	I_{OUT} = 300 mA		0.85	1.05	V
		I_{OUT} = 150 mA		0.75	0.95	

(1) This current flowing from V_{IN} to GND.
(2) Dropout is not measured for V_{OUT} < 1.0 V

Electrical Characteristics (continued)

over T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} PSRR	V_{IN} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		60		dB
		f = 100 kHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		36		
		f = 1 MHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		32		
		f = 1.5 MHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		35		
V_{BIAS} PSRR	V_{BIAS} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		60		dB
		f = 100 kHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		40		
		f = 1 MHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		35		
V_n	Output voltage noise	Bandwidth = 10 Hz to 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		93.9		μV_{RMS}
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} rising	1.46	1.54	1.63	V
		V_{BIAS} falling	1.35	1.44	1.55	
$V_{UVLO\_HYST(BIAS)}$	Bias supply hysteresis	V_{BIAS} hysteresis		80		mV
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising	645	675	710	mV
		V_{IN} falling	565	600	640	mV
$V_{UVLO\_HYST(IN)}$	Input supply hysteresis	V_{IN} hysteresis		75		mV
t_{STR}	Start-up time(3)			525	1200	µs
$V_{HI(EN)}$	EN pin logic high voltage		0.9			V
$V_{LO(EN)}$	EN pin logic low voltage				0.4	V
I_{EN}	EN pin current	EN = 5.5 V		10		nA
$R_{PULLDOWN}$	Pulldown resistor	V_{BIAS} = 3.3 V, P version only		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature rising		160		°C
		Reset, temperature falling		145		

(3) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.

6.6 Typical Characteristics

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

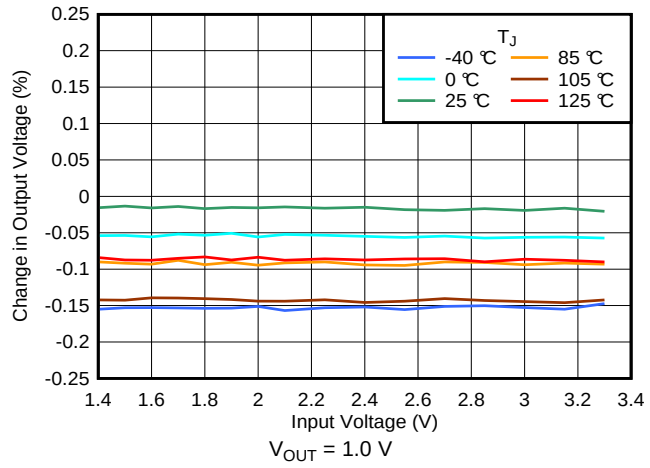


図 1. Output Accuracy Over Temperature, YKA Package

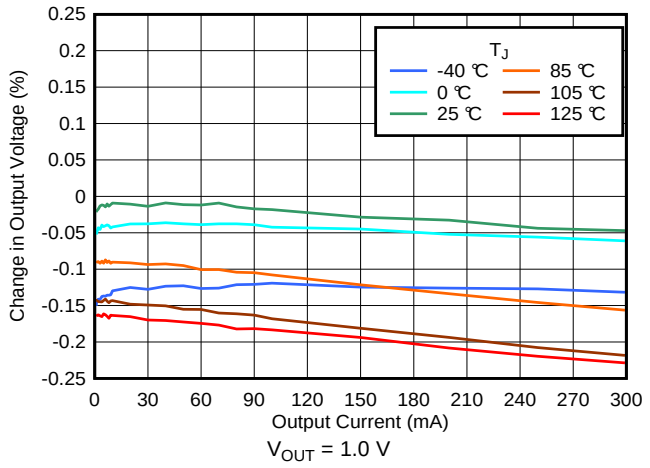


図 2. Output Accuracy Over Temperature, YKA Package

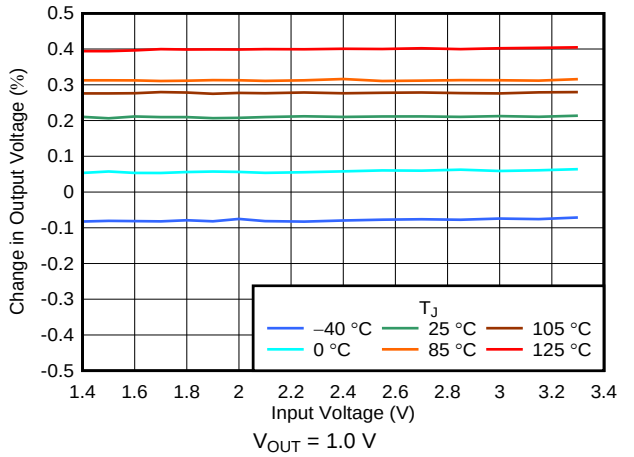


図 3. Output Accuracy Over Temperature, DSE Package

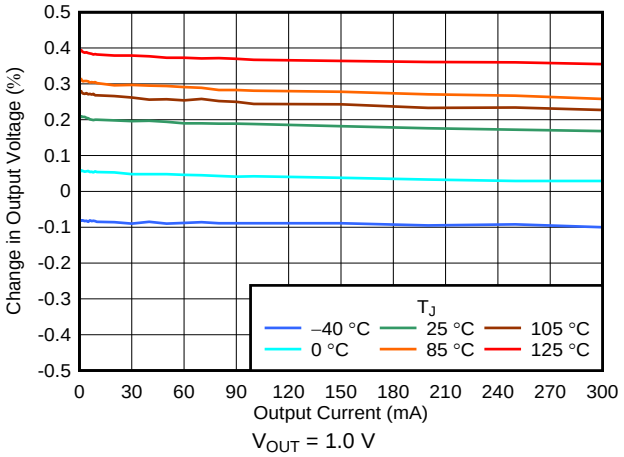


図 4. Output Accuracy Over Temperature, DSE Package

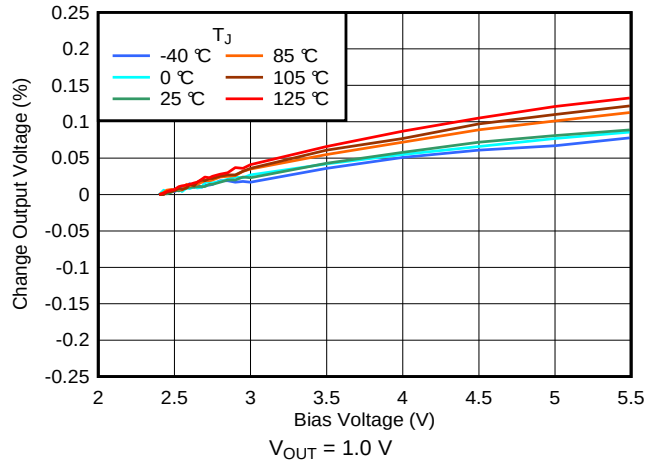


図 5. Output Accuracy Over Temperature and V_{BIAS}

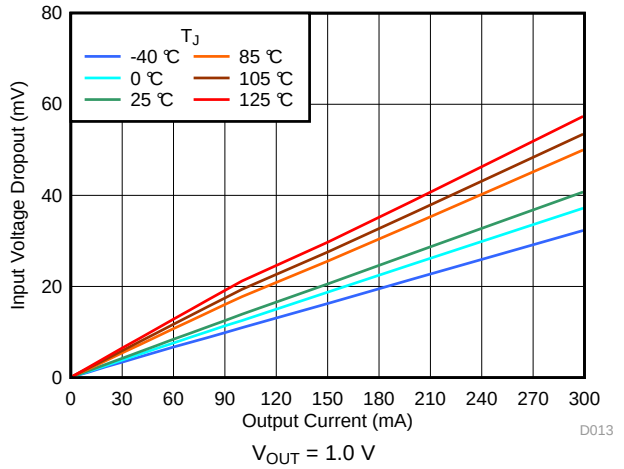


図 6. Dropout vs I_{IOUT} and Temperature, YKA Package

Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

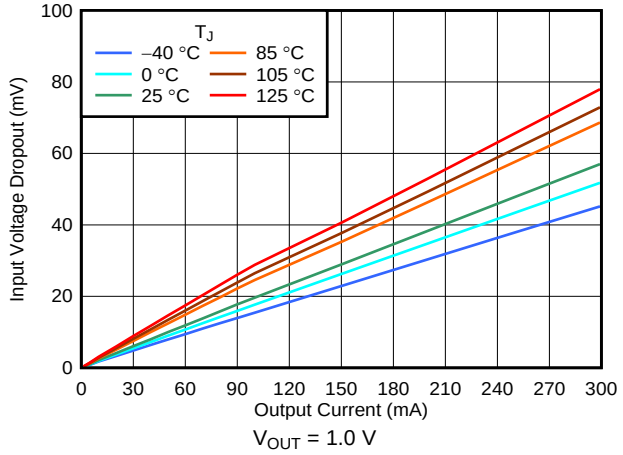


図 7. Dropout vs I_{IOUT} and Temperature, DSE Package

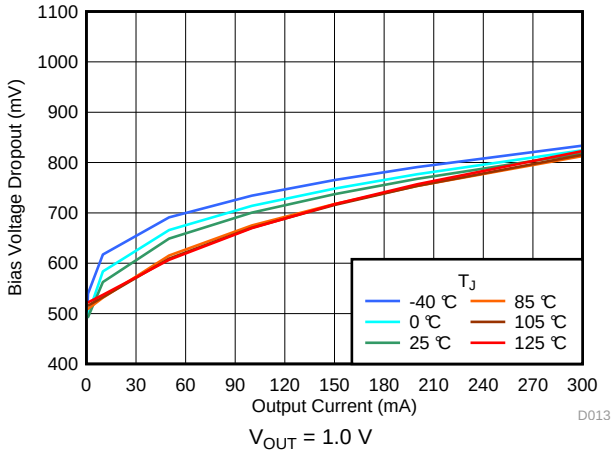


図 8. Dropout vs V_{BIAS} and Temperature

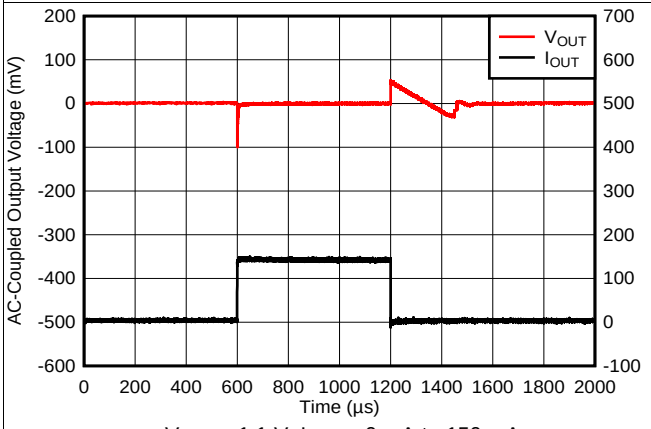


図 9. I_{OUT} Transient

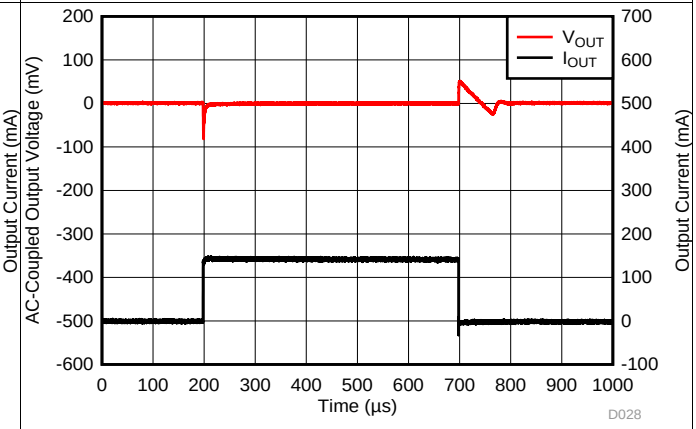


図 10. I_{OUT} Transient

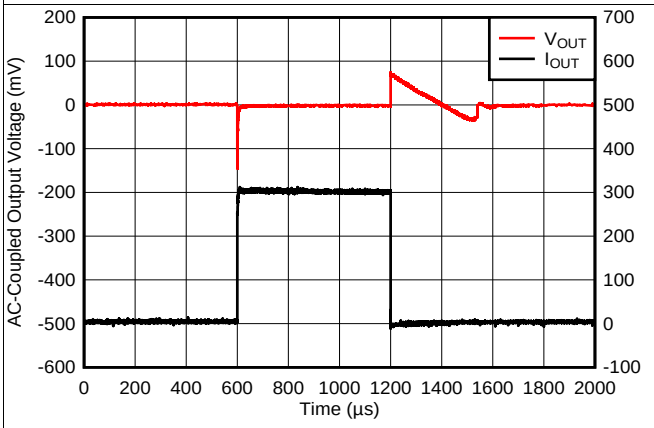


図 11. I_{OUT} Transient

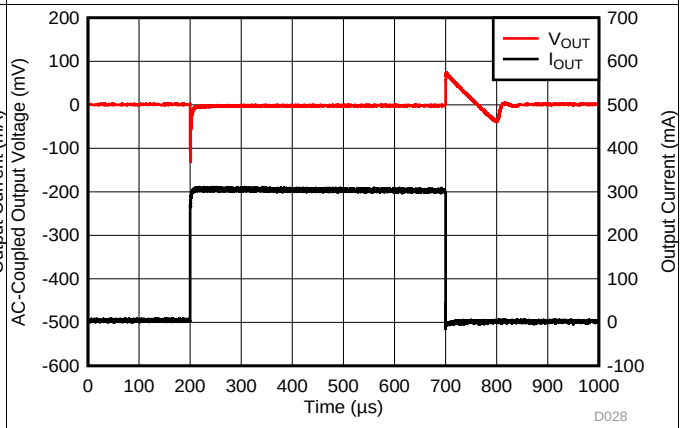
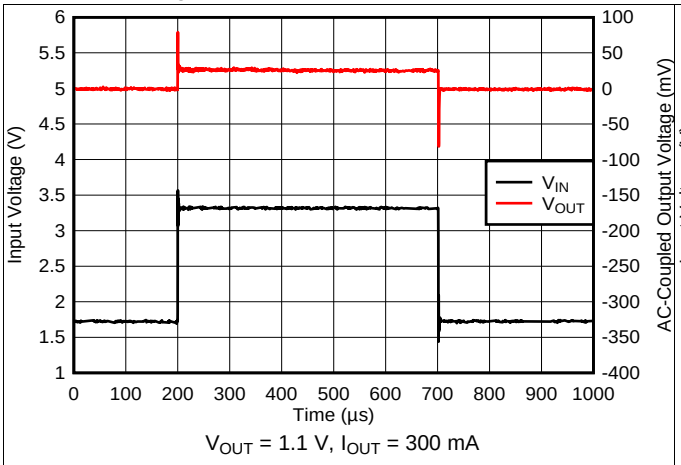


図 12. I_{OUT} Transient

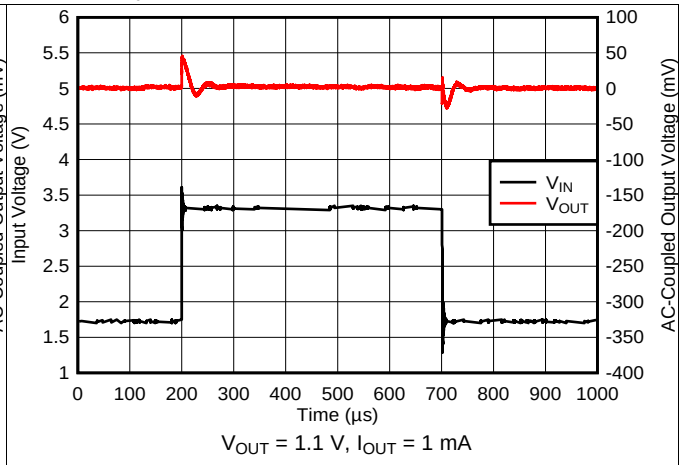
Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



V_{OUT} = 1.1 V, I_{OUT} = 300 mA

図 13. V_{IN} Transient



V_{OUT} = 1.1 V, I_{OUT} = 1 mA

図 14. V_{IN} Transient

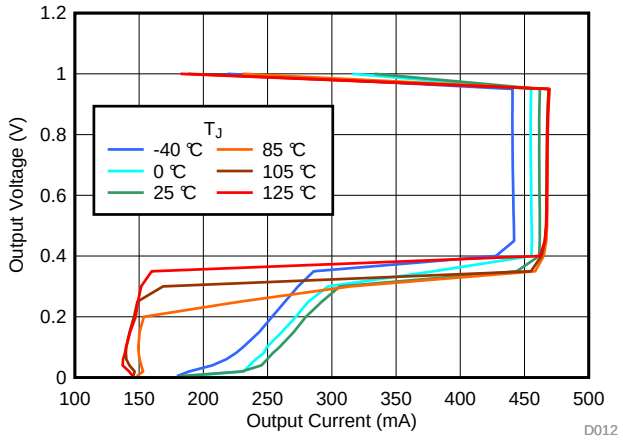
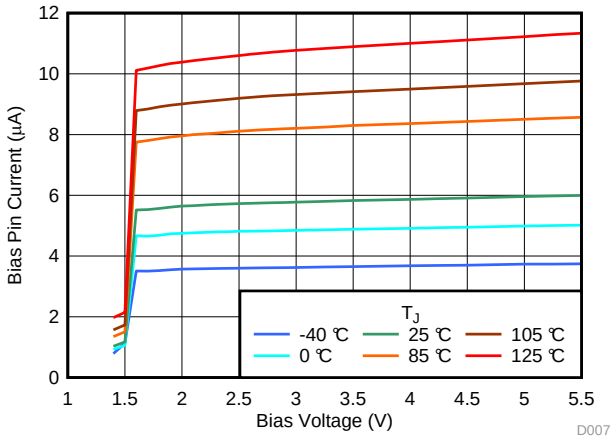
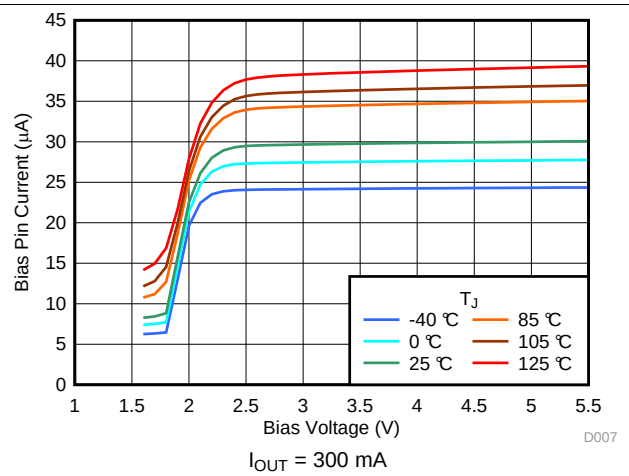


図 15. Foldback Current Limit Over Temperature



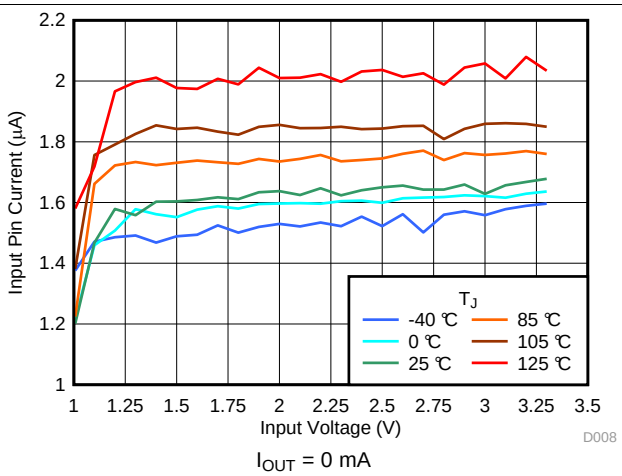
I_{OUT} = 0 mA

図 16. I_Q (V_{BIAS}) Over Temperature



I_{OUT} = 300 mA

図 17. I_Q (V_{BIAS}) Over Temperature

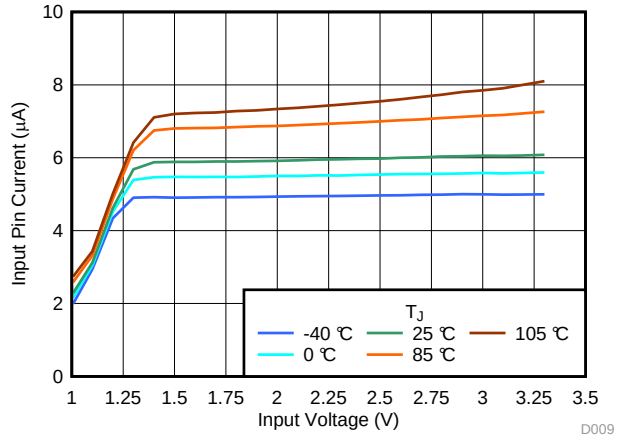


I_{OUT} = 0 mA

図 18. I_Q (V_{IN}) Over Temperature

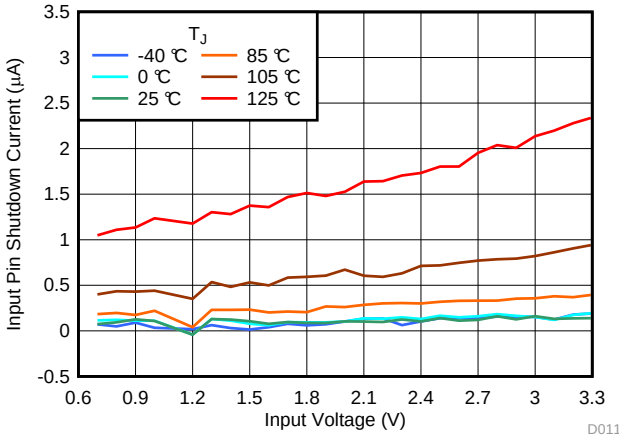
Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



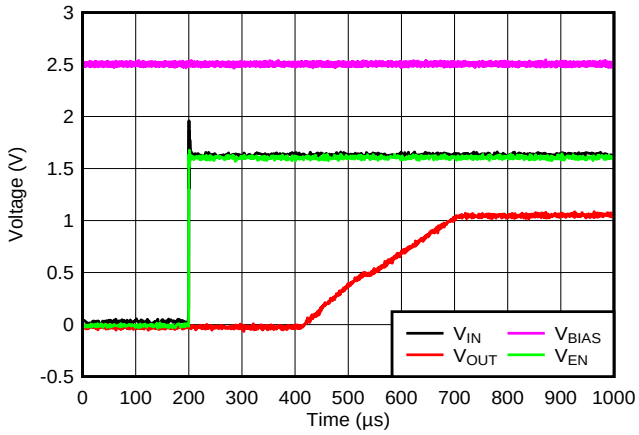
I_{OUT} = 300 mA

図 19. I_Q (V_{IN}) Over Temperature



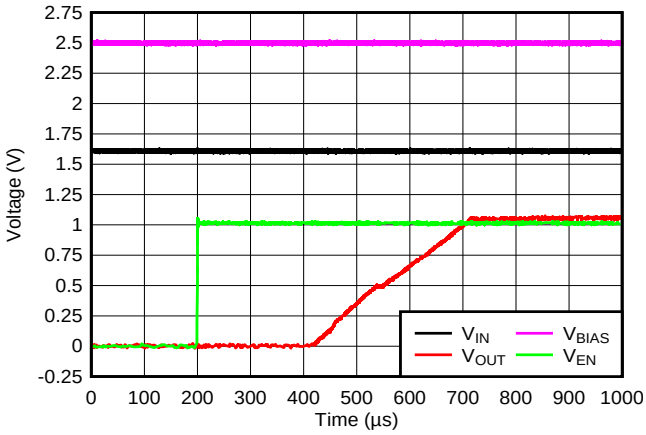
V_{OUT} = 1.0 V, V_{EN} < 0.4 V

図 20. I_{SHDN} (V_{IN}) Over Temperature



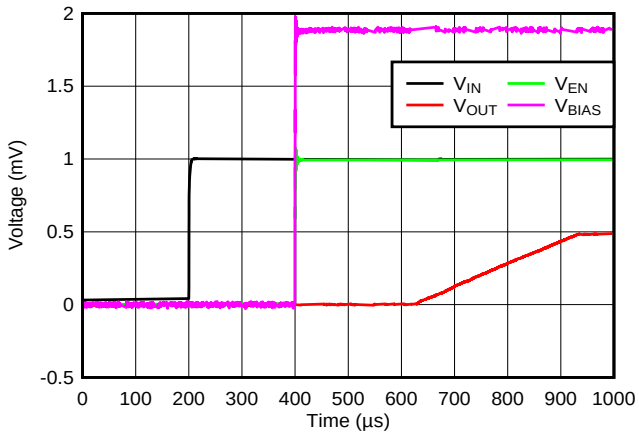
V_{OUT} = 1.1 V

図 21. Startup With V_{EN} = V_{IN}



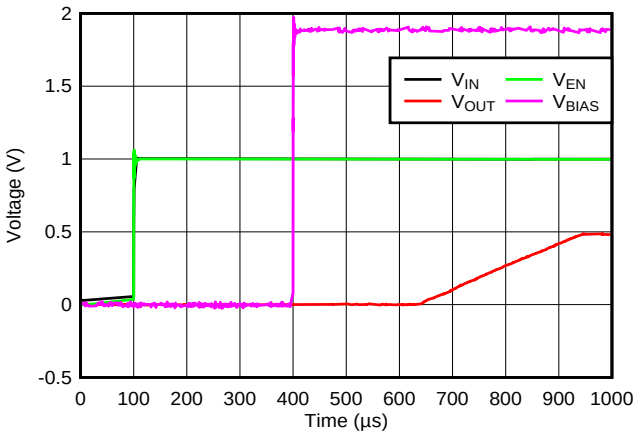
V_{OUT} = 1.1 V

図 22. Startup With Separated V_{EN}



V_{OUT} = 0.5 V

図 23. Startup With V_{EN} and V_{BIAS} Powering Up Simultaneously

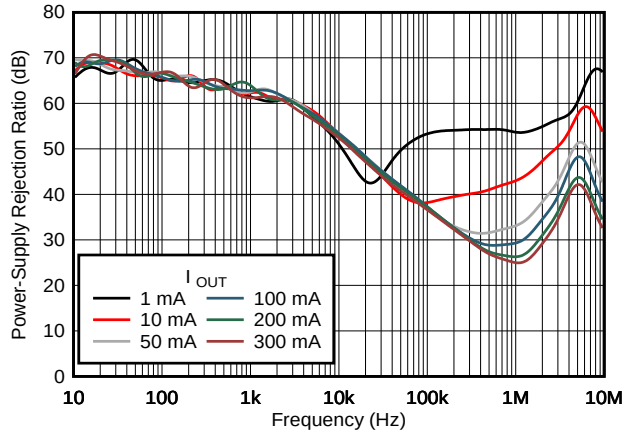


V_{OUT} = 0.5 V

図 24. Startup With V_{BIAS} Powering Up After V_{IN} and V_{EN}

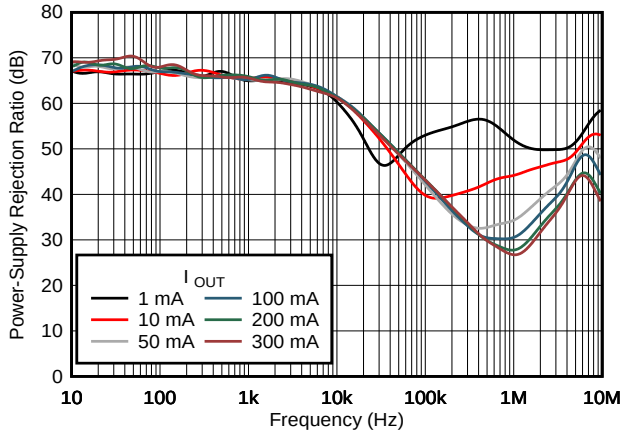
Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



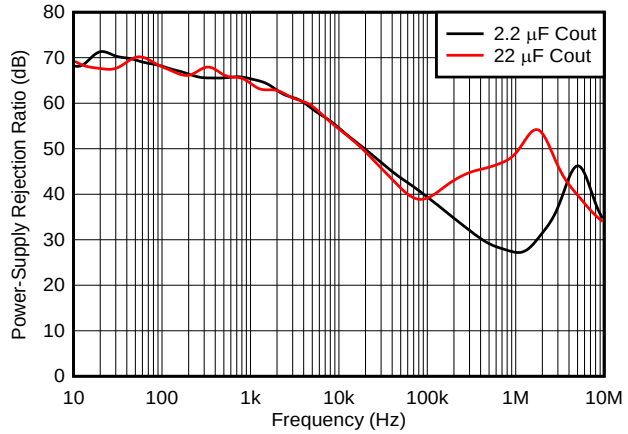
C_{IN} = 0 µF, V_{OUT} = 1.1 V, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

図 25. PSRR vs Frequency and I_{OUT}



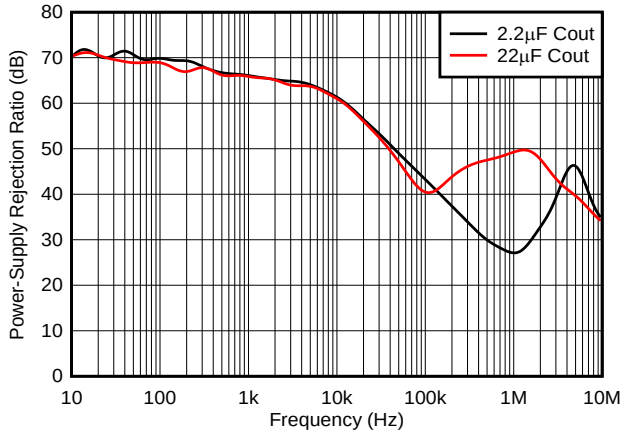
C_{IN} = 0 µF, V_{OUT} = 0.5 V, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

図 26. PSRR vs Frequency and I_{OUT}



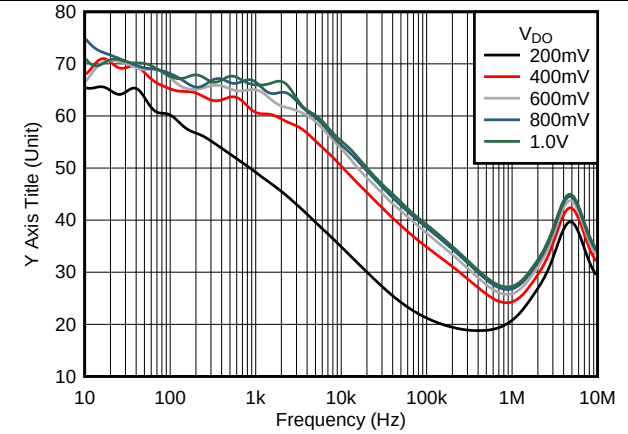
C_{IN} = 0 µF, V_{OUT} = 1.1 V, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

図 27. PSRR vs Frequency and C_{OUT}



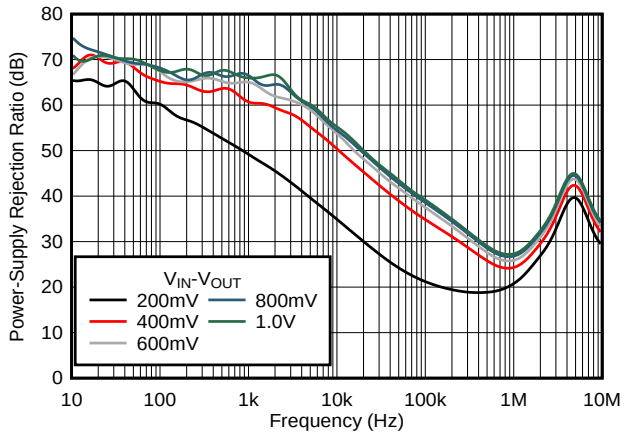
C_{IN} = 0 µF, V_{OUT} = 0.5 V, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

図 28. PSRR vs Frequency and C_{OUT}



C_{IN} = 0 µF, V_{OUT} = 1.1 V, I_{OUT} = 300 mA, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

図 29. PSRR vs Frequency and V_{DO}

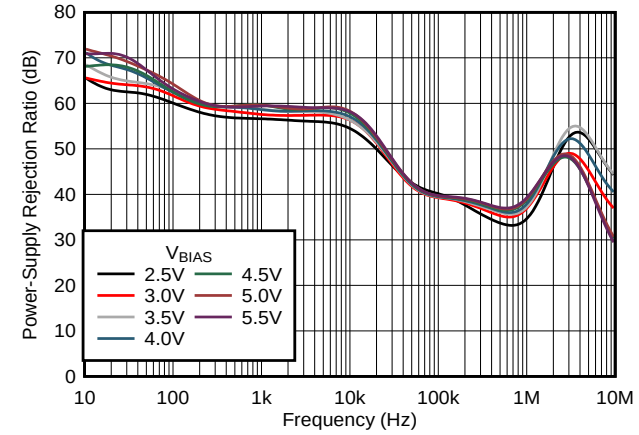


C_{IN} = 0 µF, V_{OUT} = 0.5 V, I_{OUT} = 300 mA, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

図 30. PSRR vs Frequency and V_{DO}

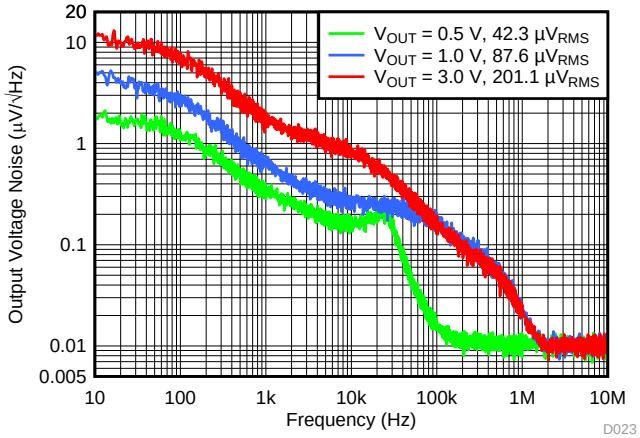
Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



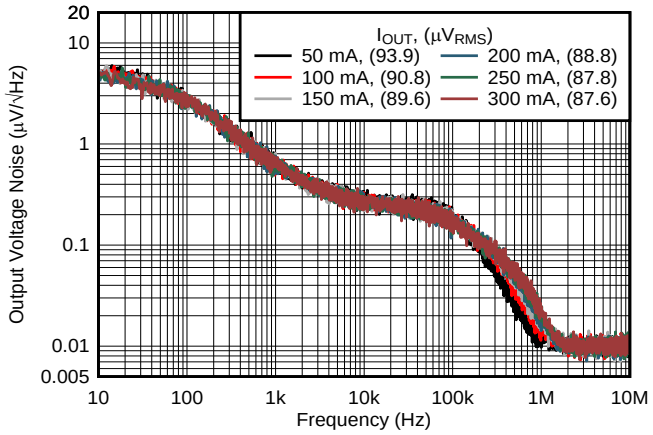
V_{OUT} = 1.1 V, I_{OUT} = 300 mA, C_{BIAS} = 0 µF

図 31. V_{BIAS} PSRR vs Frequency and V_{BIAS}



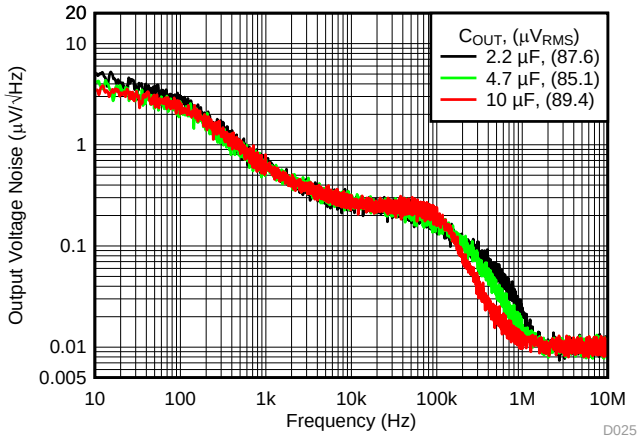
I_{OUT} = 300 mA

図 32. Output Noise vs Frequency and V_{OUT}



V_{OUT} = 1.0 V, V_{BIAS} = 2.5 V

図 33. Output Noise vs Frequency and I_{OUT}



V_{OUT} = 1.0 V, I_{OUT} = 300 mA

図 34. Output Noise vs Frequency and C_{OUT}

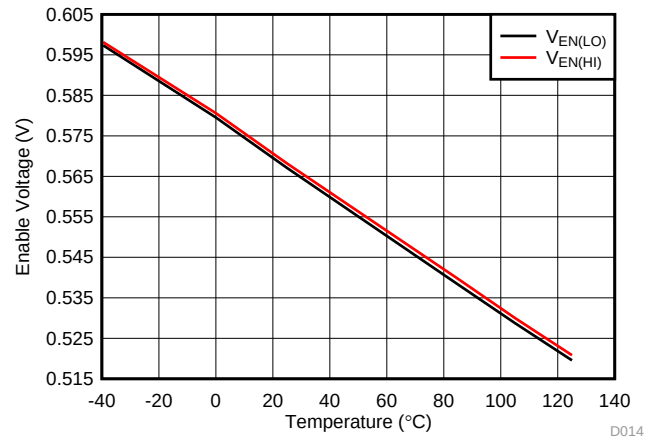


図 35. Enable High and Low Thresholds vs Temperature

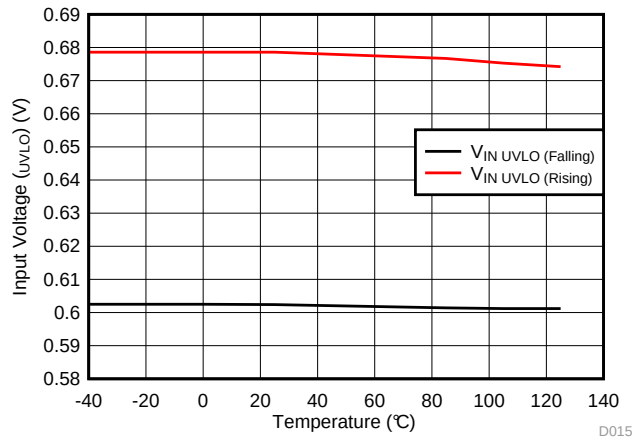


図 36. $V_{UVLO(IN)}$ Rising and Falling Thresholds vs Temperature

Typical Characteristics (continued)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

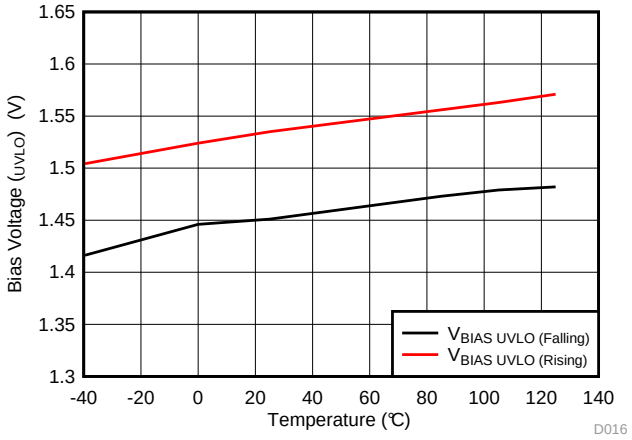


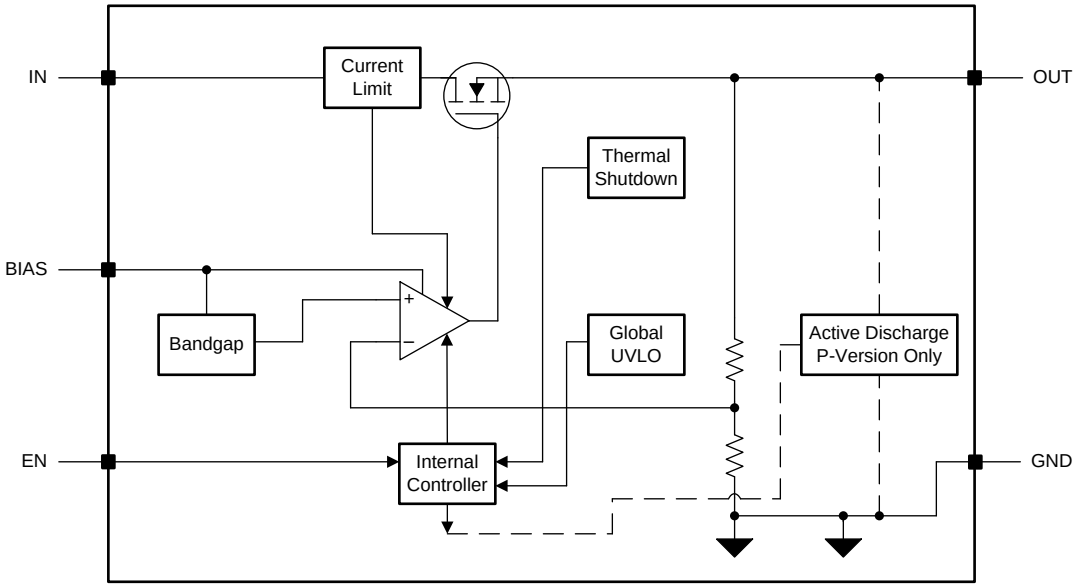
図 37. $V_{UVLO(BIAS)}$ Rising and Falling Thresholds vs Temperature

7 Detailed Description

7.1 Overview

The TPS7A10 is a low input, ultra-low dropout, and low quiescent current linear regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications. The implementation of the BIAS pin on the TPS7A10 vastly improves efficiency of low-voltage output applications by allowing the use of a preregulated, low-voltage input supply that offers sub-band-gap output voltages. The high power-supply rejection ratio (PSRR), low noise, low ground pin current, and ultra-small packaging make this device suitable for ultra-portable applications. This device also offers high output voltage accuracy of 1.5% over the recommended junction temperature range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excellent Transient Response

The TPS7A10 responds quickly to a transient on the input supply (line transient) or the output current (load transient) that results from the device high input impedance and low output impedance across frequency. This same capability also means that the device has a high power-supply rejection ratio (PSRR) and low internal noise floor (e_n). The low-dropout regulator (LDO) approximates an ideal power supply in ac (small-signal) and dc (large-signal) conditions.

The choice of external component values optimizes the small- and large-signal response; see the *Input and Output Capacitor Requirements* section for proper selection.

7.3.2 Global Undervoltage Lockout (UVLO)

The TPS7A10 uses two undervoltage lockout (UVLO) circuits: one on the BIAS pin and one on the IN pin to prevent the device from turning on before both V_{BIAS} and V_{IN} rise above their lockout voltages. The two UVLO signals are connected internally through an AND gate, as shown in 図 38. This internal connection allows the device to be turned off when either rail is below its lockout voltage.

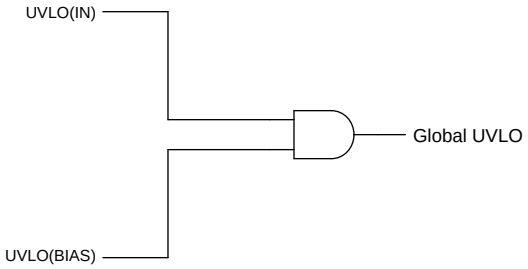


図 38. Global UVLO circuit

7.3.3 Active Discharge

The active discharge option (P version only) have internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled in order to actively discharge the output voltage. The active discharge circuit is activated by driving the enable pin to logic low to disable the device, or when the device is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. 式 1 calculates the discharge time constant:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.4 Enable

The enable pin for this device is active high. The output of the device is turned on when the enable pin voltage is greater than the EN pin logic high voltage, and the output of the device is turned off when the enable pin voltage is less than the EN pin voltage logic low .

The EN pin can be tied to the IN pin, the BIAS pin, or can be driven separately to enable and disable the device; however, connecting the EN pin to the IN pin is only acceptable if the V_{IN} voltage is greater than 0.9 V.

Feature Description (continued)

7.3.5 Sequencing Requirement

The V_{IN}, V_{BIAS}, and V_{EN} voltages can be sequenced in any order without causing damage to the device. The start up is always monotonic regardless of the sequencing order or the ramp rates of IN, BIAS, and EN pins. For optimum device performance, have V_{BIAS} present before enabling the device in any sequence order between V_{IN} and V_{EN} because the device internal circuitry is powered off the V_{BIAS}, refer to *Recommended Operating Conditions* for proper voltage ranges of V_{IN}, V_{BIAS}, and V_{EN}.

7.3.6 Internal Foldback Current Limit

The internal foldback current limit circuit is used to protect the LDO against high-load current faults or shorting events. The foldback mechanism lowers the current limit as the output voltage decreases, and limits power dissipation during short-circuit events while still allowing for the device to operate at the rated output current; see 図 15.

For example, when V_{OUT} is 90% of $V_{OUT(nom)}$, the current limit is I_{CL} (typical); however, if V_{OUT} is forced to 0 V, the current limit is I_{SC} (typical).

In many LDOs, the foldback current limit can prevent start up into a constant-current load or a negatively-biased output. A *brick-wall* current limit is when there is an abrupt current stop after the current limit is reached. The foldback mechanism for this device goes into a *brick-wall* current limit when V_{OUT} > 500 mV (typical), thus limiting current to I_{CL} (typical). When V_{OUT} is approximately 0 V, current is limited to I_{SC} (typical) in order to provide normal start up into a variety of loads.

Thermal shutdown can activate during a current-limit event because of the high power dissipation typically found in these conditions. To provide proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

7.3.7 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the thermal junction temperature (T_J) of the main pass-FET rises to the thermal shutdown temperature (T_{SD}) for shutdown listed in the *Electrical Characteristics*. Thermal shutdown hysteresis makes sure that the LDO resets again (turns on) when the temperature falls to the T_{SD} for reset.

The thermal time constant of the semiconductor die is fairly short, and thus the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

A fast start up when T_J > the T_{SD} for reset causes the device thermal shutdown to assert at T_{SD} for reset, and prevents the device from turning on until the junction temperature is reduced below T_{SD} for reset.

7.4 Device Functional Modes

The device has the following modes of operation:

- Normal operation: The device regulates to the nominal output voltage.
- Dropout operation: The pass element operates as a resistor and the output voltage is set as $V_{IN} – V_{DO}$.
- Disabled: The output of the device is disabled and the discharge circuit is activated.

表 1 shows the conditions that lead to the different modes of operation.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{BIAS} > V_{OUT} + 1.05$ V	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{BIAS} < V_{OUT} + 1.05$ V	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J > T_{SD}$ for shutdown

7.4.1 Normal Mode

The device regulates the output to the nominal output voltage when all normal mode conditions in 表 1 are met.

7.4.2 Dropout Mode

The device is not in regulation, and the output voltage tracks the input voltage minus the voltage drop across the pass element of the device. In this mode, PSRR and the noise performance of the device are significantly degraded.

7.4.3 Disable Mode

In this mode, the pass element is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and the best implementation to achieve a reliable design.

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and BIAS pins. Multilayer ceramic capacitors are the industry standard for these types of applications, but must be used with good judgment. Ceramic capacitors that use X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. Avoid Y5V-rated capacitors because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, assume that effective capacitance decreases by as much as 50%. The input, output, and bias capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

A minimum 2.2-µF ceramic capacitor at the input is required for stability, A minimum 2.2-µF ceramic capacitor with a maximum ESR value of less than 250 mΩ at the output is also required for stability. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. A higher-value input capacitor may be necessary if large, fast rise-time load or line transients are anticipated, or if the device is located several inches from the input power source. Dynamic performance of the device is improved with the use of an output capacitor larger than the minimum value specified in the *Recommended Operating Conditions* table.

Although a bias capacitor is not required, connect a 0.1-µF ceramic capacitor from BIAS to GND for best analog design practice. This capacitor counteracts reactive bias sources if the source impedance is not sufficiently low.

Place the input, output, and bias capacitors as close as possible to the device to minimize traces parasitics.

Application Information (continued)

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current while output voltage regulation is maintained. See 図 9, 図 10, 図 11, and 図 12 for typical load transient response. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions in 図 39 are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state operation.

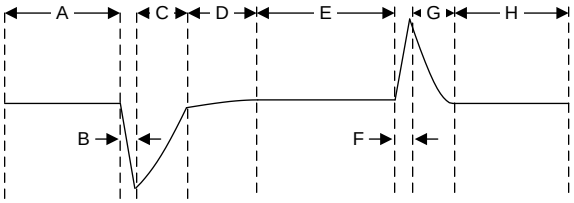


図 39. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient, but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered, and a higher current discharge path is provided for the output capacitor.

8.1.4 Dropout Voltage

Generally, dropout voltage refers to the minimum voltage difference between the input and output voltage (V_{DO} = V_{IN} – V_{OUT}) that is required for regulation. When V_{IN} – V_{OUT} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch.

Dropout voltage is affected by the drive strength of the pass-element gate. This drive strength is nonlinear with respect to V_{IN} on this device.

8.1.5 Behavior During Transition From Dropout Into Regulation

Some applications may have transients that place this device into dropout, especially when this device can be powered from a battery with relatively high ESR. The load transient saturates the output stage of the error amplifier when the pass element is driven fully on, making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is limited because the error amplifier must first recover from saturation and then place the pass element back into active mode. During this time, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}.

When V_{IN} ramps up slowly for start-up, the slow ramp-up voltage may place the device in dropout. As with many other LDOs, the output can overshoot on recovery from this condition. However, this condition is easily avoided through the use of the enable signal.

If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot. These solutions provide a path to dissipate the excess charge.

Application Information (continued)

8.1.6 Undervoltage Lockout Circuit Operation

The V_{IN} UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range. The V_{IN} UVLO circuit also makes sure that the device shuts down when the input supply collapses. Similarly, the V_{BIAS} UVLO circuit makes sure that the device stays disabled before the bias supply reaches the minimum operational voltage range. The V_{BIAS} UVLO circuit also makes sure that the device shuts down when the bias supply collapses.

図 40 depicts the UVLO circuit response to various input or bias voltage events. This figure can be separated into the following parts:

- Region A: The device does not start until the input or bias voltage reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation, but the device is still enabled.
- Region D: Normal operation, regulating device
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases, and the output falls as a result of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached, and a normal start-up follows.
- Region F: Normal operation followed by the input or bias falling to the UVLO falling threshold
- Region G: The device is disabled as the input or bias voltages fall below the UVLO falling threshold to 0 V. The output falls as a result of the load and active discharge circuit.

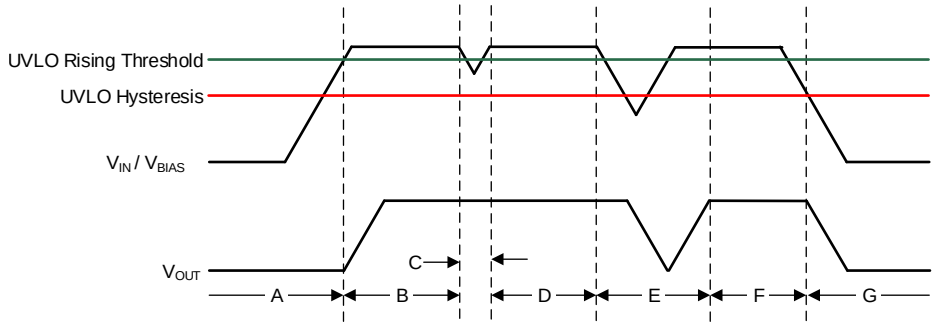


図 40. Typical V_{IN} or V_{BIAS} UVLO Circuit Operation

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

式 2 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = [(T_J - T_A) / R_{\theta JA}] \quad (2)$$

式 3 represents the actual power being dissipated in the device:

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (3)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A10 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Application Information (continued)

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 4, maximum power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). The equation is rearranged in 式 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (5)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance.

8.1.7.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 6 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 式 3
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(6)

8.1.7.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is shown in 図 41, and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - 式 5 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO, thus when $V_{IN} - V_{OUT}$ increases, the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

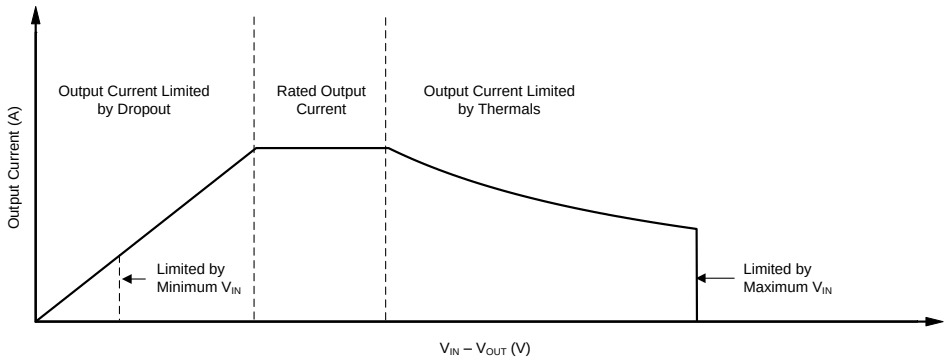


図 41. Region Description of Continuous Operation Regime

8.2 Typical Application

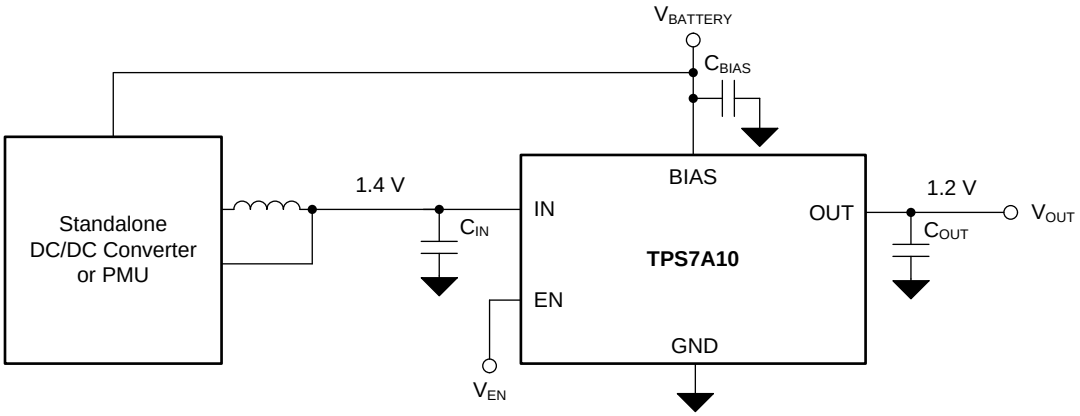


図 42. Supplying a Clean DC Voltage

8.2.1 Design Requirements

表 2 summarizes the design requirements for 図 42.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.4 V
V_{BIAS}	2.7 V
V_{OUT}	1.2 V
I_{OUT}	10-mA typical, 300-mA peak
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

For this design example, the 1.2-V, fixed-version TPS7A1012 device is selected. Use a 4.7-µF input capacitor to minimize transient currents drawn from the DC/DC convertor. Use a 4.7-µF output capacitor for optimized load transient response. The dropout voltage (V_{DO}) is kept within the TPS7A10 dropout voltage specification for the 1.2-V output voltage option inorder to keep the device in regulation under all load and temperature conditions for this design. The high-PSRR and low-noise measurements for this design example are given in the *Thermal Dissipation* section.

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 式 7 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (7)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 式 8 to calculate the power dissipation. As 式 9 shows, multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (8)$$

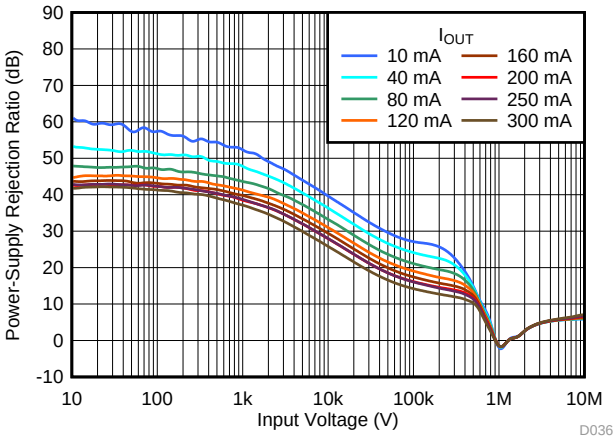
$$T_J = R_{\theta JA} \times P_D + T_A \quad (9)$$

If the ($T_{J(MAX)}$) value does not exceed 125°C, use 式 10 to calculate the maximum ambient temperature. 式 11 calculates the maximum ambient temperature with a value of 99.59°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (10)$$

$$T_{A(MAX)} = 125°C - 169.4 \times (1.4\ V - 1.2\ V) \times (0.3\ A) = 114.84°C \quad (11)$$

8.2.3 Application Curve



V_{IN} = 1.4 V, V_{OUT} = 1.2 V, V_{BIAS} = 2.7 V,
C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF, C_{BIAS} = 0.1 µF

図 43. PSRR vs Frequency and I_{OUT}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 0.75 V to 3.3 V, and a bias supply voltage range of 1.7 V to 5.5 V. The input and bias supplies must be well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V and $V_{BIAS} = V_{OUT(nom)}$ + 1.05 V.

10 Layout

10.1 Layout Guidelines

For correct printed circuit board (PCB) layout, follow these guidelines:

- Place input, output, and bias capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.

10.2 Layout Examples

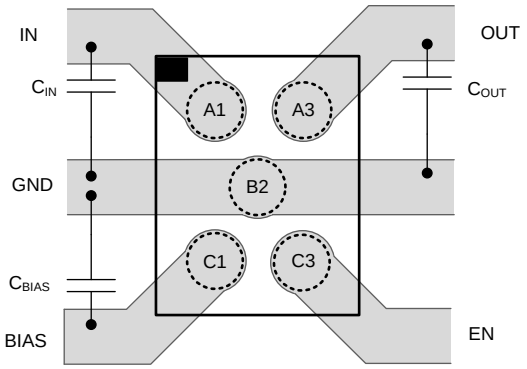


図 44. Recommended Layout for the YKA Package

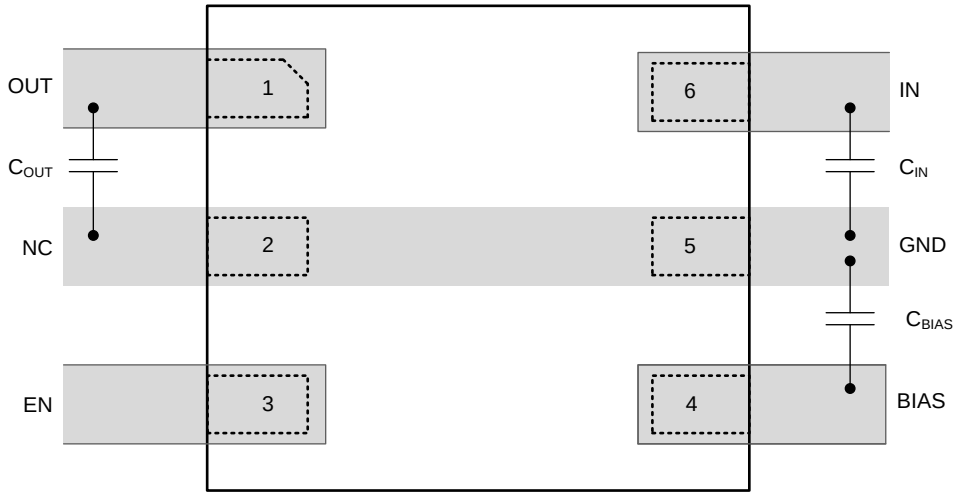


図 45. Recommended Layout for the DSE Package

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS7A10を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。*TPS7A10EVM*は、テキサス・インスツルメンツのWebサイトの製品フォルダから請求するか、TI eStoreから直接お求めになれます。

11.1.1.2 Spiceモデル

このデバイスのSpiceモデルは、TPS7A10製品フォルダの*ツールとソフトウェア*タブから入手できます。

11.1.2 デバイスの項目表記

表 3. デバイスの項目表記(1)(2)

製品名	V_{OUT}
TPS7A10**xx(x)yyyz**	**xx(x)**は公称出力電圧です。出力電圧の分解能が50mVの場合、注文番号に2桁が使用されます。それ以外の場合は3桁が使用されます(例: 28＝2.8V、125＝1.25V)。 **yyy**はパッケージ指定子です。 **z**はパッケージ数量です。Rはリール、Tはテープを表します。

(1) 最新のパッケージと発注情報については、このデータシートの末尾にある「パッケージ・オプション」の付録を参照するか、www.ti.comにあるデバイスの製品フォルダをご覧ください。
(2) 出力電圧は、0.5Vから3.0Vまで、50mV刻みで利用できます。詳細と在庫については、工場にお問い合わせください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『TPS7A10EVM-004評価モジュール』ユーザー・ガイド*
- テキサス・インスツルメンツ、*『新しい熱評価基準の解説』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『AN-1112　DSBGAウェハー・レベルのチップ・スケール・パッケージ』アプリケーション・レポート*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A1006PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF
TPS7A1006PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF
TPS7A1006PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF
TPS7A1006PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF
TPS7A1006PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
TPS7A1006PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
TPS7A1008PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2
TPS7A1008PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2
TPS7A1008PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2
TPS7A1008PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2
TPS7A1008PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
TPS7A1008PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
TPS7A10105PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ
TPS7A10105PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ
TPS7A10105PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ
TPS7A10105PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ
TPS7A10105PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
TPS7A10105PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
TPS7A1010PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1
TPS7A1010PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1
TPS7A1010PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1
TPS7A1010PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1
TPS7A1010PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
TPS7A1010PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
TPS7A1011PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX
TPS7A1011PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX
TPS7A1011PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX
TPS7A1011PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX
TPS7A1011PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A1011PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D
TPS7A1012PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW
TPS7A1012PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW
TPS7A1012PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW
TPS7A1012PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW
TPS7A1012PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E
TPS7A1012PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E
TPS7A1015PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV
TPS7A1015PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV
TPS7A1015PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV
TPS7A1015PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV
TPS7A1015PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F
TPS7A1015PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F
TPS7A1018PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU
TPS7A1018PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU
TPS7A1018PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU
TPS7A1018PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU
TPS7A1018PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G
TPS7A1018PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G
TPS7A1025PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT
TPS7A1025PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT
TPS7A1025PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT
TPS7A1025PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT
TPS7A1025PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H
TPS7A1025PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H
TPS7A1028PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS
TPS7A1028PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS
TPS7A1028PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS
TPS7A1028PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS
TPS7A1028PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	I
TPS7A1028PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A1030PDSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR
TPS7A1030PDSER.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR
TPS7A1030PDSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR
TPS7A1030PDSET.B	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR
TPS7A1030PYKAR	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J
TPS7A1030PYKAR.A	Active	Production	DSBGA (YKA) | 5	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

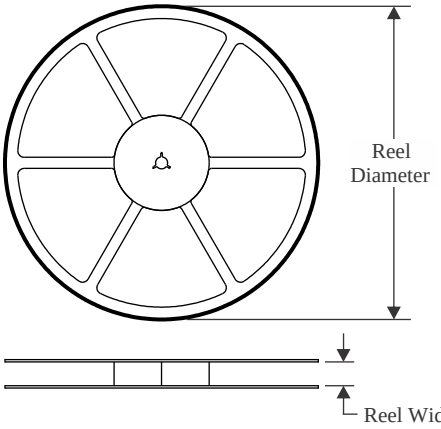
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

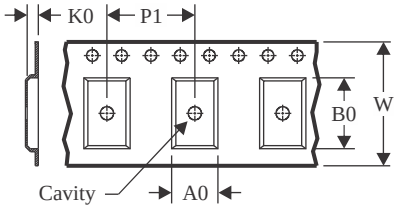
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

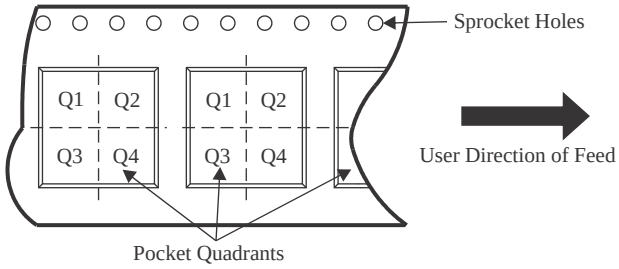


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

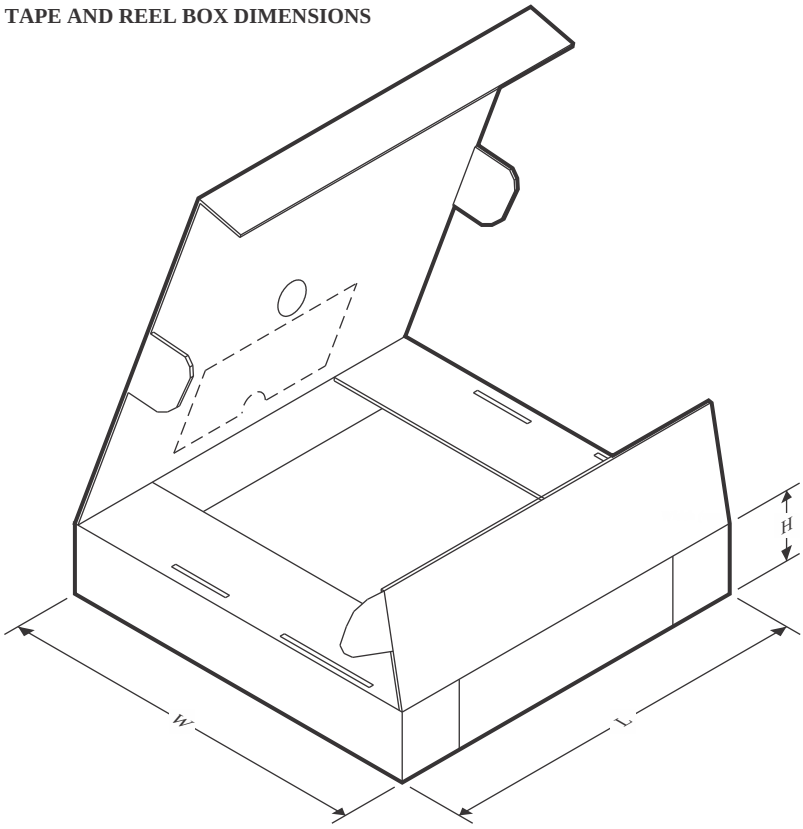


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1006PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1006PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1006PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1008PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1008PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1008PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A10105PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A10105PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A10105PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1010PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1010PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1010PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1011PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1011PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1011PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1012PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1012PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1012PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1015PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1015PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1015PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1018PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1018PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1018PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1025PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1025PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1025PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1028PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1028PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1028PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1030PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1030PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1030PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1006PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1006PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1006PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1008PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1008PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1008PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A10105PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A10105PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A10105PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1010PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1010PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1010PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1011PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1011PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1011PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1012PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1012PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1012PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0

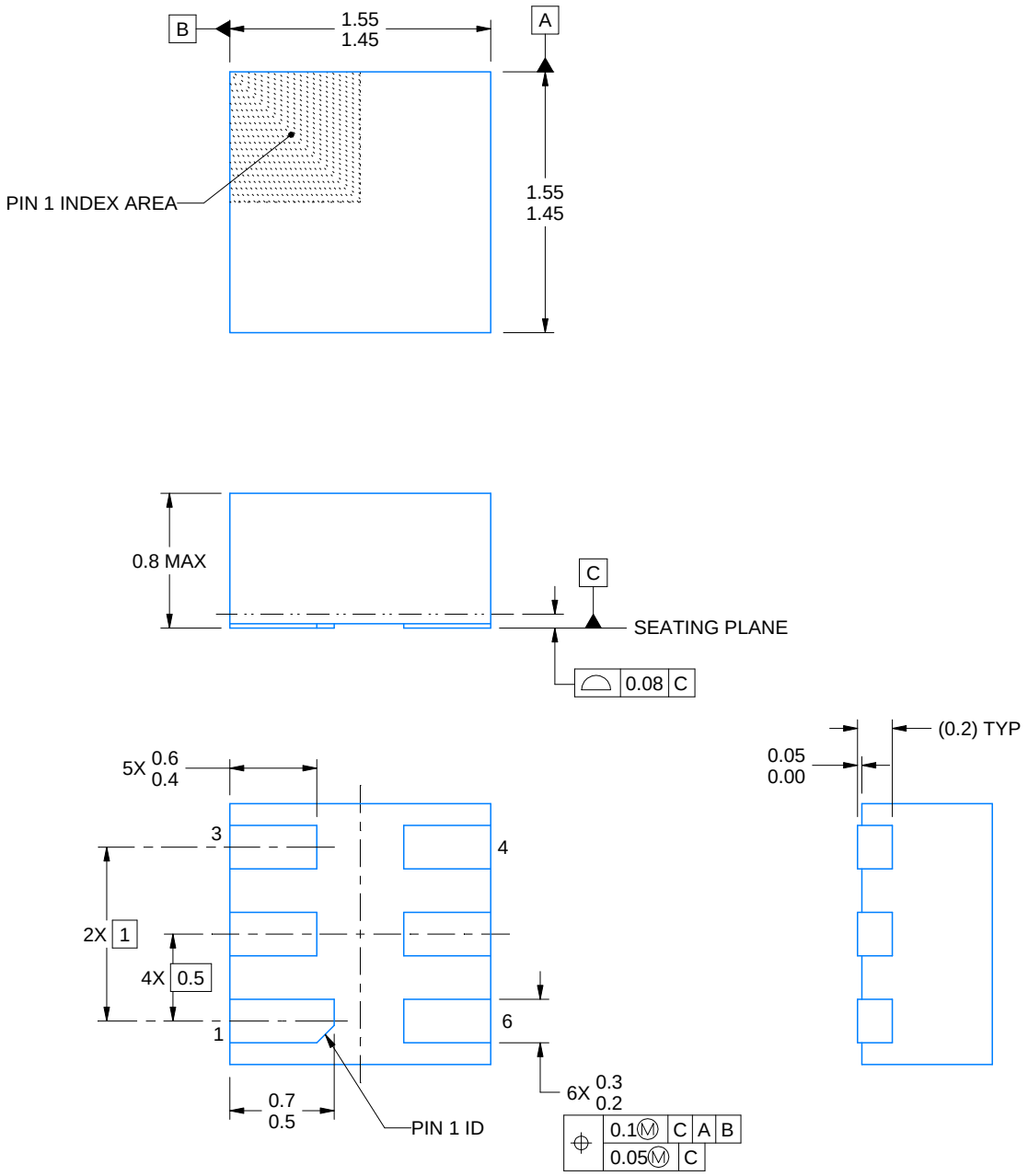
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1015PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1015PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1015PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1018PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1018PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1018PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1025PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1025PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1025PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1028PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1028PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1028PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1030PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1030PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1030PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

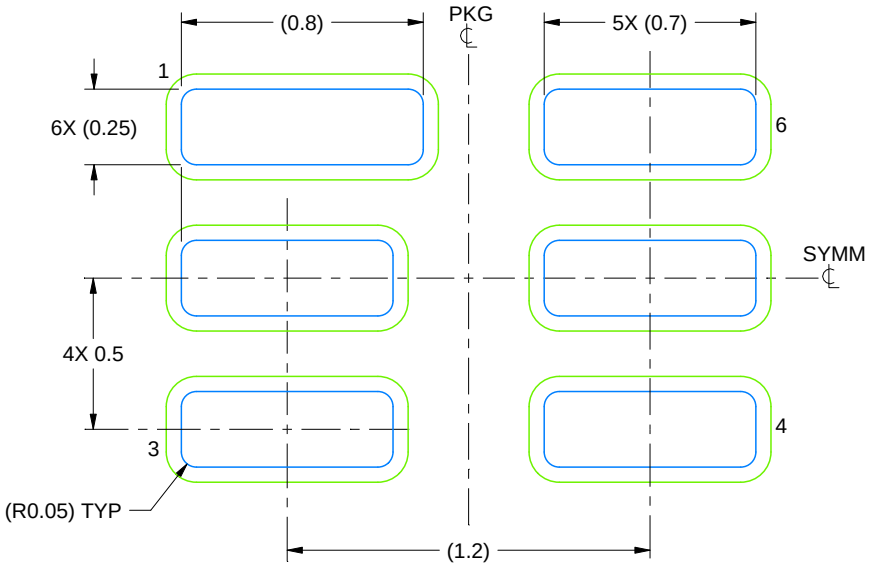
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

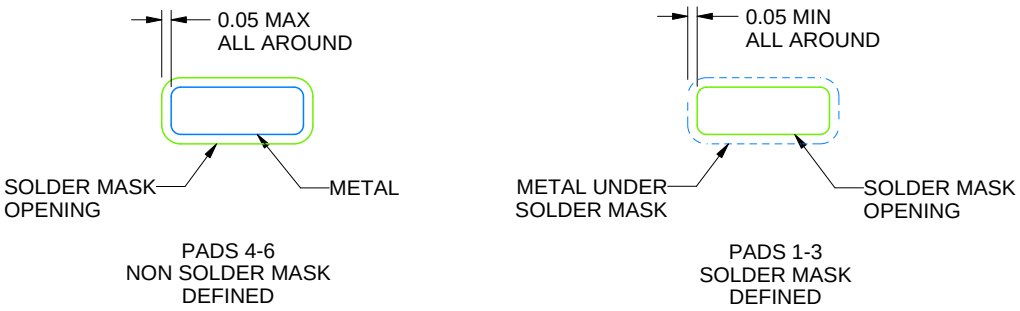
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

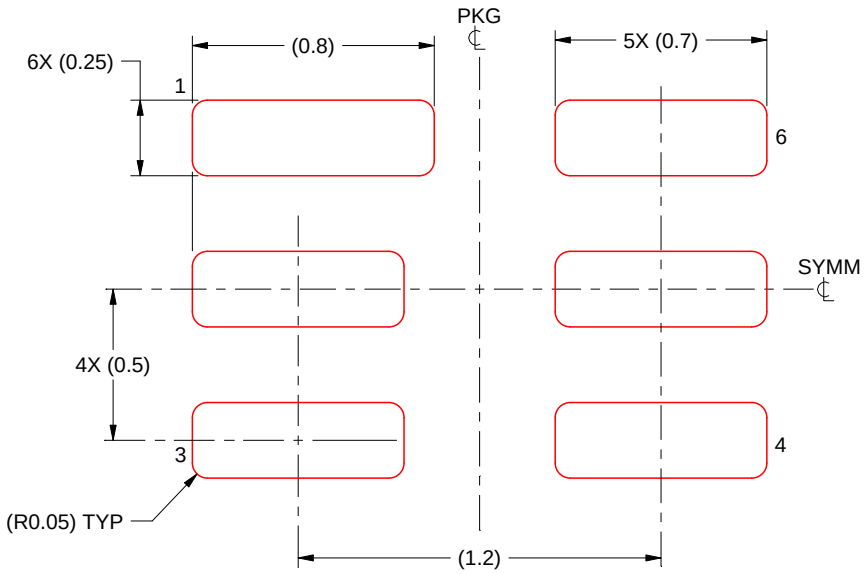
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

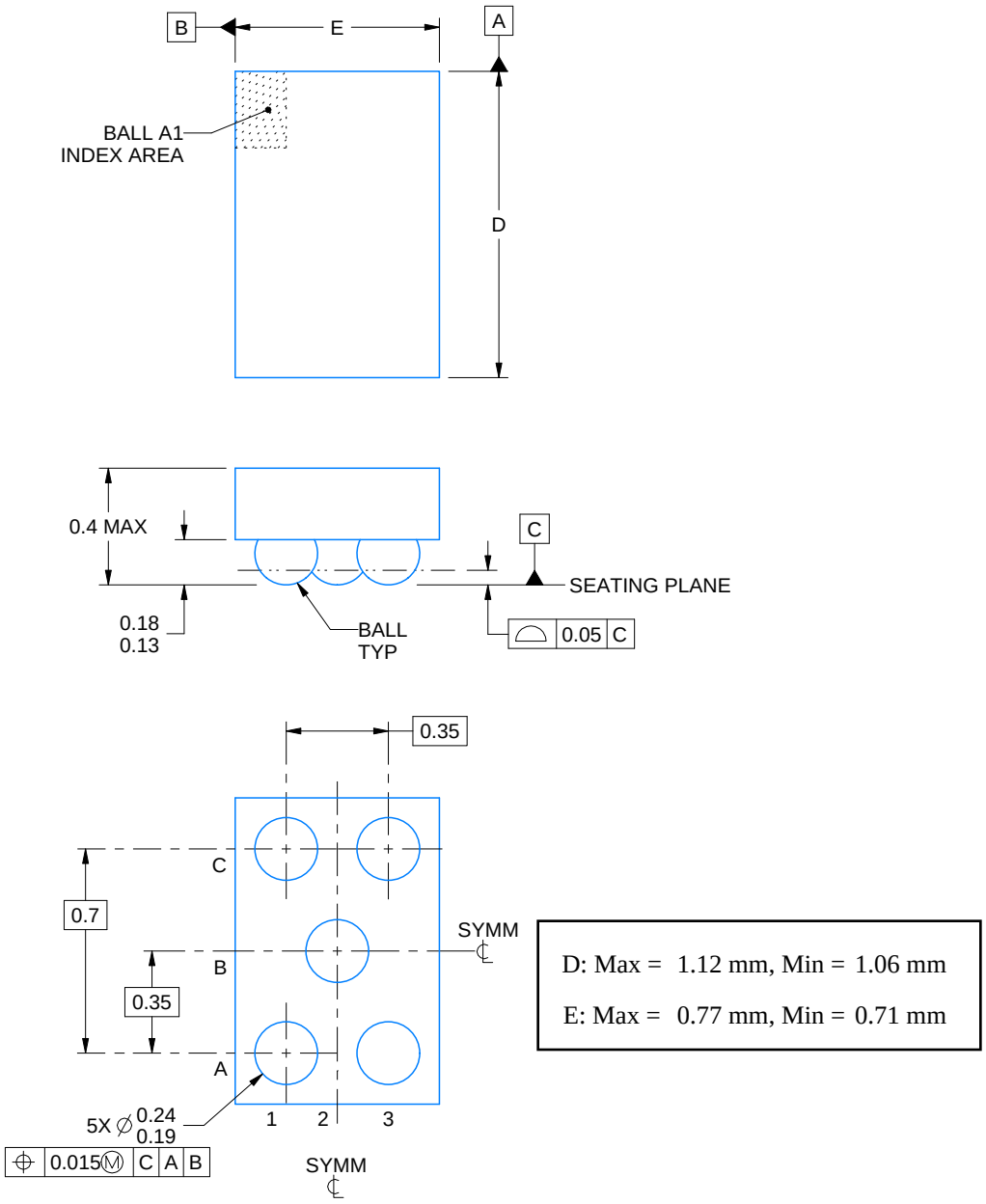
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YKA0005

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

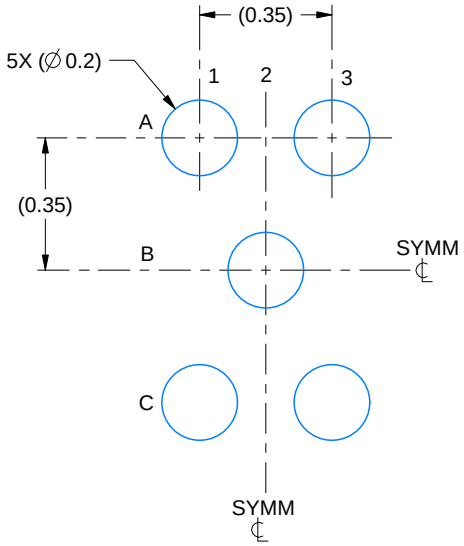


4223737/B 05/2017

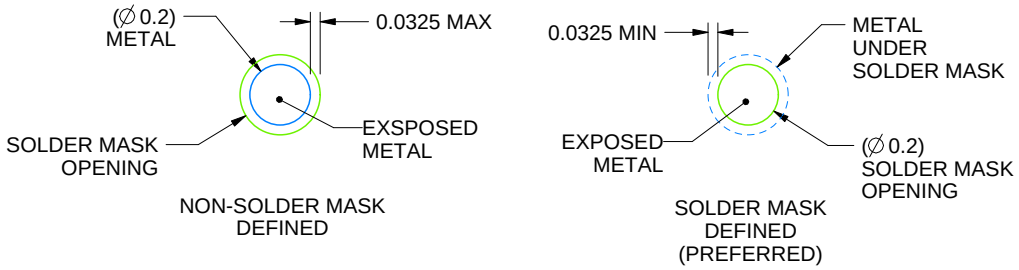
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223737/B 05/2017

NOTES: (continued)

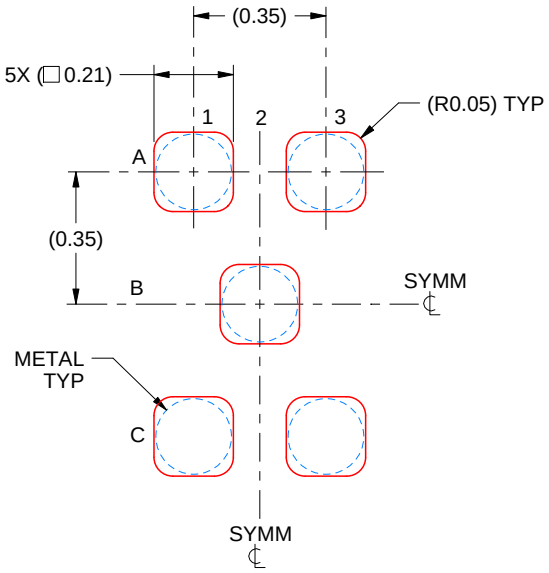
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0005

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

4223737/B 05/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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