

TPS79901-EP 200mA、低静止電流、超低ノイズ、高PSRR 低ドロップアウト・リニア・レギュレータ

1 特長

- ENを備えた200mA低ドロップアウト・レギュレータ
- 複数の出力電圧バージョンを利用可能:
 - 可変出力: 1.2V～6.5V
- ENトグルによる突入電流保護
- 低い I_Q : 40 μ A
- 高PSRR:
 - 1kHz時に66dB
 - 10kHz時に51dB
- 標準2 μ Fの低ESR出力容量で安定動作
- 非常に優れた負荷/ライン過渡応答
- 総合精度2% (負荷、ライン、温度)
- 非常に低いドロップアウト: 100mV
- パッケージ: 6ピンSON
- 防衛、航空宇宙、および医療アプリケーションをサポート
 - 管理されたベースライン
 - 単一のアセンブリ/テスト施設
 - 単一の製造施設
 - 軍用温度範囲(-55°C～125°C)で利用可能
 - 長期にわたる製品ライフ・サイクル
 - 製品変更通知の延長
 - 製品のトレーサビリティ

2 アプリケーション

- 基地局
- スマートフォン
- EPOS
- ウェアラブル・エレクトロニクス
- VCO、RF
- ワイヤレスLAN、Bluetooth®

3 概要

TPS79901ファミリの低ドロップアウト(LDO)低消費電力リニア・レギュレータは、極めて低いグラウンド電流で優れたAC性能を提供します。高い電源除去比(PSRR)、低ノイズ、高速スタートアップ、優れたライン/負荷過渡応答を実現しながら、消費するグラウンド電流はわずか40 μ A (標準)です。

TPS79901は、セラミック・コンデンサで安定動作が可能であり、また、先進のBiCMOS製造プロセスの採用により、200mA出力で標準100mVのドロップアウト電圧を実現しています。高性能な電圧リファレンスと帰還ループにより、すべての負荷、ライン、製造プロセス、および温度変化に対して2%の総合精度を達成できます。TPS79901は、ENトグルを使用したデバイス起動時の突入電流保護を特長としており、即座に電流をクランプします。

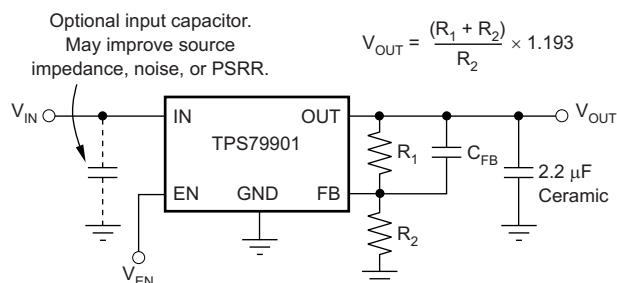
TPS79901は、 $T_J = -55^\circ\text{C} \sim +125^\circ\text{C}$ の温度範囲で仕様が完全に規定されています。低プロファイルで供給され、ワイヤレス・ハンドセットやWLANカードに最適です。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS79901-EP	SON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション回路



Copyright © 2017, Texas Instruments Incorporated



目次

1	特長	1	8	Application and Implementation	14
2	アプリケーション	1	8.1	Application Information	14
3	概要	1	8.2	Typical Applications	14
4	改訂履歴	2	8.3	Do's and Don'ts	16
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	16
6	Specifications	4	10	Layout	16
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	16
6.2	ESD Ratings	4	10.2	Layout Example	17
6.3	Recommended Operating Conditions	4	11	デバイスおよびドキュメントのサポート	18
6.4	Thermal Information	4	11.1	デバイス・サポート	18
6.5	Electrical Characteristics	5	11.2	ドキュメントのサポート	18
6.6	Typical Characteristics	7	11.3	ドキュメントの更新通知を受け取る方法	18
7	Detailed Description	12	11.4	コミュニティ・リソース	18
7.1	Overview	12	11.5	商標	19
7.2	Functional Block Diagram	12	11.6	静電気放電に関する注意事項	19
7.3	Feature Description	12	11.7	Glossary	19
7.4	Device Functional Modes	13	12	メカニカル、パッケージ、および注文情報	20

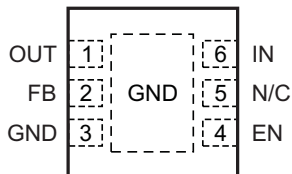
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年9月発行のものから更新		Page
• 「特長」セクションの内容 変更		1
• 「概要」セクションの内容 変更		1
• Deleted NR from the Pin Functions table		3
• Changed HBM value from ± 2000 : to ± 1500 in the <i>ESD Ratings</i> section		4
• Deleted errant part numbers from the <i>Electrical Characteristics</i> section		5
• Deleted errant part numbers from the <i>Typical Characteristics</i> section		7

5 Pin Configuration and Functions

**DRV Package
6-Pin SON With Exposed Thermal Pad
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	6	I	Input supply.
GND	3, Pad	—	Ground. The pad must be tied to GND.
EN	4	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	2	I	Adjustable voltage version only. Feedback; this pin is the input to the control loop error amplifier and sets the output voltage of the device.
OUT	1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance $\geq 2 \mu\text{F}$) is required from this pin to ground.
N/C	5	—	Not internally connected. This pin must either be left open or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN	–0.3	7	V
	EN	–0.3	$V_{IN} + 0.3$	
	OUT	–0.3	$V_{IN} + 0.3$	
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage temperature range, T_{stg}	–55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage ⁽¹⁾	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–55		125	°C

- (1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS799	UNIT
		DRV (SON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	145.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

at $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		6.5	V
V_{FB}	Internal reference			1.169	1.193	1.217	V
V_{OUT}	Output voltage range			V_{FB}	$6.5 - V_{DO}$		V
	Output accuracy, nominal	$T_J = 25^{\circ}\text{C}$		-1%		1%	
	Output accuracy ⁽¹⁾ over V_{IN} , I_{OUT} , temperature	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ $500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$		-2%	$\pm 1\%$	2%	
$\Delta V_{O(\Delta V)}$	Line regulation ⁽¹⁾	$V_{OUT(nom)} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$			0.02		%/V
$\Delta V_{O(\Delta I)}$	Load regulation	$500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$			0.002		%/mA
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$)	$I_{OUT} = 200\text{ mA}$	$V_{OUT(nom)} \leq 3.3\text{ V}$		100	175	mV
			$V_{OUT(nom)} \geq 3.3\text{ V}$		90	160	
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$		220	400	600	mA
I_{GND}	Ground pin current	$500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$			40	60	μA
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.4\text{ V}$, $2.7\text{ V} \leq V_{IN} \leq 6.5\text{ V}$			0.15	1	μA
I_{FB}	Feedback pin current			-0.5		0.5	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 3.85\text{ V}$, $V_{OUT} = 2.85\text{ V}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $I_{OUT} = 100\text{ mA}$	$f = 100\text{ Hz}$		70		dB
			$f = 1\text{ kHz}$		66		
			$f = 10\text{ kHz}$		51		
			$f = 100\text{ kHz}$		38		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, $V_{OUT} = 2.85\text{ V}$	$C_{NR} = 0.01\text{ }\mu\text{F}$		$10.5 \times V_{OUT}$		μVRMS
			$C_{NR} = \text{none}$		$94 \times V_{OUT}$		
	Start-up time	$V_{OUT} = 2.85\text{ V}$, $R_L = 14\text{ }\Omega$, $C_{OUT} = 2.2\text{ }\mu\text{F}$	$C_{NR} = 0.001\text{ }\mu\text{F}$		45		μs
			$C_{NR} = 0.047\text{ }\mu\text{F}$		45		
			$C_{NR} = 0.01\text{ }\mu\text{F}$		50		
			$C_{NR} = \text{none}$		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	$V_{EN} = V_{IN} = 6.5\text{ V}$			0.03	1	μA
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	UVLO hysteresis	V_{IN} falling			70		mV
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			165		$^{\circ}\text{C}$
		Reset, temperature decreasing			145		

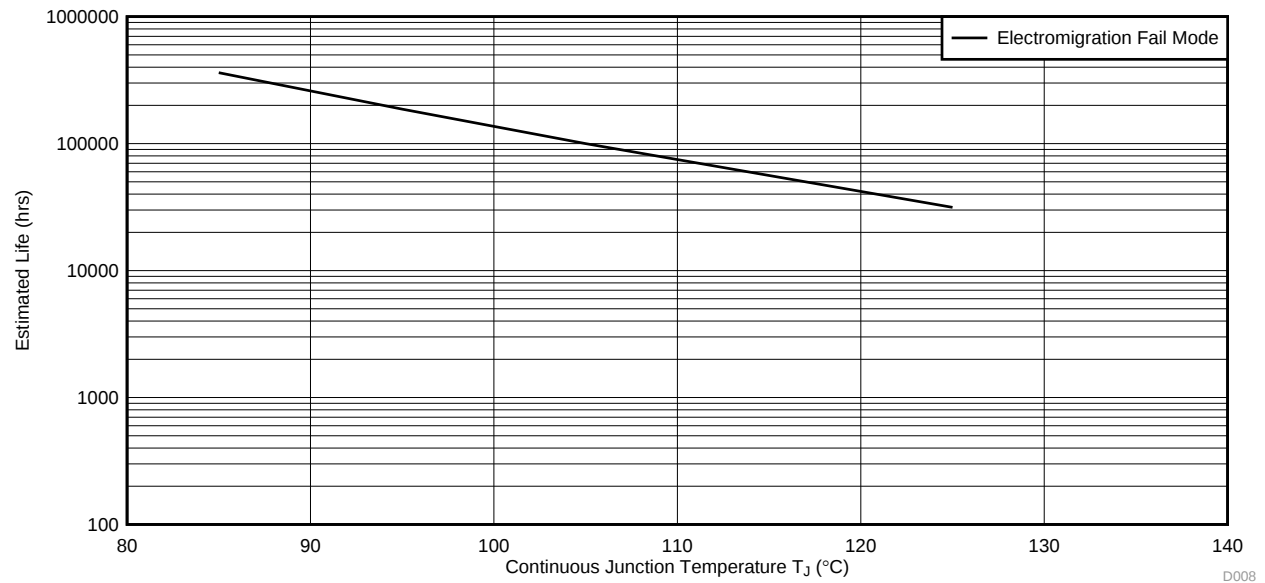
(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V , whichever is greater.

(2) V_{DO} is not measured for $V_{OUT(nom)} < 2.8\text{ V}$ because minimum $V_{IN} = 2.7\text{ V}$.

TPS79901-EP

JAJSDS1A – SEPTEMBER 2017 – REVISED OCTOBER 2017

www.ti.com



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

Figure 1. TPS79901-EP Derating Chart

6.6 Typical Characteristics

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

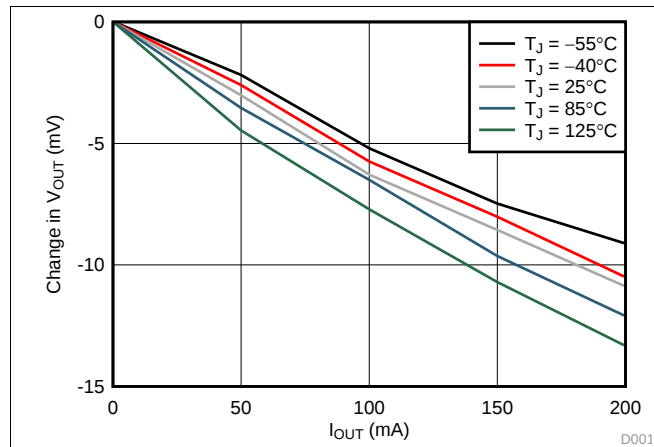


Figure 2. Load Regulation

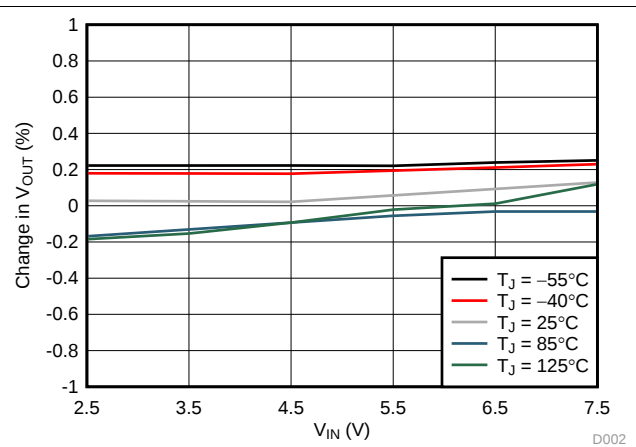


Figure 3. Line Regulation

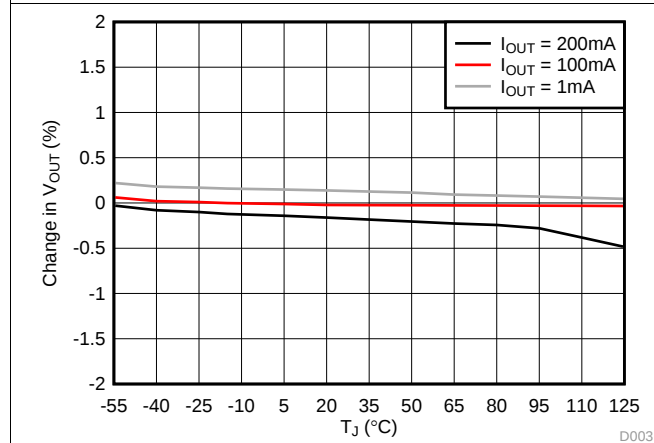


Figure 4. Output Voltage vs Junction Temperature

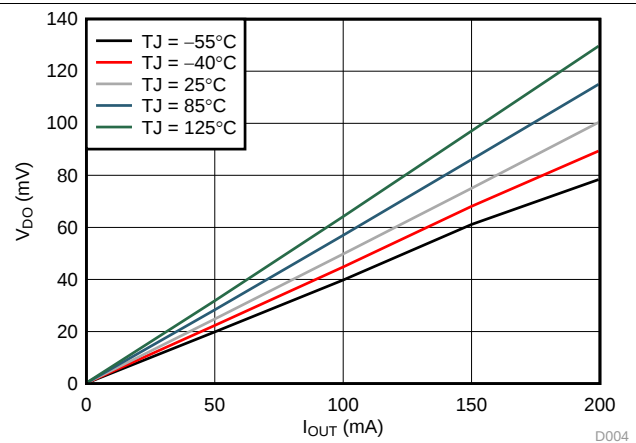


Figure 5. Dropout Voltage vs Output Current

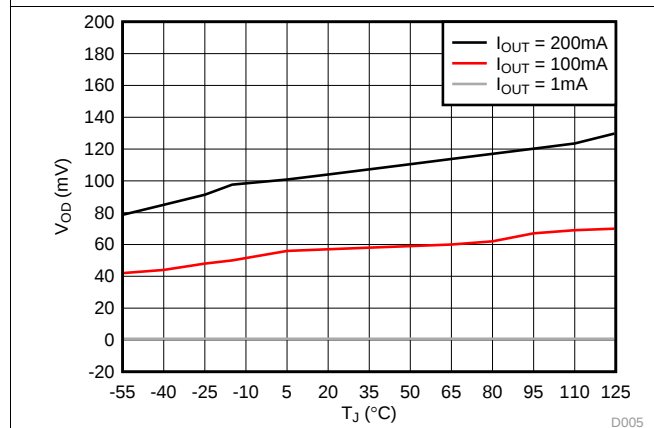


Figure 6. Dropout Voltage vs Junction Temperature

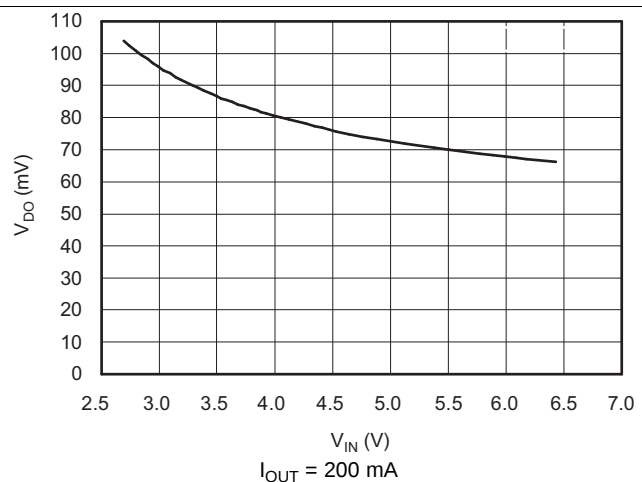


Figure 7. Dropout vs Input Voltage

Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

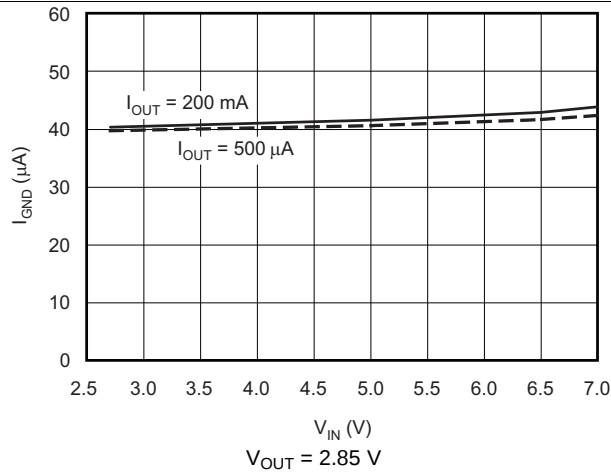


Figure 8. Ground Pin Current vs Input Voltage

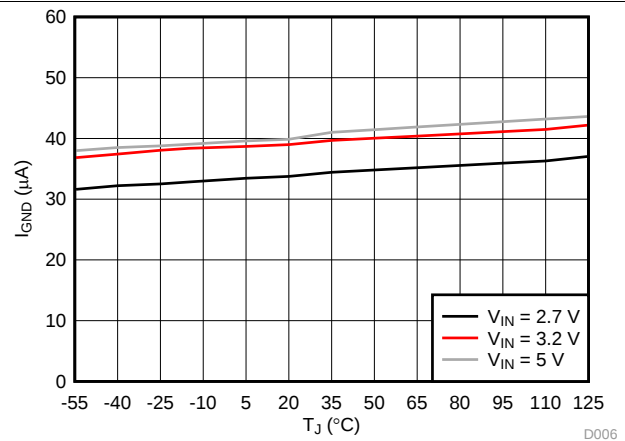


Figure 9. Ground Pin Current vs Junction Temperature

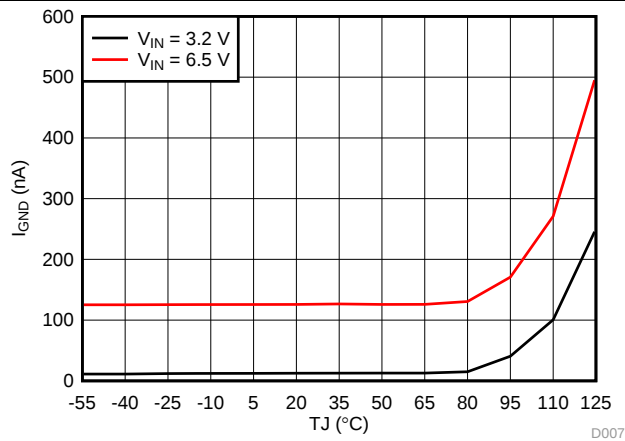


Figure 10. Ground Pin Current (Disabled) vs Junction Temperature

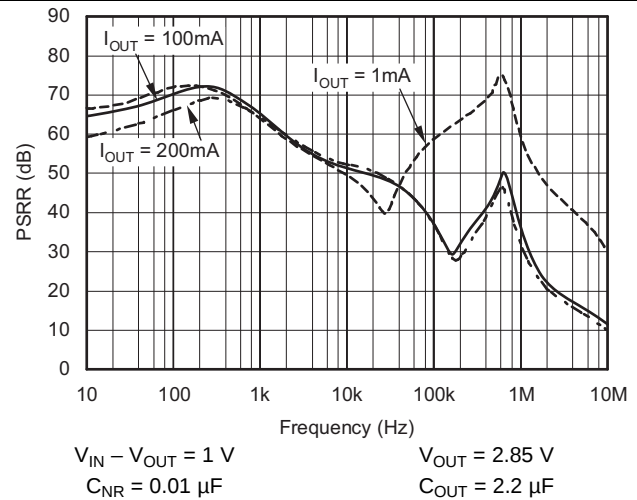


Figure 11. Power-Supply Ripple Rejection vs Frequency

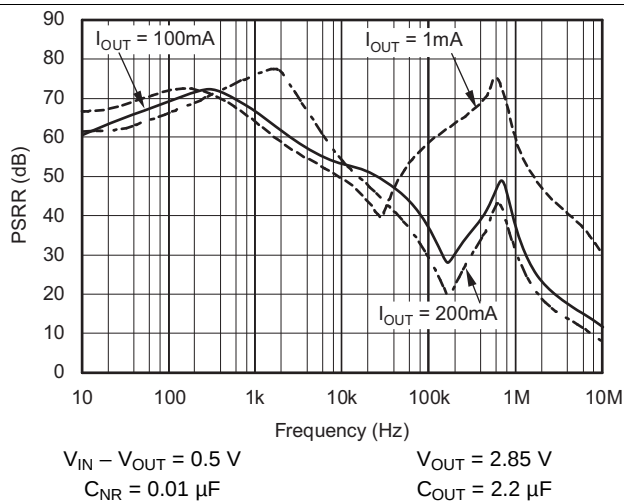


Figure 12. Power-Supply Ripple Rejection vs Frequency

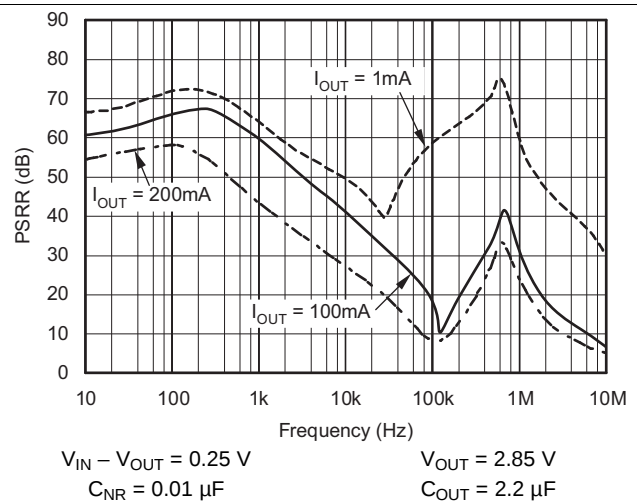


Figure 13. Power-Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

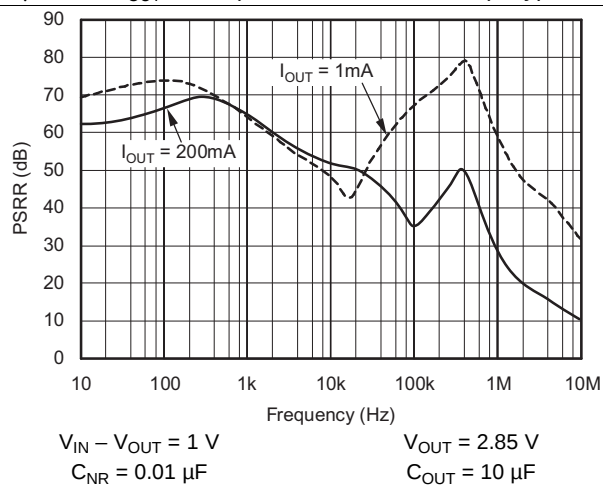


Figure 14. Power-Supply Ripple Rejection vs Frequency

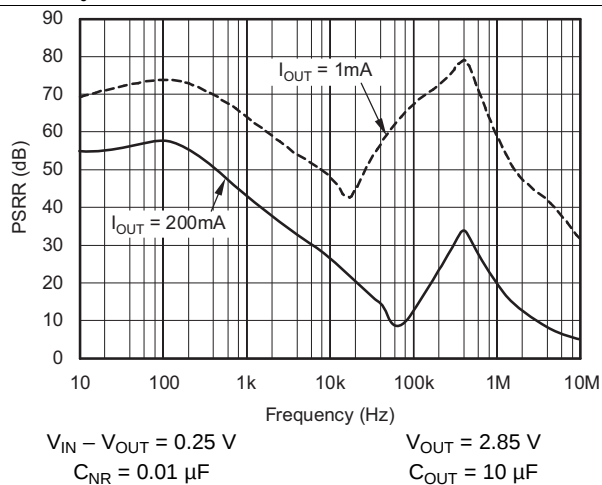


Figure 15. Power-Supply Ripple Rejection vs Frequency

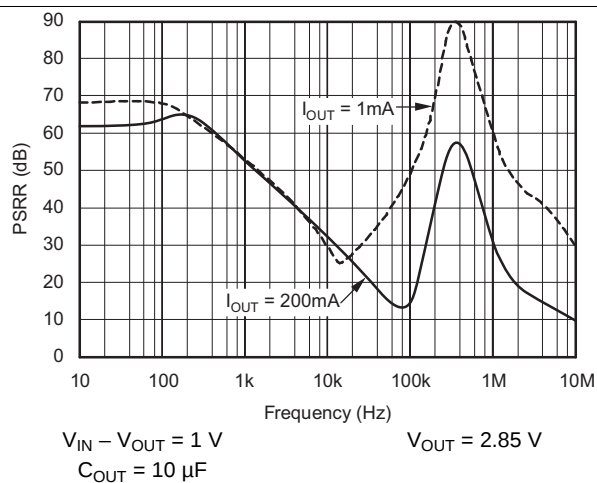


Figure 16. Power-Supply Ripple Rejection vs Frequency

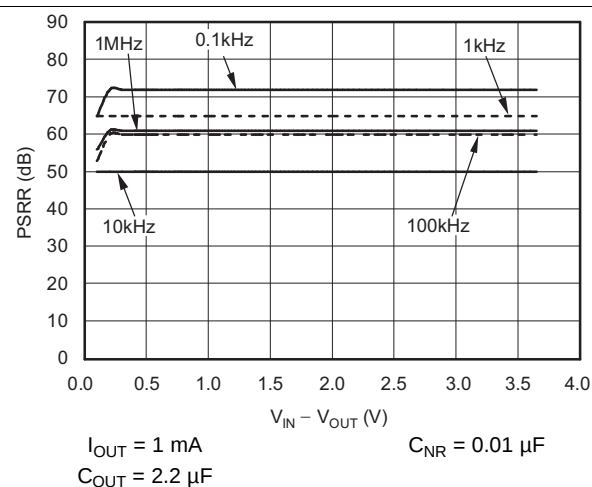


Figure 17. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

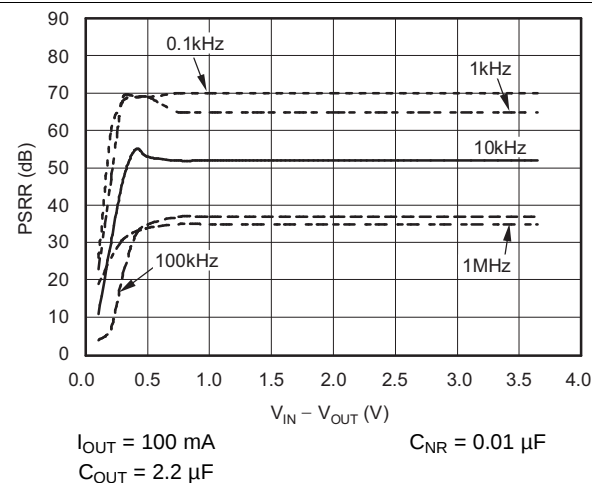


Figure 18. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

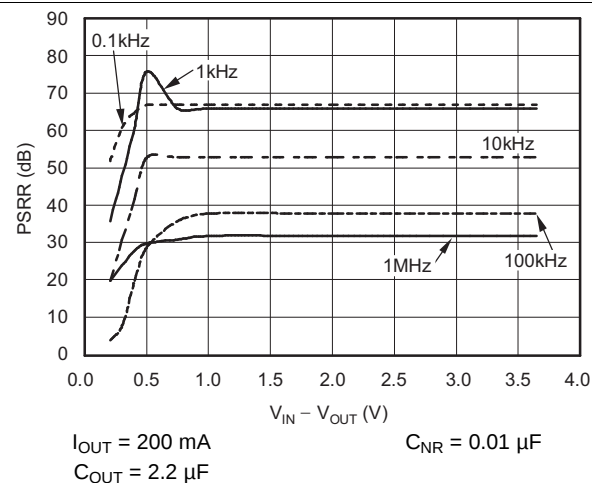
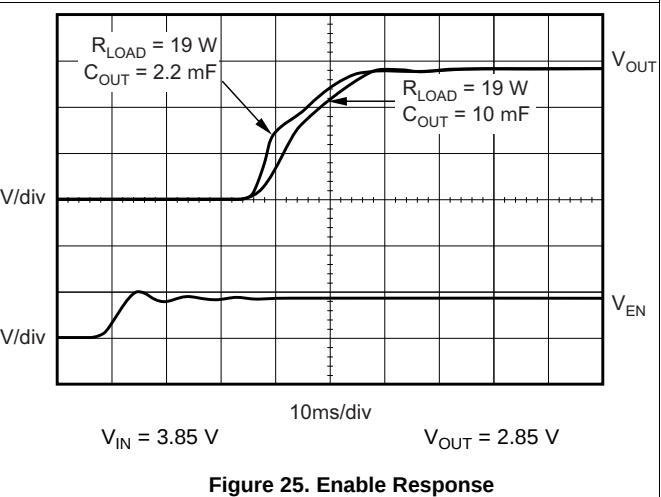
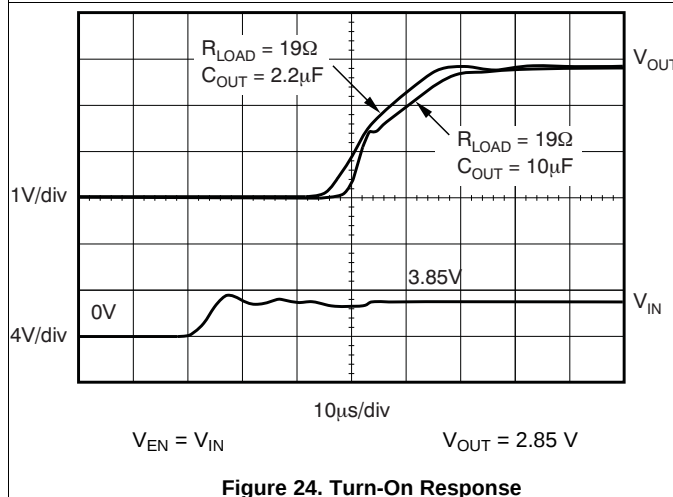
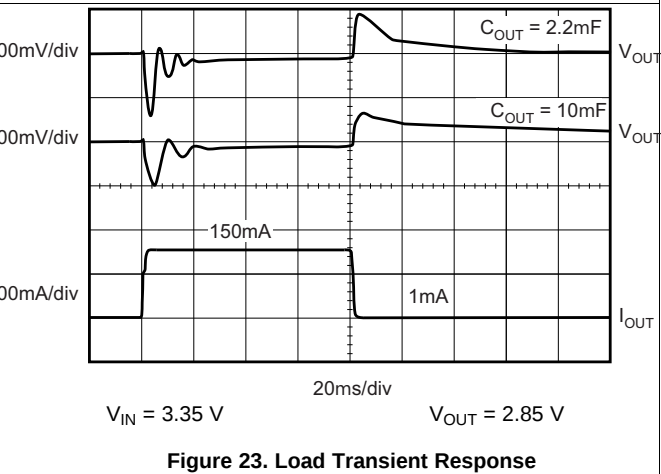
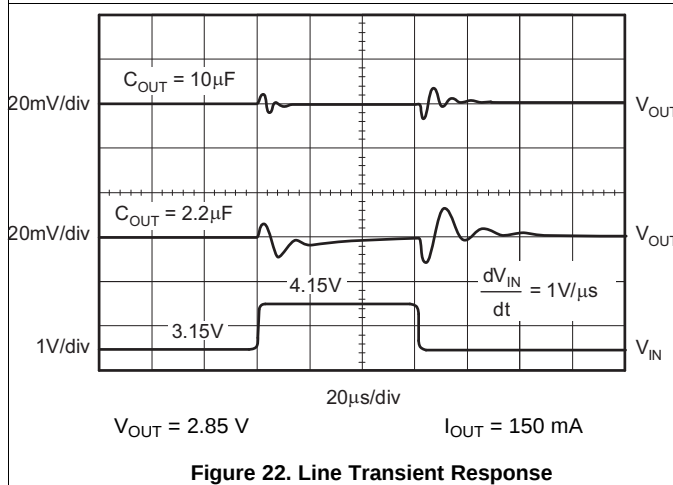
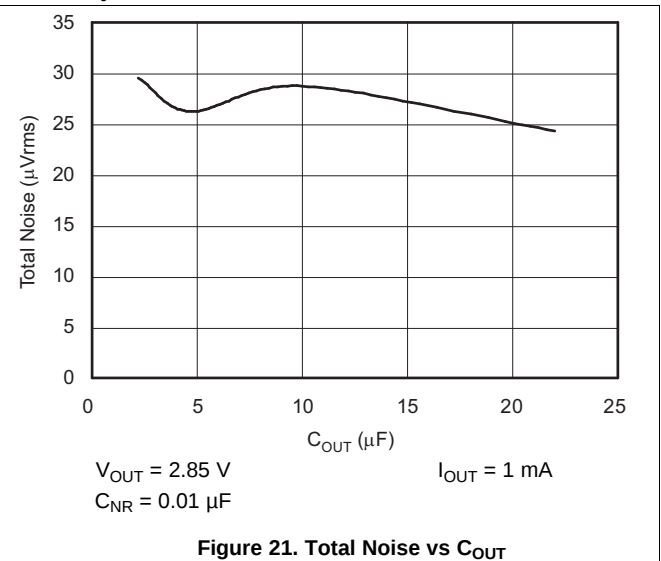
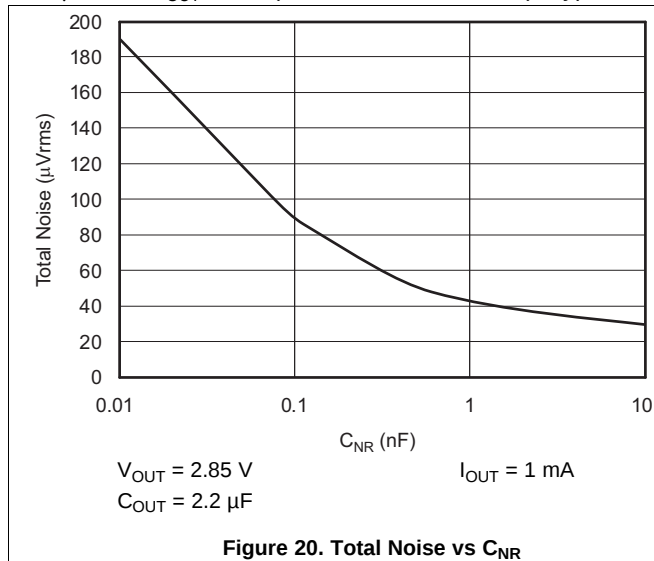


Figure 19. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

Typical Characteristics (continued)

at $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.



Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

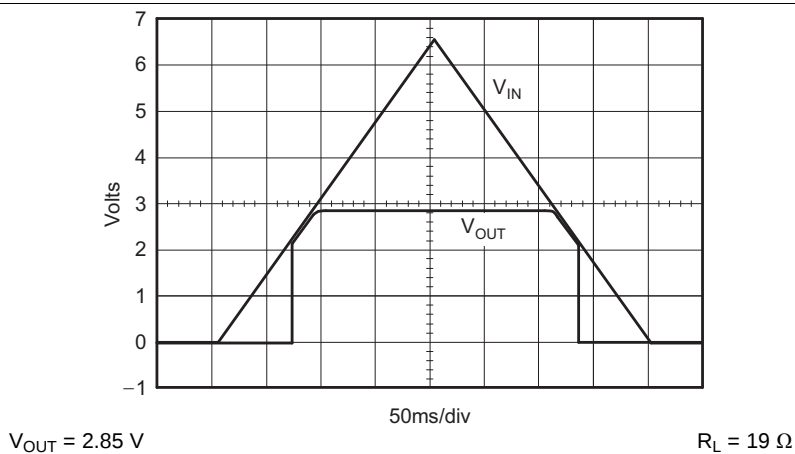


Figure 26. Power-Up and Power-Down

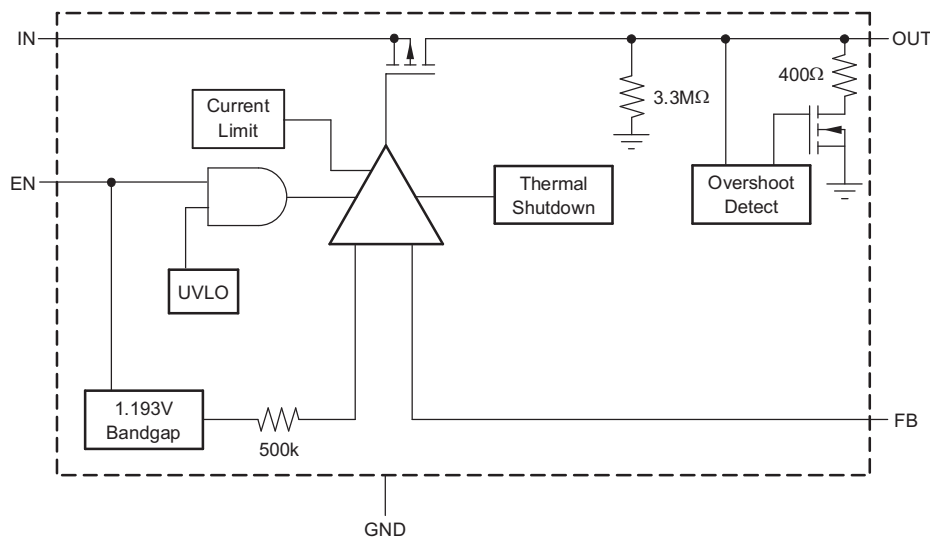
7 Detailed Description

7.1 Overview

The TPS79901 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with ultra-low-current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from -55°C to $+125^{\circ}\text{C}$.

The TPS79901 also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in the [Functional Block Diagram](#).

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

Figure 27. Adjustable-Voltage Versions

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS79901 internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS79901 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Feature Description (continued)

7.3.3 Start Up

The TPS79901 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR} , if present (see the [Functional Block Diagram](#)). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 μ s. To ensure that C_{NR} is fully charged during start-up, use a 0.01- μ F or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS79901 use an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 μ s in duration.

7.4 Device Functional Modes

Driving EN over 1.2-V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

NOTE

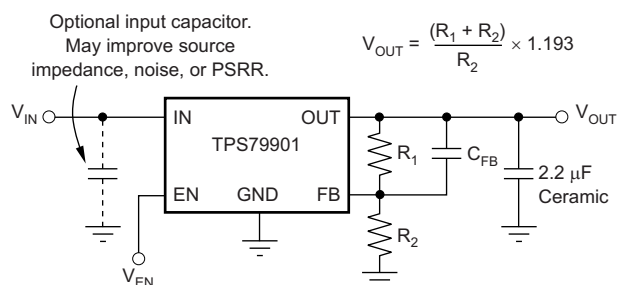
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS79901 LDO regulator provides high PSRR while maintaining ultra-low-current consumption. The device also features inrush current protection and overshoot detection at the output.

8.2 Typical Applications

Figure 28 shows the basic circuit connections.



Copyright © 2017, Texas Instruments Incorporated

Figure 28. Typical Application Circuit for Adjustable Voltage Version

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

Typical Applications (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 1-μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS79901 is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

8.2.2.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS79901, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with $C_{NR} = 0.01 \mu\text{F}$ total noise is approximately given by [Equation 1](#):

$$V_N = \frac{10.5 \mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

8.2.2.3 Dropout Voltage

The TPS79901 uses a PMOS pass transistor to achieve a low-dropout voltage. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{\text{DS(on)}}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout. This effect is illustrated in [Figure 11](#) through [Figure 19](#) in the [Typical Characteristics](#) section.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799 is enhanced by an active pulldown device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

8.2.2.5 Minimum Load

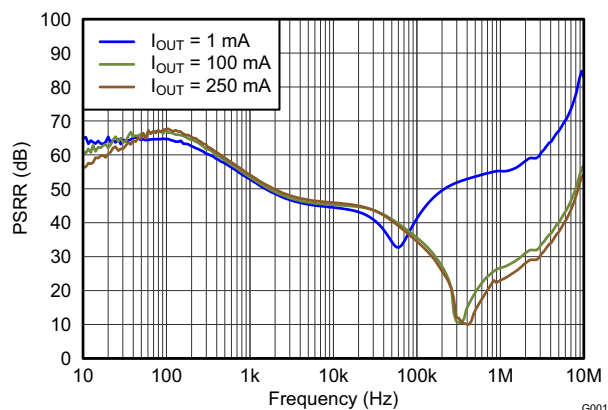
The TPS79901 is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. With loads less than 500 μA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown device to turn on. The output pulldown device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 μA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2.6 Feedback Capacitor Requirements

The feedback capacitor, C_{FB} , shown in [Figure 28](#) is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB} .

Typical Applications (continued)

8.2.3 Application Curve



$$C_{OUT} = 2.2 \mu F$$

$$C_{NR} = 0.01 \mu F$$

Figure 29. Power-Supply Rejection Ratio vs Frequency

8.3 Do's and Don'ts

Do place at least one 2.2- μF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1- μF to 1- μF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.2 Thermal Information

10.1.2.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Layout Guidelines (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

10.1.2.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

10.1.2.3 Package Mounting

Solder pad footprint recommendations for the TPS799 are available from the TI's website at www.ti.com.

10.2 Layout Example

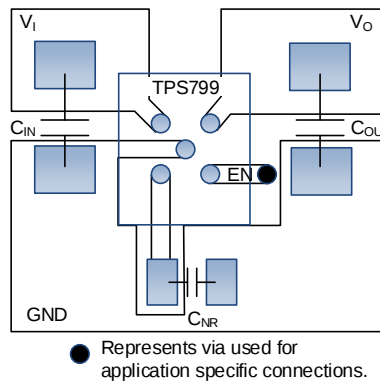


Figure 30. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS799を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。このEVM、TPS799評価モジュールは、テキサス・インスツルメンツのWebサイトの製品フォルダからご請求されるか、[TI eStore](#)から直接お求めになれます。

11.1.1.2 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TPS799用のSPICEモデルは、製品フォルダの「シミュレーション・モデル」で入手できます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- アプリケーション・レポート: 『新しい熱測定基準の使用』、[SBVA025](#)
- アプリケーション・レポート: 『ICパッケージの熱指標』、[SPRA953](#)
- 『TPS799xxEVM-105 ユーザー・ガイド』、[SLVU130](#)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79901MDRVTEP	Active	Production	WSO (DRV) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L
V62/17614-01XE	Active	Production	WSO (DRV) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

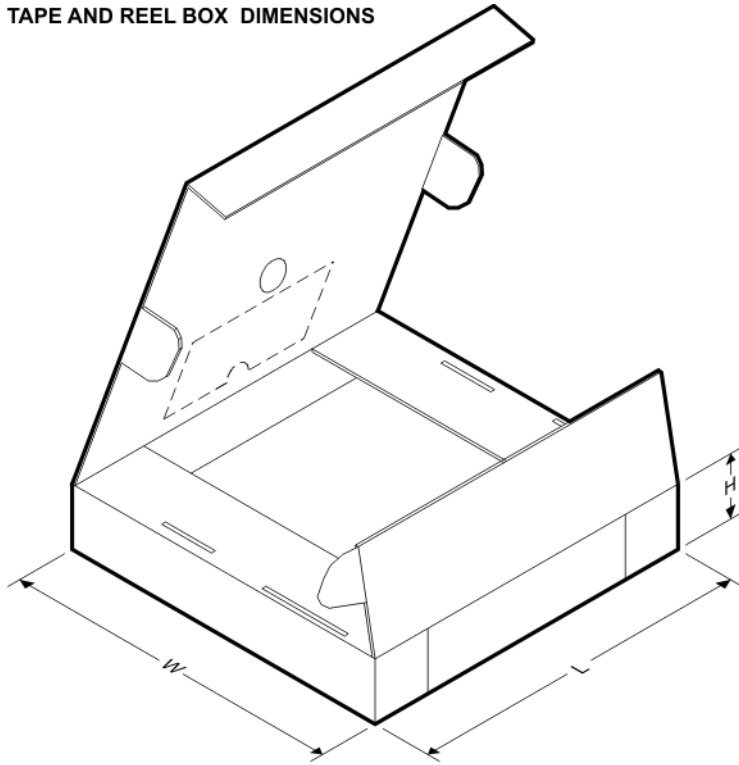
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

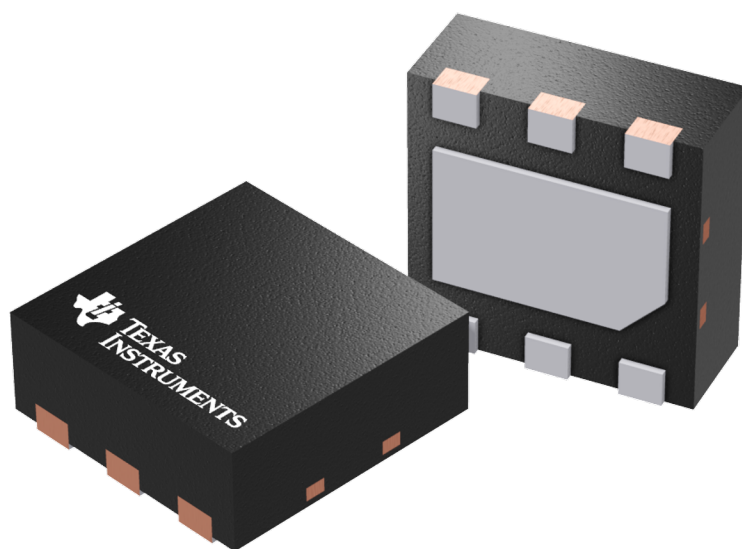
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901MDRVTEP	WSO	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

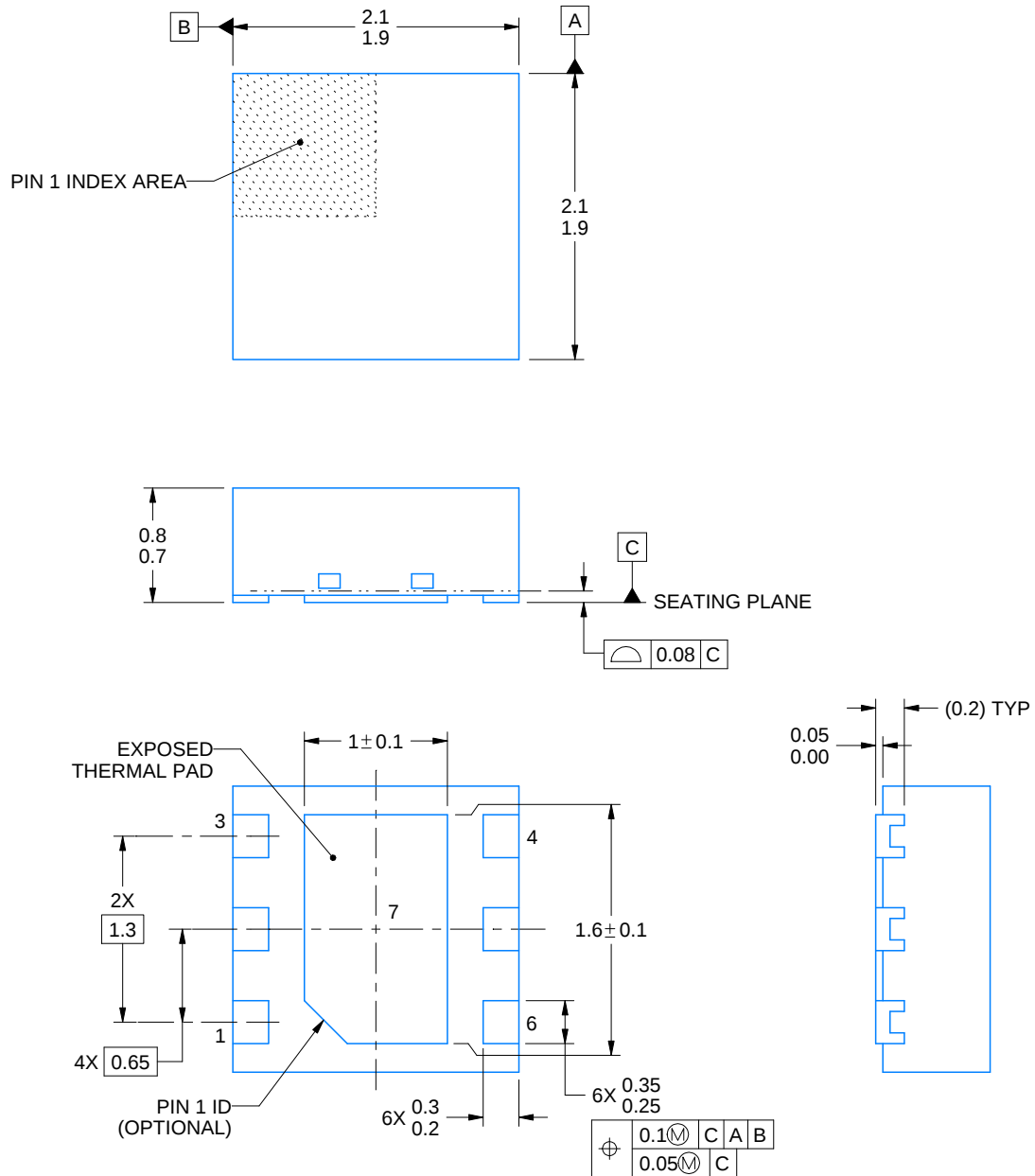


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901MDRVTEP	WSON	DRV	6	250	200.0	183.0	25.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225563/A 12/2019

NOTES:

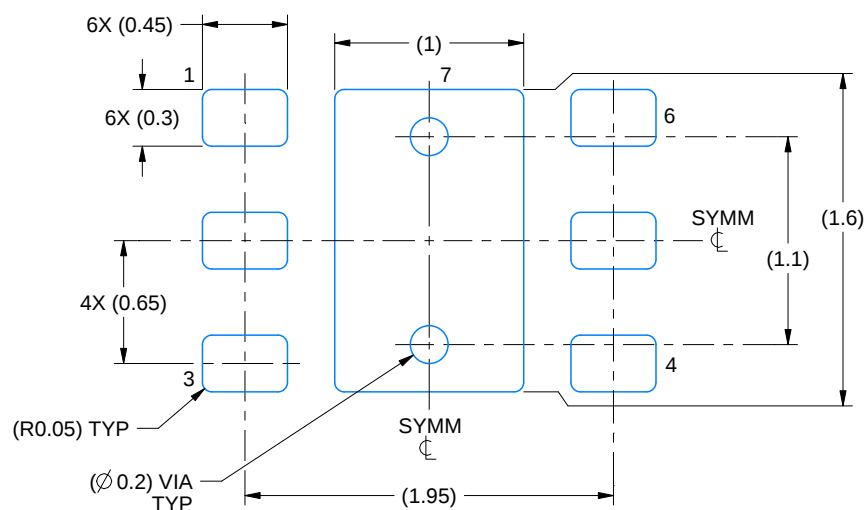
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

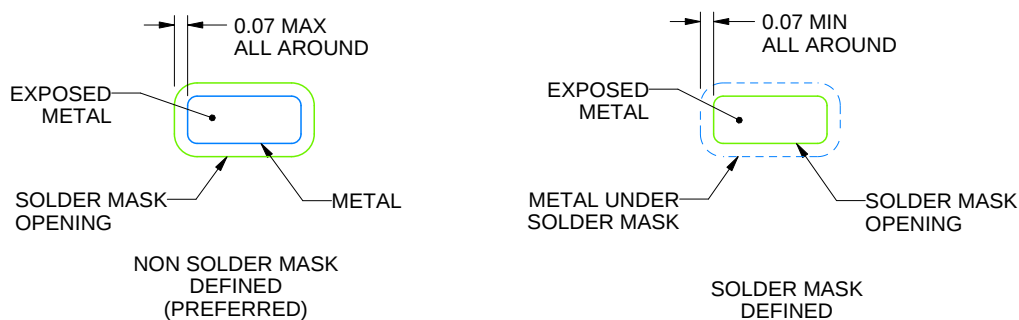
DRV0006D

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

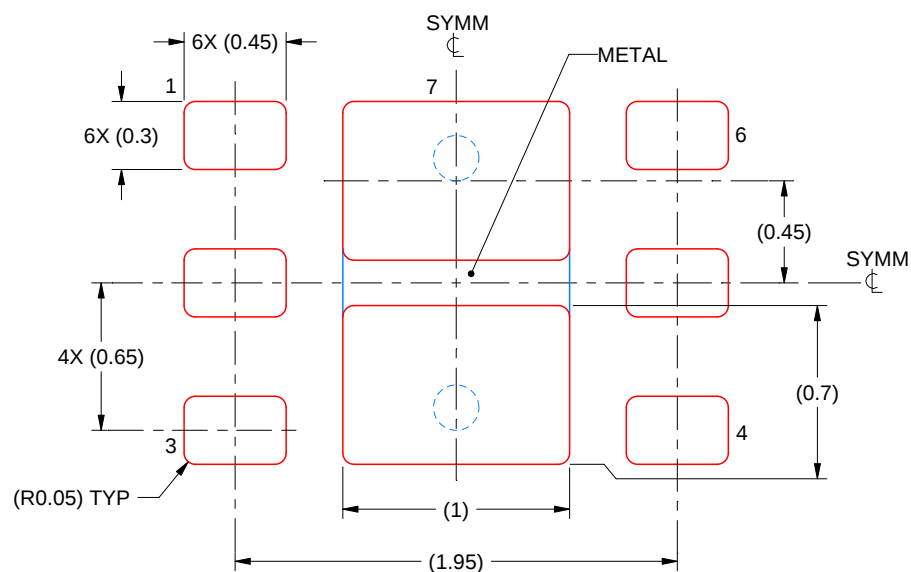
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006D

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとしします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated