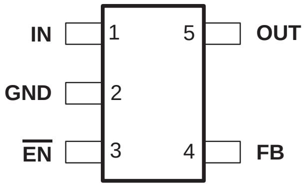
TPS76201
LOW OUTPUT ADJUSTABLE
ULTRALOW-POWER 100-mA LDO LINEAR REGULATOR

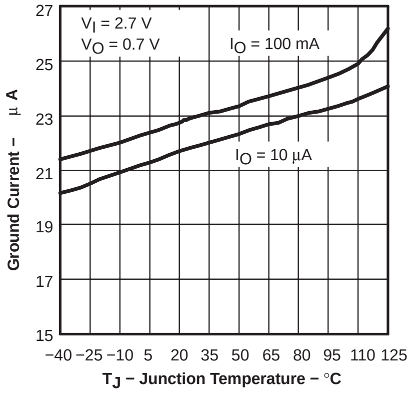
SLVS323B − FEBRUARY 2001 − REVISED JANUARY 2007

- **100-mA Low-Dropout Regulator**
- **Adjustable Output Voltage (0.7 V to 5.5 V)**
- **Only 23 µA Quiescent Current at 100 mA**
- **1 µA Quiescent Current in Standby Mode**
- **Over Current Limitation**
- **−40°C to 125°C Operating Junction Temperature Range**
- **5-Pin SOT-23 (DBV) Package**

DBV PACKAGE
(TOP VIEW)



GROUND CURRENT
vs
JUNCTION TEMPERATURE



description

The TPS76201 low-dropout (LDO) voltage regulator features an adjustable output voltage as low as 0.7 V. It is an ideal regulator for sub 1.2-V DSP core voltage supplies and is equally suited for similar applications with other low-voltage processors and controllers. SOT-23 packaging and the high-efficiency that results from the regulator's ultralow power operation make the TPS76201 especially useful in handheld and portable battery applications. This regulator features low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS76201 is ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (30 µA maximum) and is stable over the entire range of output load current (10 µA to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-power operation results in a significant increase in the system battery operating life.

The TPS76201 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 µA typical at T_J = 25°C. The TPS76201 is offered in an adjustable version (programmable over the range of 0.7 V to 5.5 V).

AVAILABLE OPTIONS[†]

T_J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
−40°C to 125°C	Variable 0.7 V to 5.5 V	SOT-23 (DBV)	TPS76201DBVT[‡]	TPS76201DBVR[§]	PFUI

[†] Contact the factory for availability of fixed output options.
[‡] The DBVT indicates tape and reel of 250 parts.
[§] The DBVR indicates tape and reel of 3000 parts.

TEXAS INSTRUMENTS
www.ti.com

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1)	−0.3 V to 13.5 V
Voltage range at $\overline{EN}$	−0.3 V to V_I + 0.3 V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K‡	DBV	65.8°C/W	259°C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K§	DBV	65.8°C/W	180°C/W	5.6 mW/°C	555 mW	305 mW	222 mW

‡ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

§ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 2)	2.7		10	V
Output voltage range, V_O	0.7		5.5	V
Continuous output current, I_O (see Note 3)	0.01		100	mA
Operating junction temperature, T_J	−40		125	°C

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_{Imin} = V_{Omax} + V_{DO}$(max load)

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, I_O = 100 mA, $\overline{EN}$ = 0 V, C_o = 4.7 μF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 100 mA load) (see Note 4)	0.7 V ≤ V_O ≤ 5.5 V, T_J = 25°C		V_O		V
	0.7 V ≤ V_O ≤ 5.5 V, T_J = −40°C to 125°C	0.97V_O		1.03V_O	
Quiescent current (GND current) (see Notes 4 and 5)	$\overline{EN}$ = 0V, T_J = 25°C 10 μA < I_O < 100 mA		23		μA
	$\overline{EN}$ = 0 V, T_J = −40°C to 125°C, 10 μA < I_O < 100 mA			30	
Load regulation	$\overline{EN}$ = 0 V, T_J = 25°C 10 μA < I_O < 100 mA		12		mV
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 5)	2.7 V < V_I ≤ 10 V, T_J = 25°C, See Note 4		0.04		%/V
	2.7 V < V_I ≤ 10 V, T_J = −40°C to 125°C, See Note 4			0.1	
Output noise voltage	BW = 300 Hz to 50 kHz, C_O = 10 μF, V_O = 0.7 V, T_J = 25°C		60		μV_{RMS}
Output current limit	V_O = 0 V, See Note 4		350	750	mA
Standby current	$\overline{EN}$ = V_I, 2.7 < V_I < 10 V		1		μA
	T_J = −40°C to 125°C			2	μA
FB input current	FB = 0.666 V	−1		1	μA
High level enable input voltage	2.7 V < V_I < 10 V	1.7			V
Low level enable input voltage	2.7 V < V_I < 10 V			0.8	V
Power supply ripple rejection	f = 1 kHz, C_O = 10 μF, T_J = 25°C, See Note 4		60		dB
Input current ($\overline{EN}$)	$\overline{EN}$ = 0 V	−1	0	1	μA
	$\overline{EN}$ = V_I	−1		1	μA

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA, maximum output current 100 mA.

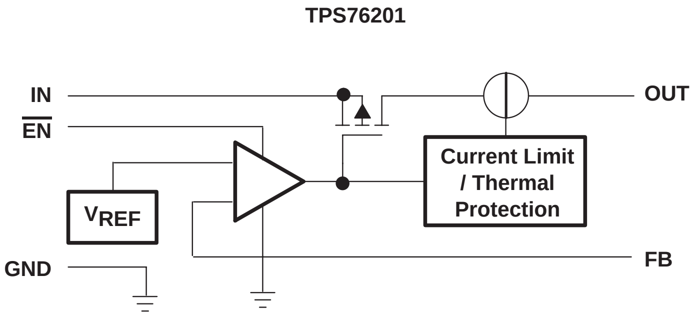
5. If $V_O \le 1.8$ V then V_{Imin} = 2.7 V, V_{Imax} = 10 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - 2.7\ \text{V}\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{Imin} = V_O + 1$ V, V_{Imax} = 10 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ \text{V}\right)\right)}{100} \times 1000$$

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	2		Ground
$\overline{EN}$	3	I	Enable input
FB	4	I	Feedback voltage
IN	1	I	Input supply voltage
OUT	5	O	Regulated output voltage

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1, 2
		vs Junction temperature	3
	Ground current	vs Junction temperature	4
	Output spectral noise density	vs Frequency	5
z_o	Output impedance	vs Frequency	6
V_{DO}	Dropout voltage	vs Input voltage	7
		vs Junction temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output voltage and enable voltage	vs Time (start-up)	10
	Line transient response		11, 13
	Load transient response		12, 14
	Equivalent series resistance (ESR)	vs Output current	15, 16

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

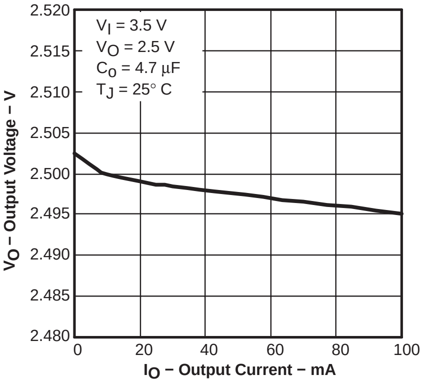


Figure 1

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

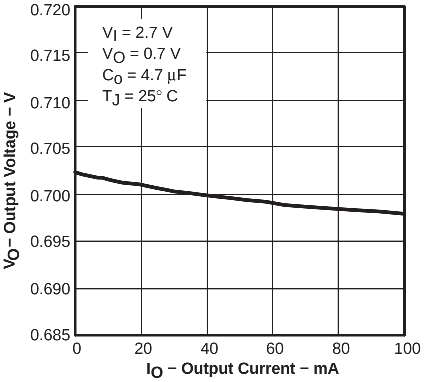


Figure 2

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

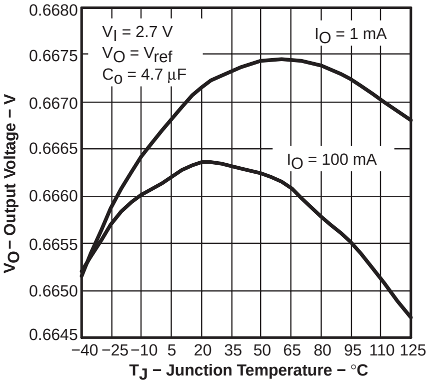


Figure 3

GROUND CURRENT
vs
JUNCTION TEMPERATURE

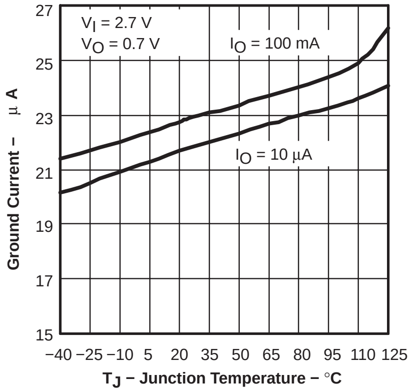


Figure 4

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

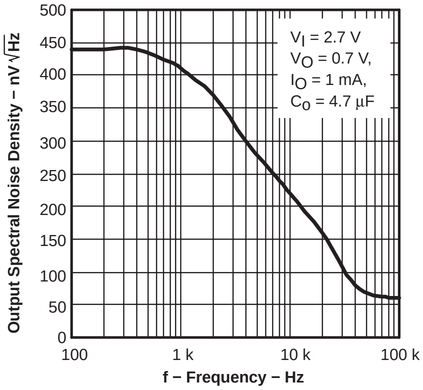


Figure 5

OUTPUT IMPEDANCE
vs
FREQUENCY

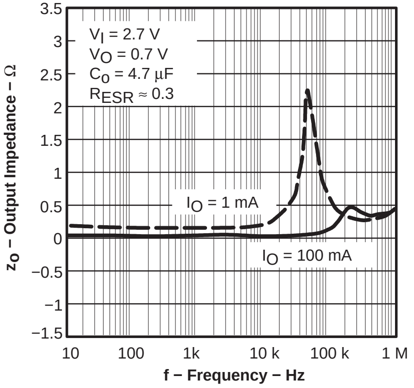


Figure 6

DROPOUT VOLTAGE
vs
INPUT VOLTAGE

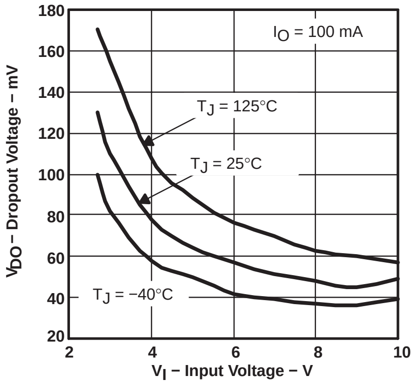


Figure 7

DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

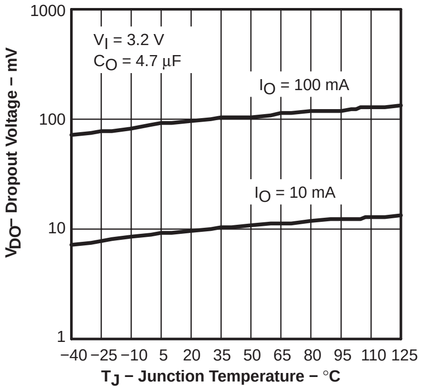


Figure 8

POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

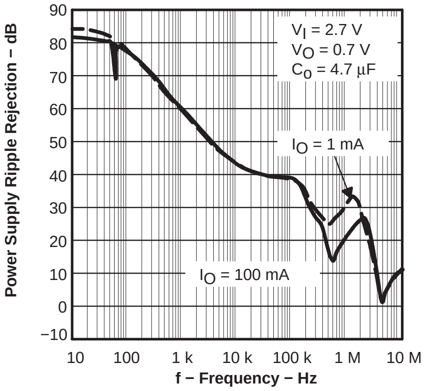
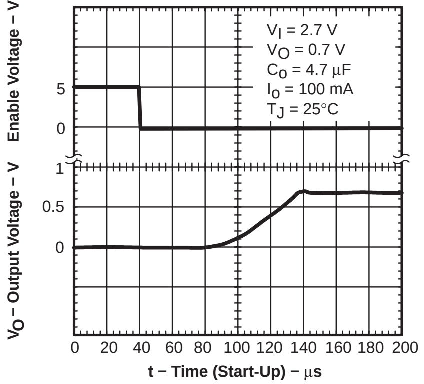


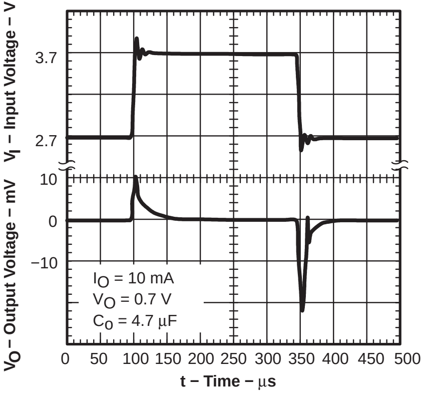
Figure 9

TYPICAL CHARACTERISTICS



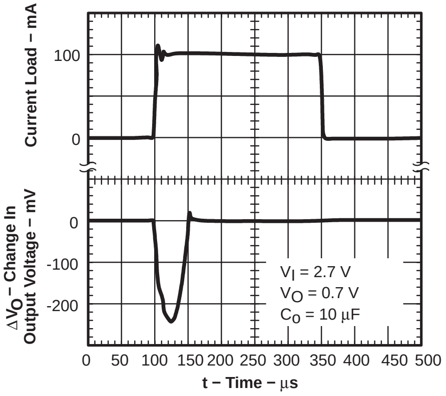
OUTPUT VOLTAGE AND ENABLE VOLTAGE vs TIME (START-UP)

Figure 10



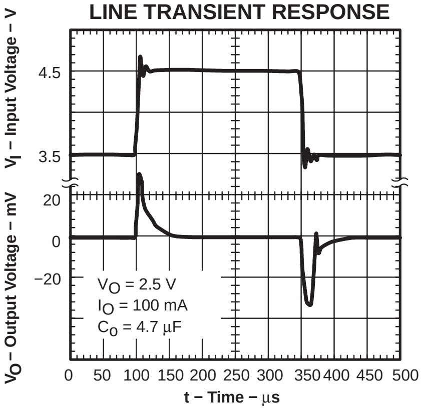
LINE TRANSIENT RESPONSE

Figure 11



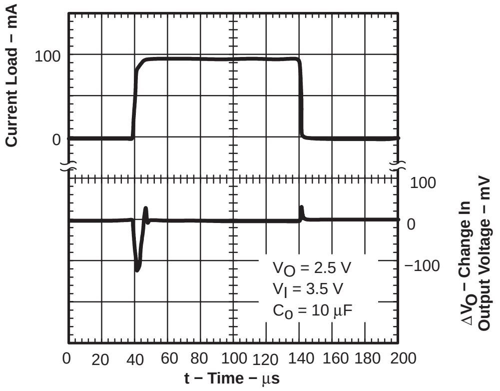
LOAD TRANSIENT RESPONSE

Figure 12



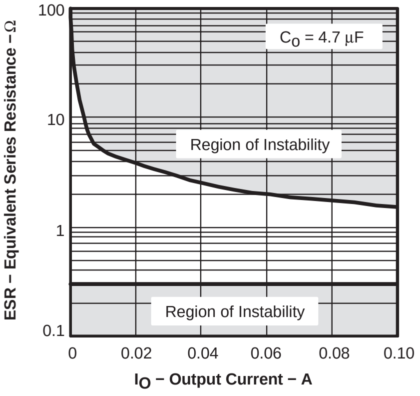
LINE TRANSIENT RESPONSE

Figure 13



LOAD TRANSIENT RESPONSE

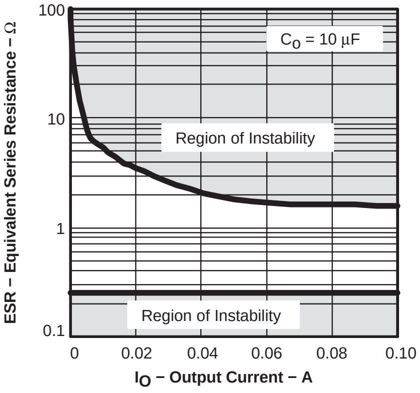
Figure 14



TYPICAL REGIONS OF STABILITY

EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

Figure 15



TYPICAL REGIONS OF STABILITY

EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

Figure 16

APPLICATION INFORMATION

The TPS76201 low-dropout (LDO) regulator has been optimized for use in battery-operated equipment including, but not limited to, the sub 1.2-V DSP core voltage supplies. It features low quiescent current (23 µA nominally) and enable inputs to reduce supply currents to 1 µA when the regulators are turned off.

A typical application circuit is shown in Figure 17.

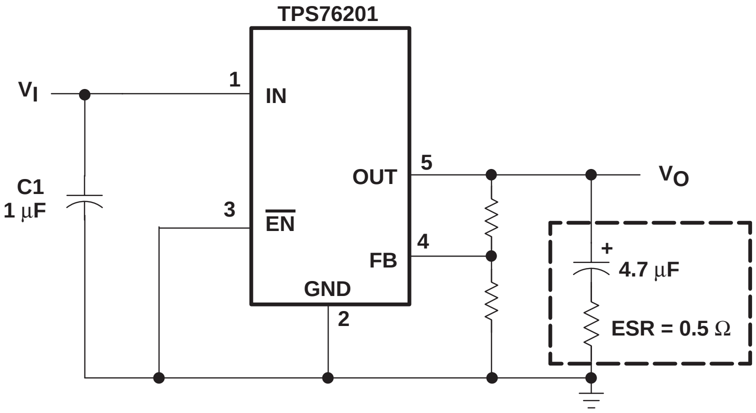


Figure 17. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS76201, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS76201 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 µF. The ESR (equivalent series resistance) of the capacitor should be between 0.3 Ω and 1.5 Ω. to ensure stability. Capacitor values larger than 4.7 µF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 µF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR[†]	SIZE (H × L × W)[‡]
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6.0 × 3.2

[†] ESR is maximum resistance in Ohms at 100 kHz and T_A = 25°C. Contact manufacturer for minimum ESR values.
[‡] Size is in mm.

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS76201 adjustable regulator is programmed using an external resistor divider as shown in Figure 18. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

V_{ref} = 0.6663 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 66.5 kΩ to set the divider current at 10 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)‡	
	R1	R2
0.7	3.36	66.5
0.9	23.2	66.5
1.2	53.6	66.5
1.5	83.5	66.5
1.8	113	66.5
2.5	182	66.5
3.3	246	66.5
3.6	294	66.5
4	332	66.5
5	432	66.5

‡ 1% values shown.

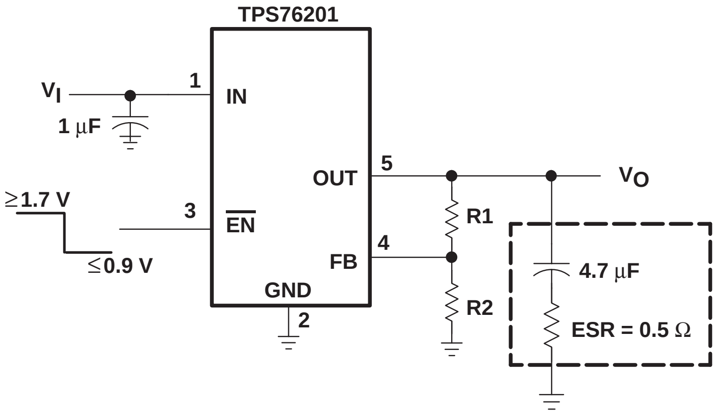


Figure 18. TPS76201 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

regulator protection

The TPS76201 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS76201 features internal current limiting and thermal protection. During normal operation, the TPS76201 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76201DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFUI
TPS76201DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFUI
TPS76201DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFUI
TPS76201DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFUI
TPS76201DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFUI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS76201 :

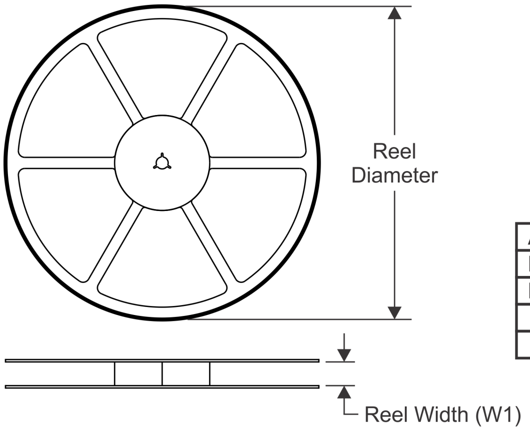
- Automotive : TPS76201-Q1

NOTE: Qualified Version Definitions:

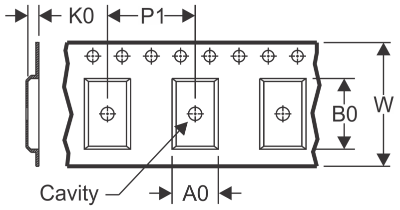
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

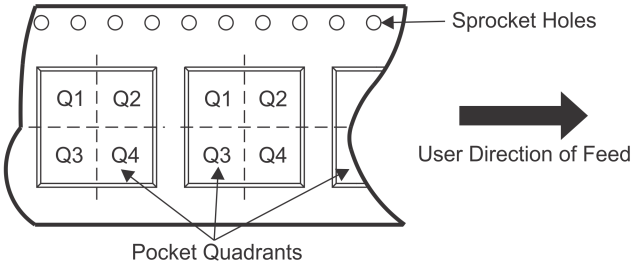


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

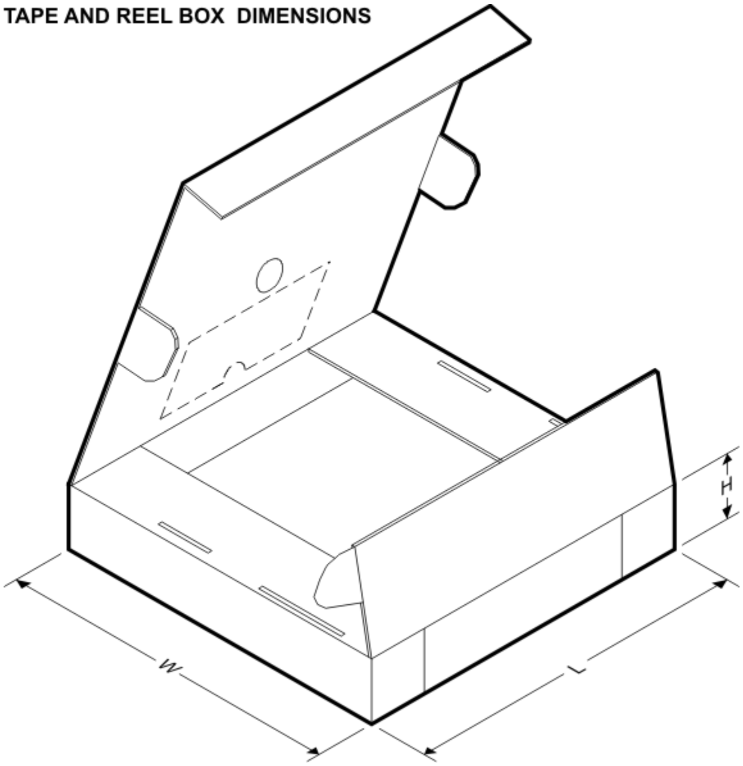
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

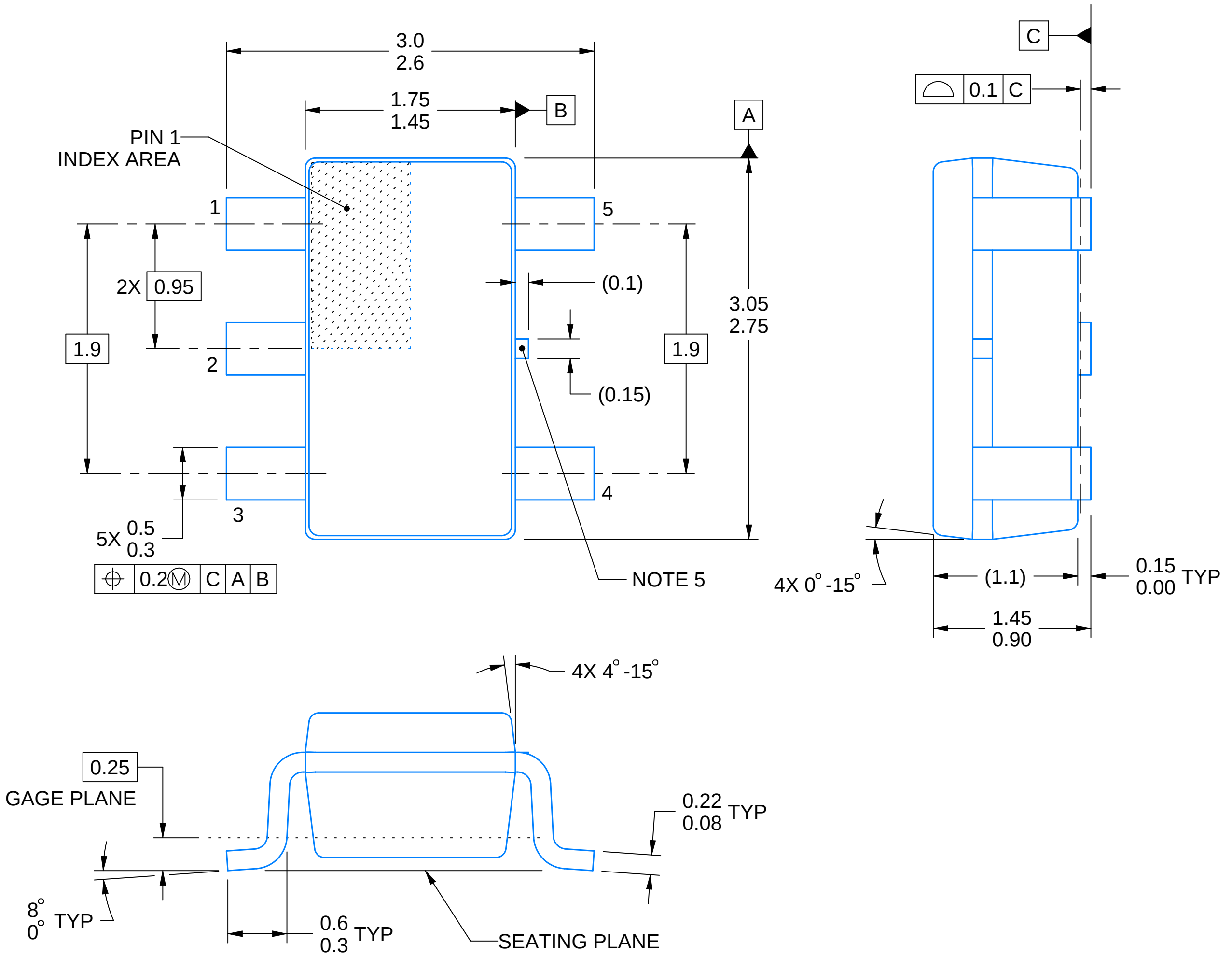
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76201DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76201DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



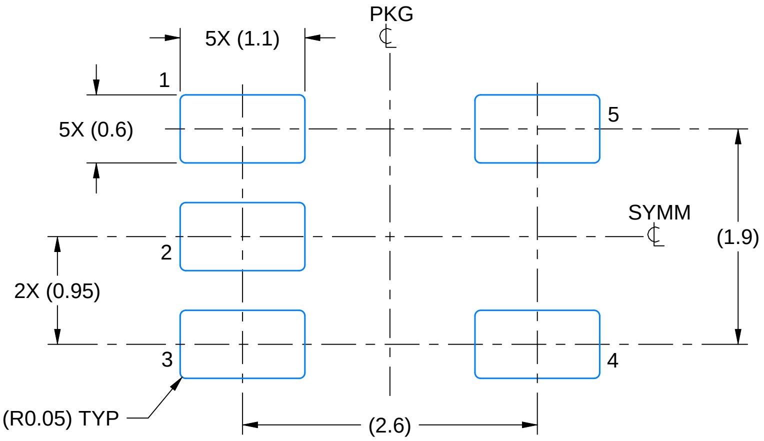
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76201DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76201DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

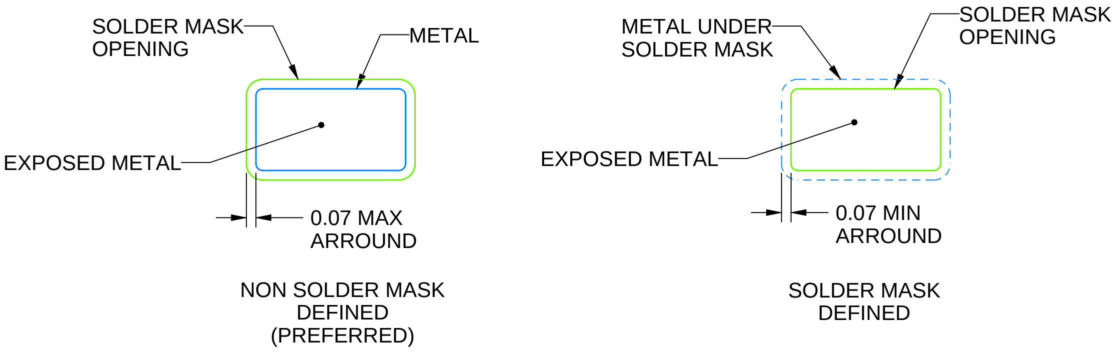


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



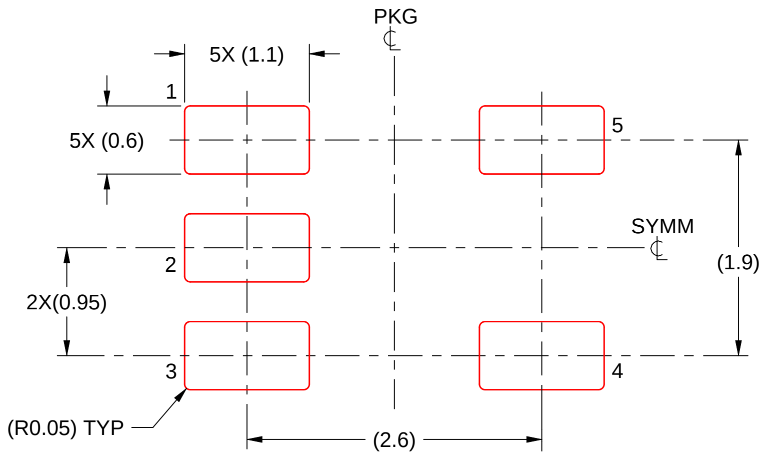
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated