SLVS242C–MARCH 2000–REVISED OCTOBER 2007

TPS752xxQ with $\overline{\text{RESET}}$ Output, TPS754xxQ with Power Good Output FAST-TRANSIENT-RESPONSE 2-A LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

- **2-A Low-Dropout Voltage Regulator**
- **Available in 1.5 V, 1.8 V, 2.5 V, 3.3 V Fixed Output and Adjustable Versions**
- **Open Drain Power-On Reset With 100ms Delay (TPS752xxQ)**
- **Open Drain Power-Good (PG) Status Output (TPS754xxQ)**
- **Dropout Voltage Typically 210 mV at 2 A (TPS75233Q)**
- **Ultralow 75-µA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **20-Pin TSSOP PowerPAD™ (PWP) Package**
- **Thermal Shutdown Protection**

APPLICATIONS

- **Telecom**
- **Servers**
- **DSP, FPGA Supplies**

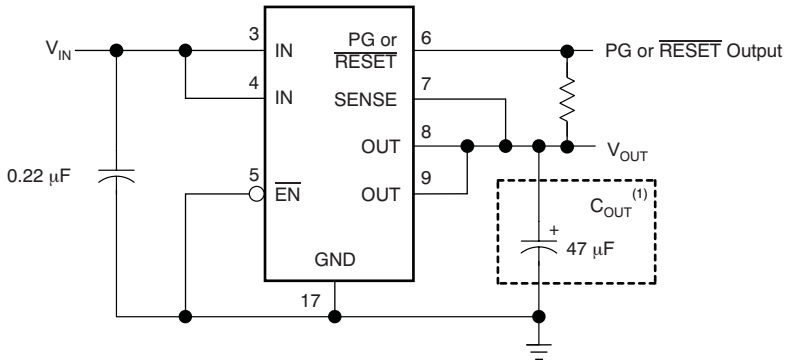
DESCRIPTION

The TPS752xxQ and TPS754xxQ devices are low-dropout regulators with integrated power-on reset and power-good (PG) functions respectively. These devices are capable of supplying 2 A of output current with a dropout of 210 mV (TPS75233Q, TPS75433Q). Quiescent current is 75 µA at full load and drops down to 1 µA when the device is disabled. These devices are designed to have fast transient response for larger load current changes.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 210 mV at an output current of 2 A for the TPS75x33Q) and is directly proportional to the output current. Additionally, because the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 75 µA over the full range of output current, 1 mA to 2 A). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when $\overline{\text{EN}}$ is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 µA at T_J = +25°C.

Typical Application Circuit (Fixed Voltage Options)



(1) See *Application Information* for capacitor selection details.

DESCRIPTION, CONTINUED

The $\overline{\text{RESET}}$ (SVS, POR, or power on reset) output of the TPS752xxQ initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS752xxQ monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When the output reaches 95% of its regulated voltage, $\overline{\text{RESET}}$ goes to a high-impedance state after a 100-ms delay. $\overline{\text{RESET}}$ goes to a logic-low state when the regulated output voltage is pulled below 95% (that is, during an overload condition) of its regulated voltage.

The TPS754xxQ has a power good terminal (PG) as an active high, open drain output for use with a power-on reset or a low-battery indicator.

The TPS754xxQ and TPS752xxQ are offered in 1.5 V, 1.8 V, 2.5 V and 3.3 V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS754xxQ and TPS752xxQ families are available in a 20-pin TSSOP (PWP) package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS752**xxyyyz**, TPS754**xxyyyz**	**XX** is nominal output voltage (for example, 15 = 1.5 V, 01 = Adjustable(3)). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Custom fixed output voltages are available; minimum order quantities may apply. Contact factory for details and availability.
(3) The TPS75x01 is programmable using an external resistor divider (see *Application Information*).

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

PARAMETER	TPS752xxQ, TPS754xxQ	UNIT
Input voltage range, V_{IN}(2)	–0.3 to +6	V
Voltage range at $\overline{\text{EN}}$	–0.3 to +16.5	V
Maximum $\overline{\text{RESET}}$ voltage (TPS752xxQ)	16.5	V
Maximum PG voltage (TPS754xxQ)	16.5	V
Peak output current	Internally limited	
Output voltage range at OUT, FB	5.5	V
Continuous total power dissipation	See Dissipation Ratings Table	
Operating virtual junction temperature range, T_J	–40 to +125	°C
Storage junction temperature range , T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV

(1) Stresses above these ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to network terminal ground.

DISSIPATION RATINGS

BOARD	PACKAGE	AIRFLOW (CFM)	T_A < +25°C	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C	T_A = +85°C
Low-K(1)	PWP	0	2.9 mW	23.5 mW/°C	1.9 W	1.5 W
		300	4.3 mW	34.6 mW/°C	2.8 W	2.2 W
High-K(2)	PWP	0	3 W	23.8 mW/°C	1.9 W	1.5 W
		300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer, 5-in ɹ5-in printed circuit board (PCB), 1-ounce copper, 2-in ɹ2-in coverage (4 in^2).
(2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer, 1.5-in ɹ2-in PCB, 1-ounce copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	MAX
V_{IN}	Input voltage range(1)	2.7	5.5	V
V_{OUT}	Output voltage range	1.5	5	V
I_{OUT}	Output current	0	2.0	A
T_J	Operating virtual junction temperature	–40	+125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{IN(min)} = V_{OUT(max)} + V_{DO(max\ load)}$.

ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 1 V; I_{OUT} = 1 mA, $V_{\overline{EN}}$ = 0 V, C_{OUT} = 47 µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	TPS752xxQ, TPS754xxQ MIN	TYP	MAX	UNIT
V_{OUT}[1]	Adjustable output		1.5 V ≤ V_{OUT} ≤ 5.5 V	0.98V_{OUT}	V_{OUT}	1.02V_{OUT}	V
	1.5 V output		2.7 V < V_{IN} < 5.5 V	1.470	1.5	1.530	
	1.8 V output		2.8 V < V_{IN} < 5.5 V	1.764	1.8	1.836	
	2.5 V output		3.5 V < V_{IN} < 5.5 V	2.450	2.5	2.550	
	3.3 V output		4.3 V < V_{IN} < 5.5 V	3.234	3.3	3.336	
I_{GND}[2]	Ground pin current		I_{OUT} = 1 mA to 2 A		75	125	µA
ΔV_{OUT}%/ V_{OUT}[1],[2]	Output voltage line regulation		V_{OUT} + 1 V < V_{IN} ≤ 5 V		0.01	0.1	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation		I_{OUT} = 1 mA to 2 A		1		mV
V_N	Output noise voltage BW = 300 Hz to 50 kHz		V_{OUT} = 1.5 V, C_{OUT} = 100 µF		60		μV_{RMS}
V_{DO}	Dropout voltage[3]	TPS75433Q TPS75233Q	I_{OUT} = 2 A, V_{IN} = 3.2 V		210	400	mV
I_{CL}	Output current limit		V_{OUT} = 0 V		3.3	4.5	A
T_{SD}	Shutdown temperature				+150		°C
I_{STBY}	Standby current		$\overline{EN}$ = V_{IN}		1	10	µA
I_{FB}	FB input current	TPS75x01Q	FB = 1.5 V	–1		1	µA
$V_{EN(HI)}$	High-level enable input voltage			2			V
$V_{EN(LO)}$	Low-level enable input voltage					0.7	V
PSRR	Power-supply ripple rejection[2]		f = 100 Hz, C_{OUT} = 100 µF, I_{OUT} = 2 A, See [1]		60		dB
RESET (TPS752xxQ)	Minimum input voltage for valid $\overline{RESET}$		$I_{OUT(\overline{RESET})}$ = 300 µA, $V_{(\overline{RESET})}$ ≤ 0.8 V		1	1.3	V
	Trip threshold voltage		V_{OUT} decreasing	92		98	%V_{OUT}
	Hysteresis voltage		Measured at V_{OUT}		0.5		%V_{OUT}
	Output low voltage		V_{IN} = 2.7 V, $I_{OUT(\overline{RESET})}$ = 1 mA		0.15	0.4	V
	Leakage current		$V_{(\overline{RESET})}$ = 5.5 V			1	µA
	RESET timeout delay				100		ms
PG (TPS754xxQ)	Minimum input voltage for valid PG		$I_{OUT(PG)}$ = 300 µA, $V_{(PG)}$ ≤ 0.8 V		1.1	1.3	V
	Trip threshold voltage		V_{OUT} decreasing	80		86	%V_{OUT}
	Hysteresis voltage		Measured at V_{OUT}		0.5		%V_{OUT}
	Output low voltage		$I_{OUT(PG)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5.5 V			1	µA
	Input current ($\overline{EN}$)		$\overline{EN}$ = V_{IN}	–1		1	µA
			$\overline{EN}$ = 0 V	–1	0	1	

(1) Minimum V_{IN} = (V_{OUT} + 1 V) or 2.7 V, whichever is greater. Maximum V_{IN} = 5.5 V.
(2) If V_{OUT} ≤ 1.8 V, then $V_{IN(min)}$ = 2.7 V, $V_{IN(max)}$ = 5.5 V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_{OUT}(V_{IN(Max)} - 2.7V)}{100} \times 1000$$

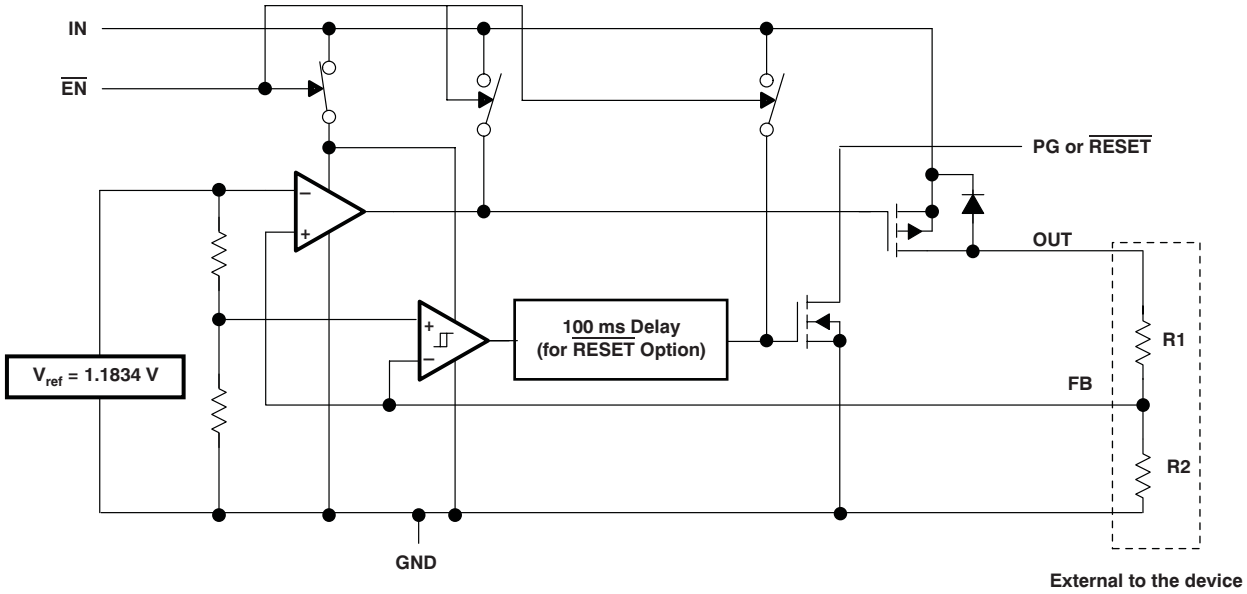
If V_{OUT} ≥ 2.5 V, then $V_{IN(min)}$ = V_{OUT} + 1 V, $V_{IN(max)}$ = 5.5 V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_{OUT}[V_{IN(Max)} - (V_{OUT} + 1V)]}{100} \times 1000$$

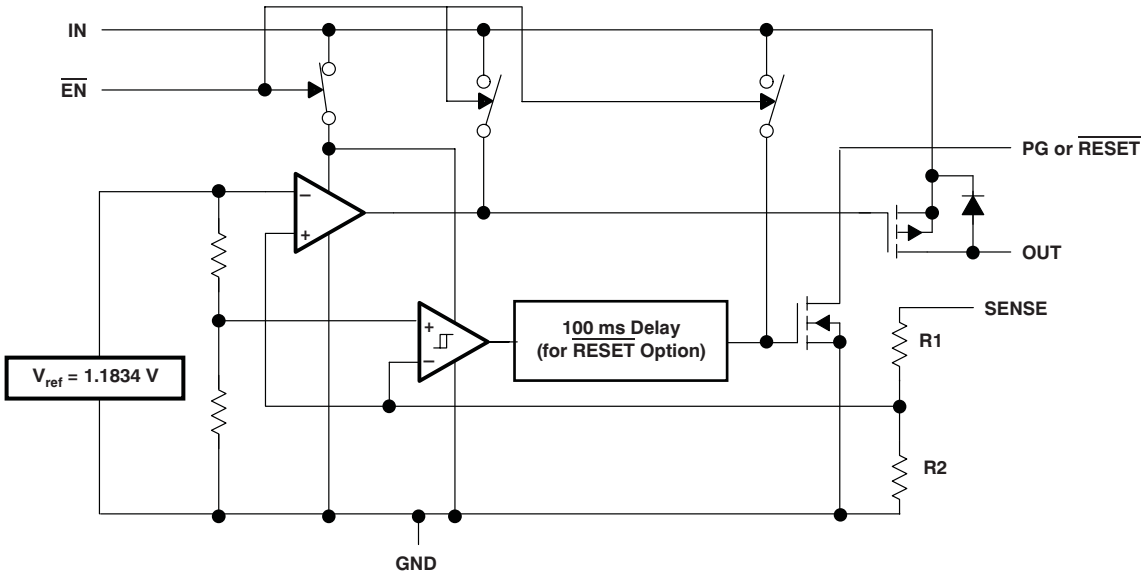
(3) Input voltage equals $V_{OUT(Typ)}$ – 100 mV; TPS75x33Q input voltage must drop to 3.2 V for this test.

FUNCTIONAL BLOCK DIAGRAMS

Adjustable Voltage Versions



Fixed-Voltage Versions



PIN CONFIGURATIONS

TSSOP-20
PWP
(TOP VIEW)

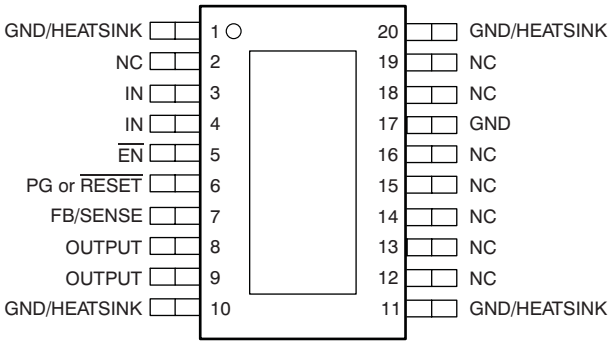
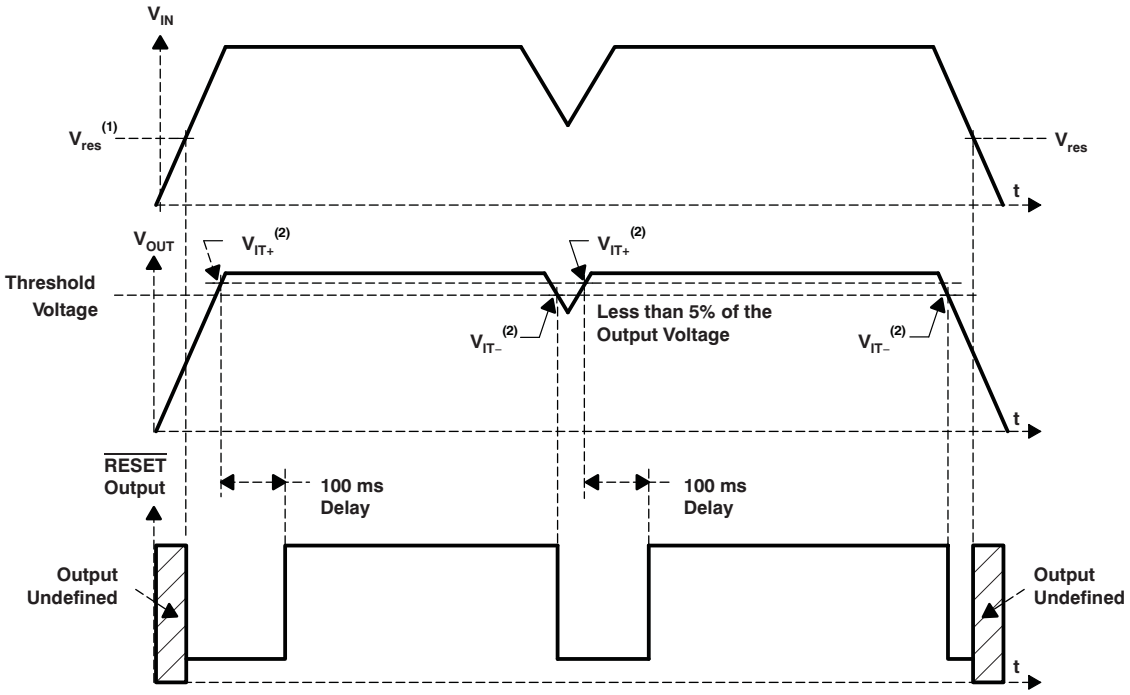


Table 1. PIN DESCRIPTIONS

TPS754xxQ, TPS752xxQ			
NAME	**TSSOP-20 (PWP) PIN NO.**	**I/O**	**DESCRIPTION**
$\overline{\text{EN}}$	5	I	Negative polarity enable ($\overline{\text{EN}}$) input
FB/SENSE	7	I	Adjustable voltage version only; feedback voltage for setting output voltage of the device. Not internally connected on adjustable versions. Sense input for fixed options.
GND	17		Ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12, 13, 14, 15, 16, 18, 19		Not connected
OUTPUT	8, 9	O	Regulated output voltage
$\overline{\text{RESET}}$/PG	6	O	TPS752xxQ devices only; open-drain $\overline{\text{RESET}}$ output.
			TPS754xxQ devices only; open-drain power-good (PG) output.

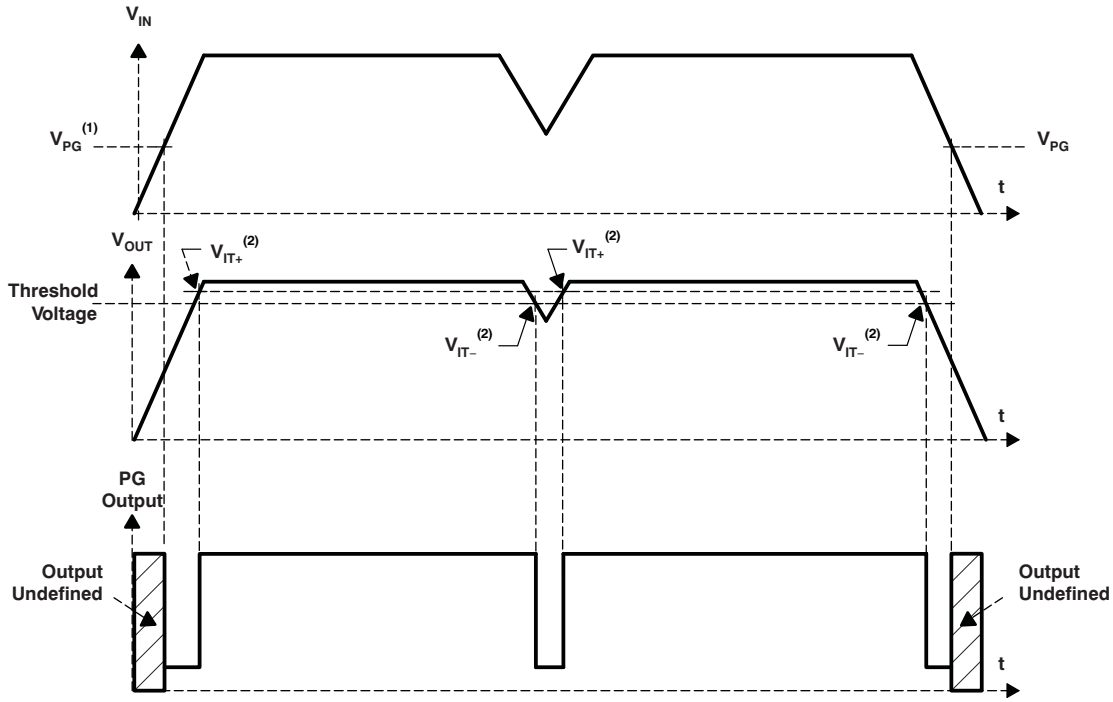
TPS752xxQ $\overline{\text{RESET}}$ Timing Diagram



(1) V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT}: Trip voltage is typically 5% lower than the output voltage (95% V_{OUT}). V_{IT-} to V_{IT+} is the hysteresis voltage.

TPS754xxQ Power Good Timing Diagram



(1) V_{PG} is the minimum input voltage for a valid Power Good. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT}: Trip voltage is typically 17% lower than the output voltage (83% V_{OUT}). V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE NO.
V_{OUT}	Output Voltage	vs Output Current	Figure 3, Figure 4
		vs Junction Temperature	Figure 5, Figure 6
		vs Time	Figure 18
I_{GND}	Ground Current	vs Junction Temperature	Figure 7
PSRR	Power-Supply Ripple Rejection	vs Frequency	Figure 8
	Output Spectral Noise Density	vs Frequency	Figure 9
Z_{OUT}	Output Impedance	vs Frequency	Figure 10
V_{DO}	Dropout Voltage	vs Input Voltage	Figure 11
		vs Junction Temperature	Figure 12
V_{IN}	Input Voltage (Min)	vs Output Voltage	Figure 13
LINE	Line Transient Response		Figure 14, Figure 16
LOAD	Load Transient Response		Figure 15, Figure 17
ESR	Equivalent Series Resistance	vs Output Current	Figure 20, Figure 21

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

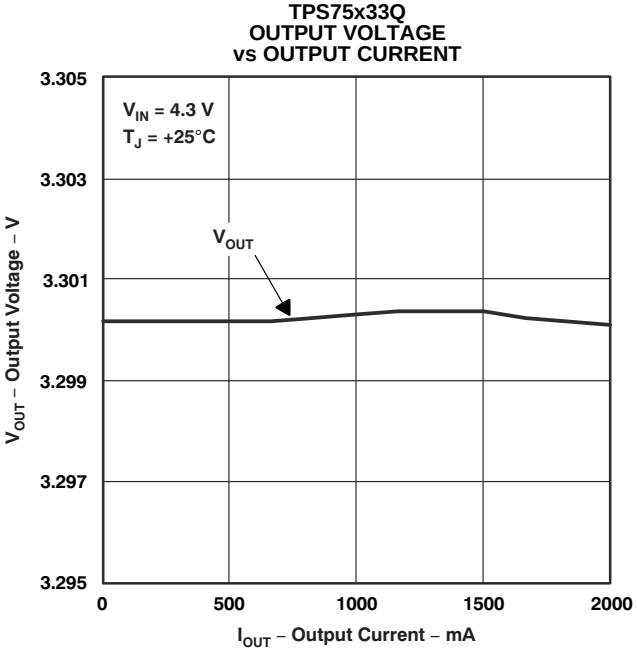


Figure 3.

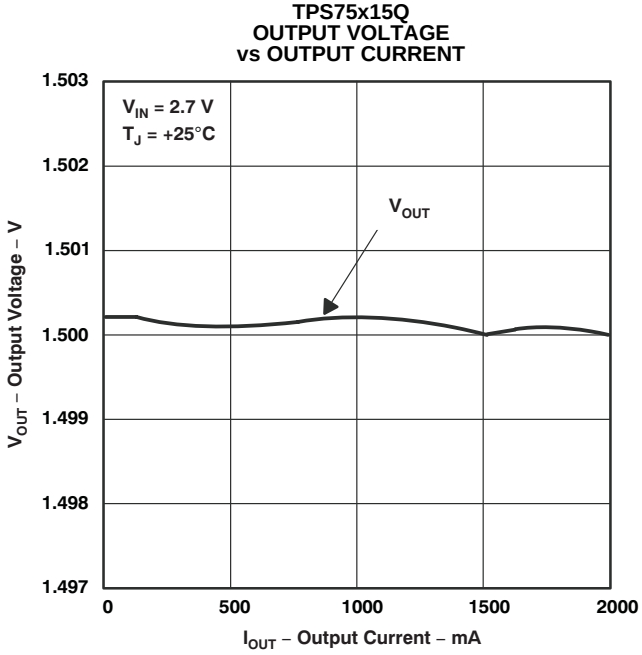


Figure 4.

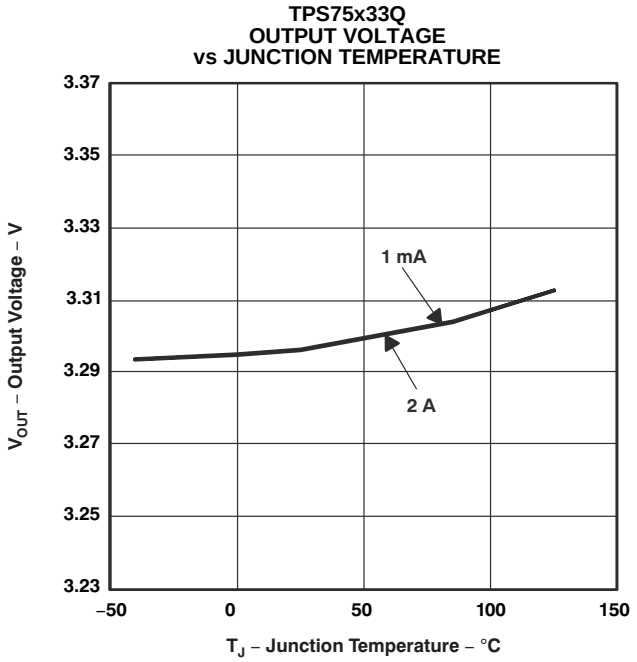


Figure 5.

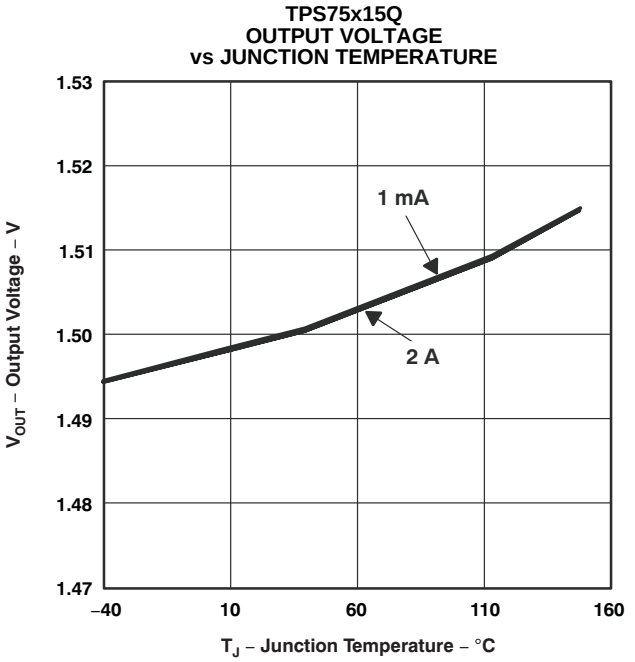


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

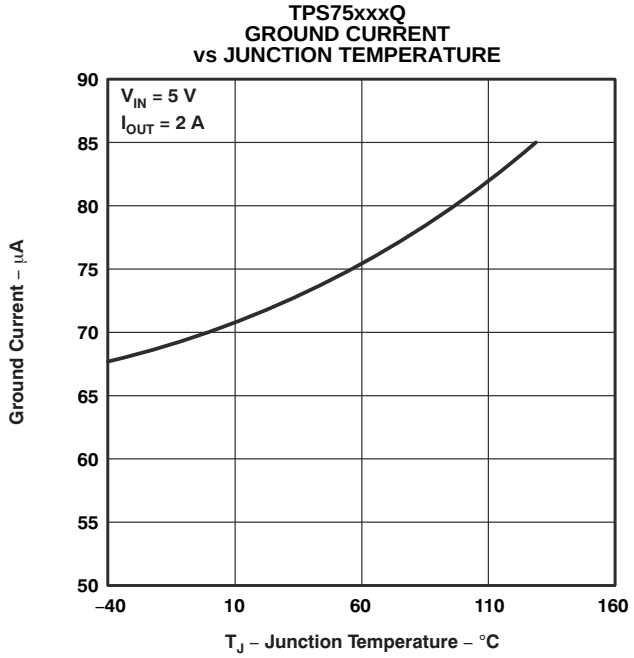


Figure 7.

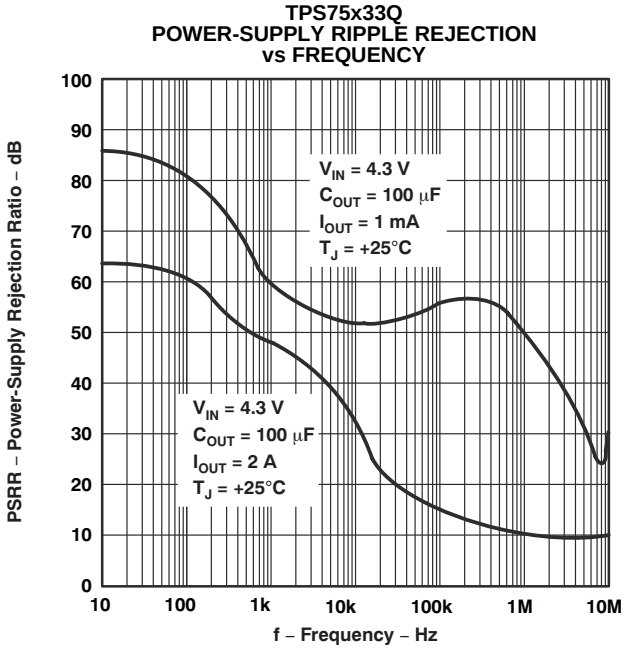


Figure 8.

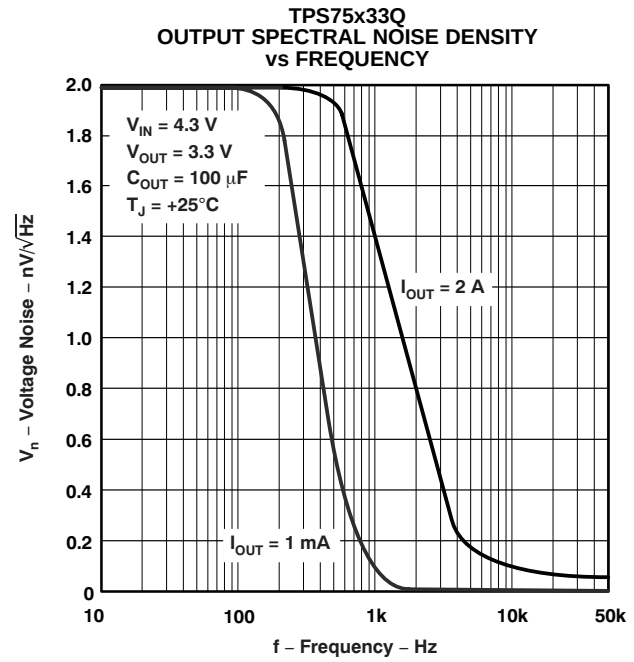


Figure 9.

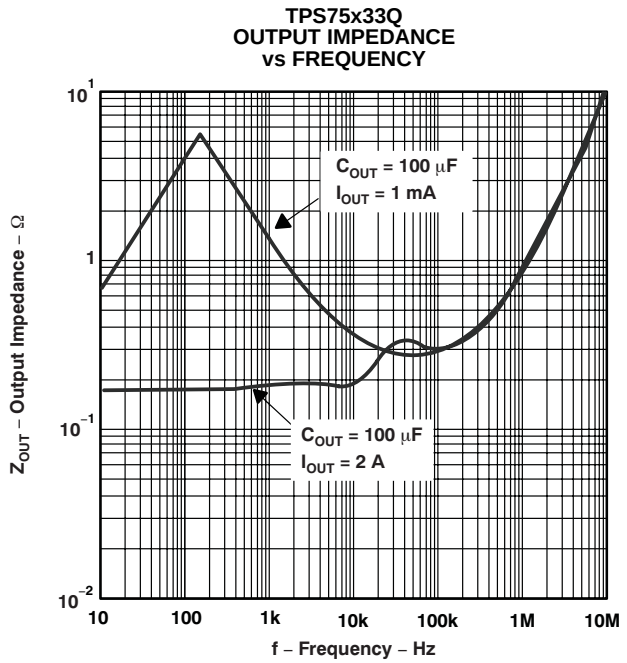


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

TPS75x01Q
DROPOUT VOLTAGE
vs INPUT VOLTAGE

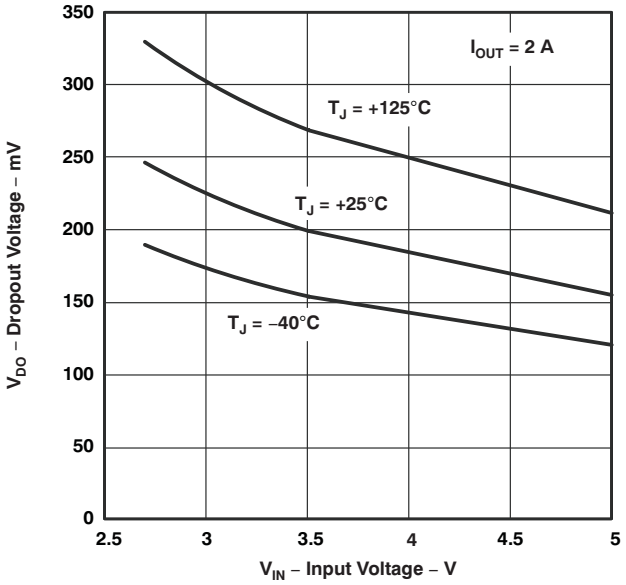


Figure 11.

TPS75x33Q
DROPOUT VOLTAGE
vs JUNCTION TEMPERATURE

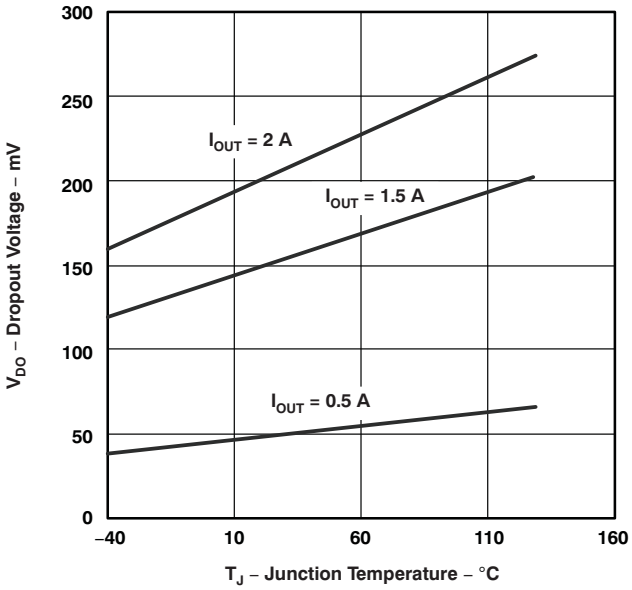


Figure 12.

INPUT VOLTAGE (MIN)
vs OUTPUT VOLTAGE

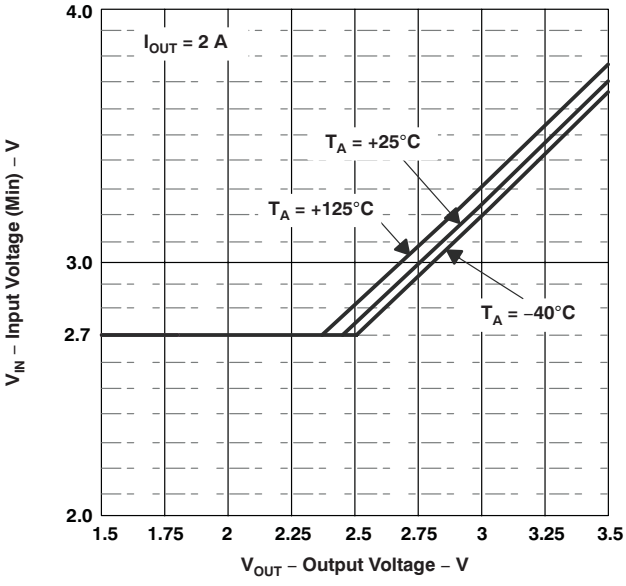


Figure 13.

TPS75x15Q
LINE TRANSIENT RESPONSE

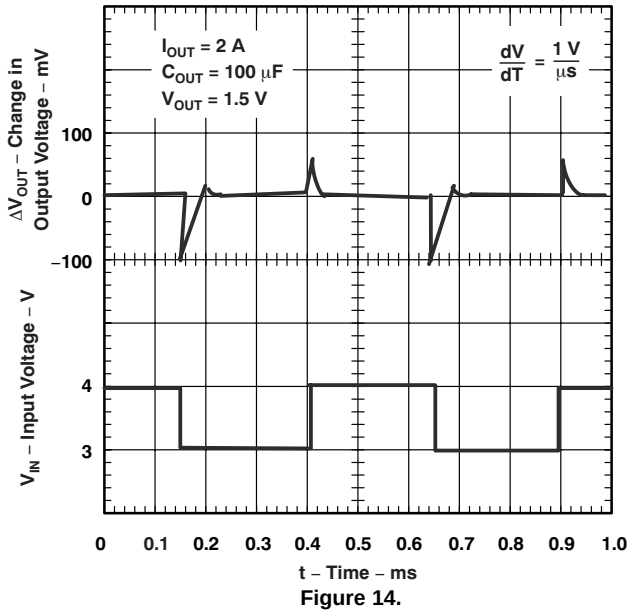


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

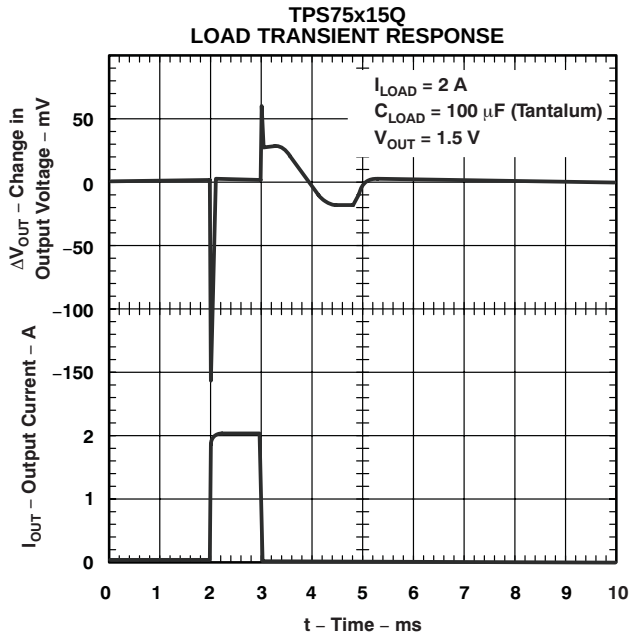


Figure 15.

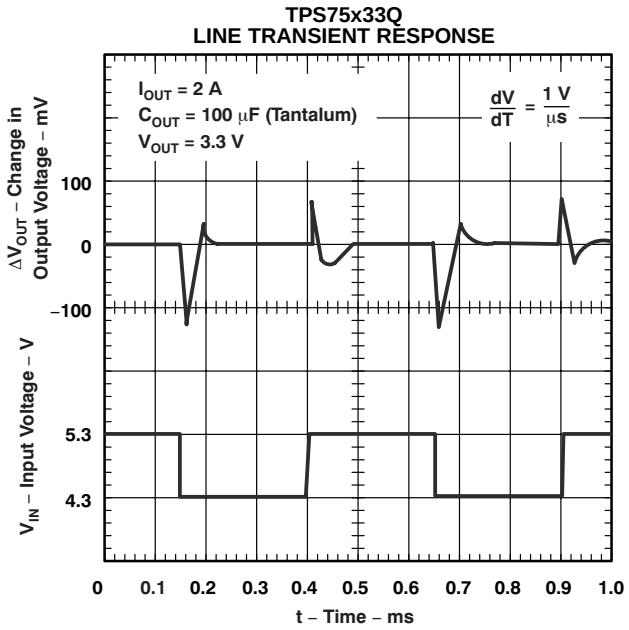


Figure 16.

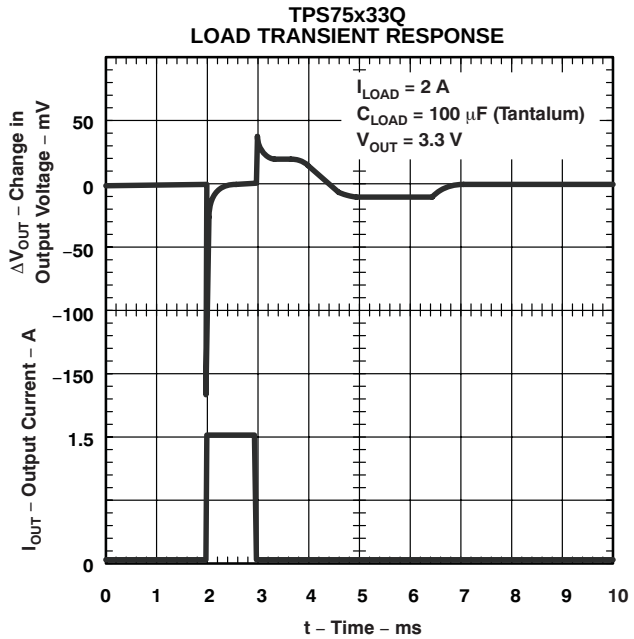


Figure 17.

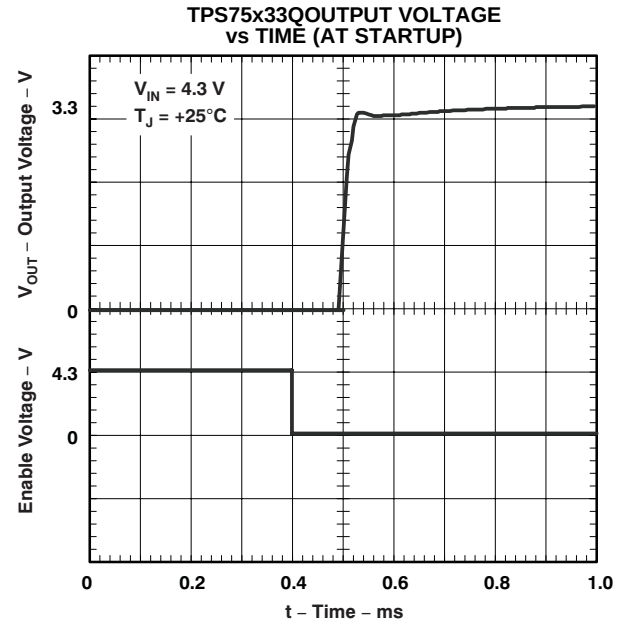


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

Test Circuit for Typical Regions of Stability (Figure 20 and Figure 21) (Fixed Output Options)

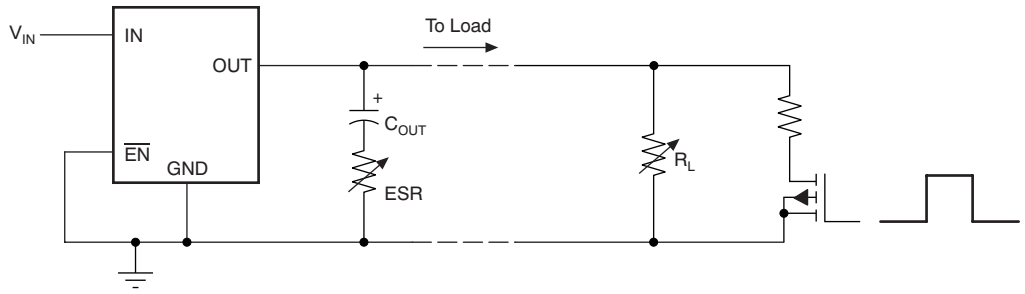


Figure 19.

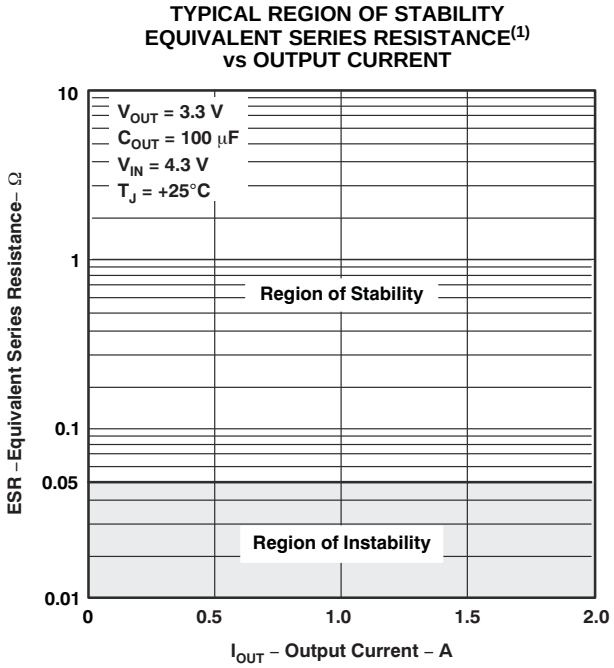


Figure 20.

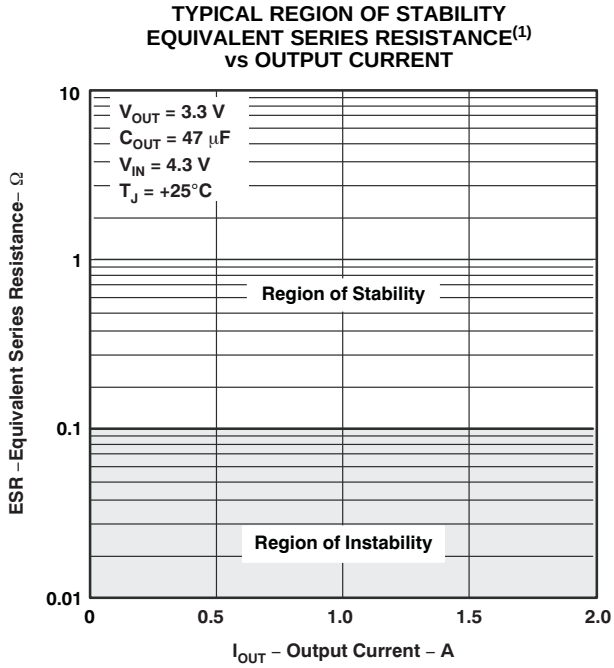


Figure 21.

(1). Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_{OUT}.

APPLICATION INFORMATION

The TPS752xxQ and TPS754xxQ devices include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V and 3.3 V), and an adjustable regulator, the TPS75x01Q (adjustable from 1.5 V to 5 V).

Minimum Load Requirements

The TPS752xxQ and TPS754xxQ families are stable even at zero load; no minimum load is required for operation.

Pin Functions

Enable ($\overline{EN}$)

The $\overline{EN}$ terminal is an input that enables or shuts down the device. If $\overline{EN}$ is a logic high, the device is in shutdown mode. When $\overline{EN}$ goes to logic low, then the device is enabled.

Power-Good (PG)—TPS754xxQ

The PG terminal is an open drain, active high output that indicates the status of V_{OUT} (output of the LDO). When V_{OUT} reaches 83% of the regulated voltage, PG goes to a high impedance state. It goes to a low-impedance state when V_{OUT} falls below 83% (that is, an overload condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

Sense (SENSE)

The SENSE terminal of the fixed output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_{OUT} to filter noise is not recommended because these types of networks may cause the regulator to oscillate.

Feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_{OUT} to filter noise is not recommended because these types of networks may cause the regulator to oscillate.

Reset ($\overline{RESET}$)—TPS752xxQ

The $\overline{RESET}$ terminal is an open drain, active low output that indicates the status of V_{OUT}. When V_{OUT} reaches 95% of the regulated voltage, $\overline{RESET}$ goes to a high-impedance state after a 100-ms delay. $\overline{RESET}$ goes to a low-impedance state when V_{OUT} is below 95% of the regulated voltage. The open-drain output of the $\overline{RESET}$ terminal requires a pullup resistor.

GND/HEATSINK

All GND/HEATSINK terminals are connected directly to the mount pad for thermal-enhanced operation. These terminals could be connected to GND or left floating.

Input Capacitor

For a typical application, an input bypass capacitor (0.22 µF to 1 µF) is recommended for device stability. This capacitor should be as close to the input pins as possible. For fast transient conditions where droop at the input of the LDO may occur because of high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor depends on the output current and response time of the main power supply, as well as the distance to the load (LDO).

Output Capacitor

As with most LDO regulators, the TPS752xxQ and TPS754xxQ require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 µF and the ESR (equivalent series resistance) must be between 100 mΩ and 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information, along with the ESR graphs (see Figure 20 and Figure 21), is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 22.

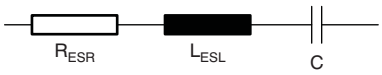


Figure 22. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR..

Figure 23 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

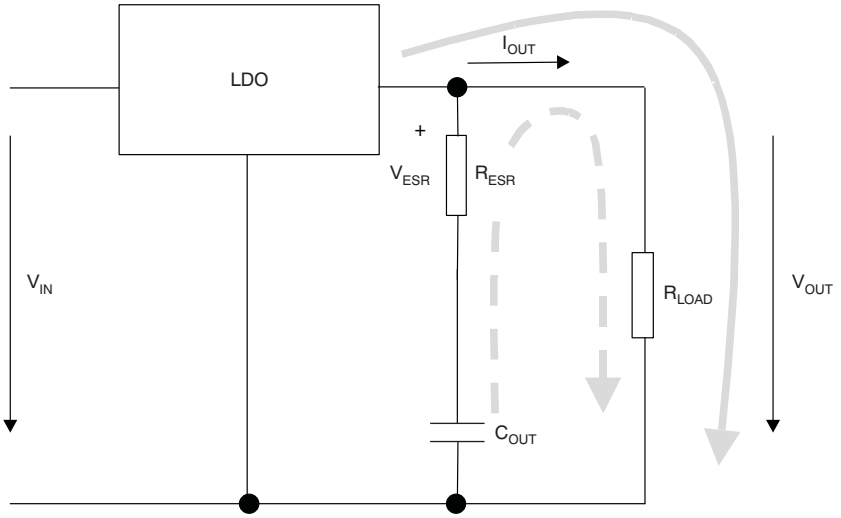


Figure 23. LDO Output Stage With Parasitic Resistances ESR and ESL

In steady state operation (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_{OUT}) = V_{OUT}$). This condition means that no current is flowing into the C_{OUT} branch. If I_{OUT} suddenly increases (that is, a transient condition), the following events occur:

- The LDO is not able to supply the sudden current need because of its response time (t_1 in Figure 24). Therefore, capacitor C_{OUT} provides the current for the new load condition (the dashed arrow). C_{OUT} now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at R_{ESR}. This voltage is shown as V_{ESR} in Figure 23.
- When C_{OUT} is conducting current to the load, initial voltage at the load is $V_{OUT} = V(C_{OUT}) – V_{ESR}$. As a result of the discharge of C_{OUT}, the output voltage V_{OUT} drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 24.

Figure 24 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From the above discussion, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

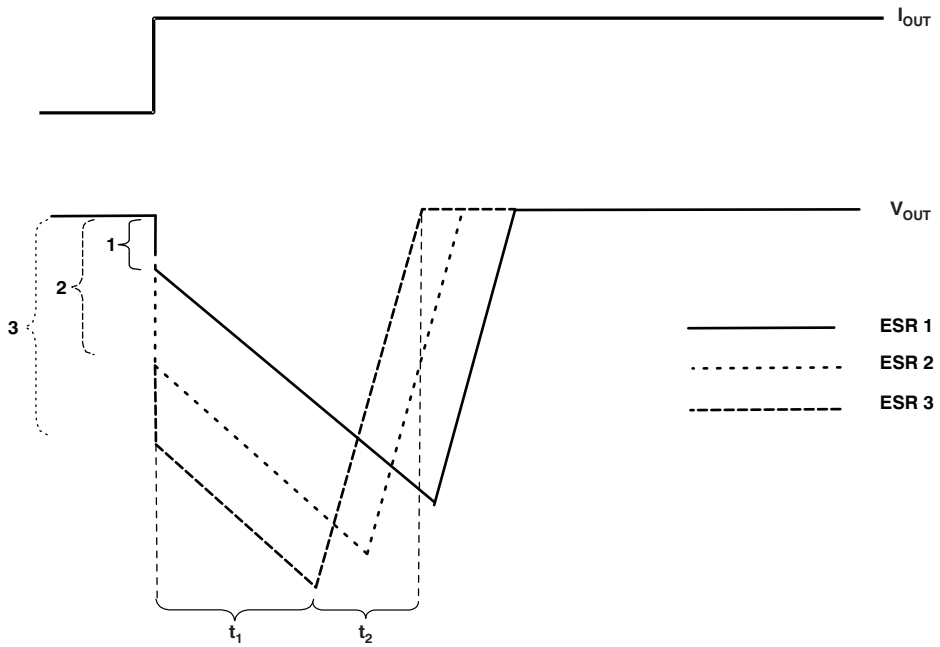


Figure 24. Correlation of Different ESRs and Their Influence to the Regulation of V_{OUT} at a Load Step From Low-to-High Output Current

Programming the TPS75x01Q Adjustable LDO Regulator

The output voltage of the TPS77x01Q adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1:

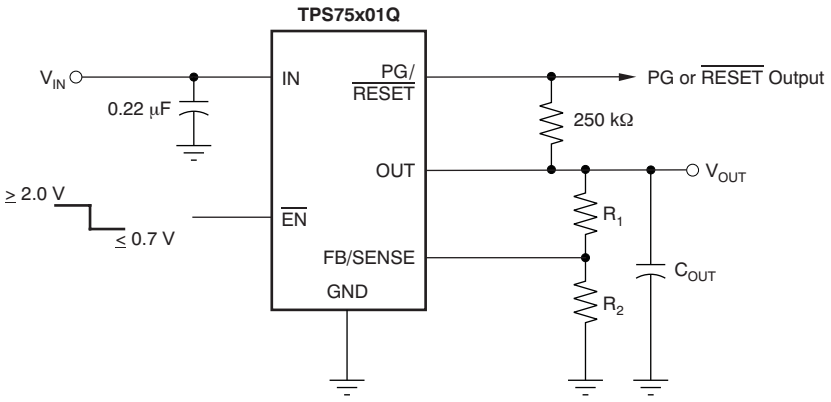
$$V_{OUT} = V_{ref} \times (1 + \frac{R_1}{R_2}) \quad (1)$$

Where:

- V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40µA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at approximately 40µA and then calculate R_1 using Equation 2:

$$R_1 = (\frac{V_{OUT}}{V_{ref}} - 1) \times R_2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ

NOTE: To reduce noise and prevent oscillation, R_1 and R_2 must be as close as possible to the FB/SENSE terminal.

Figure 25. TPS75x01Q Adjustable LDO Regulator Programming

Regulator Protection

The TPS752xxQ and TPS754xxQ PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS752xxQ and TPS754xxQ also feature internal current limiting and thermal protection. During normal operation, the TPS752xxQ and TPS754xxQ limit output current to approximately 3.3 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3:

$$P_{D(Max)} = \frac{T_{J(Max)} - T_A}{R_{\theta JA}} \quad (3)$$

where:

- $T_{J(max)}$ is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; that is, 34.6°C/W for the 20-terminal PWP with no airflow (see Dissipation Ratings Table).
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

THERMAL INFORMATION

Thermally-Enhanced TSSOP-20 (PWP–PowerPAD)

The thermally-enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 26(c)] to provide an effective thermal contact between the IC and the printed wiring board (PWB).

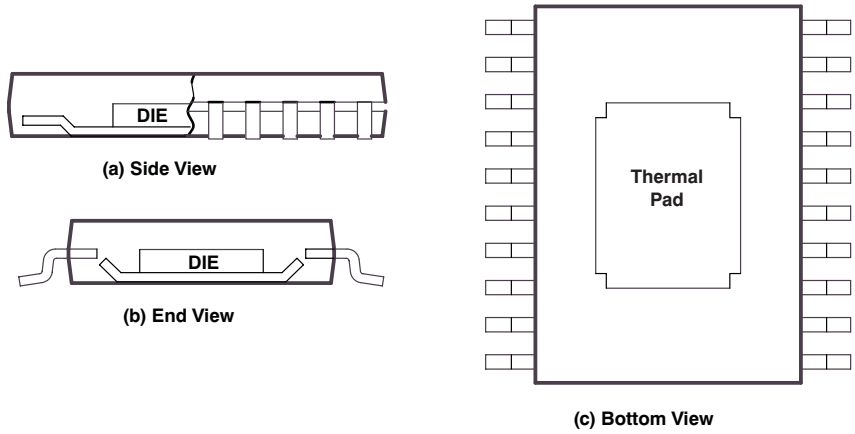


Figure 26. Views of Thermally-Enhanced PWP Package

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (less than 2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (a thermally-enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heatsink surface) that is coupled to the thermal pad enables the PWP package to dissipate 2.5 W in free air (see Figure 28(a), 8 cm^2 of copper heatsink and natural convection). Increasing the heatsink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 27 and Figure 28). The line drawn at 0.3 cm^2 in Figure 27 and Figure 28 indicates performance at the minimum recommended heatsink size, illustrated in Figure 30.

The thermal pad is directly connected to the substrate of the IC, which for the TPS752xxQPWP and TPS754xxQPWP series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 16 independent leads that can be used as inputs and outputs. (Note: leads 1, 10, 11, and 20 are internally connected to the thermal pad and the IC substrate.)

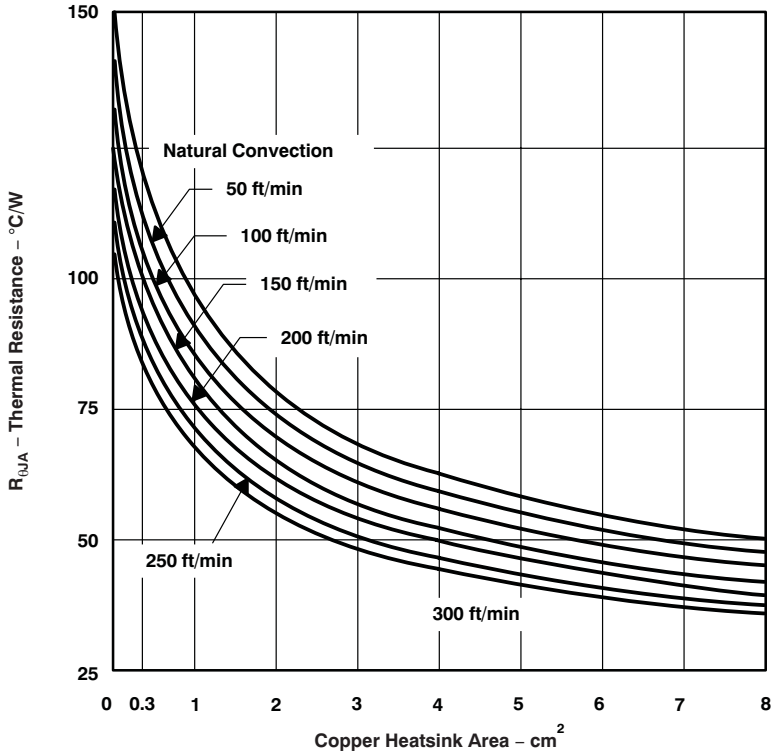


Figure 27. Thermal Resistance vs Copper Heatsink Area

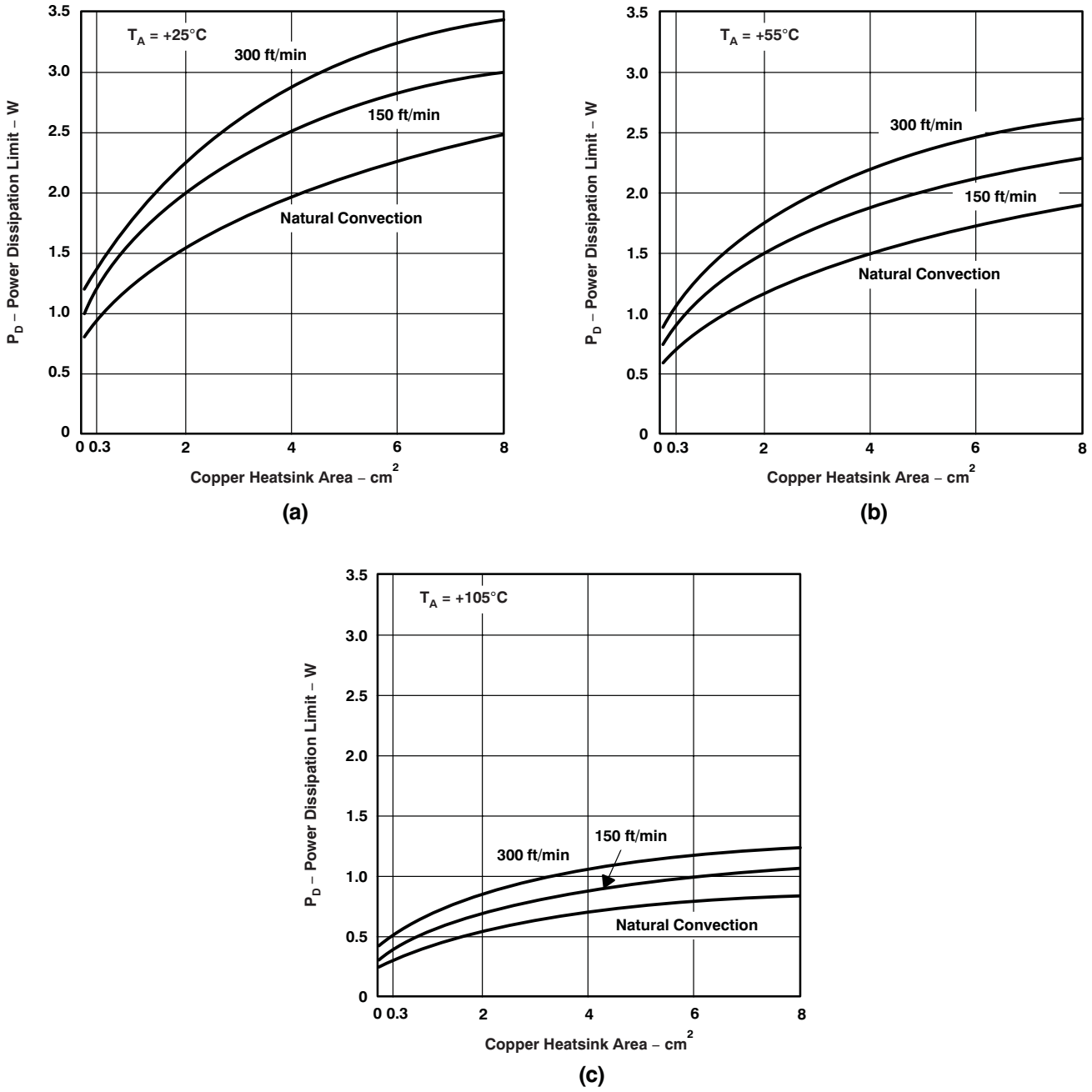
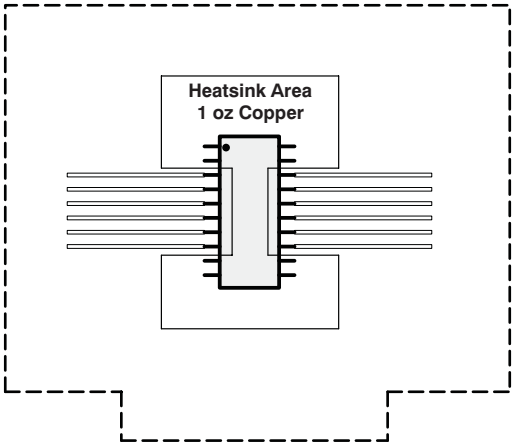


Figure 28. Power Ratings of the PWP Package at Ambient Temperatures of +25°C, +55°C, and +105°C

Figure 29 is an example of a thermally-enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 27 and Figure 28. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 27 as a function of heatsink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils (0.15748 cm)
Board size	3.2 in. x 3.2 in.
Board material	FR4
Copper trace/heatsink	1 oz
Exposed pad mounting	63/67 tin/lead (Sn/Pb) solder

Figure 29. PWB Layout (Including Copper Heatsink Area) for Thermally-Enhanced PWP Package

From Figure 27, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(Max)} = \frac{T_{J(Max)} - T_A}{R_{\theta JA\ (System)}} \tag{5}$$

Where T_{Jmax} is the maximum specified junction temperature (+150°C absolute maximum limit, +125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS75433QPWP regulator. The equation for calculating total internal power dissipation of the TPS75433QPWP is:

$$P_{D(total)} = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q \tag{6}$$

Because the quiescent current of the TPS75433QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

For the case where T_A = +55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 27, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(Max)} = \frac{T_{J(Max)} - T_A}{R_{\theta JA\ (System)}} = \frac{125°C - 55°C}{50°C/W} = 1.4\ W \tag{8}$$

If the system implements a TPS75433QPWP regulator, where V_{IN} = 5 V and I_{OUT} = 800 mA, the internal power dissipation is:

$$P_{D(total)} = (V_{IN} - V_{OUT}) \times I_{OUT} = (5 - 3.3) \times 0.8 = 1.36\ W \tag{9}$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: either raise the power-dissipation limit by increasing the airflow or the heat-sink area, or loweri the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

Mounting Information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figure 27 and Figure 28 are for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 30 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 10, 11, and 20.

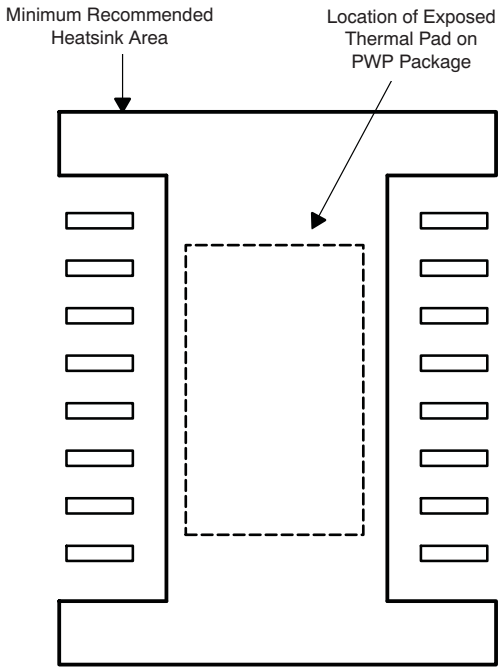


Figure 30. PWP Package Land Pattern

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS75201QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75201
TPS75201QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75201
TPS75201QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75201
TPS75201QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75201
TPS75215QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75215
TPS75215QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75215
TPS75215QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75215
TPS75215QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75215
TPS75218QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75218
TPS75218QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75218
TPS75218QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75218
TPS75218QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75218
TPS75225QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75225
TPS75225QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75225
TPS75225QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75225
TPS75225QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75225
TPS75233QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75233
TPS75233QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75233
TPS75233QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75233
TPS75233QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75233
TPS75401QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75401
TPS75401QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75401
TPS75401QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75401
TPS75401QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75401
TPS75415QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75415
TPS75415QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75415
TPS75418QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75418
TPS75418QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75418
TPS75418QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75418

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS75418QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75418
TPS75418QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75418
TPS75425QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75425
TPS75425QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75425
TPS75425QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75425
TPS75425QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75425
TPS75425QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75425
TPS75433QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75433
TPS75433QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75433
TPS75433QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75433
TPS75433QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT75433

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS752 :

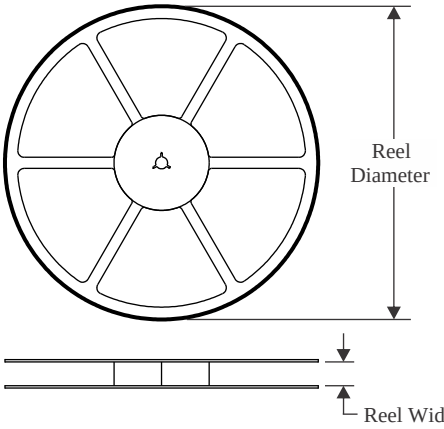
- Automotive : TPS752-Q1

NOTE: Qualified Version Definitions:

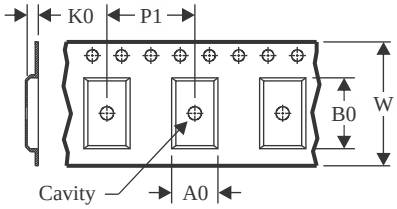
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

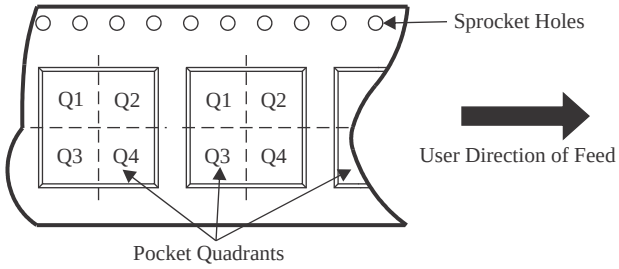


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

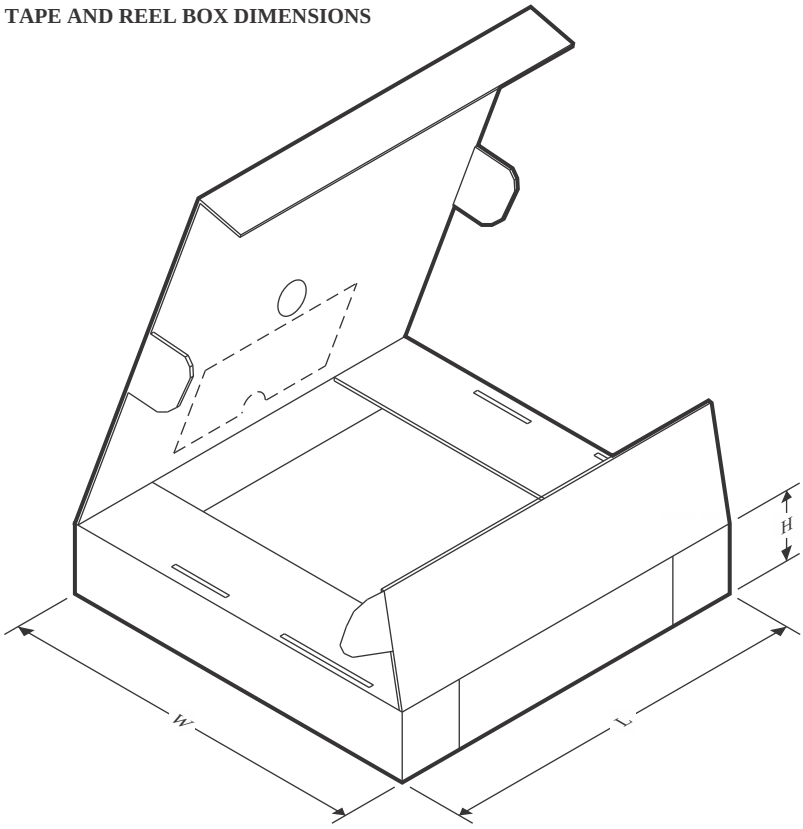
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75201QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75215QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75218QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75225QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75233QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75401QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75418QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75425QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75433QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

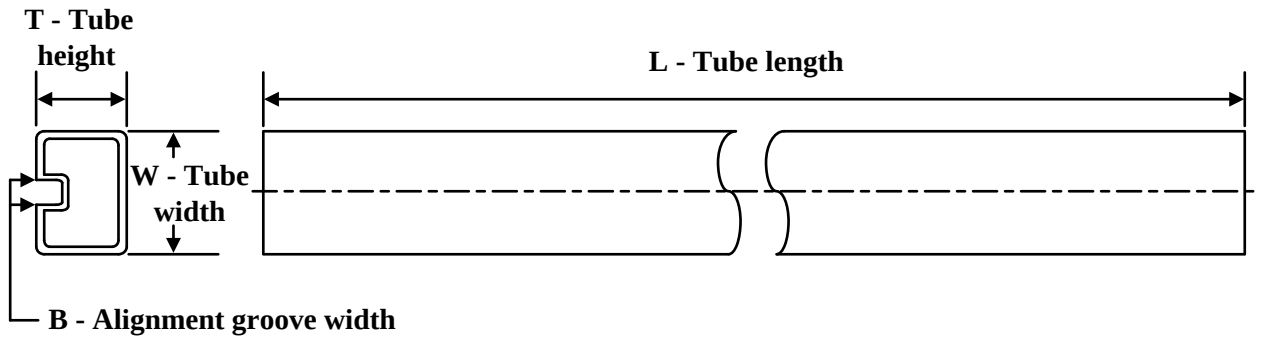
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75201QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75215QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75218QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75225QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75233QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75401QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75418QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75425QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75433QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS75201QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75201QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75215QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75215QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75218QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75218QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75225QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75225QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75233QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75233QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75401QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75401QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75415QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75415QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75418QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75418QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75418QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75425QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75425QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75425QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75433QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS75433QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

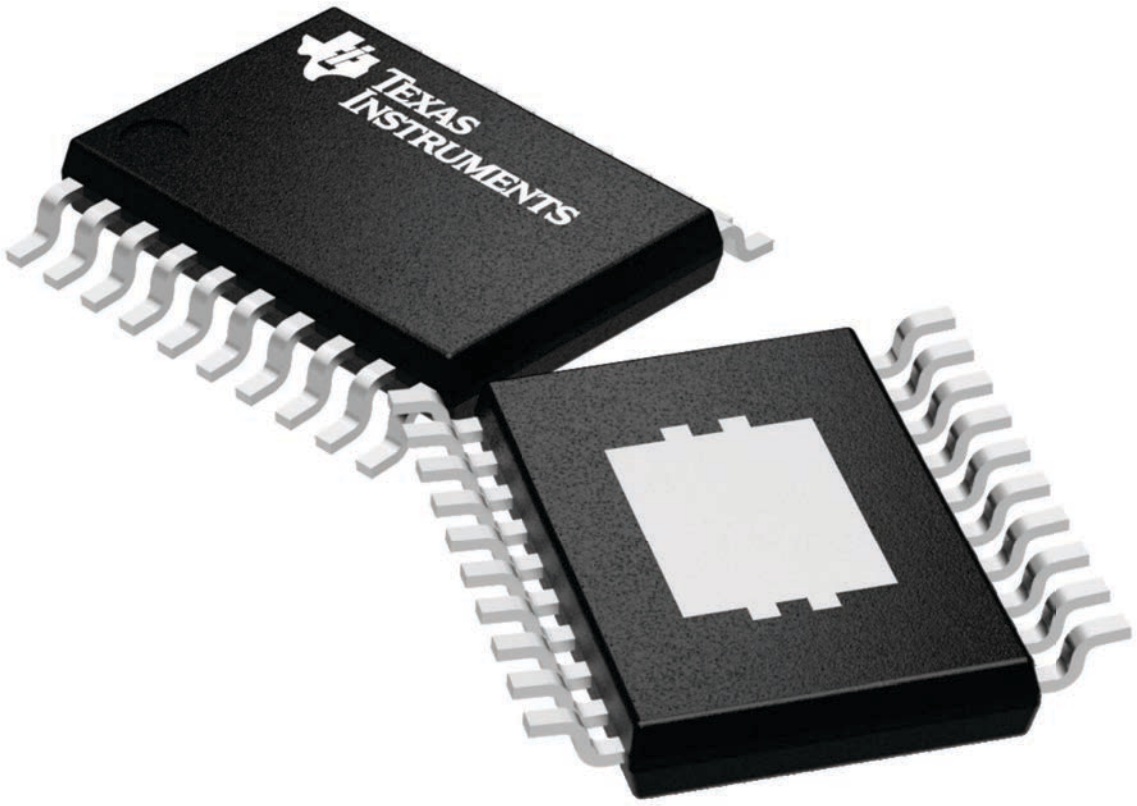
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

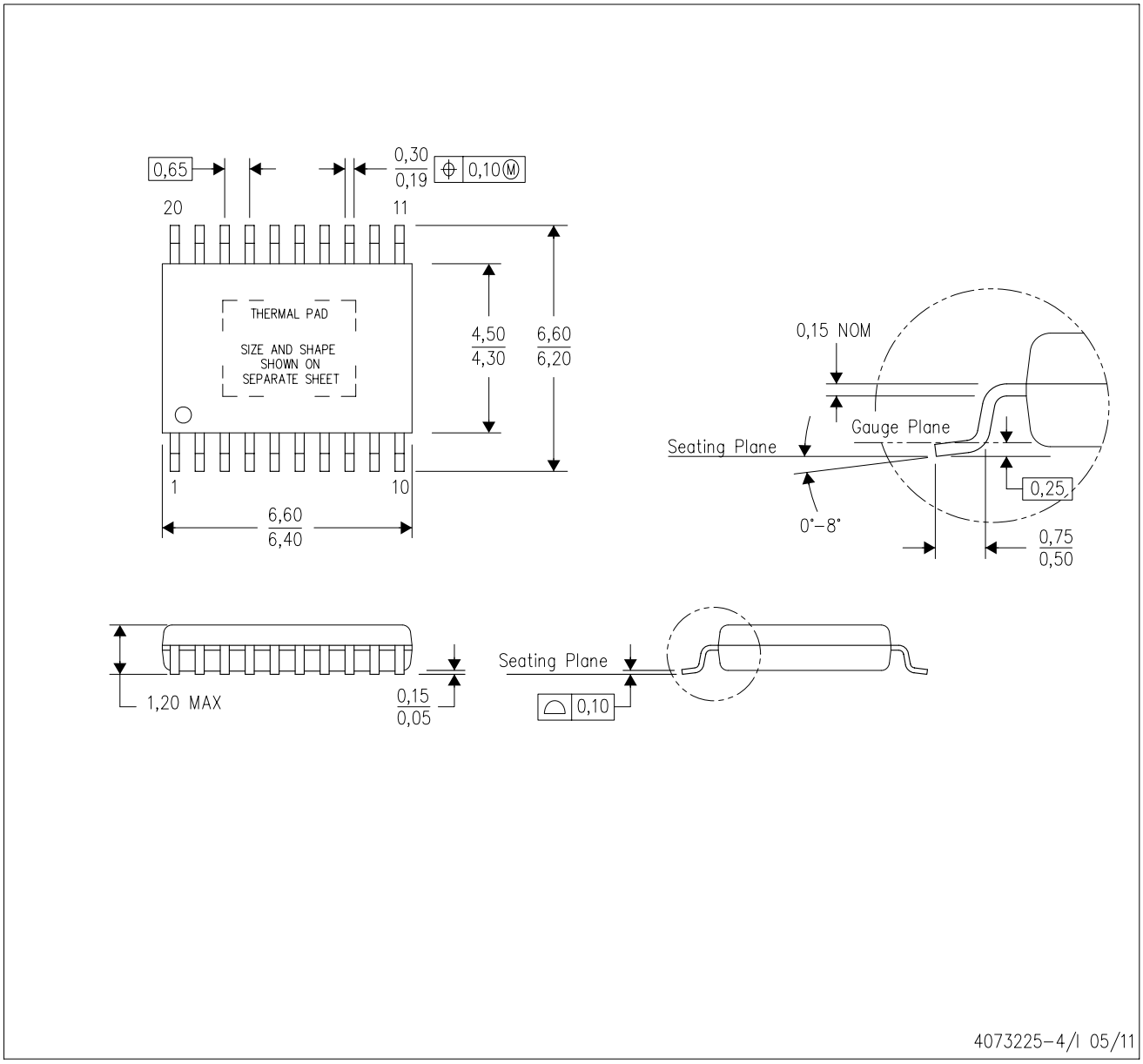
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

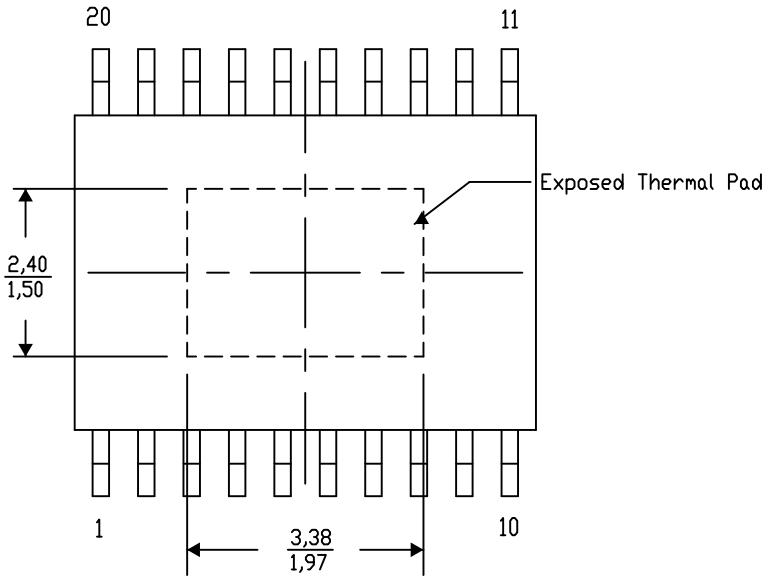
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

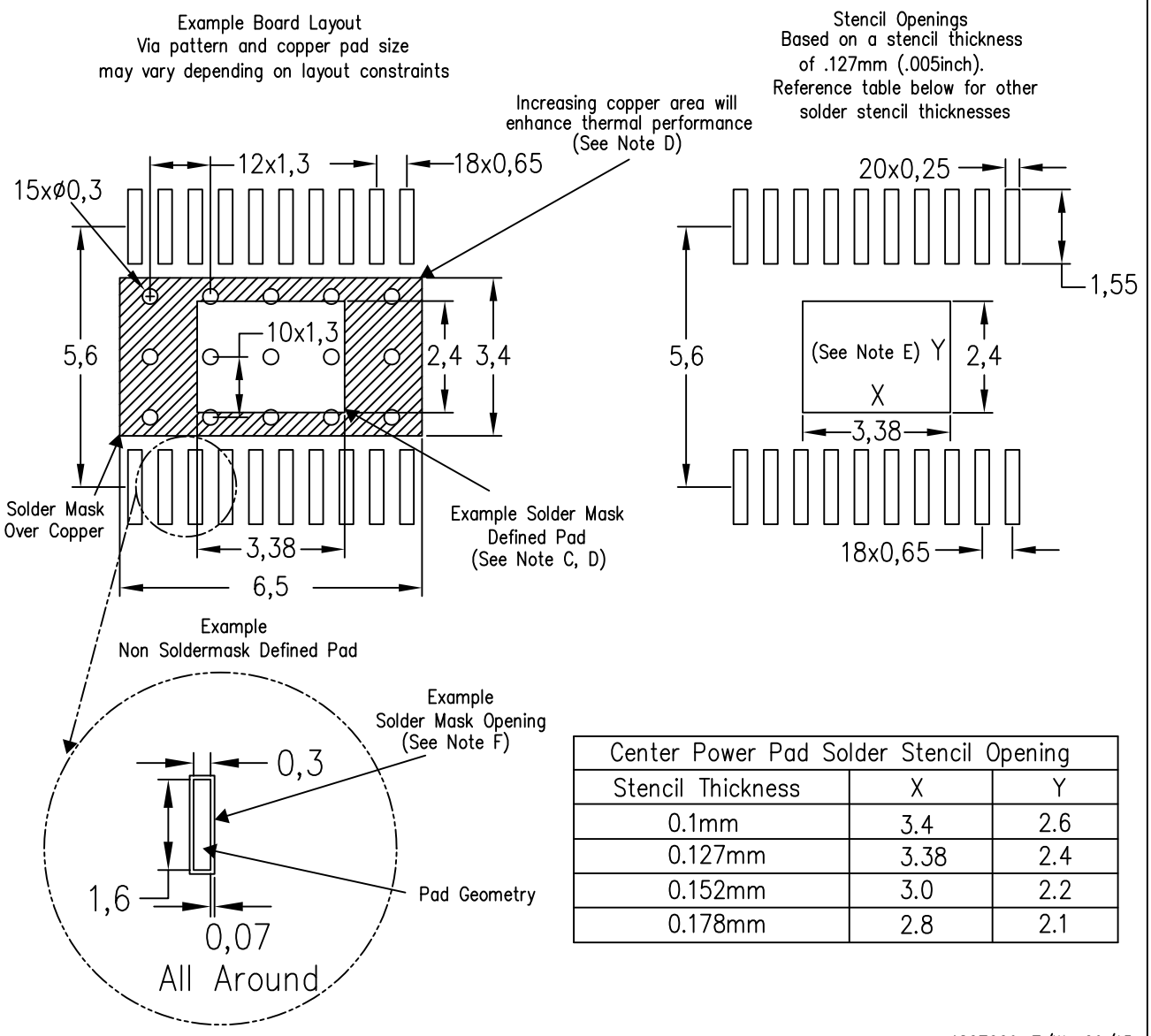
Exposed Thermal Pad Dimensions

4206332–19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609–7/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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